

#### **General Description**

The MAX11043ATL evaluation kit (EV kit) provides a proven design to evaluate the MAX11043 4-channel, 16-bit, simultaneous-sampling ADCs. The EV kit also includes Windows XP®-, Windows Vista®-, and Windows® 7compatible software that provides a simple graphical user interface (GUI) for exercising the features of the IC.

The EV kit is installed with a MAX11043ATL+ in a 40-pin TQFN package with an exposed pad.

#### Ordering Information appears at end of data sheet

#### **Features**

- ♦ 40MHz SPI Interface
- Windows XP-, Windows Vista-, and Windows 7-Compatible Software
- Time Domain and FFT Plotting in the EV Kit Software
- Collects Up to 4 Mega Samples for Each of the 4 Channels
- USB-PC Connection
- Proven PCB Layout
- Fully Assembled and Tested

#### **Component List**

DESIGNATION	QTY	DESCRIPTION
AGND, DGND, TP17	3	Black multipurpose test points
BC5–BC18, BC20–BC29, BC40–BC56	41	0.1µF ±10%, 16V X5R ceramic capacitors (0402) Murata GRM155R61C104K
C1–C8, C18–C21, C49–C54, C69, C71, C73	21	1μF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C105K
C9–C17, C23–C30, C47, C48, C60, C63	21	10µF ±10%, 10V X7R ceramic capacitors (0805) Murata GRM21BR71A106K
C22, C55, C56, C57, C62, C65, C68, C70, C72, C74–C77	13	0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104K
C31–C34	4	2200pF ±10%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H222K
C46	1	100µF ±20%, 6.3V X5R ceramic capacitor (1210) Murata GRM32ER60J107M
C58, C59	2	22pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H220J

DESIGNATION	QTY	DESCRIPTION
C61, C64	2	1000pF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H102K
C66	1	0.47µF ±10%, 10V X5R ceramic capacitor (0603) Murata GRM188R61A474K
C67	1	100pF ±5%, 50V C0G ceramic capacitor (0603) Murata GRM1885C1H101J
CONVRUN, CS, DACSTEP, DIN, DOUT, EOC, SCLK, SHDN, TP14, TP15, UP/DWN	11	Yellow multipurpose test points
D1	1	Hyper-bright, low-current green LED (0603)
D2-D5	4	Hyper-bright, low-current red LEDs (0603)
EXT_AVDD, EXT_DVDD, TP16	3	Red multipurpose test points
FB1, FB2, FB3	3	0.1Ω DCR, 60Ω at 100MHz ferrite beads (0603) TDK MMZ1608R600A

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

#### **Component List (continued)**

DESIGNATION	QTY	DESCRIPTION
J1	1	12-position terminal block
J2	1	6-position terminal block
J3	1	10-pin (2 x 5) dual-row header
J4	1	Mini USB type-AB, right-angle receptacle
J5	1	2-position terminal block
JU1–JU14, JU20–JU27	22	2-pin headers
JU16–JU19	4	3-pin headers
Q1	1	n-channel low-threshold voltage MOSFET (SOT523F)
R1, R2	2	$0.1\Omega \pm 1\%$ , 1/2W sensing resistors (1206)
R3	1	47kΩ ±5% resistor (0603)
R4	1	12.1kΩ ±1% resistor (0603)
R5, R10–R13	5	10k $\Omega$ ±5% resistors (0603)
R6	1	10Ω ±5% resistor (0603)
R7, R8, R9	3	1k $\Omega$ ±5% resistors (0603)
R14, R61–R64	5	$160\Omega \pm 5\%$ resistors (0603)
R15	1	$0\Omega \pm 5\%$ resistor (0805)
R31–R38	8	$22\Omega \pm 5\%$ , 8-element chip resistor networks (0603 x 8)
R39	1	22Ω ±5% resistor (0603)
R40-R54	15	5.1k $\Omega$ ±5% resistors (0603)
R55–R60	6	100k $\Omega$ ±5% resistors (0603)
SW1-SW6	6	Light-touch switches
U1	1	4-channel, 16-bit simultaneous- sampling ADCs (40 TQFN-EP*) Maxim MAX11043ATL+
U2	1	3.3V LDO Maxim MAX1793EUE33+
U3	1	2.5V LDO Maxim MAX1793EUE25+

DESIGNATION	QTY	DESCRIPTION
U4	1	1.8V LDO Maxim MAX1793EUE18+
U5	1	1.2V LDO Maxim MAX1982EUT+
U6	1	2.5V high-precision reference generator (8 SO) Maxim MAX6126AASA25+
U7	1	Cyclone III FPGA (324 FBGA) Altera EP3C25F324C8N
U8	1	Ultra-precision high-side current- sense amplifier (10 µMAX®) Maxim MAX9923HEUB+
U9	1	256K x 36-bit SSRAM (100 TQFP)
U10	1	16M x 16-bit flash memory (64 Easy BGA)
U11	1	Ultra-precision, high-side current-sense amplifier (10 µMAX) Maxim MAX9923FEUB+
U12	1	ULPI Hi-Speed USB 2.0 OTG transceiver (32 HVQFN-EP*)
Y1	1	16MHz crystal Epson MA-505 16.0000M-C0:ROHS
Y2	1	50MHz clock oscillator Hong Kong X'tals C4M50000NSMi02601-0
_	26	Shunts
_	1	PCB: MAX11043 EVALUATION KIT

\*EP = Exposed pad.

#### **Component Suppliers**

SUPPLIER	PHONE	WEBSITE
Altera Corp.	800-800-3753	www.altera.com
Hong Kong X'tals Ltd.	852-35112388	www.hongkongcrystal.com
Murata Electronics North America Inc.	770-436-1300	www.murata-northamerica.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: Indicate that you are using the MAX11043 when contacting these component suppliers.

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#### MAX11043 EV Kit Files

FILE	DESCRIPTION
INSTALL.EXE	Installs the EV kit files on your computer
MAX11043EVKIT.EXE	Application program
UNINSTALL.EXE	Uninstalls the EV kit software
SLS_USB_Driver_Help_200.PDF	USB driver installation help file

#### **Quick Start**

#### **Required Equipment**

- MAX11043 EV kit
- Windows XP, Windows Vista, or Windows 7 PC with a spare USB port
- Function generator

**Note:** In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and under-lined** refers to items from the Windows operating system.

#### Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

- Visit <u>www.maxim-ic.com/evkitsoftware</u> to download the latest version of the EV kit software, 11043Rxx.ZIP. Save the EV kit software to a temporary folder and uncompress the ZIP file.
- 2) Install the EV kit software and USB driver on your computer by running the INSTALL.EXE program inside the temporary folder. The program files are copied to your PC and icons are created in the Windows <u>Start I Programs</u> menu. During software installation, some versions of Windows may show a warning message indicating that this software

is from an unknown publisher. This is not an error condition and it is safe to proceed with installation. Administrator privileges are required to install the USB device driver on Windows.

- 3) Verify that the jumpers on the EV kit board are in their default positions, as shown in Table 1. The jumper locations are shown in Figure 1.
- 4) Set the signal source to generate a 1kHz, 2.0V peakto-peak sinusoidal wave with 0V offset.
- 5) Connect the positive terminal of the signal generator to the AINAP terminal block connector. Connect the negative terminal of the signal generator to the AINAN terminal block connector.
- 6) Connect the USB cable from the PC to the EV kit board. Follow the instructions on the SLS\_USB\_ Driver\_Help\_200.PDF file to manually install the USB driver. Administrator privileges are required to install the USB device driver on Windows.
- 7) Enable the function generator.
- Start the EV kit software by opening its icon in the Windows <u>All Programs</u> menu. The EV kit software main window appears, as shown in Figure 2.
- 9) The main window should display **Hardware Connected** on the status bar.
- 10) Check channel **A** in the **Automatic ADC result output** group box.
- Navigate to the ADC Configuration and Gain tab shown in Figure 5. In the ADC\_A (0Ch) group box, set PGA gain to 1, programmable filter to LP, and then press the Write button.
- 12) Navigate to the **Data Acquisition** tab (Figure 4). Click on the **Number of Samples Requested** dropdown list and select **8192**.
- 13) Press the **Start Conversion** button.
- 14) Verify that the waveform displayed in the GUI FFT graph is approximately 1000Hz, as shown in Figure 3.



Figure 1. MAX11043 EV Kit Jumper Locations





Figure 2. MAX11043 EV Kit Software (Main Window)





Figure 3. MAX11043 EV Kit Software (Quick Start Data Sampling Graph)

#### **Detailed Description of Software**

The main window of the evaluation software (Figure 2) displays the MAX11043 device status register, device configuration register, digital filter purge interval and reference register, and five tab sheets.

**Device Status (07h) Group Box** 

Press the **Read** button in this group box to read the status of the IC.

**Device Configuration (08h) Group Box** This group box displays the configuration register. Press the **Read** button in the group box to read the register. To write new values to the register, first select the desired configuration, and then press the **Write** button.

#### Digital Filter Purge Interval & References (10h) Group Box

This group box displays the digital purge interval and reference configuration register. Press the **Read** button in the group box to read the register. To write new values to the register, first select the desired configuration, and then press the **Write** button.

If internal references are used, the user should measure the real reference values and type in the measured values in the respective edit box and press Enter to update the reference values. Otherwise, the nominal values are used.

If external references are used, apply the external references on the respective terminal block connectors.

#### Configure SHDN Pin and Configure CONVRUN Pin Group Boxes

These two group boxes are used to set or clear the SHDN or CONVRUN pins on the IC.

#### **Data Acquisition Tab**

On the **Data Acquisition** tab sheet (Figure 4), the user can select the desired number of conversions in the **Number of Samples Requested** drop-down list. The sampling

rate is also displayed. Press the **Start Conversion** button to start sampling. After sampling is finished, the user can save the data to a file by pressing the **Save Data to File...** button.

After the **Start Conversion** button is pressed, the sampled data in the time domain is plotted in the **Scope** window. The user can select the scope window in either counts or in calculated voltages. The sampled data in the frequency domain is plotted in the **FFT** window. The user can select the FFT calculation based on the maximum ADC resolution (16-bit or 24-bit) by clicking on the **Peak** radio button, or the FFT calculation based on maximum input value by clicking on the **Input Range** radio button.

#### **ADC Configuration and Gain Tab**

On the **ADC Configuration and Gain** tab sheet, all ADC configuration registers and fine gain registers are displayed, as shown in Figure 5.

#### **DAC Registers Tab**

On the **DAC Registers** tab sheet, the fine DAC register, the DAC step register, and the coarse DAC registers are displayed, as shown in Figure 6.

The UP/ $\overline{\text{DWN}}$  and DACSTEP pin functions are also provided.

#### **C-RAM and Flash Tab**

As shown in Figure 7, this tab sheet provides the functions of C-RAM and flash operations.

**Important Note:** Save the content of the flash to a file in case they are needed later.

#### **Direct Register Access Tab**

The controls on this tab sheet (Figure 8) are provided for low-level device debugging purposes. The user can manually send read and write commands to each register on the IC.



Figure 4. MAX11043 EV Kit Software Main Window (Data Acquisition Tab)

		ect Register Access	Positive input bias enable	Include the input bias enable	Input Mode	€ 2x input C Normal PGA Gain	Modulator Gain © 1 0 2 0 4	Analog EQ	Programmable Filter	Read	x desired gain).		Read		Read	Read		Head	Scan Mode: Yes
		isters   C-RAM & Flash   Dire	Positive input bias enable	Inequative input plas enable	Input Mode	● 2x input ○ Normal PGA Gain	Modulator Gain	Analog EQ © Disabled © Enabled	Programmable Filter © EQ C LP	Read	nent binary value (8192	Gain	7FFF 1.000000		7FFF 1.000000	7FFF 1.000000		7FFF 1.000000	
		figuration & Gain DAC Regindant	Positive input bias enable	Inegative input plas enable	Input Mode	C 2x input C Normal PGA Gain	Modulator Gain	Analog EQ	Programmable Filter	Read	unnel is a two's complen Range is -4 to 4-1/8192.	Fine Gain Register 0x 2000	<b>0</b>	0x 2000		0× 2000	0x 2000		Data Aquisition: Success
		Data Acquisition ADC Cor ADC A (IICh)	Positive input bias enable	Incut hise: Ener and a shape	Input Mode	C 2x input C Normal PGA Gain	Modulator Gain © 1 C 2 C 4	Analog EQ	Programmable Filter	Read	Fine gain for each chí Resolution is 16 bits.		ADC_A (11h): 0x8000		ADC_B (12h) 0x8000	ADC_C (13h) 0x8000		ADC_D (14h) 0x8000	Version: 09
		00T No Read	FLGC No OFLGD No		xternal (38.4MHz)	.4 @ 1:6	🗖 ADC_B power-down	C ADC_D power-down	utomatic ADC result output	C Decimate by 12	& References (10h)	ADC_A reference • Internal 2,500000 V	C External 2.50000 V ADC_C reference	<ul> <li>Internal <u>2.500000</u> V</li> <li>C External <u>2.500000</u> V</li> </ul>	Coarse DAC reference internal 1.250000 V C External 1.250000 V	Fine DAC low reference C Internal 0.000000 V C External 0.000000 V	pective terminals, then type in the senter to update the references.	Configure CONVRUN Pin © 0 0 1	EV Kit Board Firmware
XX11043 Evaluation Kit	Help	svice Status (07h) Ish Busy No B	LGA No OFLGB No O	vice Configuration (08h)	lock Source Selection	lock Divide Ratio 1:2 C 1:3 C 1:	Power-down analog circuitry ADC_A power-down	ADC_C power-down Fine DAC power-down	DC output data format A © 16 bits C 24 bits ि	ecimate Selection Cocimate by 24	gital Filter Purge Interval lital Filter Purge Interval: 0	ain reference Internal 2.500000 V	External 2.500000 V DC_B reference	Internal 2.500000 V External 2.500000 V	DC_D reference Internal 2:500000 V External 2:500000 V	ine DAC high reference Internal 0.000000 V External 0.000000 V	asure the voltages at the rest ASURED voltages and press	nfigure SHDN Pin 0 C 1	dware: Connected

Figure 5. MAX11043 EV Kit Software Main Window (ADC Configuration & Gain Tab)

tion Kit	Data Acquisition     ADC Configuration       B00T     No     Read       No     0FLGC     No       Fine DAC Register (03h):     0;	on (08h) C External (38.4MHz) C 1:4 © 1:5 DAC Step Register (0Ah): 0:	g circuity m C ADC_B power-down m ADC_D power-down the ADC_D power-down the ADC_D power-down the ADC result output the ADC B power-down the ADC B POWER B POW	C Decimate by 12	rvat 0 - Read Write 0 V C External 2.500000 V 0 V C External 2.500000 V 0 V C External 2.500000 V 0 0 0 1	ADC_C reference	at the respective terminals, then type in the and press enter to update the references.
1	& Gain       DAC Registers       C-RAM & Flash       Direct Register Act         0x 000       2x Fine DAC Voltage (AOUT)         0       0x 00000       V         0       0x FFF       0.000000       V	0 0x 000 DAC Step Voltage 0.00000 V Read	0 0 0x 00 DACH Voltage 0.000000 V Read 0x 00 DACL Voltage	0 0 00000 V These are TARGET voltages.	Apply one pulse on the DACSTEP pin		

Figure 6. MAX11043 EV Kit Software Main Window (DAC Registers Tab)



		C Registers C-RAM & Flash Direct Register Access	Load File to C-RAM	Load File to Flash	Load C-RAM to Flash Page 2 & 3	Load C-RAM to Flash Page 6 & 7	Load Flash Page 2 & 3 to C-RAM	Load Flash Page 5 & 7 to C-HAM	<ul> <li>Address 0x 00 Data 0x ????</li> <li>Address 0x 00 Data 0x ????</li> </ul>	Cress Moder Vec
		Data Acquisition ADC Configuration & Gain DA	Load C-RAM to File	Load Flash to File	Load C-RAM to Flash Page 0 & 1	Load C-RAM to Flash Page 4 & 5	Load Flash Page 0 & 1 to C-RAM	Load Flash Page 4 & 5 to C-HAM	Flash Single Word Read     Page 0       Flash Single Word Write     Page 0       Flash Single Page Erase     Page 0       Flash Mass Erase     Page 0	Version: 09 Data Aquisition: Suc
Gt		BOOT No Read	OFLGC No OFLGD No	8h) Read C External (38.4MHz)	1:4 @ 1:6	uitry	Automatic ADC result output Automatic ADC result output	C Decimate by 12	val & References (10h)       with the second of the second	FV Kit Board Firmware
AX11043 Evaluation K	Help	vice Status (07h) sh Busv No	GA No OFLGB No	vice Configuration (0. lock Source Selection Crystal (16MHz) C	lock Divide Ratio 0 1:2 C 1:3 C	Power-down analog circ. ADC_A power-down ADC_C power-down Eine DAC power-down	DC output data format 16 bits C 24 bits ecimate Selection	Decimate by 24	gital Filter Purge Interval: [ itial Filter Purge Interval: [ lain reference Internal 2.500000 V External 2.500000 V	rdware: Connected

Figure 7. MAX11043 EV Kit Software Main Window (C-RAM & Flash Tab)



2			_			
dia <u>L</u>						
evice Status (07h) ash Busy No B	00T No Read	Data Acquisition ADC	Configuration &	Gain DAC Re	gisters C-RAM & Flash	Direct Register Access
FLGA No OFLGB No C	FLGC No OFLGD No	Register:			ength (Bits):	
evice Configuration (08h	-	07h Status		F	8	
Clock Source Selection	xternal (38.4MHz)					
Clock Divide Ratio	4 © 1.6	Write 0x	00000000	0000000	0000000	
Power-down analog circuitry						
ADC_A power-down ADC_C power-down	C ADC_B power-down	Read 0x	00000000	00000000	0000000	
Fine DAC power-down	C 0scillator power-down					
ADC output data format	utomatic ADC result output					
Contraction Contraction						
<ul> <li>Decimate by 24</li> </ul>	O Decimate by 12					
igital Filter Purge Interva	l & References (10h)					
gital Filter Purge Interval: 0	Read     Write					
Main reference	ADC_A reference					
i Internal 2.500000 V External 2.500000 V	<ul> <li>Internal 2.500000 V</li> <li>External 2.500000 V</li> </ul>					
ADC_B reference	ADC_C reference					
External 2.500000 V	<ul> <li>Internal 2.500000 V</li> <li>External 2.500000 V</li> </ul>					
ADF D reference	foarse D&C reference					
Thermal 2.500000 V External 2.500000 V	C External 1.250000 V					
Fine DAC high reference	Fine DAC low reference					
Finternal 0.000000 V External 0.000000 V	<ul> <li>Internal 0.000000 V</li> <li>External 0.000000 V</li> </ul>					
easure the voltages at the res	pective terminals, then type in the					
EASUMEN voltages and pres	s enter to update the references.					
onfigure SHDN Pin 0 0 1	Configure CONVRUN Pin © 0 0 1					
rdware: Connected	EV Kit Board Firmware	Version: 09	Data Aqu	uisition: Success		Scan Mode: Yes

Figure 8. MAX11043 EV Kit Software Main Window (Direct Register Access Tab)

#### **Detailed Description of Hardware**

The MAX11043ATL EV kit is a fully assembled and tested PCB that evaluates the MAX11043 4-channel, 16-bit, simultaneous-sampling ADCs with PGA, filter, and an 8-/12-bit dual-stage DAC.

The EV kit is installed with a MAX11043ATL+ in a 40-pin TQFN package with an exposed pad. An on-board +2.5V voltage reference (MAX6126) is provided. Contact Maxim for other high-precision voltage references if reference voltages other than +2.5V are required.

#### User-Supplied SPI Interface and GPIO Controls

For a user-supplied control interface, first remove the shunts on jumpers JU5–JU13 and connect the user-supplied control signals to the corresponding SHDN, EOC, SCLK, DIN, DOUT, CS, CONVRUN, DACSTEP, UP/DWN test points on the EV kit.

#### Table 1. Jumper Descriptions (JU1–JU14, JU16–JU27)

JUMPER	SHUNT POSITION	DESCRIPTION
	1-2	Channel A is configured for single-ended input operation.
JUT	Pin 1*	Channel A is configured for differential input operation.
	1-2	Channel B is configured for single-ended input operation.
JU2	Pin 1*	Channel B is configured for differential input operation.
	1-2	Channel C is configured for single-ended input operation.
103	Pin 1*	Channel C is configured for differential input operation.
11.1.4	1-2	Channel D is configured for single-ended input operation.
504	Pin 1*	Channel D is configured for differential input operation.
11.15	1-2*	Use the on-board UP/DOWN control.
105	Pin 1	Use the user-supplied UP/DOWN control.
1116	1-2*	Use the on-board DACSTEP control.
100	Pin 1	Use the user-supplied DACSTEP control.
11.17	1-2*	Use the on-board CONVRUN control.
507	Pin 1	Use the user-supplied CONVRUN control.
11.10	1-2*	Use the on-board CS control.
508	Pin 1	Use the user-supplied CS control.
11.10	1-2*	Use the on-board DOUT control.
109	Pin 1	Use the user-supplied DOUT control.
11.110	1-2*	Use the on-board DIN control.
3010	Pin 1	Use the user-supplied DIN control.
11.14.4	1-2*	Use the on-board SCLK control.
5011	Pin 1	Use the user-supplied SCLK control.
1112	1-2*	Use the on-board EOC control.
JU12	Pin 1	Use the user-supplied EOC control.
1112	1-2*	Use the on-board SHDN control.
5015	Pin 1	Use the user-supplied SHDN control.
11.11.4	1-2	Use the on-board 2.5V as REFBP.
5014	Pin 1*	Use the internal REFBP.
1116	1-2	FPGA generated 38.4MHz clock connected to the OSCIN pin.
5010	2-3*	On-board 16MHz crystal connected to the OSCIN pin.
1117	1-2*	AVDD is connected to the on-board 3.3V DC.
JU17	2-3	AVDD is connected to the user-supplied power supply.
11119	1-2*	DVDD is connected to the on-board 3.3V DC.
JUIO	2-3	DVDD is connected to the user-supplied power supply.

#### Table 1. Jumper Descriptions (JU1–JU14, JU16–JU27) (continued)

JUMPER	SHUNT POSITION	DESCRIPTION
11.110	1-2*	The board is powered by the USB.
3019	2-3	The board is powered by the user-supplied 5V DC.
11.120	1-2	AINAP connected to the signal source directly.
JU20	Pin 1*	AINAP coupled to the signal source through a 10µF capacitor.
11.10.1	1-2	AINAN connected to the signal source directly.
JUZI	Pin 1*	AINAN coupled to the signal source through a 10µF capacitor.
11.100	1-2	AINBP connected to the signal source directly.
JU22	Pin 1*	AINBP coupled to the signal source through a 10µF capacitor.
11.100	1-2	AINBN connected to the signal source directly.
JU23	Pin 1*	AINBN coupled to the signal source through a 10µF capacitor.
11.10.4	1-2	AINCP connected to the signal source directly.
JU24	Pin 1*	AINCP coupled to the signal source through a 10µF capacitor.
11.105	1-2	AINCN connected to the signal source directly.
0020	Pin 1*	AINCN coupled to the signal source through a 10µF capacitor.
11.106	1-2	AINDP connected to the signal source directly.
JU20	Pin 1*	AINDP coupled to the signal source through a 10µF capacitor.
11 107	1-2	AINDN connected to the signal source directly.
JUZI	Pin 1*	AINDN coupled to the signal source through a 10µF capacitor.

\*Default position.



Figure 9a. MAX11043 EV Kit Schematic (Sheet 1 of 10)



Figure 9b. MAX11043 EV Kit Schematic (Sheet 2 of 10)





Figure 9c. MAX11043 EV Kit Schematic (Sheet 3 of 10)







Figure 9e. MAX11043 EV Kit Schematic (Sheet 5 of 10)



Figure 9f. MAX11043 EV Kit Schematic (Sheet 6 of 10)





Figure 9g. MAX11043 EV Kit Schematic (Sheet 7 of 10)





Figure 9h. MAX11043 EV Kit Schematic (Sheet 8 of 10)



Figure 9i. MAX11043 EV Kit Schematic (Sheet 9 of 10)





Figure 9j. MAX11043 EV Kit Schematic (Sheet 10 of 10)





Figure 10. MAX11043 EV Kit Component Placement Guide—Component Side



Figure 11. MAX11043 EV Kit Component Placement Guide—Solder Side



Figure 12. MAX1104311043 EV Kit PCB Layout—Component Side



Figure 13. MAX11043 EV Kit PCB Layout—Ground Layer 2



Figure 14. MAX11043 EV Kit PCB Layout—Signal Layer 3



Figure 15. MAX11043 EV Kit PCB Layout—Ground Layer 4



Figure 16. MAX11043 EV Kit PCB Layout—Power Layer 5



Figure 17. MAX11043 EV Kit PCB Layout—Signal Layer 6



Figure 18. MAX11043 EV Kit PCB Layout—Ground Layer 7



Figure 19. MAX11043 EV Kit PCB Layout—Ground Layer 8



Figure 20. MAX11043 EV Kit PCB Layout—Signal Layer 9



Figure 21. MAX11043 EV Kit PCB Layout—Solder Side

#### **Ordering Information**

PART	TYPE
MAX11043ATLEVKIT#	EV Kit

#Denotes RoHS compliant.

#### **Revision History**

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	5/12	Initial release	

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;

- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком):

- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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