



PMV65XP

20 V, single P-channel Trench MOSFET

12 February 2013

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Low on-state resistance
- Trench MOSFET technology

3. Applications

- Low power DC-to-DC converters
- Load switching
- Battery management
- Battery powered portable equipment

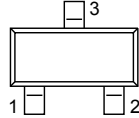
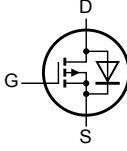
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	-	-4.3	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2.8\text{ A}; T_j = 25\text{ °C}$		-	58	74	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-236AB (SOT23)	 017aaa257
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV65XP	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code [1]
PMV65XP	%M9

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-20	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ }^{\circ}\text{C}$		-	-4.3	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-2.8	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-1.8	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-16	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	480	mW
			[1]	-	833	mW
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	4165	mW

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{sp} = 25 °C		-	-1.6	A

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

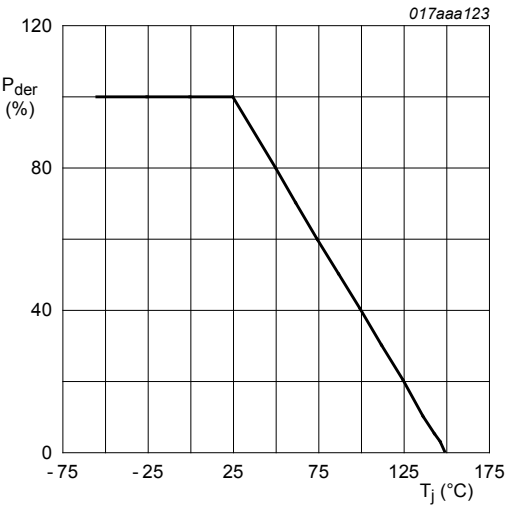


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

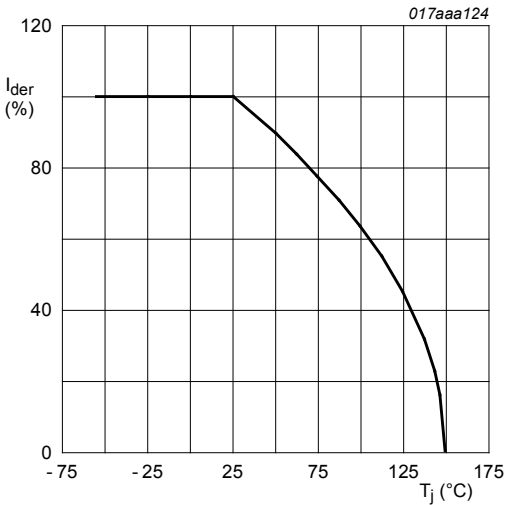
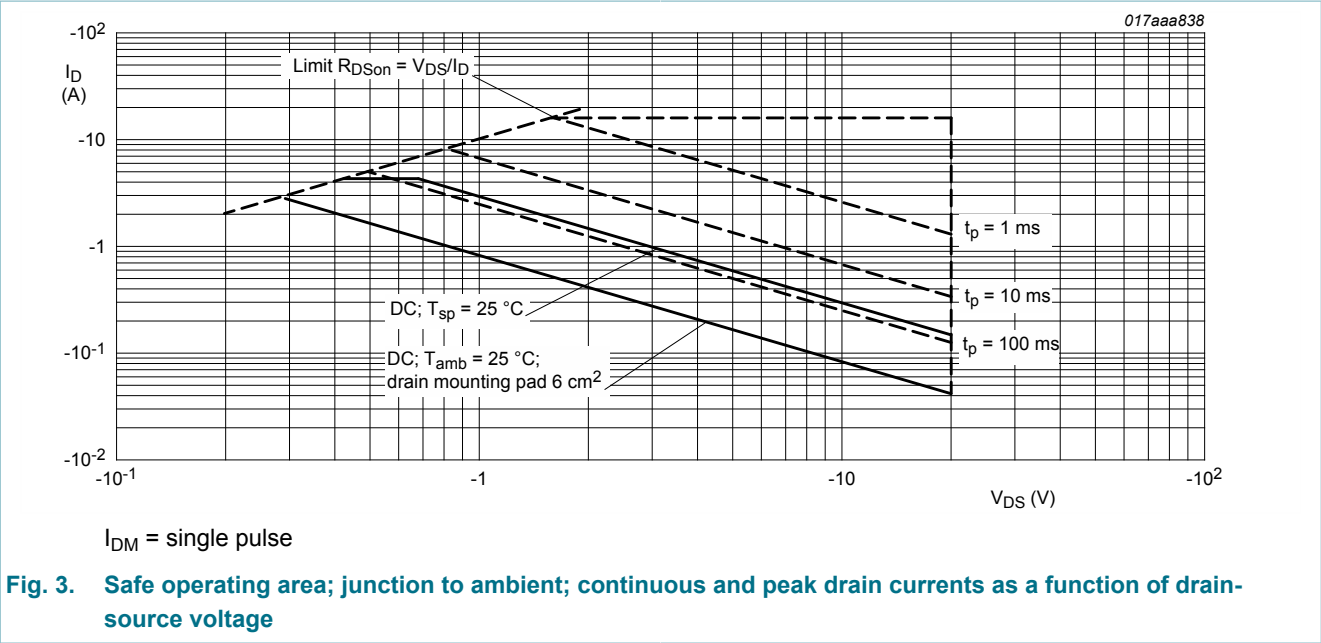


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

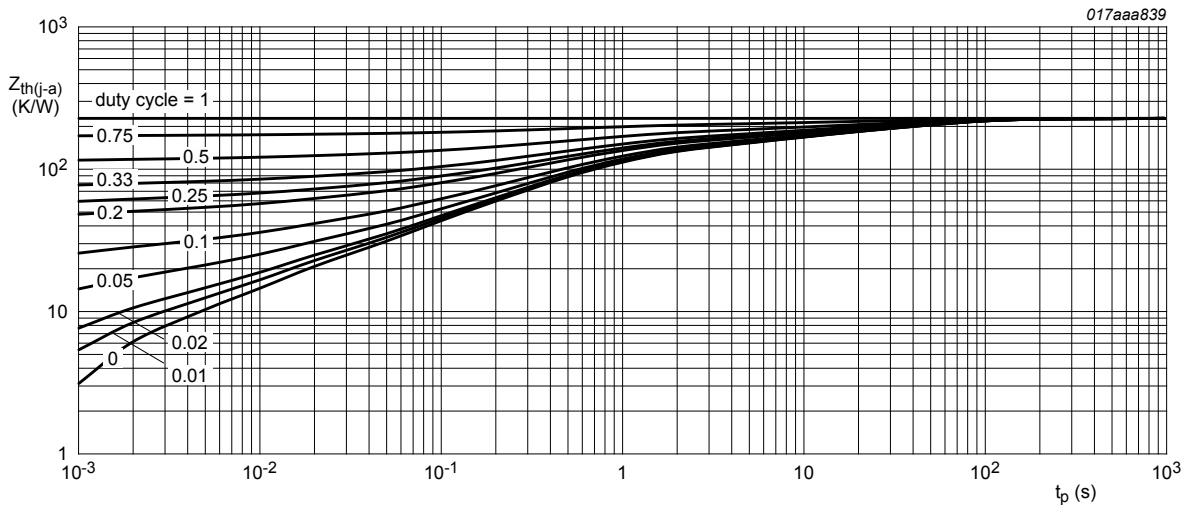


9. Thermal characteristics

Table 6. Thermal characteristics

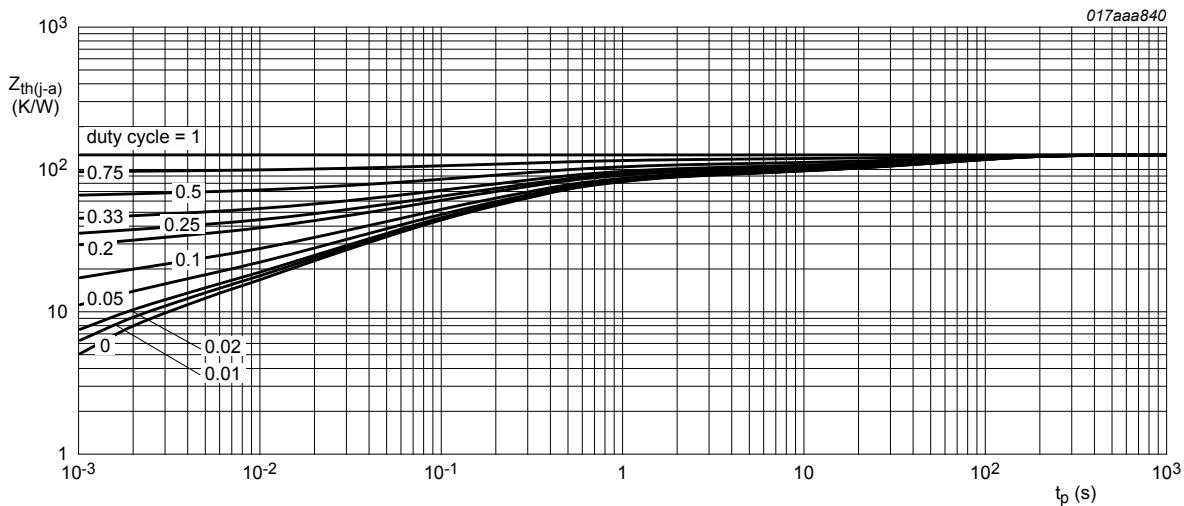
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	230	260	K/W
			[2]	-	125	150	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	25	30	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$	-0.47	-0.65	-0.9	V
I_{DSS}	drain leakage current	$V_{DS} = -20\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$	-	-	-100	μA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -2.8 A; T _j = 25 °C		-	58	74	mΩ
		V _{GS} = -4.5 V; I _D = -2.8 A; T _j = 150 °C		-	82	105	mΩ
		V _{GS} = -2.5 V; I _D = -2.3 A; T _j = 25 °C		-	67	92	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C		-	87	135	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -2.8 A; T _j = 25 °C		-	15	-	S
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -6 V; I _D = -2.8 A; V _{GS} = -4.5 V; T _j = 25 °C		-	7.7	-	nC
Q _{GS}	gate-source charge			-	1	-	nC
Q _{GD}	gate-drain charge			-	1.65	-	nC
C _{iss}	input capacitance	V _{DS} = -20 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	744	-	pF
C _{oss}	output capacitance			-	65	-	pF
C _{rss}	reverse transfer capacitance			-	53	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -6 V; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C; I _D = -1 A		-	7	-	ns
t _r	rise time			-	18	-	ns
t _{d(off)}	turn-off delay time			-	135	-	ns
t _f	fall time			-	68	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -0.9 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V

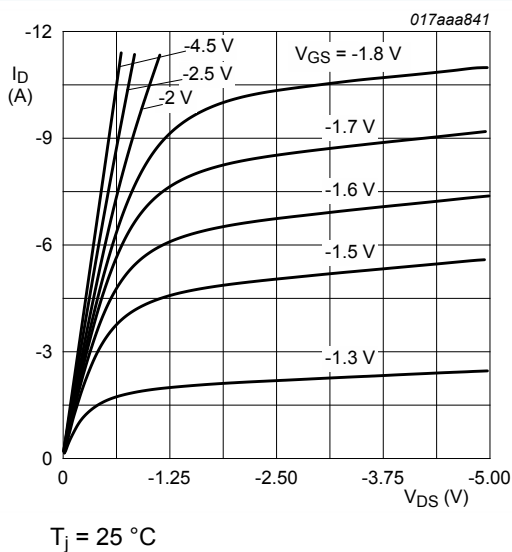


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

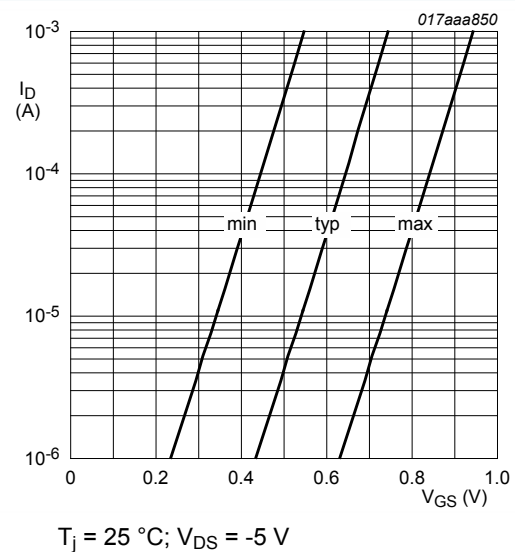


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

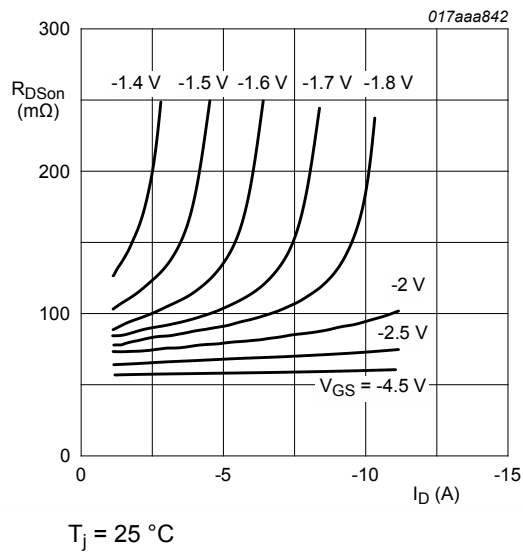


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

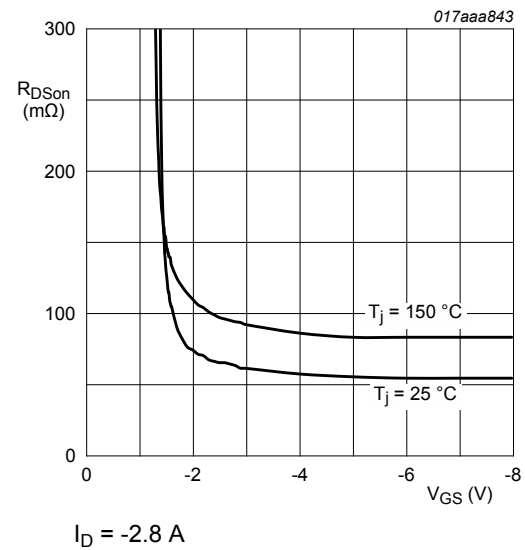


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

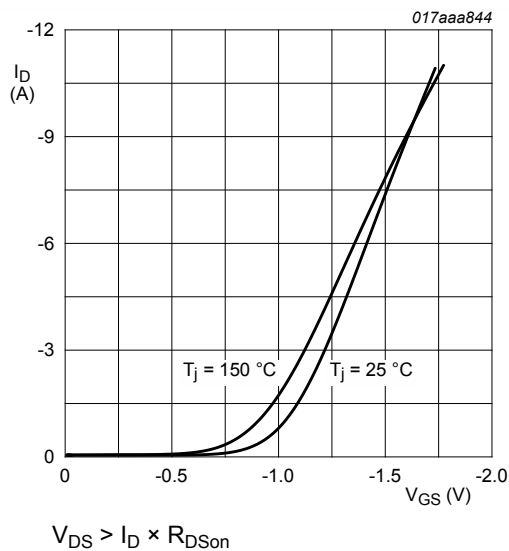


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

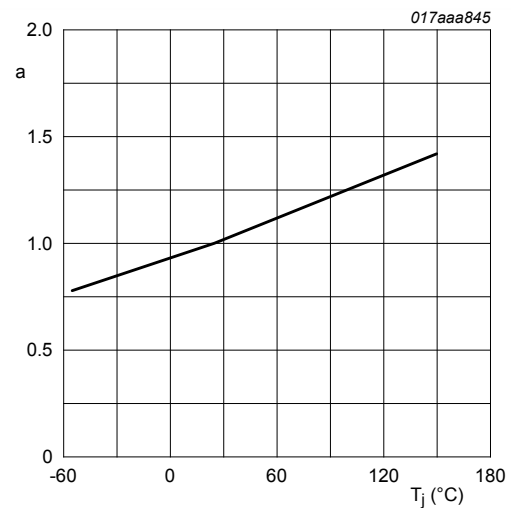


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

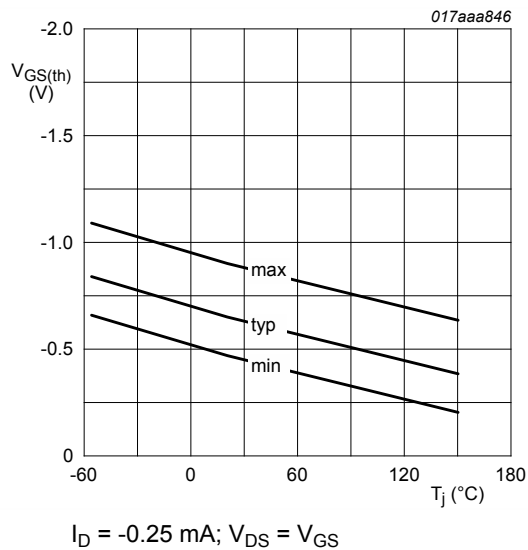


Fig. 12. Gate-source threshold voltage as a function of junction temperature

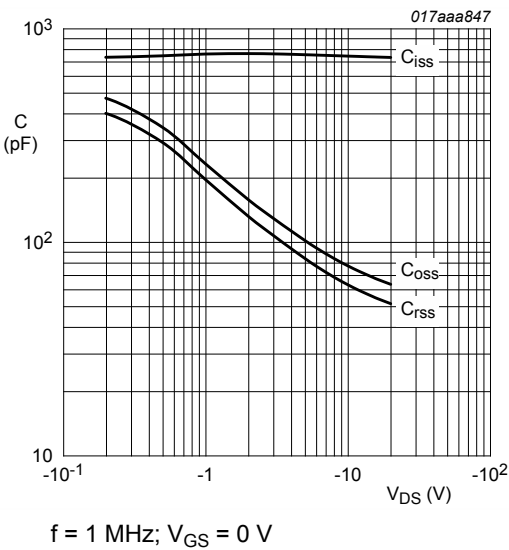


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

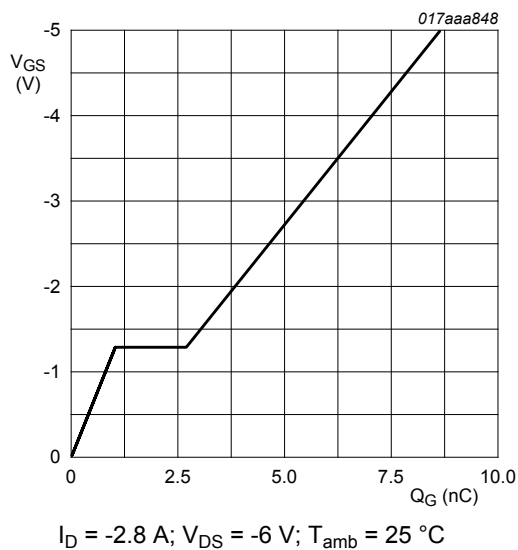


Fig. 14. Gate-source voltage as a function of gate charge; typical values

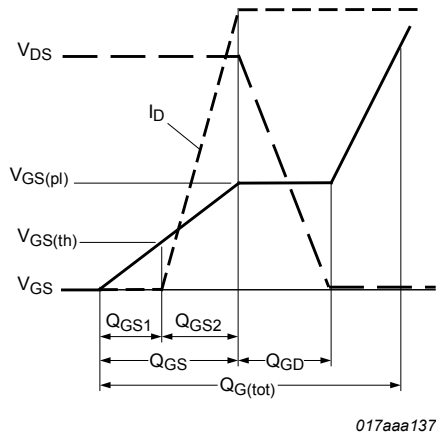
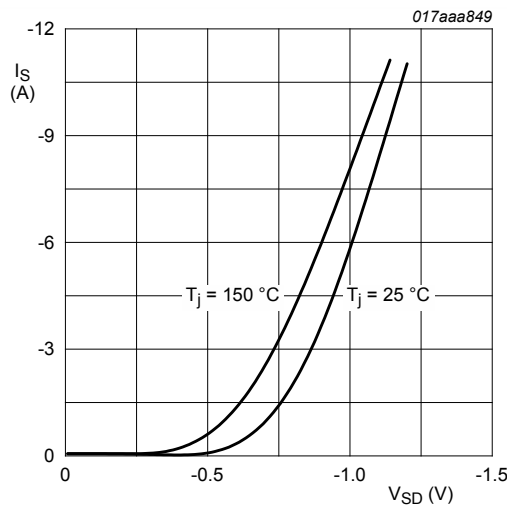


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$
(1) $T_j = 150\text{ }^{\circ}\text{C}$
(2) $T_j = 25\text{ }^{\circ}\text{C}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

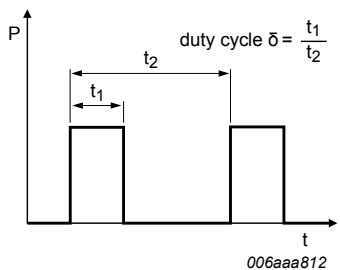
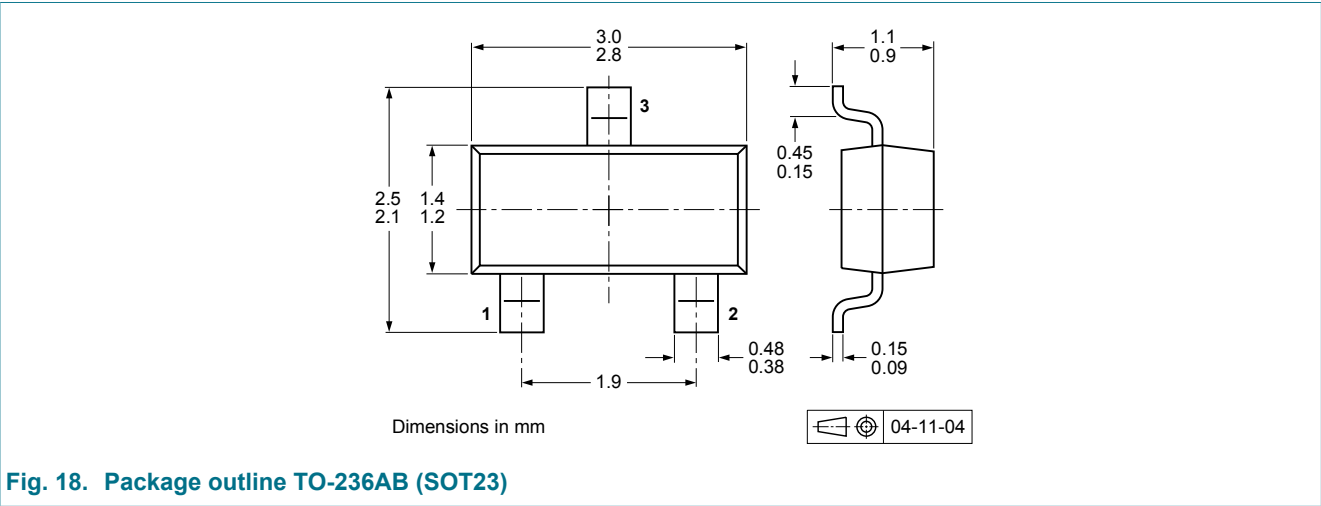
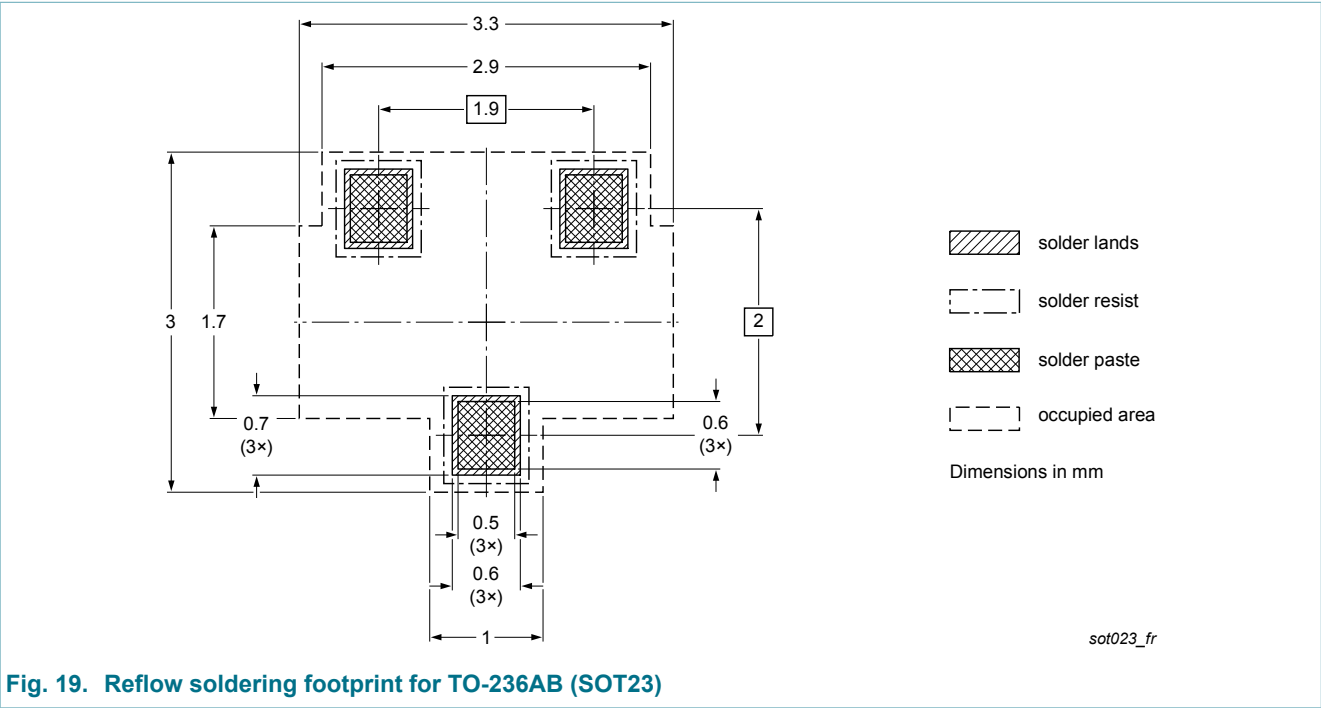


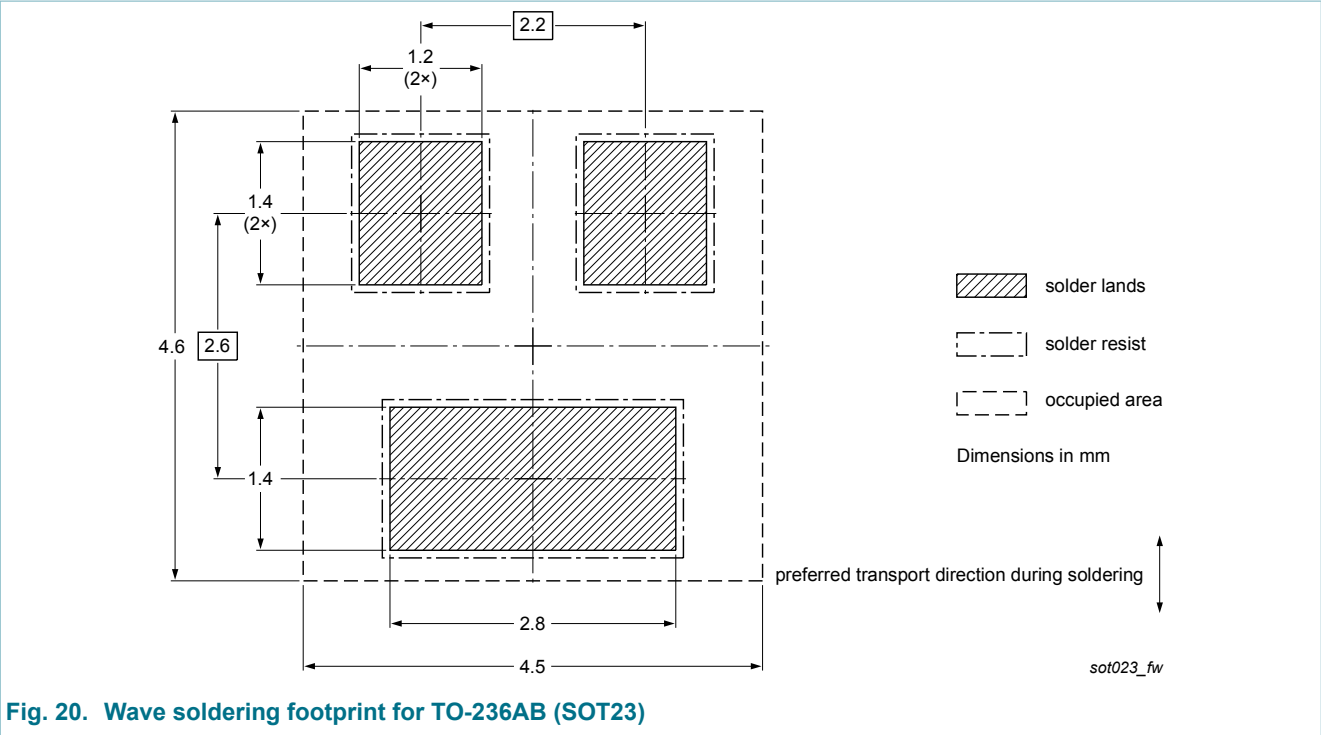
Fig. 17. Duty cycle definition

12. Package outline



13. Soldering





14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV65XP v.2	20130212	Product data sheet	-	PMV65XP v.1
Modifications:	• Pinning information corrected			
PMV65XP v.1	20120921	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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