

The mini analog series is a group of ICs that incorporate a general-purpose analog circuit in an ultra-small package.

The S-89530A/89531A Series are CMOS type comparators that feature Rail-to-Rail^{*1} I/O and can be driven at a lower voltage and lower current consumption than existing comparators, making the S-89530A/89531A for use in battery-powered compact portable devices.

*1. Rail-to-Rail is a registered trademark of Motorola Inc.

■ Features

- Can be driven lower voltage than existing general-purpose comparators: $V_{DD} = 0.9\text{ V to }5.5\text{ V}$
- Low current consumption: $I_{DD} = 0.7\ \mu\text{A (Typ.)}$
- Rail-to-Rail wide input and output voltage range: $V_{CMR} = V_{SS}\text{ to }V_{DD}$
- Low input offset voltage: 5.0 mV max.
- Lead-free, Sn100%, halogen-free^{*1}

*1. Refer to “■ Product Code List” for details.

■ Applications

- Cellular phones
- PDAs
- Notebook PCs
- Digital cameras
- Digital video cameras

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
SC-88A	NP005-B-P-SD	NP005-B-C-SD	NP005-B-R-SD

■ Product Code List

Table 1

Input Offset Voltage	Product Name (Single)
$V_{IO} = 10\text{ mV max.}$	S-89530ACNC-HCBTF□
$V_{IO} = 5\text{ mV max.}$	S-89531ACNC-HCCTF□

Remark □: G, S or U

■ Pin Configuration

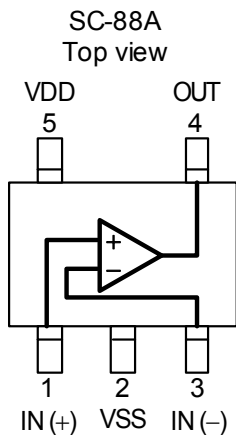


Figure 1

Table 2

Pin No.	Symbol	Description	Internal Equivalent Circuit
1	IN(+)	Non-inverted input pin	Figure 3
2	VSS	GND pin	—
3	IN(-)	Inverted input pin	Figure 3
4	OUT	Output pin	Figure 2
5	VDD	Positive power supply pin	Figure 4

■ Internal Equivalent Circuits

(1) Output pin

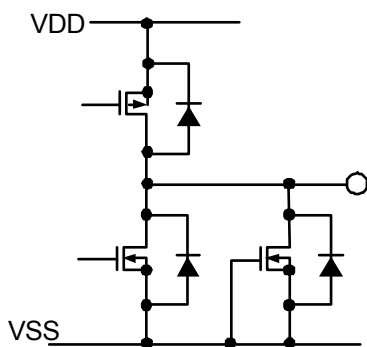


Figure 2

(2) Input pin

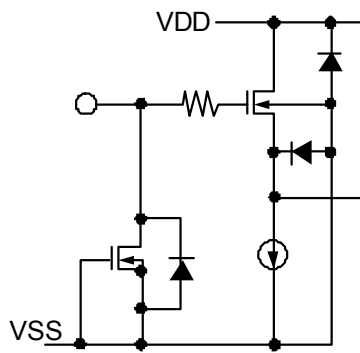


Figure 3

(3) VDD pin

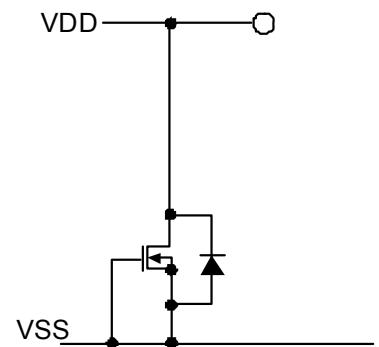


Figure 4

■ **Absolute Maximum Ratings**

Table 3

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Input voltage	V_{IN}	$V_{SS}-0.3$ to $V_{SS}+7.0$ (7.0 max.)	V
Output voltage	V_{OUT}	$V_{SS}-0.3$ to $V_{DD}+0.3$ (7.0 max.)	V
Differential input voltage	V_{IND}	± 5.5	V
Power dissipation	P_D	200 (When not mounted on board)	mW
		350^{*1}	mW
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature	T_{sto}	-55 to +125	°C

*1. When mounted on board

[Mounted board]

- (1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

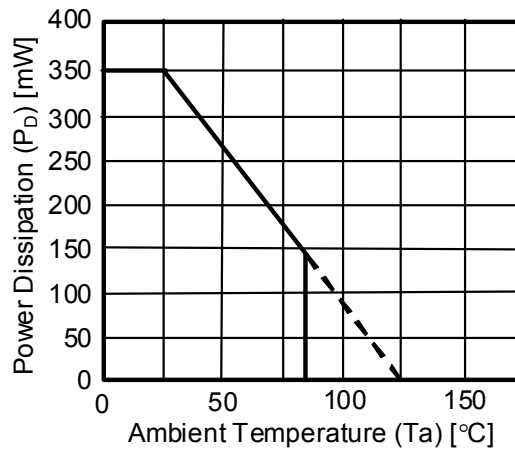


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ **Recommended Operating Voltage Range**

Table 4

Parameter	Symbol	Range	Unit
Operating power supply voltage range	V_{DD}	0.9 to 5.5	V

■ **Electrical Characteristics**

The S-89530ACNC and S-89531ACNC only differ in the input offset voltage. All other specifications are the same.

1. $V_{DD} = 3.0$ V

Table 5

DC Characteristics ($V_{DD} = 3.0$ V)

($T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measurement circuit
Supply current	I_{DDH}	$V_{IN1} = V_{SS}, V_{IN2} = V_{DD}, R_L = \infty$	—	0.7	1.4	μA	Figure 11
	I_{DDL}	$V_{IN1} = V_{DD}, V_{IN2} = V_{SS}, R_L = \infty$	—	0.25	0.5		
Input offset voltage	V_{IO}	S-89530A: $V_{CMR} = 1.5$ V	-10	± 5	+10	mV	Figure 7
		S-89531A: $V_{CMR} = 1.5$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—		
Common-mode input voltage range	V_{CMR}	—	0	—	3.0	V	Figure 8
Voltage gain (open loop)	A_{VOL}	$V_{CMR} = 1.5$ V, $R_L = 1$ M Ω	—	86	—	dB	—
Maximum output swing voltage	V_{OH}	$R_L = 1$ M Ω	2.98	—	—	V	Figure 9
	V_{OL}	$R_L = 1$ M Ω	—	—	0.02		Figure 10
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	45	65	—	dB	Figure 8
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ V to 5.5 V	66	75	—	dB	Figure 6
Source current*1	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	380	500	—	μA	Figure 12
		$V_{OUT} = 0$ V	4000	5500	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	400	550	—	μA	Figure 13
		$V_{OUT} = V_{DD}$	4800	6000	—		

*1. Be sure to use the product with a source current of no more than 7 mA.

Table 6

AC Characteristics ($V_{DD} = 3.0$ V)

($T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV $C_L = 15$ pF (Refer to Figure 14)	—	110	—	μs
Fall propagation delay time	t_{PHL}		—	280	—	
Rise response time	t_{TLH}		—	10	—	
Fall response time	t_{THL}		—	30	—	

2. $V_{DD} = 1.8$ V

Table 7

DC Characteristics ($V_{DD} = 1.8$ V) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measurement circuit
Supply current	I_{DDH}	$V_{IN1} = V_{SS}, V_{IN2} = V_{DD}, R_L = \infty$	—	0.7	1.4	μA	Figure 11
	I_{DDL}	$V_{IN1} = V_{DD}, V_{IN2} = V_{SS}, R_L = \infty$	—	0.25	0.5		
Input offset voltage	V_{IO}	S-89530A: $V_{CMR} = 0.9$ V	-10	± 5	+10	mV	Figure 7
		S-89531A: $V_{CMR} = 0.9$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—		
Common-mode input voltage range	V_{CMR}	—	0	—	1.8	V	Figure 8
Voltage gain (open loop)	A_{VOL}	$V_{CMR} = 0.9$ V, $R_L = 1$ M Ω	—	80	—	dB	—
Maximum output swing voltage	V_{OH}	$R_L = 1$ M Ω	1.78	—	—	V	Figure 9
	V_{OL}	$R_L = 1$ M Ω	—	—	0.02		Figure 10
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	35	55	—	dB	Figure 8
		$V_{SS} \leq V_{CMR} \leq V_{DD} - 0.2$ V	45	60	—		
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ V to 5.5 V	66	75	—	dB	Figure 6
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	200	250	—	μA	Figure 12
		$V_{OUT} = 0$ V	1000	1500	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	220	300	—	μA	Figure 13
		$V_{OUT} = V_{DD}$	1200	1800	—		

Table 8

AC Characteristics ($V_{DD} = 1.8$ V) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV $C_L = 15$ pF (Refer to Figure 14)	—	90	—	μs
Fall propagation delay time	t_{PHL}		—	160	—	
Rise response time	t_{TLH}		—	8	—	
Fall response time	t_{THL}		—	25	—	

3. $V_{DD} = 0.9$ V

Table 9

DC Characteristics ($V_{DD} = 0.9$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measurement circuit
Supply current	I_{DDH}	$V_{IN1} = V_{SS}, V_{IN2} = V_{DD}, R_L = \infty$	—	0.7	1.3	μ A	Figure 11
	I_{DDL}	$V_{IN1} = V_{DD}, V_{IN2} = V_{SS}, R_L = \infty$	—	0.25	0.5		
Input offset voltage	V_{IO}	S-89530A: $V_{CMR} = 0.45$ V	-10	± 5	+10	mV	Figure 7
		S-89531A: $V_{CMR} = 0.45$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—		
Common-mode input voltage range	V_{CMR}	—	0	—	0.9	V	Figure 8
Voltage gain (open loop)	A_{VOL}	$V_{CMR} = 0.45$ V, $R_L = 1$ M Ω	—	74	—	dB	—
Maximum output swing voltage	V_{OH}	$R_L = 1$ M Ω	0.88	—	—	V	Figure 9
	V_{OL}	$R_L = 1$ M Ω	—	—	0.02		Figure 10
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	25	50	—	dB	Figure 8
		$V_{SS} \leq V_{CMR} \leq V_{DD} - 0.3$ V	40	60	—		
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ V to 5.5 V	66	75	—	dB	Figure 6
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	10	45	—	μ A	Figure 12
		$V_{OUT} = 0$ V	12	70	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	10	65	—	μ A	Figure 13
		$V_{OUT} = V_{DD}$	12	120	—		

Table 10

AC Characteristics ($V_{DD} = 0.9$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV $C_L = 15$ pF (Refer to Figure 14)	—	65	—	μ s
Fall propagation delay time	t_{PHL}		—	65	—	
Rise response time	t_{TLH}		—	5	—	
Fall response time	t_{THL}		—	20	—	

■ **Measurement Circuits**

1. Power supply voltage rejection ratio

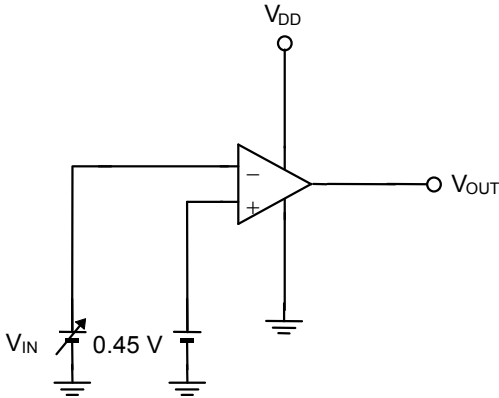


Figure 6

- The power supply voltage rejection ratio (PSRR) is calculated by the following expression, with the value of V_{IO} measured at each V_{DD} .

Measurement conditions:

When $V_{DD} = 0.9\text{ V}$: $V_{DD} = V_{DD1}$, $V_{IO} = V_{IO1}$

When $V_{DD} = 5.5\text{ V}$: $V_{DD} = V_{DD2}$, $V_{IO} = V_{IO2}$

$$PSRR = 20\log\left(\left|\frac{V_{DD1} - V_{DD2}}{V_{IO1} - V_{IO2}}\right|\right)$$

2. Input offset voltage

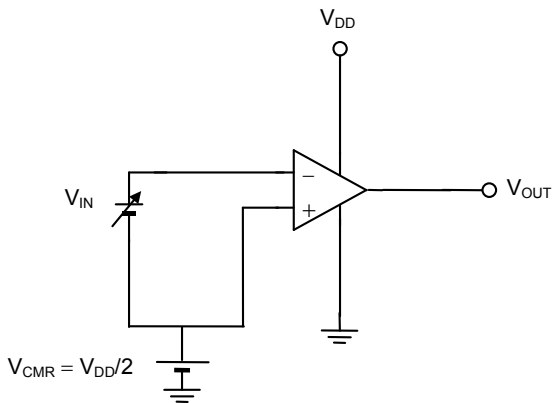


Figure 7

- Input offset voltage (V_{IO})
 The input offset voltage (V_{IO}) is defined as V_{IN} at which V_{OUT} changes by changing V_{IN} .

3. Common-mode input signal rejection rate, common-mode input voltage range

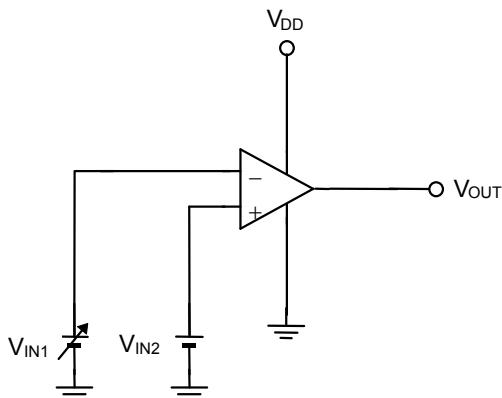


Figure 8

- Common-mode input signal rejection ratio (CMRR)
 The common-mode input signal rejection ratio, CMRR, can be calculated by the following expression, with the offset voltage (V_{IO}) defined as V_{IN1} minus V_{IN2} at which V_{OUT} is changed by changing V_{IN1} .

Measurement conditions:

When $V_{IN2} = V_{CMR}(\text{max.})$: $V_{IO} = V_{IO1}$

When $V_{IN2} = V_{CMR}(\text{min.})$: $V_{IO} = V_{IO2}$

$$CMRR = 20 \log \left(\frac{V_{CMR}(\text{max.}) - V_{CMR}(\text{min.})}{V_{IO1} - V_{IO2}} \right)$$

- Common-mode input voltage range (V_{CMR})
 The common-mode input voltage range is the range of V_{IN2} within which V_{OUT} satisfies the common mode input signal rejection ratio specification.

4. Maximum output swing voltage

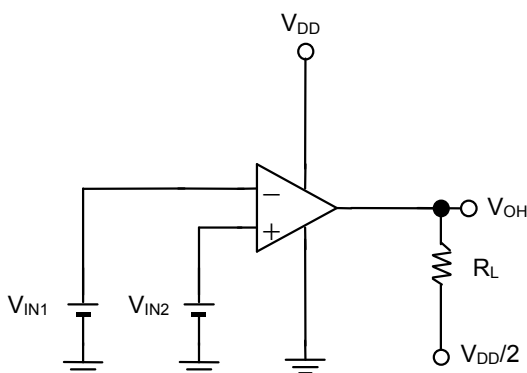


Figure 9

- Maximum output swing voltage (V_{OH})

Measurement conditions: $V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$

$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$

$R_L = 1 \text{ M}\Omega$

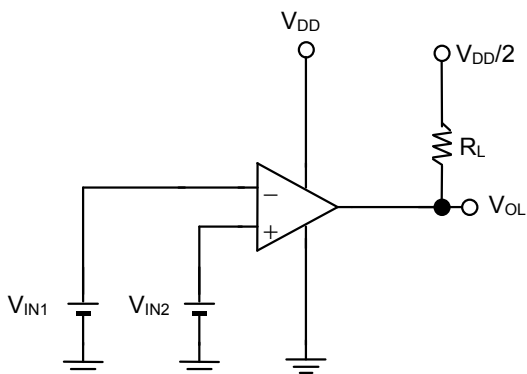


Figure 10

- Maximum output swing voltage (V_{OL})

Measurement conditions: $V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$

$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$

$R_L = 1 \text{ M}\Omega$

5. Supply current

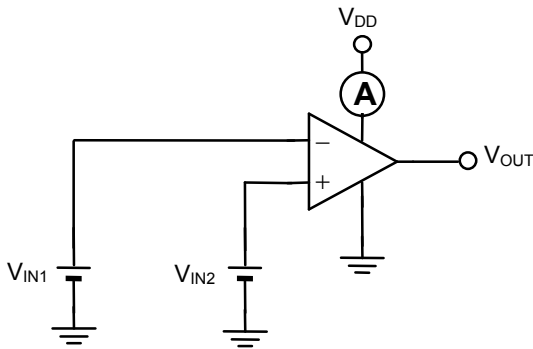


Figure 11

- Supply current (I_{DDH})
 Measurement conditions: $V_{IN1} = V_{SS}$
 $V_{IN2} = V_{DD}$
- Supply current (I_{DDL})
 Measurement conditions: $V_{IN1} = V_{DD}$
 $V_{IN2} = V_{SS}$

6. Source current

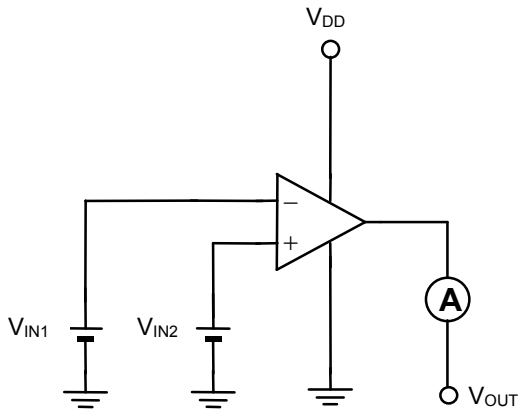


Figure 12

- Source current (I_{SOURCE})
 Measurement conditions: $V_{IN1} = \frac{V_{DD}}{2} - 0.1V$
 $V_{IN2} = \frac{V_{DD}}{2} + 0.1V$
 $V_{OUT} = V_{DD} - 0.1V$ or
 $V_{OUT} = 0V$

7. Sink current

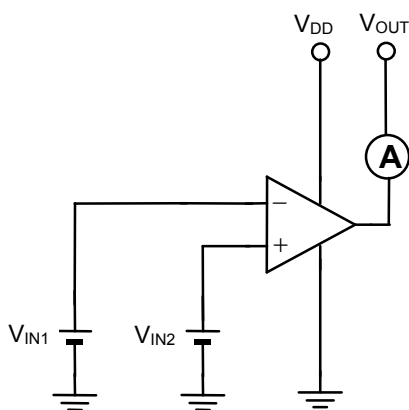


Figure 13

- Sink current (I_{SINK})
 Measurement conditions: $V_{IN1} = \frac{V_{DD}}{2} + 0.1V$
 $V_{IN2} = \frac{V_{DD}}{2} - 0.1V$
 $V_{OUT} = 0.1V$ or
 $V_{OUT} = V_{DD}$

8. Propagation delay time/transient response time

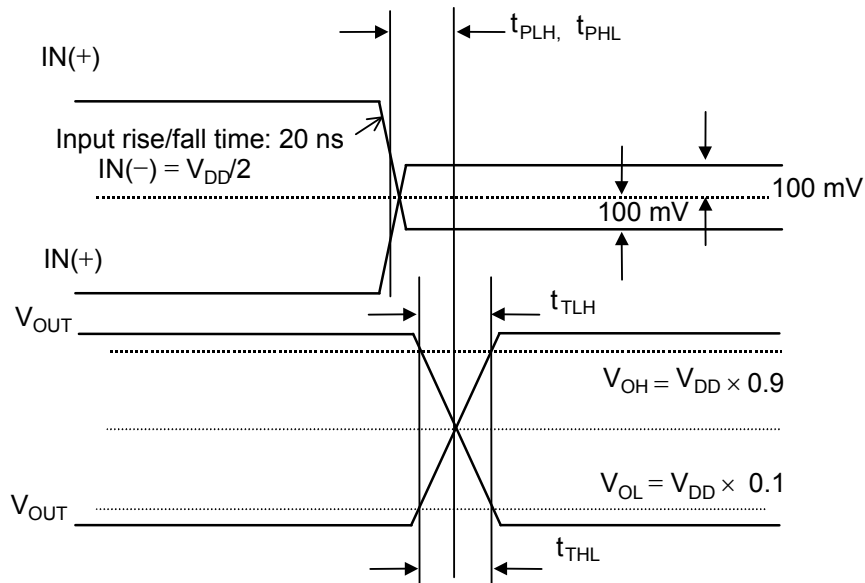


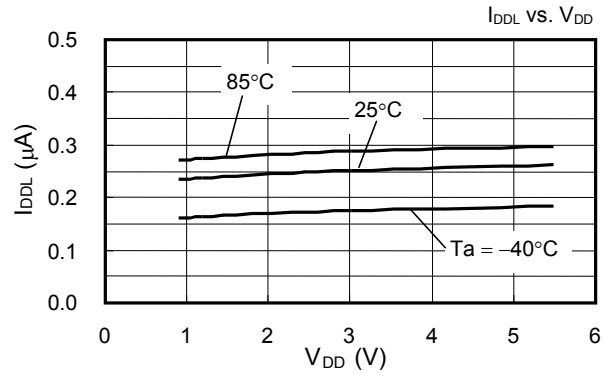
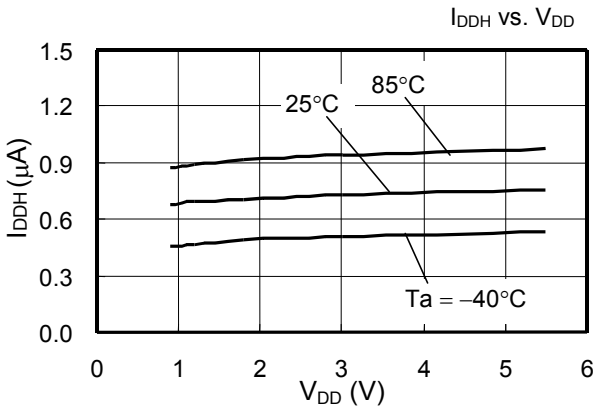
Figure 14

■ Cautions

- When $R_L = 100 \text{ k}\Omega$, V_{OH} may rise only 0.65 V if the temperature is -40°C and $V_{DD} = 0.9 \text{ V}$.
 If the temperature is -20°C , however, V_{OH} rises to 0.8 V, which is 100 mV below V_{DD} , when $V_{DD} = 0.9 \text{ V}$, even if $R_L = 100 \text{ k}\Omega$.
 If V_{DD} is 1.2 V, V_{OH} rises to 0.88 V, which is 20 mV below V_{DD} when $R_L = 100 \text{ k}\Omega$, even at -40°C .
 The temperature characteristics data described above can be used as reference data. Note that 100% testing under these conditions has not been performed.
- Be sure to use the product with a source current of no more than 7 mA.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

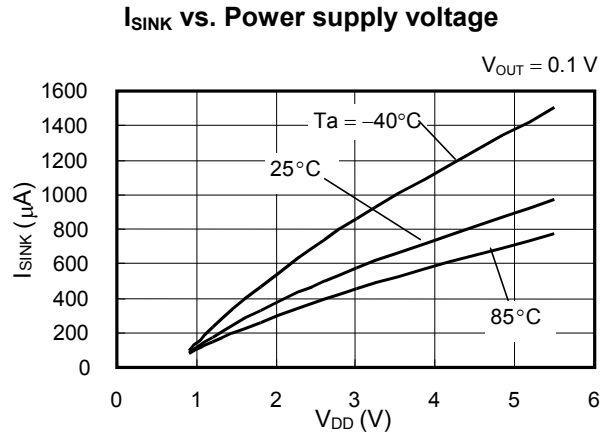
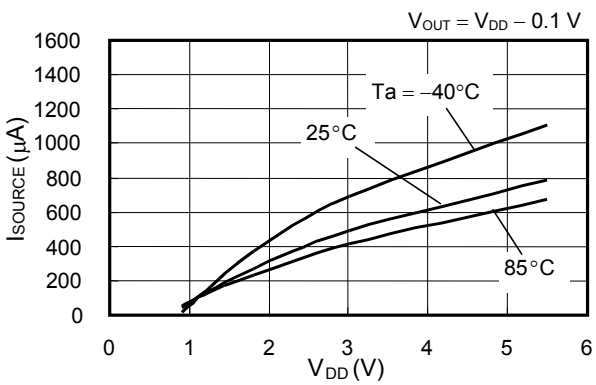
■ Characteristics (Reference Data)

1. Current consumption vs. Power supply voltage

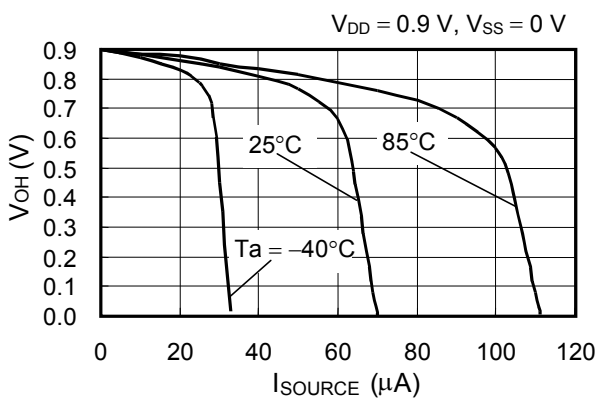
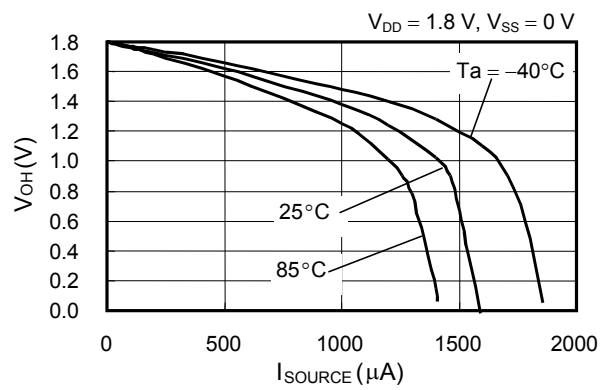
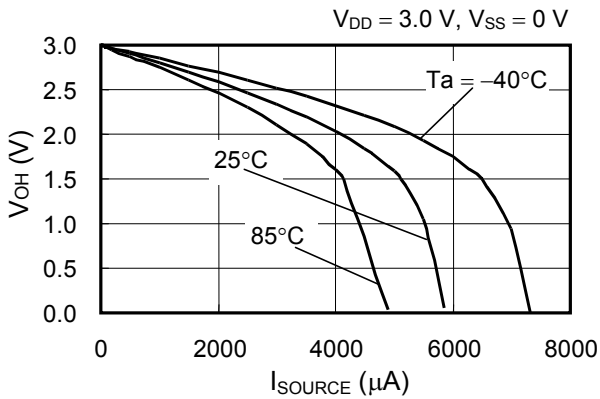


2. Output current

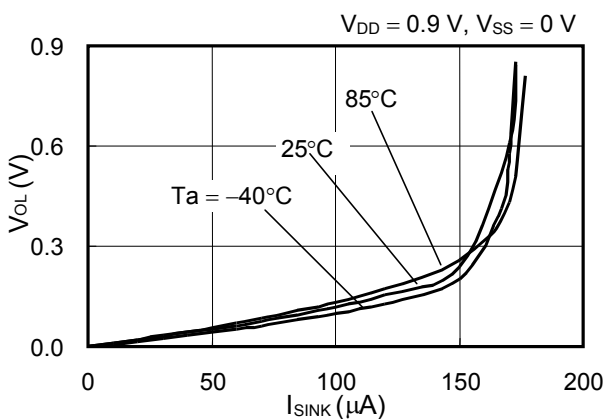
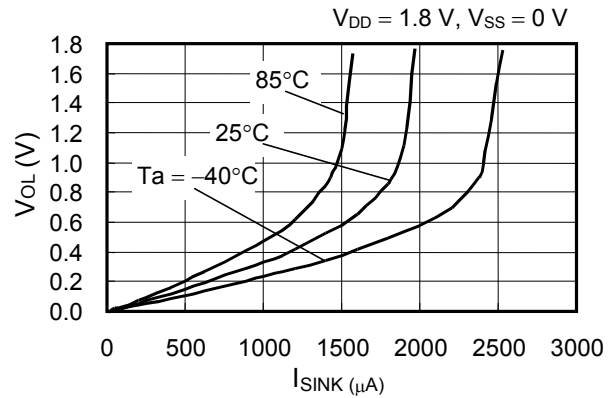
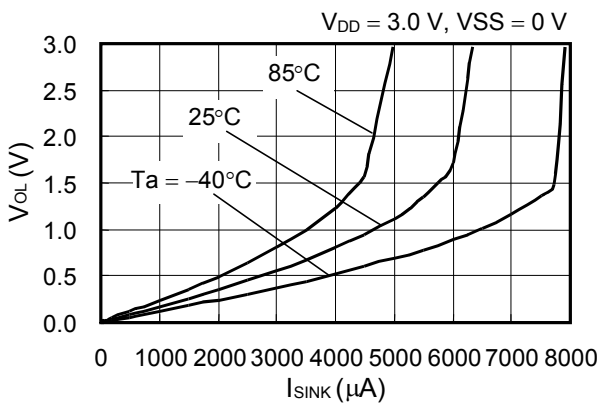
2-1. I_{SOURCE} vs. Power supply voltage

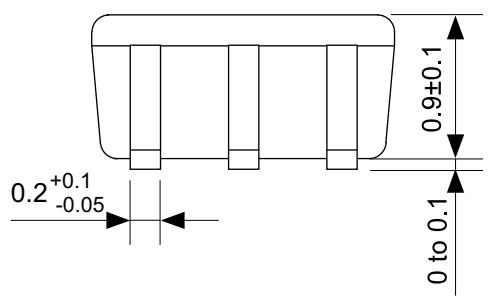
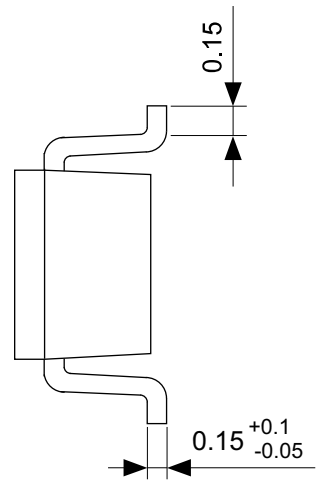
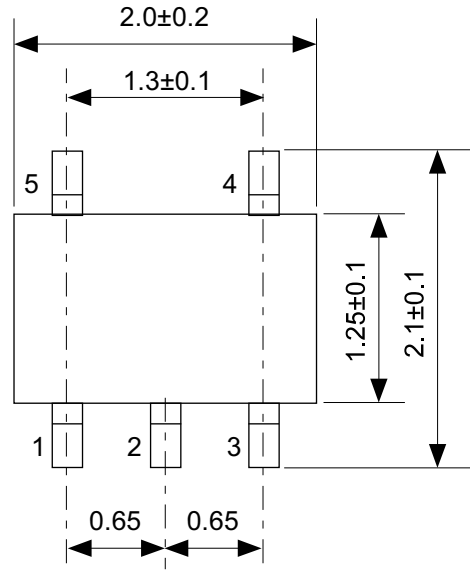


2-2. Output voltage (V_{OH}) vs. I_{SOURCE}



2-3. Output Voltage (V_{OL}) vs. I_{SINK}

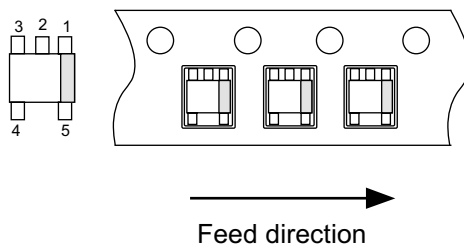
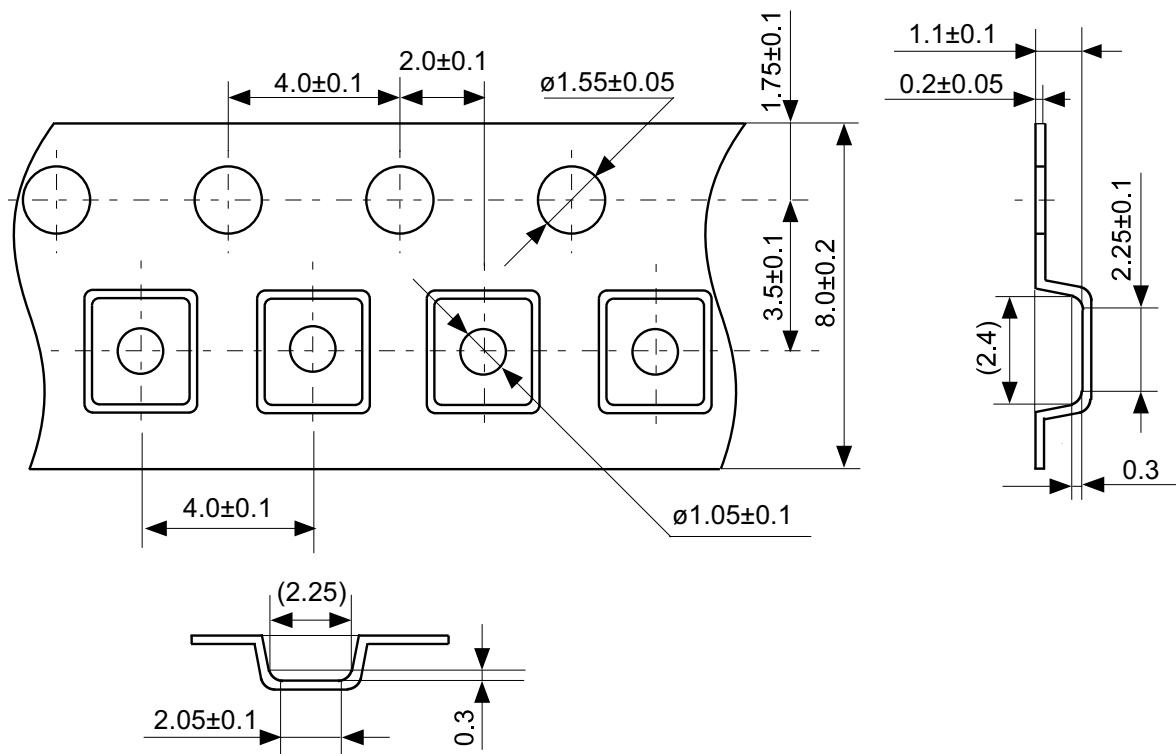




No. NP005-B-P-SD-1.2

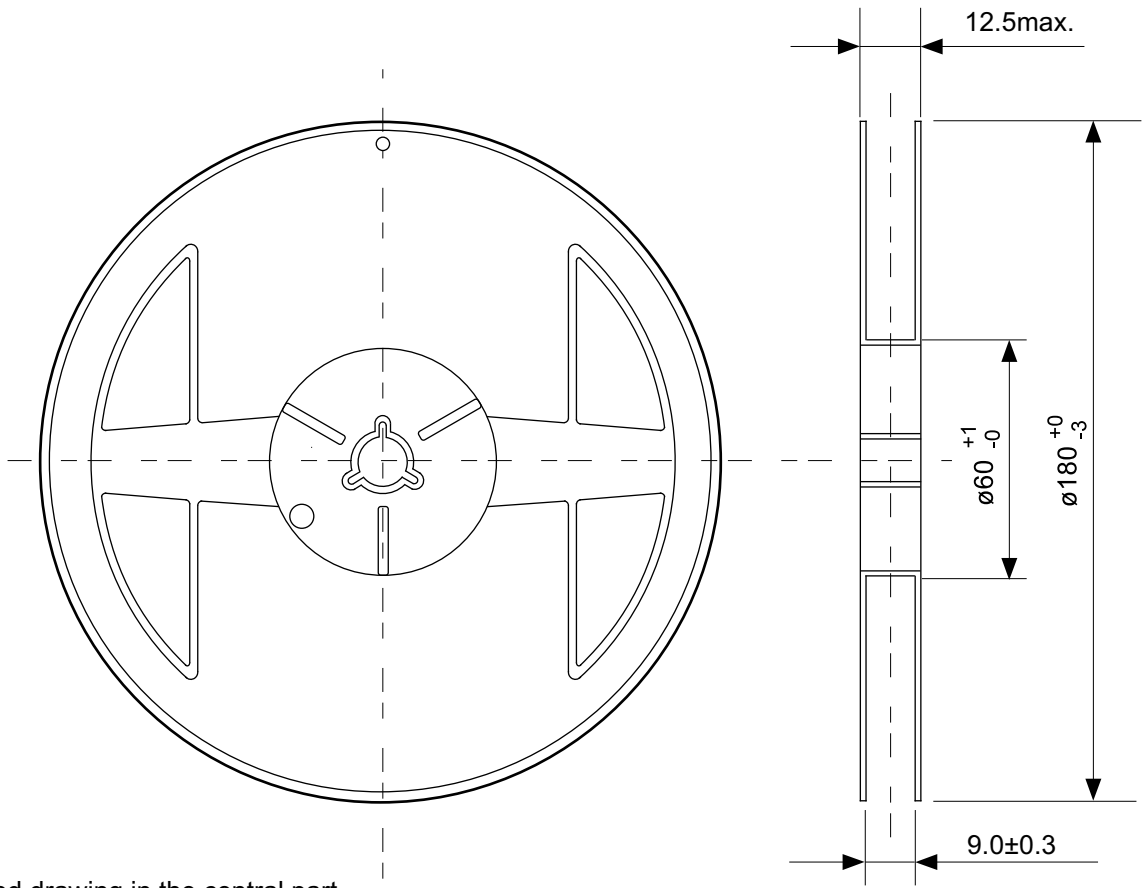
TITLE	SC88A-B-PKG Dimensions
No.	NP005-B-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.

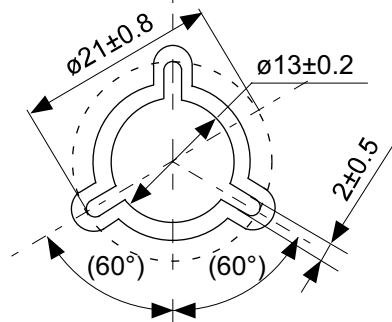


No. NP005-B-C-SD-2.0

TITLE	SC88A-B-Carrier Tape
No.	NP005-B-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. NP005-B-R-SD-2.1

TITLE	SC88A-B-Reel		
No.	NP005-B-R-SD-2.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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