

DF2B5M4SL

Application

- ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

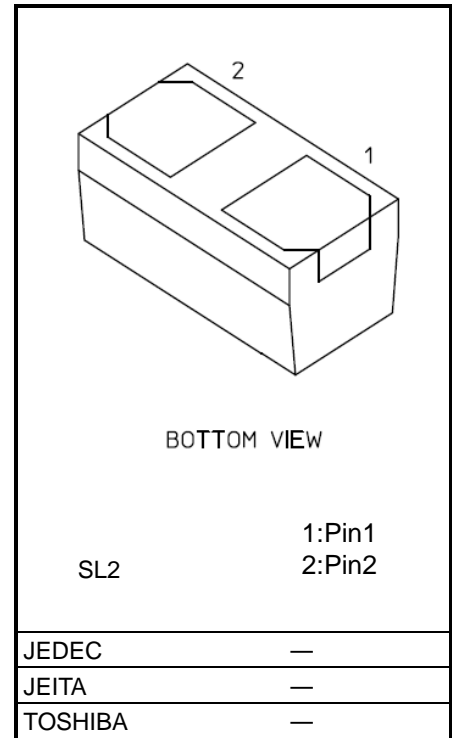
Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Electrostatic discharge voltage IEC61000-4-2(Contact) IEC61000-4-2(Air)	V _{ESD} (Note 1)	± 23 ± 25	kV
Peak pulse power (tp = 8 / 20 s)	P _{PK}	30	W
Maximum peak pulse current (tp = 8 / 20 s)	I _{PP} (Note 2)	2	A
Junction temperature	T _j	150	°C
Storage temperature range	T _{stg}	-55 to 150	°C

Note1 : according to IEC61000-4-2

Note2 : according to IEC61000-4-5

Note3:Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/ “Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



Electrical Characteristics (Ta = 25°C)

V_{RWM} : Working peak reverse voltage

V_{BR} : Reverse breakdown voltage

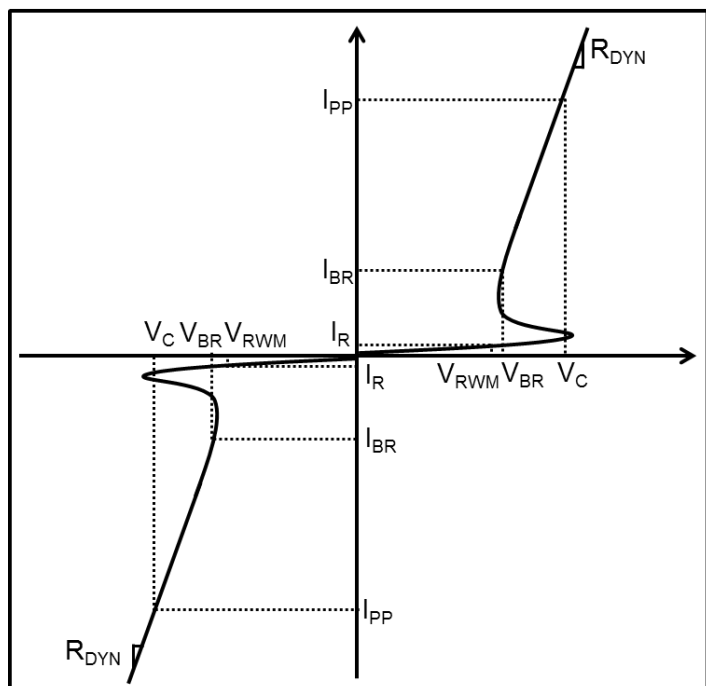
I_{BR} : Reverse breakdown current

I_R : Reverse Current

V_C : Clamping Voltage

I_{PP} : Peak pulse current

R_{DYN} : Dynamic resistance



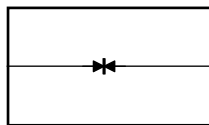
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse stand-off voltage	V_{RWM}	—	—	—	3.6	V
Reverse breakdown voltage	V_{BR}	$I_{BR} = 1 \text{ mA}$	4.0	5.0	6.0	V
Reverse current	I_R	$V_{RWM} = 5.5 \text{ V}$	—	—	0.1	μA
Clamping Voltage	V_c	$I_{pp}=1\text{A}$ (Note1)	—	7.5	—	V
	V_c	$I_{pp}=2\text{A}$ (Note1)	—	10	15	V
Clamping Voltage	V_c	$I_{TLP}=16\text{A}$ (Note2)	—	17	—	V
	V_c	$I_{TLP}=30\text{A}$ (Note2)	—	24	—	V
Dynamic resistance	R_{DYN}	(Note2)	—	0.5	—	Ω
Total capacitance	C_t	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$ (Note3)	—	0.2	0.3	pF

Note1 : Based on IEC61000-4-5 8/20 μs pulse.

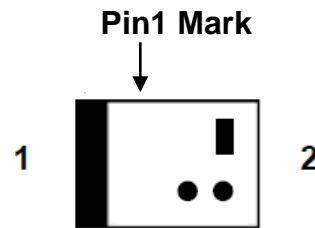
Note2 : TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100\text{ns}$, $t_r = 300\text{ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$,
extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 8\text{A}$ and $I_{PP2} = 16\text{A}$.

Note3 : Guaranteed by design.

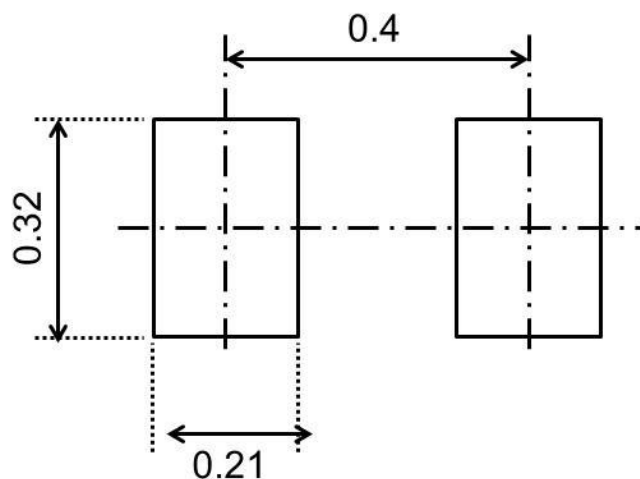
Equivalent Circuit (Top View)



Marking

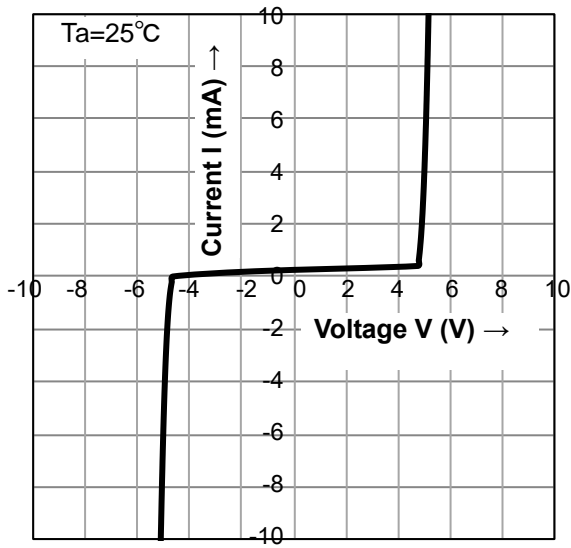


Land Pattern Dimensions for Reference Only (Unit : mm)

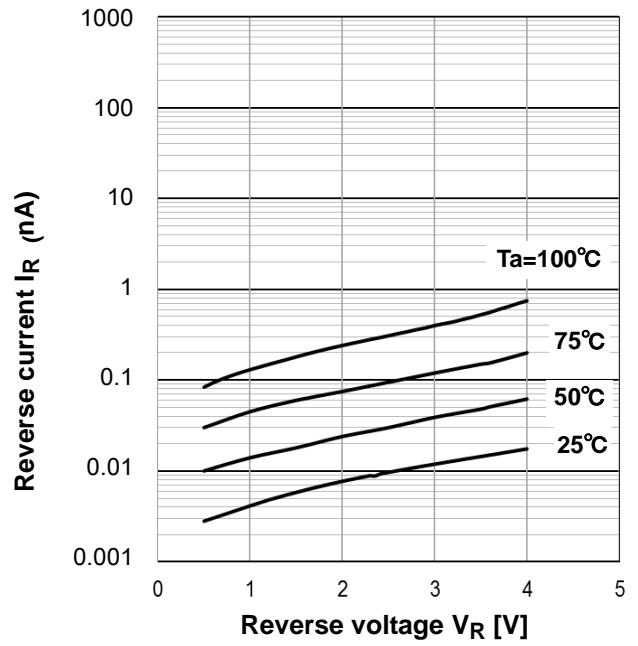


Characteristics Curves (Note)

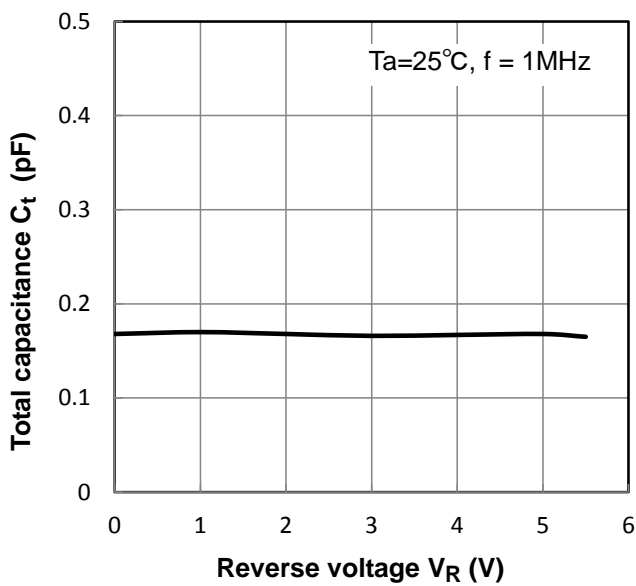
I - V



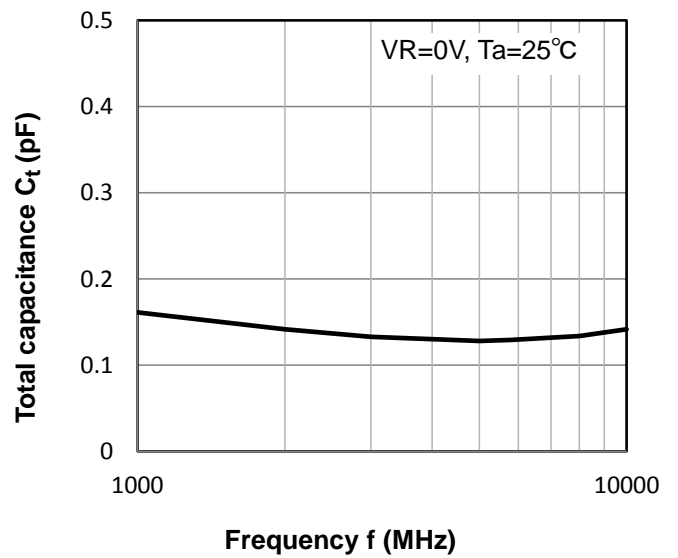
$I_R - V_R$



$C_t - V_R$

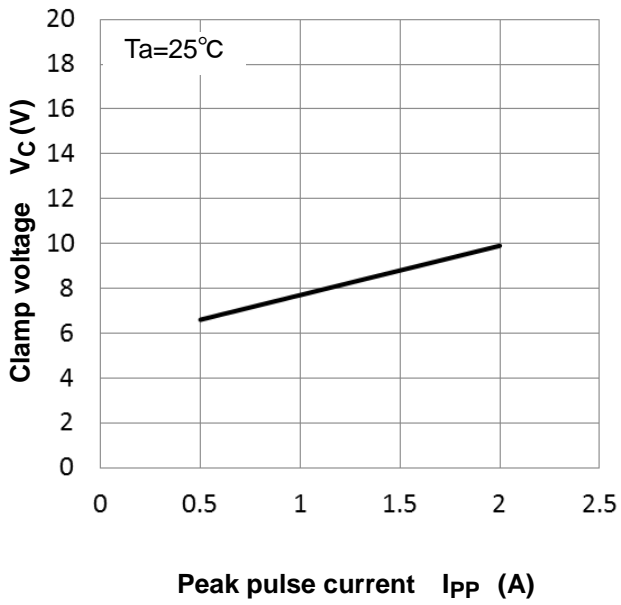


$C_t - f$



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

V_C - I_{PP}



Based on IEC61000-4-5 8/20 μ s pulse.(Ed2)

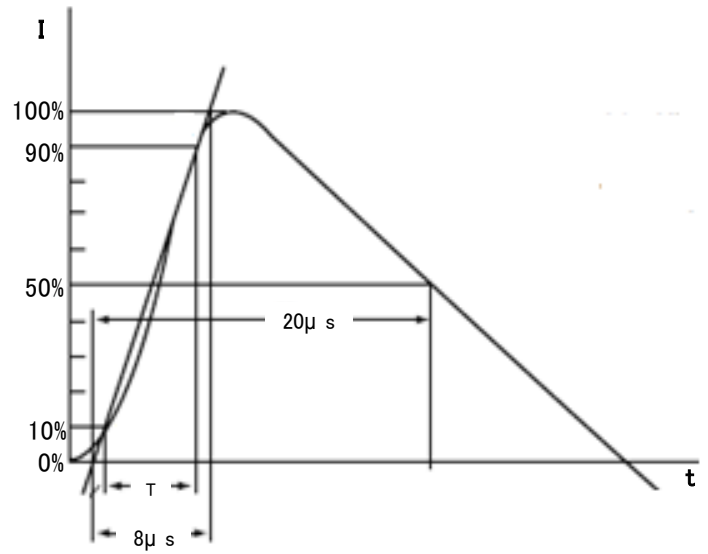
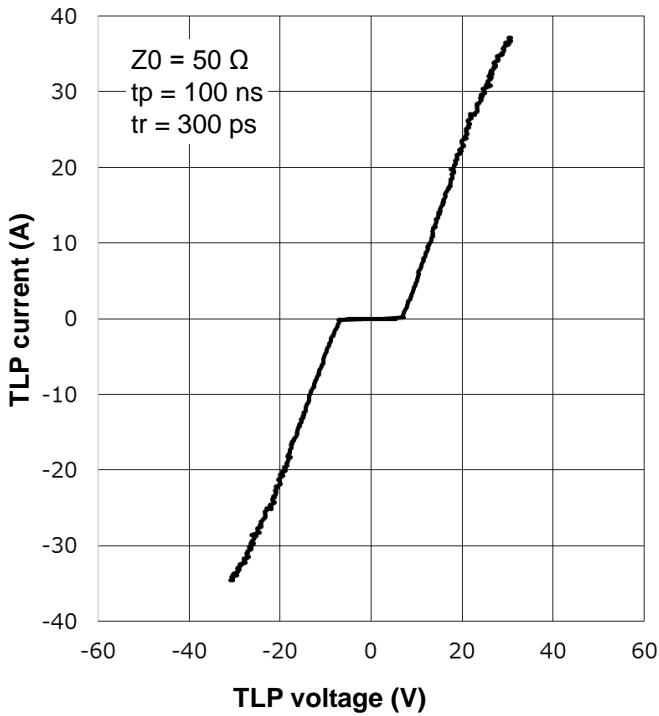


Fig Based on IEC61000-4-5 8/20 μ s pulse.(Ed.2)

TLP



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Insertion Loss (S21)

S21-f

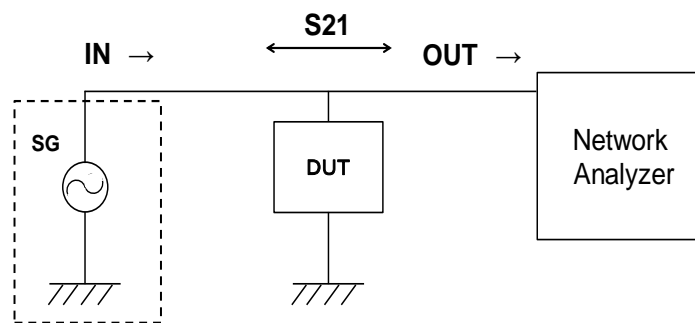
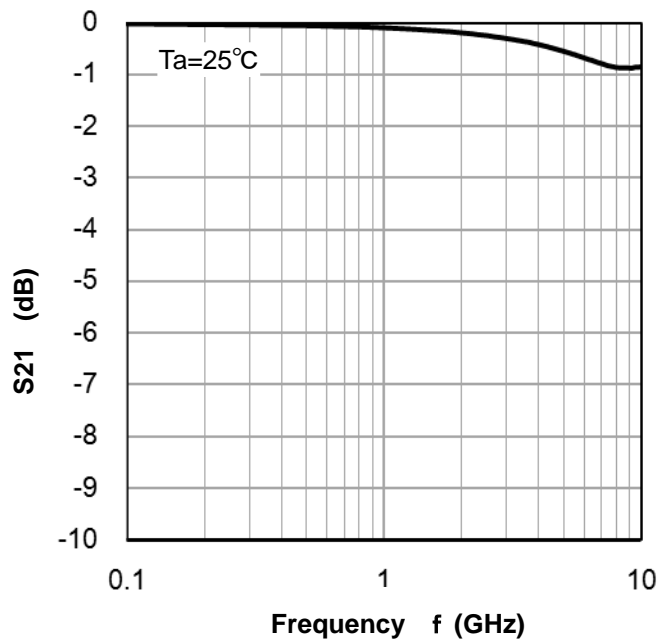


Fig. S21 measurement circuit

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ESD Clamp Waveform (IEC61000-4-2) (Note)

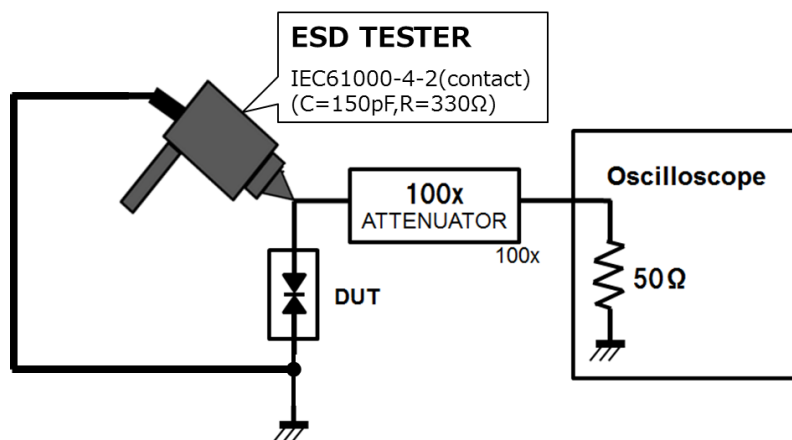
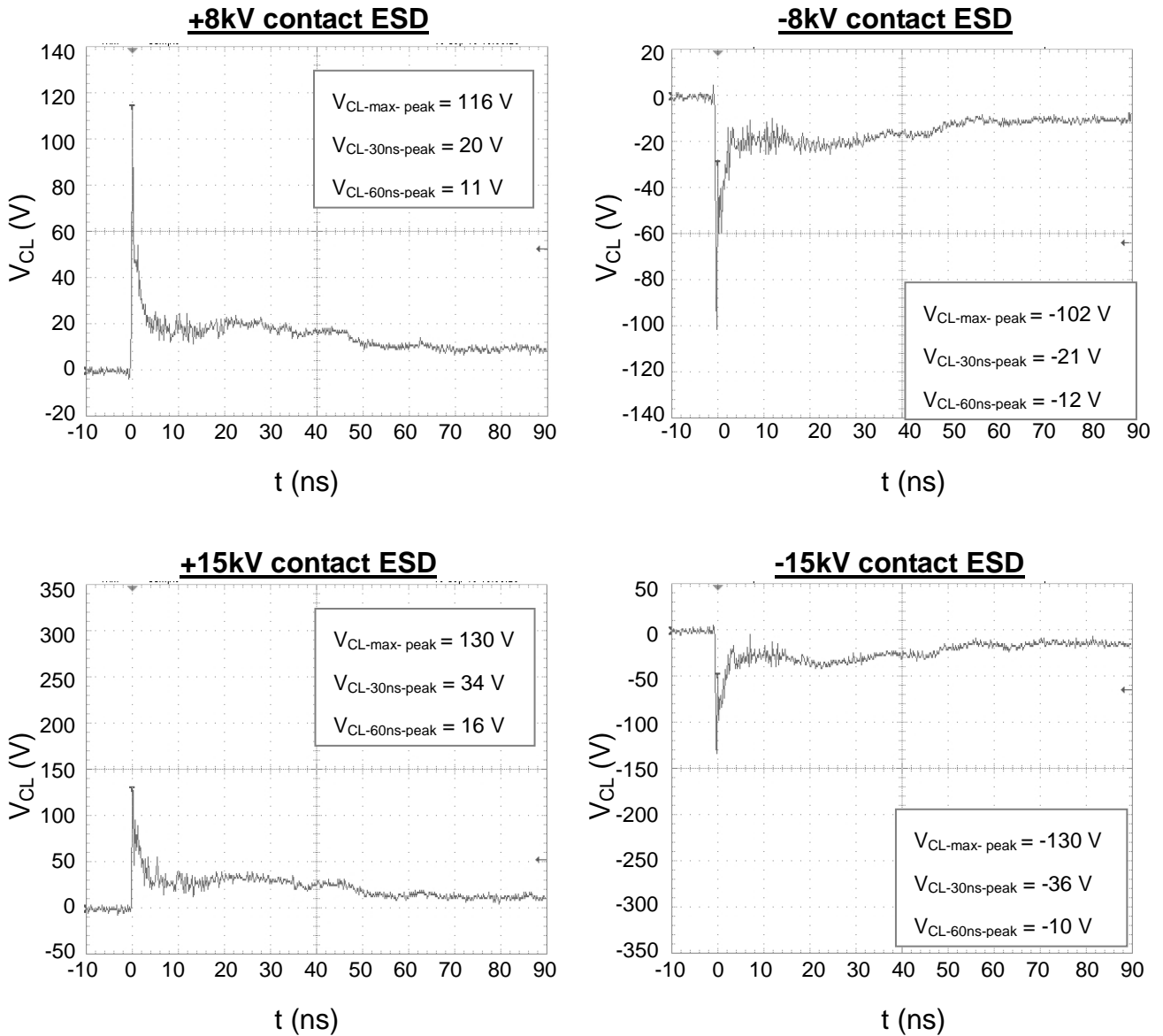
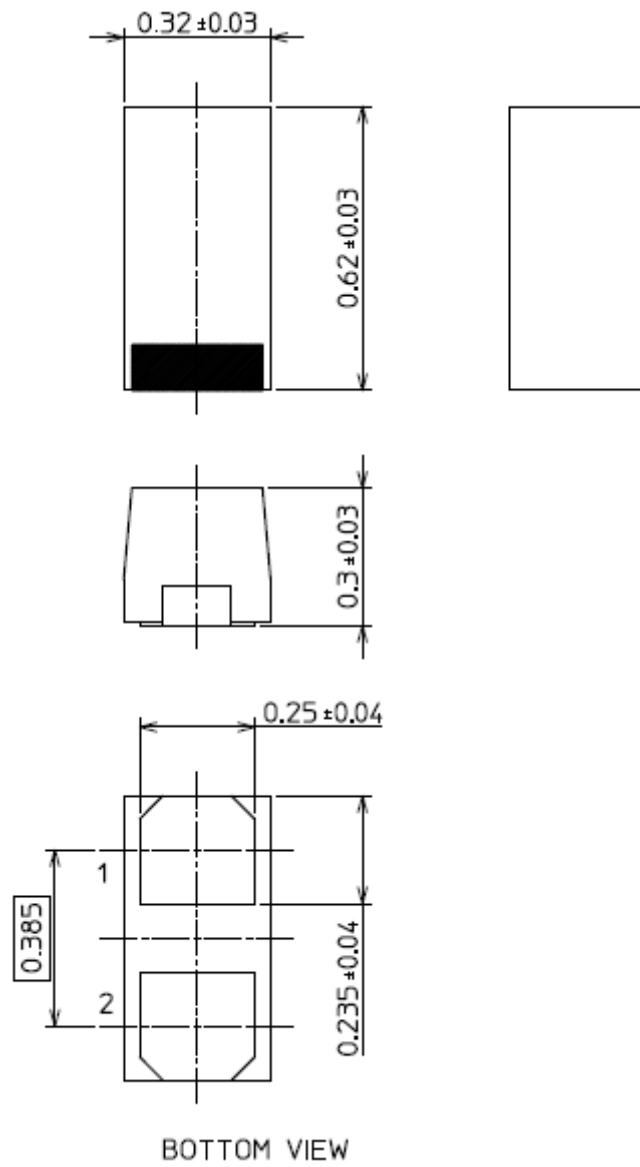


Fig. IEC61000-4-2 (Contact)

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Package Dimensions (Unit : mm)



Weight: 0.2 mg (typ.)

Package Name(s)	
TOSHIBA:	
Nickname:	SL2

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