

FEATURES

- 128 Position Potentiometer Replacement
- 10 k Ω , 50 k Ω , 100 k Ω
- Very Low Power: 40 μ A Max
- Increment/Decrement Count Control
- Qualified for automotive applications

APPLICATIONS

- Mechanical Potentiometer Replacement
- Remote Incremental Adjustment Applications
- Instrumentation: Gain, Offset Adjustment
- Programmable Voltage-to-Current Conversion
- Programmable Filters, Delays, Time Constants
- Line Impedance Matching
- Power Supply Adjustment

GENERAL DESCRIPTION

The AD5220 provides a single channel, 128-position digitally controlled variable resistor (VR) device. This device performs the same electronic adjustment function as a potentiometer or variable resistor. These products were optimized for instrument and test equipment push-button applications. A choice between bandwidth or power dissipation are available as a result of the wide selection of end-to-end terminal resistance values.

The AD5220 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digitally controlled UP/DOWN counter. The resistance between the wiper and either end point of the fixed resistor provides a constant resistance step size that is equal to the end-to-end resistance divided by the number of positions (e.g., $R_{STEP} = 10 \text{ k}\Omega / 128 = 78 \Omega$). The variable resistor offers a true adjustable value of resistance, between the A terminal and the wiper, or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10 k Ω , 50 k Ω , or 100 k Ω has a nominal temperature coefficient of 800 ppm/ $^{\circ}$ C.

The chip select \overline{CS} , count CLK and U/\overline{D} direction control inputs set the variable resistor position. These inputs that control the internal UP/DOWN counter can be easily generated with mechanical or push button switches (or other contact closure devices). External debounce circuitry is required for the negative-edge sensitive CLK pin. This simple digital interface eliminates the need for microcontrollers in front panel interface designs.

The AD5220 is available in both surface mount (SO-8) and the 8-lead plastic DIP package. For ultracompact solutions selected models are available in the thin μ SOIC package. All parts are guaranteed to operate over the extended industrial temperature range of -40° C to $+85^{\circ}$ C. For 3-wire, SPI compatible interface applications, see the AD7376/AD8400/AD8402/AD8403 products.

REV. A

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FUNCTIONAL BLOCK DIAGRAM



Figure 1. Typical Push-Button Control Application



Figure 2a. Stair-Step Increment Output

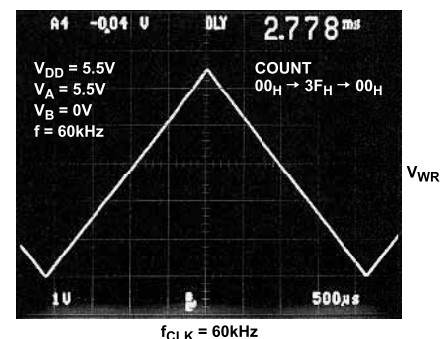


Figure 2b. Full-Scale Up/Down Count

AD5220—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($V_{DD} = +3\text{ V} \pm 10\%$ or $+5\text{ V} \pm 10\%$, $V_A = +V_{DD}$, $V_B = 0\text{ V}$, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL ²	R-DNL	R_{WB} , $V_A = \text{NC}$, $R_{AB} = 10\text{ k}\Omega$	-1	± 0.4	+1	LSB
Resistor Nonlinearity ²	R-INL	R_{WB} , $V_A = \text{NC}$, $R_{AB} = 50\text{ k}\Omega$ or $100\text{ k}\Omega$	-0.5	± 0.1	+0.5	LSB
		R_{WB} , $V_A = \text{NC}$, $R_{AB} = 10\text{ k}\Omega$	-1	± 0.5	+1	LSB
Nominal Resistor Tolerance	ΔR	R_{WB} , $V_A = \text{NC}$, $R_{AB} = 50\text{ k}\Omega$ or $100\text{ k}\Omega$	-0.5	± 0.1	+0.5	LSB
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	$T_A = +25^\circ\text{C}$	-30		+30	%
Wiper Resistance	R_W	$V_{AB} = V_{DD}$, Wiper = No Connect		800		ppm/ $^\circ\text{C}$
		$I_W = V_{DD}/R$, $V_{DD} = +3\text{ V}$ or $+5\text{ V}$		40	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications Apply to All VRs						
Resolution	N		7			Bits
Integral Nonlinearity ³	INL	$R_{AB} = 10\text{ k}\Omega$	-1	± 0.5	+1	LSB
		$R_{AB} = 50\text{ k}\Omega$, $100\text{ k}\Omega$	-0.5	± 0.2	+0.5	LSB
Differential Nonlinearity Error ³	DNL	$R_{AB} = 10\text{ k}\Omega$	-1	± 0.4	+1	LSB
		$R_{AB} = 50\text{ k}\Omega$, $100\text{ k}\Omega$	-0.5	± 0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 40 _H		20		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSE}	Code = 7F _H	-2	-0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00 _H	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range ⁴	V_A , V_B , V_W		0		V_{DD}	V
Capacitance ⁵ A, B	C_A , C_B	$f = 1\text{ MHz}$, Measured to GND, Code = 40 _H		10		pF
Capacitance ⁵ W	C_W	$f = 1\text{ MHz}$, Measured to GND, Code = 40 _H		48		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		7.5		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	$V_{DD} = +5\text{ V}/+3\text{ V}$	2.4/2.1			V
Input Logic Low	V_{IL}	$V_{DD} = +5\text{ V}/+3\text{ V}$			0.8/0.6	V
Input Current	I_{IL}	$V_{IN} = 0\text{ V}$ or $+5\text{ V}$			± 1	μA
Input Capacitance ⁵	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
Supply Current	I_{DD}	$V_{IH} = +5\text{ V}$ or $V_{IL} = 0\text{ V}$, $V_{DD} = +5\text{ V}$		15	40	μA
Power Dissipation ⁶	P_{DISS}	$V_{IH} = +5\text{ V}$ or $V_{IL} = 0\text{ V}$, $V_{DD} = +5\text{ V}$		75	200	μW
Power Supply Sensitivity	PSS			0.004	0.015	%/%
DYNAMIC CHARACTERISTICS^{5, 7, 8}						
Bandwidth -3 dB	BW_10K	$R_{AB} = 10\text{ k}\Omega$, Code = 40 _H		650		kHz
	BW_50K	$R_{AB} = 50\text{ k}\Omega$, Code = 40 _H		142		kHz
	BW_100K	$R_{AB} = 100\text{ k}\Omega$, Code = 40 _H		69		kHz
Total Harmonic Distortion	THD _W	$V_A = 1\text{ V rms} + 2.5\text{ V dc}$, $V_B = 2.5\text{ V dc}$, $f = 1\text{ kHz}$		0.002		%
V_W Settling Time	t_s	$V_A = V_{DD}$, $V_B = 0\text{ V}$, 50% of Final Value, 10K/50K/100K		0.6/3/6		μs
Resistor Noise Voltage	e_{NWB}	$R_{WB} = 5\text{ k}\Omega$, $f = 1\text{ kHz}$		14		$\text{nV}/\sqrt{\text{Hz}}$
INTERFACE TIMING CHARACTERISTICS Applies to All Parts ^{5, 9}						
Input Clock Pulsewidth	t_{CH} , t_{CL}	Clock Level High or Low	25			ns
$\overline{\text{CS}}$ to CLK Setup Time	t_{CSS}		20			ns
$\overline{\text{CS}}$ Rise to Clock Hold Time	t_{CSH}		20			ns
$\text{U}/\overline{\text{D}}$ to Clock Fall Setup Time	t_{UDS}		10			ns

NOTES

¹Typicals represent average readings at $+25^\circ\text{C}$ and $V_{DD} = +5\text{ V}$.

²Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 29 test circuit.

³INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0\text{ V}$. DNL specification limits of ± 1 LSB maximum are guaranteed monotonic operating conditions. See Figure 28 test circuit.

⁴Resistor terminals A, B, W have no limitations on polarity with respect to each other.

⁵Guaranteed by design and not subject to production test.

⁶ P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.

⁷Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

⁸All dynamic characteristics use $V_{DD} = +5\text{ V}$.

⁹See timing diagrams for location of measured values. All input control voltages are specified with $t_R = t_F = 1\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using both $V_{DD} = +3\text{ V}$ or $+5\text{ V}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to GND	-0.3 V, +7 V
V_A , V_B , V_W to GND	0 V, V_{DD}
A_X - B_X , A_X - W_X , B_X - W_X	± 20 mA
Digital Input Voltage to GND	0 V, $V_{DD} + 0.3$ V
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Maximum Junction Temperature (T_J MAX)	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Package Power Dissipation	$(T_J \text{ max} - T_A) / \theta_{JA}$
Thermal Resistance θ_{JA}		
P-DIP (N-8)	$103^\circ\text{C}/\text{W}$
SOIC (SO-8)	$158^\circ\text{C}/\text{W}$
μ SOIC (RM-8)	$206^\circ\text{C}/\text{W}$

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

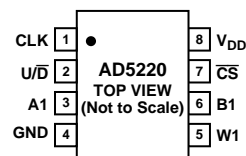
Table I. Truth Table

$\overline{\text{CS}}$	CLK	$\text{U}/\overline{\text{D}}$	Operation
L	↓	H	Wiper Increment Toward Terminal A
L	↓	L	Wiper Decrement Toward Terminal B
H	X	X	Wiper Position Fixed



Figure 3. Detail Timing Diagram

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	CLK	Serial Clock Input, Negative Edge Triggered
2	$\text{U}/\overline{\text{D}}$	UP/DOWN Direction Increment Control
3	A1	Terminal A1
4	GND	Ground
5	W1	Wiper Terminal
6	B1	Terminal B1
7	$\overline{\text{CS}}$	Chip Select Input, Active Low
8	V_{DD}	Positive Power Supply

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5220 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5220—Typical Performance Characteristics



Figure 4. Wiper to End Terminal Resistance vs. Code

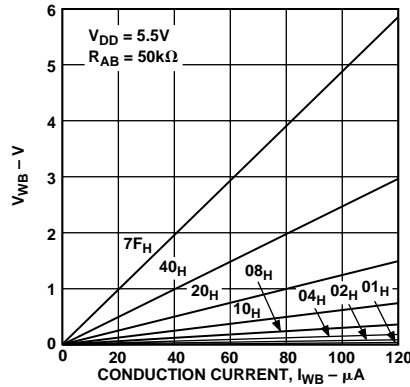


Figure 5. Resistance Linearity vs. Conduction Current

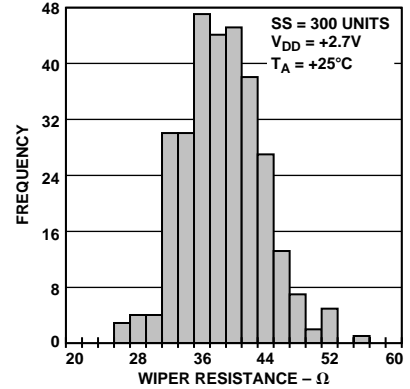


Figure 6. Wiper Contact Resistance



Figure 7. R-DNL Relative Resistance Step Position Nonlinearity Error vs. Code

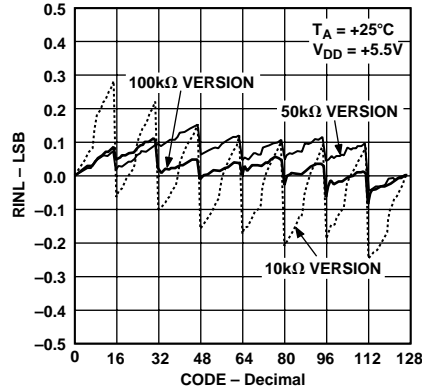


Figure 8. R-INL Resistance Nonlinearity Error vs. Supply Voltage



Figure 9. Potentiometer Divider INL Error vs. Code



Figure 10. Potentiometer Divider DNL Error vs. Code



Figure 11. Potentiometer Divider INL Error vs. Supply Voltage

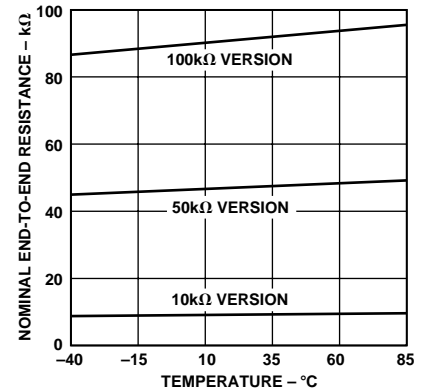


Figure 12. Nominal Resistance vs. Temperature



Figure 13. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco (10 k Ω and 50 k Ω)

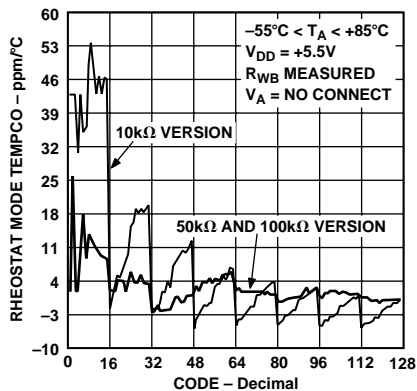


Figure 14. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco



Figure 15. 10 k Ω Gain vs. Frequency vs. Code



Figure 16. 50 k Ω Gain vs. Frequency vs. Code

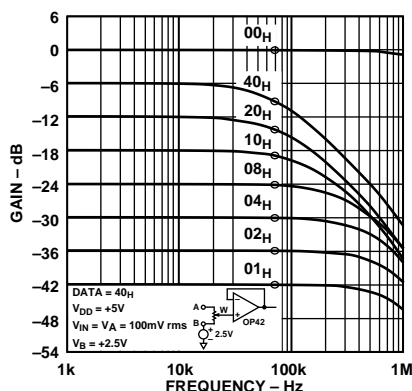


Figure 17. 100 k Ω Gain vs. Frequency vs. Code



Figure 18. Digital Feedthrough



Figure 19. Midscale Transition Glitch

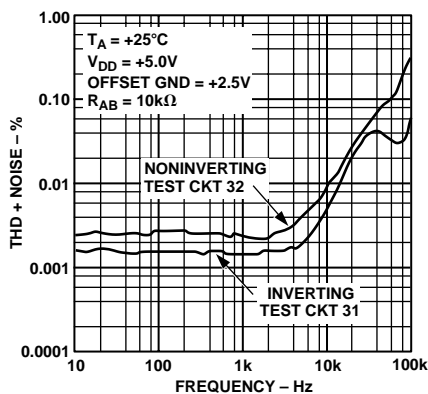


Figure 20. Total Harmonic Distortion Plus Noise vs. Frequency



Figure 21. Normalized Gain Flatness vs. Frequency

AD5220

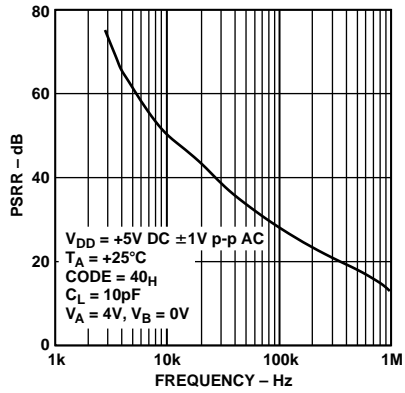


Figure 22. Power Supply Rejection vs. Frequency



Figure 23. I_{DD} Supply Current vs. Clock Frequency



Figure 24. Incremental Wiper Contact Resistance vs. V_B



Figure 25. Supply Current vs. Temperature I_{DD}



Figure 26. Supply Current vs. Input Logic Voltage

Parametric Test Circuits—AD5220



Figure 27. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

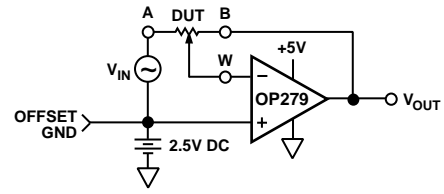


Figure 31. Inverting Programmable Gain Test Circuit



Figure 28. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



Figure 32. Noninverting Programmable Gain Test Circuit



Figure 29. Wiper Resistance Test Circuit

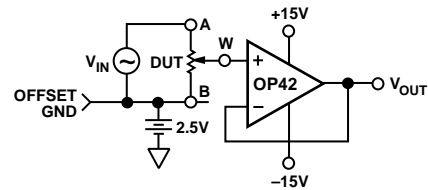


Figure 33. Gain vs. Frequency Test Circuit



Figure 30. Power Supply Sensitivity Test Circuit (PSS, PSRR)



Figure 34. Incremental ON Resistance Test Circuit

PROGRAMMING THE POTENTIOMETER DIVIDER**Voltage Output Operation**

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A Terminal to +5 V and B Terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across terminals AB divided by the 128-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(D) = D/128 \times V_{AB} + V_B \quad (1)$$

D represents the current contents of the internal UP/DOWN counter.

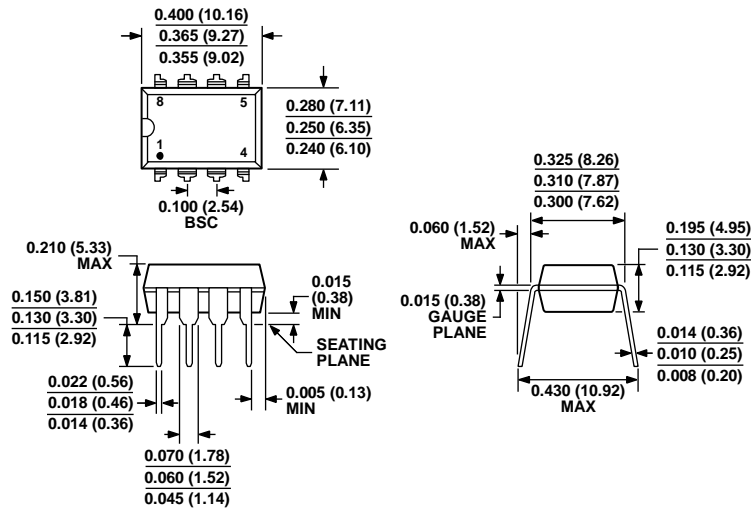
Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors, not the absolute value, therefore, the drift improves to 20 ppm/°C.

APPLICATIONS INFORMATION

The negative-edge sensitive CLK pin does not contain any internal debounce circuitry. This standard CMOS logic input responds to fast negative edges and needs to be debounced externally with an appropriate circuit designed for the type of switch closure device being used. Good performance results at the CLK input pin when the negative logic transition has a minimum slew rate of 1 V/μs. A wide variety of standard circuits can be used such as a one-shot multivibrator, Schmitt Triggered gates, cross coupled flip-flops, or RC filters to drive the CLK pin with uniform negative edges. This will prevent the digital potentiometer from skipping output codes while counting due to switch contact bounce.

AD5220

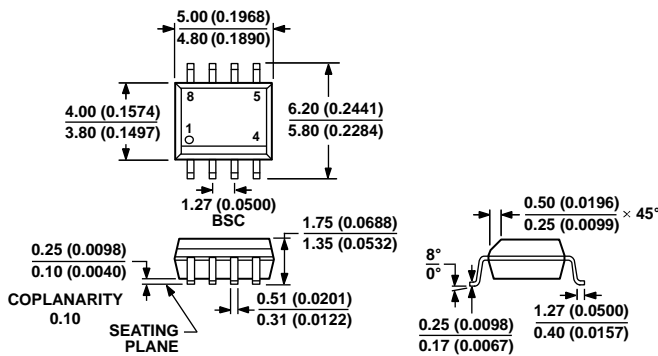
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 39. 8-Lead Plastic Dual In-Line Package [PDIP]
 Narrow Body
 (N-8)
 Dimensions shown in inches and (millimeters)

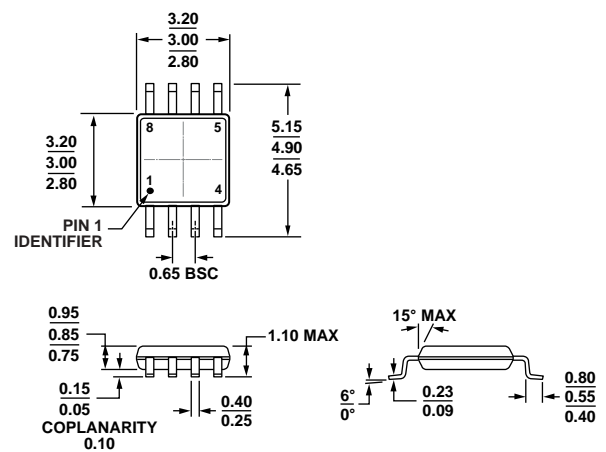
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COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)
 Dimensions in millimeters and (inches)

012407-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA
 Figure 41. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)
 Dimensions shown in millimeters

10-07-2009-B

ORDERING GUIDE

Model ^{1,2,3}	R _{AB} (kΩ)	Temperature Range	Package Description	Package Option	Branding
AD5220BNZ10	10	-40°C to +85°C	8-Lead PDIP	N-8	
AD5220BNZ100	100	-40°C to +85°C	8-Lead PDIP	N-8	
AD5220BNZ50	50	-40°C to +85°C	8-Lead PDIP	N-8	
AD5220BR10	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BR10-REEL7	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BR100	100	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BR100-REEL	100	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BR100-REEL7	100	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ10	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ10-REEL	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ10-REEL7	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220WBRZ10-REEL7	10	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ100	100	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ100-REEL7	100	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRZ50	50	-40°C to +85°C	8-Lead SOIC_N	R-8	
AD5220BRM100	100	-40°C to +85°C	8-Lead MSOP	RM-8	DQC
AD5220BRM100-REEL7	100	-40°C to +85°C	8-Lead MSOP	RM-8	DQC
AD5220BRMZ10	10	-40°C to +85°C	8-Lead MSOP	RM-8	D9H
AD5220BRMZ10-REEL7	10	-40°C to +85°C	8-Lead MSOP	RM-8	D9H
AD5220BRMZ100	100	-40°C to +85°C	8-Lead MSOP	RM-8	#DQC
AD5220BRMZ100-R7	100	-40°C to +85°C	8-Lead MSOP	RM-8	#DQC
AD5220BRMZ50	50	-40°C to +85°C	8-Lead MSOP	RM-8	#DQB
AD5220BRMZ50-RL7	50	-40°C to +85°C	8-Lead MSOP	RM-8	#DQB

¹ Z = RoHS Compliant Part.

² The AD5220 die size is 37 mil × 54 mil, 1998 sq mil; 0.938 mm × 1.372 mm, 1.289 sq mm. Contains 754 transistors. Patent Number 5495245 applies.

³ W = Qualified for Automotive Products.

AUTOMOTIVE PRODUCTS

The AD5220W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

REVISION HISTORY

12/10—Rev. 0 to Rev. A

Changes to Features Section	1
Updated Outline Dimensions	10
Changes to Ordering Guide	11
Added Automotive Products Section	11

10/98—Revision 0: Initial Version

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JONHON

«JONHON» (основан в 1970 г.)

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(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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