

GENERAL DESCRIPTION

This document describes specifications for the F1653NLGI I/Q Modulator implementing Zero-Distortion™ technology for low power consumption with improved ACLR. This device interfaces directly to a high performance dual DAC.

COMPETITIVE ADVANTAGE

In typical multi-mode, multi-carrier basestation transmitters the modulator has limited linearity and high power consumption which penalizes the system ACLR and system Power consumptions budgets in a Digital-Pre-Distortion environment.

The IDTF1653 is designed to eliminate these penalties by embedding Zero-Distortion™ technology into the device such that very high IP3 and IP2 are achieved with minimal current draw.

- Power consumption ↓**45%**
- IM3 Distortion ↓**14 dB**

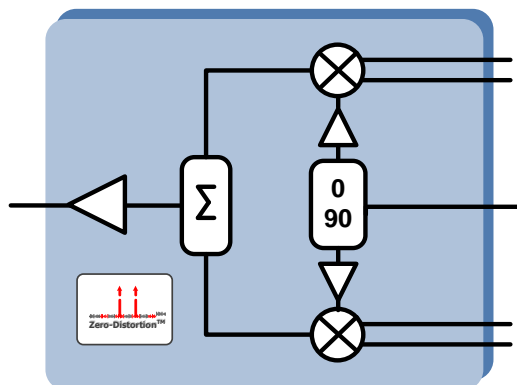
PART# MATRIX

| Part# | RF freq Range | IP2 _o | Power Cons. | IP3 _o | Noise |
|--------------|-------------------|------------------|---------------|------------------|--------------------|
| F1650 | 600 – 2400 | +60 dBm | 587 mW | +36 dBm | -158 dBm/Hz |
| F1653 | 600 – 2900 | +64 dBm | 587 mW | +36 dBm | -159 dBm/Hz |

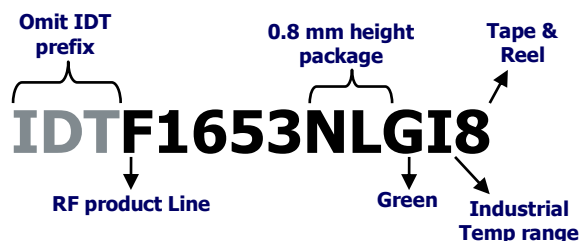
FEATURES

- Power Gain = 3dB
- Direct 100Ω differential drive from Tx DAC
- **< 590mW Power Consumption**
- -159 dBm/Hz Output Noise
- -161 dBc/Hz Internal LO Path Noise
- IP2_o = +64 dBm @ 2GHz
- **IP3_o = +36 dBm @ 2GHz**
- Excellent native LO and image suppression
- 600 MHz input 1dB Bandwidth
- 600 MHz to 2900 MHz RF BW
- **Fast Settling for TDD (< 200 nsec)**
- 3.3V Single Power Supply
- LO port can be driven single ended or differential
- 4mm x 4mm, 24-pin TQFN package

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION





ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| VDD to GND | -0.3V to +3.6V |
| STBY | -0.3V to (VDD + 0.3V) |
| BB_I+, BB_I-, BB_Q+, BB_Q- | -0.3V to 1.8V |
| LO_IN | -0.3V to 0.3V |
| RF_OUT | (VDD-0.35V) to (VDD-0.05V) |
| Continuous Power Dissipation | 1.5W |
| θ_{JA} (Junction – Ambient) | +45°C/W |
| θ_{JC} (Junction – Case) The Case is defined as the exposed paddle | +2.5°C/W |
| Operating Temperature Range (Case Temperature) | $T_{CASE} = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +260°C |

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability



IDTF1653 RECOMMENDED OPERATION CONDITIONS

| Parameter | Symbol | Comment | min | typ | max | units |
|-----------------------------------|------------|---|------|-------------|------|-------|
| Supply Voltage(s) | V_{DD} | All V_{DD} pins | 3.15 | 3.30 | 3.45 | V |
| Operating Temperature | T_{CASE} | Case Temperature | -40 | 25 | +105 | deg C |
| LO Freq Range | F_{LO} | LO power -3dBm to +5dBm | 600 | | 2900 | MHz |
| BB Common Mode Voltage | V_{CM} | <ul style="list-style-type: none">• $T_{CASE} = -40C$ to $+105C$• $V_{DD} = 3.3$ V• LO level = 0dBm | 0.1 | 0.25 | 0.8 | V |
| BB input voltage compliance range | | For each BB pin | 0 | | 1 | Vpeak |
| BB Freq Range | F_{BB} | <ul style="list-style-type: none">▪ $F_{LO} = 1950$ MHz, $BB_IQ = 200$ mVp-p▪ P_{RF} degrades < 1 dB | DC | | 600 | MHz |

IDTF1653 SPECIFICATION

See application circuit. Typical values are measured at $V_{DD} = +3.3V$, $F_{LO} = 1950$ MHz, $P_{LO} = 0$ dBm, $T_{CASE} = +25^{\circ}C$, STBY = GND, BB_IQ frequency = 49, 50 MHz, BB_I&Q levels = 200 mVp-p each (-13dBm and 14 dB backoff from 1V DAC compliance), I & Q = 0.250V common-mode bias unless otherwise noted.

| Parameter | Symbol | Comment | min | typ | max | units |
|------------------------------------|-------------------|--|-----------------------|------------|------------------------|----------|
| Logic Input High | V_{IH} | For STBY Pin | 1.07 | | | V |
| Logic Input Low | V_{IL} | For STBY Pin | | | 0.68 | V |
| Logic Current | I_{IH}, I_{IL} | For STBY Pin | -100 | | +1 | μA |
| Supply Current (ON) | I_{SUPP} | Total V_{DD} | | 178 | 190¹ | mA |
| Supply Current (STBY) | I_{STBY} | Total V_{DD} , STBY = V_{IH} | | 2.8 | 5 | mA |
| LO Power | P_{LO} | 600MHz to 2900MHz | -3 | | +5 | dBm |
| BB Input Resistance (Differential) | R_{BB} | Freq = 100 MHz | | 113 | | Ω |
| LO port Impedance | Z_{LO} | <ul style="list-style-type: none"> Single Ended (RL < -10dB) Can be driven differentially | | 50 | | Ω |
| RF port Impedance | Z_{RF} | Single Ended (RL < -10dB) | | 50 | | Ω |
| Power Gain | G | | 2.0 | 3.0 | 4.0 | dB |
| Output IP3 @ 850 MHz | IP3 _{O1} | LO = 800 MHz | | 37 | | dBm |
| Output IP3 @ 2.00 GHz | IP3 _{O2} | LO = 1950 MHz | 30 | 36 | | |
| Output IP3 @ 2.85 GHz | IP3 _{O3} | LO = 2800 MHz | | 31 | | |
| Output IP2 @ 850 MHz | IP2 _{O1} | LO = 800 MHz Differential baseband input | | 65 | | dBm |
| Output IP2 @ 2.00 GHz | IP2 _O | LO = 1950 MHz Differential baseband input | 58² | 64 | | |
| Output IP2 @ 2.85 GHz | IP3 _{O2} | LO = 2800 MHz Differential baseband input | | 63 | | |
| Turn on time | P_{ON} | STBY = low to 90% final output power | | 175 | | nsec |
| Turn off time | P_{OFF} | STBY = high to initial output power -30dB | | 26 | | |
| LO (Carrier) Suppression | LO_{supp} | Native, Uncorrected $F_{LO} = 1950$ MHz | | -39 | -30 | dBm |
| Sideband (Image) Suppression | SS | Native, Uncorrected $F_{LO} = 1950$ MHz Differential baseband input | | -34 | -30 | dBc |
| Output P1dB | P1dB _O | Output Compression | | 15 | | dBm |
| Output Noise | NSD | <ul style="list-style-type: none"> 10 MHz offset from LO BB I&Q levels = 0 V_{p,p} | -157 | -159 | | dBm/Hz |
| LO Path Noise (internal) | $\Phi_{N,LO}$ | +10 MHz offset | | -161 | | dBc/Hz |

SPECIFICATION NOTES:

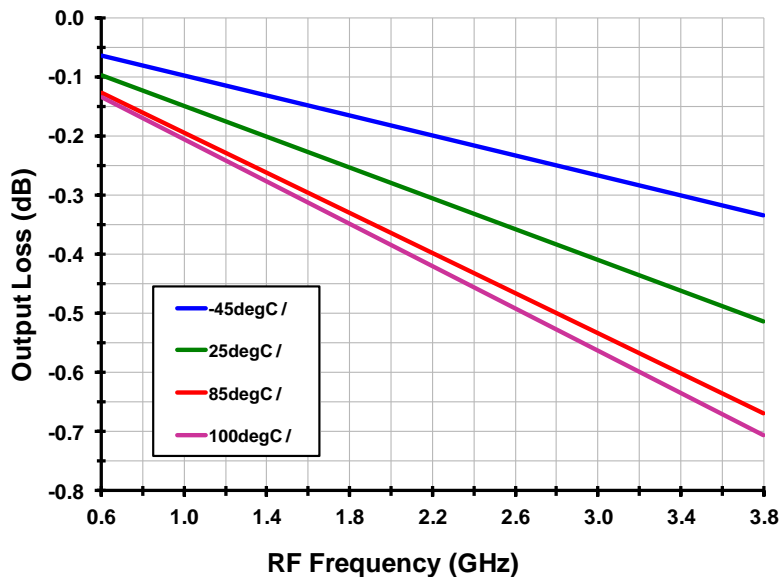
- 1 – Items in min/max columns in **bold italics** are Guaranteed by Test
- 2 – All other Items in min/max columns are Guaranteed by Design Characterization

TYPICAL OPERATING CONDITIONS GRAPHS

Unless otherwise noted, the following conditions apply:

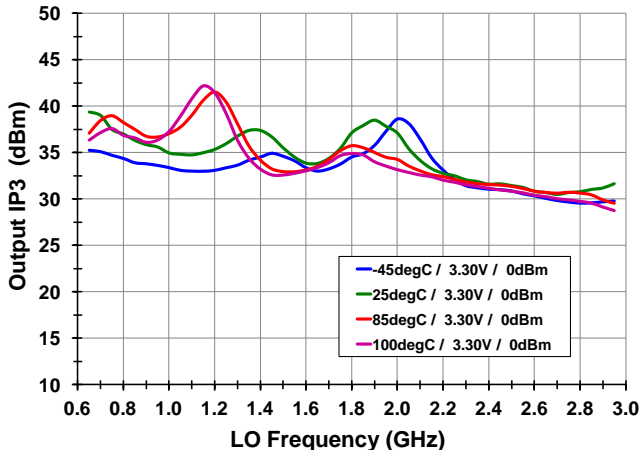
- Baseband I&Q levels = 200 mV_{PP} each (-13 dBm / Channel / Tone)
- Baseband I&Q tones = 49, 50 MHz
- Low Side Injection
- T_{AMB} = 25C, V_{CC} = 3.30 V, LO Power = 0 dBm
- V_{CM} = 0.250 Volts
- Flo = 1.95GHz unless otherwise specified
- EVKit RF output Trace and Connector Losses De-Embedded

EVkit RF output loss (Trace + Connector)

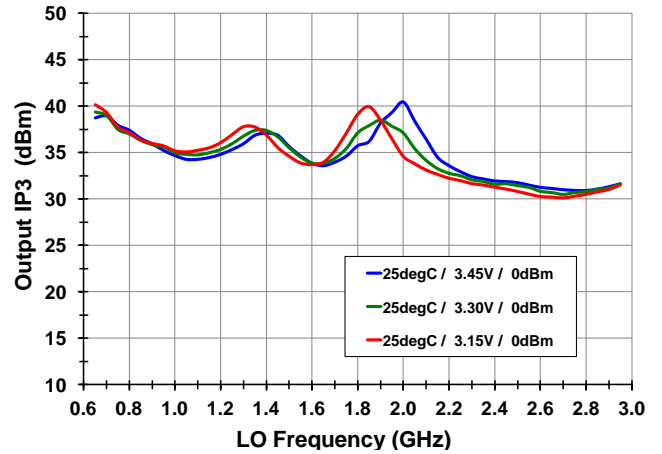


TYPICAL OPERATING CONDITIONS (-1-)

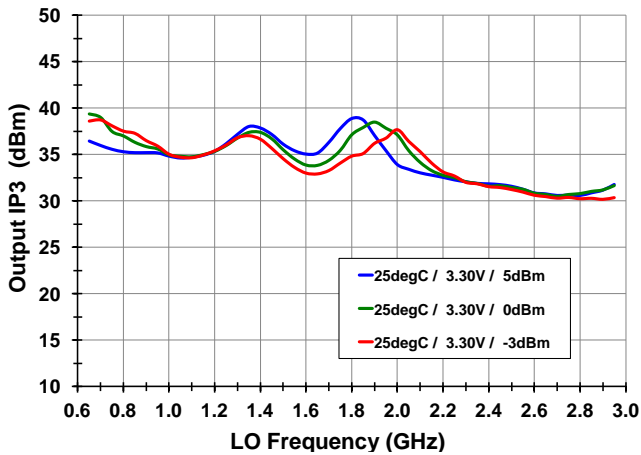
OIP3 vs. T_{AMB}



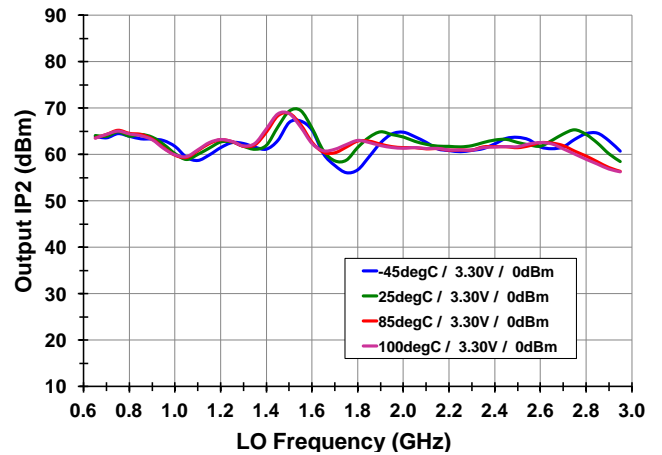
OIP3 vs. V_{CC}



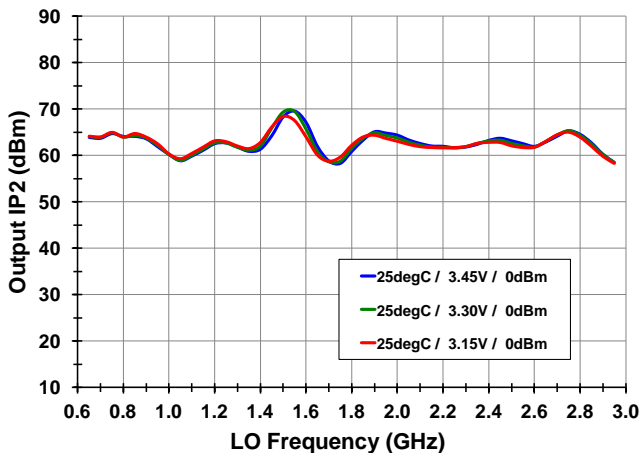
OIP3 vs. LO level



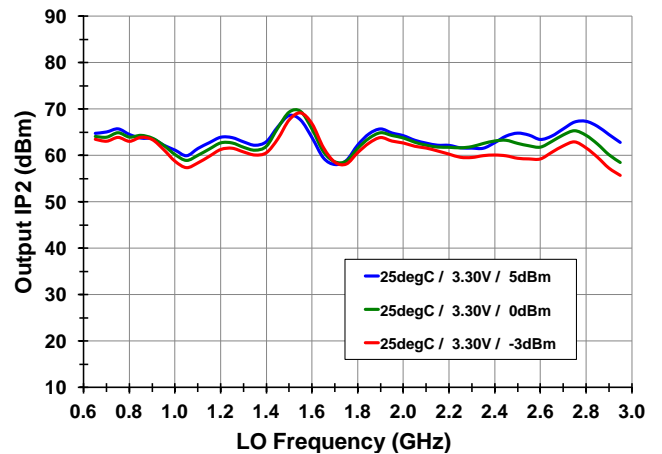
OIP2 vs. T_{AMB}



OIP2 vs. V_{CC}

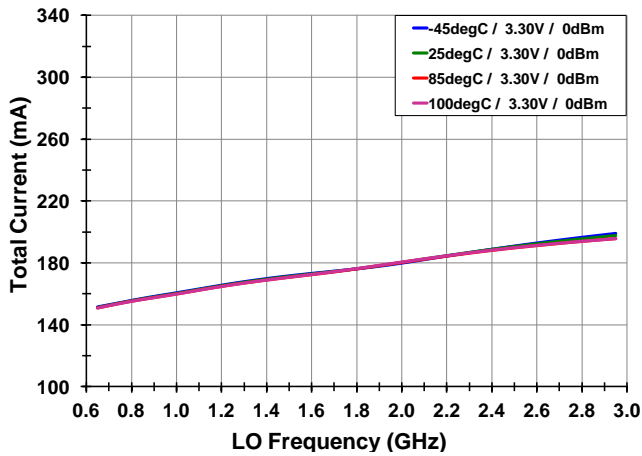


OIP2 vs. LO level

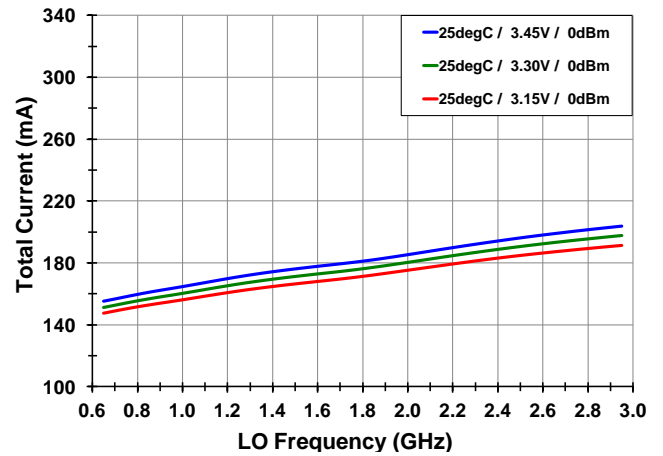


TYPICAL OPERATING CONDITIONS (-2-)

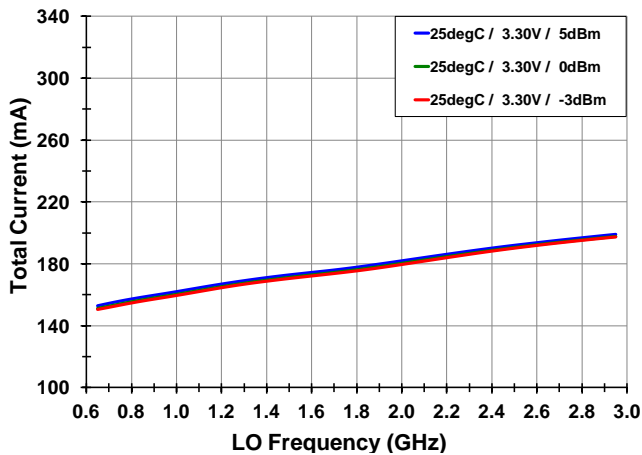
I_{CC} vs. T_{AMB}



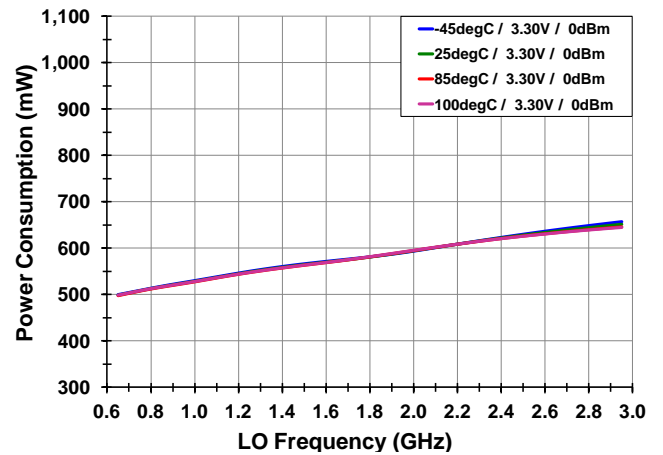
I_{CC} vs. V_{CC}



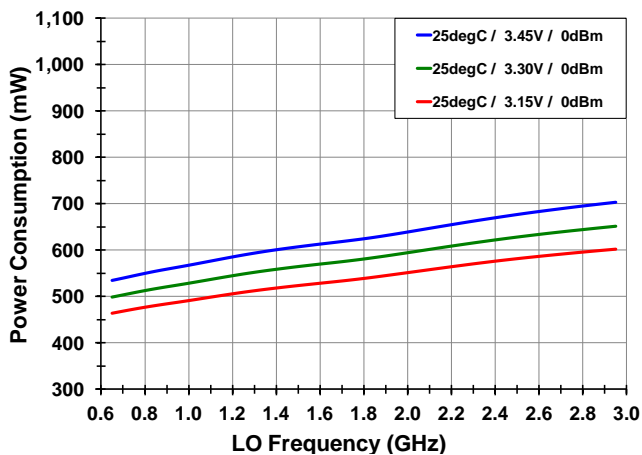
I_{CC} vs. LO level



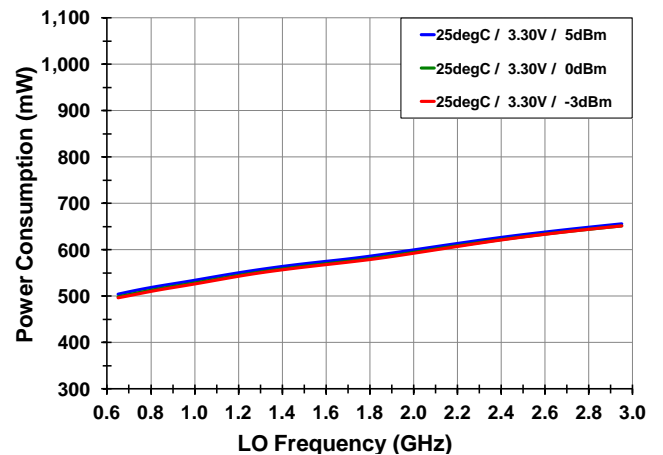
Power Consumption vs. T_{AMB}



Power Consumption vs. V_{CC}

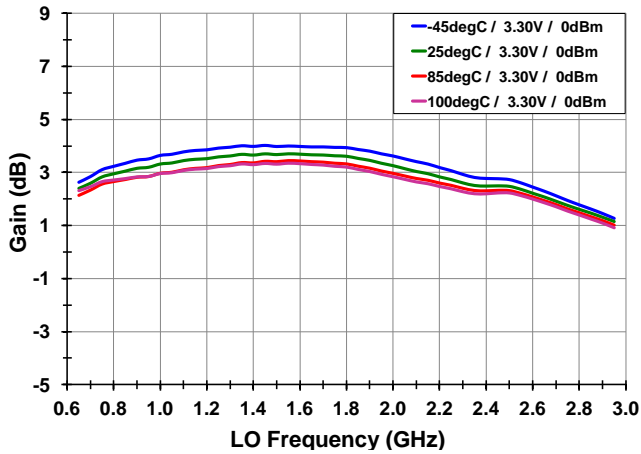


Power Consumption vs. LO level

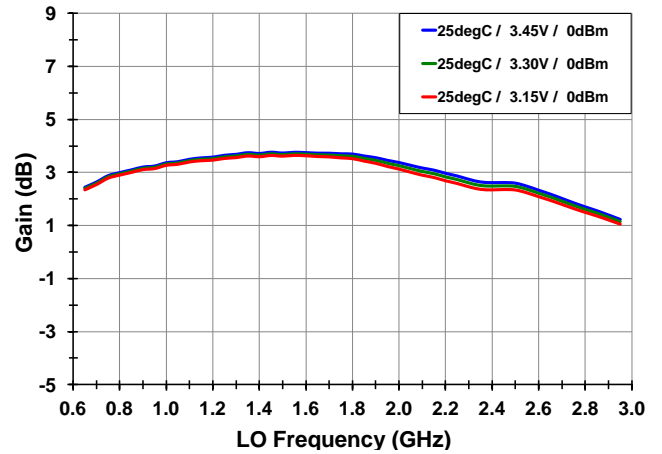


TYPICAL OPERATING CONDITIONS (-3-)

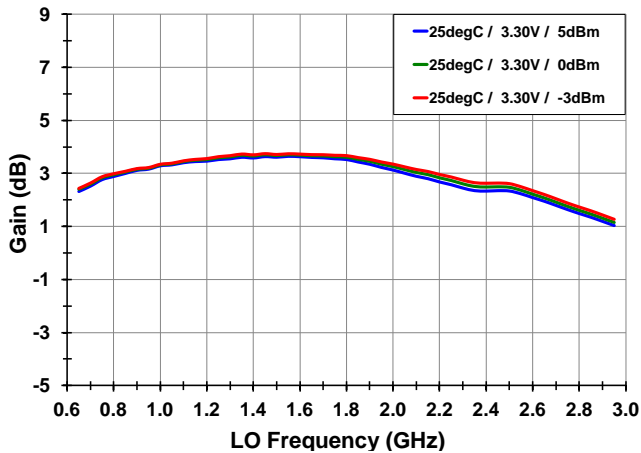
Gain vs. T_{AMB}



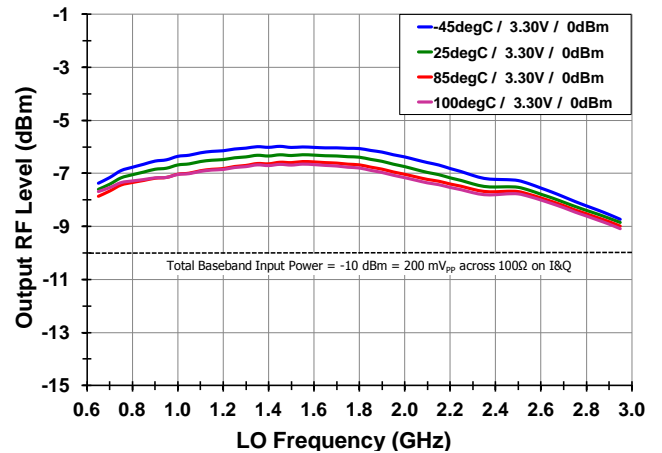
Gain vs. V_{CC}



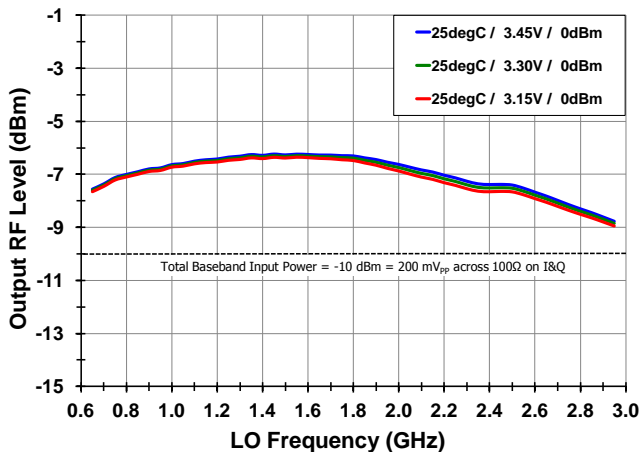
Gain vs. LO level



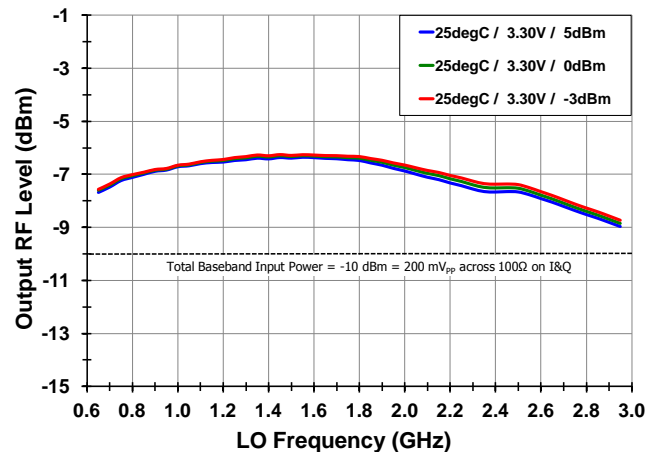
RF Output Power vs. T_{AMB}



RF Output Power vs. V_{CC}

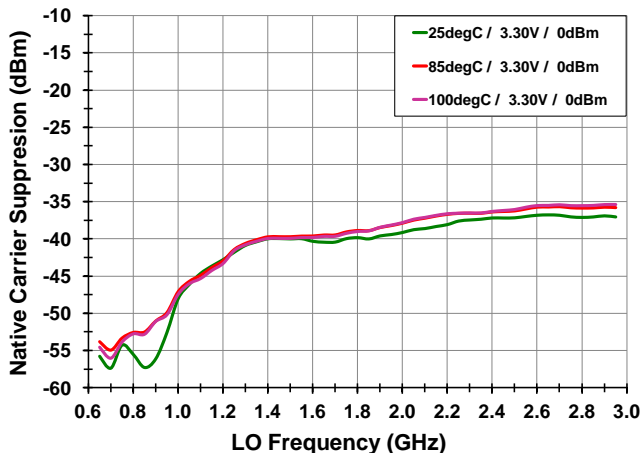


RF Output Power vs. LO level

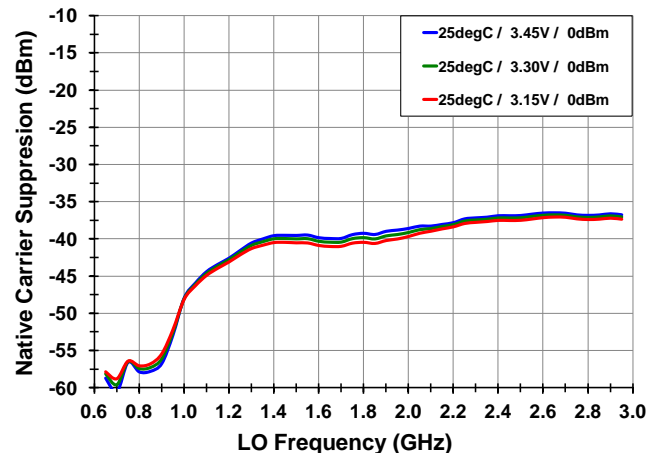


TYPICAL OPERATING CONDITIONS (-4-)

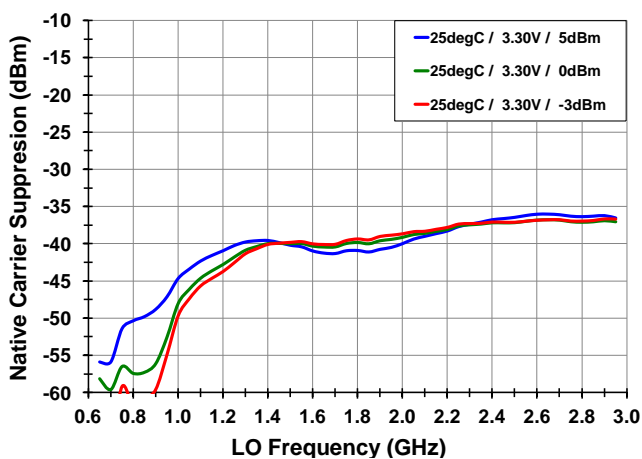
Unadjusted LO Suppression vs. T_{AMB}



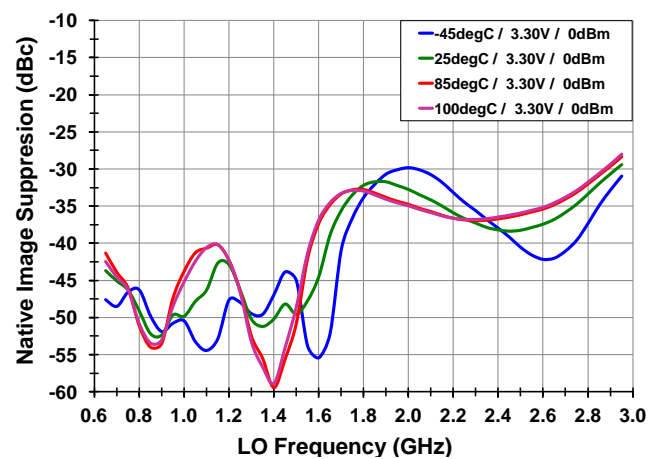
Unadjusted LO Suppression vs. V_{CC}



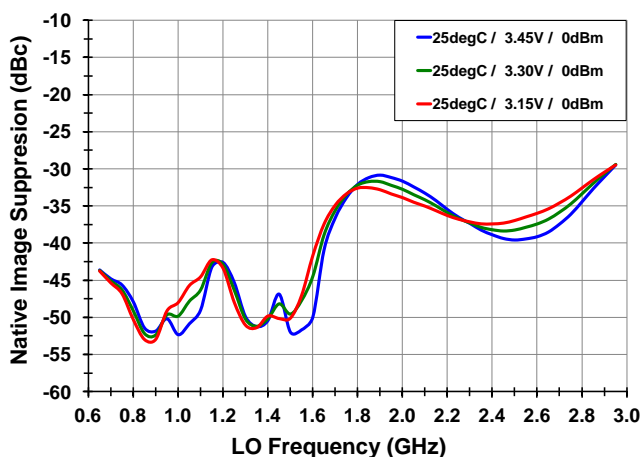
Unadjusted LO Suppression vs. LO level



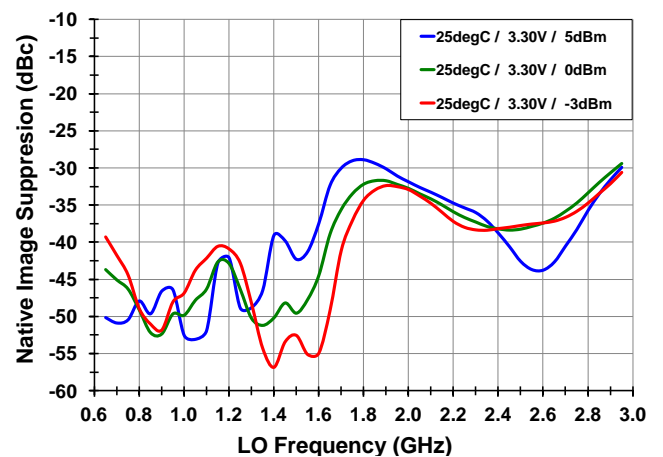
Unadjusted Sideband Suppression vs. T_{AMB}



Unadjusted Sideband Suppression vs. V_{CC}

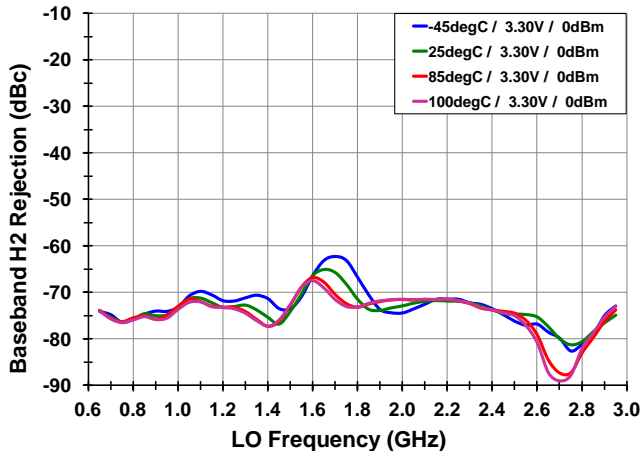


Unadjusted Sideband Suppression vs. LO level

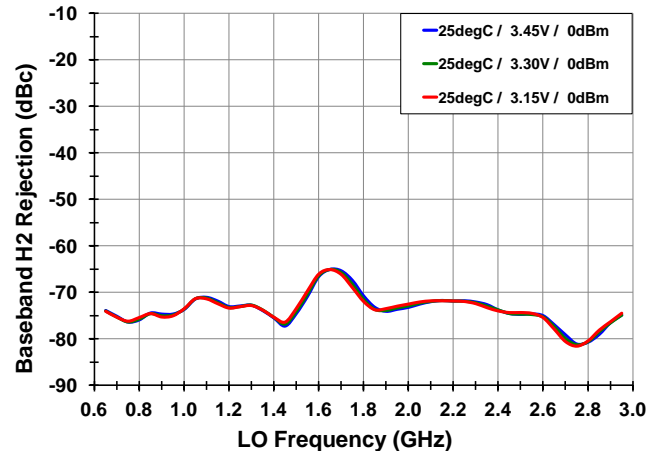


TYPICAL OPERATING CONDITIONS (-5-)

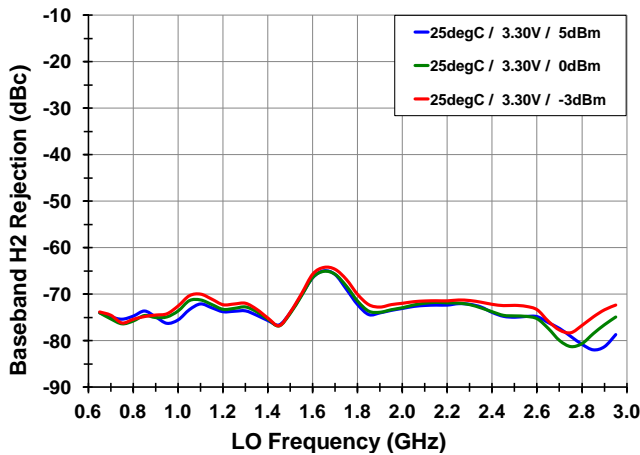
Baseband 2nd Harmonic vs. T_{AMB}



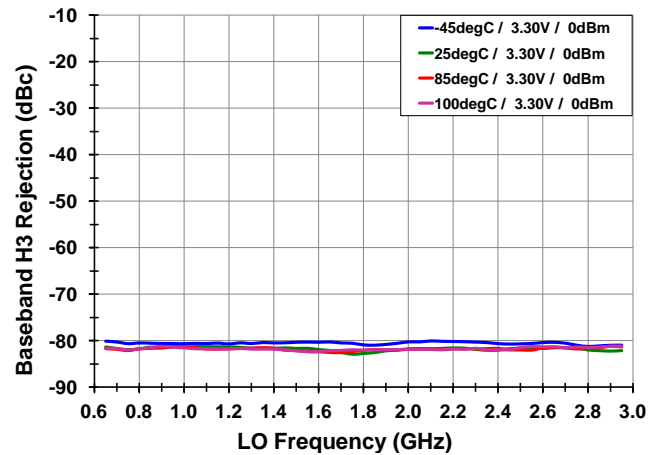
Baseband 2nd Harmonic vs. V_{CC}



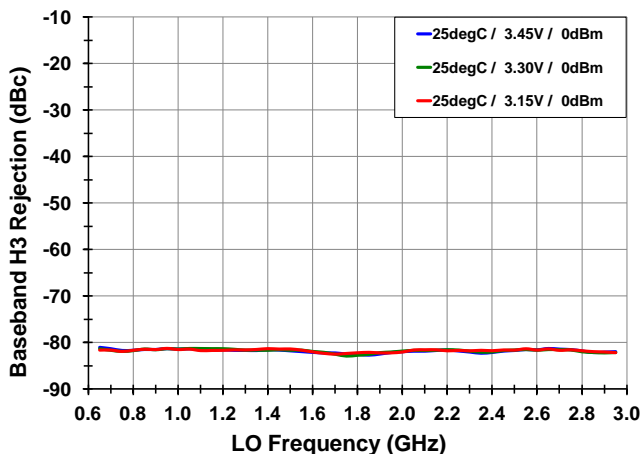
Baseband 2nd Harmonic vs. LO level



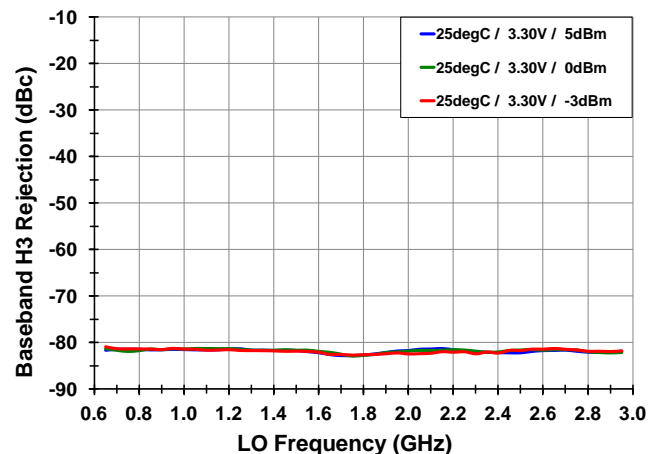
Baseband 3rd Harmonic vs. T_{AMB}



Baseband 3rd Harmonic vs. V_{CC}

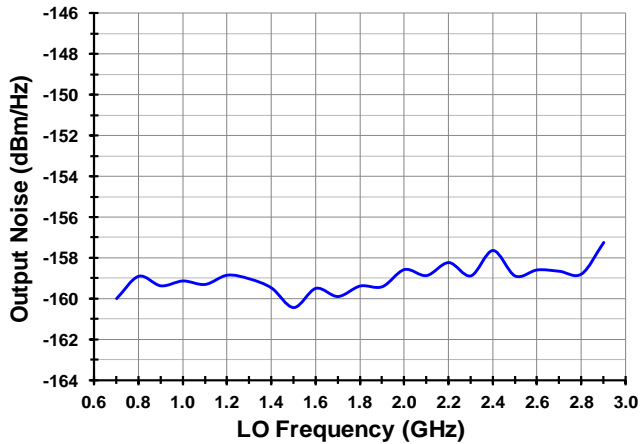


Baseband 3rd Harmonic vs. LO level

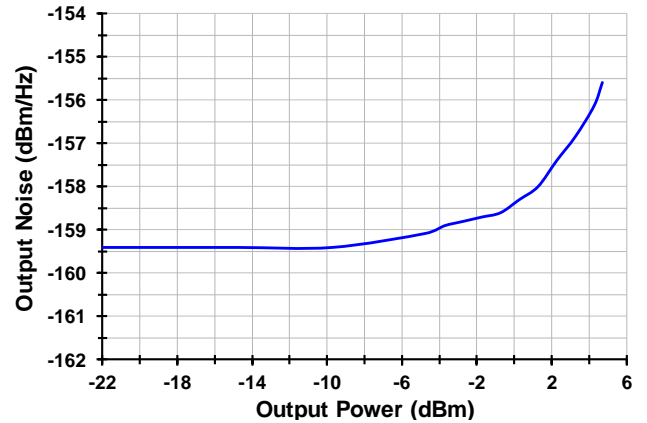


TYPICAL OPERATING CONDITIONS (-6-)

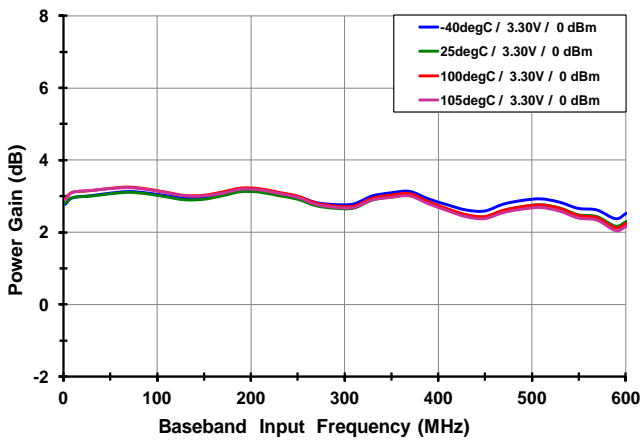
Output Noise vs. Frequency



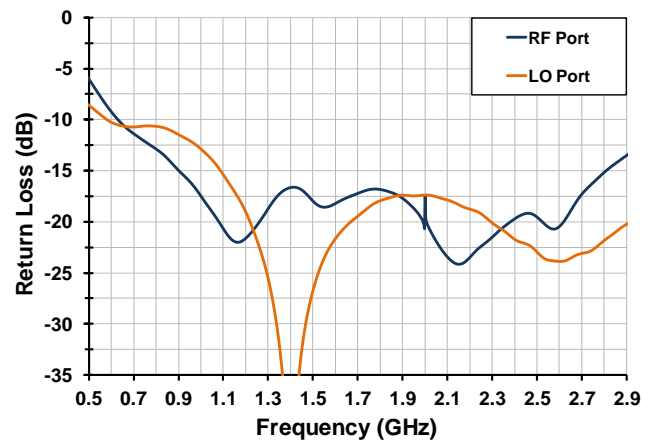
Output Noise vs. P_{OUT} [V_{CC} = 3.3V, T_{AMB} = 25C]



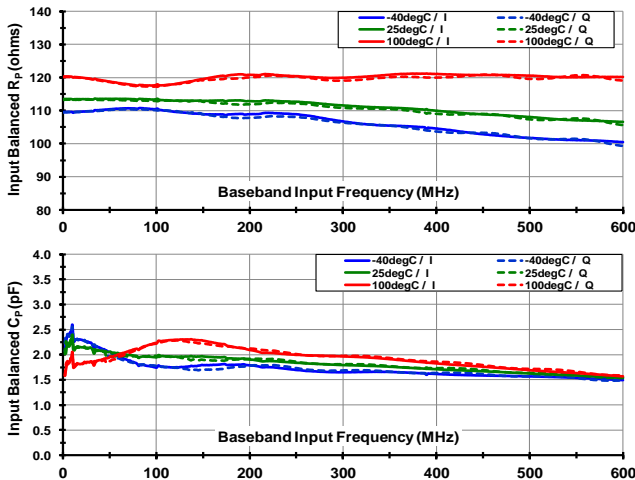
Input Bandwidth (fixed LO = 2.092 GHz)



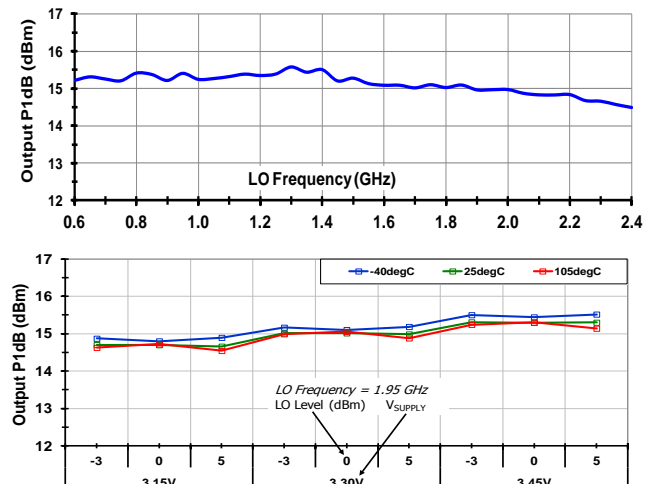
LO & RF Port Return Loss



I&Q Input Parallel Resistance/Capacitance

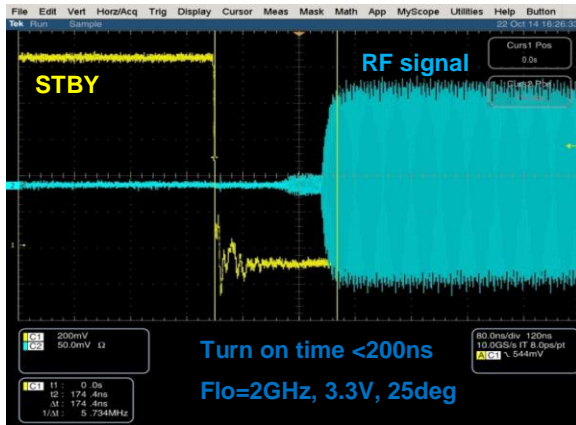


1dB Compression

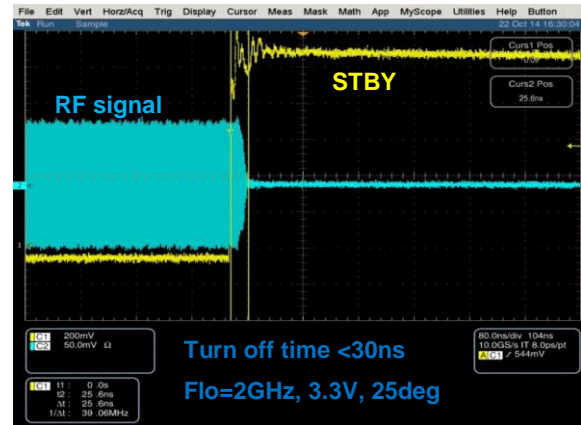


TYPICAL OPERATING CONDITIONS (-7-)

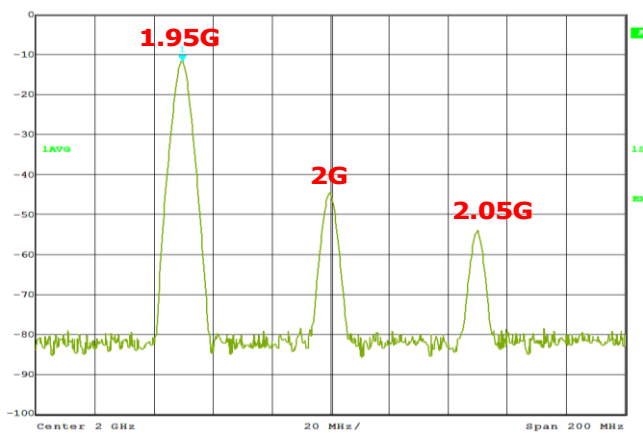
Turn On Time



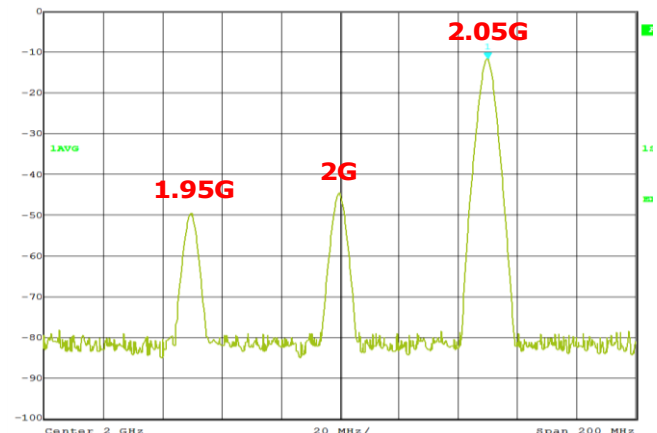
Turn Off Time



Polarity: LO = 2.0GHz, BB_I+/- leads BB_Q+/-



Polarity: LO = 2.0GHz, BB_I+/- lags BB_Q+/-



Carrier Suppression Nulling Performance

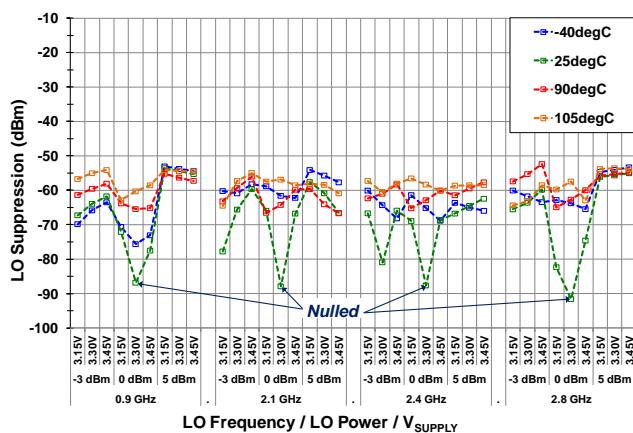
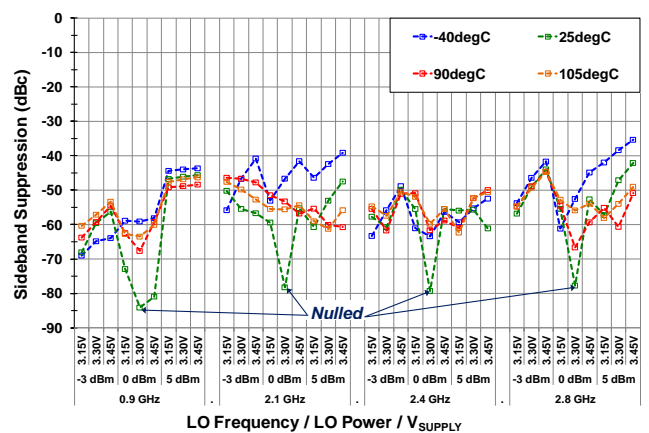
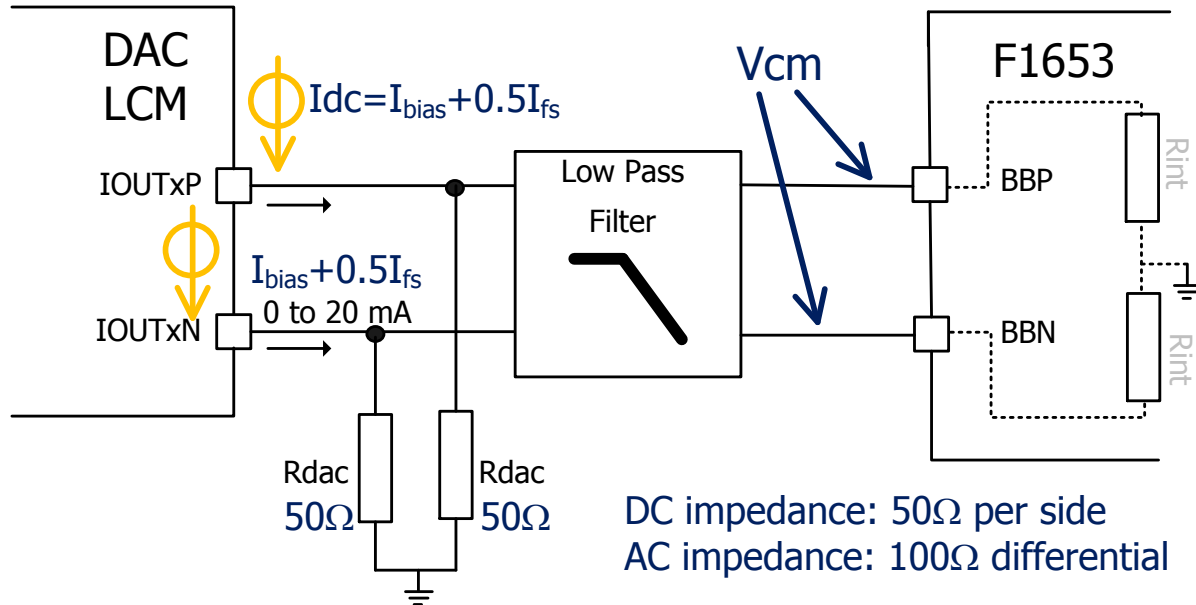


Image Suppression Nulling Performance

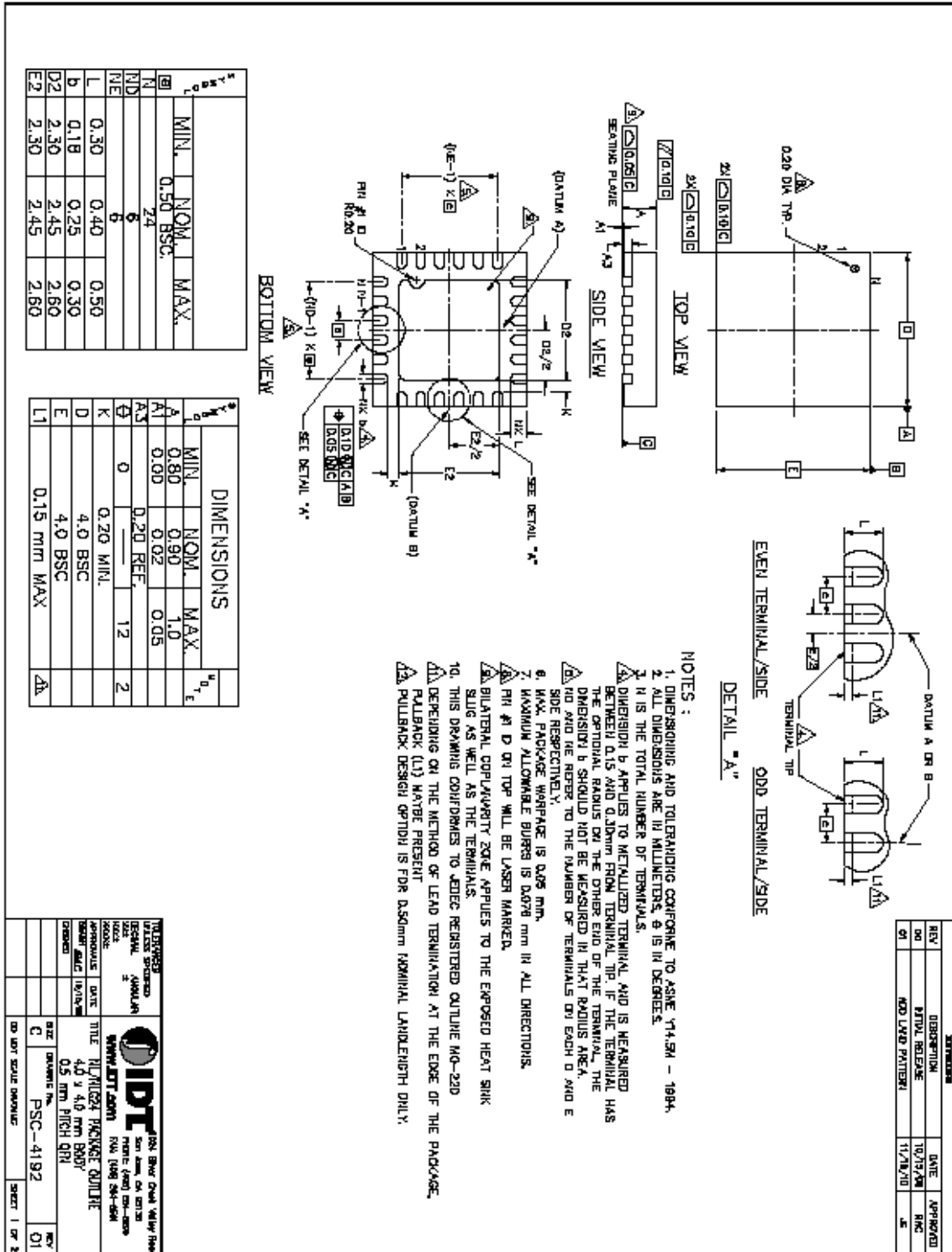


GENERIC DAC INTERFACE



- LCM DAC: low common mode voltage DAC usually has high output impedance and sourcing current out
- LPF: to filter out unwanted harmonics
- DC common mode voltage on BBP/BBN V_{cm} : $V_{cm} = I_{DC} \times R_{dac} // R_{dc_IQMOD}$
- V_{cm} is determined by DAC bias current and IQ Mod input DC impedance

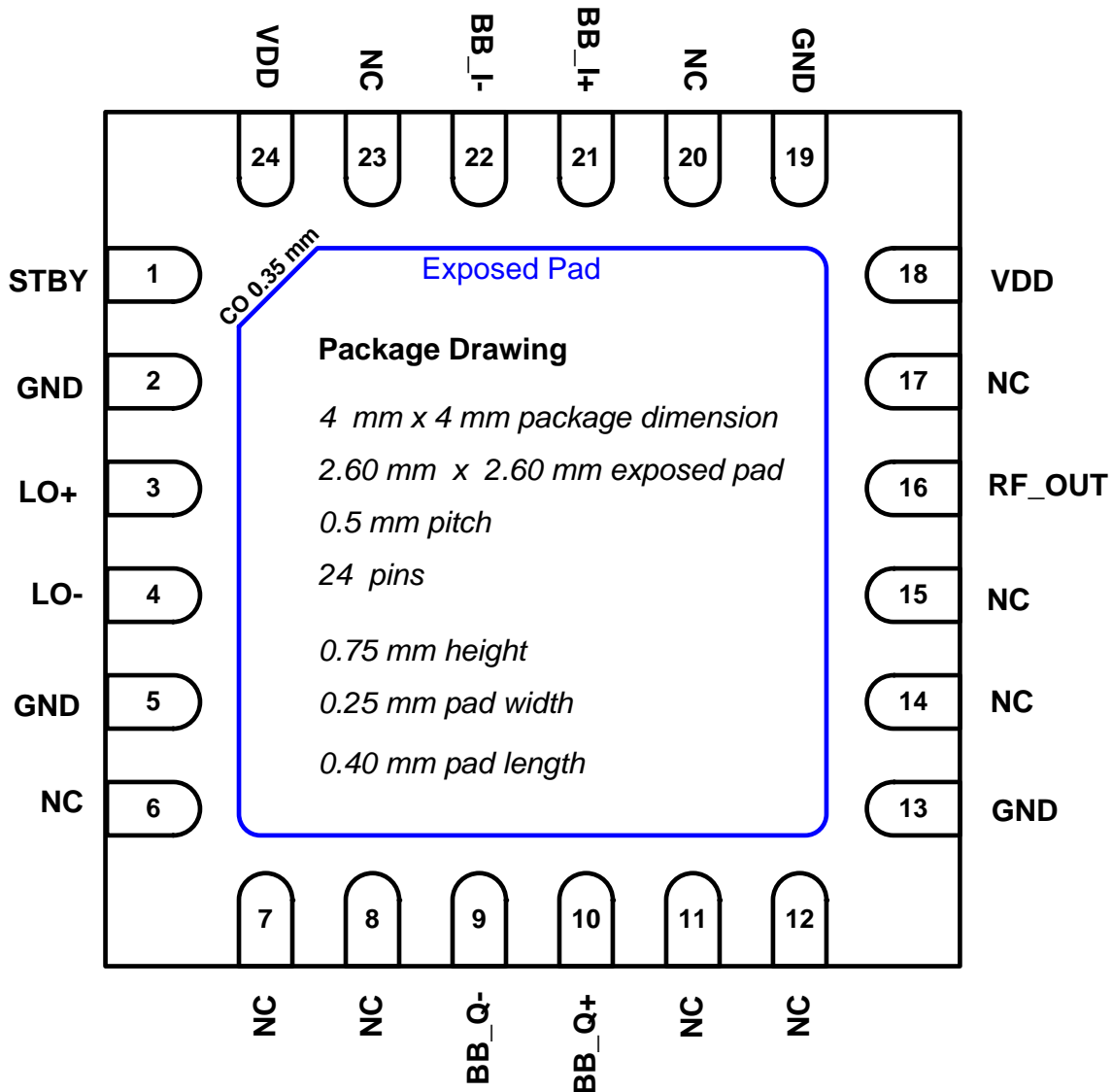
PACKAGE DRAWING (4x4 24 PIN)



PIN DIAGRAM

TOP View

(looking through the top of the package)

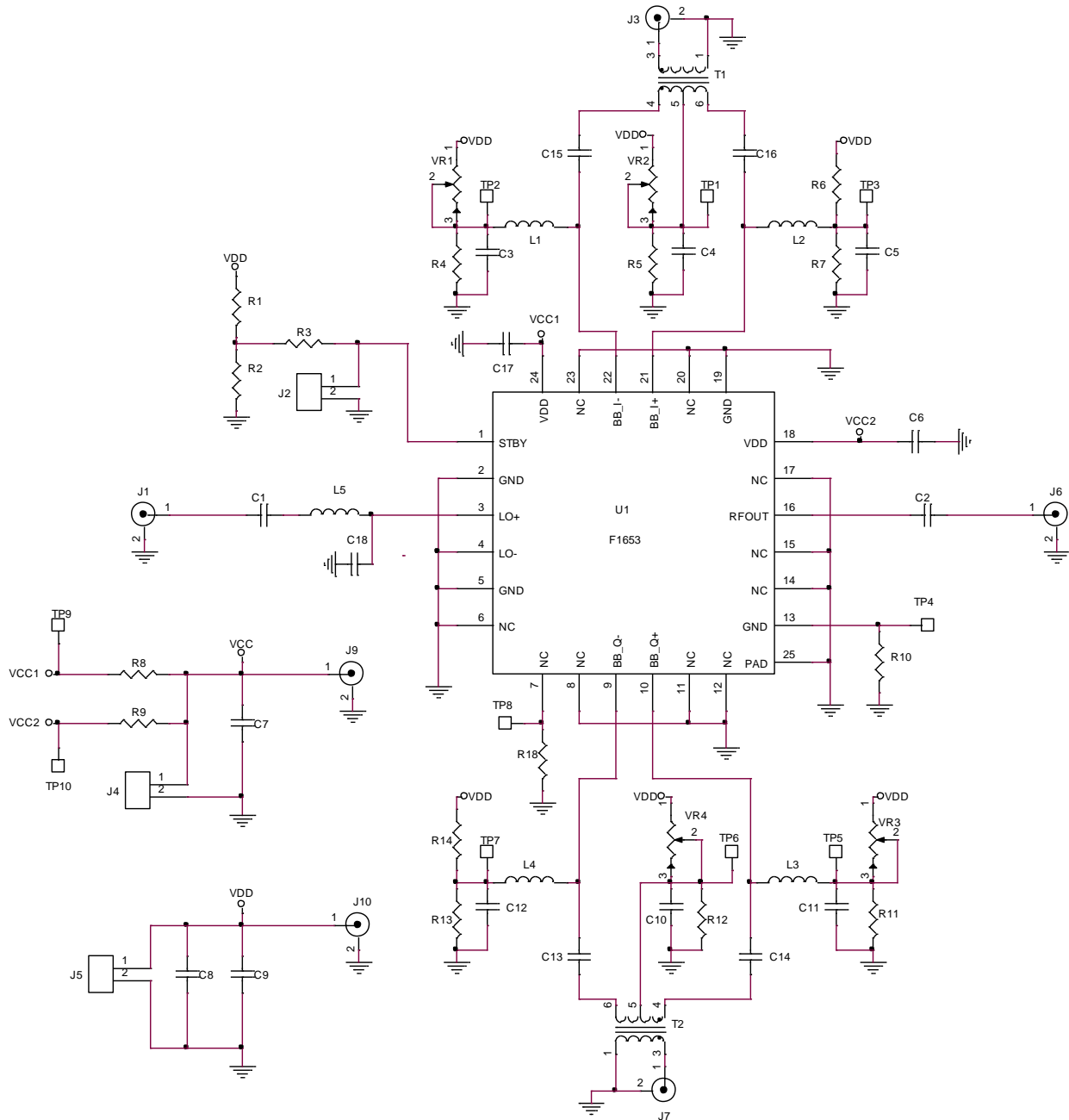




PIN DESCRIPTIONS

| Pins | Name | Function |
|-------------------------------------|--------------|--|
| 1 | STBY | STBY Mode. Pull this pin high for Standby Mode. Pull low or ground for Normal Operation. |
| 2, 5, 13, 19 | GND | Ground these pins. |
| 6, 7, 8, 11, 12, 14, 15, 17, 20, 23 | NC | IDT recommends grounding these pins. |
| 3, 4 | LO+, LO- | Local oscillator (LO) 50 ohm differential or 25ohm each pin single-ended input. Pins must be ac-coupled. For 50 ohm single-ended operation, ac-couple USED Pin to 50 ohm termination and ac-couple UNUSED pin to GND. |
| 9, 10 | BB_Q-, BB_Q+ | <i>Quadrature</i> differential baseband input. Internally matched to 100 ohms. |
| 16 | RF_OUT | RF output. Must be ac-coupled. |
| 18, 24 | VDD | Power Supply. Bypass to GND with capacitors as shown in the Typical Application Circuit as close to pin as possible. |
| 21, 22 | BB_I+, BB_I- | <i>In-Phase</i> differential baseband input. Internally matched to 100 ohms. |
| | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance. |

EVKIT SCHEMATIC



POWER SUPPLIES

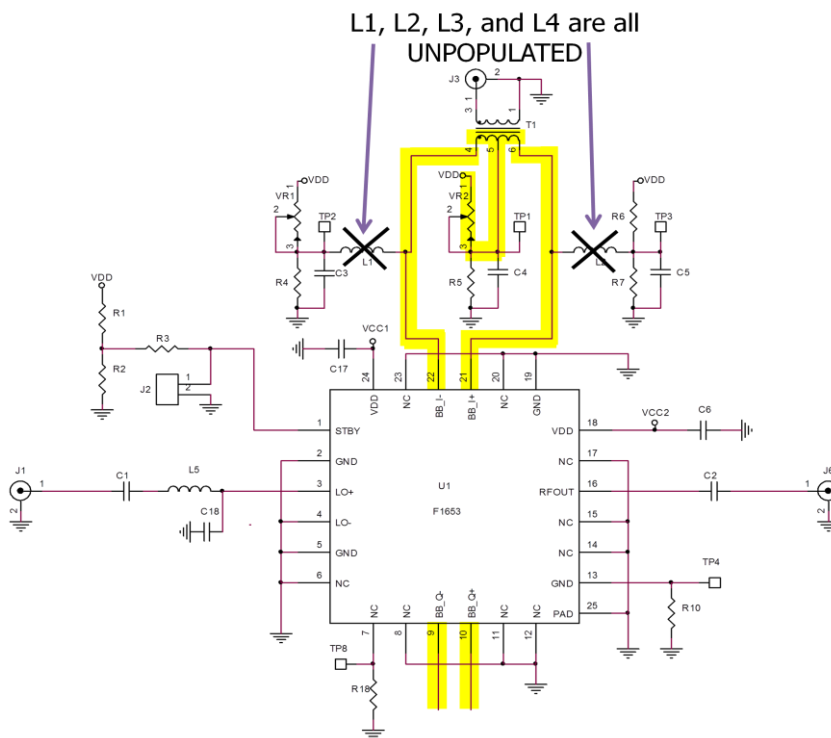
All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1V/20\mu s$. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

EVKIT BOM

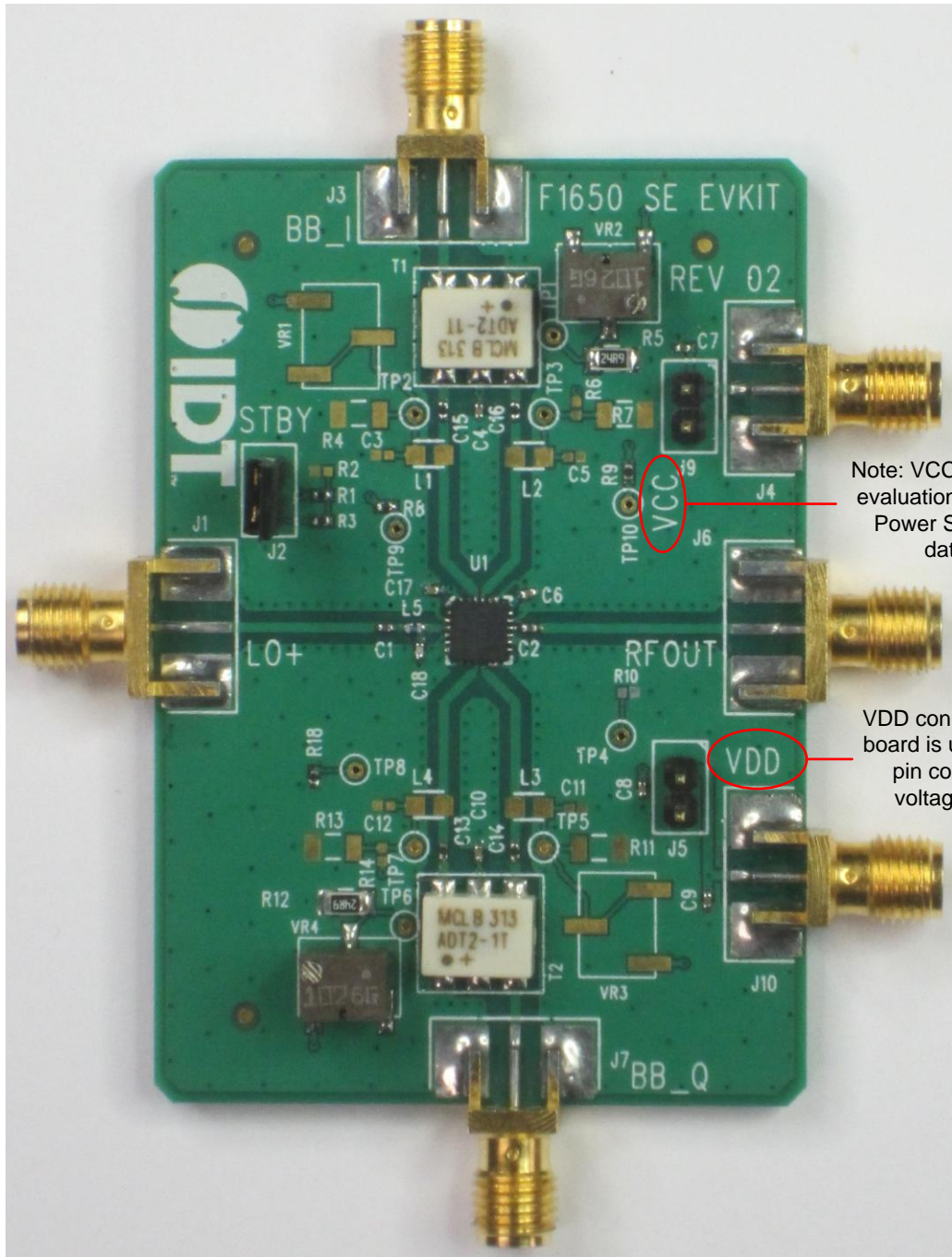
| Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|---------------------|-----|--|-------------------------|-----------------------|
| C2 | 1 | 8pF ±0.5pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H8R0D | MURATA |
| C4,C6,C8,C10,C17 | 5 | 10nF ±10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71C103K | MURATA |
| C1 | 1 | 39PF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H390J | MURATA |
| C7,C9 | 2 | 100nF ±10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71C104K | MURATA |
| R3,R8,R9,C13-C16,L5 | 8 | 0Ω 1/10W Resistor (0402) | ERJ-2GE0R00X | Panasonic |
| R5,R12 | 2 | 24.9 Ω ±1%, 1/4W Resistor (1206) | RMCF1206FT24R9 | Stackpole Electronics |
| R1 | 1 | 47.0KΩ ±1%, 1/16W Resistor (0402) | RC0402FR-0747KL | Yageo |
| VR2,VR4 | 2 | 1KΩ ±10%, 1/4W Resistor Trimmer | TS63Y102KR10 | Vishay/Sfernice |
| J2,J5,J8,J9 | 4 | CONN HEADER VERT SGL 2 X 1 POS GOLD | 961102-6404-AR | 3M |
| J3,J4,J7,J10 | 4 | Edge Launch SMA (0.250 inch width, round center contact) | 142-0711-821 | Emerson Johnson |
| J1,J6 | 2 | Edge Launch SMA (0.375 inch width, flat center contact) | 142-0701-851 | Emerson Johnson |
| T1,T2 | 2 | 2:1 Center Tap Balun | ADT2-1T+ | Mini Circuits |
| U1 | 1 | IQ MOD | F1653 | IDT |
| | 1 | Printed Circuit Board | F1650 SE EVKIT REV (02) | Coastal Circuits |
| VR1,VR3 | | DNP | | |
| C3,C5,C11,C12,C18 | | DNP | | |
| L1,L2,L3,L4 | | DNP | | |
| R2,R4,R6,R7,R10,R11 | | DNP | | |
| R13,R14,R16,R18 | | DNP | | |

APPLYING V_{CM} AT THE BASEBAND INPUTS

With L1, L2, L3, and L4 unpopulated, the common mode voltage is set by VR2 and VR4. The voltage set by VR2 has a DC path through the balun transformer T1 to pins BB_{I+} and BB_{I-}, as highlighted. This also applies for VR4, T2, and pins BB_{Q+} and BB_{Q-}. With this configuration, the same voltage will be applied to BB_{I+} and BB_{I-} and the same voltage will be applied to BB_{Q+} and BB_{Q-}. The I and Q common mode voltages may be different from each other to null LO (carrier) leakage.



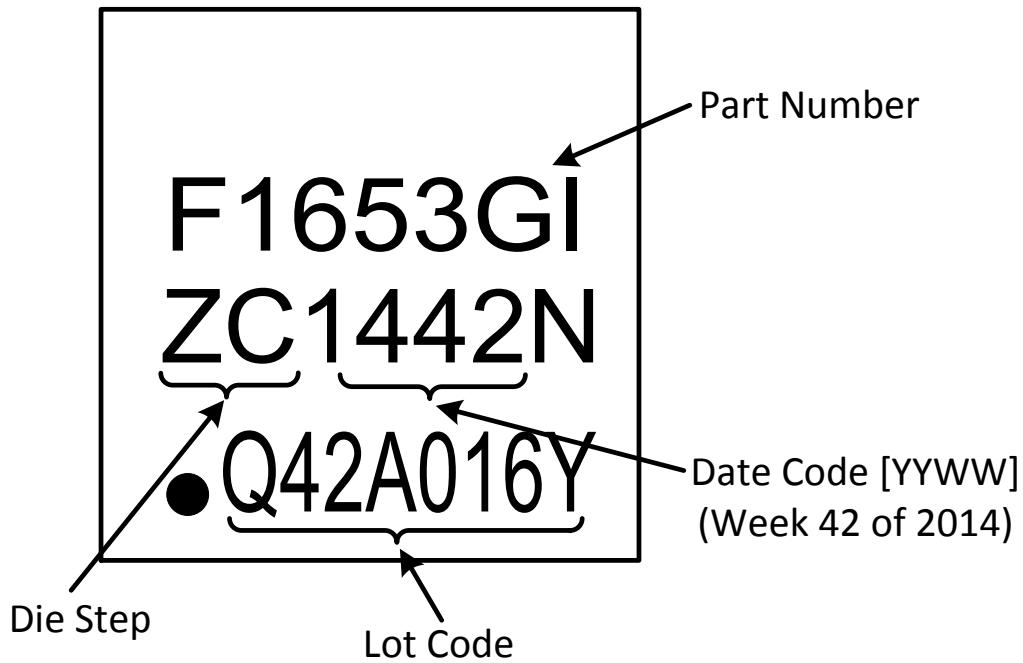
EVKIT PICTURE:



Note: VCC connection on evaluation board is VDD Power Supply on the datasheet.

VDD connection on evaluation board is used to set baseband pin common mode (CM) voltage (see schematic)

TOP MARKINGS



Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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