Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

February 2016

FDMC8588DC

N-Channel Dual Cool^{TM} 33 PowerTrench® MOSFET

25 V, 40 A, 5.7 mΩ

Features

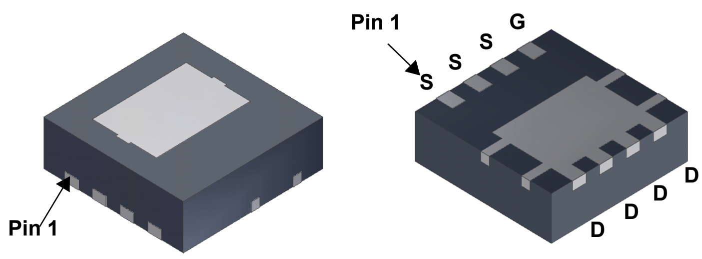
- Dual Cool^{TM} Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 5.7 mΩ at V_{GS} = 4.5 V, I_D = 17 A
- State-of-the-art switching performance
- Lower output capacitance, gate resistance, and gate charge boost efficiency
- Shielded gate technology reduces switch node ringing and increases immunity to EMI and cross conduction
- RoHS Compliant

General Description

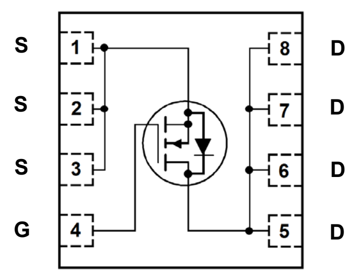
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- High side switching for high end computing
- High power density DC-DC synchronous buck converter



Top   Dual Cool^{TM} 33   Bottom



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage (Note 5)	25	V
V_{GS}	Gate to Source Voltage (Note 4)	±12	V
I_D	Drain Current - Continuous (Package limited) T_C = 25 °C	40	A
	- Continuous (Silicon Limited) T_C = 25 °C	73	
	- Continuous (Note 1a)	17	
	- Pulsed	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	29	mJ
P_D	Power Dissipation T_C = 25 °C	41	W
	Power Dissipation T_A = 25 °C (Note 1a)	3.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	7.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	3.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
08DC	FDMC8588DC	Dual Cool^{TM} 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

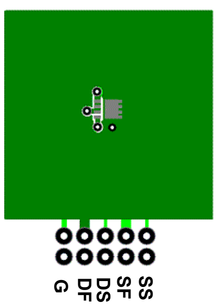
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA , V_{GS} = 0 V	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA , referenced to 25 °C		5		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.8	1.2	1.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA , referenced to 25 °C		-4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 18 A		3.6	5.0	mΩ
		V_{GS} = 4.5 V, I_D = 17 A		4.1	5.7	
		V_{GS} = 10 V, I_D = 18 A, T_J = 125 °C		5.5	7.6	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 17 A		103		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHz		1695		pF
C_{oss}	Output Capacitance			493		pF
C_{rss}	Reverse Transfer Capacitance			63		pF
R_g	Gate Resistance			0.4		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 13 V, I_D = 17A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8		ns
t_r	Rise Time			3		ns
$t_{d(off)}$	Turn-Off Delay Time			25		ns
t_f	Fall Time			2		ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	V_{DD} = 13 V, I_D = 17 A		12		nC
Q_{gs}	Total Gate Charge			3.0		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.0		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 17 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 17 A, di/dt = 100 A/μs		25		ns
Q_{rr}	Reverse Recovery Charge			10		nC

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	7.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	3.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	16	

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 105 °C/W when mounted on a minimum pad of 2 oz copper

c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

g. 200FPM Airflow, No Heat Sink,1 in^2 pad of 2 oz copper

h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 29 mJ is based on starting T_J = 25 °C, L = 1.2 mH, I_{AS} = 7 A, V_{DD} = 23 V, V_{GS} = 10V. 100% tested at L = 0.1 mH, I_{AS} = 16 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
5. The continuous Vds rating is 25V; however, a pulse of 28 V peak voltage for no longer than 3ns duration at 500KHz frequency can be applied.

Typical Characteristics T_J = 25°C unless otherwise noted

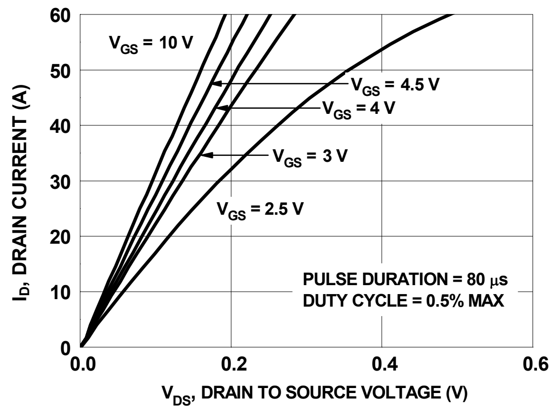


Figure 1. On Region Characteristics

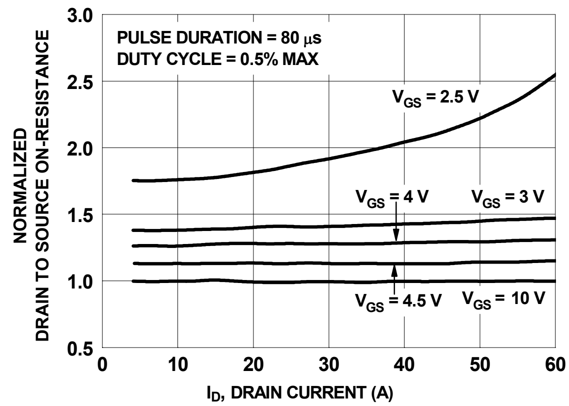


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

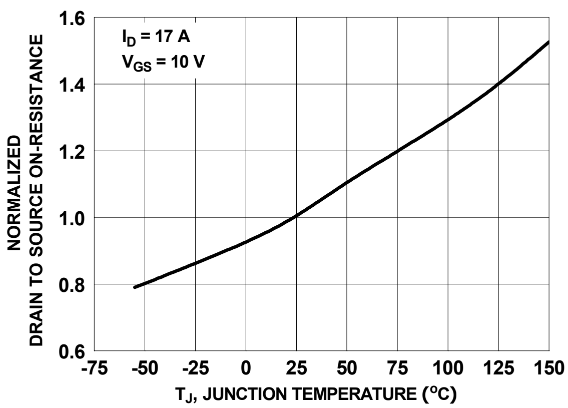


Figure 3. Normalized On Resistance vs Junction Temperature

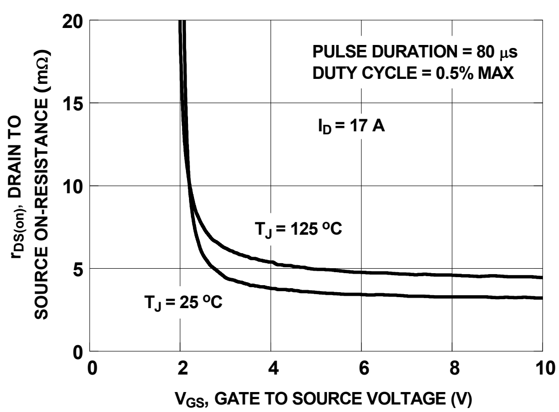


Figure 4. On-Resistance vs Gate to Source Voltage

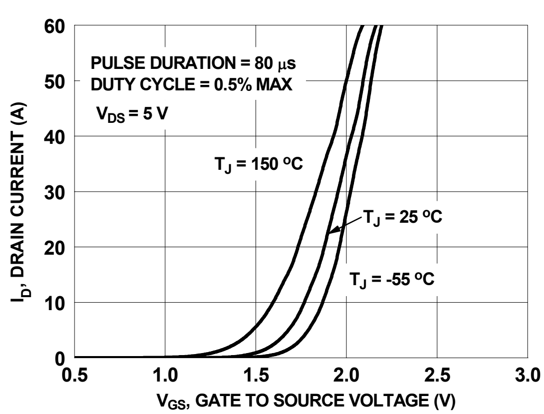


Figure 5. Transfer Characteristics

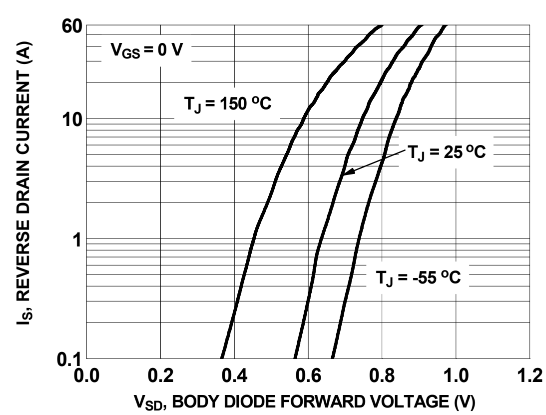


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

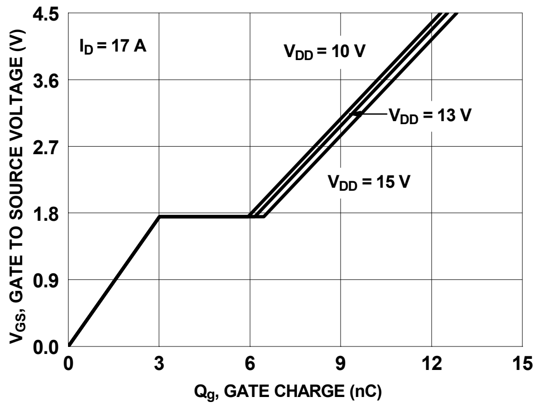


Figure 7. Gate Charge Characteristics

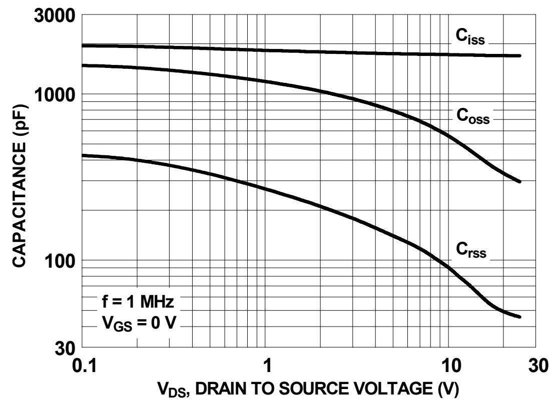


Figure 8. Capacitance vs Drain to Source Voltage

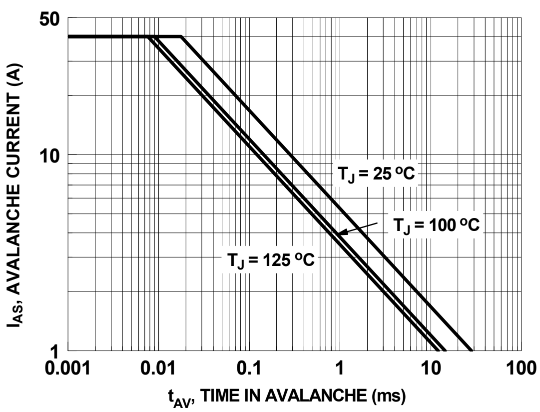


Figure 9. Unclamped Inductive Switching Capability

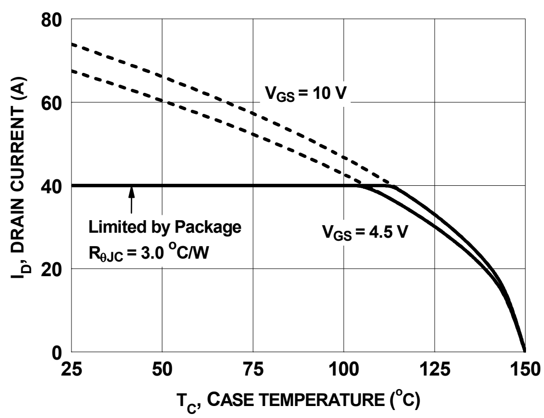


Figure 10. Maximum Continuous Drain Current vs Case Temperature

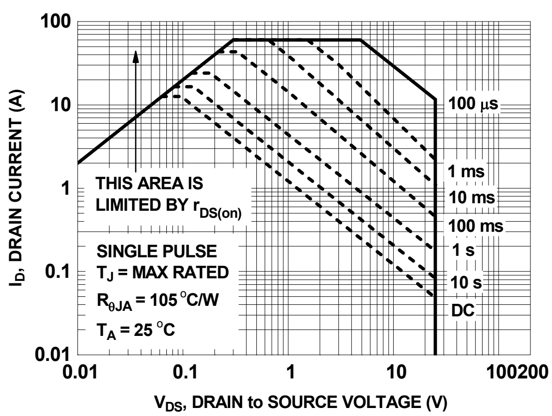


Figure 11. Forward Bias Safe Operating Area

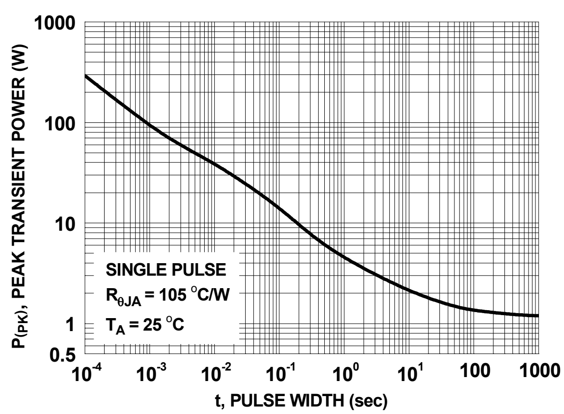


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

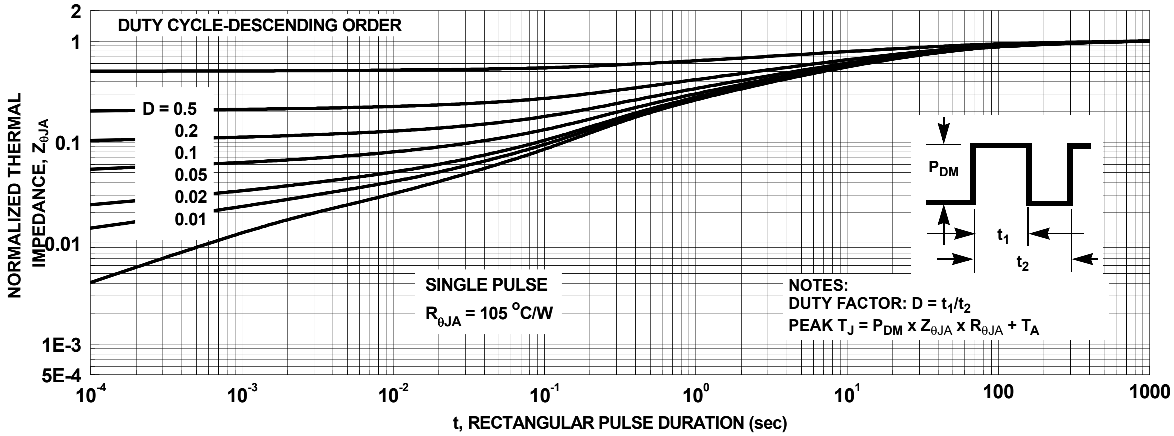
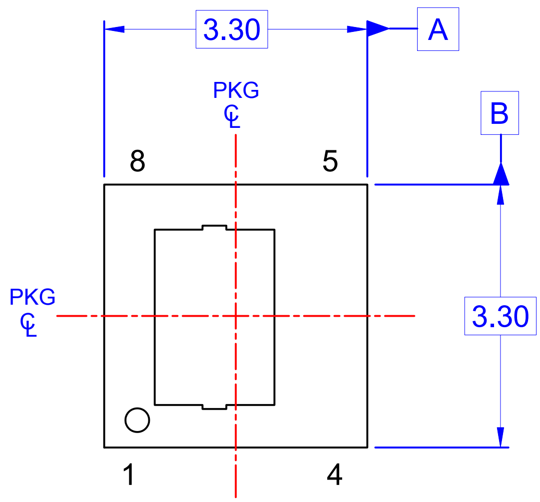
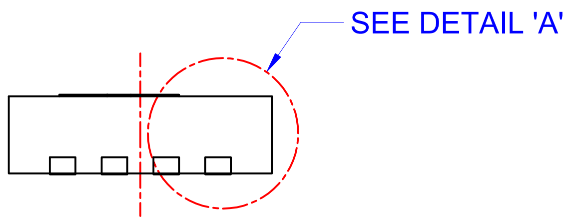
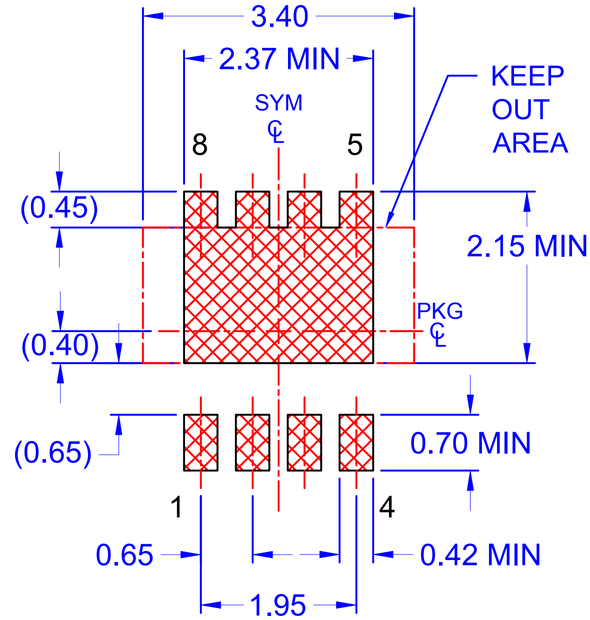


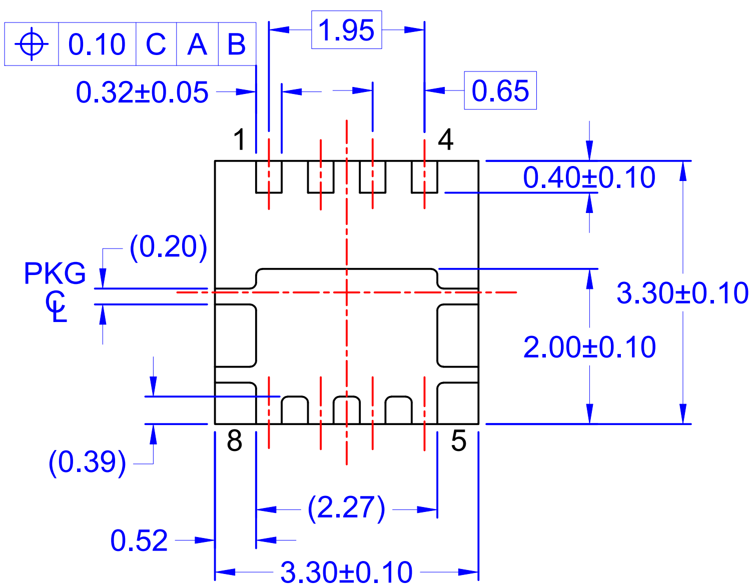
Figure 13. Junction-to-Ambient Transient Thermal Response Curve





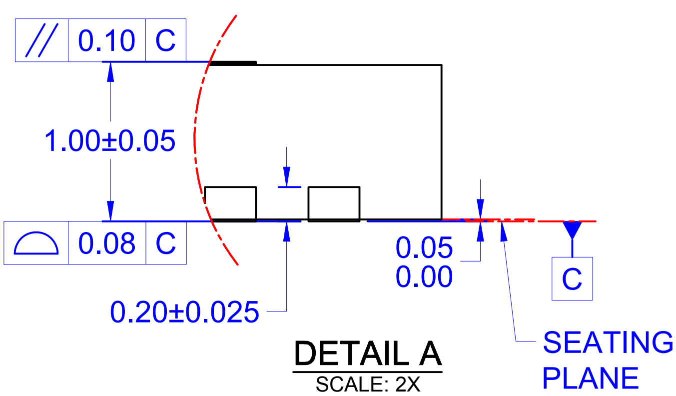


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) DRAWING FILE NAME: PQFN08CREV3



DETAIL A
SCALE: 2X

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative