RF LDMOS Wideband Integrated Power Amplifiers

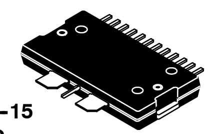
A2I25D012NR1
A2I25D012GNR1

The A2I25D012N wideband integrated power amplifier is optimized to function with a single multi-band circuit usable from 2300 to 2690 MHz. This multi-stage structure is rated from 26 to 32 V operation and covers all typical cellular base station modulation formats.

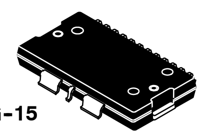
- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA, $I_{DQ2(A+B)}$ = 110 mA, P_{out} = 2.2 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2300 MHz	31.8	18.5	–47.8
2350 MHz	31.8	18.4	–48.7
2400 MHz	31.9	18.3	–49.3
2496 MHz	32.2	18.3	–49.8
2590 MHz	32.5	18.6	–48.3
2690 MHz	33.2	19.8	–46.8

2300–2690 MHz, 2.2 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS



TO-270WB-15 PLASTIC A2I25D012NR1



TO-270WBG-15 PLASTIC A2I25D012GNR1

Features

- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

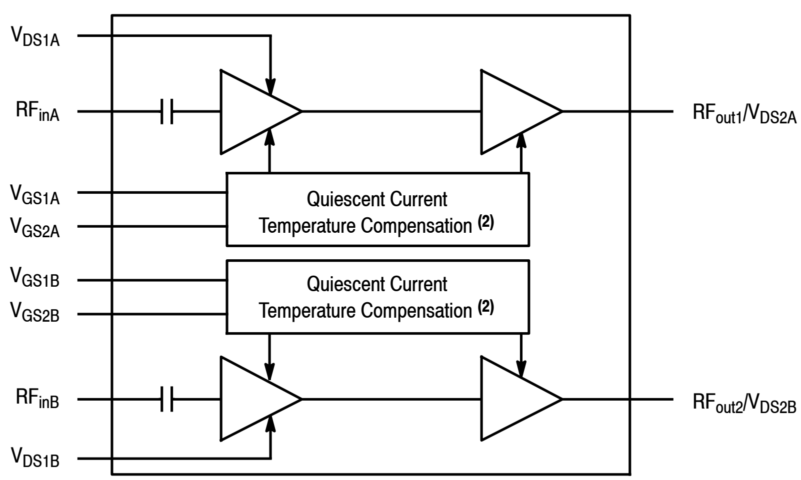
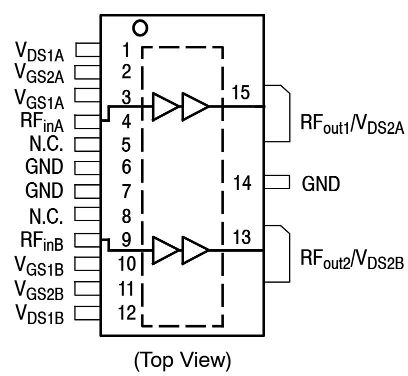


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 2 W CW, 2500 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 110 mA	$R_{\theta JC}$	 9.3 3.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 3 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA, Measured in Functional Test)	$V_{GG(Q)}$	5.3	6.7	8.0	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 – Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics					
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 10 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 110 mA)	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 110 mA, Measured in Functional Test)	$V_{GG(Q)}$	4.0	5.0	6.0	Vdc
Drain-Source On-Voltage [1] (V_{GS} = 10 Vdc, I_D = 100 mAdc)	$V_{DS(on)}$	0.1	0.32	1.5	Vdc

Functional Tests [2,3] (In Freescale Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA, $I_{DQ2(A+B)}$ = 110 mA, P_{out} = 2.2 W Avg., f = 2690 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	31.0	32.4	35.0	dB
Power Added Efficiency	PAE	18.0	19.7	—	%
P_{out} @ 1 dB Compression Point, CW	P1dB	13.5	15.5	—	W

Load Mismatch [4] (In Freescale Characterization Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 45 mA, $I_{DQ2(A+B)}$ = 110 mA, f = 2690 MHz

VSWR 10:1 at 32 Vdc, 24 W CW Output Power (3 dB Input Overdrive from 13 W CW Rated Power)	No Device Degradation

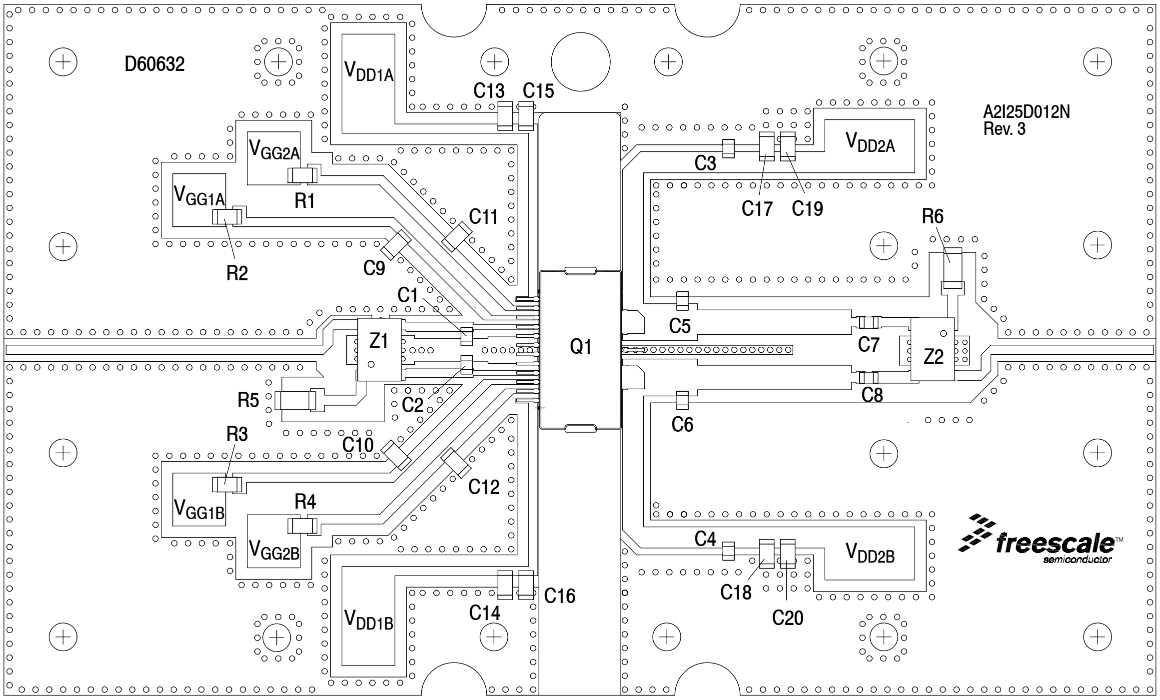
Typical Performance [4] (In Freescale Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 45 mA, $I_{DQ2(A+B)}$ = 110 mA, 2300–2690 MHz Bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
P_{out} @ 3 dB Compression Point, CW [5]	P3dB	—	24	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2690 MHz frequency range.)	Φ	—	–11.1	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	160	—	MHz
Quiescent Current Accuracy over Temperature [6]	ΔI_{QT}				%
with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1		—	2.77	—	
with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2		—	1.83	—	
Gain Flatness in 390 MHz Bandwidth @ P_{out} = 2.2 W Avg.	G_F	—	1.4	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.033	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I25D012NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-Reel	TO-270WB-15
A2I25D012GNR1		TO-270WBG-15

1. Each side of device measured separately.
2. Part internally input matched.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. All data measured in fixture with device soldered to heatsink.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
6. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

Figure 3. A2I25D012NR1 Characterization Test Circuit Component Layout — 2300–2690 MHz

Table 7. A2I25D012NR1 Test Circuit Component Designations and Values — 2300–2690 MHz

Part	Description	Part Number	Manufacturer
C1, C2	1.1 pF Chip Capacitors	ATC600F1R1AW250XT	ATC
C3, C4	6.8 pF Chip Capacitors	ATC600F6R8BW250XT	ATC
C5, C6	1.8 pF Chip Capacitors	ATC600F1R8AWT250XT	ATC
C7, C8	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C9, C10, C11, C12, C17, C18	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C13, C14, C19, C20	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C15, C16	1.0 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
Q1	RF LDMOS Power Amplifier	A2I25D012NR1	Freescale
R1, R4	4.7 KΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R2*, R3*	2.4 KΩ, 1/4 W Chip Resistors	CRCW12062K40FKEA	Vishay
R5, R6	50 Ω, 4 W Chip Resistors	CW12010T0050GBK	ATC
Z1, Z2	2300–2900 MHz Band, 90°, 3 dB Hybrid Couplers	X3C26P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, $\varepsilon_r = 3.66$	D60632	MTL

*In production fixture only.

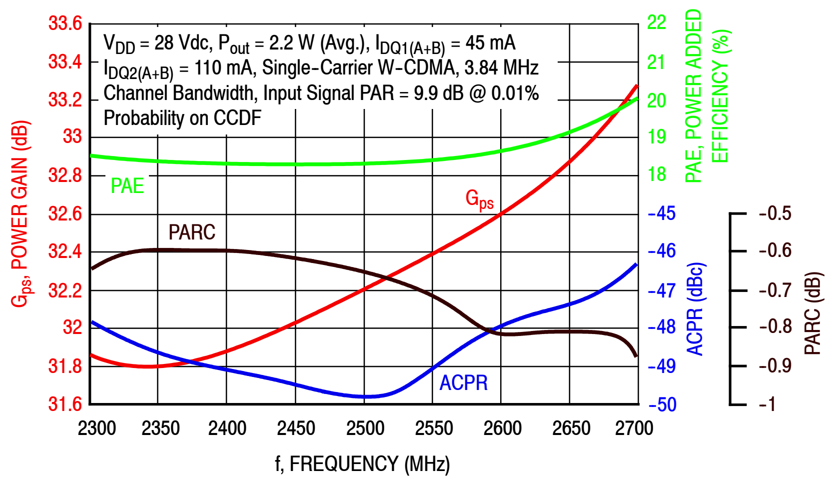


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 2.2 Watts Avg.

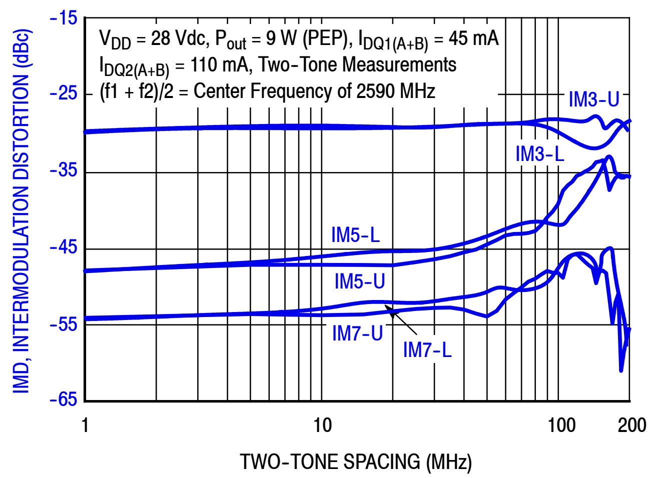


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

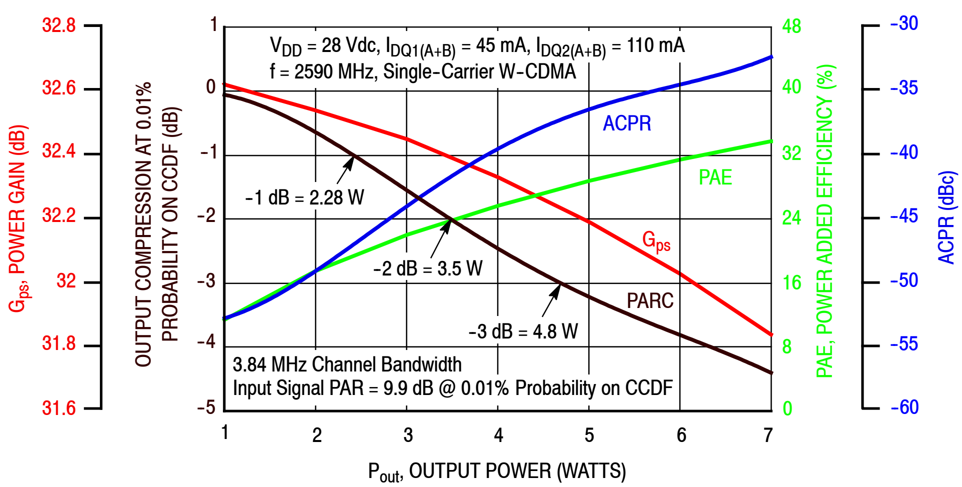


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

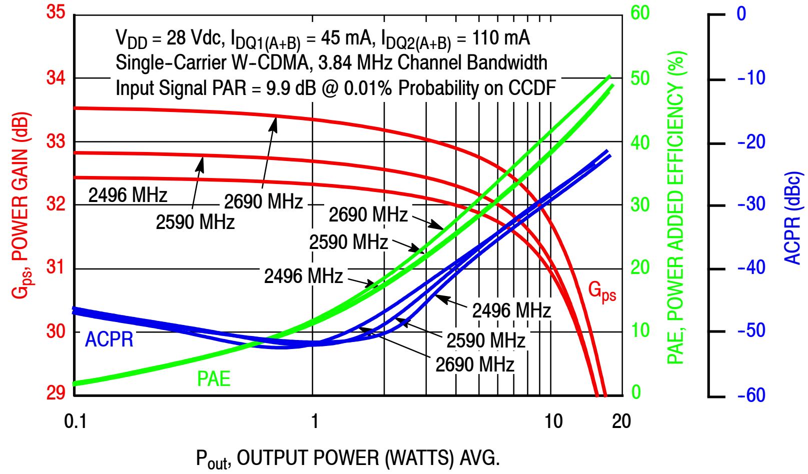


Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power — 2496–2690 MHz

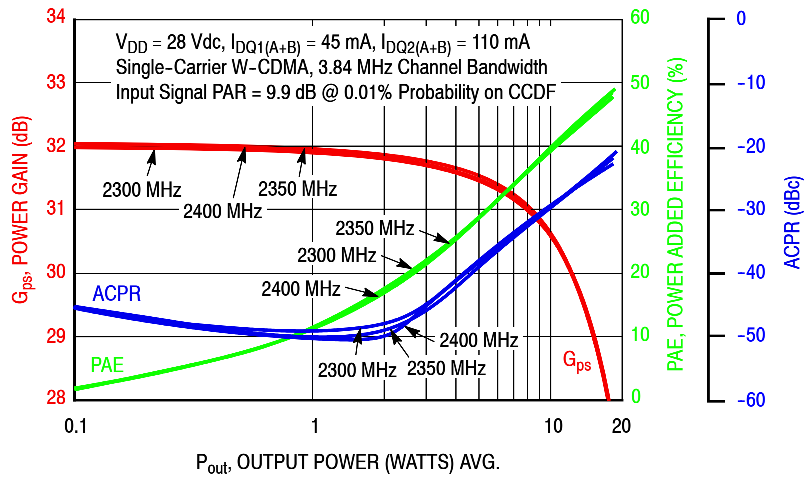


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power — 2300–2400 MHz

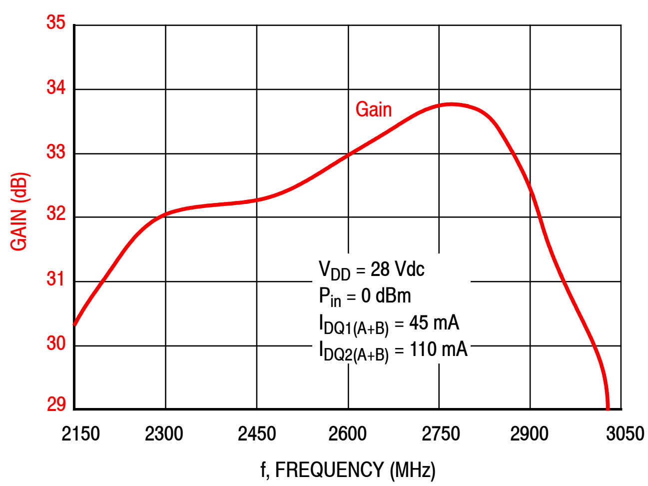


Figure 9. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 22.5 mA, $I_{DQ2(A)}$ = 55 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	20.5 + j19.7	19.8 – j20.5	9.60 – j0.52	31.3	40.3	11	54.9	–3
2350	24.5 + j16.0	23.6 – j16.1	8.79 – j0.88	31.7	40.2	10	53.9	–3
2400	30.8 + j8.79	29.5 – j11.3	7.87 – j1.08	32.1	40.1	10	54.1	–4
2496	45.1 + j5.61	43.9 – j9.82	8.92 – j1.11	32.5	40.1	10	53.3	–3
2590	52.3 + j22.1	55.9 – j21.5	8.86 – j1.91	33.1	40.2	11	55.0	–2
2690	46.0 + j43.0	42.9 – j35.7	10.1 – j2.57	33.2	40.3	11	55.1	–3

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	20.5 + j19.7	20.6 – j21.0	10.4 – j1.17	29.0	41.2	13	55.9	–6
2350	24.5 + j16.0	24.6 – j17.1	9.88 – j1.42	29.3	41.1	13	55.1	–6
2400	30.8 + j8.79	30.6 – j13.3	9.77 – j1.59	29.6	41.1	13	55.1	–7
2496	45.1 + j5.61	43.4 – j12.7	10.1 – j1.50	30.2	41.1	13	55.2	–6
2590	52.3 + j22.1	52.8 – j23.3	10.4 – j2.22	30.7	41.2	13	55.6	–5
2690	46.0 + j43.0	41.0 – j35.0	11.5 – j2.97	30.9	41.2	13	56.0	–5

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

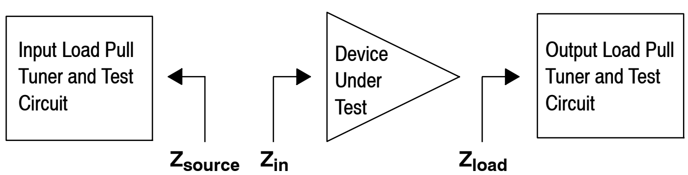


Table 9. Load Pull Performance — Maximum Power Added Efficiency Tuning

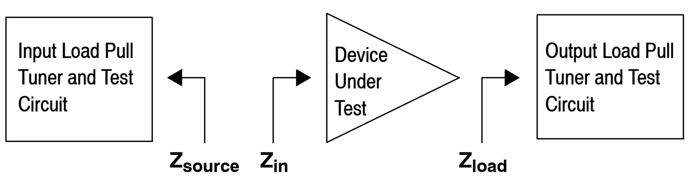
V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 22.5 mA, $I_{DQ2(A)}$ = 55 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	20.5 + j19.7	20.8 – j18.5	5.29 + j2.95	33.3	38.7	7	62.6	–8
2350	24.5 + j16.0	24.8 – j13.5	5.06 + j2.20	33.7	38.8	8	61.9	–8
2400	30.8 + j8.79	32.4 – j8.18	4.95 + j2.11	34.2	38.6	7	60.8	–8
2496	45.1 + j5.61	50.5 – j8.00	5.25 + j1.60	34.5	38.9	8	60.6	–7
2590	52.3 + j22.1	61.3 – j27.8	5.42 + j1.07	34.9	39.0	8	61.9	–7
2690	46.0 + j43.0	42.1 – j41.4	5.33 – j0.09	35.2	38.8	8	62.2	–8

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	20.5 + j19.7	21.2 – j19.2	5.18 + j2.83	31.3	39.4	9	63.6	–13
2350	24.5 + j16.0	25.5 – j14.7	5.15 + j2.29	31.7	39.6	9	63.3	–12
2400	30.8 + j8.79	32.7 – j10.3	5.16 + j2.22	32.2	39.5	9	63.0	–12
2496	45.1 + j5.61	50.1 – j10.8	4.96 + j1.89	32.8	39.4	9	62.9	–12
2590	52.3 + j22.1	57.9 – j27.9	5.33 + j1.26	33.0	39.7	9	63.5	–9
2690	46.0 + j43.0	40.9 – j39.8	5.33 + j0.11	33.2	39.5	9	63.7	–10

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB - TYPICAL LOAD PULL CONTOURS — 2590 MHz

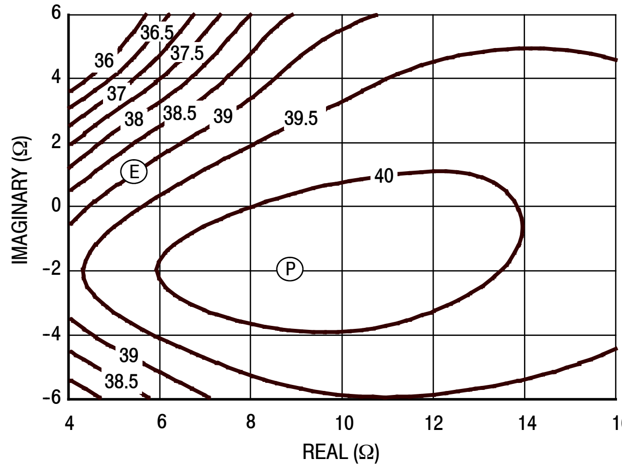


Figure 10. P1dB Load Pull Output Power Contours (dBm)

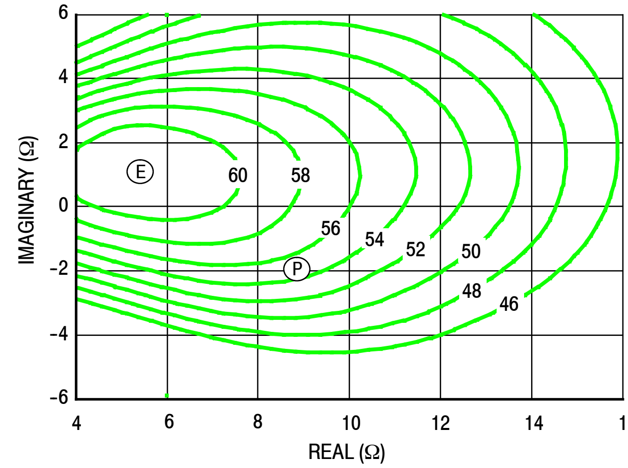


Figure 11. P1dB Load Pull Efficiency Contours (%)

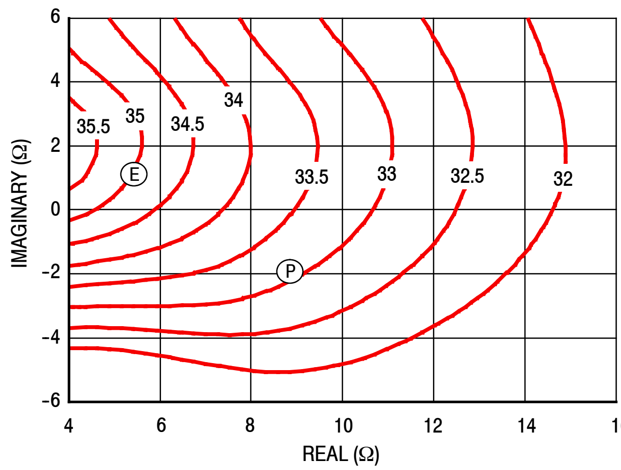


Figure 12. P1dB Load Pull Gain Contours (dB)

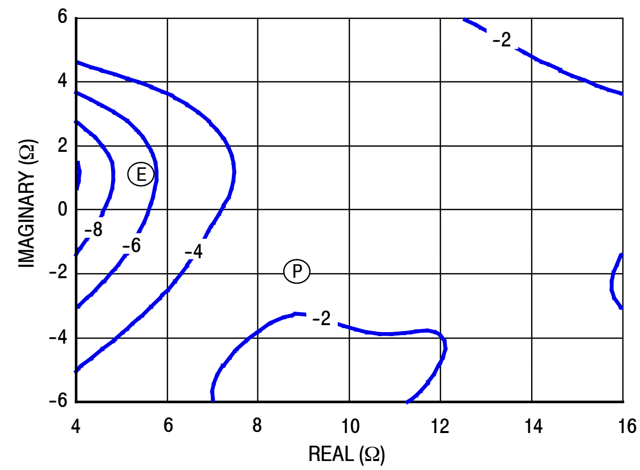


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Power Added Efficiency

Gain
Power Added Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 2590 MHz

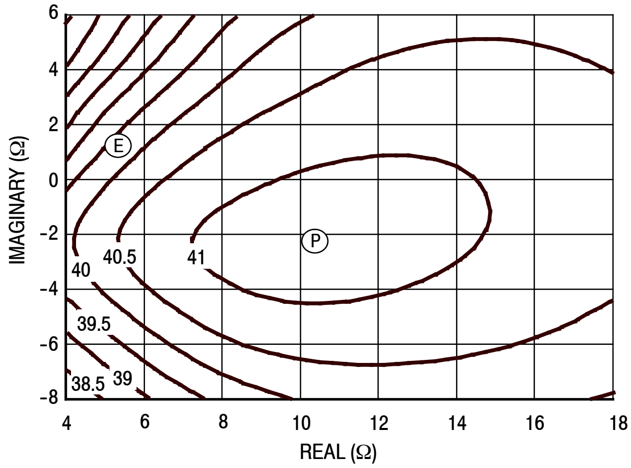


Figure 14. P3dB Load Pull Output Power Contours (dBm)

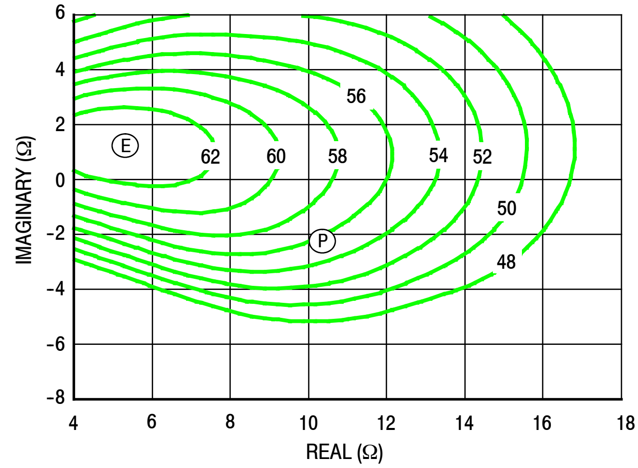


Figure 15. P3dB Load Pull Efficiency Contours (%)

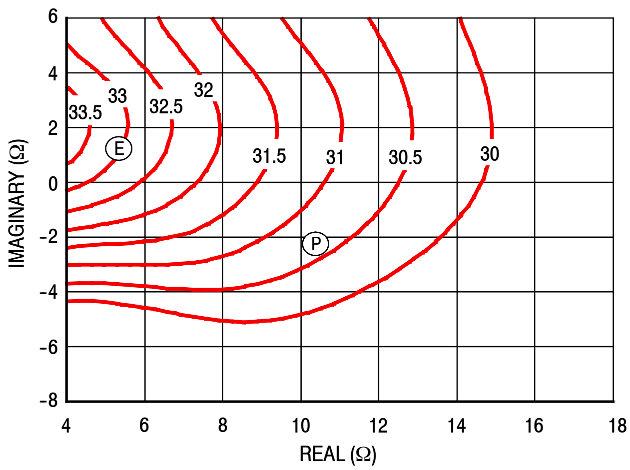


Figure 16. P3dB Load Pull Gain Contours (dB)

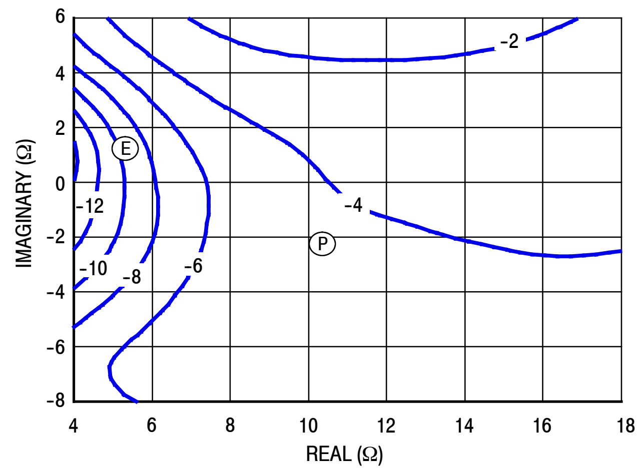


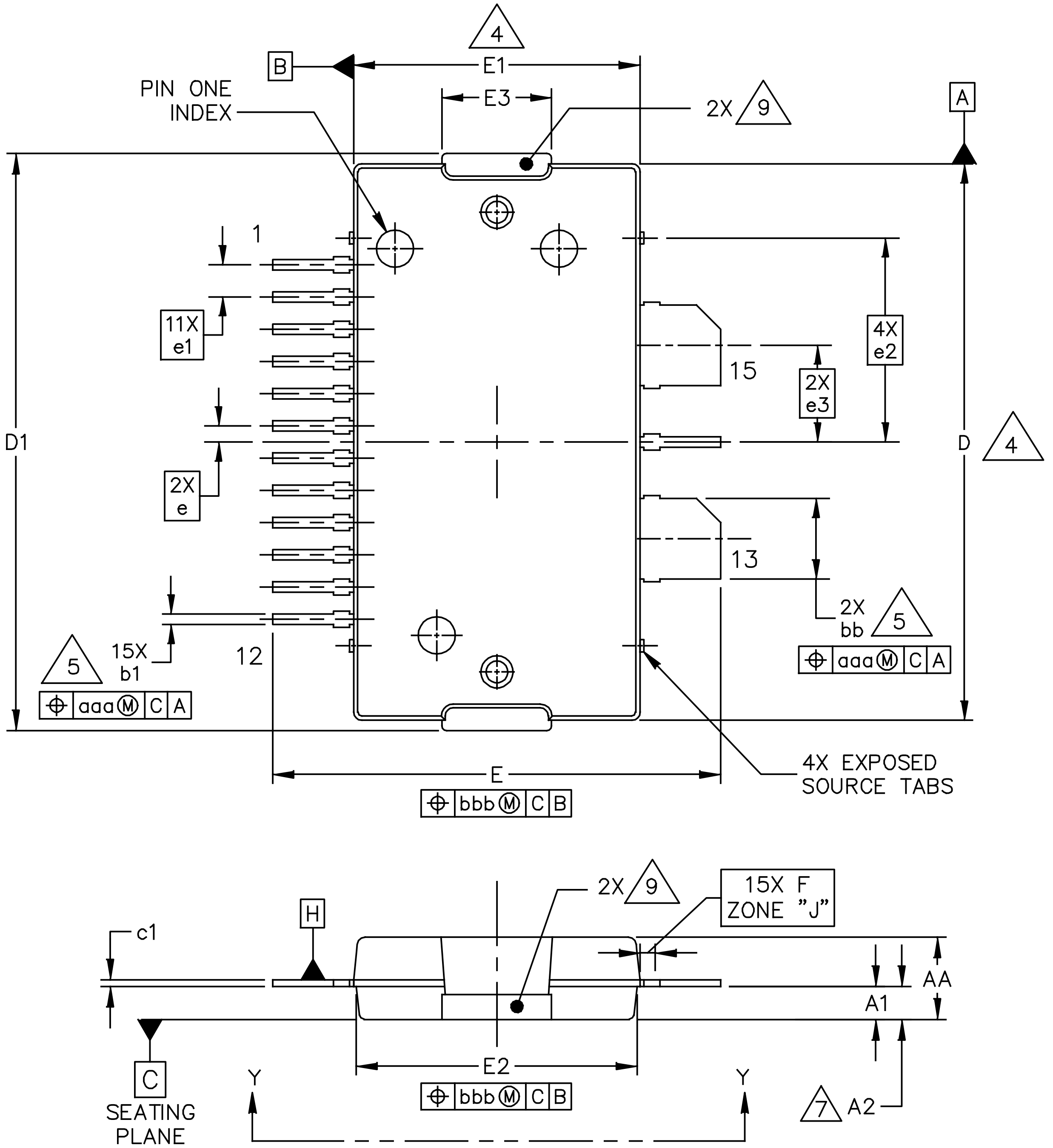
Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Power Added Efficiency

Gain
Power Added Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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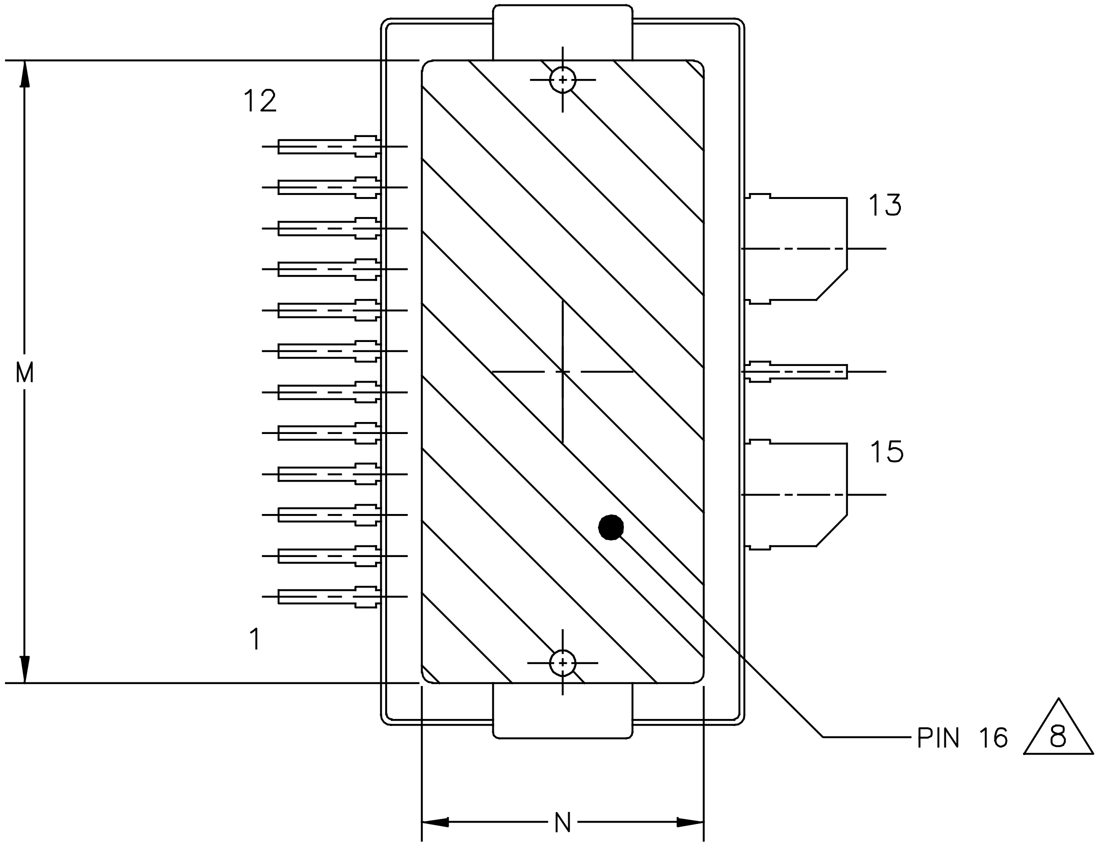

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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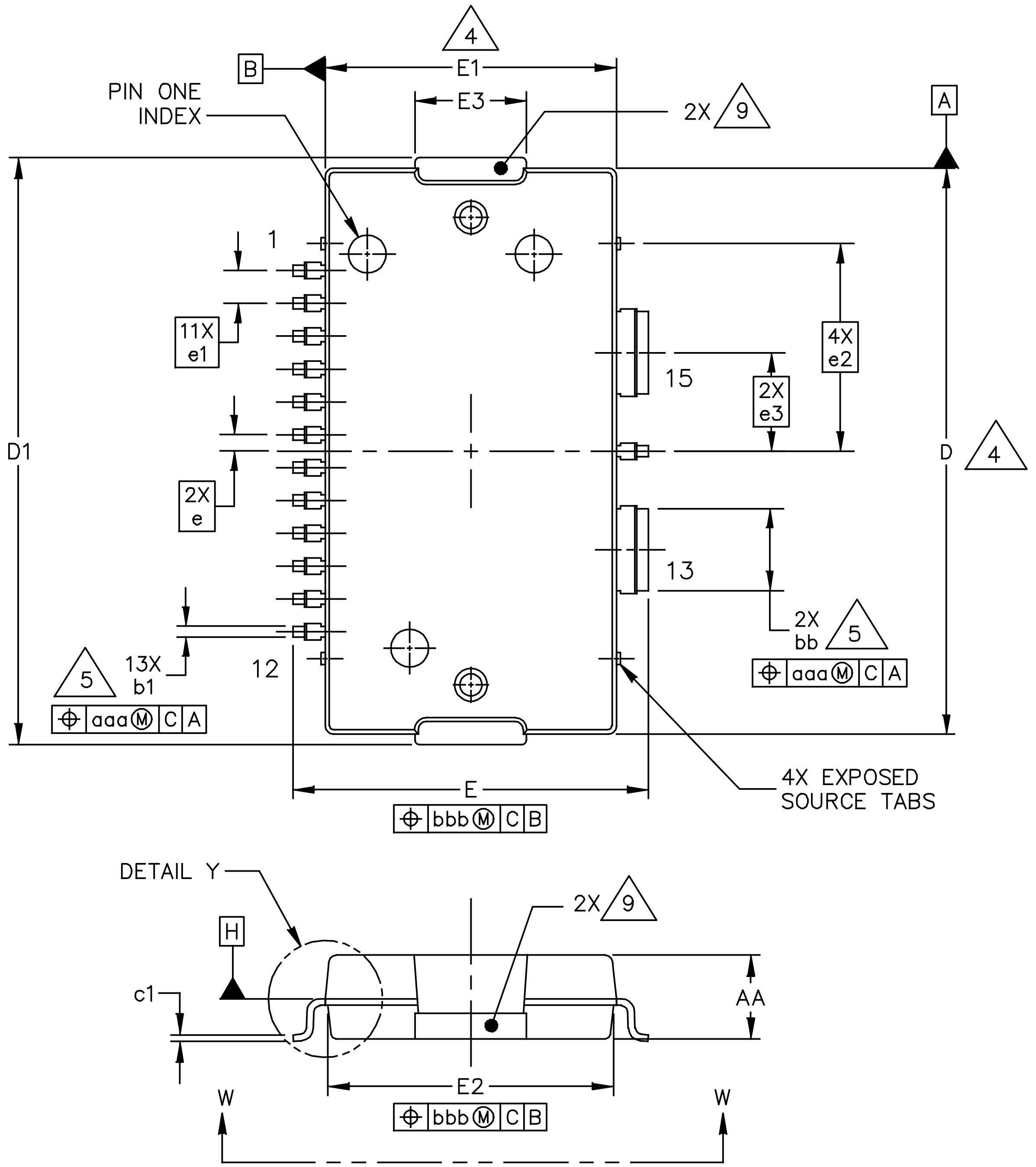
	STANDARD: NON-JEDEC	
		17 JUN 2014



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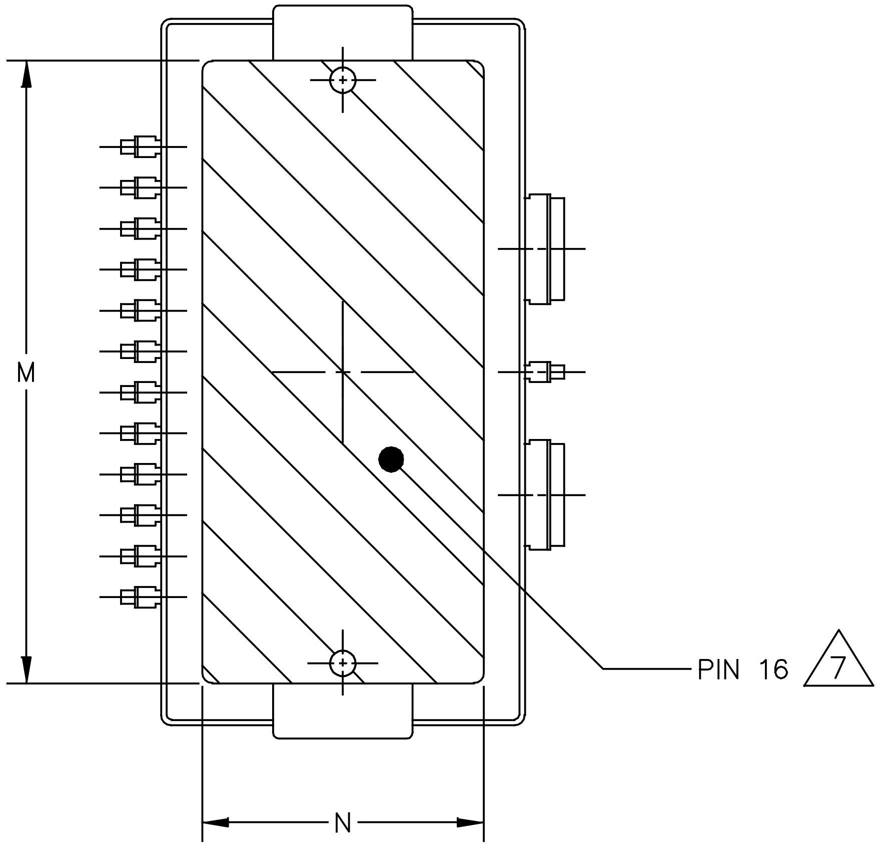
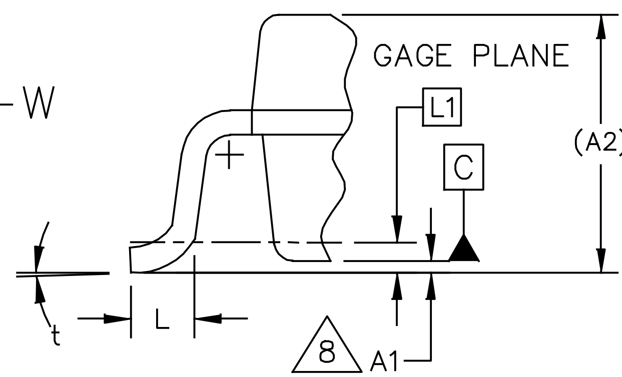


VIEW W–W



DETAIL "Y"

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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	STANDARD: NON–JEDEC	
	17 JUN 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

△4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

△7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

△8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

△9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270WBG-15	DOCUMENT NO: 98ASA00684D	REV: O
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	17 JUN 2014	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2014	• Initial release of data sheet
1	Mar. 2015	• Figs. 4, 6–8: changed drain efficiency to power added efficiency for plots and axes labels, pp. 5, 6 • Tables 7 and 8: changed drain efficiency to power added efficiency and added measurement made on a per side basis note, pp. 7, 8

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OCEAN CHIPS
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Поставка электронных компонентов

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- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А