TOSHIBA Field-Effect Transistor Silicon N-Channel MOS MOS

SSM6K403TU

- Power Management Switch Applications
- High-Speed Switching Applications

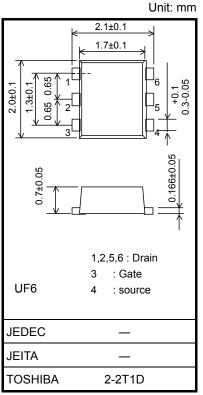
• 1.5V drive

Low ON-resistance: R_{on} = 66mΩ (max) (@V_{GS} = 1.5V)

$$\begin{split} R_{On} &= 43 m \Omega \; (\text{max}) \; (\text{@V}_{GS} = 1.8 \text{V}) \\ R_{On} &= 32 m \Omega \; (\text{max}) \; (\text{@V}_{GS} = 2.5 \text{V}) \\ R_{On} &= 28 m \Omega \; (\text{max}) \; (\text{@V}_{GS} = 4.0 \text{V}) \end{split}$$

Absolute Maximum Ratings (Ta = 25°C) (Note)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	20	V	
Gate-source voltage		V _{GSS}	±10	V	
Drain current	DC	I _D	4.2	А	
	Pulse	I _{DP}	8.4		
Drain power dissipation		P _D (Note1)	500	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature		T _{stg}	-55 to 150	°C	



Weight: 7.0mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 645 mm²)



Electrical Characteristics (Ta = 25°C)

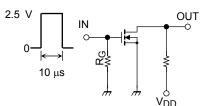
Char	acteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain-source breakdown voltage	V (BR) DSS	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	20	_	_	V	
	V _{(BR) DSX}	I _D = 1 mA, V _{GS} = -10V	12	_	_]	
Drain cutoff curren	ıt	I _{DSS}	V _{DS} =20 V, V _{GS} = 0 V	_	_	1	μА
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Gate threshold vol	tage	V _{th}	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.35	_	1.0	V
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = 3 \text{ V}, I_{D} = 3.0 \text{ A}$ (Note2)	10	20	_	S
Drain-source ON-resistance	R _{DS} (ON)	$I_D = 3.0 \text{ A}, V_{GS} = 4.0 \text{ V}$ (Note2)	_	19	28	- mΩ	
		$I_D = 3.0 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note2)	_	23	32		
		I _D = 1.0 A, V _{GS} = 1.8 V (Note2)	_	28	43		
		$I_D = 0.5 \text{ A}, V_{GS} = 1.5 \text{ V}$ (Note2)	_	35	66		
Input capacitance		C _{iss}		_	1050	_	
Output capacitance Reverse transfer capacitance		Coss	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		175	_	pF
		C _{rss}		_	160	_	
Gate-Source Charge C		Qg		_	16.8	_	nC
		Q _{gs}	V _{DD} = 10 V, I _D = 4.2 A V _{GS} = 4 V	_	12.1	_	
		Q _{gd}	VGS - 4 V		4.7	_	
Switching time	Turn-on time	t _{on}	$V_{DD} = 10 \text{ V}, I_D = 1 \text{ A}$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 4.7 \Omega$	_	18	_	- ns
	Turn-off time	t _{off}		_	32	_	
Drain-source forwa	ard voltage	V _{DSF}	$I_D = -4.2 \text{ A}, V_{GS} = 0 \text{ V}$ (Note2)	_	-0.8	-1.2	V

Note 2: Pulse test

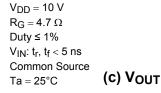
2 2014-03-01

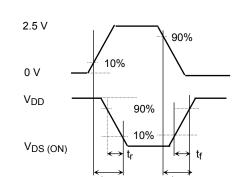
Switching Time Test Circuit

(a) Test Circuit



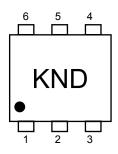
(b) V_{IN}

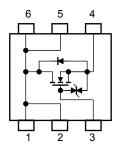




Marking

Equivalent Circuit (top view)





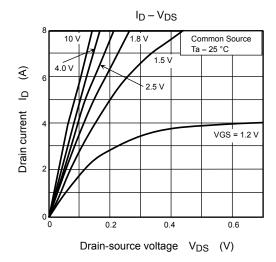
Notice on Usage

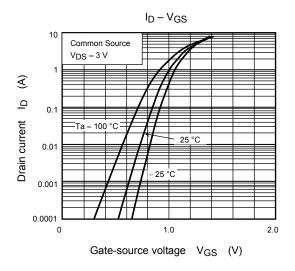
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 1 mA for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} . (The relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on).)

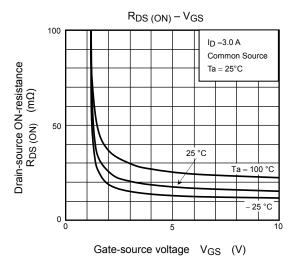
Take this into consideration when using the device.

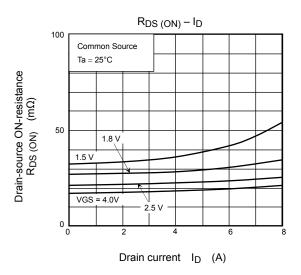
Handling Precaution

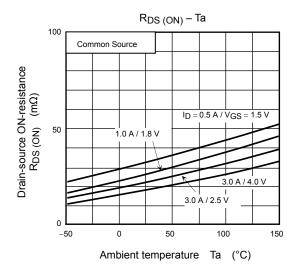
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

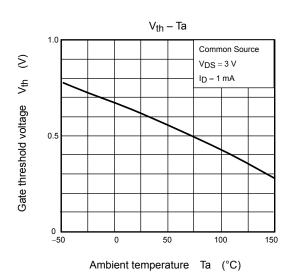




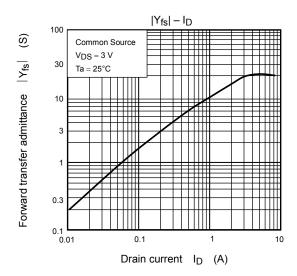


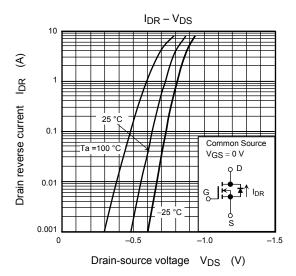


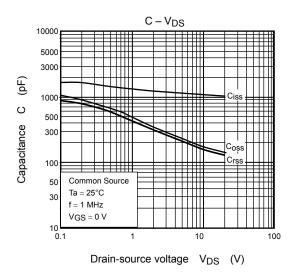


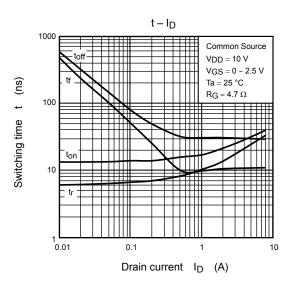


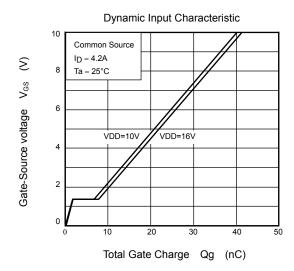
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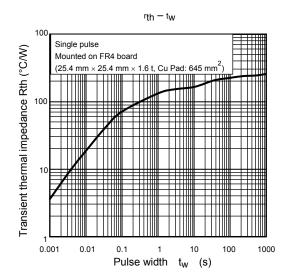


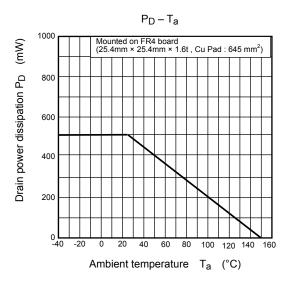






5 2014-03-01





6 2014-03-01

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