



# Improved, Quad, SPST Analog Switches

DG411/DG412/DG413

## General Description

Maxim's redesigned DG411/DG412/DG413 analog switches now feature low on-resistance matching between switches ( $3\Omega$  max) and guaranteed on-resistance flatness over the signal range ( $\Delta 4\Omega$  max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off-leakage current over temperature (less than 5nA at +85°C).

The DG411/DG412/DG413 are quad, single-pole/single-throw (SPST) analog switches. The DG411 is normally closed (NC), and the DG412 is normally open (NO). The DG413 has two NC switches and two NO switches. Switching times are less than 150ns max for  $t_{ON}$  and less than 100ns max for  $t_{OFF}$ . These devices operate from a single +10V to +30V supply, or bipolar  $\pm 4.5V$  to  $\pm 20V$  supplies. Maxim's improved DG411/DG412/DG413 are fabricated with a 44V silicon-gate process.

## Applications

- |                            |                          |
|----------------------------|--------------------------|
| Sample-and-Hold Circuits   | Communication Systems    |
| Test Equipment             | Battery-Operated Systems |
| Heads-Up Displays          | PBX, PABX                |
| Guidance & Control Systems | Audio Signal Routing     |
| Military Radios            |                          |

## New Features

- ◆ Plug-In Upgrade for Industry-Standard DG411/DG412/DG413
- ◆ Improved  $R_{DS(ON)}$  Match Between Channels ( $3\Omega$  max)
- ◆ Guaranteed  $R_{FLAT(ON)}$  Over Signal Range ( $\Delta 4\Omega$ )
- ◆ Improved Charge Injection (10pC max)
- ◆ Improved Off-Leakage Current Over Temperature (< 5nA at +85°C)
- ◆ Withstand Electrostatic Discharge (2000V min) per Method 3015.7

## Existing Features

- ◆ Low  $R_{DS(ON)}$  ( $35\Omega$  max)
- ◆ Single-Supply Operation +10V to +30V
- ◆ Bipolar-Supply Operation  $\pm 4.5V$  to  $\pm 20V$
- ◆ Low Power Consumption ( $35\mu W$  max)
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG411CJ	0°C to +70°C	16 Plastic DIP
DG411CUE	0°C to +70°C	16 TSSOP
DG411EUE	-40°C to +85°C	16 TSSOP
DG411CY	0°C to +70°C	16 Narrow SO
DG411C/D	0°C to +70°C	Dice†

Ordering Information continued at end of data sheet.

†Contact factory for dice specifications.

## Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

**DIP/SO/TSSOP**  
DG411

LOGIC	SWITCH
0	ON
1	OFF

**DIP/SO/TSSOP**  
DG412

LOGIC	SWITCH
0	OFF
1	ON

**DIP/SO/TSSOP**  
DG413

LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

Pin Configurations and Functional Diagrams continued at end of data sheet.

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## ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to V-.)

V+	.....44V
GND	.....25V
V <sub>L</sub>	.....(GND -0.3V) to (V+ +0.3V)
Digital Inputs, V <sub>S</sub> , V <sub>D</sub> (Note 1)	.....(V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal)	.....30mA
Peak Current (pulsed at 1ms, 10% duty cycle max)	.....100mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)	.842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)	.....800mW
16-Pin TSSOP (derate 6.7mW/°C above +70°C)	.....457mW
16-Pin QFN (derate 19.2mW/°C above +70°C)	.....1538mW

Operating Temperature Ranges

DG41_C	.....0°C to +70°C
DG41_D	.....-40°C to +85°C
DG41_AK	.....-55°C to +125°C
Storage Temperature Range	.....-65°C to +150°C
Lead Temperature (soldering, 10s)	.....+300°C

**Note 1:** Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V<sub>L</sub> = 5V, V<sub>GND</sub> = 0V, V<sub>INH</sub> = 2.4V, V<sub>INL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
<b>SWITCH</b>								
Analog Signal Range	V <sub>ANALOG</sub>	(Note 3)		-15		15	V	
Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V+ = 13.5V, V- = -13.5V, V <sub>D</sub> = ±8.5V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C	C, D	17	45	Ω	
				A	17	30		
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			45		
On-Resistance Match Between Channels (Note 4)	ΔR <sub>DS(ON)</sub>	V+ = 15V, V- = -15V, V <sub>D</sub> = ±10V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C			3	Ω	
				T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		5		
On-Resistance Flatness (Note 4)	R <sub>FLAT(ON)</sub>	V+ = 15V, V- = -15V, V <sub>D</sub> = ±5V, 0V, I <sub>S</sub> = -10mA	T <sub>A</sub> = +25°C			4	Ω	
				T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		6		
Source Off-Leakage Current (Note 7)	I <sub>S(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C	C, D, A	-0.25	-0.10	0.25	nA
				C, D	-5		5	
				A	-10		10	
Drain Off-Leakage Current (Note 7)	I <sub>D(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C	C, D, A	-0.25	-0.10	0.25	nA
				C, D	-5		5	
				A	-10		10	
Drain On-Leakage Current (Note 7)	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C	C, D, A	-0.4	-0.1	0.4	nA
				C, D	-20		20	
				A	-40		40	

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## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, VL = 5V, VGND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS	
<b>INPUT</b>							
Input Current with Input Voltage High	I <sub>INH</sub>	IN = 2.4V, all others = 0.8V	-0.500	0.005	0.500	μA	
Input Current with Input Voltage Low	I <sub>INL</sub>	IN = 0.8V, all others = 2.4V	-0.500	0.005	0.500	μA	
<b>SUPPLY</b>							
Power-Supply Range			±4.5		±20.0	V	
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	0.0001	1	μA
			TA = TMIN to TMAX	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = TMIN to TMAX	-5		5	
Logic Supply Current	IL	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	0.0001	1	μA
			TA = TMIN to TMAX	-5		5	
Ground Current	IGND	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = TMIN to TMAX	-5		5	
<b>DYNAMIC</b>							
Turn-On Time	t <sub>ON</sub>	VD = ±10V, Figure 2	TA = +25°C	110	175	ns	
			TA = TMIN to TMAX		220		
Turn-Off Time	t <sub>OFF</sub>	VD = ±10V, Figure 2	TA = +25°C	100	145	ns	
			TA = TMIN to TMAX		160		
Break-Before-Make Time Delay	t <sub>D</sub>	DG413 only, RL = 300Ω, CL = 35pF, Figure 3	TA = +25°C	25		ns	
Charge Injection (Note 3)	Q	CL = 1.0nF, VGEN = 0V, RGEN = 0Ω, Figure 4	TA = +25°C	5	10	pC	
Off-Isolation (Note 5)	OIRR	RL = 50Ω, CL = 5pF, f = 1MHz, Figure 5	TA = +25°C	68		dB	
Crosstalk (Note 6)		RL = 50Ω, CL = 5pF, f = 1MHz, Figure 6	TA = +25°C	85		dB	
Source Off-Capacitance	CS(OFF)	f = 1MHz, Figure 7	TA = +25°C	9		pF	
Drain Off-Capacitance	CD(OFF)	f = 1MHz, Figure 7	TA = +25°C	9		pF	
Drain On-Capacitance	CD(ON) + CS(ON)	f = 1MHz, Figure 8	TA = +25°C	35		pF	

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## ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, VL = 5V, VGND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>SWITCH</b>							
Analog Signal Range	VANALOG	(Note 3)		0		12	V
Drain-Source On-Resistance	RDS(ON)	V+ = 10.8V, VD = 3.8V, IS = -10mA	TA = +25°C	40	80	100	Ω
			TA = TMIN to TMAX				
<b>SUPPLY</b>							
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, VIN = 0V or 5V	TA = +25°C	-1	0.0001	1	μA
			TA = TMAX	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, VIN = 0V or 5V	TA = +25°C	-1	0.0001	1	μA
			TA = TMAX	-5		5	
Logic Supply Current	IL	All channels on or off, VL = 5.25V, VIN = 0V or 5V	TA = +25°C	-1	0.0001	1	μA
			TA = TMAX	-5		5	
Ground Current	IGND	All channels on or off, VL = 5.25V, VIN = 0V or 5V	TA = +25°C	-1	-0.0001	1	μA
			TA = TMAX	-5		5	
<b>DYNAMIC</b>							
Turn-On Time	tON	VS = 8V, Figure 2	TA = +25°C	175	250	315	ns
			TA = TMIN to TMAX				
Turn-Off Time	tOFF	VS = 8V, Figure 2	TA = +25°C	95	125	140	ns
			TA = TMIN to TMAX				
Break-Before-Make Time Delay	tD	DG413 only, RL = 300Ω, CL = 35pF, Figure 3	TA = +25°C	25			ns
Charge Injection (Note 3)	Q	CL = 1.0nF, VGEN = 0V, RGEN = 0V, Figure 4	TA = +25°C		5	10	pC

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:**  $\Delta R_{ON} = \Delta R_{ON\ max} - \Delta R_{ON\ min}$ . On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

**Note 5:** Off-Isolation =  $20\log(V_D/V_S)$ , VD = output, VS = input to off switch. See Figure 5.

**Note 6:** Between any two switches. See Figure 6.

**Note 7:** Leakage parameters IS(OFF), ID(OFF), and ID(ON) are 100% tested at the maximum-rated hot temperature and guaranteed by correlation at +25°C.

# Improved, Quad, SPST Analog Switches

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

DG411/DG412/DG413

**ON-RESISTANCE vs.  $V_D$  AND POWER-SUPPLY VOLTAGE**



**ON-RESISTANCE vs.  $V_D$  AND TEMPERATURE**



**ON-RESISTANCE vs.  $V_D$  AND TEMPERATURE (SINGLE SUPPLY)**



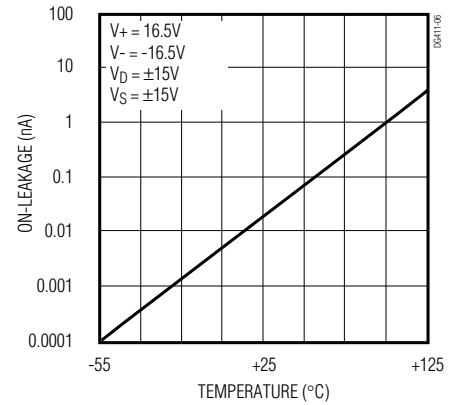
**ON-RESISTANCE vs.  $V_D$  (SINGLE SUPPLY)**



**OFF-LEAKAGE CURRENTS vs. TEMPERATURE**



**ON-LEAKAGE CURRENTS vs. TEMPERATURE**



**CHARGE INJECTION vs. ANALOG VOLTAGE**



**SUPPLY CURRENT vs. TEMPERATURE**



# Improved, Quad, SPST Analog Switches

## Pin Description

PIN		NAME	FUNCTION
DIP/SO/TSSOP	QFN		
1, 16, 9, 8	15, 14, 7, 6	IN1–IN4	Input
2, 15, 10, 7	16, 13, 8, 5	D1–D4	Analog Switch Drain Terminal
3, 14, 11, 6	1, 12, 9, 4	S1–S4	Analog Switch Source Terminal
4	2	V-	Negative-Supply Voltage Input
5	3	GND	Ground
12	10	V <sub>L</sub>	Logic Supply Voltage
13	11	V+	Positive-Supply Voltage Input—Connected to Substrate
—	—	EP	Exposed Paddle (QFN Only). Connect EP to V+.

## Applications Information

### Operation with Supply Voltages Other Than 15V

Using supply voltages other than 15V will reduce the analog signal range. The DG411/DG412/DG413 switches operate with  $\pm 4.5\text{V}$  to  $\pm 20\text{V}$  bipolar supplies or with a +10V to +30V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24V and -5V. V<sub>L</sub> must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with  $\pm 15\text{V}$ ,  $\pm 10\text{V}$ , and  $\pm 5\text{V}$  supplies. (Switching times increase by a factor of two or more for operation at  $\pm 5\text{V}$ .)

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V<sub>L</sub>, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to 1V below V+ and 1V below V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.



Figure 1. Overvoltage Protection Using External Blocking Diodes

# Improved, Quad, SPST Analog Switches

## Timing Diagrams/Test Circuits

DG411/DG412/DG413

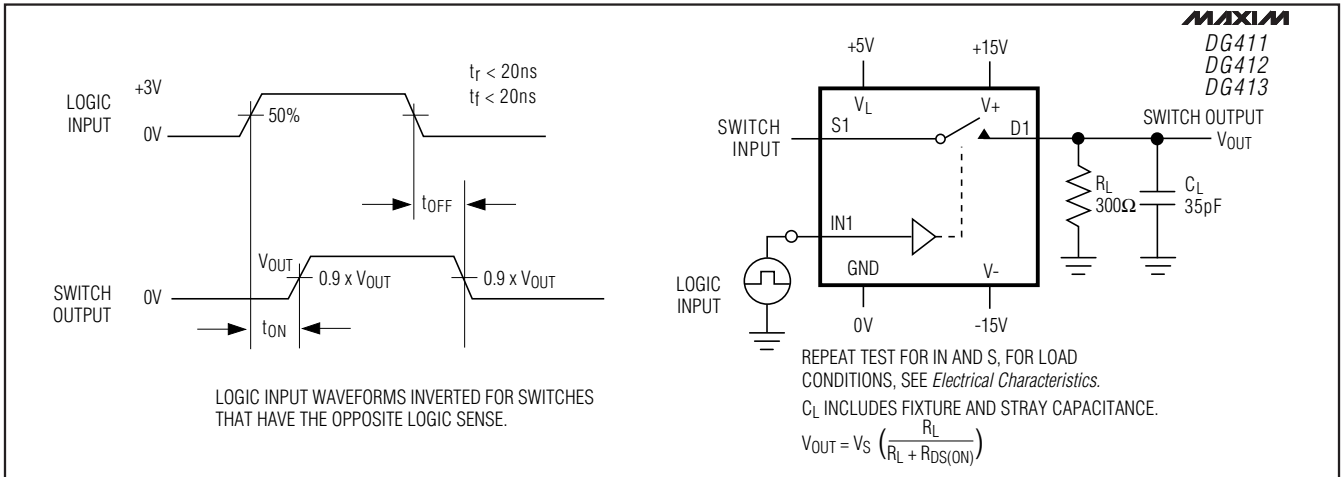


Figure 2. Switching-Time

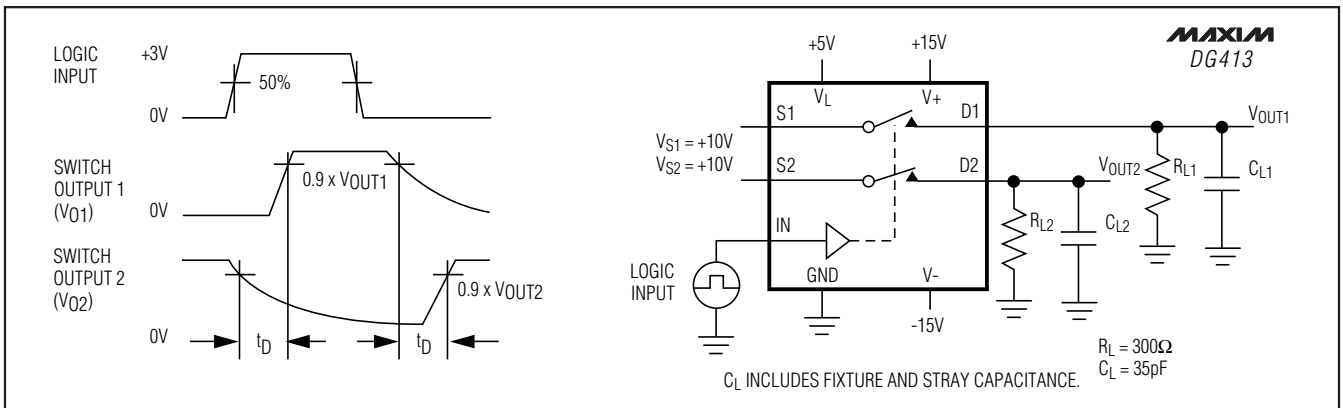


Figure 3. DG413 Break-Before-Make

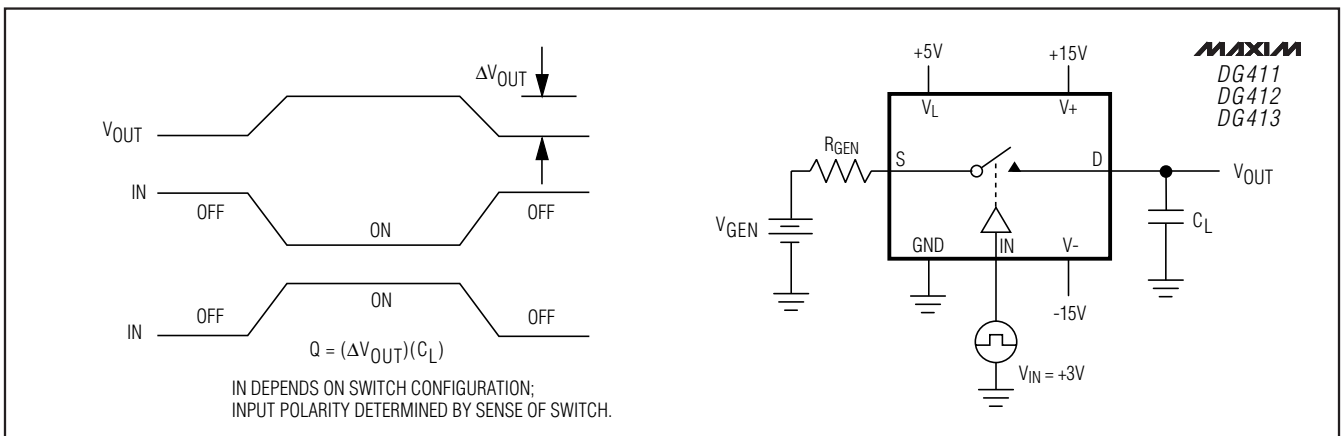


Figure 4. Charge-Injection

# Improved, Quad, SPST Analog Switches

## Timing Diagrams/Test Circuits (continued)

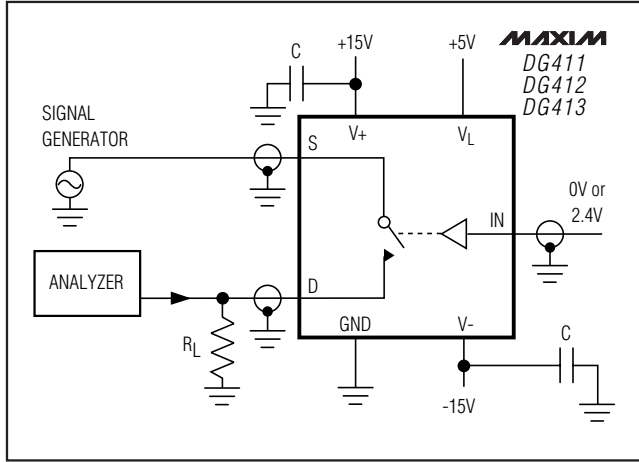


Figure 5. Off-Isolation

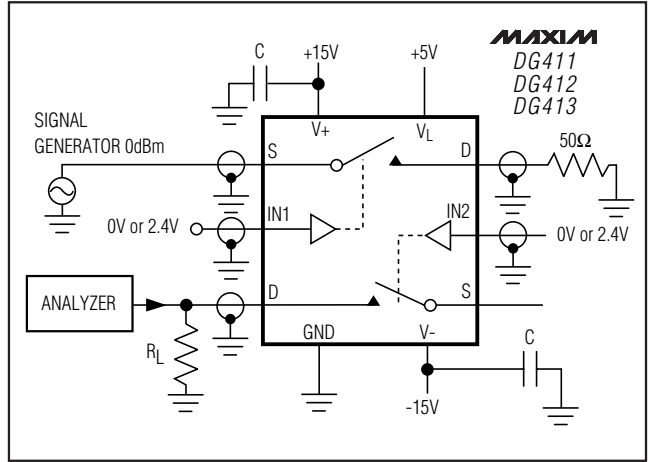


Figure 6. Crosstalk



Figure 7. Channel Off-Capacitance



Figure 8. Channel On-Capacitance



# Improved, Quad, SPST Analog Switches

DG411/DG412/DG413

## Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG411EGE	-40°C to +85°C	16 QFN-EP*
DG411DJ	-40°C to +85°C	16 Plastic DIP
DG411DY	-40°C to +85°C	16 Narrow SO
DG411DK	-40°C to +85°C	16 CERDIP
DG411AK	-55°C to +125°C	16 CERDIP**
DG411MY/PR	-55°C to +125°C	16 SO***
DG411MY/PR-T	-55°C to +125°C	16 SO***
<b>DG412CJ</b>	0°C to +70°C	16 Plastic DIP
DG412CUE	0°C to +70°C	16 TSSOP
DG412EUE	-40°C to +85°C	16 TSSOP
DG412CY	0°C to +70°C	16 Narrow SO
DG412C/D	0°C to +70°C	Dice†
DG412DJ	-40°C to +85°C	16 Plastic DIP
DG412EGE	-40°C to +85°C	16 QFN-EP*
DG412DY	-40°C to +85°C	16 Narrow SO
DG412DK	-40°C to +85°C	16 CERDIP
DG412AK	-55°C to +125°C	16 CERDIP**
DG412MY/PR	-55°C to +125°C	16 SO***
DG412MY/PR-T	-55°C to +125°C	16 SO***
<b>DG413CJ</b>	0°C to +70°C	16 Plastic DIP
DG413CUE	0°C to +70°C	16 TSSOP
DG413EUE	-40°C to +85°C	16 TSSOP
DG413CY	0°C to +70°C	16 Narrow SO
DG413C/D	0°C to +70°C	Dice†
DG413EGE	-40°C to +85°C	16 QFN-EP*
DG413DJ	-40°C to +85°C	16 Plastic DIP
DG413DY	-40°C to +85°C	16 Narrow SO
DG413DK	-40°C to +85°C	16 CERDIP
DG413AK	-55°C to +125°C	16 CERDIP**

†Contact factory for dice specifications.

\*EP = Exposed pad.

\*\*Contact factory for availability and processing to MIL-STD-883B.

\*\*\*Contact factory for availability.

## Chip Topography



# Improved, Quad, SPST Analog Switches

## Pin Configurations/Functional Diagrams (continued)



# Improved, Quad, SPST Analog Switches

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QFN-EP	G1655-3	<a href="#">21-0091</a>
16 Plastic DIP	P16-1	<a href="#">21-0043</a>
16 TSSOP	U16-2	<a href="#">21-0066</a>
16 CERDIP	J16-3	<a href="#">21-0045</a>
16 Narrow SO	S16-1	<a href="#">21-0041</a>
16 SO	S16-1	<a href="#">21-0041</a>

DG411/DG412/DG413

# **Improved, Quad, SPST Analog Switches**

## **Revision History**

<b>REVISION NUMBER</b>	<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
6	9/07	Addition of exposed pad information	1, 6, 9, 14, 15
7	9/08	Addition of rugged plastic information	1, 9

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(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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