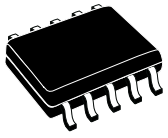
L6564T

10-pin transition-mode PFC controller

Features

- Guaranteed for extreme temperature range (outdoor)
- Fast “bi-directional” input voltage feedforward ($1/V^2$ correction)
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- AC brownout detection
- Low (≤100 µA) startup current
- 6 mA max. operating bias current
- 1% (@ T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SSOP10 package

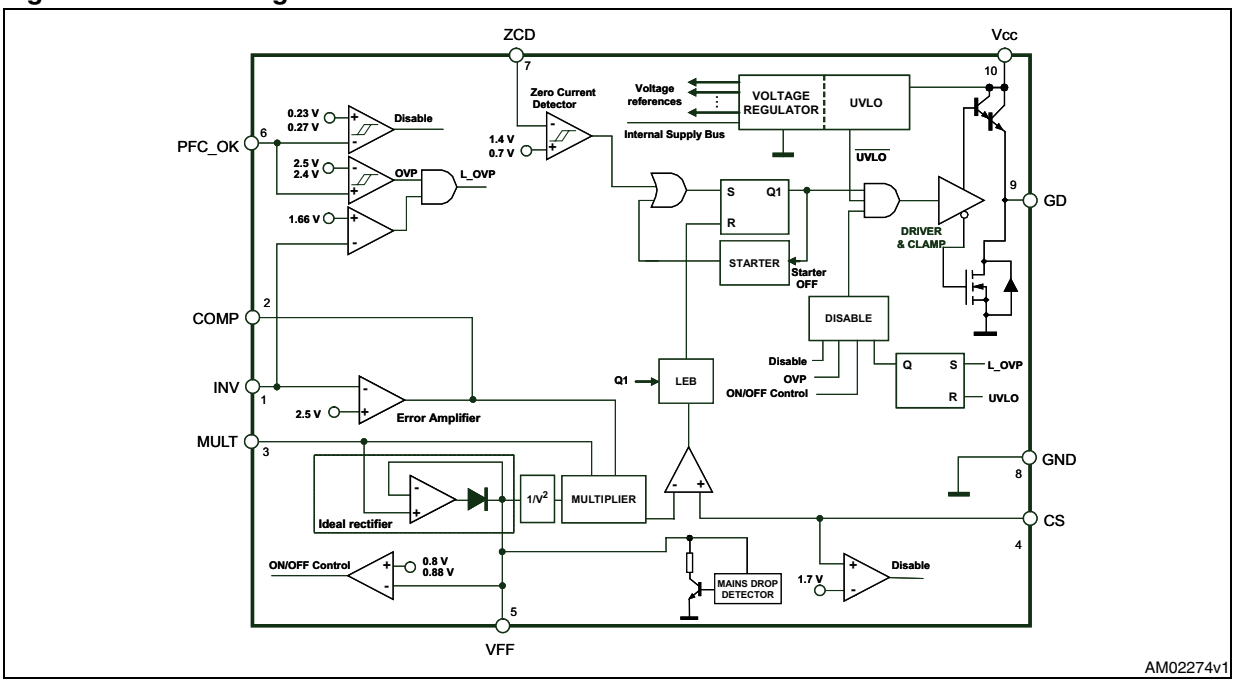


SSOP10

Applications

- PFC pre-regulators for:
  - High-end AC-DC adapter/charger
  - Desktop PC, server, web server
  - IEC61000-3-2 or JEITA-MITI compliant SMPS
- SMPS for LED luminaires

Figure 1. Block diagram



Contents

List of tables

List of figures

1 Description

The L6564T is a current-mode PFC controller operating in transition mode (TM) and represents the compact version of the L6563S as it embeds the same driver, reference and control stages in a very compact 10-pin SO package.

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @T_J = 25 °C) internal voltage reference. The loop stability is optimized by the voltage feedforward function ($1/V^2$ correction), which in this IC uses a proprietary technique that also considerably improves line transient response in case of both mains drops and surges (“bidirectional”).

In addition to overvoltage protection able to control the output voltage during transient conditions, the IC also provides protection against feedback loop failures or erroneous settings. Other on-board protection functions allow brownout conditions and boost inductor saturation to be safely handled.

The totem-pole output stage, capable of a 600 mA source and 800 mA sink current, is suitable for a high power MOSFET or IGBT drive. This, combined with the other features and the possibility to operate with ST's proprietary fixed-off-time control, makes the device an excellent solution for SMPS up to 400 W that requires compliance with EN61000-3-2 and JEITA-MITI standards.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
Vcc	10	IC supply voltage (Icc ≤20 mA)	Self-limited	V
---	1, 3, 6	Max. pin voltage (I_{pin} ≤1 mA)	Self-limited	V
---	2, 4, 5	Analog inputs and outputs	-0.3 to 8	V
I_{ZCD}	7	Zero current detector max. current	-10 (source) 10 (sink)	mA
VFF pin	5	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” Acceptance criteria: “normal performance”	+/- 1750	V
Other pins	1 to 4 6 to 10		+/- 2000	V

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction-to-ambient	120	°C/W
Ptot	Power dissipation @T_A = 50 °C	0.75	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Pin connection

Figure 2. Pin connection

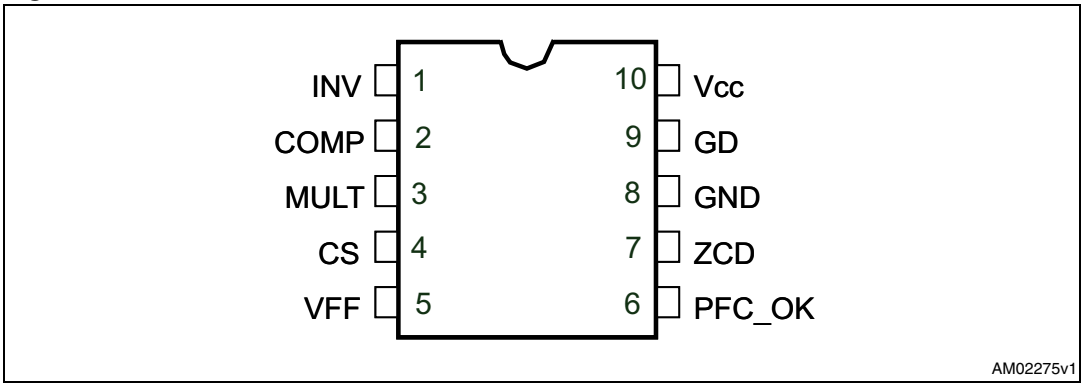


Table 3. Pin description

n°	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD. To avoid uncontrolled rise of the output voltage at zero load, when the voltage on the pin falls below 2.4 V the gate driver output is inhibited (burst-mode operation).
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. A second comparison level at 1.7 V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage on pin MULT (3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND but with a resistor ranging from 100 K ohm (minimum) to 2 M ohm (maximum). This pin is internally connected to a comparator in order to provide the brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The IC restarts as the voltage at the pin goes above 0.88 V.

Table 3. Pin description (continued)

n°	Name	Function
6	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if at the same time the voltage of the INV pin falls below 1.66 V, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling Vcc. bringing its value lower than 6 V before moving up to the turn-on threshold. If the voltage on this pin is brought below 0.23 V the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can be used as a remote on/off control input.
7	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
8	GND	Ground. Current return for both the signal part of the IC and the gate driver.
9	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages.
10	Vcc	Supply voltage of both the signal part of the IC and the gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.

4 Electrical characteristics

T_J = -40 to 125 °C, V_{CC} = 12 V, C_O = 1 nF between pin GD and GND, C_{FF} = 1 µF and R_{FF} = 1 MΩ between pin V_{FF} and GND; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Vcc	Operating range	After turn-on	10.3		22.5	V
Vcc_{On}	Turn-on threshold	(1)	11	12	13.2	V
Vcc_{Off}	Turn-off threshold	(1)	8.7	9.5	10.5	V
$Vcc_{restart}$	Vcc for resuming from latch	OVP latched	5	6	7	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener voltage	Icc = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, Vcc=10 V		90	180	µA
I_q	Quiescent current	After turn-on, V_{MULT} = 1 V		4	5.5	mA
I_{CC}	Operating supply current	@ 70 kHz		5	6.0	mA
I_{qdis}	Idle state quiescent current	V_{PFC_OK}> $V_{PFC\_OK\_S}$ AND V_{INV} < V_{FFD}		180	320	µA
		V_{PFC_OK}<$V_{PFC\_OK\_D}$		1.5	2.5	µA
I_q	Quiescent current	V_{PFC_OK}>$V_{PFC\_OK\_S}$ OR VCOMP<2.3V		2.2	3.2	µA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V		-0.2	-1	µA
V_{MULT}	Linear operation range		0 to 3			V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5		V
ΔVcs ΔV_{MULT}	Output max. slope	V_{MULT} = 0 to 0.4 V, V_{VFF} = 1 V V_{COMP} = upper clamp	1.33	1.66		V/V
K_M	Gain (2)	V_{MULT} = 1 V, V_{COMP}= 4 V	0.375	0.45	0.525	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.3 V < Vcc < 22.5 V (3)	2.45		2.55	
	Line regulation	Vcc = 10.3 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 4 V		-0.2	-1	µA
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	8	9		V
Gv	Voltage gain	Open loop	60	80		dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	1.5	4		mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Burst-mode voltage	(3)	2.3	2.4	2.5	
	Lower clamp voltage	I_{SINK} = 0.5 mA (3)	2.1	2.25	2.4	
Boost inductor saturation detector						
V_{CS_th}	Threshold on current sense	(3)	1.6	1.7	1.8	V
I_{INV}	E/A input pull-up current	After $V_{CS} > V_{CS\_th}$, before restarting	5	10	13	µA
Startup timer						
t_{START_DEL}	Startup delay	First cycle after wake-up	20	50	100	µs
t_{START}	Timer period		75	150	350	µs
		Restart after $V_{CS} > V_{CS\_th}$	150	300	700	
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			1	µA
t_{LEB}	Leading edge blanking		70	150	300	ns
$td_{(H-L)}$	Delay to output		70	200	350	ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = upper clamp, V_{MULT} =1 V, V_{VFF} = 1 V	0.97	1.08	1.2	V
Vcs_{ofst}	Current sense offset	V_{MULT} = 0 V, V_{VFF} = 3 V		40	70	mV
		V_{MULT} = 3 V, V_{VFF} = 3 V		20		
PFC_OK functions						
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.6 V		-0.1	-1	µA
$V_{PFC\_OK\_C}$	Clamp voltage	I_{PFC_OK} = 1 mA	8.5	9.5		V
$V_{PFC\_OK\_S}$	OVP threshold	(1) Voltage rising	2.435	2.5	2.565	V
$V_{PFC\_OK\_R}$	Restart threshold after OVP	(1) Voltage falling	2.34	2.4	2.46	V
$V_{PFC\_OK\_D}$	Disable threshold	(1) Voltage falling	0.08		0.40	V
$V_{PFC\_OK\_D}$	Disable threshold	(1) Voltage falling Tj = 25 °C	0.17	0.23	0.29	V
$V_{PFC\_OK\_E}$	Enable threshold	(1) Voltage rising	0.10		0.43	V
$V_{PFC\_OK\_E}$	Enable threshold	(1) Voltage rising Tj = 25 °C	0.21	0.27	0.32	V
V_{FFD}	Feedback failure detection threshold (V_{INV} falling)	$V_{PFC\_OK} = V_{PFC\_OK\_S}$	1.61	1.66	1.71	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage feedforward						
V_{VFF}	Linear operation range		1		3	V
ΔV	Dropout V_{MULTpk}-V_{VFF}	Vcc < Vcc_{On}			850	mV
		Vcc > or = to Vcc_{On}			20	
ΔV_{VFF}	Line drop detection thresh.	Below peak value	30	70	110	mV
ΔV_{VFF}	Line drop detection thresh.	Below peak value Tj =25°C	50	70	90	mV
R_{DISCH}	Internal discharge resistor	Tj = 25 °C	7.5	10	12.5	kΩ
			5		20	
V_{DIS}	Disable threshold	(2) Voltage falling	0.725	0.8	0.875	V
V_{EN}	Enable threshold	(2) Voltage rising	0.845	0.88	0.915	V
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7		V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)		1.1	1.4	1.9	V
V_{ZCDT}	Triggering voltage (negative-going edge)		0.5	0.7	1	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V			1	µA
I_{ZCDsrc}	Source current capability		-2.0	-4		mA
I_{ZCDsnk}	Sink current capability		2.0	5		mA
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.4	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.5	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			30	60	ns
t_r	Voltage rise time			45	150	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc= 0 to V_{CCon}, I_{sink}= 2 mA			1.2	V

1. Parameters tracking each other.
2. The multiplier output is given by: $V_{CS} = V_{CS\_Ofst} + K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$
3. Parameters tracking each other.

5 Typical electrical performance

Figure 3. IC consumption vs. V_{CC}

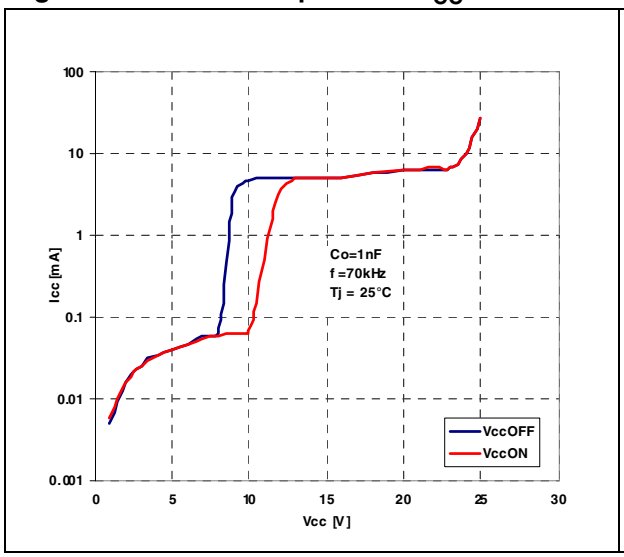


Figure 4. IC consumption vs. T_J

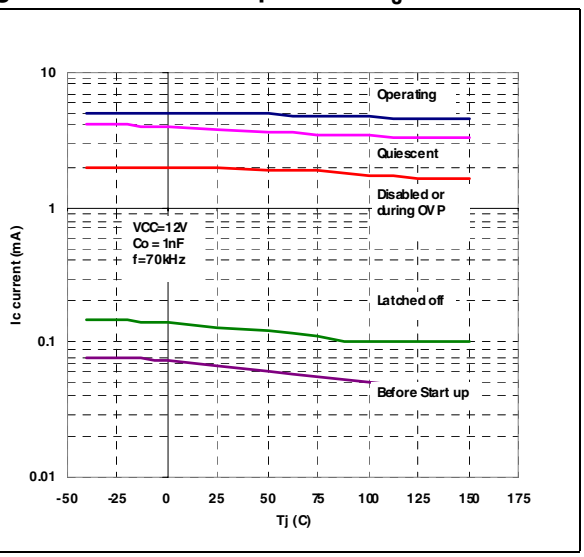


Figure 5. Vcc Zener voltage vs. T_J

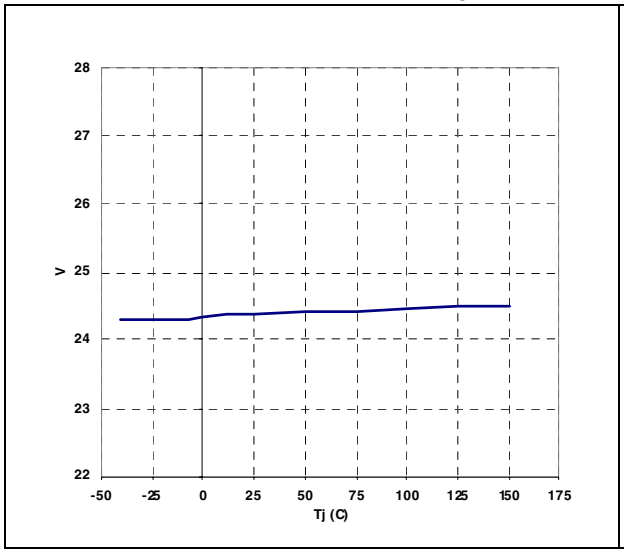


Figure 6. Startup and UVLO vs. T_J

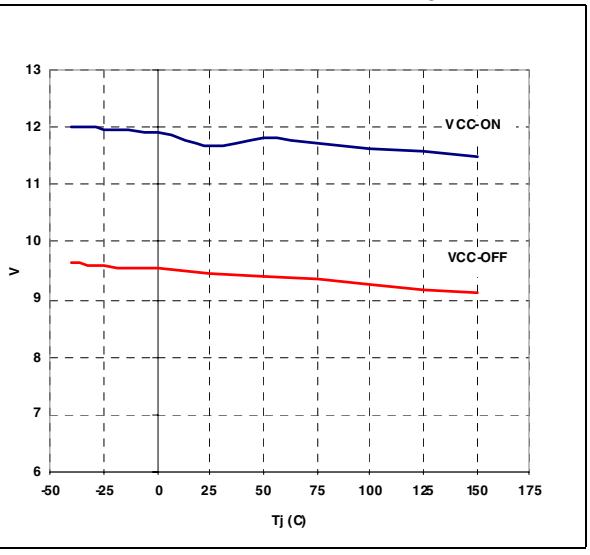


Figure 7. Feedback reference vs. T_J

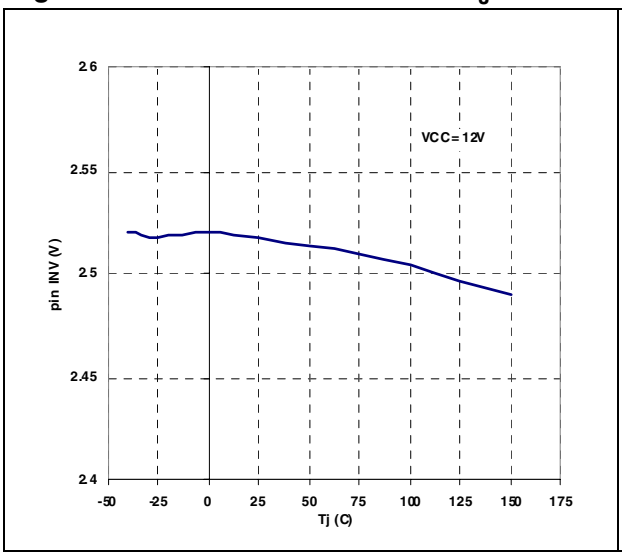


Figure 8. E/A output clamp levels vs. T_J

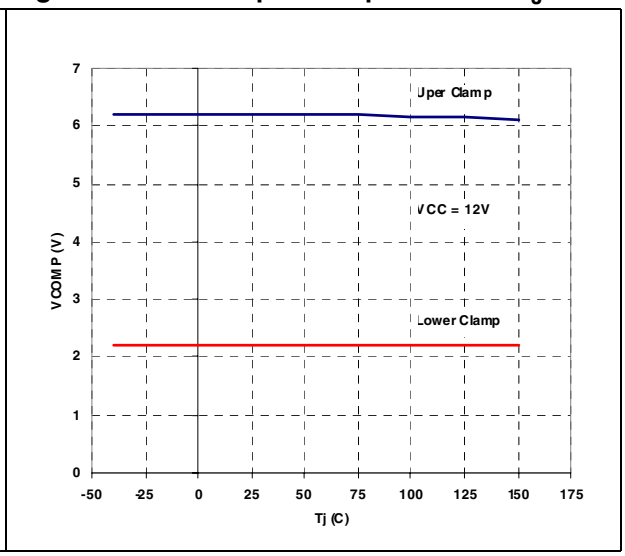


Figure 9. UVLO saturation vs. T_J

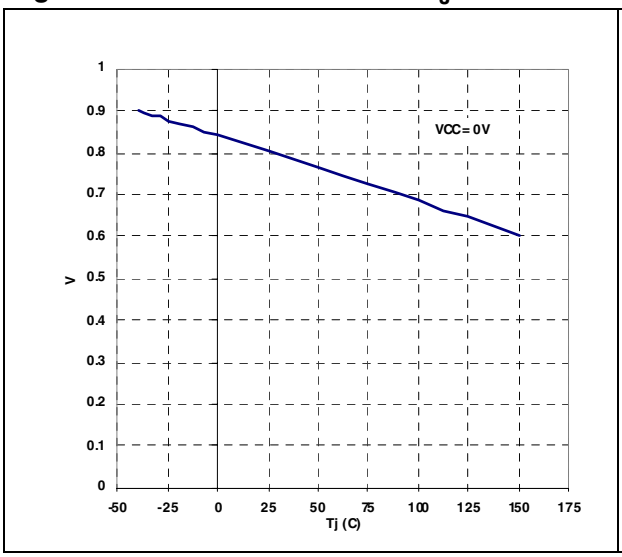


Figure 10. OVP levels vs. T_J

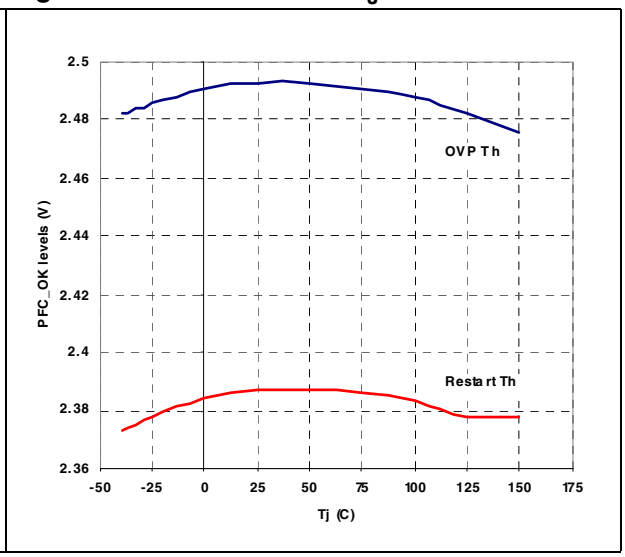


Figure 11. Inductor saturation threshold vs. T_J

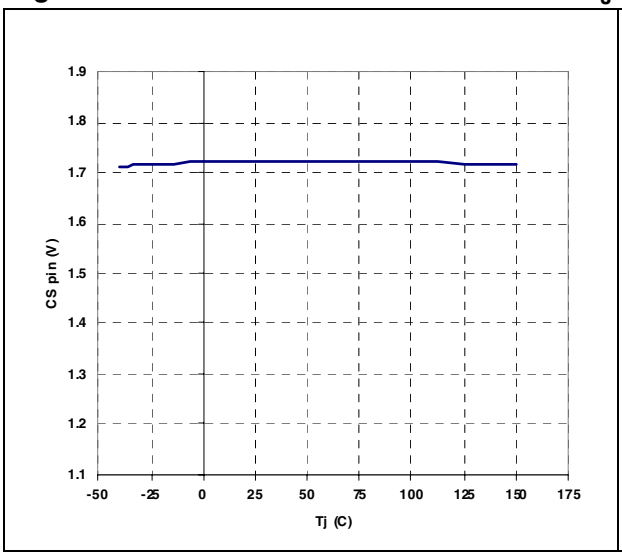


Figure 12. Vcs clamp vs. T_J

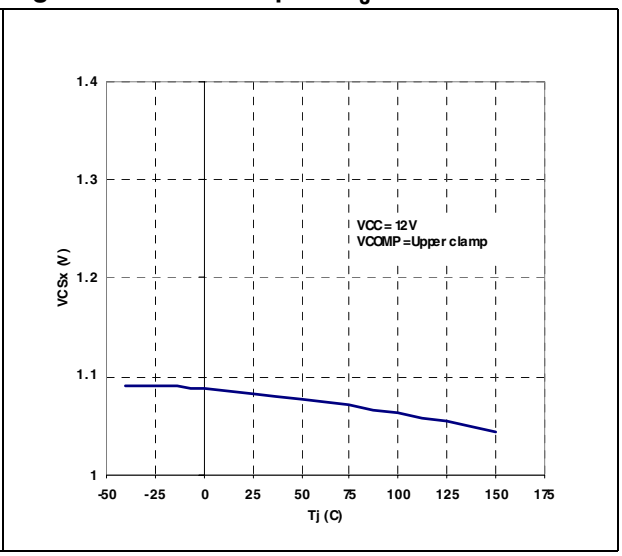


Figure 13. ZCD sink/source capability vs. T_J

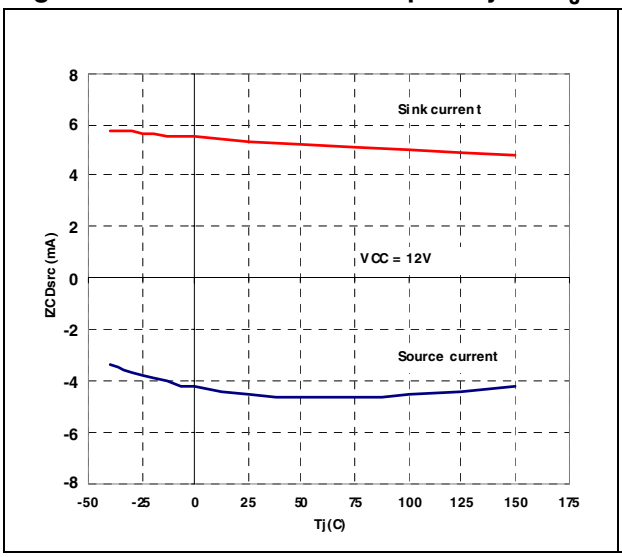


Figure 14. ZCD clamp level vs. T_J

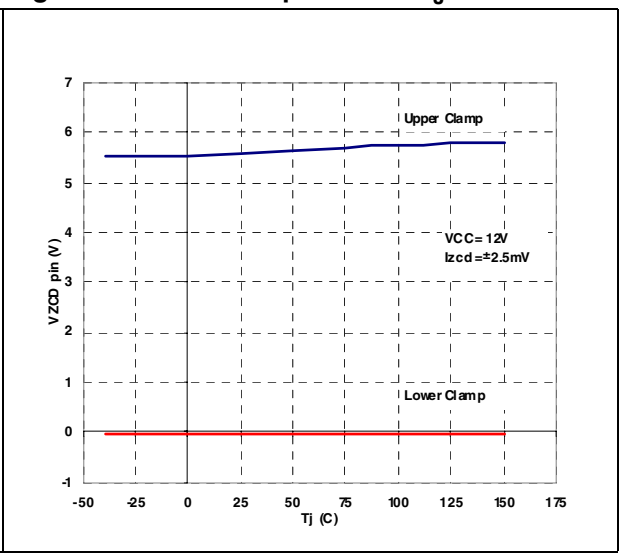


Figure 15. R discharge vs. T_J

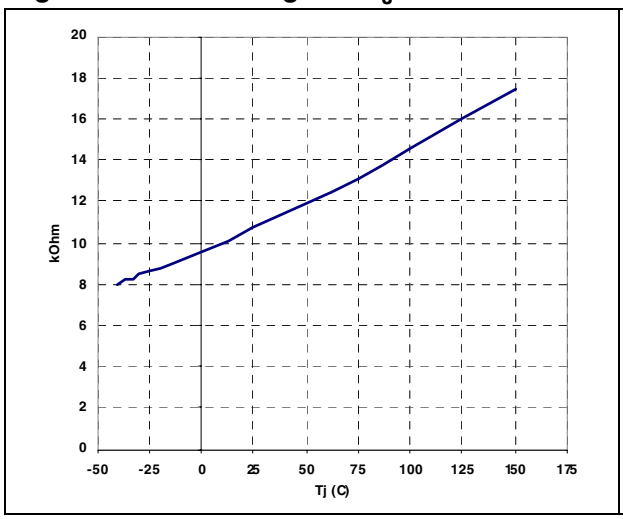


Figure 16. Line drop detection threshold vs. T_J

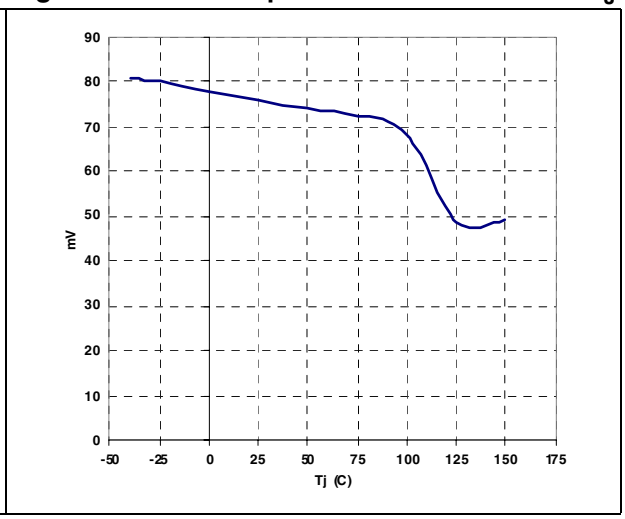


Figure 17. V_{MULTpk} - V_{VFF} dropout vs. T_J

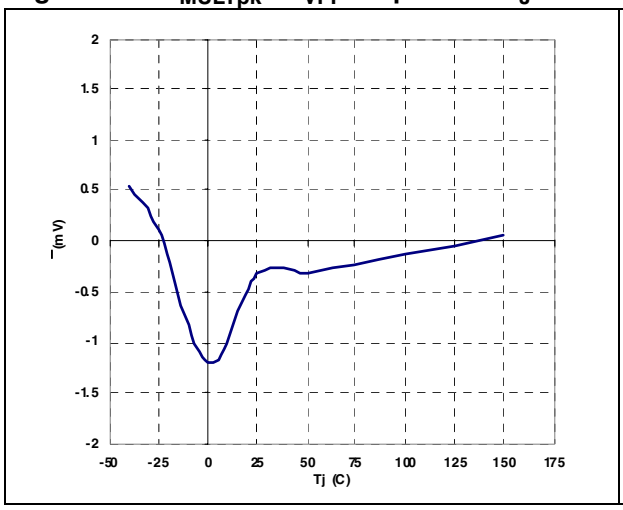


Figure 18. PFC_OK threshold vs. T_J

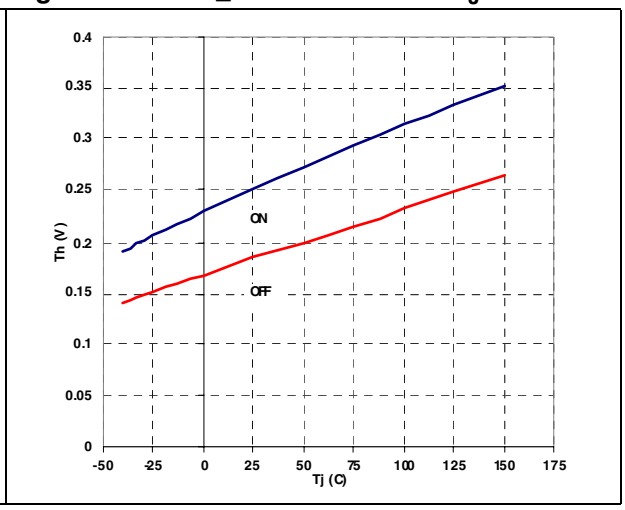


Figure 19. PFC_OK FFD threshold vs. T_J

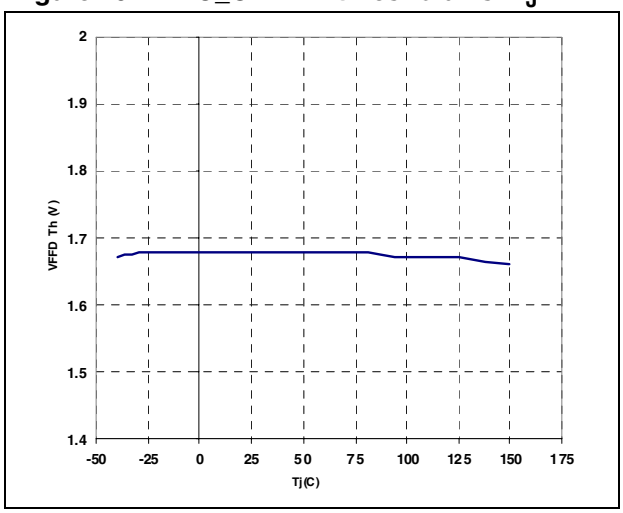


Figure 20. Multiplier characteristics @ V_{FF} = 1 V

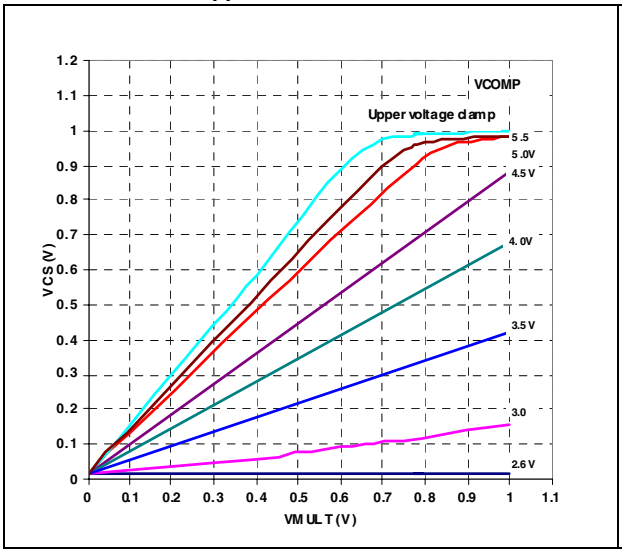


Figure 21. Multiplier characteristics @ V_{FF} = 3 V

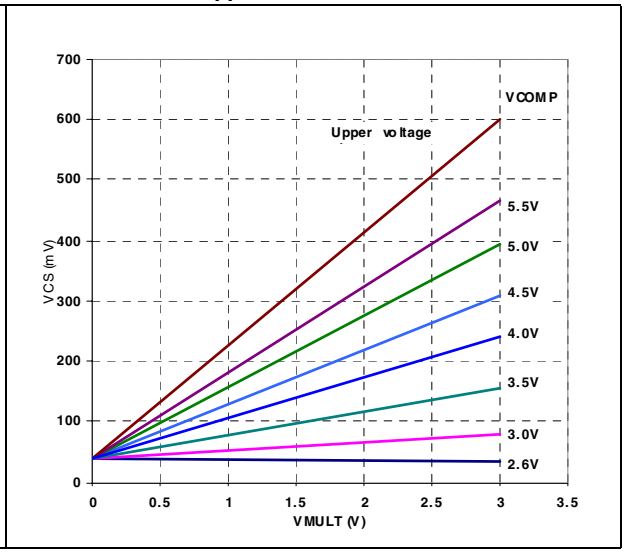


Figure 22. Multiplier gain vs. T_J

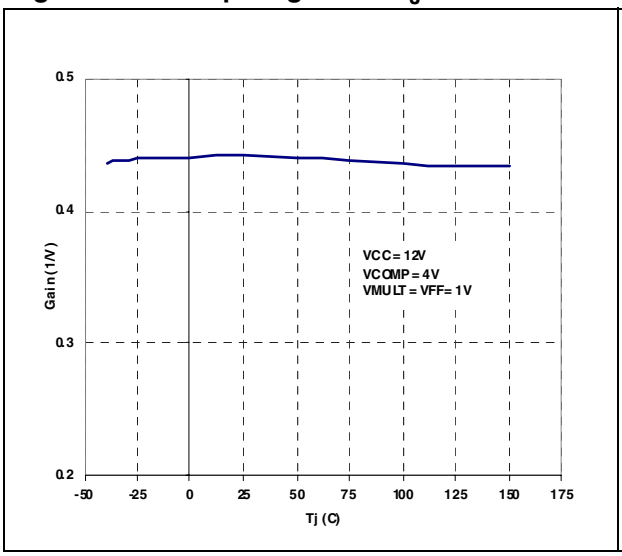


Figure 23. Gate drive clamp vs. T_J

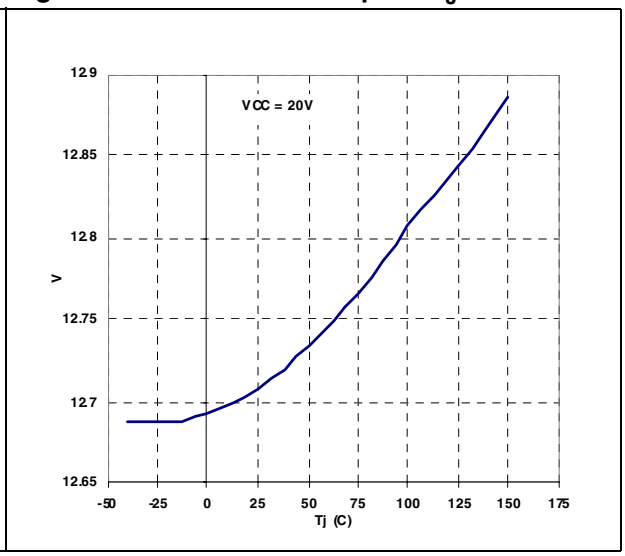


Figure 24. Gate drive output saturation vs. T_J

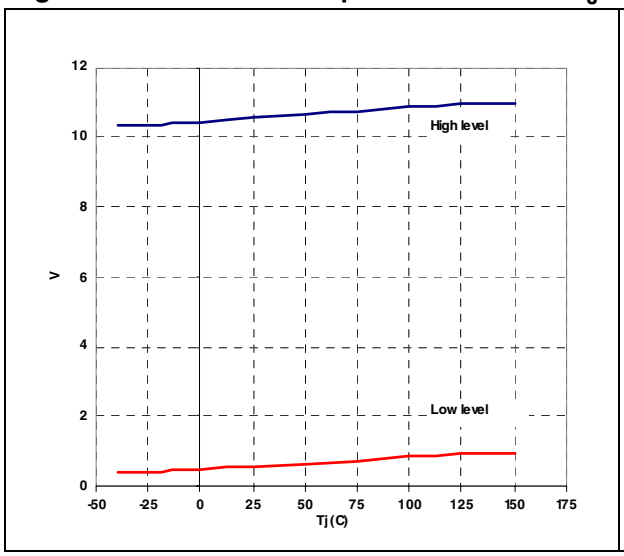


Figure 25. Delay to output vs. T_J

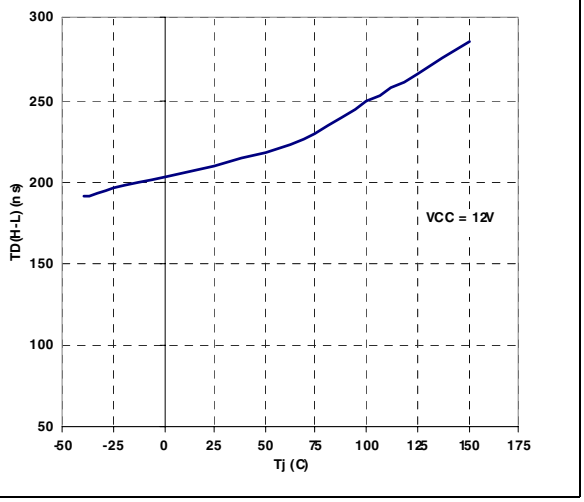
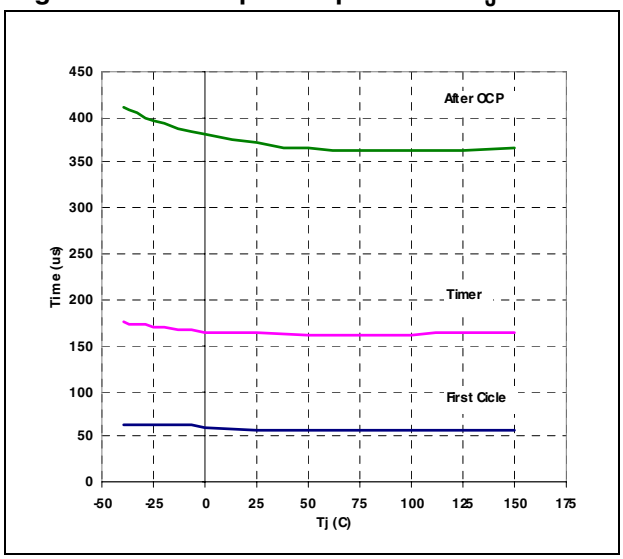


Figure 26. Startup timer period vs. T_J



6 Application information

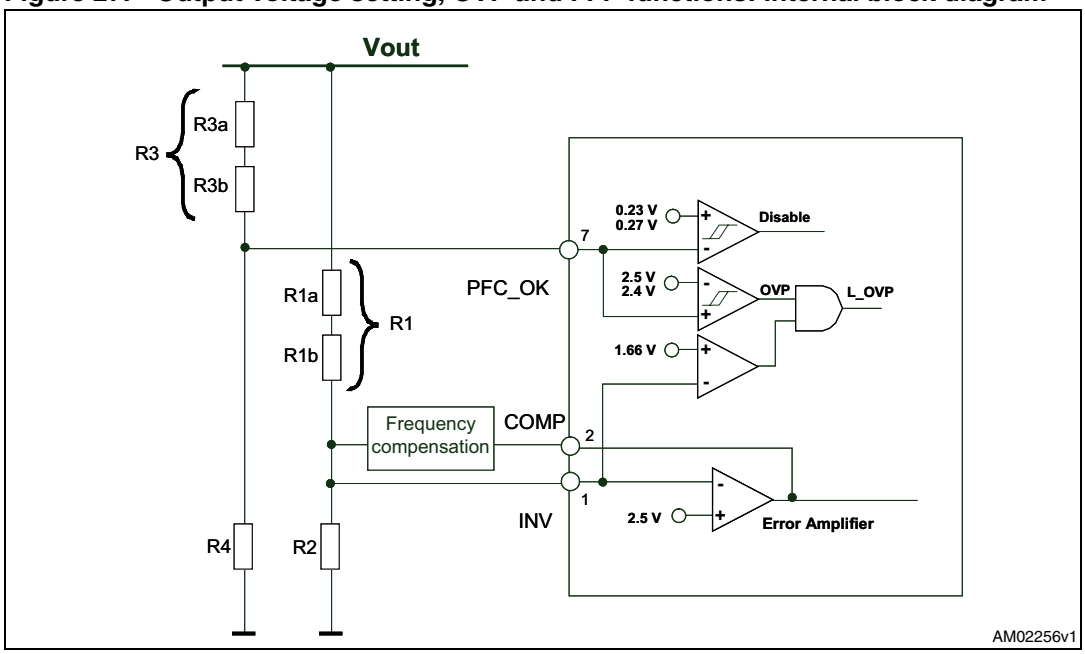
6.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage Vo of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. A pin of the device (PFC_OK) has been dedicated to monitor the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 27*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected.

Example: V_O = 400 V, V_{OX} = 434 V. Select: R3 = 8.8 MΩ; then: R4 = 8.8 MΩ·2.5/(434-2.5) = 51 kΩ

When this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. Note that R1, R2, R3 and R4 can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the bias current of both INV and PFC_OK pins.

Figure 27. Output voltage setting, OVP and FFP functions: internal block diagram



6.2 Feedback failure protection (FFP)

The OVP function described above handles “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the overvoltage is generated by a feedback disconnection, for instance when the upper resistor of the output divider (R1) fails to open, the comparator detects the voltage at pin INV. If the voltage is lower than 1.66 V and the OVP is active, the FFP is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of the L6564T goes below 6 V.

The pin PFC_OK doubles its function as a not-latched IC ‘Disable’: a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

Note that these functions offer complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating results in shutting down the IC and stopping the pre-regulator.

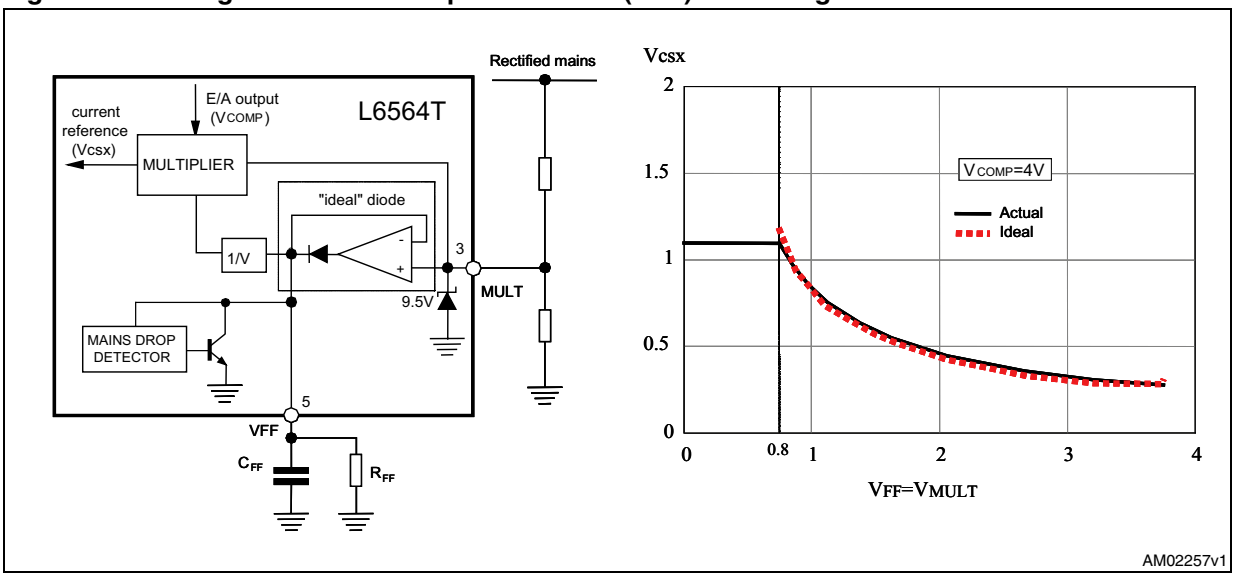
6.3 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency FC of the overall open-loop gain because the gain has a single pole characteristic. This leads to a large trade-off in the design.

For example, setting the gain of the error amplifier to get FC = 20 Hz @ 264 Vac means having FC 4 Hz @ 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feedforward can compensate for the gain variation with the line voltage and allow the minimizing of all the above-mentioned issues. It consists in deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 28*).

Figure 28. Voltage feedforward: squarer/divider (1/V^2) block diagram and transfer characteristic



In this way a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which significantly improves dynamic behavior at low line and simplifies loop design.

In fact, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6564T realizes a NEW voltage feed forward that, with a technique that makes use of just two external parts, strongly minimizes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor RFF, both connected from pin VFF (#5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (#3). In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode; in case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges C_{FF} avoiding long settling time before reaching the new voltage level. The discharge of C_{FF} is stopped as its voltage equals the voltage on the MULT pin or if the voltage on the VFF pin falls below 0.88 V, to prevent the “Brownout protection” function from being improperly activated (see *Section 6.3*).

As a result of the VFF pin functionality, an acceptably low steady-state ripple and low current distortion can be achieved with a limited undershoot or overshoot on the pre-regulator's output.

The twice-mains-frequency ($2 \cdot f_L$) ripple appearing across C_{FF} is triangular with a peak-to-peak amplitude that, with good approximation, is given by:

$$\Delta V_{FF} = \frac{2 V_{MULTpk}}{1 + 4 f_L R_{FF} C_{FF}}$$

where f_L is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its $2 \cdot f_L$ component, is:

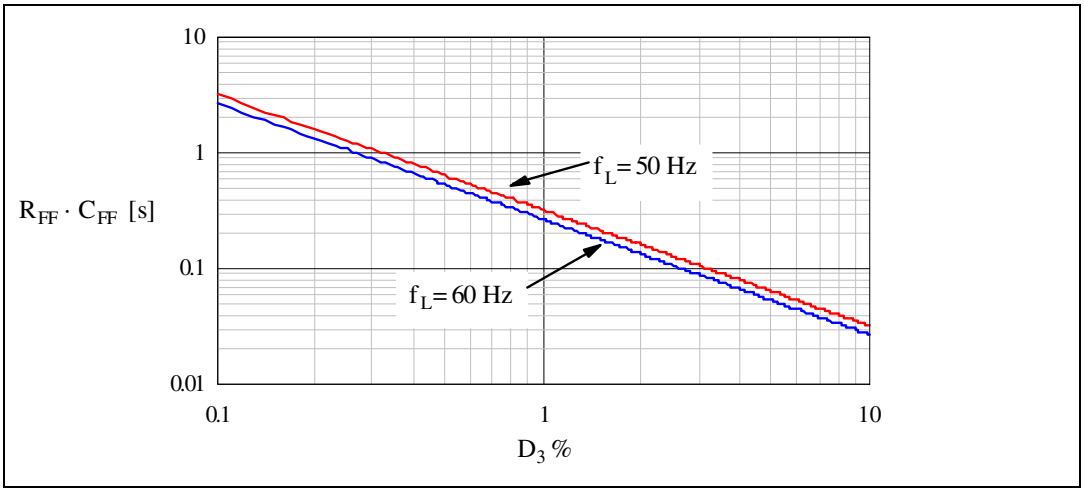
$$D_3\% = \frac{100}{2\pi f_L R_{FF} C_{FF}}$$

Figure 29 shows a diagram that helps choose the time constant $R_{FF} \cdot C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion. Note that there is a minimum value for the time constant $R_{FF} \cdot C_{FF}$ below which improper activation of the VFF fast discharge may occur. In fact, the twice-mains-frequency ripple across C_{FF} under steady-state conditions must be lower than the minimum line drop detection threshold (ΔV_{FF_min} = 40 mV). Therefore:

$$R_{FF} \cdot C_{FF} > \frac{2 \frac{V_{MULTpk\_max}}{\Delta V_{VFF\_min}} - 1}{4 f_{L\_min}}$$

Always connect RFF and CFF to the pin, the IC does not work properly if the pin is either left floating or connected directly to ground.

Figure 29. $R_{FF} \cdot C_{FF}$ as a function of 3rd harmonic distortion introduced in the input current



6.4 THD optimizer circuit

The L6564T is provided with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (total harmonic distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 30 shows the internal block diagram of the THD optimizer circuit.

Figure 30. THD optimizer circuit

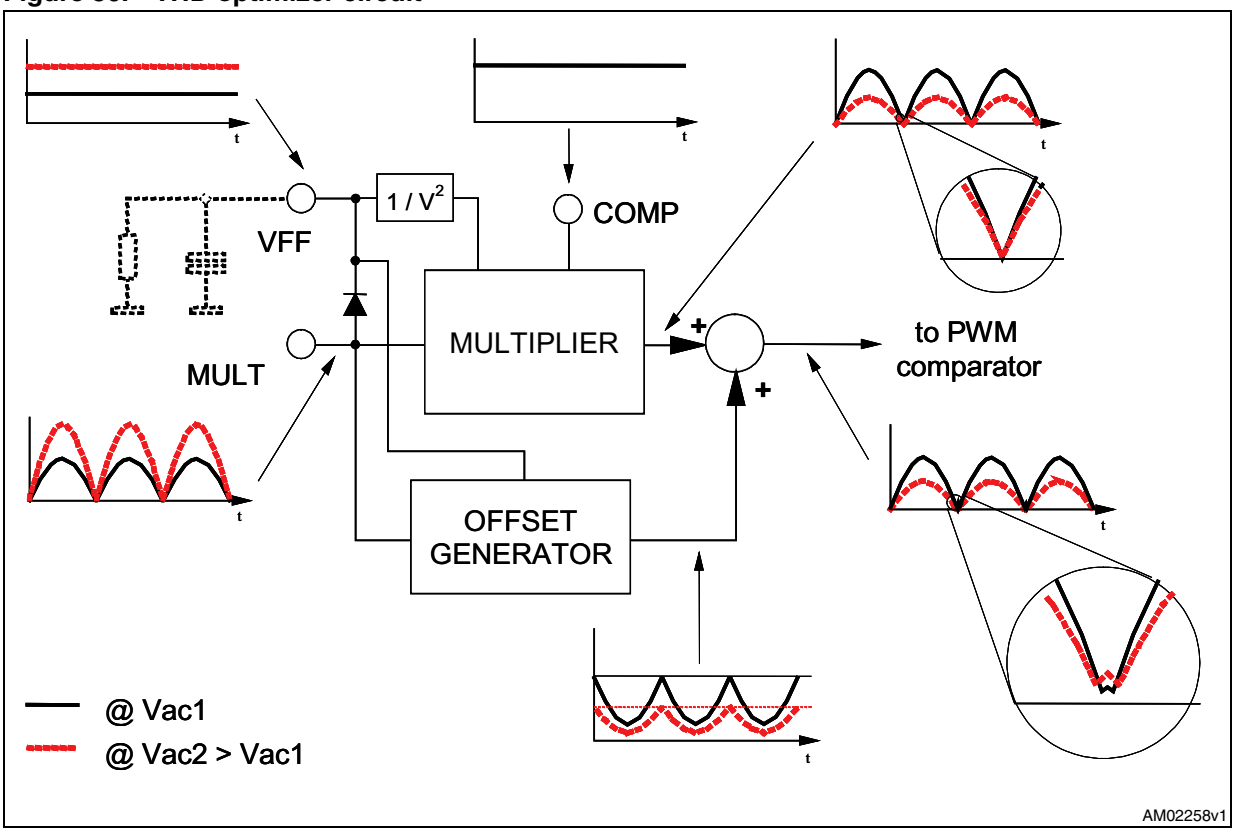
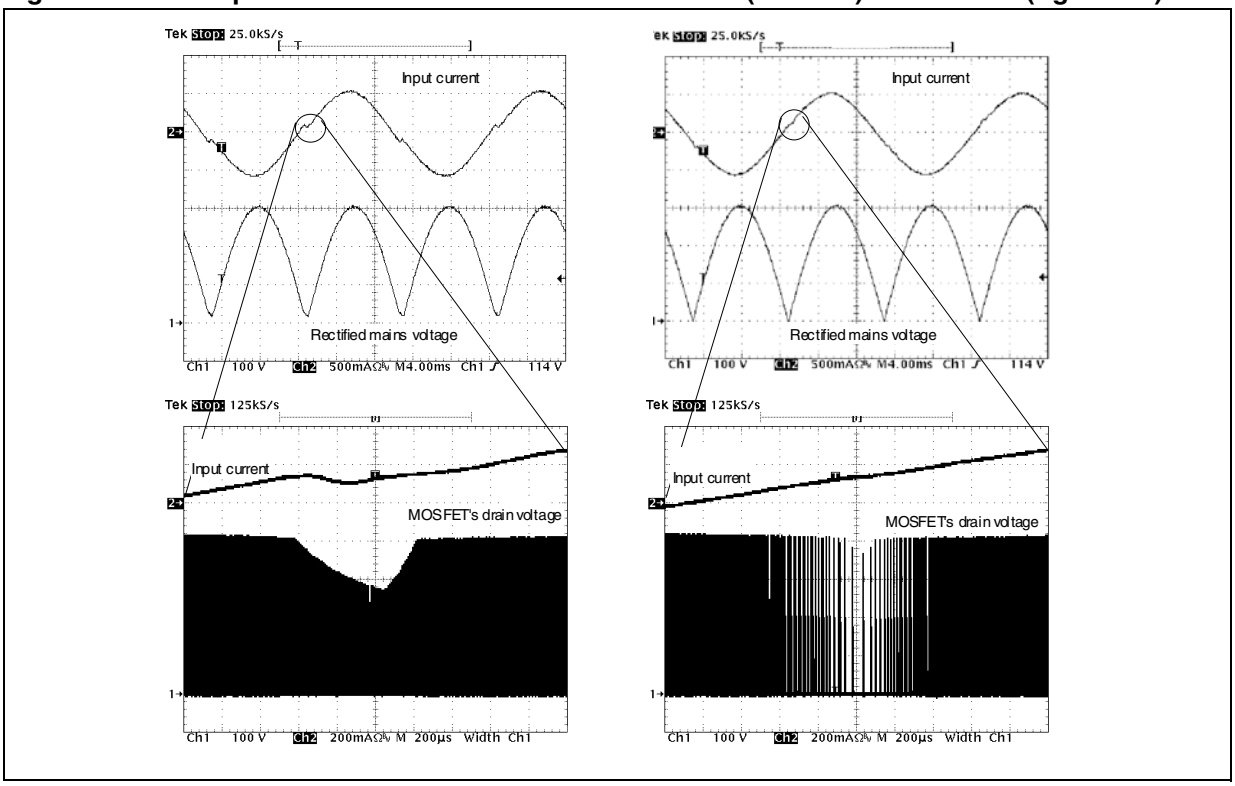


Figure 31. THD optimization: standard TM PFC controller (left side) and L6564T (right side)



Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the VFF pin (see *Section 6.3*) so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

The effect of the circuit is shown in *Figure 31*, where the key waveforms of a standard TM PFC controller are compared to those of this chip.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - therefore reducing the effectiveness of the optimizer circuit.

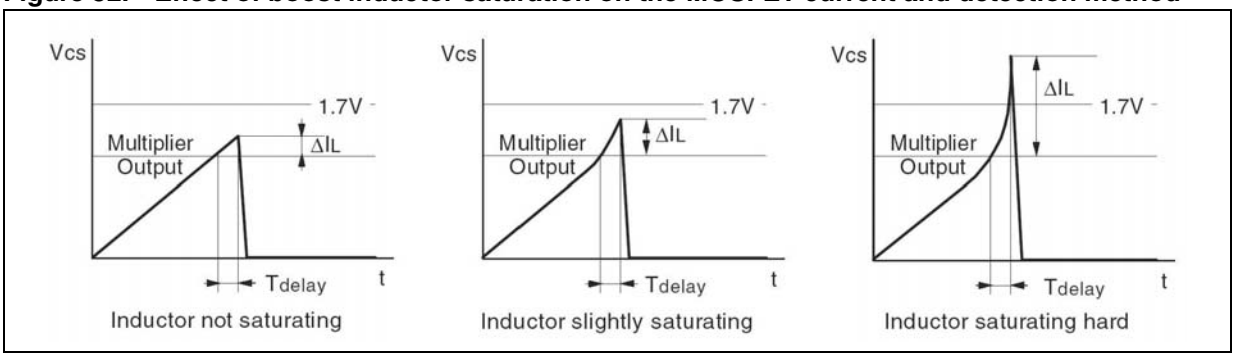
6.5 Inductor saturation detection

The boost inductor's hard saturation may be a fatal event for a PFC pre-regulator: the current up-slope becomes so large (50-100 times steeper, see *Figure 32*) that during the current sense propagation delay the current may reach abnormally high values. The voltage drop caused by this abnormal current on the sense resistor reduces the gate-to-source voltage, so that the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after few switching cycles.

However, in some applications such as AC-DC adapters, where the PFC pre-regulator is turned off at light load for energy saving reasons, even a well-designed boost inductor may occasionally slightly saturate when the PFC stage is restarted because of a larger load demand. This happens when the restart occurs at an unfavorable line voltage phase, i.e. when the output voltage is significantly below the rectified peak voltage. As a result, in the boost inductor the inrush current coming from the bridge rectifier adds up to the switched current and, furthermore, there is little or no voltage available for demagnetization.

To cope with a saturated inductor, the L6564T is provided with a second comparator on the current sense pin (CS, pin 4) that stops the IC if the voltage, normally limited within 1.1 V, exceeds 1.7 V. After that, the IC is attempted to restart by the internal starter circuitry; the starter repetition time is twice the nominal value to guarantee lower stress for the inductor and boost diode. Hence, the system safety is considerably increased.

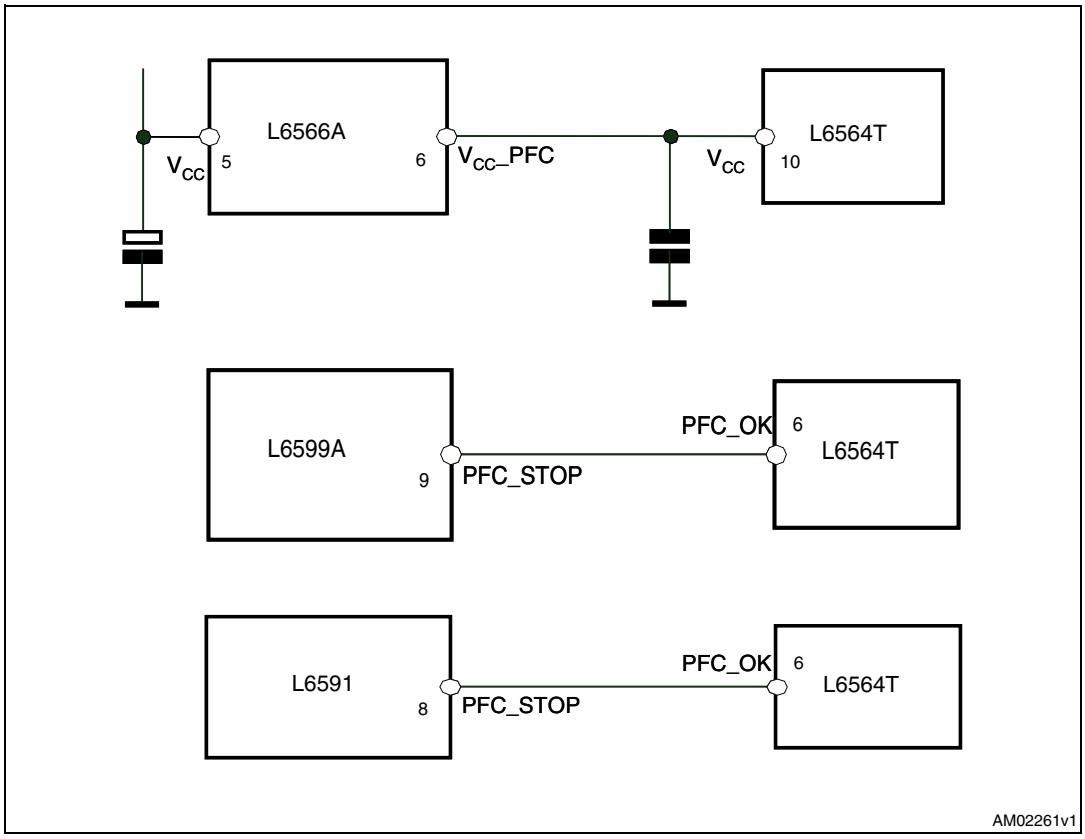
Figure 32. Effect of boost inductor saturation on the MOSFET current and detection method



6.6 Power management/housekeeping functions

A communication line with the control IC of the cascaded DC-DC converter can be established via the disable function included in the PFC_OK pin (see *Section 6.2* for more details). This line is typically used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6564T in case of light load and to minimize the no-load input consumption. Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. The interface circuits are shown in *Figure 32*. Needless to say, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage.

Figure 33. Interface circuits that let DC-DC converter's controller IC disable the L6564T



Another function available is the brownout protection which is basically a not-latched shutdown function that is activated when a condition of mains undervoltage is detected. This condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to function in open loop and this may be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power-down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shut down the unit in case of brownout. The brownout threshold is internally fixed at 0.8 V and is sensed on pin VFF (5) during the voltage falling and an 80 mV threshold hysteresis prevents rebounding at input voltage turn-off. In *Table 5* it is possible to find a summary of all of the above mentioned working conditions that cause the device to stop operating.

Table 5. Summary of L6564 idle states

Condition	Caused or revealed by	IC behavior	Restart condition	Typical IC consumption
UVLO	$Vcc < Vcc_{Off}$	Disabled	$Vcc > Vcc_{On}$	90 µA
Feedback disconnected	$PFC\_OK > V_{PFC\_OK\_S}$ and INV < 1.66 V	Latched	$Vcc < Vcc_{restart}$ then $Vcc > Vcc_{On}$	180 µA
Standby	$PFC\_OK < V_{PFC\_OK\_D}$	Stop switching	$PFC\_OK > V_{PFC\_OK\_E}$	1.5 mA
AC brownout	$VFF < V_{DIS}$	Stop switching	$RUN > V_{EN}$	1.5 mA
OVP	$PFC\_OK > V_{PFC\_OK\_S}$	Stop Switching	$PFC\_OK < V_{PFC\_OK\_R}$	2.2 mA
Low consumption	COMP < 2.4 V	Burst mode	COMP > 2.4V	2.2 mA
Saturated boost inductor	$Vcs > V_{CS\_th}$	Doubled T_{start}	Auto restart	2.2 mA

7 Application examples and ideas

Figure 34. Demonstration board EVL6564-100W, wide-range mains: electrical schematic

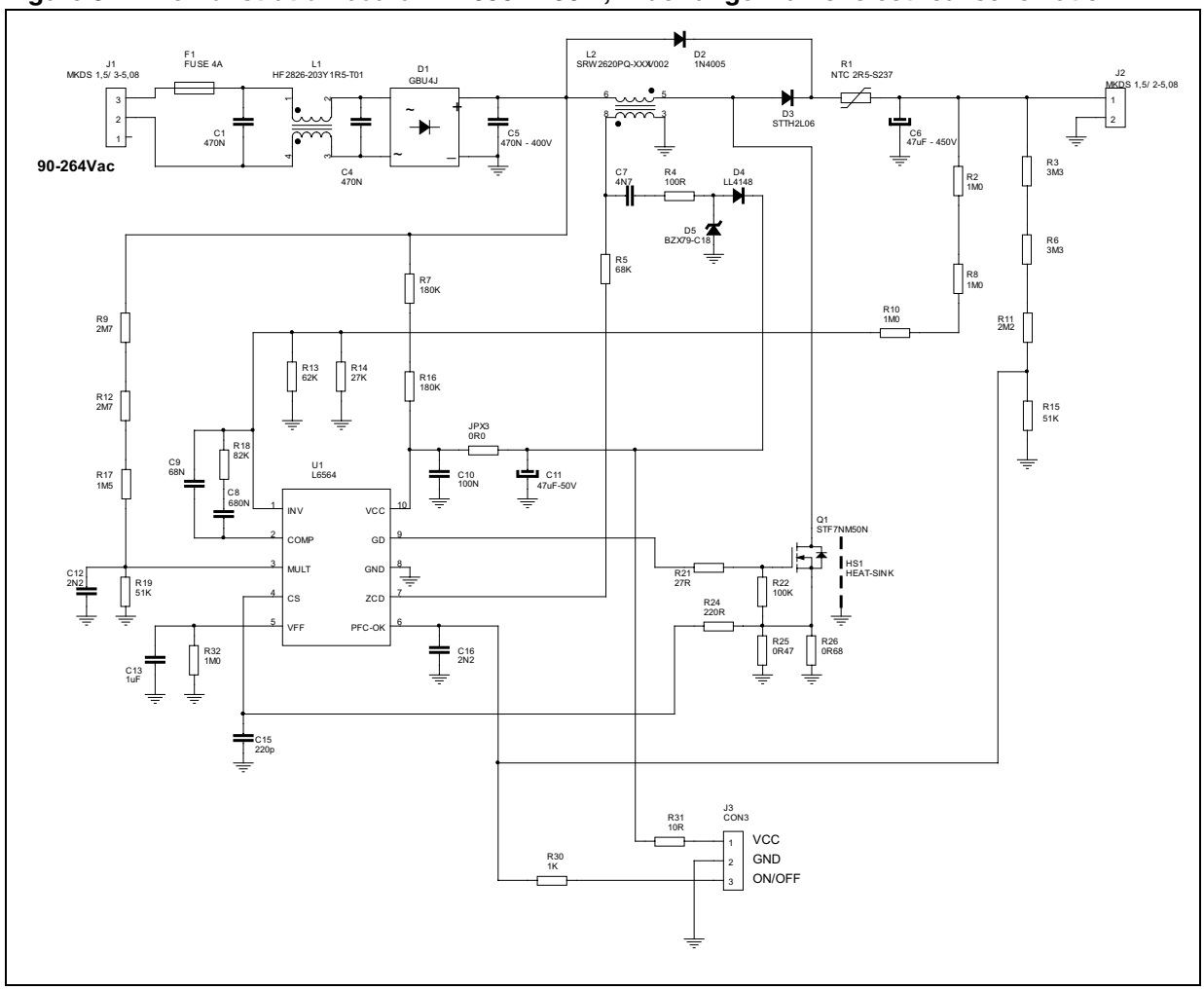


Figure 35. L6564 100 W TM PFC: compliance with EN61000-3-2 standard

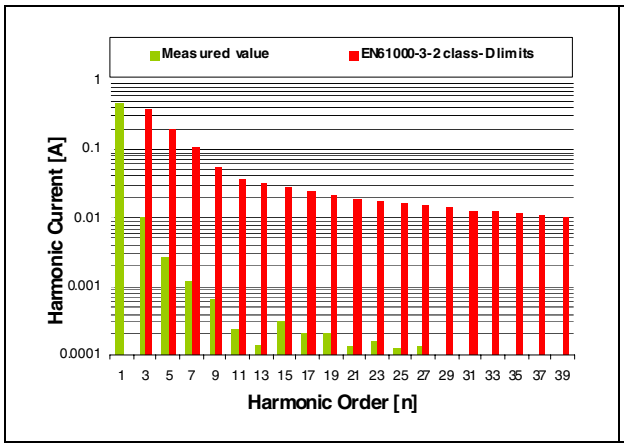


Figure 36. L6564 100 W TM PFC: compliance with JEITA-MITI standard

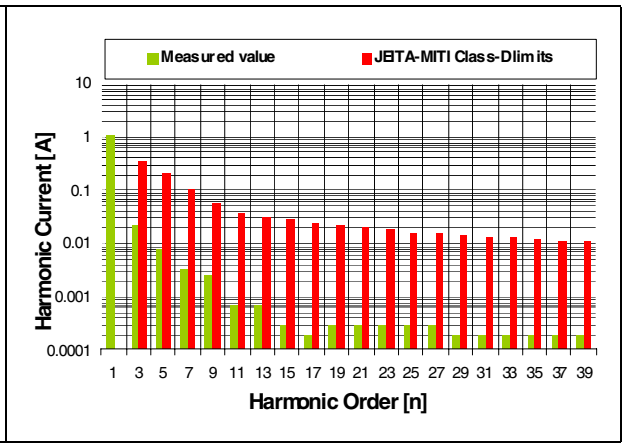


Figure 37. L6564 100 W TM PFC: input current waveform @230-50 Hz - 100 W load

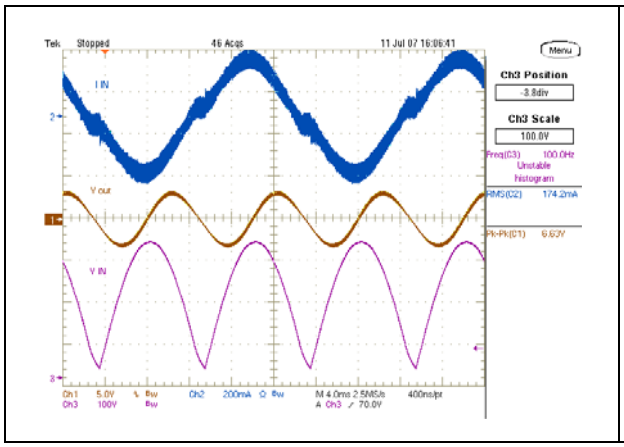
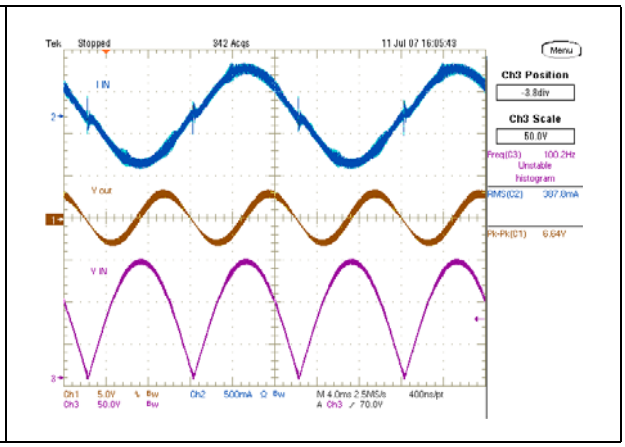


Figure 38. L6564 100W TM PFC: input current waveform @100 V-50 Hz - 100 W load



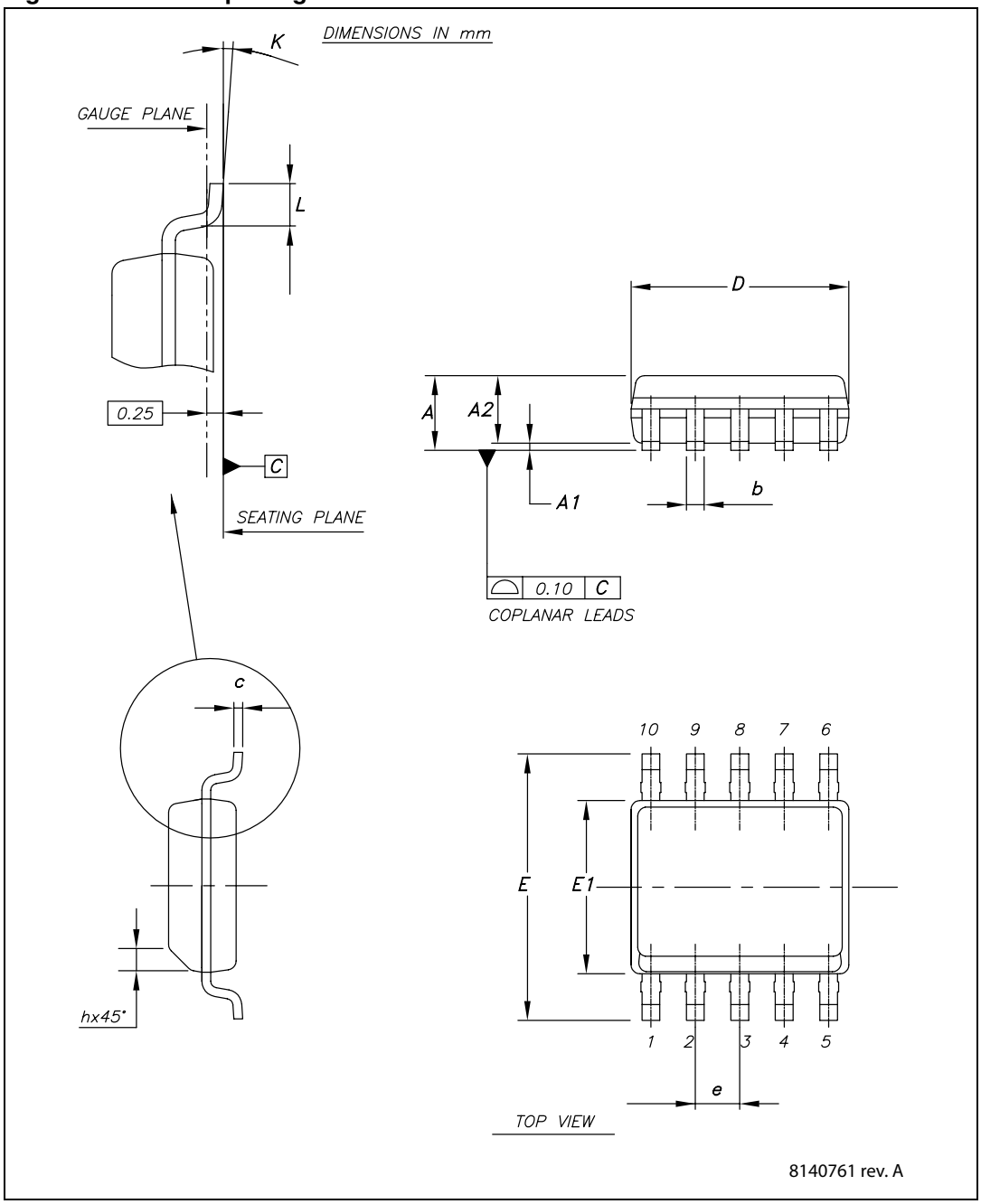
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 6. SSO10 mechanical data

Dim.	Databook (mm.)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
h	0.25		0.50
L	0.40		0.90
K	0°		8°

Figure 39. SSO10 package dimensions



9 Ordering codes

Table 7. Ordering information

Order codes	Package	Packing
L6564TD	SSO10	Tube
L6564TDTR		Tape and reel

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
18-Jan-2012	1	Initial release

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А