PIC18(L)F2X/4X/5XK42

Highly Integrated 8-Bit PIC® Microcontrollers in 28- to 48- Pins

Description

The PIC18(L)F2X/4X/5XK42 microcontroller family is available in 28/40/44/48-pin devices. This family features a 12-bit ADC with Computation (ADC^2) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and threshold comparison. Additionally, Vectored Interrupt Controller with fixed latency for handling interrupts, System Bus Arbiter, Direct Memory Access capabilities, UART with support for Asynchronous, DMX, DALI and LIN protocols, SPI, I^2C, memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - Up to 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Two Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User programmable source and destination sizes
  - Hardware and software triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed Interrupt latency
  - Programmable vector table base address
- 31-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-Out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware or software
- Programmable Code Protection:
  - Configurable Boot and App region sizes

Memory

- Up to 128 KB Flash Program Memory
- Up to 8 KB Data SRAM Memory
- Up to 1 KB Data EEPROM
- Memory Access Partition (MAP):
  - Bootloader write-protect
  - Configurable partition
- Device Information Area (DIA) Stores:
  - Temp sensor factory calibrated data
  - Fixed Voltage Reference
  - Device ID

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC18LF2X/4X/5XK42)
  - 2.3V to 5.5V (PIC18F2X/4X/5XK42)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- DOZE mode: Ability to run CPU core slower than the system clock
- IDLE mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest power consumption
- Peripheral Module Disable (PMD):
  - Ability to disable peripherals to minimize power consumption

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals

- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWGs):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Four 16-Bit Capture/Compare/16-Bit PWM (CCP) modules
- Four 10-bit Pulse Width Modulators (PWMs)

Digital Peripherals (Continued)

- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < f_{NCO} < 64 MHz
  - Resolution: f_{NCO}/220
- DSM: Data Signal Modulator:
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash
- Two UART Modules:
  - Asynchronous UART, RS-232, RS-485 compatible.
  - One of the UART modules supports LIN master and slave, DMX mode, DALI gear and device protocols
  - Automatic and user timed BREAK period generation
  - DMA compatible
  - Automatic checksums
  - Programmable 1, 1.5, and 2 Stop bits
  - Wake-up on BREAK reception
- One SPI module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Receive-without-transmit option
  - Transmit-without-receive option
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- Two I^2C modules, SMBus, PMBus™ compatible:
  - Dedicated address, transmit and receive buffers
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Multi-Master mode, including self-addressing
- Device I/O Port Features:
  - 25 I/O pins (PIC18(L)F24/25/26/27K42)
  - 36 I/O pins (PIC18(L)F45/46/47K42)
  - 44 I/O pins (PIC18(L)F55/56/57K42)
  - One input-only pin
  - Individually programmable I/O direction, controlled current, open-drain, slew rate, weak pull-up control
  - Interrupt-on-change
  - Three external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
  - 12-bit with up to 43 external channels
  - Automated post-processing
  - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Temperature Sensor
    - Internal connection to ADC
    - Can be calibrated for improved accuracy
  - Hardware Capacitive Voltage Divider (CVD):
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
    - Adjustable sample and hold capacitor array
    - Two guard ring output drives
- Two Comparators:
  - Comparator Hysteresis enable
  - Invert output polarity
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Connection to ADC, Comp and DAC

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 64 MHz
  - Safe clock switching while running
  - ±1% at calibration (nominal)
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator
- External Oscillator Block with:
  - x4 PLL with external sources
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripherals clock stops
- Oscillator Start-up Timer (OST)
  - Ensures stability of crystal oscillator sources

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TABLE 1: PIC18(L)F2X/4X/5XK42 FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KB)	Data EEPROM (B)	Data SRAM (bytes)	I/OPins	12-bit ADC^2 (ch)	5-bit DAC	Comparator	8-bit/16-bit Timer	Window Watchdog Timer (WWDT)	Signal Measurement Timer (SMT)	CCP/10-bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Direct Memory Access (DMA) (channels)	Memory Access Partition	Vectored Interrupts	UART/UART with LIN, DMX, DALI Protocol Support	I^{2}C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug (1)
PIC18(L)F24K42	A	16	256	1024	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F25K42	A	32	256	2048	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F26K42	B	64	1024	4096	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F27K42	C	128	1024	8192	25	24	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F45K42	B	32	256	2048	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F46K42	B	64	1024	4096	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F47K42	C	128	1024	8192	36	35	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F55K42	B	32	1024	2048	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F56K42	B	64	1024	4096	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I
PIC18(L)F57K42	C	128	1024	8192	44	43	1	2	3/4	Y	Y	4/4	3	1	4	Y	2	Y	Y	1/1	2/1	Y	Y	I

Note 1: I – Debugging integrated on chip.

Data Sheet Index:

A: Future Release PIC18(L)F24/44K42 Data Sheet, 28-Pin

B: Future Release PIC18(L)F26/45/55/46/56K42 Data Sheet, 48-Pin

C: Future Release PIC18(L)F27/47/57K42 Data Sheet, 48-Pin

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

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TABLE 2: PACKAGES

Device	(S)PDIP	SOIC	SSOP	UQFN (4x4)	QFN (6x6)	TQFP	QFN (8x8)	UQFN (5x5)	UQFN (6x6)
PIC18(L)F24K42	X	X	X	X	X	—	—	—	—
PIC18(L)F25K42	X	X	X	X	X	—	—	—	—
PIC18(L)F26K42	X	X	X	X	—	—	—	—	—
PIC18(L)F27K42	X	X	X	—	X	—	—	—	—
PIC18(L)F45K42	X	—	—	—	—	X	X	X	—
PIC18(L)F46K42	X	—	—	—	—	X	X	X	—
PIC18(L)F47K42	X	—	—	—	—	X	X	X	—
PIC18(L)F55K42	X	—	—	—	—	X	X	—	X
PIC18(L)F56K42	X	—	—	—	—	X	X	—	X
PIC18(L)F57K42	X	—	—	—	—	X	X	—	X

Note: Pin details are subject to change.

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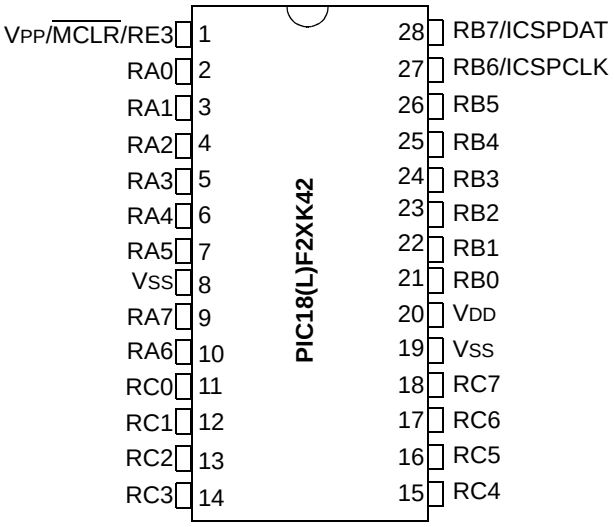
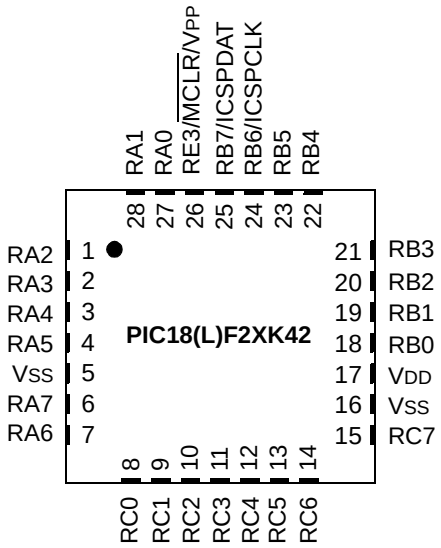
PIN DIAGRAMS

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP FOR PIC18(L)F2XK42



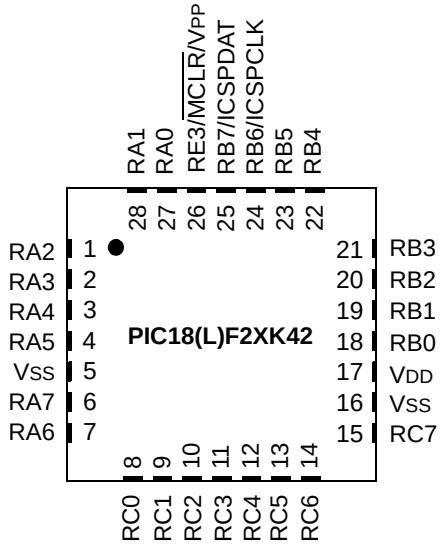
Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 28-PIN UQFN (4X4) FOR PIC18(L)F2XK42



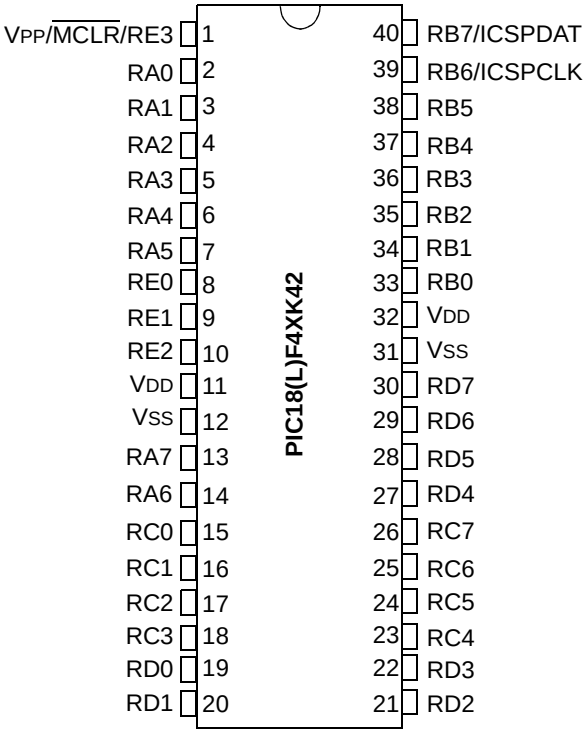
Note: See Table 3 or the pin allocation tables.

FIGURE 3: 28-PIN QFN (6X6X0.9 mm) FOR PIC18(L)F2XK42



Note: See Table 3 or the pin allocation tables.

FIGURE 4: 40-PIN PDIP FOR PIC18(L)F4XK42



Note: See Table 4 for location of all peripheral functions.

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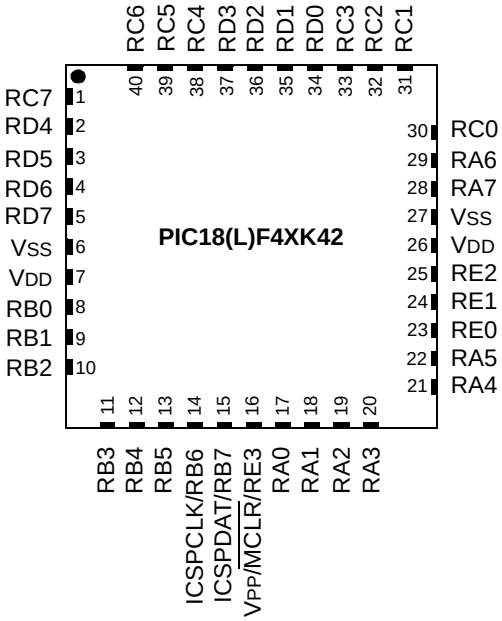
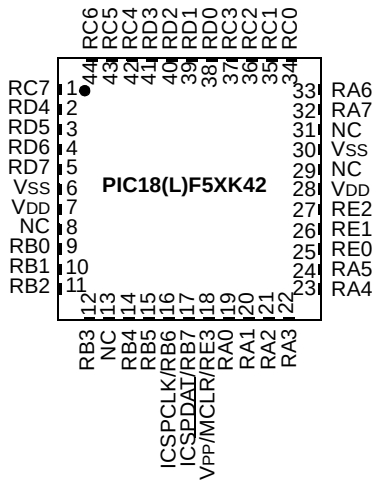
FIGURE 5: 40-PIN UQFN (5X5X0.5 mm) FOR PIC18(L)F4XK42



Note: See Table 4 for the pin allocation tables.

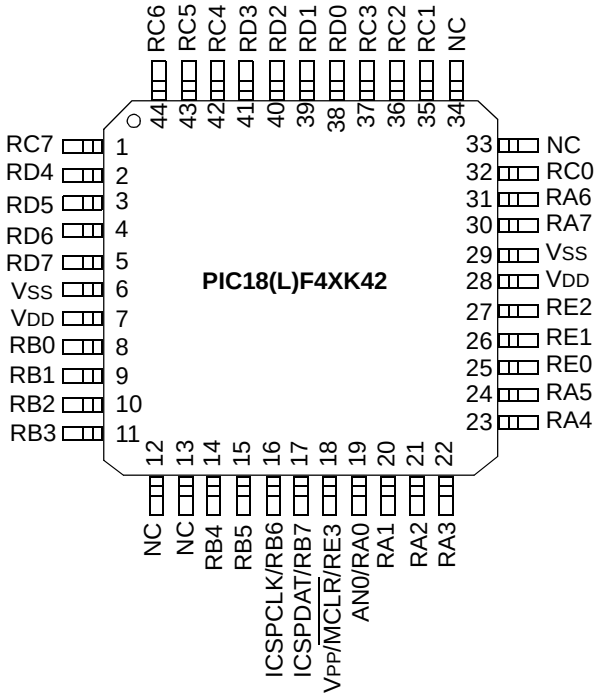
FIGURE 6: 44-PIN QFN (8X8X0.9 mm) FOR PIC18(L)F5XK42



Note 1: See Table 4 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to Vss, however it must not be the only Vss connection to the device.

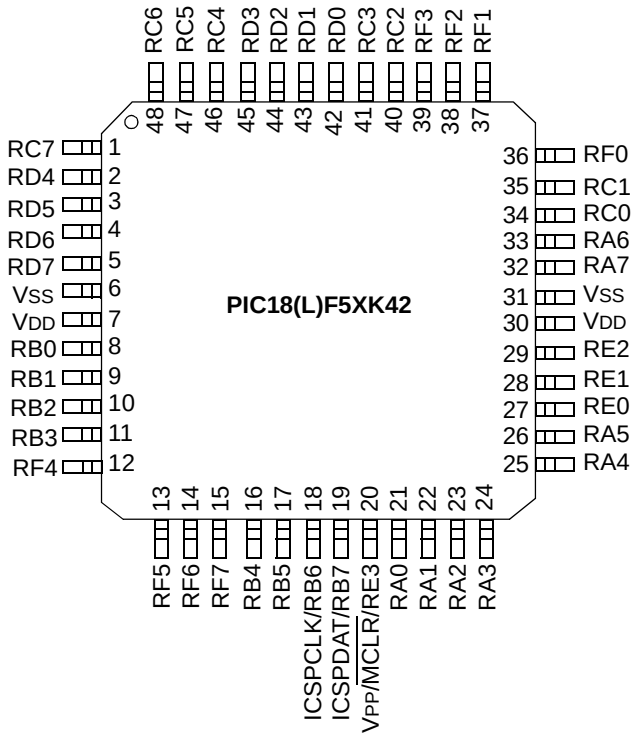
FIGURE 7: 44-PIN TQFP FOR PIC18(L)F4XK42



Note 1: See Table 4 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

FIGURE 8: 48-PIN TQFP/UQFN FOR PIC18(L)F5XK42



Note: See Table 5 for location of all peripheral functions.

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PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK42)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	27	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—
RA1	3	28	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—
RA2	4	1	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	2	ANA3	VREF+	—	C1IN1+	—	—	—	—	MDCARL(1)	—	—	—	—	—	—	IOCA3	—
RA4	6	3	ANA4	—	—	—	—	—	—	—	MDCARH(1)	T0CKI(1)	—	—	—	—	—	IOCA4	—
RA5	7	4	ANA5	—	—	—	—	—	SS1(1)	—	MDSRC(1)	—	—	—	—	—	—	IOCA5	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	21	18	ANB0	—	—	C2IN1+	ZCD	—	—	—	—	—	CCP4(1)	CWG1IN(1)	—	—	—	INT0(1) IOCB0	—
RB1	22	19	ANB1	—	—	C1IN3- C2IN3-	—	SCL2(3,4)	—	—	—	—	—	CWG2IN(1)	—	—	—	INT1(1) IOCB1	—
RB2	23	20	ANB2	—	—	—	—	SDA2(3,4)	—	—	—	—	—	CWG3IN(1)	—	—	—	INT2(1) IOCB2	—
RB3	24	21	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	25	22	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	T5G(1)	—	—	—	—	—	IOCB4	—
RB5	26	23	ANB5	—	—	—	—	—	—	—	—	T1G(1)	CCP3(1)	—	—	—	—	IOCB5	—
RB6	27	24	ANB6	—	—	—	—	—	—	CTS2(1)	—	—	—	—	CLCIN2(1)	—	—	IOCB6	ICSPCLK
RB7	28	25	ANB7	—	DAC1OUT2	—	—	—	—	RX2(1)	—	T6IN(1)	—	—	CLCIN3(1)	—	—	IOCB7	ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

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TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK42) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC0	11	8	ANC0	—	—	—	—	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMTWIN1(1)	—	—	—	—	—	IOCC0	SOSCO
RC1	12	9	ANC1	—	—	—	—	—	—	—	—	SMTSIG1(1)	CCP2(1)	—	—	—	—	IOCC1	SOSCI
RC2	13	10	ANC2	—	—	—	—	—	—	—	—	T5CKI(1)	CCP1(1)	—	—	—	—	IOCC2	—
RC3	14	11	ANC3	—	—	—	—	SCL1(3,4)	SCK1(1)	—	—	T2IN(1)	—	—	—	—	—	IOCC3	—
RC4	15	12	ANC4	—	—	—	—	SDA1(3,4)	SDI1(1)	—	—	—	—	—	—	—	—	IOCC4	—
RC5	16	13	ANC5	—	—	—	—	—	—	—	—	T4IN(1)	—	—	—	—	—	IOCC5	—
RC6	17	14	ANC6	—	—	—	—	—	—	CTS1(1)	—	—	—	—	—	—	—	IOCC6	—
RC7	18	15	ANC7	—	—	—	—	—	—	RX1(1)	—	—	—	—	—	—	—	IOCC7	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	$\overline{MCLR}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
V_{SS}	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDA1 SCL1 SDA2 SCL2	SS1 SCK1 SDO1	RTS1 TXDE1 TX1 RTS2 TXDE2 TX2	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 PWM5OUT PWM6OUT PWM7OUT PWM8OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

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TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42

I/O	40-Pin PDIP	44-Pin TQFP	40-Pin UQFN	44-Pin QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	19	17	19	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—
RA1	3	20	18	20	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—
RA2	4	21	19	21	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	22	20	22	ANA3	VREF+	—	C1IN1+	—	—	—	—	MDCARL(1)	—	—	—	—	—	—	IOCA3	—
RA4	6	23	21	23	ANA4	—	—	—	—	—	—	—	MDCARH(1)	T0CKI(1)	—	—	—	—	—	IOCA4	—
RA5	7	24	22	24	ANA5	—	—	—	—	—	SS1(1)	—	MDSRC(1)	—	—	—	—	—	—	IOCA5	—
RA6	14	31	29	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	13	30	28	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	33	8	8	9	ANB0	—	—	C2IN1+	ZCD	—	—	—	—	—	CCP4(1)	CWG1IN(1)	—	—	—	INT0(1) IOCB0	—
RB1	34	9	9	10	ANB1	—	—	C1IN3- C2IN3-	—	SCL2(3,4)	—	—	—	—	—	CWG2IN(1)	—	—	—	INT1(1) IOCB1	—
RB2	35	10	10	11	ANB2	—	—	—	—	SDA2(3,4)	—	—	—	—	—	CWG3IN(1)	—	—	—	INT2(1) IOCB2	—
RB3	36	11	11	12	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	37	14	12	14	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	T5G(1)	—	—	—	—	—	IOCB4	—
RB5	38	15	13	15	ANB5	—	—	—	—	—	—	—	—	T1G(1)	CCP3(1)	—	—	—	—	IOCB5	—
RB6	39	16	14	16	ANB6	—	—	—	—	—	—	CTS2(1)	—	-	—	—	CLCIN2(1)	—	—	IOCB6	ICSPCLK
RB7	40	17	15	17	ANB7	—	DAC1OUT2	—	—	—	—	RX2(1)	—	T6IN(1)	—	—	CLCIN3(1)	—	—	IOCB7	ICSPDAT
RC0	15	32	30	34	ANC0	—	—	—	—	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMTWIN1(1)	—	—	—	—	—	IOCC0	SOSCO
RC1	16	35	31	35	ANC1	—	—	—	—	—	—	—	—	SMTSIG1(1)	CCP2(1)	—	—	—	—	IOCC1	SOSCI

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

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TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42 (CONTINUED)

I/O	40-Pin PDIP	44-Pin TQFP	40-Pin UQFN	44-Pin QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC2	17	36	32	36	ANC2	—	—	—	—	—	—	—	—	T5CKI(1)	CCP1(1)	—	—	—	—	IOCC2	—
RC3	18	37	33	37	ANC3	—	—	—	—	SCL1(3,4)	SCK1(1)	—	—	T2IN(1)	—	—	—	—	—	IOCC3	—
RC4	23	42	38	42	ANC4	—	—	—	—	SDA1(3,4)	SDI1(1)	—	—	—	—	—	—	—	—	IOCC4	—
RC5	24	43	39	43	ANC5	—	—	—	—	—	—	—	—	T4IN(1)	—	—	—	—	—	IOCC5	—
RC6	25	44	40	44	ANC6	—	—	—	—	—	—	CTS1(1)	—	—	—	—	—	—	—	IOCC6	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	RX1(1)	—	—	—	—	—	—	—	IOCC7	—
RD0	19	38	34	38	AND0	—	—	—	—	—(4)	—	—	—	—	—	—	—	—	—	—	—
RD1	20	39	35	39	AND1	—	—	—	—	—(4)	—	—	—	—	—	—	—	—	—	—	—
RD2	21	40	36	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	22	41	37	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE0	8	25	23	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE1	9	26	24	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE2	10	27	25	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE3	1	18	16	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	$\overline{MCLR}$ V_{PP}
V_{DD}	11, 32	7, 28	7, 26	8, 28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
V_{SS}	12, 31	6, 29	6, 27	6, 31, 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

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TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42 (CONTINUED)

I/O	40-Pin PDIP	44-Pin TQFP	40-Pin UQFN	44-Pin QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
OUT(2)	—	—	—	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDA1 SCL1 SDA2 SCL2	SS1 SCK1 SDO1	RTS1 TXDE1 TX1 RTS2 TXDE2 TX2	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 PWM5OUT PWM6OUT PWM7OUT PWM8OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

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TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42

I/O	48-Pin TQFP	48-Pin UQFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	21	21	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—
RA1	22	22	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—
RA2	23	23	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	24	24	ANA3	VREF+	—	C1IN1+	—	—	—	—	MDCARL(1)	-	—	—	—	—	—	IOCA3	—
RA4	25	25	ANA4	—	—	—	—	—	—	—	MDCARH(1)	T0CKI(1)	—	—	—	—	—	IOCA4	—
RA5	26	26	ANA5	—	—	—	—	—	SS1(1)	—	MDSRC(1)	—	—	—	—	—	—	IOCA5	—
RA6	33	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	32	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	8	8	ANB0	—	—	C2IN1+	ZCD	—	—	—	—	—	CCP4(1)	CWG1IN(1)	—	—	—	INT0(1) IOCB0	—
RB1	9	9	ANB1	—	—	C1IN3- C2IN3-	—	SCL2(3,4)	—	—	—	—	—	CWG2IN(1)	—	—	—	INT1(1) IOCB1	—
RB2	10	10	ANB2	—	—	—	—	SDA2(3,4)	—	—	—	—	—	CWG3IN(1)	—	—	—	INT2(1) IOCB2	—
RB3	11	11	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	16	16	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	T5G(1)	—	—	—	—	—	IOCB4	—
RB5	17	17	ANB5	—	—	—	—	—	—	—	—	T1G(1)	CCP3(1)	-	—	—	—	IOCB5	—
RB6	18	18	ANB6	—	—	—	—	—	—	CTS2(1)	—	—	—	—	CLCIN2(1)	—	—	IOCB6	ICSPCLK
RB7	19	19	ANB7	—	DAC1OUT2	—	—	—	—	RX2(1)	—	T6IN(1)	—	—	CLCIN3(1)	—	—	IOCB7	ICSPDAT
RC0	34	34	ANC0	—	—	—	—	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMTWIN1(1)	—	—	—	—	—	IOCC0	SOSCO
RC1	35	35	ANC1	—	-	—	—	—	—	—	—	SMTSIG1(1)	CCP2(1)	—	—	—	—	IOCC1	SOSCI

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

Advance Information

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TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42 (CONTINUED)

I/O	48-Pin TQFP	48-Pin UQFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC2	40	40	ANC2	—	-	—	—	—	—	—	—	T5CKI(1)	CCP1(1)	—	—	—	—	IOCC2	—
RC3	41	41	ANC3	—	-	—	—	SCL1(3,4)	SCK1(1)	—	—	T2IN(1)	-	—	—	—	—	IOCC3	—
RC4	46	46	ANC4	—	—	—	—	SDA1(3,4)	SDI1(1)	—	—	—	—	—	—	—	—	IOCC4	—
RC5	47	47	ANC5	—	—	—	—	—	—	—	—	T4IN(1)	—	—	—	—	—	IOCC5	—
RC6	48	48	ANC6	—	—	—	—	—	—	CTS1(1)	—	—	—	—	—	—	—	IOCC6	—
RC7	1	1	ANC7	—	—	—	—	—	—	RX1(1)	—	—	—	—	—	—	—	IOCC7	—
RD0	42	42	AND0	—	—	—	—	—(4)	—	—	—	—	—	—	—	—	—	—	—
RD1	43	43	AND1	—	—	—	—	—(4)	—	—	—	—	—	—	—	—	—	—	—
RD2	44	44	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	45	45	AND3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD4	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD5	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD6	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD7	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE0	27	27	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE1	28	28	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE2	29	29	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE3	20	20	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	$\overline{MCLR}$ V_{PP}
RF0	36	36	ANF0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF1	37	37	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF2	38	38	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF3	39	39	ANF3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF4	12	12	ANF4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF5	13	13	ANF5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF6	14	14	ANF6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF7	15	15	ANF7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
V_{DD}	7, 30	7, 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

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TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42 (CONTINUED)

I/O	48-Pin TQFP	48-Pin UQFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	I^2C	SPI	UART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
VSS	6, 31	6, 31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDA1 SCL1 SDA2 SCL2	SS1 SCK1 SDO1	RTS1 TXDE1 TX1 RTS2 TXDE2 TX2	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 PWM5OUT PWM6OUT PWM7OUT PWM8OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All output signals shown in this row are PPS remappable.
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