

E Series Power MOSFET


RoHS
COMPLIANT

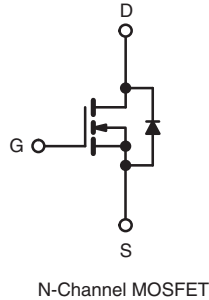
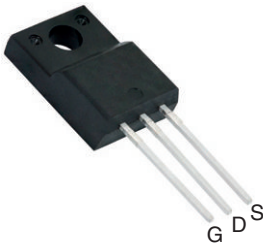
PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.145
Q_g (Max.) (nC)	86	
Q_{gs} (nC)	14	
Q_{gd} (nC)	25	
Configuration	Single	

FEATURES

- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting

Thin-Lead TO-220 FULLPAK



ORDERING INFORMATION	
Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free	SiHA25N50E-E3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		500	V
Gate-Source Voltage	V_{GS}		± 30	
Continuous Drain Current ($T_J = 150$ °C) ^e	V_{GS} at 10 V	$T_C = 25$ °C	26	A
		$T_C = 100$ °C	16	
Pulsed Drain Current ^a	I_{DM}		50	
Linear Derating Factor			0.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}		273	mJ
Maximum Power Dissipation	P_D		35	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}		-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % V_{DS}		65	V/ns
Reverse Diode dV/dt ^d			25	
Soldering Recommendations (Peak Temperature) ^c	for 10 s		300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.4$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.
- Limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.59	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	25	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	-	0.125	0.145	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 12\text{ A}$	-	6.6	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$ $V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	1980	-	pF
Output Capacitance	C_{oss}		-	105	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$		-	105	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	285	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}, V_{DS} = 400\text{ V}$	-	57	86	nC
Gate-Source Charge	Q_{gs}		-	14	-	
Gate-Drain Charge	Q_{gd}		-	25	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 12\text{ A}$ $R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$	-	19	38	ns
Rise Time	t_r		-	36	72	
Turn-Off Delay Time	$t_{d(off)}$		-	57	86	
Fall Time	t_f		-	29	58	
Gate Input Resistance	R_g		$f = 1\text{ MHz}, \text{open drain}$	-	0.56	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	12	A
Pulsed Diode Forward Current	I_{SM}		-	-	50	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 16.5\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S,$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$	-	338	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.3	-	μC
Reverse Recovery Current	I_{RRM}		-	29	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

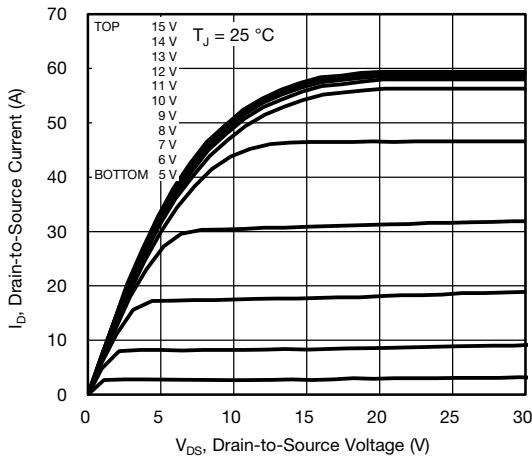


Fig. 1 - Typical Output Characteristics

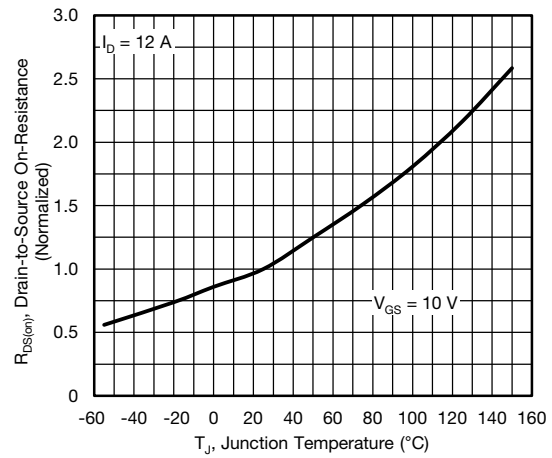


Fig. 4 - Normalized On-Resistance vs. Temperature

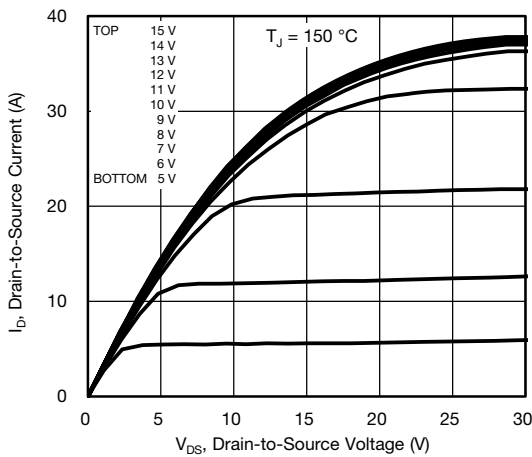


Fig. 2 - Typical Output Characteristics

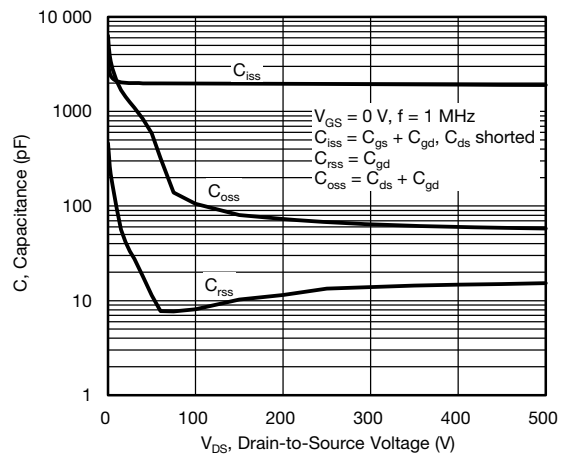


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

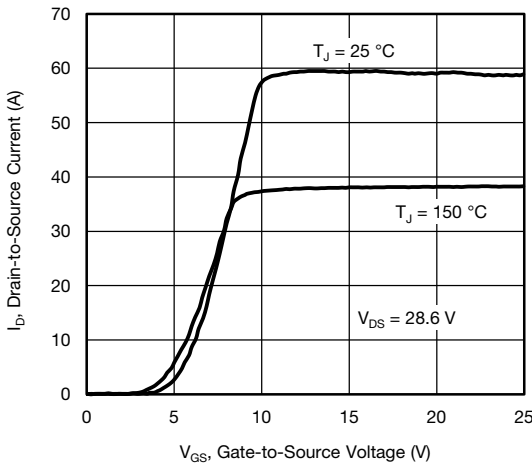


Fig. 3 - Typical Transfer Characteristics

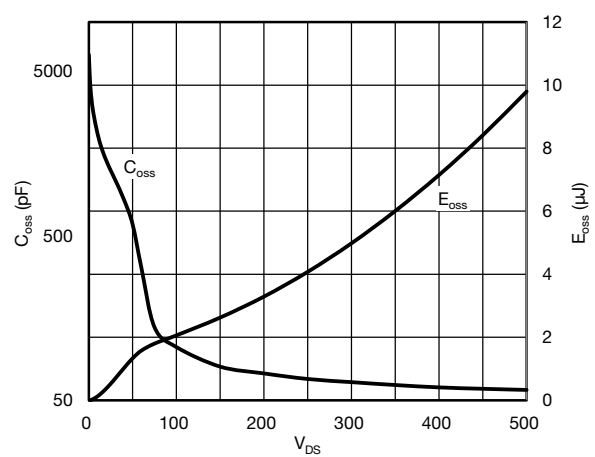


Fig. 6 - Coss and Eoss vs. VDS

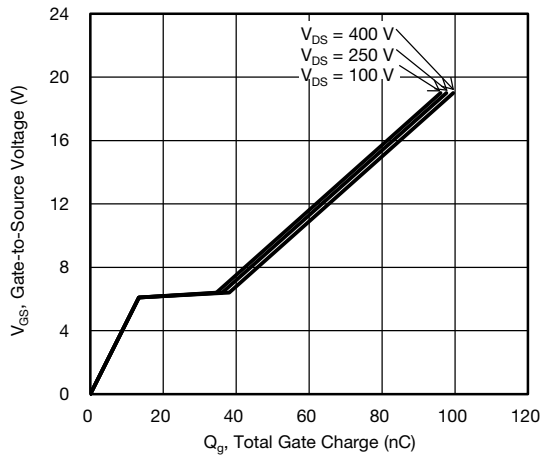


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

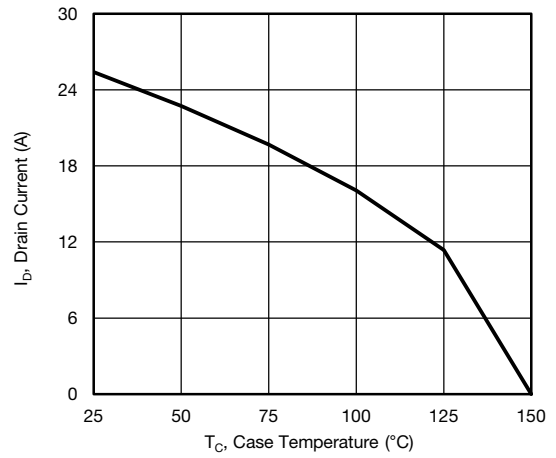


Fig. 10 - Maximum Drain Current vs. Case Temperature

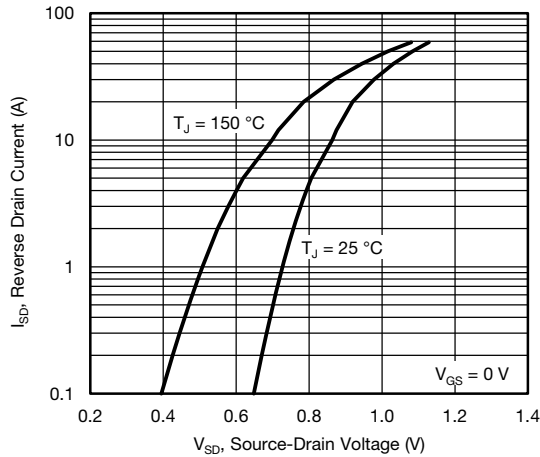


Fig. 8 - Typical Source-Drain Diode Forward Voltage

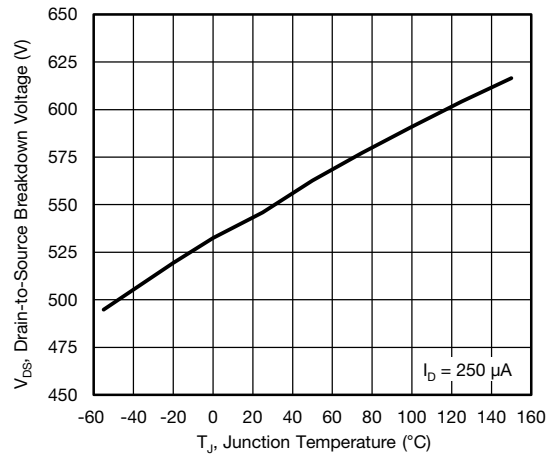


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

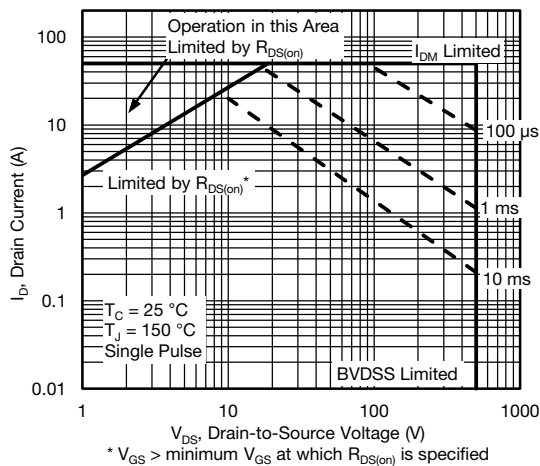


Fig. 9 - Maximum Safe Operating Area

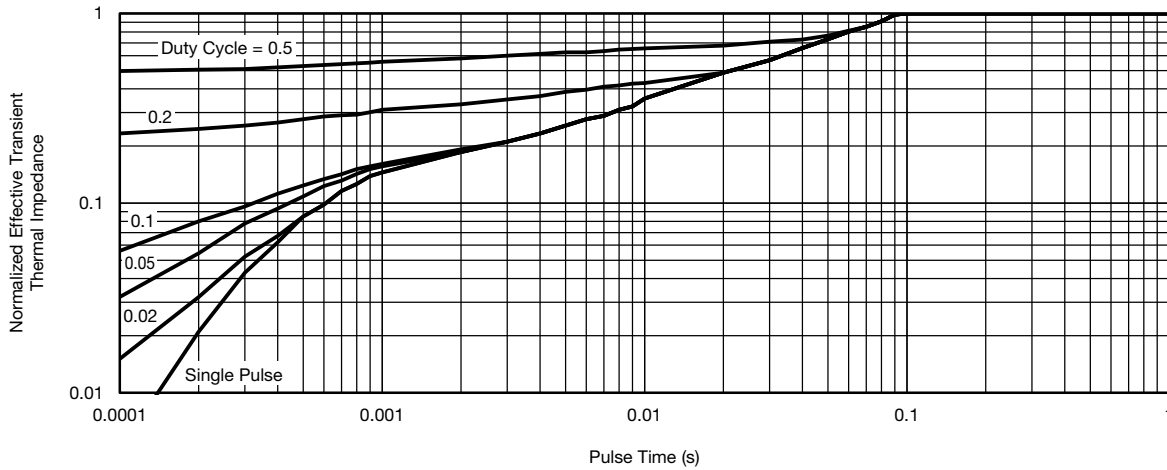


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

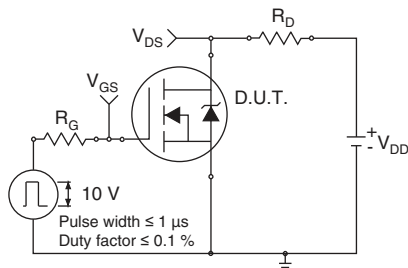


Fig. 13 - Switching Time Test Circuit

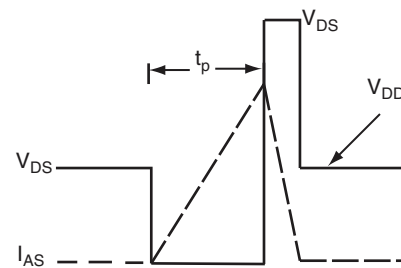


Fig. 16 - Unclamped Inductive Waveforms

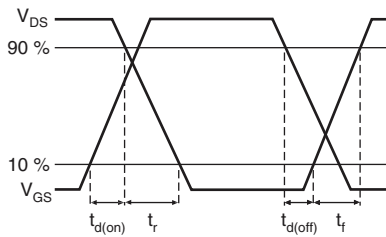


Fig. 14 - Switching Time Waveforms

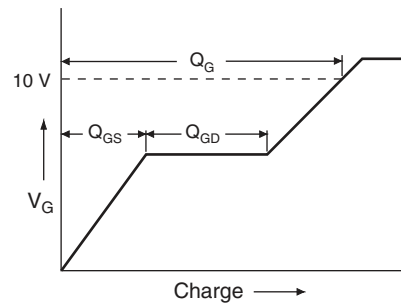


Fig. 17 - Basic Gate Charge Waveform

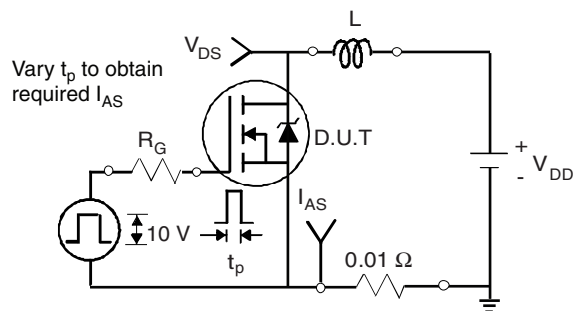


Fig. 15 - Unclamped Inductive Test Circuit

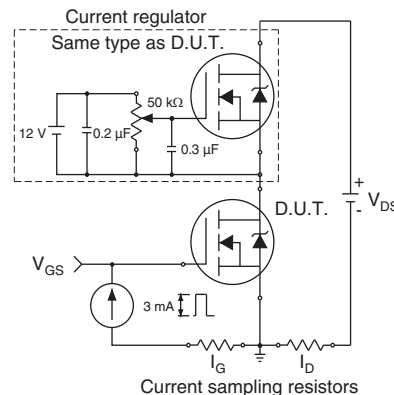
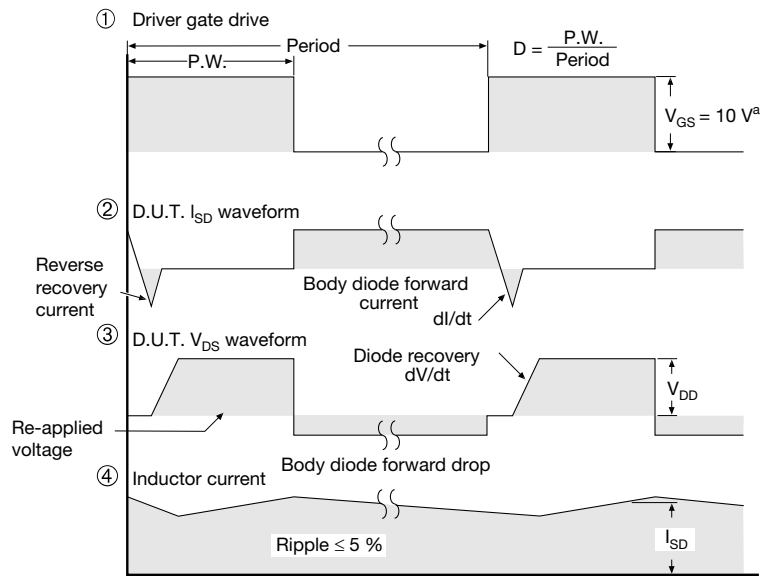


Fig. 18 - Gate Charge Test Circuit



Note

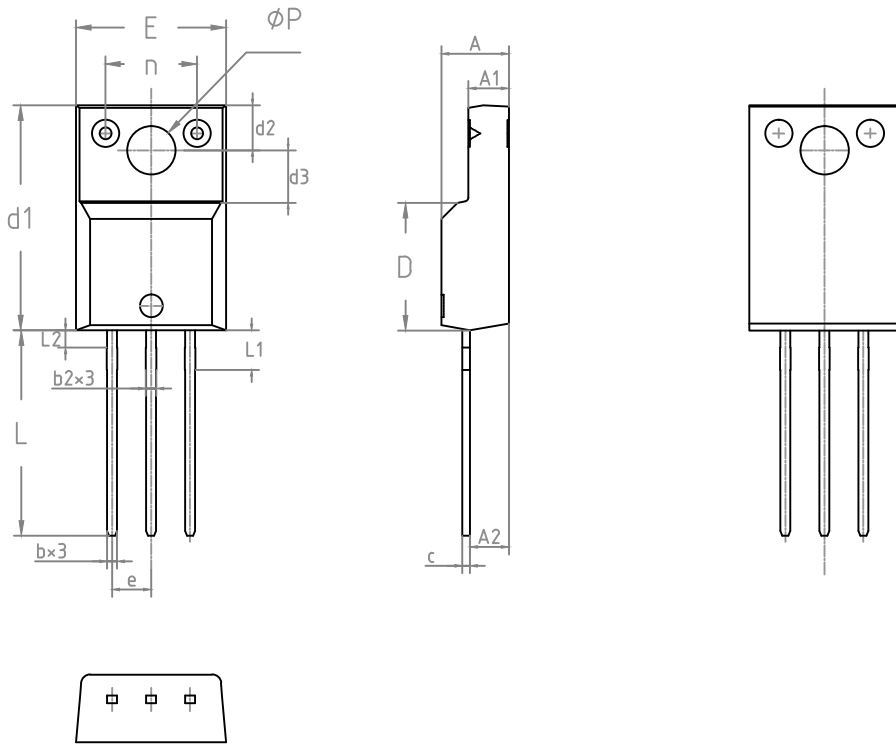
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.50	2.70	0.098	0.106
b	0.60	0.80	0.024	0.031
b2	0.60	0.80	0.024	0.031
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.40	3.60	0.134	0.142
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	2.50	2.80	0.098	0.110
L2	-	1.20	-	0.047
n	6.05	6.15	0.238	0.242

ECN: X13-0219-Rev. A, 23-Dec-13
 DWG: 6021



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