

Constant Current LED Drivers

50V 200mA

1ch Source Driver for Automotive

BD8372HFP-M BD8372EFJ-M

General Description

BD8372HFP-M and BD8372EFJ-M are LED source drivers capable of withstanding high input voltage (50V MAX). The constant current output is set by either of two external resistors. It has built-in LED open/short protection, external resistance open/short protection and overvoltage protection that can achieve high reliability. It is possible to control all LEDs together and turn OFF even if LED causes short/open in a certain row when driving two or more LEDs by using multiple ICs.

Key Specifications

- Input Voltage Range: 5.5V to 40V
- Max Output Current: 200mA(MAX)
- Output Current Accuracy: ±8%(Max)
- Operating Temperature Range: -40°C to +125°C

Packages

HRP7
HTSOP-J8

W (Typ) x D (Typ) x H (Max)
9.395mm x 10.540mm x 2.005mm
4.90mm x 6.00mm x 1.00mm

Features

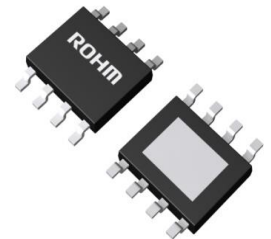
- Variable form Constant- Current Source
- H/L Current Setting Switch Control
- LED Open/Short Protection Circuit Integrated
- ISET Open/Short Protection Circuit Integrated
- Overvoltage Mute and Temperature Protection Function Integrated
- Abnormal Output Detection and Output Functions (PBUS)

Applications

For automotive (Rear lamp, Interior light, etc.).



HRP7



HTSOP-J8

Basic Application Circuit

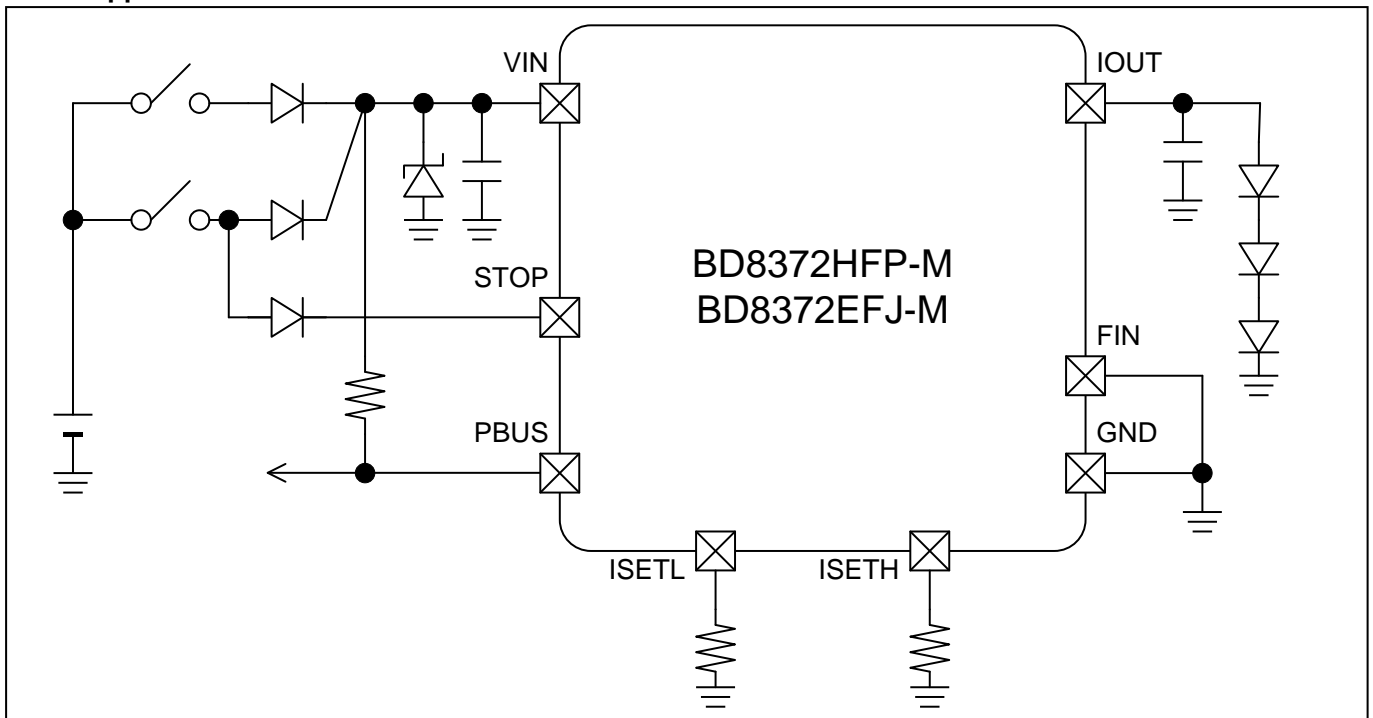


Figure 1. Typical Application Circuit

Pin Configurations

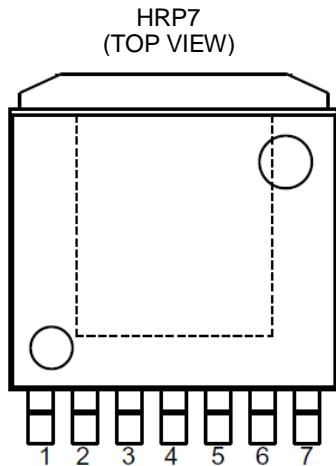


Figure 2. HRP7 Package Pin Configuration

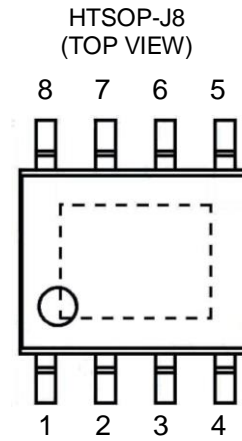


Figure 3. HTSOP-J8 Package Pin Configuration

Pin Descriptions

HRP7

Pin No.	Pin Name	Description
1	STOP	Input terminal for Brake lamp
2	PBUS	Error detection I/O terminal
3	ISETL	Current setting terminal (L mode)
4	GND	GND
5	ISETH	Current setting terminal (H mode)
6	VIN	Power supply input
7	IOUT	Current output terminal

HTSOP-J8

Pin No.	Pin Name	Description
1	VIN	Power supply input
2	IOUT	Current output terminal
3	GND	GND
4	GND	GND
5	STOP	Input terminal for Brake lamp
6	PBUS	Error detection I/O terminal
7	ISETL	Current setting terminal (L mode)
8	ISETH	Current setting terminal (H mode)

Block Diagram

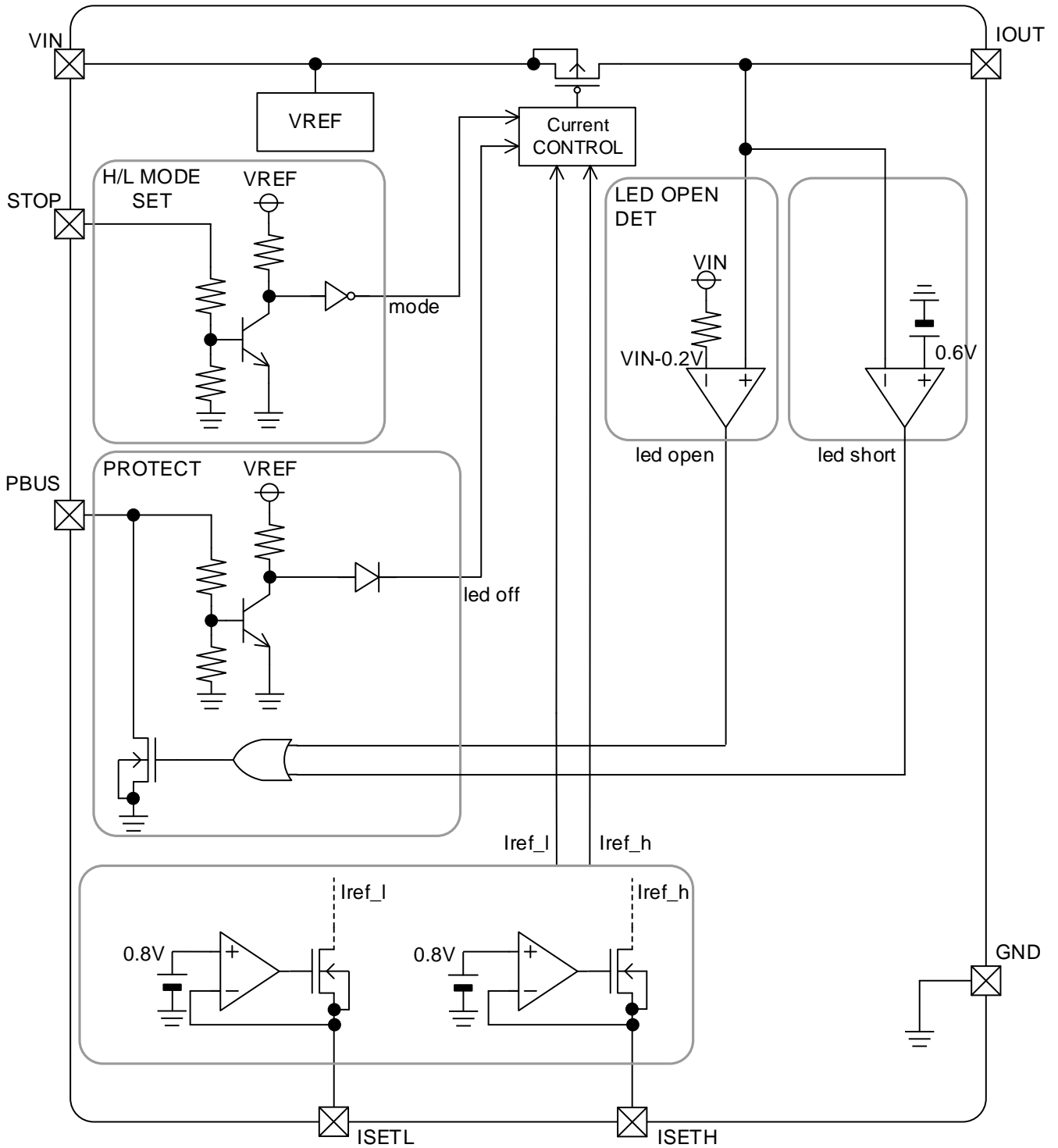


Figure 4. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	
Power Supply Voltage	V _{IN}	-0.3 to +50	V	
STOP, IOOUT, PBUS Terminal	V _{STOP} , V _{IOOUT} , V _{PBUS}	-0.3 to V _{IN} +0.3	V	
ISETH, ISETL Terminal	V _{ISETH} , V _{ISETL}	-0.3 to +7	V	
Power Consumption	Pd	HRP7	2.3 (Note 1)	W
		HTSOP-J8	1.1 (Note 2)	
Operating Temperature Range	Topr	-40 to +125	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature	Tjmax	150	°C	
IOOUT Output Maximum Current	I _{IOOUT}	200	mA	

(Note 1) HRP7

IC mounted on glass epoxy 2-layer board area 15mmx15mm of the back copper foil, measuring 70mmx70mmx1.6mm.
Pd decreased at 18.4mW/°C for temperatures above Ta=25°C.

(Note 2) HTSOP-J8

IC mounted on glass epoxy 2-layer board area 15mmx15mm of the back copper foil, measuring 70mmx70mmx1.6mm.
Pd decreased at 8.8mW/°C for temperatures above Ta=25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +125°C)

(Please set after considering power consumption for the power-supply voltage.)

Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Power Supply Voltage	V _{IN}	5.5	13	40	V	-
Current Setting Resistor	R _{ISETH}	10	-	100	kΩ	STOP=H
	R _{ISETL}	10	-	100	kΩ	STOP=L
Minimum Capacitor connecting IOOUT terminal	C _{IOOUT}	0.1	-	-	μF	

Electrical Characteristics

(Unless otherwise specified, Ta=-40°C to 125°C, V_{IN}=13V, R_{ISETL}=R_{ISETH}=40kΩ, R_{PBUS}=10kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I _{VIN}	-	2.9	5	mA	
IOUT Output Current H	I _{OUT_H}	48.5	50	51.5	mA	50mA setting (I _{SET} =40kΩ) STOP=High, Ta=25°C
		46	50	54	mA	50mA setting (I _{SET} =40kΩ) STOP=High, Ta=-40°C to +125°C
IOUT Output Current L	I _{OUT_L}	4.85	5	5.15	mA	5mA setting (I _{SET} =40kΩ) STOP=Low, Ta=25°C
		4.6	5	5.4	mA	5mA setting (I _{SET} =40kΩ) STOP=Low, Ta=-40°C to +125°C
IOUT Drop Voltage H	V _{DRH_IOUT}	-	0.7	1.2	V	200mA setting(I _{SET} =10kΩ) STOP=High
IOUT Drop Voltage L	V _{DRL_IOUT}	-	0.5	0.7	V	20mA setting(I _{SET} =10kΩ) STOP=Low
IOUT OFF Current	I _{IOUT_OFF}	-	-	1	μA	V _{IOUT} =2V, P _{BUS} =L, Ta=25°C
IOUT Current at GND Short	I _{IOUT_SHORT}	-	-	40	μA	V _{IOUT} =0V
ISET Terminal Voltage	V _{ISET}	-	0.8	-	V	At ISETL or ISETH pins
ISET Short Detection Resistor	R _{ISET_SHORT}	-	5.1k	7.5k	Ω	At ISETL or ISETH pins
ISET Open Detection Resistor	R _{ISET_OPEN}	125k	400k	-	Ω	At ISETL or ISETH pins
IOUT LED OPEN Detection	V _{IOUT_OPEN}	V _{IN} -0.3	V _{IN} -0.2	V _{IN} -0.1	V	
IOUT LED Short Detection	V _{IOUT_SHORT}	0.2	0.6	1.0	V	
STOP Input Voltage H	V _{IH_STOP}	4.0	-	V _{IN} +0.2	V	
STOP Input Voltage L	V _{IL_STOP}	GND	-	1.0	V	
STOP Input Current	I _{IN_STOP}	-	40	100	μA	V _{STOP} =13V
PBUS Input Voltage H	V _{IH_PBUS}	4.0	-	V _{IN} +0.2	V	
PBUS Input Voltage L	V _{IL_PBUS}	GND	-	2.0	V	
PBUS Low Voltage	V _{OL_PBUS}	-	-	1.5	V	I _{PBUS} =20mA
PBUS Input Current	I _{IN_PBUS}	-	38	100	μA	V _{PBUS} =13V
IN Under Voltage Open Detection Mask Voltage	V _{UVLO_IOPEN}	7.5	8.0	8.5	V	
Over Voltage Mute Voltage	V _{IN_OVPMUTE}	16	19	24	V	200mA setting (I _{SET} =10kΩ) STOP=High

Typical Performance Curves (Reference Data)

(Unless otherwise specified $T_a=25^\circ\text{C}$, $V_{IN}=13\text{V}$)

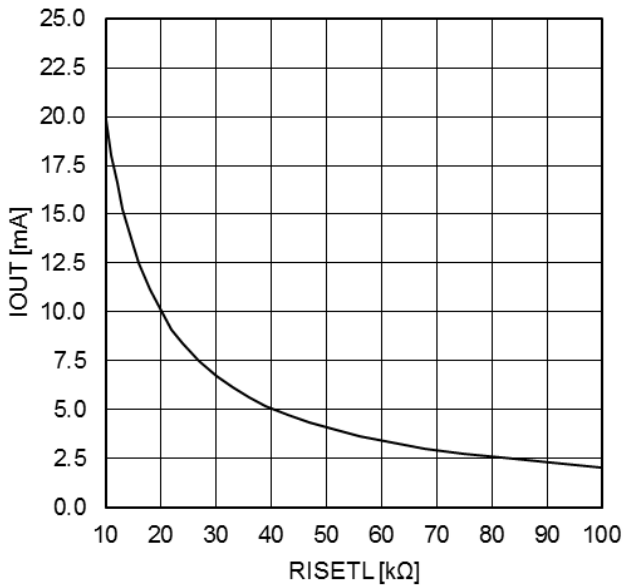


Figure 5. I_{OUT} vs R_{ISETL} (STOP=Low)

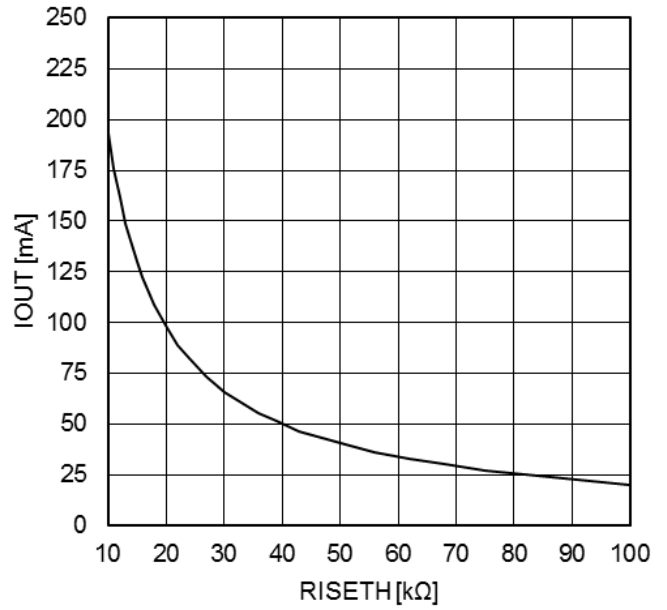


Figure 6. I_{OUT} vs R_{ISETH} (STOP=High)

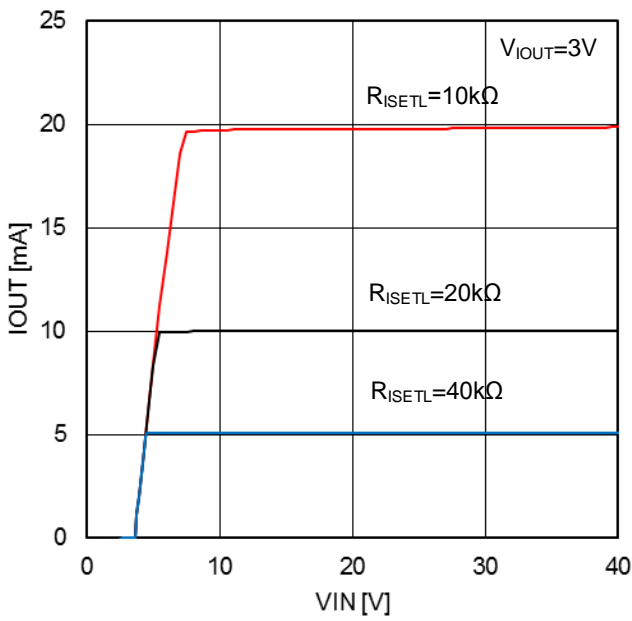


Figure 7. I_{OUT} vs V_{IN} (STOP=Low)

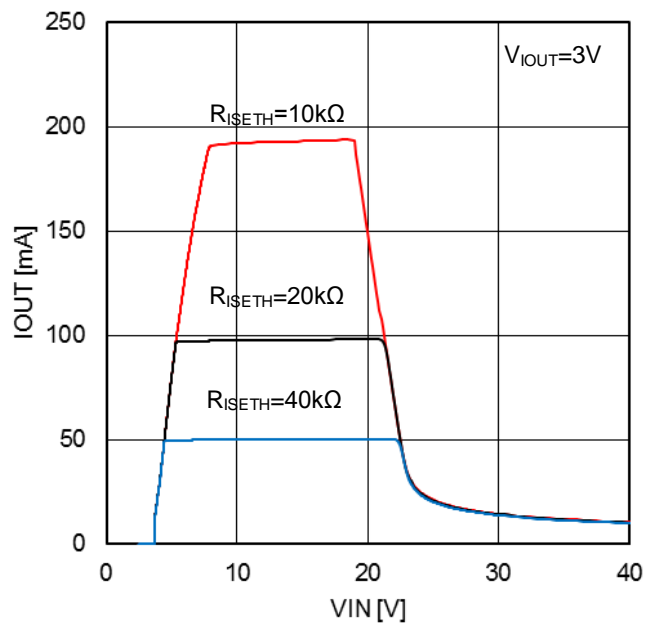


Figure 8. I_{OUT} vs V_{IN} (STOP=High)

Typical Performance Curves (Reference Data) - continued

(Unless otherwise specified $T_a=25^{\circ}\text{C}$, $V_{IN}=13\text{V}$)

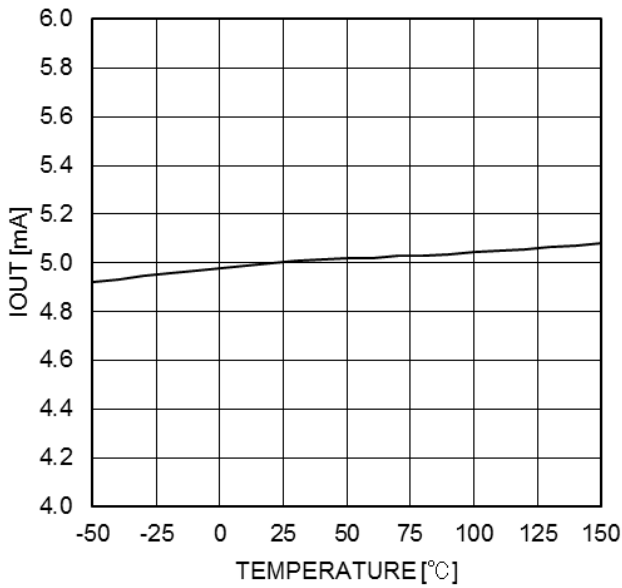


Figure 9. I_{OUT} vs T_a (STOP=Low)

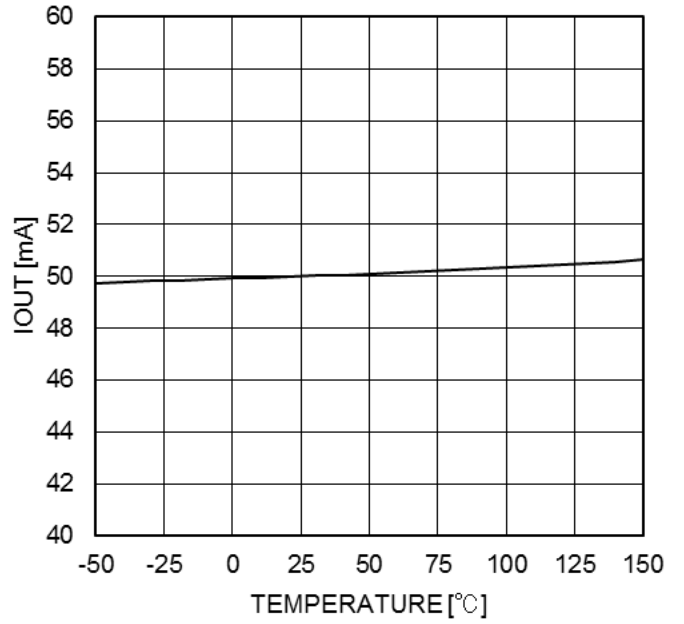


Figure 10. I_{OUT} vs T_a (STOP=High)

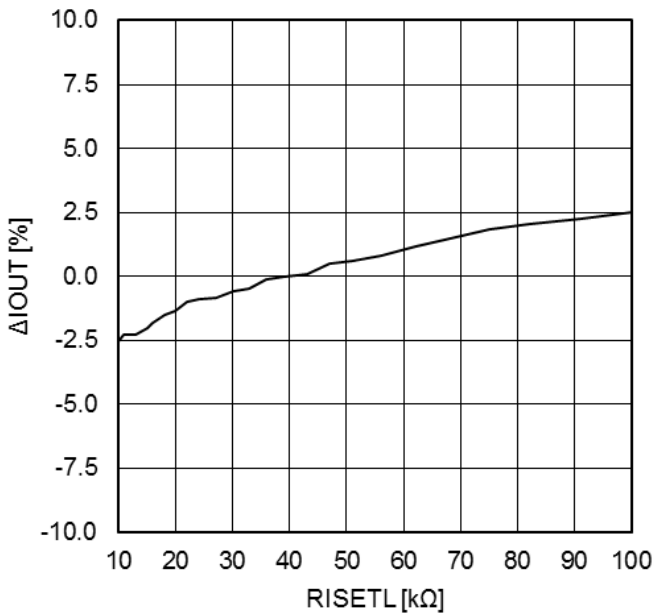


Figure 11. ΔI_{OUT} vs R_{ISETL} (STOP=Low)

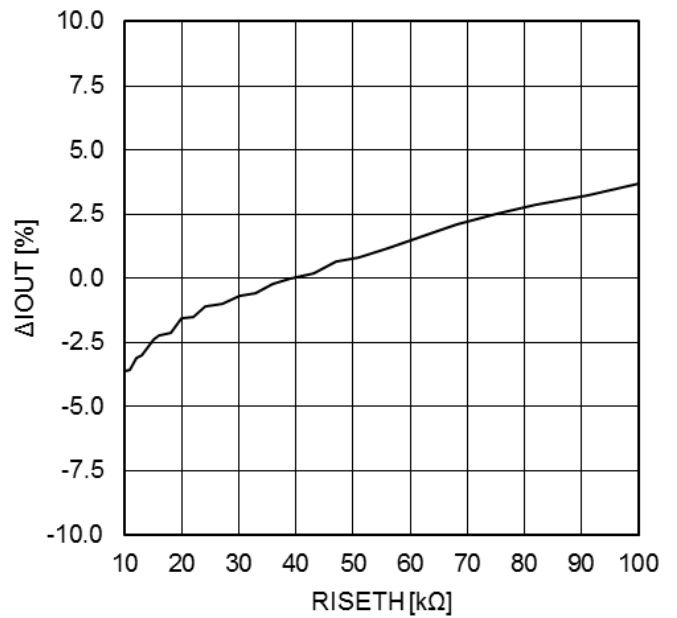


Figure 12. ΔI_{OUT} vs R_{ISETH} (STOP=High)

Timing Chart

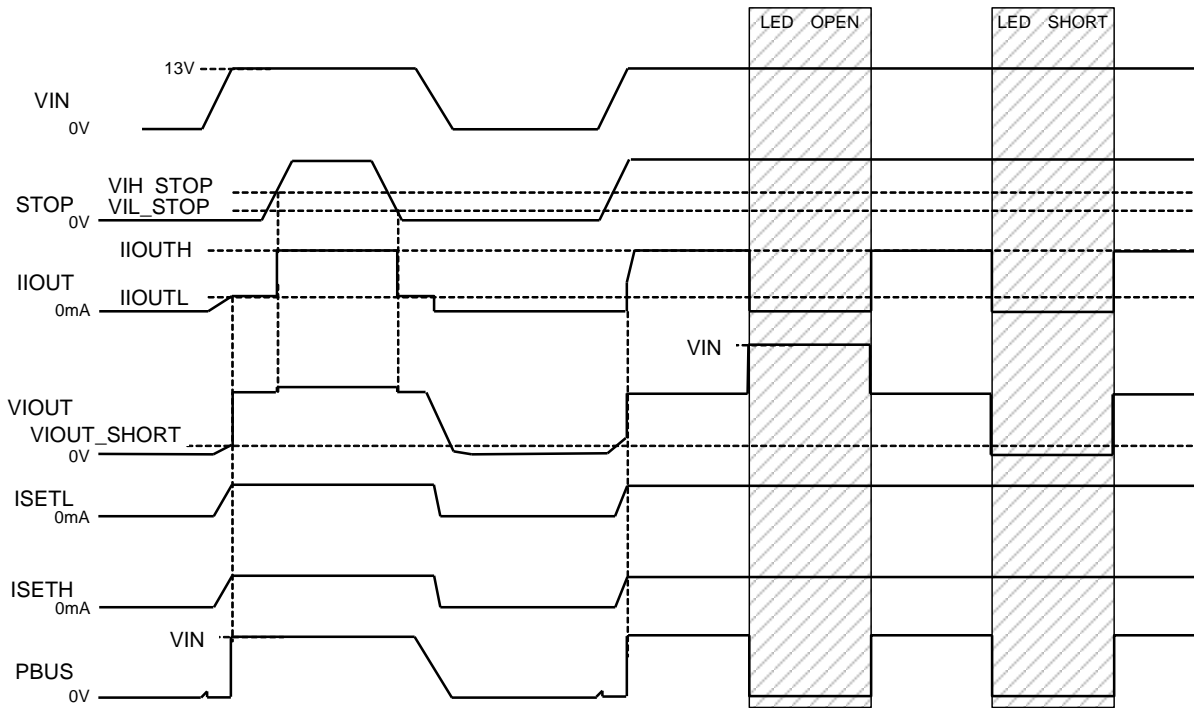
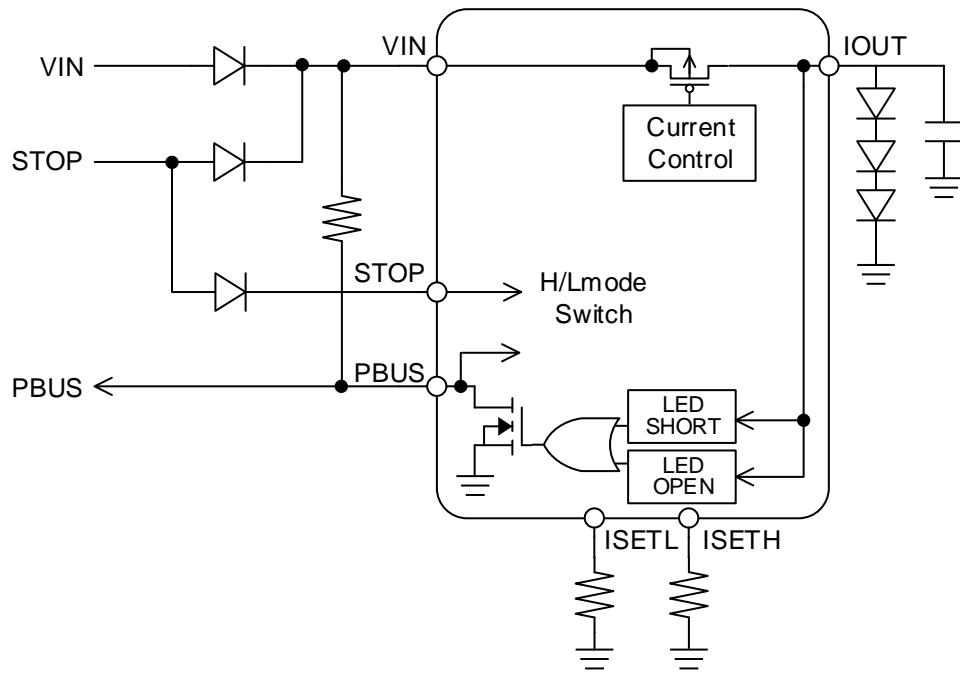


Figure 13. Timing Chart

Function Description

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{\text{IN}}=13\text{V}$, $R_{\text{ISETL}}=R_{\text{ISETH}}=40\text{k}\Omega$, the numerical value in the table are TYP values.)

1. Table for Operation

STOP	V_{IOUT}	R_{ISETL}	R_{ISETH}	MODE	I_{OUT}	PBUS
L	$2\text{V} < V_{\text{IOUT}} < V_{\text{IN}} - 0.7\text{V}(\text{Max})$	$10\text{k}\Omega \leq R_{\text{ISETL}} \leq 100\text{k}\Omega$	-	L mode normal operation	2mA to 20mA	Hi-Z
H	$2\text{V} < V_{\text{IOUT}} < V_{\text{IN}} - 1.2\text{V}(\text{Max})$	-	$10\text{k}\Omega \leq R_{\text{ISETH}} \leq 100\text{k}\Omega$	H mode normal operation	20mA to 200mA	Hi-Z
L/H	$V_{\text{IOUT}} \leq 0.6\text{V}(\text{Typ})$	-	-	Output short	40 $\mu\text{A}(\text{Max})$	LOW output
L/H	$V_{\text{IOUT}} \geq V_{\text{IN}} - 0.2\text{V}(\text{Typ})$	-	-	Output open	1 $\mu\text{A}(\text{Max})$	LOW output
L	-	$R_{\text{ISETL}} < 7.5\text{k}\Omega(\text{Max})$	-	I_{SETL} short	1 $\mu\text{A}(\text{Max})$	LOW output
L	-	$R_{\text{ISETL}} > 125\text{k}\Omega(\text{Min})$	-	I_{SETL} open	1 $\mu\text{A}(\text{Max})$	LOW output
H	-	-	$R_{\text{ISETH}} < 7.5\text{k}\Omega(\text{Max})$	I_{SETH} short	1 $\mu\text{A}(\text{Max})$	LOW output
H	-	-	$R_{\text{ISETH}} > 125\text{k}\Omega(\text{Min})$	I_{SETH} open	1 $\mu\text{A}(\text{Max})$	LOW output
L	$2\text{V} < V_{\text{IOUT}} < V_{\text{IN}} - 0.7\text{V}(\text{Max})$	$10\text{k}\Omega \leq R_{\text{ISETL}} \leq 100\text{k}\Omega$	-	PBUS control OFF	1 $\mu\text{A}(\text{Max})$	LOW input
H	$2\text{V} < V_{\text{IOUT}} < V_{\text{IN}} - 1.2\text{V}(\text{Max})$	-	$10\text{k}\Omega \leq R_{\text{ISETH}} \leq 100\text{k}\Omega$	PBUS control OFF	1 $\mu\text{A}(\text{Max})$	LOW input

Protection Mode Operation Voltage(The numerical value are typical)

V_{IN}	LED open	LED short	ISET open	ISET short	PBUS	Oversvoltage protection
$5.5\text{V} < V_{\text{IN}} \leq 8\text{V}$	x	o	o	o	o	x
$8\text{V} \leq V_{\text{IN}} \leq 19\text{V}$	o	o	o	o	o	x
$19\text{V} \leq V_{\text{IN}}$	o	o	o	o	o	o

o : Protection mode ON

x : Protection mode OFF

The LED open function is masked with $V_{\text{IN}} \leq 8\text{V}$.

2. Method of Setting Current

The IC regulates the voltage at ISETL/ISETH to V_{ISET} (0.8V typ) across the external resistor to set I_{OUT} . Then I_{OUT} is set by setting STOP High or Low.

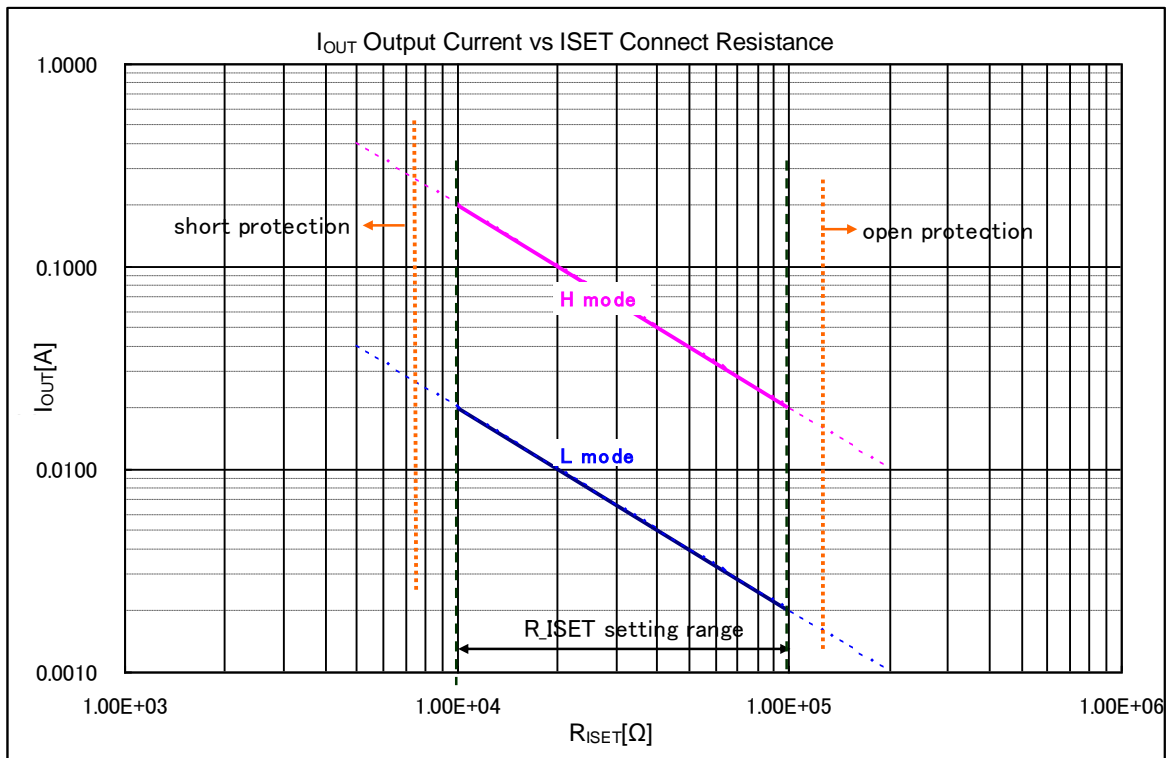
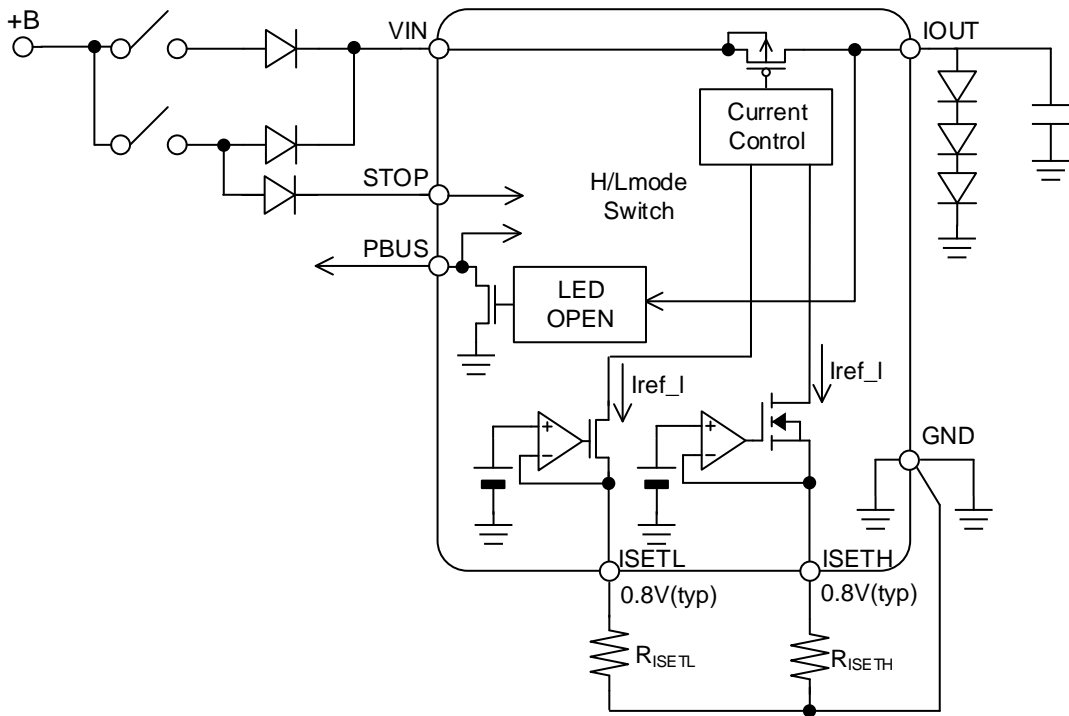


Figure 14. Current setting method

- L mode (STOP=Low)

$$I_{IOUT} = \frac{0.8V}{R_{ISETL}} \times 250A$$

exp) $R_{ISETL} = 40k\Omega$ $I_{IOUT} = \frac{0.8V}{40k\Omega} \times 250 = 5mA$

- H mode (STOP=High)

$$I_{IOUT} = \frac{0.8V}{R_{ISETH}} \times 2500A$$

exp) $R_{ISETH} = 40k\Omega$ $I_{IOUT} = \frac{0.8V}{40k\Omega} \times 2500 = 50mA$

3. Current Control at Output Saturation

When $V_{IOUT} (=V_F) - V_{IN} > 0.5V$ (TYP), the LED current I_F is decreased to a set current $20\mu A$ (TYP). Therefore, V_F decreases due to the decrease in the current. Open detection can be prevented by keeping $V_{IOUT} \leq V_{IN} - 0.5V$. The current controlled to $I_{OUT} < 20\mu A$ and the LED current I_F must be set so that V_F does not exceed V_{UVLO_OPEN} by $20\mu A$. If $V_{IN} < V_{UVLO_OPEN}$ this function is not active.

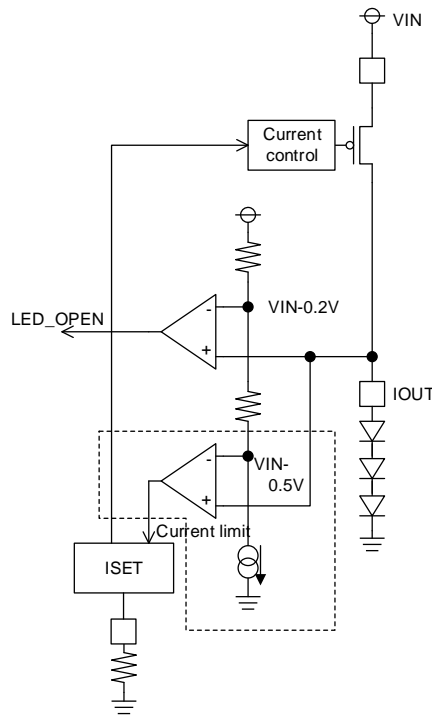
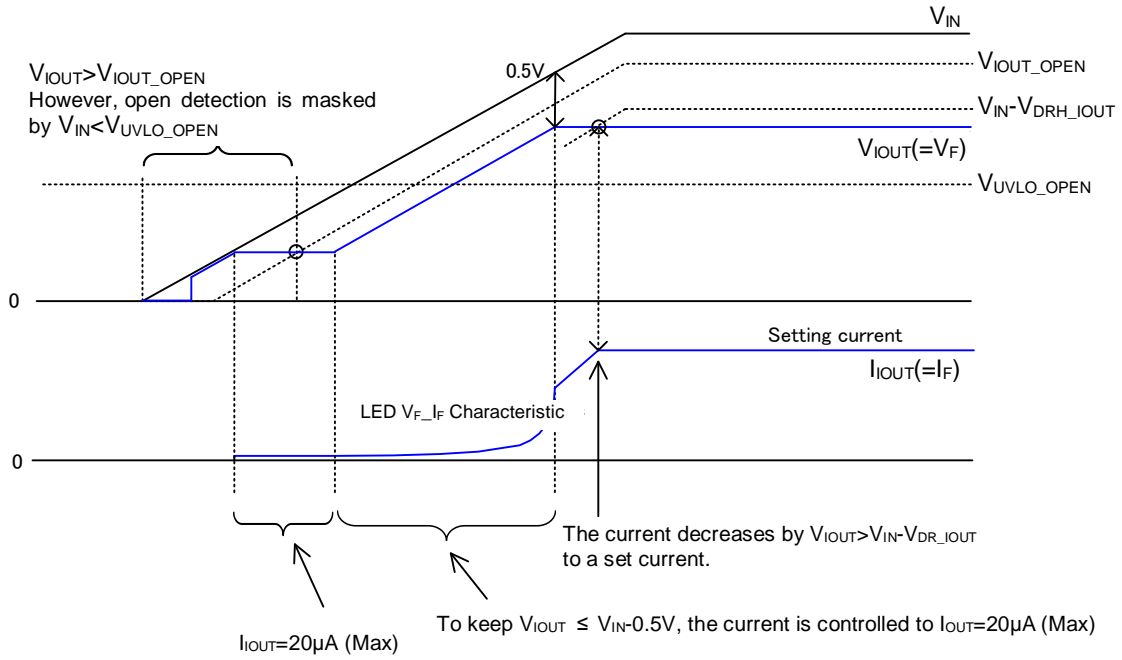


Figure 15. Current Control at Output Saturation

4. PROTECT BUS (PBUS)

PBUS is an I/O terminal that outputs any detected error by switching PBUS from Hi-Z (Note 1) to Low. The output current can also be turned OFF by pulling the PBUS Low. When driving multiple LEDs through multiple ICs, as shown in the figure below, all the rows of LEDs can be turned OFF by any fault by connecting PBUS terminal to each IC.

(Note1) PBUS terminal is an open drain terminal. Even when used separately, please be pulled up(10kΩ) to power supply voltage.

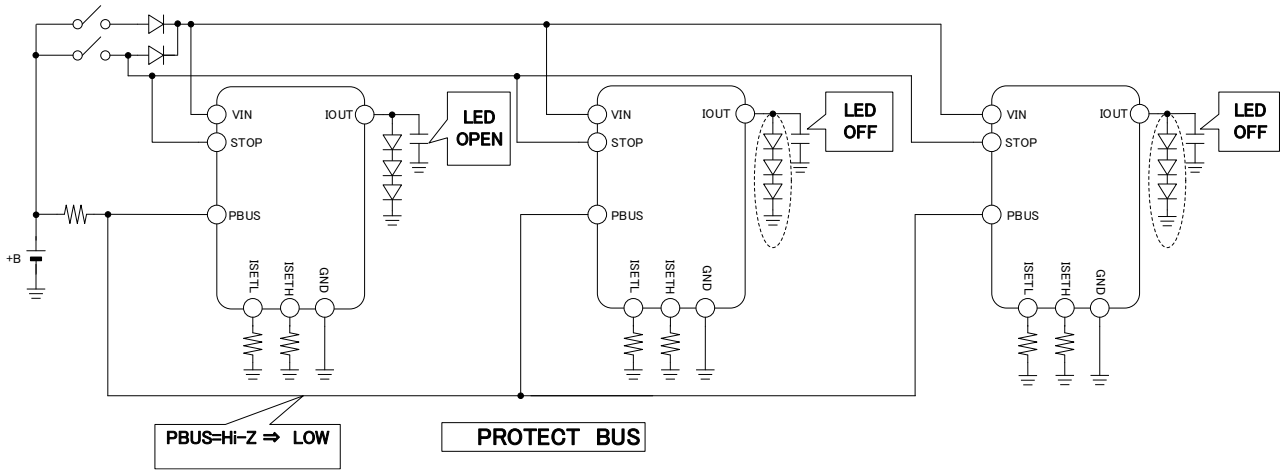


Figure 16. PBUS Function

- Example of operating protection for an LED open condition

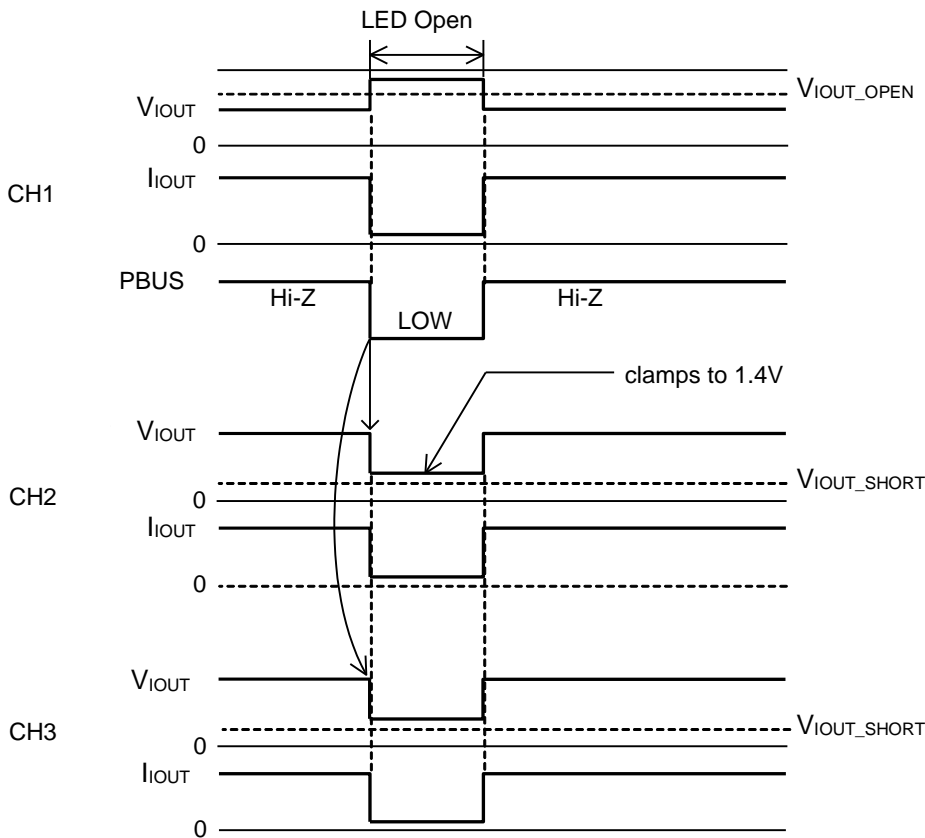


Figure 17. Example of protective Operation

When LED becomes open on the first IC, PBUS of IC1 is switched from Hi-Z to Low. As PBUS becomes Low, the other ICs detect the error and turns OFF their own LEDs. V_{IOUT} clamps to 1.4V during the OFF period in order to prevent ground short protection.

5. Protection Function

This IC has built-in short/open protection function for the external components. Any error detected will pull the PBUS terminal low.

(1) LED Open Detecting Function

When any LED connected at the IOOUT becomes open, V_{IOOUT} will go HIGH. When an error is detected at $V_{IOOUT} < V_{IOOUT_OPEN}$ the PBUS is pulled LOW.

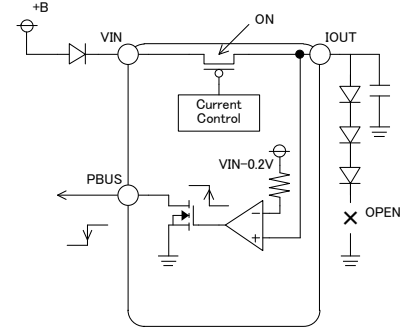


Figure 18. LED Open detection function

(2) LED Short Detecting Function

When the LEDs connected at the IOOUT terminal are shorted to ground, V_{IOOUT} will go LOW. When an error is detected at $V_{IOOUT} < V_{IOOUT_SHORT}$ 0.6V (TYP) the output current is turned OFF to prevent IC heating and the PBUS is pulled LOW.

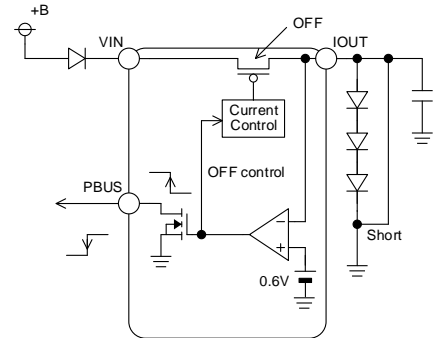


Figure 19. LED Short detection function

(3) ISET(H/L) Open Detection Function

When the external resistance connected to ISET(H/L) terminal is open, ISET(H/L) open detection will be activated by decreasing the ISET(H/L) terminal current. At L mode, ISETL open detection is activated nevertheless state of the ISETH terminal. Also at H mode, ISETH open detection is activated nevertheless state of the ISETL terminal. The output current is turned off While detecting open and it can be notify the abnormally by changing the PBUS terminal output to low.

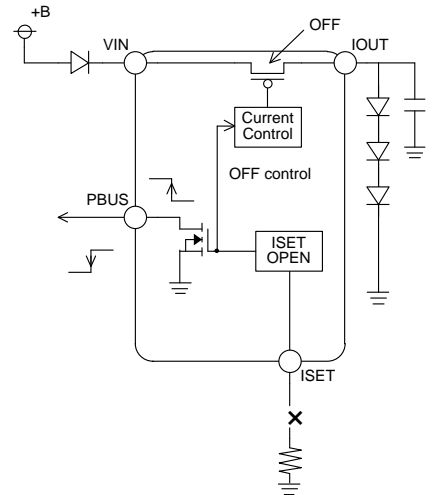


Figure 20. ISET Pin open detection function

(4) ISET(H/L) Short Detection Function

When the external resistance connected to ISET(H/L) terminal is short to GND, ISET(H/L) short detection will be activated by increasing the ISET(H/L) terminal current. At L mode, ISETL short detection is activated nevertheless state of the ISETH terminal. Also at H mode, ISETH short detection is activated nevertheless state of the ISETL terminal. The output current is turned off While detecting short to GND and it can be notify the abnormally by changing the PBUS terminal output to low.

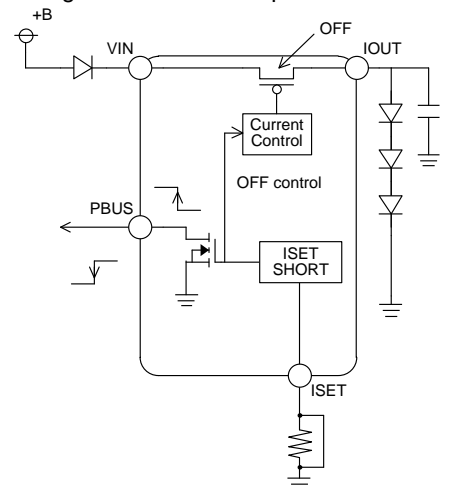


Figure 21. ISET Pin short detection function

6. Over Voltage Protection

Overvoltage protection works in ($R_{\text{SETH}}=40\text{k}\Omega$), $18\text{V (TYP)} \leq V_{\text{IN}}$ at $I_{\text{OUT}}=200\text{mA}$ setting and limits output current to suppress the upswing in heat generation of LSI.
The overvoltage mute protection is effective only for (STOP=High) at H mode time.

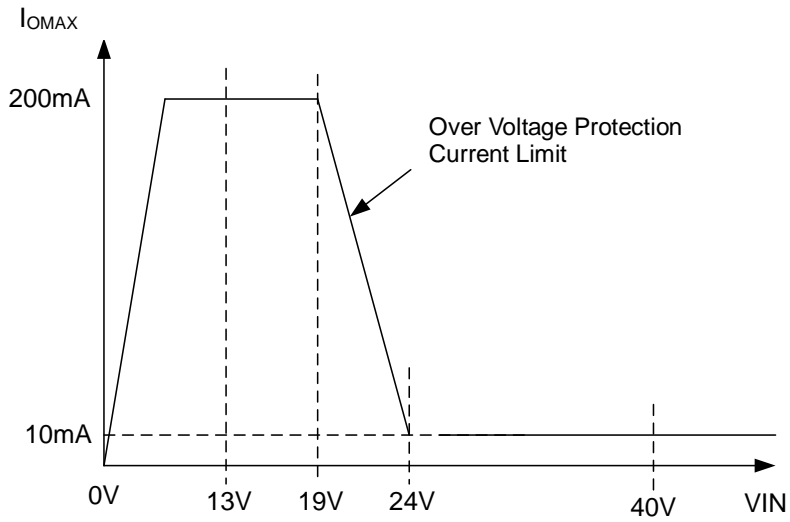


Figure 22. Overvoltage mute function

Recommended application circuit

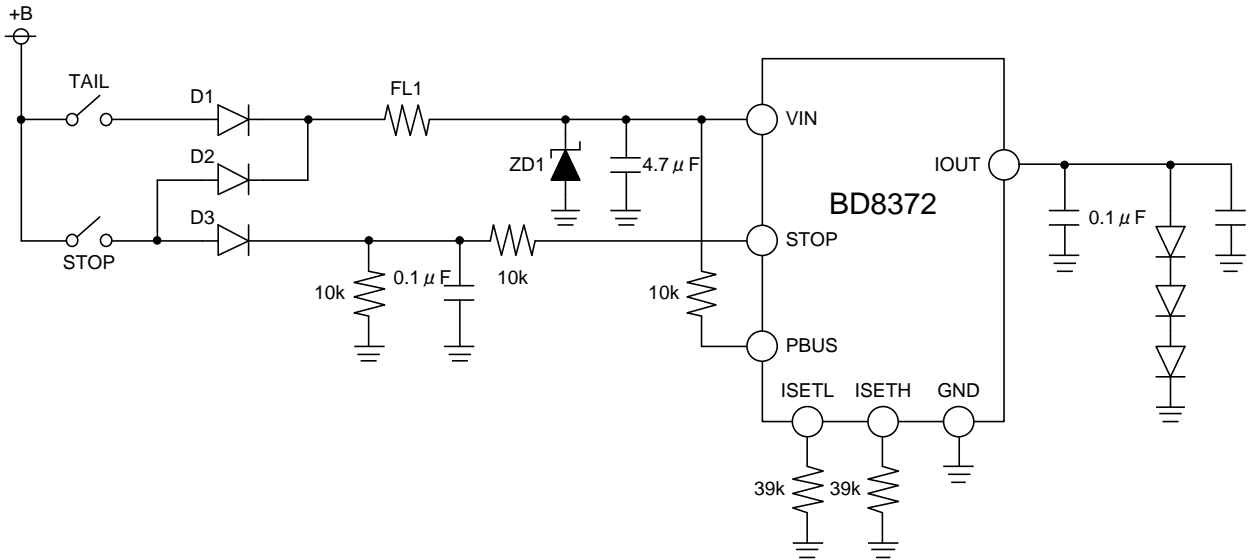


Figure 23. Recommended application circuit

(Note) EMC

ISO 11452-2 (ALSE)

ISO 11452-4 (BCI)

ISO 7637-2

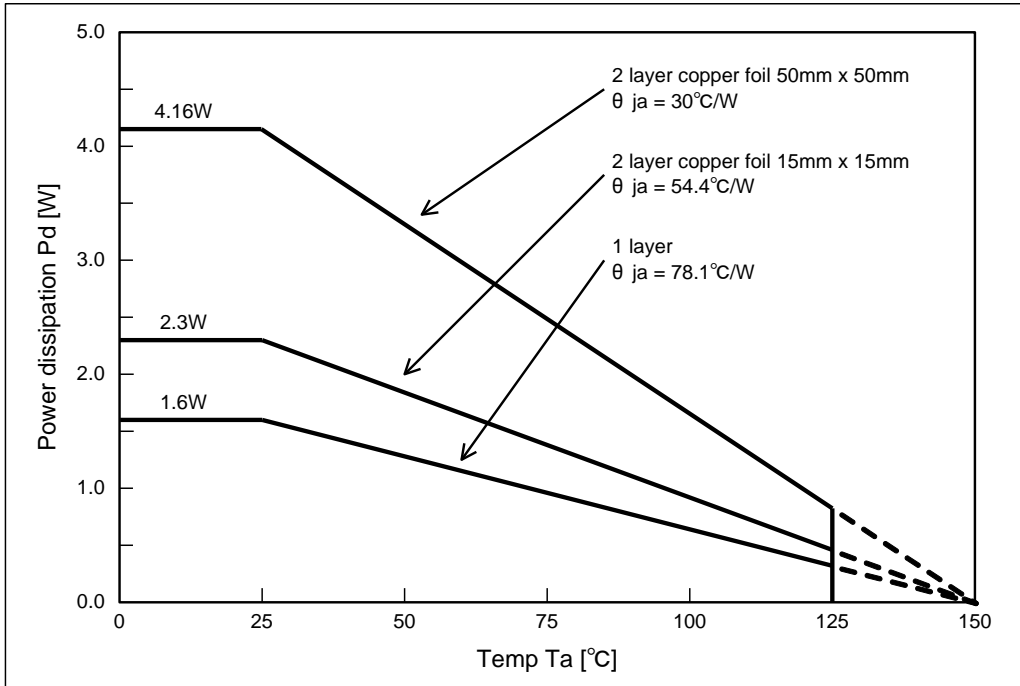
- pulse1
- Pulse2a,2b (level4)
- Pulse3a,3b (level4)

No.	Component Name	Component Value	Product Name	Company
1	D1	-	RF201L2S	ROHM
2	D2	-	RF201L2S	ROHM
3	D3	-	RF201L2S	ROHM
4	Z _{D1}	-	TNR12H-220K	NIPPON CHEMICON
5	FL1	-	MMZ2012R102A	TDK
6	C _{VIN}	4.7μF	GCM32ER71H475KA40	murata
7	C _{IOUT}	0.1μF	GCM188R11H104KA42	murata
8	C _{STOP}	0.1μF	GCM188R11H104KA42	murata
9	R _{ISETL}	39kΩ	MCR03 Series	ROHM
10	R _{ISETH}	39kΩ	MCR03 Series	ROHM
11	R _{PBUS}	10kΩ	MCR03 Series	ROHM
12	R1	10kΩ	MCR03 Series	ROHM
13	R2	10kΩ	MCR03 Series	ROHM

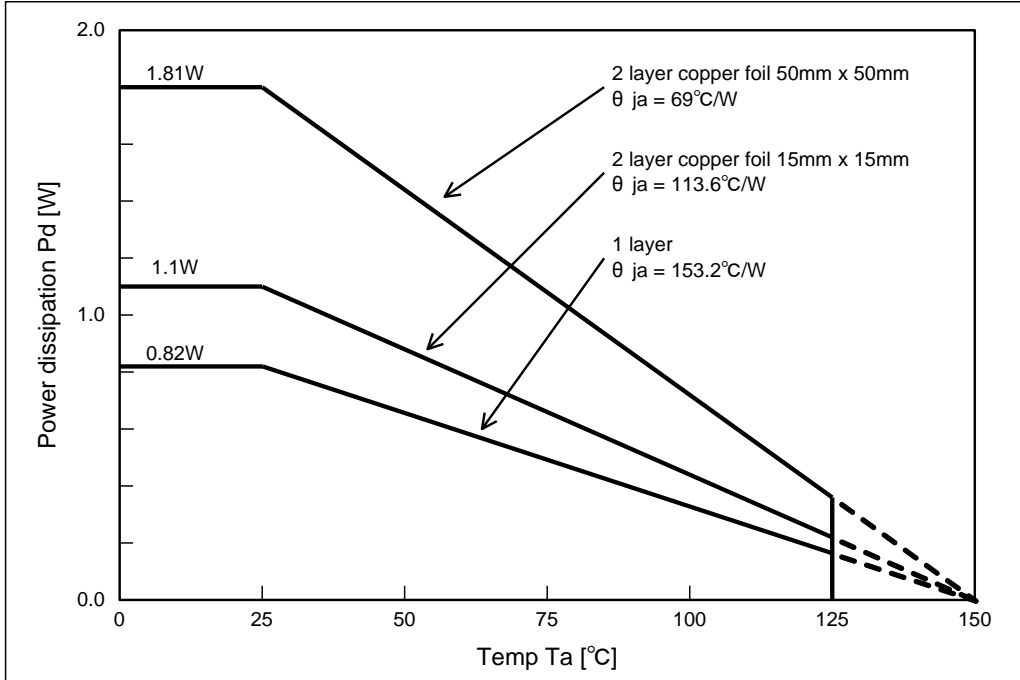
Table 1. BOM List

Power Dissipation

HRP7 Package



HTSOP-J8 Package



- (Caution1) When mounted with 70.0mm x 70.0mm x 1.6mm glass epoxy substrate.
- (Caution2) Above copper foil area indicates backside copper foil area.
- (Caution3) Value changes according to number of substrate layers and copper foil area. Note that this value is a measured value. Not a guaranteed value.

Figure 24. Thermal Dissipation Curve

Pd (Power dissipation) and I_{OMAX} (Permissible current)

The relation between Pd and I_{OMAX} by V_F of LED connected with IO_{UT} is shown.

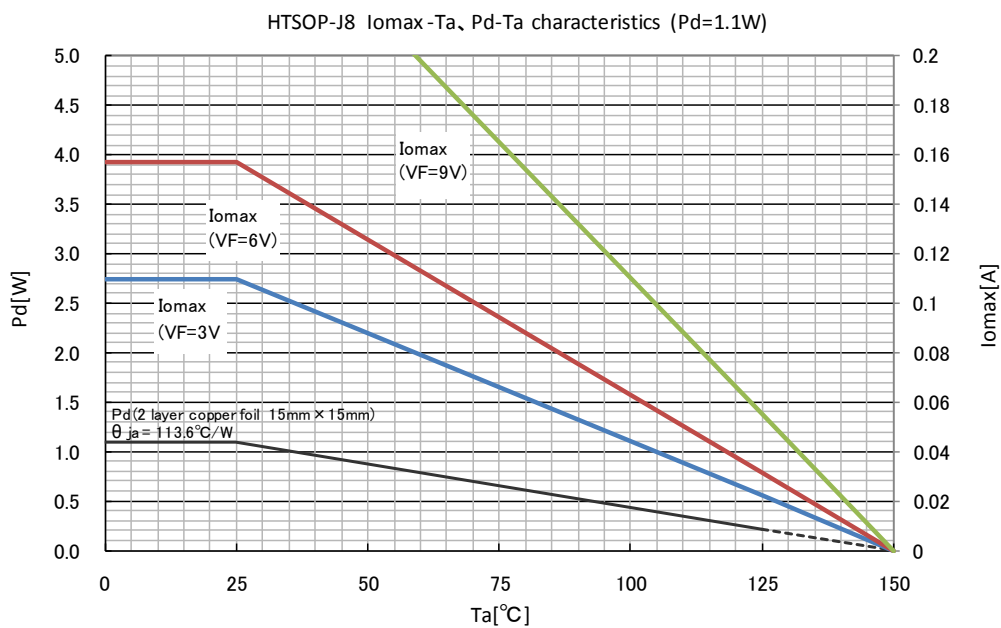
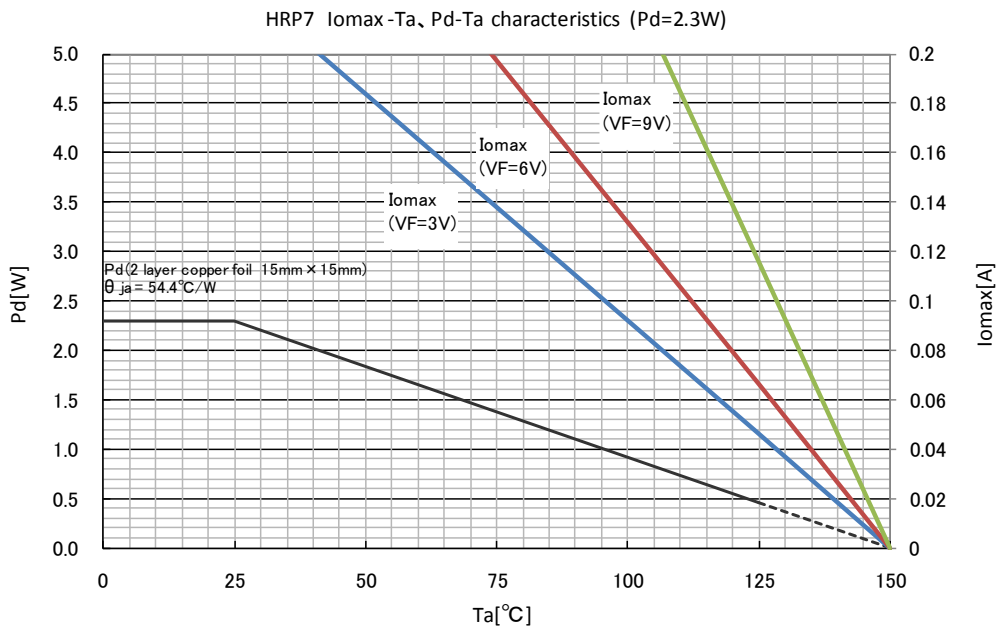
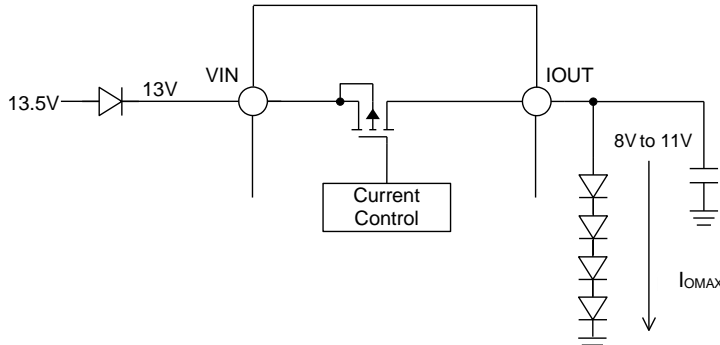


Figure 25. Heat reduction curve

I/O Equivalent Circuit (HRP7 Package)

Pin No.	Pin Name	I/O Equivalent Circuit
1	STOP	
2	PBUS	
3	ISETL	
4	GND	-

I/O Equivalent Circuit (HRP7 Package)– continued

Pin No.	Pin Name	I/O Equivalent Circuit
5	ISETH	
6	VIN	-
7	IOUT	

Operational Notes

- 1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
- 2. Power Supply Lines**

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- 3. Ground Voltage**

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
- 4. Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
- 5. Thermal Consideration**

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
- 6. Recommended Operating Conditions**

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- 7. Inrush Current**

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
- 8. Operation Under Strong Electromagnetic Field**

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 9. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- 10. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

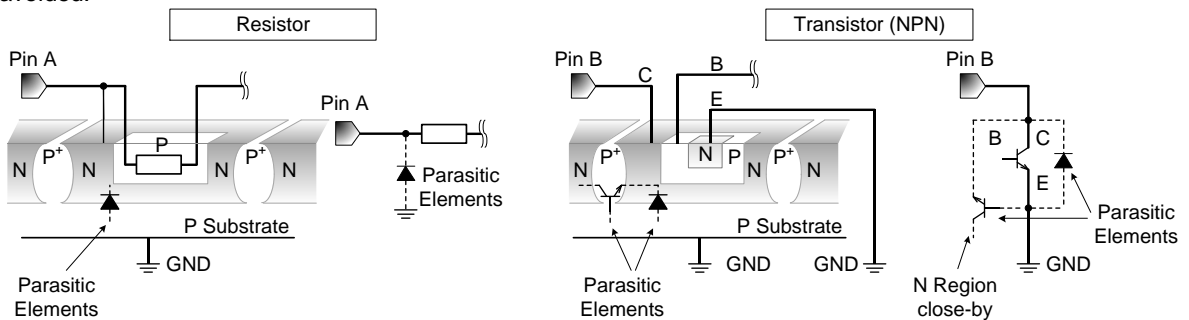


Figure 26. Example of monolithic IC structure

13. **Thermal Shutdown Circuit(TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. **Sudden Voltage Surge on VIN**

Because MOSFETs are used in the output, a very steep change in the VCC voltage may cause the transistors to conduct large current. Take this condition into account when selecting the value of external circuit constants for a certain application.

Ordering Information

B D 8 3 7 2 H F P - **M T R**

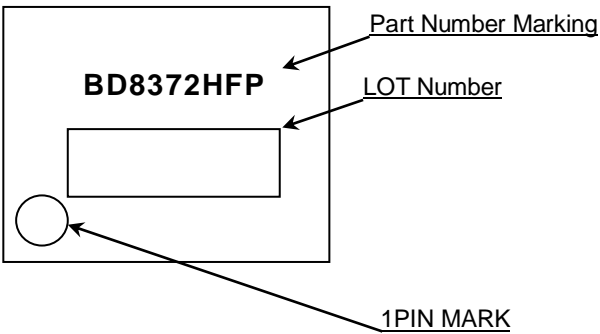
Form name	Package HFP : HRP7	Packaging and forming specification TR: Embossed tape and reel (HRP7)
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B D 8 3 7 2 E F J - **M E 2**

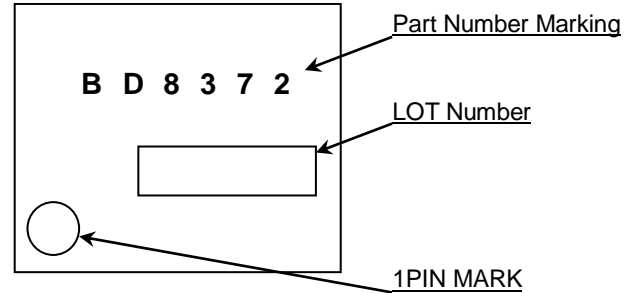
Form name	Package EFJ : HTSOP-J8	Packaging and forming specification E2: Embossed tape and reel (HTSOP-J8)
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Marking Diagrams

HRP7 (TOP VIEW)

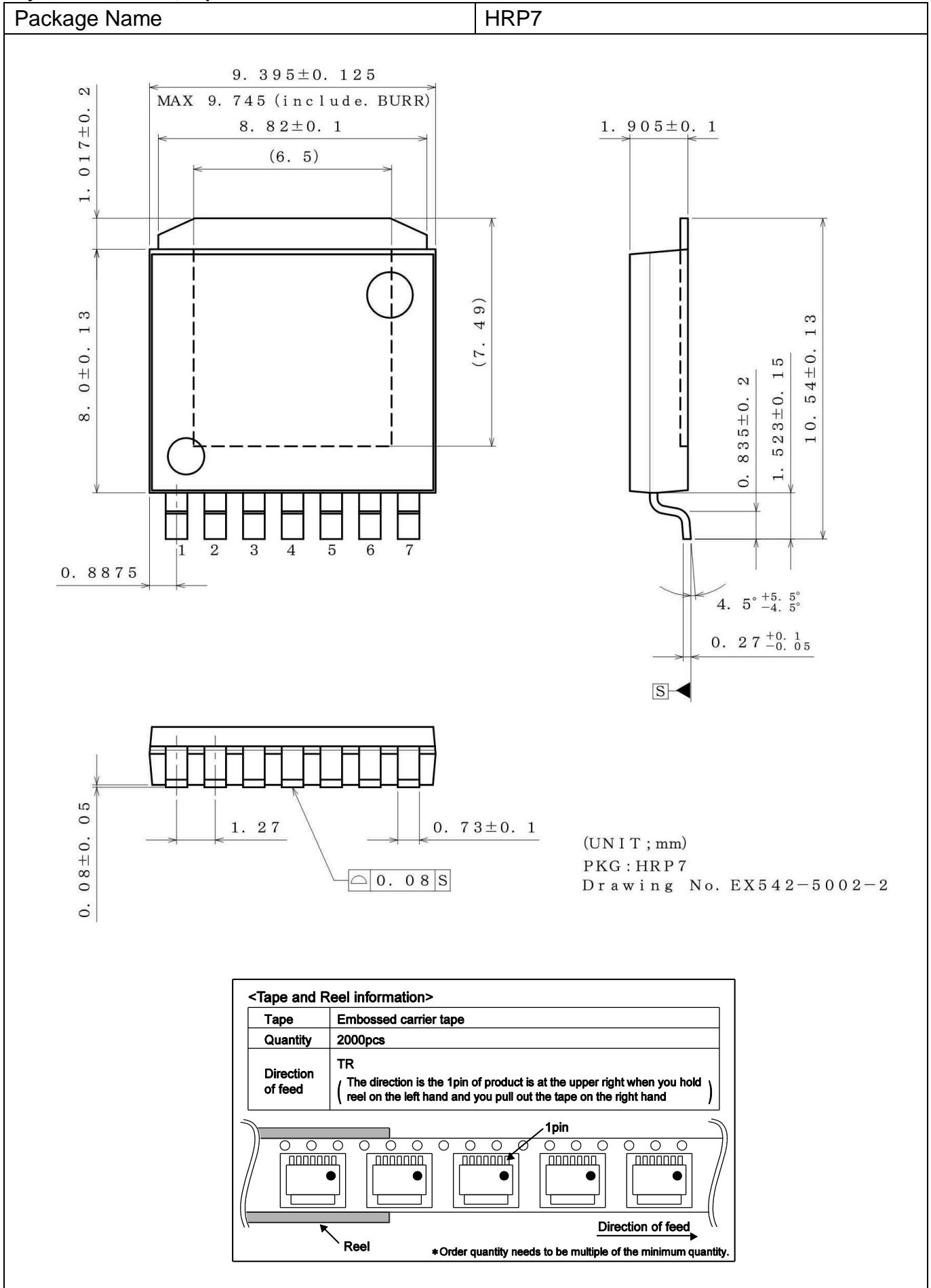


HTSOP-J8(TOP VIEW)



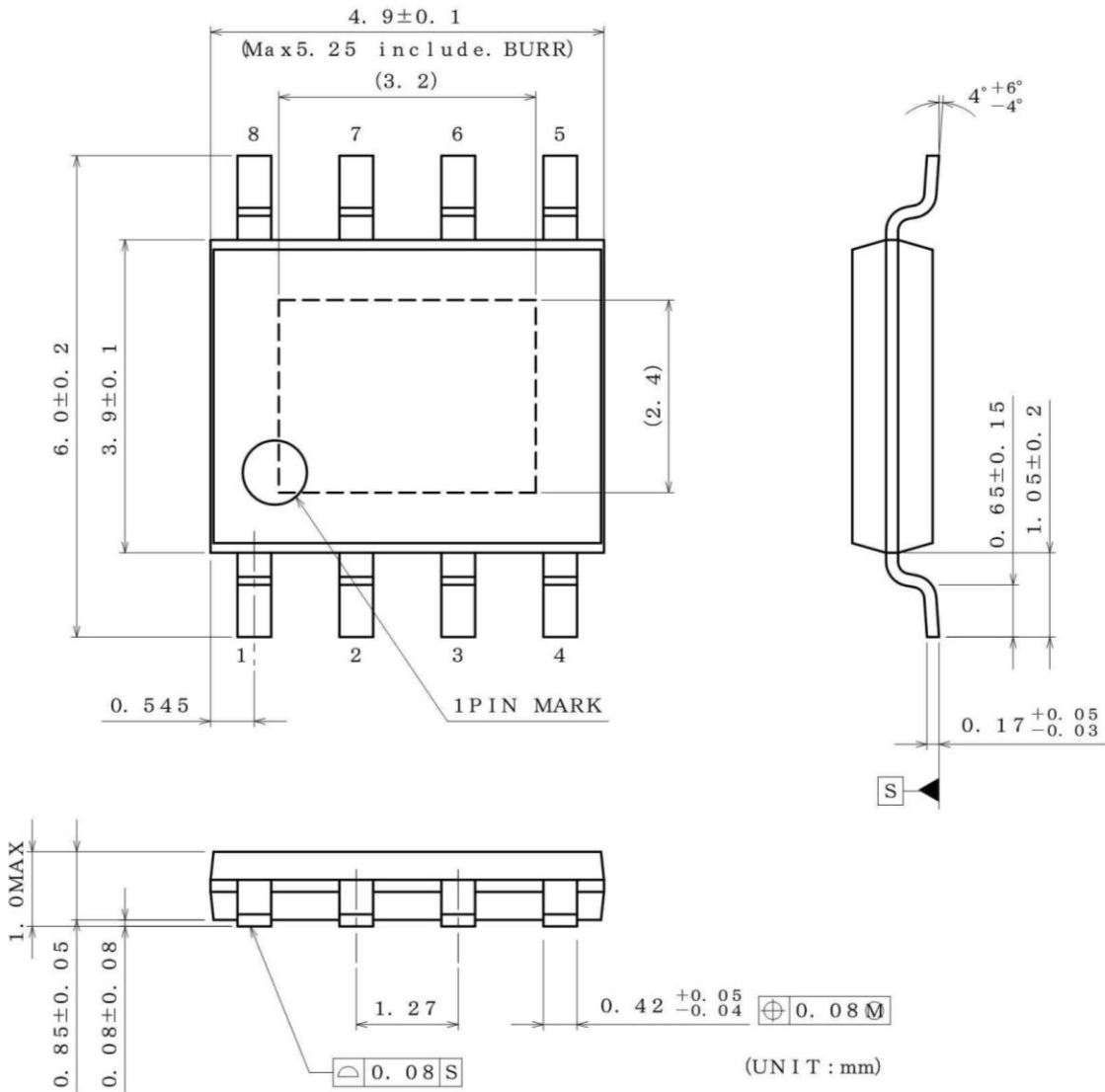
Part Number Marking	Package		Part Number
BD8372HFP	HRP7	Reel of 2000	BD8372HFP-MTR
BD8372	HTSOP-J8	Reel of 2500	BD8372EFJ-ME2

Physical Dimension, Tape and Reel Information



Physical Dimension, Tape and Reel Information – continued

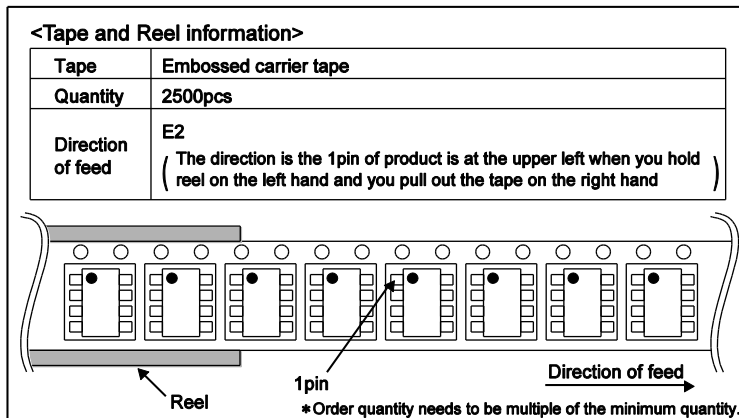
Package Name	HTSOP-J8
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(UNIT : mm)

PKG : HTSOP-J8

Drawing No. EX169-5002-2



Revision History

Date	Revision	Changes
06.Nov.2015	001	New Release
		Page. 5 Circuit Current Symbol $I_{IN} \Rightarrow I_{VIN}$ STOP Input Current Symbol $V_{IN_STOP} \Rightarrow I_{IN_STOP}$ IN Over Voltage Current \Rightarrow Over Voltage Mute Voltage
		Page. 8 Figure 13. Timing chart modify
		Page. 10 exp) $R_{ISETL} = 16k\Omega \Rightarrow$ exp) $R_{ISETL} = 40k\Omega$
		Page. 11 Figure 15. $V_{ULOO_OPEN} \Rightarrow V_{UVLO_OPEN}$ $V_{DRH_IOUT} \Rightarrow V_{DRH_IOUT}$
09.Oct.2018	002	Page.13 Figure 18. 20. 21. modify 5. Protection Function PUBS \Rightarrow PBUS (3)ISET(H/L) Open Detection Function change words (4)ISET(H/L) Short Detection Function change words
		Page.15 Figure 23. $2.5k\Omega@100MHz$ delete comment Table 1. BOM List 5 FL1 HMZ2012R102A \Rightarrow MMZ2012R102A
		Page.18 I/O Equivalent Circuit add word (HRP7 Package) 2 PBUS (28pin) \Rightarrow (2pin)

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [h] Use of the Products in places subject to dew condensation
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