

ANY-FREQUENCY PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Features

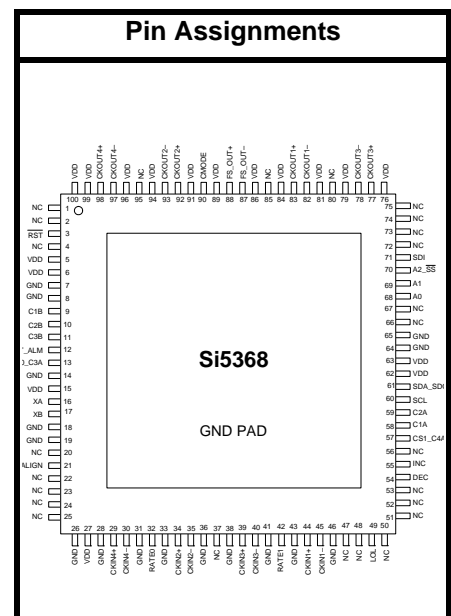
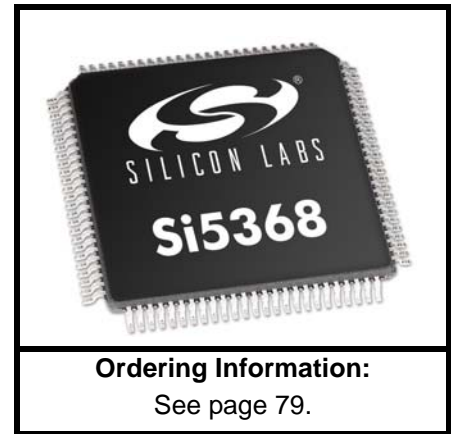
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 300 fs rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Four clock inputs with manual or automatically controlled hitless switching and phase build-out
- Small size: 14 x 14 mm 100-pin TQFP
- Supports holdover and freerun modes of operation
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- SONET frame sync switching and regeneration
- Support for ITU G.709 and custom FEC ratios (253/226, 239/237, 255/238, 255/237, 255/236)
- LOL, LOS, FOS alarm outputs
- Digitally-controlled output phase adjust
- I²C or SPI programmable settings
- Pb-free, RoHS compliant

Applications

- SONET/SDH OC-48/STM-16/OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10/16G Fibre Channel
- ITU G.709 and custom FEC line cards
- Wireless basestations
- Data converter clocking
- OTN/WDM Muxponder, MSPP, ROADM line cards
- SONET/SDH + PDH clock synthesis
- Test and measurement
- Synchronous Ethernet
- Broadcast video

Description

The Si5368 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5368 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5368 input clock frequency and clock multiplication ratio are programmable through an I²C or SPI interface. The Si5368 is based on Silicon Laboratories' third-generation DSPLL[®] technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5368 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.



Si5368

Functional Block Diagram

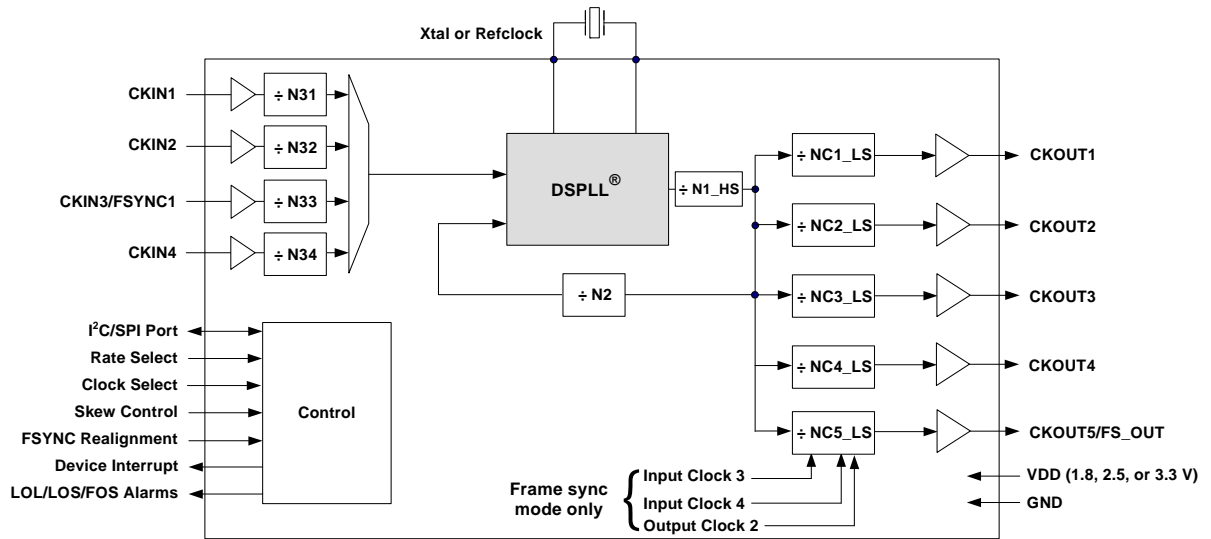


TABLE OF CONTENTS

| <u>Section</u> | <u>Page</u> |
|---|--------------------|
| 1. Electrical Specifications | 4 |
| 2. Typical Phase Noise Performance | 17 |
| 3. Typical Application Circuits | 18 |
| 4. Functional Description | 20 |
| 4.1. External Reference | 20 |
| 4.2. Further Documentation | 21 |
| 5. Register Map | 22 |
| 6. Register Descriptions | 25 |
| 7. Pin Descriptions: Si5368 | 79 |
| 8. Ordering Guide | 86 |
| 9. Package Outline: 100-Pin TQFP | 87 |
| 10. Recommended PCB Layout | 88 |
| 11. Top Marking: 100-Pin TQFP | 90 |
| 11.1. Si5368 Top Marking | 90 |
| 11.2. Top Marking Explanation | 90 |
| Document Change list | 91 |
| Contact Information | 92 |

1. Electrical Specifications

Table 1. Recommended Operating Conditions¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------|----------------------------|------|-----|------|------|
| Ambient Temperature | T_A | | -40 | 25 | 85 | C |
| Supply Voltage during Normal Operation | V_{DD} | 3.3 V Nominal ² | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V Nominal | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V Nominal | 1.71 | 1.8 | 1.89 | V |

Notes:

- All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
- The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics
 $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ } ^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|----------|---|-----|-----|-----|------|
| Supply Current ^{1,6} | I_{DD} | LVPECL Format 622.08 MHz Out All CKOUTs Enabled | — | 394 | 435 | mA |
| | | LVPECL Format 622.08 MHz Out 1 CKOUT Enabled | — | 253 | 284 | mA |
| | | CMOS Format 19.44 MHz Out All CKOUTs Enabled | — | 278 | 400 | mA |
| | | CMOS Format 19.44 MHz Out 1 CKOUT Enabled | — | 229 | 261 | mA |
| | | Disable Mode | — | 165 | — | mA |

Notes:

- Current draw is independent of supply voltage
- No under- or overshoot is allowed.
- LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$.
- This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
- LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$.
- The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------|---|-----------------|-----------------|-----------------|------------|
| CKINn Input Pins² | | | | | | |
| Input Common Mode Voltage (Input Threshold Voltage) | V_{ICM} | 1.8 V \pm 5% | 0.9 | — | 1.4 | V |
| | | 2.5 V \pm 10% | 1 | — | 1.7 | V |
| | | 3.3 V \pm 10% | 1.1 | — | 1.95 | V |
| Input Resistance | CKN_{RIN} | Single-ended | 20 | 40 | 60 | k Ω |
| Single-Ended Input Voltage Swing (See Absolute Specs) | V_{ISE} | $f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1. | 0.2 | — | — | V_{PP} |
| | | $f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1. | 0.25 | — | — | V_{PP} |
| Differential Input Voltage Swing (See Absolute Specs) | V_{ID} | $f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1. | 0.2 | — | — | V_{PP} |
| | | $f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1. | 0.25 | — | — | V_{PP} |
| Output Clocks (CKOUTn)^{3,5,6} | | | | | | |
| Common Mode | CKO_{VCM} | LVPECL 100 Ω load line-to-line | $V_{DD} - 1.42$ | — | $V_{DD} - 1.25$ | V |
| Differential Output Swing | CKO_{VD} | LVPECL 100 Ω load line-to-line | 1.1 | — | 1.9 | V_{PP} |
| Single Ended Output Swing | CKO_{VSE} | LVPECL 100 Ω load line-to-line | 0.5 | — | 0.93 | V_{PP} |
| Differential Output Voltage | CKO_{VD} | CML 100 Ω load line-to-line | 350 | 425 | 500 | m V_{PP} |
| Common Mode Output Voltage | CKO_{VCM} | CML 100 Ω load line-to-line | — | $V_{DD} - 0.36$ | — | V |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. Current draw is independent of supply voltage 2. No under- or overshoot is allowed. 3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$. 4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details. 5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$. 6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. | | | | | | |

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|--|---------------------|------|-------|------------------|
| Differential Output Voltage | CKO _{VD} | LVDS 100 Ω load line-to-line | 500 | 700 | 900 | mV _{PP} |
| | | Low Swing LVDS 100 Ω load line-to-line | 350 | 425 | 500 | mV _{PP} |
| Common Mode Output Voltage | CKO _{VCM} | LVDS 100 Ω load line-to-line | 1.125 | 1.2 | 1.275 | V |
| Differential Output Resistance | CKO _{RD} | CML, LVPECL, LVDS | — | 200 | — | Ω |
| Output Voltage Low | CKO _{VOLLH} | CMOS | — | — | 0.4 | V |
| Output Voltage High | CKO _{VOHLH} | $V_{DD} = 1.71 \text{ V}$ CMOS | $0.8 \times V_{DD}$ | — | — | V |
| Output Drive Current (CMOS driving into CKO _{VOL} for output low or CKO _{VOH} for output high. CKOUT+ and CKOUT– shorted externally) | CKO _{IO} | ICMOS[1:0] =11 $V_{DD} = 1.8 \text{ V}$ | — | 7.5 | — | mA |
| | | ICMOS[1:0] =10 $V_{DD} = 1.8 \text{ V}$ | — | 5.5 | — | mA |
| | | ICMOS[1:0] =01 $V_{DD} = 1.8 \text{ V}$ | — | 3.5 | — | mA |
| | | ICMOS[1:0] =00 $V_{DD} = 1.8 \text{ V}$ | — | 1.75 | — | mA |
| | | ICMOS[1:0] =11 $V_{DD} = 3.3 \text{ V}$ | — | 32 | — | mA |
| | | ICMOS[1:0] =10 $V_{DD} = 3.3 \text{ V}$ | — | 24 | — | mA |
| | | ICMOS[1:0] =01 $V_{DD} = 3.3 \text{ V}$ | — | 16 | — | mA |
| | | ICMOS[1:0] =00 $V_{DD} = 3.3 \text{ V}$ | — | 8 | — | mA |

Notes:

1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics (Continued)(V_{DD} = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------|--------------------------|-----|-----|-----|------|
| 2-Level LVCMOS Input Pins | | | | | | |
| Input Voltage Low | V _{IL} | V _{DD} = 1.71 V | — | — | 0.5 | V |
| | | V _{DD} = 2.25 V | — | — | 0.7 | V |
| | | V _{DD} = 2.97 V | — | — | 0.8 | V |
| Input Voltage High | V _{IH} | V _{DD} = 1.89 V | 1.4 | — | — | V |
| | | V _{DD} = 2.25 V | 1.8 | — | — | V |
| | | V _{DD} = 3.63 V | 2.5 | — | — | V |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. Current draw is independent of supply voltage 2. No under- or overshoot is allowed. 3. LVPECL outputs require nominal VDD ≥ 2.5 V. 4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details. 5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz. 6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. | | | | | | |

Table 2. DC Characteristics (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|--|----------------------|-----|----------------------|---------------|
| 3-Level Input Pins⁴ | | | | | | |
| Input Voltage Low | V_{ILL} | | — | — | $0.15 \times V_{DD}$ | V |
| Input Voltage Mid | V_{IMM} | | $0.45 \times V_{DD}$ | — | $0.55 \times V_{DD}$ | V |
| Input Voltage High | V_{IHH} | | $0.85 \times V_{DD}$ | — | — | V |
| Input Low Current | I_{ILL} | See Note 4 | -20 | — | — | μA |
| Input Mid Current | I_{IMM} | See Note 4 | -2 | — | +2 | μA |
| Input High Current | I_{IHH} | See Note 4 | — | — | 20 | μA |
| LVC MOS Output Pins | | | | | | |
| Output Voltage Low | V_{OL} | $I_O = 2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$ | — | — | 0.4 | V |
| Output Voltage Low | | $I_O = 2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$ | — | — | 0.4 | V |
| Output Voltage High | V_{OH} | $I_O = -2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$ | $V_{DD} - 0.4$ | — | — | V |
| Output Voltage High | | $I_O = -2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$ | $V_{DD} - 0.4$ | — | — | V |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. Current draw is independent of supply voltage 2. No under- or overshoot is allowed. 3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$. 4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details. 5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$. 6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS. | | | | | | |

Table 3. AC Specifications(V_{DD} = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|--|-------|-----|-------|-----------------|
| Single-Ended Reference Clock Input Pin XA (XB with cap to GND) | | | | | | |
| Input Resistance | XA _{RIN} | RATE[1:0] = LM, MH, ac coupled | — | 12 | — | kΩ |
| Input Voltage Swing | XA _{VPP} | RATE[1:0] = LM, MH, ac coupled | 0.5 | — | 1.2 | V _{PP} |
| Differential Reference Clock Input Pins (XA/XB) | | | | | | |
| Input Voltage Swing | XA/XB _{VPP} | RATE[1:0] = LM, MH | 0.5 | — | 2.4 | V _{PP} |
| CKINn Input Pins | | | | | | |
| Input Frequency | CKN _F | Input frequency and clock multiplication ratio determined by programming device PLL dividers. Consult Silicon Laboratories configuration software <i>DSPLLsim</i> or Any-Frequency Precision Clock Family Reference Manual at www.silabs.com/timing (click on Documentation) to determine PLL divider settings for a given input frequency/clock multiplication ratio combination | 0.002 | — | 710 | MHz |
| Input Clock Frequency (CKIN3, CKIN4 used as FSYNC inputs) | CK _F | | 0.002 | — | 0.512 | MHz |
| Input Duty Cycle (Minimum Pulse Width) | CKN _{DC} | Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks) | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| Input Capacitance | CKN _{CIN} | | — | — | 3 | pF |
| Input Rise/Fall Time | CKN _{TRF} | 20–80% See Figure 2 | — | — | 11 | ns |
| *Note: Input to output phase skew after an ICAL is not controlled and can assume any value. | | | | | | |

Table 3. AC Specifications (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|---|-------|-----|----------|-------------------|
| CKOUTn Output Pins | | | | | | |
| (See ordering section for speed grade vs frequency limits) | | | | | | |
| Output Frequency (Output not configured for CMOS or Disabled) | CKO _F | N1 ≥ 6 | 0.002 | — | 945 | MHz |
| | | N1 = 5 | 970 | — | 1134 | MHz |
| | | N1 = 4 | 1.213 | — | 1.4 | GHz |
| Maximum Output Frequency in CMOS Format | CKO _F | | — | — | 212.5 | MHz |
| Output Rise/Fall (20–80 %) @ 622.08 MHz output | CKO _{TRF} | Output not configured for CMOS or Disabled See Figure 2 | — | 230 | 350 | ps |
| Output Rise/Fall (20–80%) @ 212.5 MHz output | CKO _{TRF} | CMOS Output V _{DD} = 1.71 C _{LOAD} = 5 pF | — | — | 8 | ns |
| Output Rise/Fall (20–80%) @ 212.5 MHz output | CKO _{TRF} | CMOS Output V _{DD} = 2.97 C _{LOAD} = 5 pF | — | — | 2 | ns |
| Output Duty Cycle Uncertainty @ 622.08 MHz | CKO _{DC} | 100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS) | — | — | ±40 | ps |
| LVC MOS Input Pins | | | | | | |
| Minimum Reset Pulse Width | t _{RSTMN} | | 1 | | | μs |
| Reset to Microprocessor Access Ready | t _{READY} | | | | 10 | ms |
| Input Capacitance | C _{in} | | — | — | 3 | pF |
| LVC MOS Output Pins | | | | | | |
| Rise/Fall Times | t _{RF} | C _{LOAD} = 20pf See Figure 2 | — | 25 | — | ns |
| LOSn Trigger Window | LOS _{TRIG} | From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1 | — | — | 4.5 x N3 | T _{CKIN} |
| Time to Clear LOL after LOS Cleared | t _{CLRLOL} | ↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference | — | 10 | — | ms |
| *Note: Input to output phase skew after an ICAL is not controlled and can assume any value. | | | | | | |

Table 3. AC Specifications (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ } ^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|---------|------|------|----------|
| Device Skew | | | | | | |
| Output Clock Skew | t_{SKEW} | \uparrow of CKOUT _n to \uparrow of CKOUT _m , CKOUT _n and CKOUT _m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1 | — | — | 100 | ps |
| Phase Change due to Temperature Variation* | t_{TEMP} | Max phase changes from -40 to $+85 \text{ } ^\circ\text{C}$ | — | 300 | 500 | ps |
| PLL Performance ($f_{\text{in}} = f_{\text{out}} = 622.08 \text{ MHz}$; BW = 120 Hz; LVPECL) | | | | | | |
| Lock Time | t_{LOCKMP} | Start of ICAL to \downarrow of LOL | — | 35 | 1200 | ms |
| Output Clock Phase Change | $t_{\text{P_STEP}}$ | After clock switch $f_3 \geq 128 \text{ kHz}$ | — | 200 | — | ps |
| Closed Loop Jitter Peaking | J_{PK} | | — | 0.05 | 0.1 | dB |
| Jitter Tolerance | J_{TOL} | Jitter Frequency \geq Loop Bandwidth | 5000/BW | — | — | ns pk-pk |
| Phase Noise $f_{\text{out}} = 622.08 \text{ MHz}$ | CKO _{PN} | 1 kHz Offset | — | -106 | — | dBc/Hz |
| | | 10 kHz Offset | — | -121 | — | dBc/Hz |
| | | 100 kHz Offset | — | -132 | — | dBc/Hz |
| | | 1 MHz Offset | — | -132 | — | dBc/Hz |
| Spurious Noise | SP _{SPUR} | Max spur @ $n \times F_3$ ($n \geq 1, n \times F_3 < 100 \text{ MHz}$) | — | -93 | -70 | dBc |

*Note: Input to output phase skew after an ICAL is not controlled and can assume any value.

Table 4. Microprocessor Control

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|---|----------------------|-----|----------------------|------|
| I²C Bus Lines (SDA, SCL) | | | | | | |
| Input Voltage Low | $V_{IL_{I2C}}$ | | — | — | $0.25 \times V_{DD}$ | V |
| Input Voltage High | $V_{IH_{I2C}}$ | | $0.7 \times V_{DD}$ | — | V_{DD} | V |
| Hysteresis of Schmitt trigger inputs | $V_{HYS_{I2C}}$ | $V_{DD} = 1.8\text{V}$ | $0.1 \times V_{DD}$ | — | — | V |
| | | $V_{DD} = 2.5$ or 3.3 V | $0.05 \times V_{DD}$ | — | — | V |
| Output Voltage Low | $V_{OL_{I2C}}$ | $V_{DD} = 1.8 \text{ V}$ $I_O = 3 \text{ mA}$ | — | — | $0.2 \times V_{DD}$ | V |
| | | $V_{DD} = 2.5$ or 3.3 V $I_O = 3 \text{ mA}$ | — | — | 0.4 | V |

Table 4. Microprocessor Control (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------|----------------|-----|-----|-----|------|
| SPI Specifications | | | | | | |
| Duty Cycle, SCLK | t_{DC} | SCLK = 10 MHz | 40 | — | 60 | % |
| Cycle Time, SCLK | t_c | | 100 | — | — | ns |
| Rise Time, SCLK | t_r | 20–80% | — | — | 25 | ns |
| Fall Time, SCLK | t_f | 20–80% | — | — | 25 | ns |
| Low Time, SCLK | t_{lsc} | 20–20% | 30 | — | — | ns |
| High Time, SCLK | t_{hsc} | 80–80% | 30 | — | — | ns |
| Delay Time, SCLK Fall to SDO Active | t_{d1} | | — | — | 25 | ns |
| Delay Time, SCLK Fall to SDO Transition | t_{d2} | | — | — | 25 | ns |
| Delay Time, SS Rise to SDO Tri-state | t_{d3} | | — | — | 25 | ns |
| Setup Time, SS to SCLK Fall | t_{su1} | | 25 | — | — | ns |
| Hold Time, SS to SCLK Rise | t_{h1} | | 20 | — | — | ns |
| Setup Time, SDI to SCLK Rise | t_{su2} | | 25 | — | — | ns |
| Hold Time, SDI to SCLK Rise | t_{h2} | | 20 | — | — | ns |
| Delay Time between Slave Selects | t_{cs} | | 25 | — | — | ns |

Table 5. Jitter Generation

| Parameter | Symbol | Test Condition* | | Min | Typ | Max | GR-253-Specification | Unit |
|-------------------|--------|--------------------|-----------------------|-----|-----|------|----------------------|-------------------|
| | | Measurement Filter | DSPLL BW ² | | | | | |
| Jitter Gen OC-192 | JGEN | 0.02–80 MHz | 120 Hz | — | 4.2 | 6.2 | 30 | ps _{pp} |
| | | | | — | .27 | 0.42 | N/A | ps _{rms} |
| | | 4–80 MHz | 120 Hz | — | 3.7 | 6.4 | 10 | ps _{pp} |
| | | | | — | .14 | 0.31 | N/A | ps _{rms} |
| | | 0.05–80 MHz | 120 Hz | — | 4.4 | 6.9 | 10 | ps _{pp} |
| | | | | — | .26 | 0.41 | 1.0 | ps _{rms} |
| Jitter Gen OC-48 | JGEN | 0.12–20 MHz | 120 Hz | — | 3.5 | 5.4 | 40.2 | ps _{pp} |
| | | | | — | .27 | 0.41 | 4.02 | ps _{rms} |

***Note:** Test conditions:

1. f_{IN} = f_{OUT} = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. V_{DD} = 2.5 V
7. T_A = 85 °C
8. Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Value | Unit |
|--|-----------------|----------------|-------|------|
| Thermal Resistance Junction to Ambient | θ _{JA} | Still Air | 31 | C°/W |

Table 7. Absolute Maximum Limits

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------|----------------|------------------|-----|--------------|------|
| DC Supply Voltage | V_{DD} | | -0.5 | — | 3.8 | V |
| LVC MOS Input Voltage | V_{DIG} | | -0.3 | | $V_{DD}+0.3$ | V |
| CKINn Voltage Level Limits | CKN_{VIN} | | 0 | — | V_{DD} | V |
| XA/XB Voltage Level Limits | XA_{VIN} | | 0 | — | 1.2 | V |
| Operating Junction Temperature | T_{JCT} | | -55 | — | 150 | °C |
| Storage Temperature Range | T_{STG} | | -55 | — | 150 | °C |
| ESD HBM Tolerance (100 pF, 1.5 k Ω); All pins except CKIN+/CKIN- | | | 2 | — | — | kV |
| ESD MM Tolerance; All pins except CKIN+/CKIN- | | | 150 | — | — | V |
| ESD HBM Tolerance (100 pF, 1.5 k Ω); CKIN+/CKIN- | | | 700 | — | — | V |
| ESD MM Tolerance; CKIN+/CKIN- | | | 100 | — | — | V |
| Latch-up Tolerance | | | JESD78 Compliant | | | |
| Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions specified in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. | | | | | | |



Figure 1. Differential Voltage Characteristics

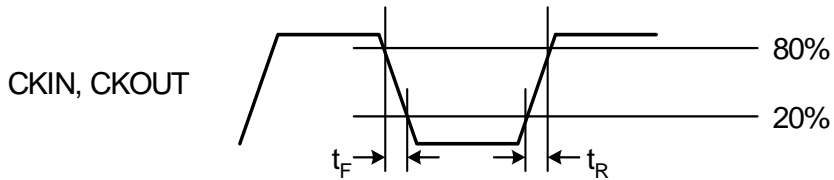


Figure 2. Rise/Fall Time Characteristics

2. Typical Phase Noise Performance



Figure 3. Typical Phase Noise Plot

Table 8. RMS Jitter by Band

| Jitter Band | Jitter, RMS |
|---------------------------------|-------------|
| SONET_OC48, 12 kHz to 20 MHz | 249 fs |
| SONET_OC192_A, 20 kHz to 80 MHz | 274 fs |
| SONET_OC192_B, 4 MHz to 80 MHz | 166 fs |
| SONET_OC192_C, 50 kHz to 80 MHz | 267 fs |
| Brick Wall_800 Hz to 80 MHz | 274 fs |

***Note:** Jitter integration bands include low-pass (-20 dB/Dec) and hi-pass (-60 dB/Dec) roll-offs per Teccordia GR-253-CORE.

3. Typical Application Circuits



Figure 4. Si5368 Typical Application Circuit (I²C Control Mode)

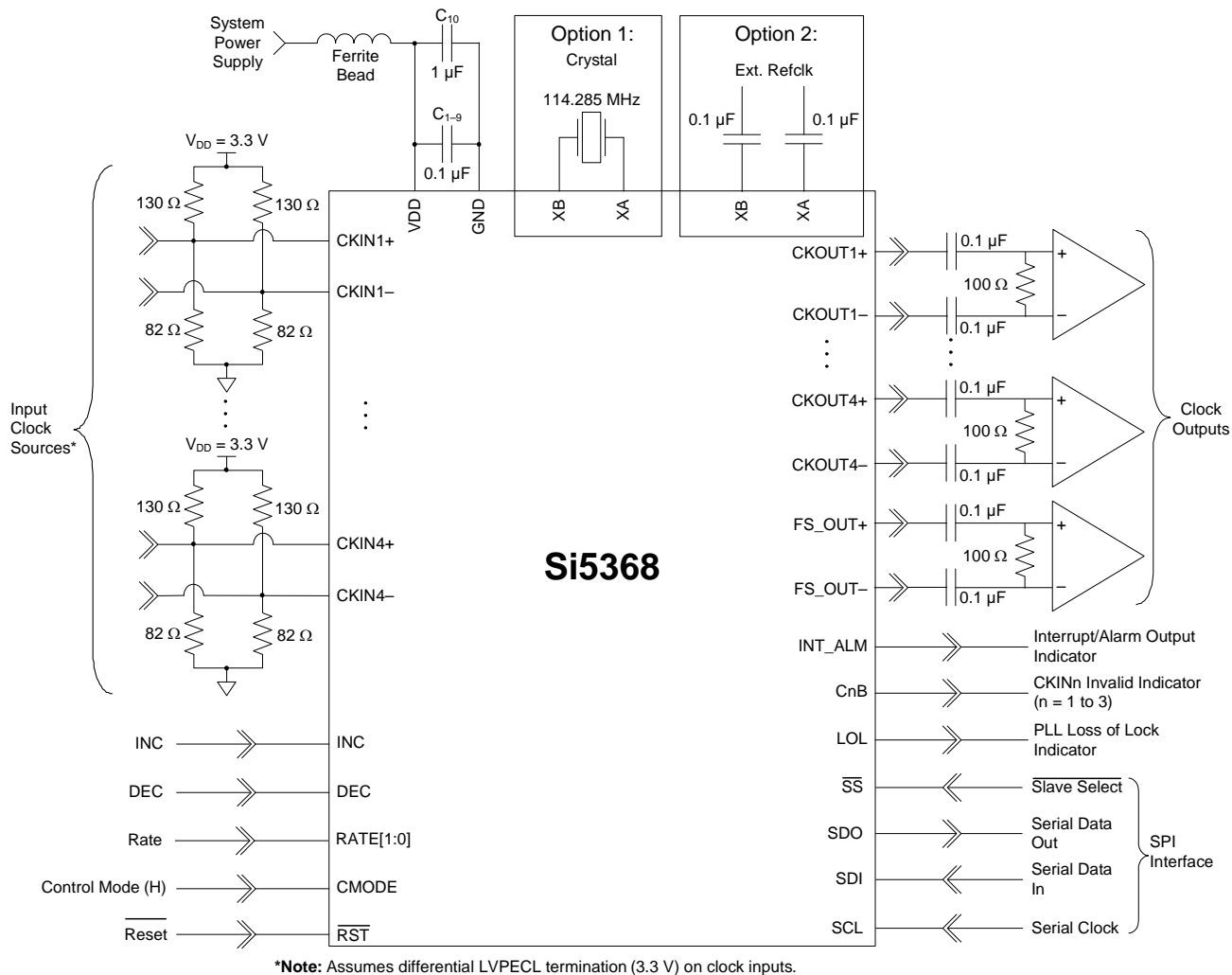


Figure 5. Si5368 Typical Application Circuit (SPI Control Mode)

4. Functional Description

The Si5368 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5368 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5368 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5368 input clock frequency and clock multiplication ratio are programmable through an I²C or SPI interface. Optionally, the fifth clock output can be configured as a 2 to 512 kHz SONET/SDH frame synchronization output that is phase aligned with one of the high-speed output clocks. Silicon Laboratories offers a PC-based software utility, *DSPLLsim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from <http://www.silabs.com/timing> (click on Documentation).

The Si5368 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5368 PLL loop bandwidth is digitally programmable and supports a range from 60 Hz to 8.4 kHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5368 supports hitless switching between input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps tp). Manual, automatic revertive and non-revertive input clock switching options are available. The Si5368 monitors the four input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on any of the four input clocks. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5368 monitors the frequency of CKIN1, CKIN2, CKIN3, and CKIN4 with respect to a selected reference frequency and generates a frequency offset alarm (FOS) if the threshold is exceeded. This FOS feature is available for SONET applications in which both the monitored frequency on CKIN1, CKIN3, and CKIN4 and the reference frequency are integer multiples of 19.44 MHz. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported.

The Si5368 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

Fine phase adjustment is available and is set using the FLAT register bits. The nominal range and resolution of the FLAT[14:0] latency adjustment word are: ± 110 ps and 3 ps, respectively.

The Si5368 has five differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the *DSPLLsim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

4.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to operate. Silicon Laboratories recommends using a high-quality crystal. Specific recommendations may be found in the Family Reference Manual. An external clock from a high-quality OCXO or TCXO can also be used as a reference for the device.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold, will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

4.2. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5368. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from <http://www.silabs.com/timing>; click on Documentation.

5. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|-------------------|-----------------|------------------|-----------------|-----------------|--------------------|-----------------|-----------|
| 0 | | FREE_RUN | CKOUT_ALWAYS_ON | | CK_CONFIG_REG | | BYPASS_REG | |
| 1 | CK_PRIOR4 [1:0] | | CK_PRIOR3 [1:0] | | CK_PRIOR2 [1:0] | | CK_PRIOR1 [1:0] | |
| 2 | BWSEL_REG [3:0] | | | | | | | |
| 3 | CKSEL_REG [1:0] | | DHOLD | SQ_ICAL | | | | |
| 4 | AUTOSEL_REG [1:0] | | | HIST_DEL [4:0] | | | | |
| 5 | ICMOS [1:0] | | SFOUT2_REG [2:0] | | | SFOUT1_REG [2:0] | | |
| 6 | | | SFOUT4_REG [2:0] | | | SFOUT3_REG [2:0] | | |
| 7 | | | SFOUT5_REG [2:0] | | | FOSREFSEL [2:0] | | |
| 8 | HLOG_4 [1:0] | | HLOG_3 [1:0] | | HLOG_2 [1:0] | | HLOG_1 [1:0] | |
| 9 | HIST_AVG [4:0] | | | | | | HLOG_5 [1:0] | |
| 10 | | | DSBL5_REG | | DSBL4_REG | DSBL3_REG | DSBL2_REG | DSBL1_REG |
| 11 | ALIGN_THR [2:0] | | | | PD_CK4 | PD_CK3 | PD_CK2 | PD_CK1 |
| 12 | FPW_VALID | FSYNC_ALIGN_REG | FSYNC_ALIGN_MODE | FSYNC_SWTCH_REG | FSKEW_VALID | FSYNC_SKEW [16:16] | FSYNC_PW [9:8] | |
| 13 | FSYNC_PW [7:0] | | | | | | | |
| 14 | FSYNC_SKEW [15:8] | | | | | | | |
| 15 | FSYNC_SKEW [7:0] | | | | | | | |
| 16 | CLAT [7:0] | | | | | | | |
| 17 | FLAT_VALID | FLAT [14:8] | | | | | | |
| 18 | FLAT [7:0] | | | | | | | |
| 19 | FOS_EN | FOS_THR [1:0] | | VALTIME [1:0] | | LOCKT [2:0] | | |
| 20 | | | ALRMOUT_PIN | CK3_BAD_PIN | CK2_BAD_PIN | CK1_BAD_PIN | LOL_PIN | INT_PIN |
| 21 | INCDEC_PIN | | FSYNC_ALIGN_PIN | CK4_ACTV_PIN | CK3_ACTV_PIN | CK2_ACTV_PIN | CK1_ACTV_PIN | CKSEL_PIN |
| 22 | FSYNC_ALIGN_POL | FSYNC_POL | | FSYNCOUT_POL | CK_ACTV_POL | CK_BAD_POL | LOL_POL | INT_POL |

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|---------------|----|-----------|----------|----------------|--------------|----------|----------|
| 23 | | | | LOS4_MSK | LOS3_MSK | LOS2_MSK | LOS1_MSK | LOSX_MSK |
| 24 | | | ALIGN_MSK | FOS4_MSK | FOS3_MSK | FOS2_MSK | FOS1_MSK | LOL_MSK |
| 25 | N1_HS [2:0] | | | | NC1_LS [19:16] | | | |
| 26 | NC1_LS [15:8] | | | | | | | |
| 27 | NC1_LS [7:0] | | | | | | | |
| 28 | | | | | NC2_LS [19:16] | | | |
| 29 | NC2_LS [15:8] | | | | | | | |
| 30 | NC2_LS [7:0] | | | | | | | |
| 31 | | | | | NC3_LS [19:16] | | | |
| 32 | NC3_LS [15:8] | | | | | | | |
| 33 | NC3_LS [7:0] | | | | | | | |
| 34 | | | | | NC4_LS [19:16] | | | |
| 35 | NC4_LS [15:8] | | | | | | | |
| 36 | NC4_LS [7:0] | | | | | | | |
| 37 | | | | | NC5_LS [19:16] | | | |
| 38 | NC5_LS [15:8] | | | | | | | |
| 39 | NC5_LS [7:0] | | | | | | | |
| 40 | N2_HS [2:0] | | | | N2_LS [19:16] | | | |
| 41 | N2_LS [15:8] | | | | | | | |
| 42 | N2_LS [7:0] | | | | | | | |
| 43 | | | | | | N31_ [18:16] | | |
| 44 | N31_ [15:8] | | | | | | | |
| 45 | N31_ [7:0] | | | | | | | |
| 46 | | | | | | N32_ [18:16] | | |
| 47 | N31_ [15:8] | | | | | | | |
| 48 | N32_ [7:0] | | | | | | | |
| 49 | | | | | | N33_ [18:16] | | |
| 50 | N33_ [15:8] | | | | | | | |
| 51 | N33_ [7:0] | | | | | | | |
| 52 | | | | | | N34_ [18:16] | | |
| 53 | N34_ [15:8] | | | | | | | |

Si5368

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|------------------------|---------------|------------------|---------------|----------------|-----------------|---------------|----------------|
| 54 | N34_[7:0] | | | | | | | |
| 55 | | | CLKIN2RATE_[2:0] | | | CLKIN1RATE[2:0] | | |
| 56 | | | CLKIN4RATE_[2:0] | | | CLKIN3RATE[2:0] | | |
| 128 | | | | | CK4_ACTV_REG | CK3_ACTV_REG | CK2_ACTV_REG | CK1_ACTV_REG |
| 129 | | | | LOS4_INT | LOS3_INT | LOS2_INT | LOS1_INT | LOSX_INT |
| 130 | CLAT-PROGRESS | DIGHOLD-VALID | ALIGN_INT | FOS4_INT | FOS3_INT | FOS2_INT | FOS1_INT | LOL_INT |
| 131 | | | | LOS4_FLG | LOS3_FLG | LOS2_FLG | LOS1_FLG | LOSX_FLG |
| 132 | | ALIGN_FLG | FOS4_FLG | FOS3_FLG | FOS2_FLG | FOS1_FLG | LOL_FLG | AIGN_ERR [8:8] |
| 133 | ALIGN_ERR [7:0] | | | | | | | |
| 134 | PARTNUM_RO [11:4] | | | | | | | |
| 135 | PARTNUM_RO [3:0] | | | | REVID_RO [3:0] | | | |
| 136 | RST_REG | ICAL | | | | | | |
| 138 | | | | | LOS4_EN [1:1] | LOS3_EN [1:1] | LOS2_EN [1:1] | LOS1_EN [1:1] |
| 139 | LOS4_EN [0:0] | LOS3_EN [0:0] | LOS2_EN [0:0] | LOS1_EN [0:0] | FOS4_EN | FOS3_EN | FOS2_EN | FOS1_EN |
| 140 | INDEPENDENTSKEW1 [7:0] | | | | | | | |
| 141 | INDEPENDENTSKEW2 [7:0] | | | | | | | |
| 142 | INDEPENDENTSKEW3 [7:0] | | | | | | | |
| 143 | INDEPENDENTSKEW4 [7:0] | | | | | | | |
| 144 | INDEPENDENTSKEW5 [7:0] | | | | | | | |

6. Register Descriptions

Register 0.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----------|-----------------|----|---------------|----|------------|----|
| Name | | FREE_RUN | CKOUT_ALWAYS_ON | | CK_CONFIG_REG | | BYPASS_REG | |
| Type | R | R/W | R/W | R | R/W | R | R/W | R |

Reset value = 0001 0100

| Bit | Name | Function |
|-----|-----------------|---|
| 7 | Reserved | |
| 6 | FREE_RUN | <p>Free Run. Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its external reference. 0: Disable Free Run 1: Enable</p> |
| 5 | CKOUT_ALWAYS_ON | <p>CKOUT Always On. This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off until the part is calibrated.</p> |
| 4 | Reserved | |
| 3 | CK_CONFIG_REG | <p>CK_CONFIG_REG. This bit controls the input clock configuration for either normal CLKIN function or FSYNC operation. Whenever CK_CONFIG_REG = 1, FSYNC_ALIGN_MODE must not be set to 1. 0: CKIN_1, 2, 3, 4 inputs do not have a synchronized relationship. CLKOUT5 is an independent output. There is no FSYNCOUT. 1: CKIN_1, 3 and CKIN_2, 4 Clock/FSYNC pairs. CKOUT5 is configured as the FSYNC output.</p> |
| 2 | Reserved | |
| 1 | BYPASS_REG | <p>Bypass Register. This bit enables or disables the PLL bypass mode. Use is only valid when the part is in digital hold or before the first ICAL. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL. Bypass mode does not support CMOS clock outputs.</p> |
| 0 | Reserved | |

Register 1.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|
| Name | CK_PRIOR4 [1:0] | | CK_PRIOR3 [1:0] | | CK_PRIOR2 [1:0] | | CK_PRIOR1 [1:0] | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 1110 0100

| Bit | Name | Function |
|-----|-----------------|--|
| 7:6 | CK_PRIOR4 [1:0] | Selects which of the input clocks will be 4th priority in the autoselection state machine. 00: CKIN1 is 4th priority 01: CKIN2 is 4th priority 10: CKIN3 is 4th priority 11: CKIN4 is 4th priority |
| 5:4 | CK_PRIOR3 [1:0] | Selects which of the input clocks will be 3rd priority in the autoselection state machine. 00: CKIN1 is 3rd priority 01: CKIN2 is 3rd priority 10: CKIN3 is 3rd priority 11: CKIN4 is 3rd priority |
| 3:2 | CK_PRIOR2 [1:0] | CK_PRIOR 2. Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority 01: CKIN2 is 2nd priority 10: CKIN3 is 2nd priority 11: CKIN4 is 2nd priority |
| 1:0 | CK_PRIOR1 [1:0] | CK_PRIOR 1. Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority 01: CKIN2 is 1st priority 10: CKIN3 is 1st priority 11: CKIN4 is 1st priority |

Register 2.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | BWSEL_REG [3:0] | | | | | | | |
| Type | R/W | | | | R | R | R | R |

Reset value = 0100 0010

| Bit | Name | Function |
|-----|-----------------|---|
| 7:4 | BWSEL_REG [3:0] | BWSEL_REG. Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect. |
| 3:0 | Reserved | |

Register 3.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------------|----|-------|---------|----|----|----|----|
| Name | CKSEL_REG [1:0] | | DHOLD | SQ_ICAL | | | | |
| Type | R/W | | R/W | R/W | R | R | R | R |

Reset value = 0000 0101

| Bit | Name | Function |
|-----|-----------------|--|
| 7:6 | CKSEL_REG [1:0] | <p>CKSEL_REG.</p> <p>If the device is operating in manual register-based clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1, the CKSEL[1:0] input pins continue to control clock selection and CKSEL_REG is of no consequence.</p> <p>00: CKIN_1 selected. 01: CKIN_2 selected. 10: CKIN_3 selected. 11: CKIN_4 selected.</p> |
| 5 | DHOLD | <p>DHOLD.</p> <p>Forces the part into digital hold. This bit overrides all other manual and automatic clock selection controls.</p> <p>0: Normal operation. 1: Force digital hold mode. Overrides all other settings and ignores the quality of all of the input clocks.</p> |
| 4 | SQ_ICAL | <p>SQ_ICAL.</p> <p>This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9.</p> <p>0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.</p> |
| 3:0 | Reserved | |

Register 4.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------------|----|----|----------------|----|----|----|----|
| Name | AUTOSEL_REG [1:0] | | | HIST_DEL [4:0] | | | | |
| Type | R/W | | R | R/W | | | | |

Reset value = 0001 0010

| Bit | Name | Function |
|-----|-------------------|--|
| 7:6 | AUTOSEL_REG [1:0] | AUTOSEL_REG [1:0]. Selects method of input clock selection to be used. 00: Manual (either register or pin controlled. See CKSEL_PIN). 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved |
| 5 | Reserved | |
| 4:0 | HIST_DEL [4:0] | HIST_DEL [4:0]. Selects amount of delay to be used in generating the history information MHIST, the value of M used during Digital Hold. |

Register 5.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|------------------|----|----|------------------|----|----|
| Name | ICMOS [1:0] | | SFOUT2_REG [2:0] | | | SFOUT1_REG [2:0] | | |
| Type | R/W | | R/W | | | R/W | | |

Reset value = 1110 1101

| Bit | Name | Function |
|-----|------------------|--|
| 7:6 | ICMOS [1:0] | <p>ICMOS [1:0]. When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT–.</p> <p>00: 8 mA/2 mA 01: 16 mA/4 mA 10: 24 mA/6 mA 11: 32 mA (3.3 V operation)/8 mA (1.8 V operation)</p> |
| 5:3 | SFOUT2_REG [2:0] | <p>SFOUT2_REG [2:0]. Controls output signal format and disable for CKOUT2 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p> |
| 2:0 | SFOUT1_REG [2:0] | <p>SFOUT1_REG [2:0]. Controls output signal format and disable for CKOUT1 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p> |

Register 6.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|------------------|----|----|------------------|----|----|
| Name | | | SFOUT4_REG [2:0] | | | SFOUT3_REG [2:0] | | |
| Type | R | R | R/W | | | R/W | | |

Reset value = 0010 1100

| Bit | Name | Function |
|-----|------------------|--|
| 7:6 | Reserved | |
| 5:3 | SFOUT4_REG [2:0] | <p>SFOUT4_REG [2:0]. Controls output signal format and disable for CKOUT4 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p> |
| 2:0 | SFOUT3_REG [2:0] | <p>SFOUT3_REG [2:0]. Controls output signal format and disable for CKOUT3 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p> |

Register 7.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|------------------|----|----|-----------------|----|----|
| Name | | | SFOUT5_REG [2:0] | | | FOSREFSEL [2:0] | | |
| Type | R | R | R/W | | | R/W | | |

Reset value = 0010 1010

| Bit | Name | Function |
|-----|------------------|--|
| 7:6 | Reserved. | Reserved. |
| 5:3 | SFOUT5_REG [2:0] | <p>SFOUT5_REG [2:0] Controls output signal format and disable for CKOUT5 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p> |
| 2:0 | FOSREFSEL [2:0] | <p>FOSREFSEL [2:0]. Selects which input clock is used as the reference frequency for Frequency Off-Set (FOS) alarms.</p> <p>000: XA/XB (External reference) 001: CKIN1 010: CKIN2 011: CKIN3 100: CKIN4 101: Reserved 110: Reserved 111: Reserved</p> |

Register 8.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|-------------|----|-------------|----|-------------|----|
| Name | HLOG_4[1:0] | | HLOG_3[1:0] | | HLOG_2[1:0] | | HLOG_1[1:0] | |
| Type | R/W | | R/W | | R/W | | R/W | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|--------------|---|
| 7:6 | HLOG_4 [1:0] | HLOG_4 [1:0]. 00: Normal operation 01: Holds CKOUT4 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT4 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved |
| 5:4 | HLOG_3 [1:0] | HLOG_3 [1:0]. 00: Normal operation 01: Holds CKOUT3 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT3 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved. |
| 3:2 | HLOG_2 [1:0] | HLOG_2 [1:0]. 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved. |
| 1:0 | HLOG_1 [1:0] | HLOG_1 [1:0]. 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved |

Register 9.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------------|----|----|----|----|----|--------------|----|
| Name | HIST_AVG [4:0] | | | | | | HLOG_5 [1:0] | |
| Type | R/W | | | | | R | R/W | |

Reset value = 1100 0000

| Bit | Name | Function |
|-----|----------------|--|
| 7:3 | HIST_AVG [4:0] | HIST_AVG [4:0]. Selects amount of averaging time to be used in generating MHIST, the value of M used during digital hold. See Family Reference Manual for settings. |
| 2 | Reserved | |
| 1:0 | HLOG_5 [1:0] | HLOG_5 [1:0]. 00: Normal Operation 01: Holds CKOUT5 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT5 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved |

Register 10.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|-----------|----|-----------|-----------|-----------|-----------|
| Name | | | DSBL5_REG | | DSBL4_REG | DSBL3_REG | DSBL2_REG | DSBL1_REG |
| Type | R | R | R/W | R | R/W | R/W | R | R |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-----------|---|
| 7:6 | Reserved | |
| 5 | DSBL5_REG | DSBL5_REG. This bit controls the powerdown and disable of the CKOUT5 output buffer. If disable mode is selected, the NC5_LS output divider is also powered down. 0: CKOUT5 enabled. 1: CKOUT5 disabled. |
| 4 | Reserved | |
| 3 | DSBL4_REG | DSBL4_REG. This bit controls the powerdown and disable of the CKOUT4 output buffer. If disable mode is selected, the NC4 output divider is also powered down. 0'b=CKOUT4 enabled 1'b=CKOUT4 disabled |
| 2 | DSBL3_REG | DSBL3_REG. This bit controls the powerdown and disable of the CKOUT3 output buffer. If disable mode is selected, the NC3 output divider is also powered down. 0: CKOUT3 enabled 1: CKOUT3 disabled |
| 1 | DSBL2_REG | DSBL2_REG. This bit controls the powerdown and disable of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled |
| 0 | DSBL1_REG | DSBL1_REG. This bit controls the powerdown and disable of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled |

Register 11.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------------|-----|-----|----|--------|--------|--------|--------|
| Name | ALIGN_THR [2:0] | | | | PD_CK4 | PD_CK3 | PD_CK2 | PD_CK1 |
| Type | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W |

Reset value = 0100 0000

| Bit | Name | Function |
|-----|-----------------|--|
| 7:5 | ALIGN_THR [2:0] | <p>ALIGN_THR [2:0]. These bits control the threshold for the alignment error alarm. Input to output sync phase skews that deviate more than the alignment threshold from the ideal value (set by FSYNC_SKEW[16:0]) in either the leading or lagging direction trigger the alignment alarm. Value is in units of Tclkout2.</p> <p>000: 4 001: 8 010: 16 011: 32 100: 48 101: 64 110: 96 111: 128</p> |
| 4 | Reserved | |
| 3 | PD_CK4 | <p>PD_CK4. This bit controls the powerdown of the CKIN4 input buffer. 0: CKIN4 enabled 1: CKIN4 disabled</p> |
| 2 | PD_CK3 | <p>PD_CK3. This bit controls the powerdown of the CKIN3 input buffer. 0: CKIN3 enabled 1: CKIN3 disabled</p> |
| 1 | PD_CK2 | <p>PD_CK2. This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled</p> |
| 0 | PD_CK1 | <p>PD_CK1. This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled</p> |

Register 12.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|-----------------|------------------|-----------------|-------------|--------------------|----------------|----|
| Name | FPW_VALID | FSYNC_ALIGN_REG | FSYNC_ALIGN_MODE | FSYNC_SWTCH_REG | FSKEW_VALID | FSYNC_SKEW [16:16] | FSYNC_PW [9:8] | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

Reset value = 1000 1000

| Bit | Name | Function |
|-----|------------------|--|
| 7 | FPW_VALID | <p>FPW_VALID.</p> <p>When in frame sync mode (CK_CONFIG_REG=1), before writing either a new FSYNC_PW[9:0] or NC5_LS [19:0] value, this bit must be set to zero. This causes the existing FSYNC_PW [9:0] or NC5_LS[19:0] value to be held by the internal state machine for use while the new values are written. Once the new FSYNC_PW [9:0] or NC5_LS [19:0] values are completely written, set FPW_VALID = 1 to enable their use.</p> <p>0: Memorize existing FSYNC_PW[9:0] and NC5_LS [19:0] values and ignore intermediate register values during write of new FSYNC_PW [9:0] and NC5_LS [19:0] values.</p> <p>1: Use FSYNC_PW[9:0] value directly from registers</p> |
| 6 | FSYNC_ALIGN_REG | <p>FSYNC_ALIGN_REG.</p> <p>If FSYNC_ALIGN_PIN=0, this bit controls realignment of FSYNCOUT to the active sync input (CKIN_3 or CKIN_4). If FSYNC_ALIGN_PIN=1, the FSYNC_ALIGN pin controls this function.</p> <p>0: No realignment</p> <p>1: Active</p> |
| 5 | FSYNC_ALIGN_MODE | <p>FSYNC_ALIGN_MODE.</p> <p>This bit must be set to 1 when in frame sync mode (when CK_CONFIG_REG = 1).</p> |
| 4 | FSYNC_SWTCH_REG | <p>FSYNC_SWTCH_REG.</p> <p>Enables or disables the use of the CKIN3 and CKIN4 loss-of-signal indicators as inputs to the automatic clock selection state machine for the clock configuration mode supporting frame sync switching (CK_CONFIG=1 or CK_CONFIG_REG=1).</p> <p>0: CKIN3 and CKIN4 status not used in clock selection</p> <p>1: CKIN3 and CKIN4 status used in clock selection</p> |
| 3 | FSKEW_VALID | <p>FSKEW_VALID.</p> <p>Before writing a new FSYNC_SKEW[16:0] value, this bit must be set to zero, which causes the existing FSYNC_SKEW[16:0] value to be held internally by the skew alignment state machine for use while the new value is being written. Once the new FSYNC_SKEW[16:0] is completely written, set FSKEW_VALID=1 to enable its use.</p> <p>0: Memorize existing FSYNC_SKEW[16:0] value and ignore intermediate register values during write of new FSYNC_SKEW value.</p> <p>1: Use FSYNC_SKEW[[16:0] value directly from registers.</p> |

| Bit | Name | Function |
|-----|-------------------|--|
| 2 | FSYNC_SKEW [16:0] | FSYNC_SKEW [16:0]. Phase skew control for FSYNCOUT. The resolution of the skew control is 1/fCKOUT2. Entered values should be less than the FSYNCOUT period. 0 0000 0000 0000 0000=Zero phase skew. 0 0000 0000 0000 0001=Delay of 1 period of CLKOUT_2. 1 0010 1111 1011 1111=Delay of 77,759 periods of CKOUT2. If CKOUT2=622.08 MHz and FSYNCOUT=8 kHz, this delay equals 125 ms - 1/fCKOUT2 and is the maximum value that should be entered. 1 1111 1111 1111 1111=Delay of 131,071 periods of CKOUT2. |
| 1:0 | FSYNC_PW [9:0] | FSYNC_PW [9:0]. These bits control the pulse width of the FSYNCOUT signal. The resolution of the pulse width control is 1/fCKOUT2. 0000000000=50% duty cycle. 0000000001=1 period of CKOUT2. 0000000010=2 periods of CKOUT2. 1111111111=1023 periods of CKOUT2. |

Register 13.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | FSYNC_PW [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0001

| Bit | Name | Function |
|-----|----------------|--|
| 7:0 | FSYNC_PW [7:0] | FSYNC_PW [7:0]. See Register 12. |

Register 14.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | FSYNC_SKEW [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-------------------|---|
| 7:0 | FSYNC_SKEW [15:8] | FSYNC_SKEW [15:8]. See Register 12. |

Register 15.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------|----|----|----|----|----|----|----|
| Name | FSYNC_SKEW [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------------|--|
| 7:0 | FSYNC_SKEW [7:0] | FSYNC_SKEW [7:0]. See Register 12. |

Register 16.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| Name | CLAT [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | CLAT [7:0] | CLAT [7:0]. With INCDEC_PIN=0, this register sets the phase delay for CKOUT_n in units of N1_HS/Fosc. Note: This can take as long as 20 seconds. 01111111: +127 x 1/fOSC (2s compliment) 00000000: 0 1000000: -128 x 1/fOSC (2s compliment) If N2-HS[2:0] = 000, CLAT does not work. |

Register 17.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| Name | FLAT_VALID | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 1000 0000

| Bit | Name | Function |
|-----|-------------|--|
| 7 | FLAT_VAILD | <p>FLAT_VAILD.</p> <p>Before writing a new FLAT[14:0] value, this bit must be set to zero, which causes the existing FLAT[14:0] value to be held internally for use while the new value is being written. Once the new FLAT[14:0] value is completely written, set FLAT_VALID = 1 to enable its use.</p> <p>0: Memorize existing FLAT[14:0] value and ignore intermediate register values during write of new FLAT[14:0] value.</p> <p>1: Use FLAT[14:0] value directly from registers.</p> |
| 6:0 | FLAT [14:0] | <p>FLAT [14:0].</p> <p>Fine resolution control for overall device latency from input clocks to output clocks. Positive values increase the skew. See DSPLLsim for details.</p> |

Register 18.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| Name | FLAT [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|---|
| 7:0 | FLAT [7:0] | <p>FLAT [7:0].</p> <p>See Register 17.</p> |

Register 19.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------|---------------|----|---------------|----|-------------|----|----|
| Name | FOS_EN | FOS_THR [1:0] | | VALTIME [1:0] | | LOCKT [2:0] | | |
| Type | R/W | R/W | | R/W | | R/W | | |

Reset value = 0010 1100

| Bit | Name | Function |
|-----|---------------|--|
| 7 | FOS_EN | FOS_EN. Frequency offset enable globally disables FOS. See the individual FOS enables (FOSx_EN, register 139). 00: FOS disable 01: FOS enabled by FOSx_EN |
| 6:5 | FOS_THR [1:0] | FOS_THR [1:0]. Frequency Offset at which FOS is declared: 00: ± 11 to 12 ppm Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK. 01: ± 48 to 49 ppm (SMC). 10: ± 30 ppm SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK. 11: ± 200 ppm |
| 4:3 | VALTIME [1:0] | VALTIME [1:0]. Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 seconds |
| 2:0 | LOCKT [2:0] | LOCKT [2:0]. Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. Refer to the Family Reference Manual for more details. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: 833 us |

Register 20.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|-------------|-------------|-------------|-------------|---------|---------|
| Name | | | ALRMOUT_PIN | CK3_BAD_PIN | CK2_BAD_PIN | CK1_BAD_PIN | LOL_PIN | INT_PIN |
| Type | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 0011 1100

| Bit | Name | Function |
|-----|-------------|---|
| 7:6 | Reserved | |
| 5 | ALRMOUT_PIN | <p>ALRMOUT_PIN. The ALRMOUT status can be reflected on the ALRMOUT output pin. The request to reflect the interrupt status on this pin (INT_PIN=1) overrides the ALRMOUT_PIN request. 0: ALRMOUT not reflected on output pin. Output pin disabled if INT_PIN=0. 1: ALRMOUT reflected to output pin if INT_PIN=0. If INT_PIN=1, interrupt status appears on the output pin and ALRMOUT is not available on an output pin.</p> |
| 4 | CK3_BAD_PIN | <p>CK3_BAD_PIN. The CK3_BAD status can be reflected on the C3B output pin. 0: C3B output pin tristated 1: C3B status reflected to output pin</p> |
| 3 | CK2_BAD_PIN | <p>CK2_BAD_PIN. The CK2_BAD status can be reflected on the C2B output pin. 0: C2B output pin tristated 1: C2B status reflected to output pin</p> |
| 2 | CK1_BAD_PIN | <p>CK1_BAD_PIN. The CK1_BAD status can be reflected on the C1B output pin. 0: C1B output pin tristated 1: C1B status reflected to output pin</p> |
| 1 | LOL_PIN | <p>LOL_PIN. The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin</p> |
| 0 | INT_PIN | <p>INT_PIN. Reflects the interrupt status on the INT output pin. 0: Interrupt status not displayed on INT output pin. If ALRMOUT_PIN = 0, output pin is tristated. 1: Interrupt status reflected to output pin. ALRMOUT_PIN ignored.</p> |

Register 21.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|---------|-----------------|--------------|--------------|--------------|--------------|-----------|
| Name | INCDEC_PIN | | FSYNC_ALIGN_PIN | CK4_ACTV_PIN | CK3_ACTV_PIN | CK2_ACTV_PIN | CK1_ACTV_PIN | CKSEL_PIN |
| Type | R/W | Force 1 | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 1111 1111

| Bit | Name | Function |
|-----|-----------------|---|
| 7 | INCDEC_PIN | INCDEC_PIN. Determines how coarse skew adjustments can be made. The adjustments can be made via hardware using the INC/DEC pins or with software via the CLAT register. 0: INC and DEC inputs ignored; use CLAT register to adjust skew. 1: INC and DEC inputs control output phase increment/decrement. |
| 6 | Reserved | |
| 5 | FSYNC_ALIGN_PIN | FSYNC_ALIGN_PIN. Realignment of FSYNCOOUT can be controlled by the FSYNC_ALIGN input pin instead of the FSYNC_ALIGN_REG register bit. 0: FSYNC_ALIGN pin ignored. FSYNC_ALIGN_REG register bit controls FSYNCOOUT realignment. 1: FSYNC_ALIGN pin controls FSYNCOOUT realignment. |
| 4 | CK4_ACTV_PIN | CK4_ACTV_PIN. If the CKSEL[1]/CK4_ACTV pin is functioning as the CK4_ACTV output (see CKSEL[1]/CK4_ACTV pin description on CK4_ACTV), the CK4_ACTV_REG status bit can be reflected to the CK4_ACTV output pin using the CK4_ACTV_PIN enable function. 0: CK4_ACTV output pin tristated 1: CK4_ACTV status reflected to output pin. |
| 3 | CK3_ACTV_PIN | CK3_ACTV_PIN. If the CKSEL[0]/CK3_ACTV pin is functioning as the CK3_ACTV output (see CKSEL[0]/CK3_ACTV pin description on CK3_ACTV), the CK3_ACTV_REG status bit can be reflected to the CK3_ACTV output pin using the CK3_ACTV_PIN enable function. 0: CK3_ACTV output pin tristated. 1: CK3_ACTV status reflected to output pin. |
| 2 | CK2_ACTV_PIN | CK2_ACTV_PIN. The CK2_ACTV_REG status bit can be reflected to the CK2_ACTV output pin using the CK2_ACTV_PIN enable function. 0: CK2_ACTV output pin tristated. 1: CK2_ACTV status reflected to output pin. |

Si5368

| Bit | Name | Function |
|-----|--------------|--|
| 1 | CK1_ACTV_PIN | CK1_ACTV_PIN. The CK1_ACTV_REG status bit can be reflected to the CK1_ACTV output pin using the CK1_ACTV_PIN enable function. 0: CK1_ACTV output pin tristated. 1: CK1_ACTV status reflected to output pin. |
| 0 | CKSEL_PIN | CKSEL_PIN. If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CKSEL[1:0] input pins. 0: CKSEL pins ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CKSEL[1:0] input pins controls clock selection. |

Note: The CKx_ACTV_PIN bits in this register are of consequence only when CKSEL_PIN is 0.

Register 22.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------------|-----------|----|--------------|-------------|------------|---------|---------|
| Name | FSYNC_ALIGN_POL | FSYNC_POL | | FSYNCOUT_POL | CK_ACTV_POL | CK_BAD_POL | LOL_POL | INT_POL |
| Type | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |

Reset value = 1101 1111

| Bit | Name | Function |
|-----|-----------------|---|
| 7 | FSYNC_ALIGN_POL | FSYNC_ALIGN_POL. Sets the active polarity or edge for the FSYNC_ALIGN input pin. 0: Active low (falling edge). 1: Active high (rising edge). |
| 6 | FSYNC_POL | FSYNC_POL. Sets the active polarity and edge for the CKIN_3 and CKIN_4 inputs when used as frame sync inputs. 0: Active low (falling edge). 1: Active high (rising edge). |
| 5 | Reserved | |
| 4 | FSYNCOUT_POL | FSYNCOUT_POL. Controls active polarity of FSYNCOUT. 0: Active low 1: Active high |

| Bit | Name | Function |
|-----|-------------|--|
| 3 | CK_ACTV_POL | CK_ACTV_POL. Sets the active polarity for the CK1_ACTV, CK2_ACTV, CK3_ACTV, and CK4_ACTV signals when reflected on an output pin. 0: Active low 1: Active high |
| 2 | CK_BAD_POL | CK_BAD_POL. Sets the active polarity for the C1B, C2B, C3B, and ALRMOUT signals when reflected on output pins. 0: Active low 1: Active high |
| 1 | LOL_POL | LOL_POL. Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high |
| 0 | INT_POL | INT_POL. Sets the active polarity for the interrupt status when reflected on the INT_ALM output pin. 0: Active low 1: Active high |

Register 23.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|----|-----------|-----------|-----------|-----------|-----------|
| Name | | | | LOS4_MSKE | LOS3_MSKE | LOS2_MSKE | LOS1_MSKE | LOSX_MSKE |
| Type | R | R | R | R/W | R/W | R/W | R/W | R/W |

Reset value = 0001 1111

| Bit | Name | Function |
|-----|-----------|--|
| 7:5 | Reserved | |
| 4 | LOS4_MSKE | LOS4_MSKE. Determines if a LOS on CKIN4 (LOS4_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS4_FLG register. 0: LOS4 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS4_FLG ignored in generating interrupt output. |
| 3 | LOS3_MSKE | LOS3_MSKE. Determines if a LOS on CKIN3 (LOS3_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS3_FLG register. 0: LOS3 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS3_FLG ignored in generating interrupt output. |

| | | |
|---|----------|---|
| 2 | LOS2_MSK | <p>LOS2_MSK. Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.</p> |
| 1 | LOS1_MSK | <p>LOS1_MSK. Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.</p> |
| 0 | LOSX_MSK | <p>LOSX_MSK. Determines if a LOS on XA/XB(LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.</p> |

Register 24.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|-----------|----------|----------|----------|----------|---------|
| Name | | | ALIGN_MSK | FOS4_MSK | FOS3_MSK | FOS2_MSK | FOS1_MSK | LOL_MSK |
| Type | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 0011 1111

| Bit | Name | Function |
|-----|-----------|--|
| 7:6 | Reserved | |
| 5 | ALIGN_MSK | <p>ALIGN_MSK. Determines if an alignment alarm (ALIGN_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the ALIGN_FLG register. 0: FSYNC alignment alarm triggers active interrupt on INT output (if INT_PIN=1). 1: ALIGN_FLG ignored in generating interrupt output.</p> |
| 4 | FOS4_MSK | <p>FOS4_MSK. Determines if the FOS4_FLG is used to in the generation of an interrupt. Writes to this register do not change the value held in the FOS4_FLG register. 0: FOS4 alarm triggers active interrupt on INToutput (if INT_PIN=1). 1: FOS4_FLG ignored in generating interrupt output.</p> |
| 3 | FOS3_MSK | <p>FOS3_MSK. Determines if the FOS3_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS3_FLG register. 0: FOS3 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: FOS3_FLG ignored in generating interrupt output.</p> |

| | | |
|---|----------|---|
| 2 | FOS2_MSK | <p>FOS2_MSK.</p> <p>Determines if the FOS2_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register.</p> <p>0: FOS2 alarm triggers active interrupt on INT output (if INT_PIN=1).</p> <p>1: FOS2_FLG ignored in generating interrupt output.</p> |
| 1 | FOS1_MSK | <p>FOS1_MSK.</p> <p>Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register.</p> <p>0: FOS1 alarm triggers active interrupt on INT output (if INT_PIN=1).</p> <p>1: FOS1_FLG ignored in generating interrupt output.</p> |
| 0 | LOL_MSK | <p>LOL_MSK.</p> <p>Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register.</p> <p>0: LOL alarm triggers active interrupt on INT output (if INT_PIN=1).</p> <p>1: LOL_FLG ignored in generating interrupt output.</p> |

Register 25.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----------------|----|----|----|
| Name | N1_HS [2:0] | | | | NC1_LS [19:16] | | | |
| Type | R/W | | | R | R/W | | | |

Reset value = 0010 0000

| Bit | Name | Function |
|-----|----------------|--|
| 7:5 | N1_HS [2:0] | <p>N1_HS [2:0].</p> <p>Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 4) low-speed divider.</p> <p>000: N1 = 4 Note: Changing the coarse skew via the INC pin is disabled for this value.</p> <p>001: N1 = 5</p> <p>010: N1 = 6</p> <p>011: N1 = 7</p> <p>100: N1 = 8</p> <p>101: N1 = 9</p> <p>110: N1 = 10</p> <p>111: N1 = 11</p> |
| 4 | Reserved | |
| 3:0 | NC1_LS [19:16] | <p>NC1_LS [19:0].</p> <p>Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd.</p> <p>00000000000000000000 = 1</p> <p>00000000000000000001 = 2</p> <p>00000000000000000011 = 4</p> <p>00000000000000000101 = 6</p> <p>...</p> <p>11111111111111111111 = 2^{20}</p> <p>Valid divider values = [1, 2, 4, 6, ..., 2^{20}].</p> |

Register 26.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | NC1_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:0 | NC1_LS [15:8] | NC1_LS [15:8]. See Register 25. |

Register 27.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | NC1_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0011 0001

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | NC1_LS [7:0] | NC1_LS [7:0]. See Register 25. |

Register 28.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----------------|----|----|----|
| Name | | | | | NC2_LS [19:16] | | | |
| Type | R | R | R | R | R/W | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:4 | Reserved | |
| 3:0 | NC1_LS [19:0] | <p>NC2_LS [19:16]. Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd.</p> <p>00000000000000000000=1 00000000000000000001=2 00000000000000000011=4 00000000000000000101=6 ... 11111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}]</p> |

Register 29.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | NC2_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:0 | NC2_LS [15:8] | NC2_LS [15:8]. See Register 28. |

Register 30.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | NC2_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0011 0001

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | NC2_LS [7:0] | NC2_LS [7:0]. See Register 28. |

Register 31.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|----|----|----------------|----|----|----|
| Name | | | | | NC3_LS [19:16] | | | |
| Type | R | R | R | R | R/W | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|--|
| 7:4 | Reserved | |
| 3:0 | NC3_LS [19:0] | <p>NC3_LS [19:0]. Sets value for NC3 low-speed divider, which drives CKOUT3 output. Must be 0 or odd. 00000000000000000000=1 00000000000000000001=2 00000000000000000011=4 00000000000000000101=6 ... 11111111111111111111=2²⁰ Valid divider values=[1, 2, 4, 6, ..., 2²⁰].</p> |

Register 32.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------------|----|----|----|----|----|----|----|
| Name | NC3_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|--|
| 7:0 | NC3_LS [15:8] | <p>NC3_LS [15:8]. See Register 31.</p> |

Register 33.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|----|----|----|----|----|----|----|
| Name | NC3_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0011 0001

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | NC3_LS [7:0] | NC3_LS [7:0]. See Register 31. |

Register 34.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------------|----|----|----|-----|----|----|----|
| Name | NC4_LS [19:16] | | | | | | | |
| Type | R | R | R | R | R/W | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:4 | Reserved | |
| 3:0 | NC4_LS [19:0] | <p>NC4_LS [19:0]. Sets value for NC4 low-speed divider, which drives CKOUT4 output. Must be 0 or odd.</p> <p>00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6, ..., 2^{20}].</p> |

Register 35.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------------|----|----|----|----|----|----|----|
| Name | NC4_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:0 | NC4_LS [15:8] | NC4_LS [15:8]. See Register 34. |

Register 36.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|----|----|----|----|----|----|----|
| Name | NC4_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0011 0001

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | NC4_LS [7:0] | NC4_LS [7:0]. See Register 34. |

Register 37.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|----|-----|----|----|----|
| Name | NC5_LS [19:16] | | | | | | | |
| Type | R | R | R | R | R/W | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:4 | Reserved | |
| 3:0 | NC5_LS [19:0] | <p>NC5_LS [19:0]. Sets value for NC5 low-speed divider, which drives CKOUT5 output. Must be 0 or odd. When CK_CONFIG = 0: 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2²⁰</p> <p>Valid divider values=[1, 2, 4, 6, ..., 2²⁰]. When CK_CONFIG=1, maximum value limited to 2¹⁹.: 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 01111111111111111111 = 2¹⁹ Valid divider values = [1, 2, 4, 6, ..., 2¹⁹].</p> |

Register 38.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | NC5_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|---------------|--|
| 7:0 | NC5_LS [15:8] | <p>NC5_LS [15:8]. See Register 37.</p> |

Register 39.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|----|----|----|----|----|----|----|
| Name | NC5_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0011 0001

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | NC5_LS [7:0] | NC5_LS [7:0]. See Register 37. |

Register 40.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|---------------|----|----|----|
| Name | N2_HS [2:0] | | | | N2_LS [19:16] | | | |
| Type | R/W | | | R | R/W | | | |

Reset value = 1100 0000

| Bit | Name | Function |
|-----|---------------|---|
| 7:5 | N2_HS [2:0] | N2_HS [2:0]. Sets value for N2 high speed divider which drives NCn_LS (n = 1 to 4) low-speed divider. 000:4 001:5 010:6 011:7 100:8 101:9 110:10 111:11. |
| 4 | Reserved | |
| 3:0 | N2_LS [19:16] | NC2_LS [19:0]. Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^{20} Valid divider values = [2, 4, 6, ..., 2^{20}]. |

Register 41.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | N2_LS [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|--------------|--|
| 7:0 | N2_LS [15:8] | N2_LS [15:8]. See Register 40. |

Register 42.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | N2_LS [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 1111 1001

| Bit | Name | Function |
|-----|-------------|---|
| 7:0 | N2_LS [7:0] | N2_LS [7:0]. See Register 40. |

Register 43.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|----|----|----|-------------|----|----|
| Name | | | | | | N31 [18:16] | | |
| Type | R | R | R | R | R | R/W | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:3 | Reserved | |
| 2:0 | N31 [18:0] | N31 [18:0]. Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]. |

Register 44.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| Name | N31 [15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | N31 [15:8] | N31 [15:8]. See Register 43. |

Register 45.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | N31 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 1001

| Bit | Name | Function |
|-----|-----------|---------------------------------------|
| 7:0 | N31 [7:0] | N31 [7:0]. See Register 43. |

Register 46.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|-------------|----|----|
| Name | | | | | | N32_[18:16] | | |
| Type | R | R | R | R | R | R/W | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:3 | Reserved | |
| 2:0 | N32_[18:0] | N32_[18:0]. Sets value for input divider for CKIN2. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2 ¹⁹ Valid divider values=[1, 2, 3, ..., 2 ¹⁹]. |

Register 47.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| Name | N32_[15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | N32_[15:8] | N32_[15:8]. See Register 46. |

Register 48.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| Name | N32_[7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 1001

| Bit | Name | Function |
|-----|-----------|---------------------------------------|
| 7:0 | N32_[7:0] | N32_[7:0]. See Register 46. |

Register 49.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|-----|----|----|
| Name | N33_[18:0] | | | | | | | |
| Type | R | R | R | R | R | R/W | | |

Reset value = 0000 0000

| Bit | Name | Function |
|------|------------|--|
| 18:0 | N33_[18:0] | N33_[18:0]. Sets value for input divider for CKIN3. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = 2 ¹⁹ Valid divider values = [1, 2, 3, ..., 2 ¹⁹]. |

Register 50.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | N33_[15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | N33_[15:8] | N33_[15:8]. See Register 49. |

Register 51.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----|----|----|----|----|----|----|
| Name | N33_[7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 1001

| Bit | Name | Function |
|-----|-----------|---------------------------------------|
| 7:0 | N33_[7:0] | N33_[7:0]. See Register 49. |

Register 52.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|----|----|----|----|-------------|----|
| Name | | | | | | | N34_[18:16] | |
| Type | R | R | R | R | R | | R/W | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | N34_[18:0] | N34_[18:0]. Sets value for input divider for CKIN4. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = 2^{19} Valid divider values = [1, 2, 3, ..., 2^{19}]. |

Register 53.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | N34_[15:8] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------|--|
| 7:0 | N34_[15:8] | N34_[15:8]. See Register 52. |

Register 54.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | N34_[7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 1001

| Bit | Name | Function |
|-----|------------|---------------------------------------|
| 7:0 | N34_[15:8] | N34_[7:0]. See Register 52. |

Register 55.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|------------------|----|----|-----------------|----|----|
| Name | | | CLKIN2RATE_[2:0] | | | CLKIN1RATE[2:0] | | |
| Type | R | R | R/W | | | R/W | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------------|--|
| 7:6 | Reserved | |
| 5:3 | CLKIN2RATE[2:0] | CLKIN2RATE[2:0]. CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved |
| 2:0 | CLKIN1RATE [2:0] | CLKIN1RATE[2:0]. CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved |

Register 56.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----|------------------|----|----|-----------------|----|----|
| Name | | | CLKIN4RATE_[2:0] | | | CLKIN3RATE[2:0] | | |
| Type | R | R | R/W | | | R/W | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------------------|--|
| 7:6 | Reserved | |
| 5:3 | CLKIN4RATE[2:0] | CLKIN4RATE[2:0]. CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved |
| 2:0 | CLKIN3RATE [2:0] | CLKIN3RATE[2:0]. CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved |

Register 128.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|--------------|--------------|--------------|--------------|
| Name | | | | | CK4_ACTV_REG | CK3_ACTV_REG | CK2_ACTV_REG | CK1_ACTV_REG |
| Type | R | R | R | R | R | R | R | R |

Reset value = 0010 0000

| Bit | Name | Function |
|-----|--------------|--|
| 7:4 | Reserved | |
| 3 | CK4_ACTV_REG | CK4_ACTV_REG. Indicates if CKIN4 is currently the active clock for the PLL input. 0: CKIN4 is not the active input clock. Either it is not selected or LOS4_INT is 1. 1: CKIN_4 is the active input clock. |
| 2 | CK3_ACTV_REG | CK3_ACTV_REG. Indicates if CKIN3 is currently the active clock for the PLL input. 0: CKIN3 is not the active input clock - either it is not selected or LOS3_INT is 1. 1: CKIN3 is the active input clock. |
| 1 | CK2_ACTV_REG | CK2_ACTV_REG. Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock. |
| 0 | CK1_ACTV_REG | CK1_ACTV_REG. Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock. |

Register 129.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----------|----------|----------|----------|----------|
| Name | | | | LOS4_INT | LOS3_INT | LOS2_INT | LOS1_INT | LOSX_INT |
| Type | R | R | R | R | R | R | R | R |

Reset value = 0001 1110

| Bit | Name | Function |
|-----|----------|---|
| 7:5 | Reserved | |
| 4 | LOS4_INT | LOS4_INT. Indicates the LOS status on CKIN4. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN4 input. |
| 3 | LOS3_INT | LOS3_INT. Indicates the LOS status on CKIN3. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN3 input. |
| 2 | LOS2_INT | LOS2_INT. Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input. |
| 1 | LOS1_INT | LOS1_INT. Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input. |
| 0 | LOSX_INT | LOSX_INT. Indicates the LOS status of the external reference on the XA/XB pins. 0: Normal operation. 1: Internal loss-of-signal alarm on XA/XB reference clock input. |

Register 130.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------------|-------------------|---------------|----------|----------|----------|----------|---------|
| Name | CLAT- PROGRESS | DIGHOLD- VALID | ALIGN_ INT | FOS4_INT | FOS3_INT | FOS2_INT | FOS1_INT | LOL_INT |
| Type | R | R | R | R | R | R | R | R |

Reset value = 0000 0001

| Bit | Name | Function |
|-----|--------------|---|
| 7 | CLATPROGRESS | CLAT Progress. Indicates if the last change in the CLAT register has been processed. 0: Coarse skew adjustment not in progress. 1: Coarse skew adjustment in progress. |
| 6 | DIGHOLDVALID | Digital Hold Valid. Indicates if the digital hold circuit has enough samples of a valid clock to meet digital hold specifications. 0: Indicates digital filter has not been filled. The digital hold output frequency (from the filter) is not valid. 1: Indicates digital hold filter has been filled. The digital hold output frequency is valid. |
| 5 | ALIGN_INT | ALIGN_INT. Alignment Alarm Status. 0: Normal operation. 1: Alignment alarm between input and output frame sync signals. |
| 4 | FOS4_INT | FOS4_INT. CKIN4 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN4 input. |
| 3 | FOS3_INT | FOS3_INT. CKIN3 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN3 input. |
| 2 | FOS2_INT | FOS2_INT. CKIN2 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input. |
| 1 | FOS1_INT | FOS1_INT. CKIN1 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input. |
| 0 | LOL_INT | LOL_INT. PLL Loss of Lock Status. 0: PLL locked. 1: PLL unlocked. |

Register 131.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----------|----------|----------|----------|----------|
| Name | | | | LOS4_FLG | LOS3_FLG | LOS2_FLG | LOS1_FLG | LOSX_FLG |
| Type | R | R | R | R/W | R/W | R/W | R/W | R/W |

Reset value = 0001 1111

| Bit | Name | Function |
|-----|----------|---|
| 7:5 | Reserved | |
| 4 | LOS4_FLG | <p>LOS4_FLG. CKIN4 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS4_MSK bit. Flag cleared by writing location to 0.</p> |
| 3 | LOS3_FLG | <p>LOS3_FLG. CKIN3 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS3_MSK bit. Flag cleared by writing location to 0.</p> |
| 2 | LOS2_FLG | <p>LOS2_FLG. CKIN2 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS2_MSK bit. Flag cleared by writing location to 0.</p> |
| 1 | LOS1_FLG | <p>LOS1_FLG. CKIN1 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS1_MSK bit. Flag cleared by writing location to 0.</p> |
| 0 | LOSX_FLG | <p>LOSX_FLG. External reference (signal on pins XA/XB) Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOSX_MSK bit. Flag cleared by writing location to 0.</p> |

Register 132.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|-----------|----------|----------|----------|----------|---------|-----------------|
| Name | | ALIGN_FLG | FOS4_FLG | FOS3_FLG | FOS2_FLG | FOS1_FLG | LOL_FLG | ALIGN_ERR [8,8] |
| Type | R | R/W | R/W | R/W | R/W | R/W | R/W | R |

Reset value = 0000 0010

| Bit | Name | Function |
|-----|-----------|---|
| 7 | Reserved | |
| 6 | ALIGN_FLG | ALIGN_FLG. Alignment Alarm Flag. 0: Normal operation. 1: Held version of ALIGN_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by ALIGN_MSK bit. Flag cleared by writing location to 0. |
| 5 | FOS4_FLG | FOS4_FLG. CLKIN_4 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS4_MSK bit. Flag cleared by writing location to 0. |
| 4 | FOS3_FLG | FOS3_FLG. CLKIN_3 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS3_MSK bit. Flag cleared by writing location to 0. |
| 3 | FOS2_FLG | FOS2_FLG. CLKIN_2 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing location to 0. |

| Bit | Name | Function |
|-----|-----------------|---|
| 2 | FOS1_FLG | FOS1_FLG. CLKIN_1 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing location to 0. |
| 1 | LOL_FLG | LOL_FLG. PLL Loss of Lock Flag. 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing location to 0. |
| 0 | ALIGN_ERR [8,8] | ALIGN_ERR [8:0]. Indicates the magnitude of the deviation of the input to output frame sync phase alignment from the ideal value set in the FSYNC_SKEW[16:0] registers. The alignment error is given in units of tCKOUT_2. If the alignment error exceeds 255 fCKOUT_2 clock cycles, ALIGN_ERR[7:0] limits to its maximum value (11111111). The polarity of the phase deviation (leading or lagging) is given by the ALIGN_ERR[8] bit. 00000000=0 11111111=255 |

Register 133.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | ALIGN_ERR [7:0] | | | | | | | |
| Type | R | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-----------------|--|
| 7:0 | ALIGN_ERR [7:0] | ALIGN_ERR [7:0]. See Register 132. |

Register 134.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------------|----|----|----|----|----|----|----|
| Name | PARTNUM_RO [11:4] | | | | | | | |
| Type | R | | | | | | | |

Reset value = 0000 0100

| Bit | Name | Function |
|-----|-------------------|--|
| 7:0 | PARTNUM_RO [11:4] | PARTNUM_RO [11:4]. Device ID: 0000 0100 0100'b=Si5368 |

Register 135.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------|----|----|----|----------------|----|----|----|
| Name | PARTNUM_RO [3:0] | | | | REVID_RO [3:0] | | | |
| Type | R | | | | R | | | |

Reset value = 0100 0010

| Bit | Name | Function |
|-----|------------------|---|
| 7:4 | PARTNUM_RO [3:0] | PARTNUM_RO [3:0]. See Register 134. |
| 3:0 | REVID_RO [3:0] | REVID_RO [3:0]. Indicates revision number of device. 0000: Revision A 0001: Revision B 0010: Revision C Other codes: Reserved |

Register 136.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|------|----|----|----|----|----|----|
| Name | RST_REG | ICAL | | | | | | |
| Type | R/W | R/W | R | R | R | R | R | R |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|----------|--|
| 7 | RST_REG | <p>RST_REG. Internal Reset. 0: Normal operation. 1: Reset of all internal logic. Outputs tristated or disabled during reset.</p> |
| 6 | ICAL | <p>ICAL. Start an Internal Calibration Sequence. For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. Note: Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. Changes in SFOUTn_REG, PD_CKn, or DSBLn_REG will cause a random change in skew until an ICAL is completed. 0: Normal operation. 1: Writing a “1” initiates internal self-calibration. Upon completion of internal self-calibration, ICAL is internally reset to zero.</p> |
| 5:0 | Reserved | |

Register 138.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|------------------|------------------|------------------|------------------|
| Name | | | | | LOS4_EN [1:1] | LOS3_EN [1:1] | LOS2_EN [1:1] | LOS1_EN [1:1] |
| Type | R | R | R | R | R/W | R/W | R/W | R/W |

Reset value = 0000 1111

| Bit | Name | Function |
|-----|---------------|---|
| 7:4 | Reserved | |
| 3 | LOS4_EN [1:0] | <p>LOS4_EN [1:0]. Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p> |
| 2 | LOS3_EN [1:0] | <p>LOS3_EN [1:0]. Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p> |
| 1 | LOS2_EN [1:0] | <p>LOS2_EN [1:0]. Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p> |
| 0 | LOS1_EN [1:0] | <p>LOS1_EN [1:0]. Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p> |

Register 139.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------|------------------|------------------|------------------|---------|---------|---------|---------|
| Name | LOS4_EN [0:0] | LOS3_EN [0:0] | LOS2_EN [0:0] | LOS1_EN [0:0] | FOS4_EN | FOS3_EN | FOS2_EN | FOS1_EN |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 1111 1111

| Bit | Name | Function |
|-----|---------------|--|
| 7 | LOS4_EN [0:0] | <p>LOS4_EN [0:0]. Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2). Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p> |
| 6 | LOS3_EN [0:0] | <p>LOS3_EN [0:0]. Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2). Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p> |
| 5 | LOS2_EN [0:0] | <p>LOS2_EN. Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2). Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p> |
| 4 | LOS1_EN [0:0] | <p>LOS1_EN [0:0]. Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2). Note: LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p> |

| Bit | Name | Function |
|-----|---------|--|
| 3 | FOS4_EN | FOS4_EN. Enables FOS on a Per Channel Basis. 0: Disable FOS monitoring. 1: Enable FOS monitoring. |
| 2 | FOS3_EN | FOS3_EN. Enables FOS on a Per Channel Basis. 0: Disable FOS monitoring. 1: Enable FOS monitoring. |
| 1 | FOS2_EN | FOS2_EN. Enables FOS on a Per Channel Basis. 0: Disable FOS monitoring. 1: Enable FOS monitoring. |
| 0 | FOS1_EN | FOS1_EN. Enables FOS on a Per Channel Basis. 0: Disable FOS monitoring. 1: Enable FOS monitoring. |

Register 140.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW1 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-------------------------|--|
| 7:0 | INDEPEND-ENTSKEW1 [7:0] | INDEPENDENTSKEW1 [7:0]. 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. |

Register 141.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW2 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0001

| Bit | Name | Function |
|-----|-------------------------|--|
| 7:0 | INDEPEND-ENTSKEW2 [7:0] | INDEPENDENTSKEW2 [7:0]. 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. |

Register 142.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW3 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-------------------------|--|
| 7:0 | INDEPEND-ENTSKEW3 [7:0] | INDEPENDENTSKEW3 [7:0]. 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. |

Register 143.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW4 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-------------------------|--|
| 7:0 | INDEPEND-ENTSKEW4 [7:0] | INDEPENDENTSKEW4 [7:0]. 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. |

Register 144.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW5 [7:0] | | | | | | | |
| Type | R/W | | | | | | | |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|-------------------------|---|
| 7:0 | INDEPEND-ENTSKEW5 [7:0] | INDEPENDENTSKEW5 [7:0]. 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider when CK_CONFIG = 0. |

Table 9. CKOUT_ALWAYS_ON and SQICAL Truth Table

| CKOUT_ALWAYS_ON | SQICAL | Results | Output to Output Skew Preserved? |
|-----------------|--------|---|----------------------------------|
| 0 | 0 | CKOUT OFF until after the first ICAL | N |
| 0 | 1 | CKOUT OFF until after the first successful ICAL (i.e., when LOL is low) | Y |
| 1 | 0 | CKOUT always ON, including during an ICAL | N |
| 1 | 1 | CKOUT always ON, including during an ICAL | Y |

Table 10 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 10. Register Locations Requiring ICAL

| Address | Register |
|---------|-----------------|
| 0 | BYPASS_REG |
| 0 | CKOUT_ALWAYS_ON |
| 1 | CK_PRIOR4 |
| 1 | CK_PRIOR3 |
| 1 | CK_PRIOR2 |
| 1 | CK_PRIOR1 |
| 2 | BWSEL_REG |
| 4 | HIST_DEL |
| 5 | ICMOS |
| 7 | FOSREFSEL |
| 9 | HIST_AVG |
| 10 | DSBL5_REG |
| 10 | DSBL4_REG |
| 10 | DSBL3_REG |
| 10 | DSBL2_REG |
| 10 | DSBL1_REG |
| 11 | PD_CK2 |
| 11 | PD_CK1 |
| 19 | FOS_EN |
| 19 | FOS_THR |
| 19 | VALTIME |
| 19 | LOCKT |
| 21 | INCDEC_PIN |
| 25 | N1_HS |
| 26 | NC1_LS |
| 28 | NC2_LS |
| 31 | NC3_LS |
| 34 | NC4_LS |
| 37 | NC5_LS |
| 40 | N2_HS |
| 40 | N2_LS |
| 43 | N31 |
| 46 | N32 |
| 49 | N33 |
| 51 | N34 |
| 55 | CLKIN2RATE |
| 55 | CLKIN1RATE |
| 56 | CLKIN4RATE |
| 56 | CLKIN3RATE |

7. Pin Descriptions: Si5368

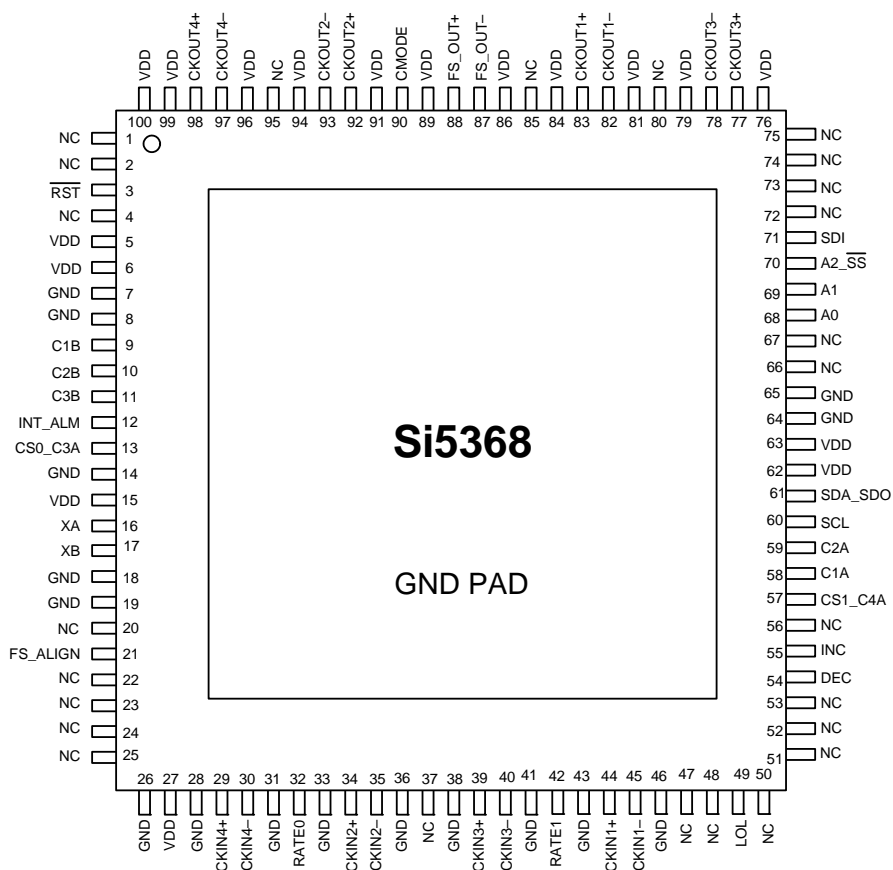


Table 11. Si5368 Pin Descriptions

| Pin # | Pin Name | I/O | Signal Level | Description | | | | | | | | | | | | | | | | | | | | |
|--|-------------------------|-----------------|--------------|---|------|------------|------|-------------------|----|-------------------|----|-------------------|--------|-------------------|--------|-------------------|--------|-------------------|--------|-------------------|--------|-------------------|-------------|-------------------|
| 1, 2, 4, 20, 22, 23, 24, 25, 37, 47, 48, 50, 51, 52, 53, 56, 66, 67, 72, 73, 74, 75, 80, 85, 95 | NC | | | No Connect. These pins must be left unconnected for normal operation. | | | | | | | | | | | | | | | | | | | | |
| 3 | $\overline{\text{RST}}$ | I | LVC MOS | External Reset. Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up. | | | | | | | | | | | | | | | | | | | | |
| 5, 6, 15, 27, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100 | V _{DD} | V _{DD} | Supply | V_{DD}. The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V _{DD} pins: <table border="0"> <thead> <tr> <th>Pins</th> <th>Bypass Cap</th> </tr> </thead> <tbody> <tr> <td>5, 6</td> <td>0.1 μF</td> </tr> <tr> <td>15</td> <td>0.1 μF</td> </tr> <tr> <td>27</td> <td>0.1 μF</td> </tr> <tr> <td>62, 63</td> <td>0.1 μF</td> </tr> <tr> <td>76, 79</td> <td>1.0 μF</td> </tr> <tr> <td>81, 84</td> <td>0.1 μF</td> </tr> <tr> <td>86, 89</td> <td>0.1 μF</td> </tr> <tr> <td>91, 94</td> <td>0.1 μF</td> </tr> <tr> <td>96, 99, 100</td> <td>0.1 μF</td> </tr> </tbody> </table> | Pins | Bypass Cap | 5, 6 | 0.1 μF | 15 | 0.1 μF | 27 | 0.1 μF | 62, 63 | 0.1 μF | 76, 79 | 1.0 μF | 81, 84 | 0.1 μF | 86, 89 | 0.1 μF | 91, 94 | 0.1 μF | 96, 99, 100 | 0.1 μF |
| Pins | Bypass Cap | | | | | | | | | | | | | | | | | | | | | | | |
| 5, 6 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 27 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 62, 63 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 76, 79 | 1.0 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 81, 84 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 86, 89 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 91, 94 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 96, 99, 100 | 0.1 μF | | | | | | | | | | | | | | | | | | | | | | | |
| 7, 8, 14, 18, 19, 26, 28, 31, 33, 36, 38, 41, 43, 46, 64, 65 | GND | GND | Supply | Ground. This pin must be connected to system ground. Minimize the ground path impedance for optimal performance. | | | | | | | | | | | | | | | | | | | | |
| 9 | C1B | O | LVC MOS | CKIN1 Invalid Indicator. This pin performs the <i>CK1_BAD</i> function if <i>CK1_BAD_PIN</i> = 1 and is tristated if <i>CK1_BAD_PIN</i> = 0. Active polarity is controlled by <i>CK_BAD_POL</i> . 0 = No alarm on CKIN1. 1 = Alarm on CKIN1. | | | | | | | | | | | | | | | | | | | | |
| 10 | C2B | O | LVC MOS | CKIN2 Invalid Indicator. This pin performs the <i>CK2_BAD</i> function if <i>CK2_BAD_PIN</i> = 1 and is tristated if <i>CK2_BAD_PIN</i> = 0. Active polarity is controlled by <i>CK_BAD_POL</i> . 0 = No alarm on CKIN2. 1 = Alarm on CKIN2. | | | | | | | | | | | | | | | | | | | | |
| Note: Internal register names are indicated by underlined italics, e.g. <i>INT_PIN</i> . See Si5368 Register Map. | | | | | | | | | | | | | | | | | | | | | | | | |

Table 11. Si5368 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description | | | | | | | | | | |
|----------|--------------------|-----|--------------|---|---------|--------------------|----|-------|----|-------|----|-------|----|-------|
| 11 | C3B | O | LVC MOS | <p>CKIN3 Invalid Indicator. This pin performs the <i>CK3_BAD</i> function if <i>CK3_BAD_PIN</i> = 1 and is tristated if <i>CK3_BAD_PIN</i> = 0. Active polarity is controlled by <i>CK_BAD_POL</i>. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.</p> | | | | | | | | | | |
| 12 | INT_ALM | O | LVC MOS | <p>Interrupt/Alarm Output Indicator. This pin functions as a maskable interrupt output with active polarity controlled by the <i>INT_POL</i> register bit. The INT output function can be turned off by setting <i>INT_PIN</i> = 0. If the ALRM-OUT function is desired instead on this pin, set <i>ALRMOUT_PIN</i> = 1 and <i>INT_PIN</i> = 0. 0 = <i>ALRMOUT</i> not active. 1 = <i>ALRMOUT</i> active. The active polarity is controlled by <i>CK_BAD_POL</i>. If no function is selected, the pin tristates.</p> | | | | | | | | | | |
| 13 57 | CS0_C3A CS1_C4A | I/O | LVC MOS | <p>Input Clock Select/CKIN3 or CKIN4 Active Clock Indicator. Input: If manual clock selection is chosen, and if <i>CKSEL_PIN</i> = 1, the CKSEL pins control clock selection and the <i>CKSEL_REG</i> bits are ignored.</p> <table border="1"> <thead> <tr> <th>CS[1:0]</th> <th>Active Input Clock</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>CKIN1</td> </tr> <tr> <td>01</td> <td>CKIN2</td> </tr> <tr> <td>10</td> <td>CKIN3</td> </tr> <tr> <td>11</td> <td>CKIN4</td> </tr> </tbody> </table> <p>If <i>CKSEL_PIN</i> = 0, the <i>CKSEL_REG</i> register bits control this function and these inputs tristate. If configured as inputs, these pins must not float. Output: If auto clock selection is enabled, then they serve as the CKIN_n active clock indicator. 0 = CKIN3 (CKIN4) is not the active input clock 1 = CKIN3 (CKIN4) is currently the active input to the PLL The <i>CK_nACTV_REG</i> bit always reflects the active clock status for CKIN_n. If <i>CK_nACTV_PIN</i> = 1, this status will also be reflected on the CnA pin with active polarity controlled by the <i>CK_ACTV_POL</i> bit. If <i>CK_nACTV_PIN</i> = 0, this output tristates.</p> | CS[1:0] | Active Input Clock | 00 | CKIN1 | 01 | CKIN2 | 10 | CKIN3 | 11 | CKIN4 |
| CS[1:0] | Active Input Clock | | | | | | | | | | | | | |
| 00 | CKIN1 | | | | | | | | | | | | | |
| 01 | CKIN2 | | | | | | | | | | | | | |
| 10 | CKIN3 | | | | | | | | | | | | | |
| 11 | CKIN4 | | | | | | | | | | | | | |
| 16 17 | XA XB | I | ANALOG | <p>External Crystal or Reference Clock. External crystal should be connected to these pins to use internal oscillator based reference. Refer to Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.</p> | | | | | | | | | | |

Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.

Table 11. Si5368 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|--|------------------|-----|--------------|--|
| 21 | FS_ALIGN | I | LVC MOS | FSYNC Alignment Control. If <i>FSYNC_ALIGN_PIN</i> = 1 and <i>CK_CONFIG</i> = 1, a logic high on this pin causes the FS_OUT phase to be realigned to the rising edge of the currently active input sync (CKIN_3 or CKIN_4). If <i>FSYNC_ALIGN_PIN</i> = 0, this pin is ignored and the <i>FSYNC_ALIGN_REG</i> bit performs this function. 0 = No realignment. 1 = Realign. This pin has a weak pull-down. |
| 29 30 | CKIN4+ CKIN4– | I | MULTI | Clock Input 4. Differential clock input. This input can also be driven with a single-ended signal. CKIN4 serves as the frame sync input associated with the CKIN2 clock when <i>CK_CONFIG_REG</i> = 1. |
| 32 42 | RATE0 RATE1 | I | 3-Level | External Crystal or Reference Clock Rate. Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M. |
| 34 35 | CKIN2+ CKIN2– | I | MULTI | Clock Input 2. Differential input clock. This input can also be driven with a single-ended signal. |
| 39 40 | CKIN3+ CKIN3– | I | MULTI | Clock Input 3. Differential clock input. This input can also be driven with a single-ended signal. CKIN3 serves as the frame sync input associated with the CKIN1 clock when <i>CK_CONFIG_REG</i> = 1. |
| 44 45 | CKIN1+ CKIN1– | I | MULTI | Clock Input 1. Differential clock input. This input can also be driven with a single-ended signal. |
| 49 | LOL | O | LVC MOS | PLL Loss of Lock Indicator. This pin functions as the active high PLL loss of lock indicator if the <i>LOL_PIN</i> register bit is set to one. 0 = PLL locked. 1 = PLL unlocked. If <i>LOL_PIN</i> = 0, this pin will tristate. Active polarity is controlled by the <i>LOL_POL</i> bit. The PLL lock status will always be reflected in the <i>LOL_INT</i> read only register bit. |
| Note: Internal register names are indicated by underlined italics, e.g. <i>INT_PIN</i> . See Si5368 Register Map. | | | | |

Table 11. Si5368 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|--|----------|-----|--------------|---|
| 54 | DEC | I | LVC MOS | <p>Coarse Latency Decrement. A pulse on this pin decreases the input to output device latency by $1/f_{OSC}$ (approximately 200 ps). Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. There is no limit on the range of latency adjustment by this method. Pin control is enabled by setting <i>INCDEC_PIN</i> = 1 (default). If <i>INCDEC_PIN</i> = 0, this pin is ignored and coarse output latency is controlled via the CLAT register. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock switch. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. This pin has a weak pull-down.</p> |
| 55 | INC | I | LVC MOS | <p>Coarse Latency Increment. A pulse on this pin increases the input to output device latency by $1/f_{OSC}$ (approximately 200 ps). Detailed operations, restrictions, and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. There is no limit on the range of latency adjustment by this method. Pin control is enabled by setting <i>INCDEC_PIN</i> = 1 (default). Note: INC does not increase latency if NI_HS = 4. If <i>INCDEC_PIN</i> = 0, this pin is ignored and coarse output latency is controlled via the CLAT register. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock switch. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. This pin has a weak pull-down.</p> |
| 58 | C1A | O | LVC MOS | <p>CKIN1 Active Clock Indicator. This pin serves as the CKIN1 active clock indicator. The <i>CK1_ACTV_REG</i> bit always reflects the active clock status for CKIN1. If <i>CK1_ACTV_PIN</i> = 1, this status will also be reflected on the C1A pin with active polarity controlled by the <i>CK_ACTV_POL</i> bit. If <i>CK1_ACTV_PIN</i> = 0, this output tristates.</p> |
| 59 | C2A | O | LVC MOS | <p>CKIN2 Active Clock Indicator. This pin serves as the CKIN2 active clock indicator. The <i>CK2_ACTV_REG</i> bit always reflects the active clock status for CKIN2. If <i>CK2_ACTV_PIN</i> = 1, this status will also be reflected on the C2A pin with active polarity controlled by the <i>CK_ACTV_POL</i> bit. If <i>CK2_ACTV_PIN</i> = 0, this output tristates.</p> |
| <p>Note: Internal register names are indicated by underlined italics, e.g. <i>INT_PIN</i>. See Si5368 Register Map.</p> | | | | |

Table 11. Si5368 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|--|--------------------|-----|--------------|---|
| 60 | SCL | I | LVC MOS | Serial Clock. This pin functions as the serial port clock input for both SPI and I ² C modes. This pin has a weak pull-down. |
| 61 | SDA_SDO | I/O | LVC MOS | Serial Data. In I ² C microprocessor control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data output. |
| 68 69 | A0 A1 | I | LVC MOS | Serial Port Address. In I ² C microprocessor control mode (CMODE = 0), these pins function as hardware controlled address bits. The I ² C address is 1101 [A2] [A1] [A0]. In SPI microprocessor control mode (CMODE = 1), these pins are ignored. This pin has a weak pull-down. |
| 70 | A2_SS | I | LVC MOS | Serial Port Address/Slave Select. In I ² C microprocessor control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI microprocessor control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down. |
| 71 | SDI | I | LVC MOS | Serial Data In. In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data input. In I ² C microprocessor control mode (CMODE = 0), this pin is ignored. This pin has a weak pull-down. |
| 77 78 | CKOUT3+ CKOUT3- | O | MULTI | Clock Output 3. Differential clock output. Output signal format is selected by <i>SFOUT3_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 82 83 | CKOUT1- CKOUT1+ | O | MULTI | Clock Output 1. Differential clock output. Output signal format is selected by <i>SFOUT1_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 87 88 | FS_OUT- FS_OUT+ | O | MULTI | Frame Sync Output. Differential frame sync output or fifth high-speed clock output. Output signal format is selected by <i>SFOUT_FS_SYNC_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. Duty cycle and active polarity are controlled by <i>FSYNC_PW</i> and <i>FSYNC_POL</i> bits, respectively. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. |
| Note: Internal register names are indicated by underlined italics, e.g. <i>INT_PIN</i> . See Si5368 Register Map. | | | | |

Table 11. Si5368 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|----------|--------------------|-----|--------------|--|
| 90 | CMODE | I | LVC MOS | Control Mode. Selects I ² C or SPI control mode for the device. 0 = I ² C Control Mode. 1 = SPI Control Mode. This pin must be tied high or low. |
| 92 93 | CKOUT2+ CKOUT2– | O | MULTI | Clock Output 2. Differential clock output. Output signal format is selected by <i>SFOUT2_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 97 98 | CKOUT4– CKOUT4+ | O | MULTI | Clock Output 4. Differential clock output. Output signal format is selected by <i>SFOUT4_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| GND PAD | GND PAD | GND | Supply | Ground Pad. The ground pad must provide a low thermal and electrical impedance to a ground plane. |

Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5368 Register Map.

8. Ordering Guide

| Ordering Part Number | Output Clock Frequency Range | Package | ROHS6, Pb-Free | Temperature Range |
|----------------------|--|-------------------------|----------------|-------------------|
| Si5368A-C-GQ | 2 kHz–945 MHz 970–1134 MHz 1.213–1.417 GHz | 100-Pin 14 x 14 mm TQFP | Yes | –40 to 85 °C |
| Si5368B-C-GQ | 2 kHz–808 MHz | 100-Pin 14 x 14 mm TQFP | Yes | –40 to 85 °C |
| Si5368C-C-GQ | 2 kHz–346 MHz | 100-Pin 14 x 14 mm TQFP | Yes | –40 to 85 °C |

Note: Add an R at the end of the device to denote tape and reel options (for example, Si5368-C-GMR).

9. Package Outline: 100-Pin TQFP

Figure 6 illustrates the package details for the Si5368. Table 12 lists the values for the dimensions shown in the illustration.



Figure 6. 100-Pin Thin Quad Flat Package (TQFP)

Table 12. 100-Pin Package Diagram Dimensions

| Dimension | Min | Nom | Max | Dimension | Min | Nom | Max |
|-----------|------------|------|------|-----------|------------|------|------|
| A | — | — | 1.20 | E | 16.00 BSC. | | |
| A1 | 0.05 | — | 0.15 | E1 | 14.00 BSC. | | |
| A2 | 0.95 | 1.00 | 1.05 | E2 | 3.85 | 4.00 | 4.15 |
| b | 0.17 | 0.22 | 0.27 | L | 0.45 | 0.60 | 0.75 |
| c | 0.09 | — | 0.20 | aaa | — | — | 0.20 |
| D | 16.00 BSC. | | | bbb | — | — | 0.20 |
| D1 | 14.00 BSC. | | | ccc | — | — | 0.08 |
| D2 | 3.85 | 4.00 | 4.15 | ddd | — | — | 0.08 |
| e | 0.50 BSC. | | | θ | 0° | 3.5° | 7° |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Recommended PCB Layout



Figure 7. PCB Land Pattern Diagram

Table 13. PCB Land Pattern Dimensions

| Dimension | MIN | MAX |
|-----------|------------|-------|
| e | 0.50 BSC. | |
| E | 15.40 REF. | |
| D | 15.40 REF. | |
| E2 | 3.90 | 4.10 |
| D2 | 3.90 | 4.10 |
| GE | 13.90 | — |
| GD | 13.90 | — |
| X | — | 0.30 |
| Y | 1.50 REF. | |
| ZE | — | 16.90 |
| ZD | — | 16.90 |
| R1 | 0.15 REF | |
| R2 | — | 1.00 |

Notes:**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Si5368

11. Top Marking: 100-Pin TQFP

11.1. Si5368 Top Marking



11.2. Top Marking Explanation

| | | |
|------------------------|--|---|
| Mark Method: | Laser | |
| Logo Size: | 9.2 x 3.1 mm Center-Justified | |
| Font Size: | 3.0 Point (1.07 mm) Right-Justified | |
| Line 1 Marking: | Device Part Number | X = Speed Grade See "7. Pin Descriptions: Si5368" on page 79. |
| Line 2 Marking: | YY = Year WW = Workweek R=Die Revision | Assigned by the Assembly Supplier. Corresponds to the year and work-week of the mold date. |
| | TTTTT = Mfg Code | Manufacturing Code |
| Line 3 Marking: | Circle = 1.8 mm Diameter Center-Justified | "e3" Pb-Free Symbol |
| | Country of Origin ISO Code Abbreviation | |

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed LVTTTL to LVCMOS in Table 9, “Absolute Maximum Ratings,” on page 18.
- Updated Figure 4 and Figure 5 on page 19.
- Updated “5. Register Map”.
 - Added RATE0 to pin description. By changing RATE[1:0] the part can emulate a Si5367.
 - Changed XA/XB pin description to support both differential and single ended external REFCLK.

Revision 0.2 to Revision 0.3

- Added Figure on p..8.
- Updated Figure 4, “Si5368 Typical Application Circuit (I²C Control Mode),” and Figure 5, “Si5368 Typical Application Circuit (SPI Control Mode),” on page 19 to show INC and DEC.
- Updated “5. Register Map”.
 - Changed font of register names to *underlined italics*.
- Updated “7. Pin Descriptions: Si5368” on page 79.
- Added “10. Recommended PCB Layout”.

Revision 0.3 to Revision 0.4

- Changed V_{DD} specification for 1.8 V.
- Updated Table 8 on page 16.
- Updated Table 9 on page 18.
- Added table under Figure on page 8.
- Updated “4. Functional Description” on page 20.
- Clarified “5. Register Map” on page 22 including correcting pin assignments for RATE0 and RATE1.

Revision 0.4 to Revision 0.41

- Added register map.
- Added 3.3 V operation.
- Removed some TBDs from the AC specifications.

Revision 0.41 to Revision 1.0

- Expanded spec tables.
- Added device top mark drawing.
- Changed “any-rate” to “any-frequency” throughout.
- Added No Bypass mode with CMOS outputs.
- Minor updates to Table 2 on page 4 and Table 6 on page 14.
- Removed “2. Typical Phase Noise Performance”.
- Updated “4. Functional Description” on page 20.
- Revised “5. Register Map” on page 22.
- Revised “11. Top Marking: 100-Pin TQFP” on page 90.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>
and register to submit a technical support request.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories, Silicon Labs, and DSPLL are trademarks of Silicon Laboratories Inc.
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А