Si4133/33G-EVB

EVALUATION BOARD FOR THE SYNTHESIZER FAMILIES

Description

The Si4133/Si4133G synthesizer family evaluation board is a complete, PC-based evaluation platform for the following Silicon Laboratories devices and their derivatives:

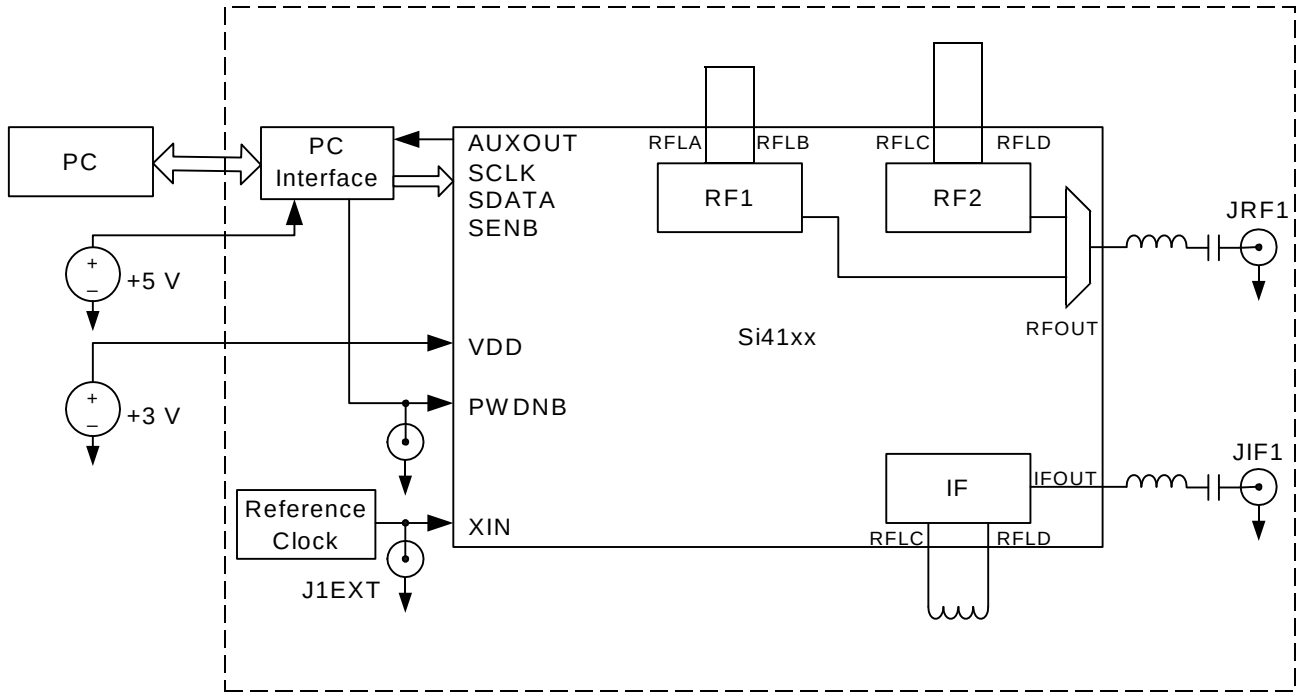
- Si4133
- Si4133G
- Si4133G-X2
- Si4113G-X5
- Si4114G
- Si4135
- Si4136

The board includes all support circuitry necessary to evaluate the synthesizer including a reference clock, SMA connections for external measurement equipment, and an interface to a personal computer for controlling the device. The PC software is a graphical, easy-to-use interface that allows the user to directly enter frequencies, set divider ratios, and toggle power control options by a parallel port connection. A PC and power supply are all that is needed for a complete evaluation system.

Features

- Single board evaluation platform
- PC-based graphical control software included on CD-ROM for Windows 95/98
- On-board frequency reference; SMA for external reference
- SMA connections for synthesizer outputs
- For use with Silicon Laboratories Si4133, Si4133G, Si4133G-X2, Si4113G-X5, Si4114G, Si4135 and Si4136 synthesizer families (TSSOP or MLP)

Function Block Diagram



Functional Description

The evaluation board accommodates the synthesizer by providing clock circuitry, a PC interface, and other support circuitry necessary for operation.

Synthesizer

The heart of the evaluation board is the Silicon Laboratories frequency synthesizer. This section includes the synthesizer integrated circuit (IC), external tuning components, output matching, and power supply decoupling circuitry.

For devices requiring an external inductor to establish the center frequency for the RF1 and RF2 synthesizers, the inductor is implemented with a printed trace. The IF synthesizer inductor is set by an 0402-size chip inductor. The inductors are set for the nominal center frequencies shown in Table 1.

Outputs of the synthesizers are ac-coupled and matched to a 50 Ω load impedance. SMA connectors are provided for easy connection to measurement equipment or to target systems. Output JRF1 is multiplexed between the RF1 and RF2 synthesizers and is toggled through the evaluation software. See the synthesizer data sheet for more detail. The second output, JIF1, is connected to the IF synthesizer output.

Both the multiplexed RF output and the IF output can be active simultaneously. Synthesizers are independently enabled using the radio buttons in the evaluation software.

The synthesizer IC is supplied by three different power supplies. VDDR supplies the analog circuitry for the RF1 and RF2 synthesizers. VDDI supplies the analog circuitry for the IF synthesizer, and VDDD supplies the digital prescaler, serial interface, and reference input circuitry. Each of these supplies is bypassed to ground with a 22 nF capacitor close to the body of the IC.

PC Interface

The frequency synthesizer IC uses a serial interface for programming. The three primary signals are serial data (SDATA), serial clock (SCLK), and serial enable (SENB). These are all mapped to data pins of the PC's parallel port. Data is read back from the IC using the BUSY input of the parallel port and SCLK.

One additional signal, GPO, is a multipurpose signal used to control the synthesizer's hardware power-down enable (PWDNB) and/or to trigger external test equipment. The intended use is for power-up and channel-to-channel settling time measurements. See the "Evaluation Software" section for more detail.

Table 1. Center Frequencies

Device	RF1 Center Frequency (MHz)	RF2 Center Frequency (MHz)	IF Center Frequency (MHz)
Si4133	1600	1200	550
Si4133G	1600	1200	550
Si4133G-X2	1600	1200	1080
Si4113G-X5	1540	1365	N/A
Si4114G	1920	1780	N/A
Si4135	1750	967	170.76, 420.76
Si4136	2400	2100	550

Clock Circuitry

The reference frequency for the synthesizer is generated on-board by a temperature-compensated, voltage-tuned, crystal oscillator. The circuit is flexible to allow evaluation with an external reference source or with different frequency oscillators in varying packages.

Header JP6 selects the reference frequency source to the frequency synthesizer IC. Either the on-board oscillator or the external SMA input, J8, can be selected.

The tuning control of the oscillator, Vc, is fixed at (Vsupply/2) by R19 and R20. C14 provides filtering for noise reduction on the tuning input. Test points JP9 and JP10 allow easy connection to the tuning voltage for external frequency trimming or reference modulation.

Power Supplies

The evaluation board requires a 5 V supply at JP11 to power the digital interface to the PC. The synthesizer's supply voltage can be taken from the on-board 3 V regulator or a user-supplied voltage at JP11 depending on the jumper setting at JP4.

AUXOUT

The AUXOUT pin of the frequency synthesizer can be programmed for a variety of functions. The evaluation board is normally populated so that this pin can be read by the PC for serial reads from the IC. Other functions can be monitored on the AUXOUT test point as well.

Refer to the appropriate synthesizer data sheet for details of AUXOUT's functionality and configuration.

Hardware Power Down

The hardware power-down input, PWDNB, can be driven several different ways on the evaluation board. The default configuration is pulled high (enabled) through a resistive pull-up, R21. This pin may be controlled through an external source or via evaluation software.

To control PWDNB with an external generator, place a shorting block on JP3. There should not be a shorting block on JP2. Connect the output of the generator to test point PWDNB. The test point labeled GND should be connected to the shield of the cable.

The evaluation software can power down the synthesizer through the PWDNB pin. JP2 and JP3 must both be jumpered to use this feature. The PWDNB test point can then be used to monitor the PWDNB signal.

Refer to the appropriate synthesizer data sheet for a complete explanation of software and hardware power management options.

Table 2. Jumper Settings

Function	Option	Jumper Settings	Notes
Synthesizer and Reference Clock Power	On-board regulator	JP4: jumper REG to 3 V	No supply required on JP11 3 V pin
	User-supplied	JP4: jumper UNREG to 3 V	Supply required on JP11 3 V pin
Reference Clock	On-board reference clock	JP5: jumper TCXO to ON JP6: TCXO to XIN	No clock required on J8
	User-supplied	JP5: jumper TCXO to OFF JP6: EXT to XIN	Clock signal required on J8; Check data sheet for requirements.
PWDNB	Always high	JP2: no jumper JP3: no jumper	Power-up/down controlled by register settings.
	Driven by PC	JP2: jumper JP3: jumper	PWDNB controlled by evaluation software; Connect instrumentation trigger to PWDNB/GND test points.
	Driven by external generator	JP2: no jumper JP3: jumper	PWDNB provided by external generator connected to PWDNB/GND test points.

Table 3. Test Points

Function	Designator	Signal
Auxiliary Output	AUXOUT	AUXOUT signal from synthesizer
PC Interface	SCLK	Serial clock from PC parallel port
	SDATA	Serial data from PC parallel port
	SENB	Serial enable from PC parallel port
	GPO	General purpose output from PC parallel port
Power	3 V	Power supply to synthesizer and on-board reference oscillator
	GND	Ground reference for 3 V test point
PWDNB	PWDNB	PWDNB signal from synthesizer or GPO from PC parallel port
	GND	Ground reference for PWDNB test point
Reference Frequency Control	VC	Frequency control input on TCVCXO
	GND	Ground reference for VC test point

Table 4. Connectors

Function	Designator	Signal
PC Parallel Port Interface	JP1	Parallel port connection to PC
Power	JP11	5 V supply for parallel port interface and optional 3 V supply for synthesizer and reference oscillator
RF Outputs	JIF1	IF synthesizer output, nominal 50 Ω
	JRF1	RF synthesizer output, nominal 50 Ω
External Reference Input	J8	External reference frequency input, selected by JP6

Evaluation Software

The Silicon Laboratories evaluation software is a graphical, Windows-based user interface to the Silicon Laboratories synthesizer family. The interface allows the user to directly enter counter integers, frequencies, or control bits without the need to compute and format bit-level register information. Hardware connection to the evaluation board is through a standard parallel port.

Installation

After the CD is inserted into the computer, the installer should run automatically. The installer can also be invoked by running the “Installer.exe” program at the root directory of the CD. The CD contains installers for several programs. Select the appropriate device from the list.

Window Overview

Control data may be entered in a variety of ways. Each numerical parameter can either be entered directly from the keyboard by selecting the box and typing or can be stepped using the up/down arrow keys. Control bits are selected or deselected by radio buttons.

Note: The windows shown in these figures are specific to the Si4133 Programmer, version 1.3.6. Evaluation software and options may vary for other synthesizers and software versions.

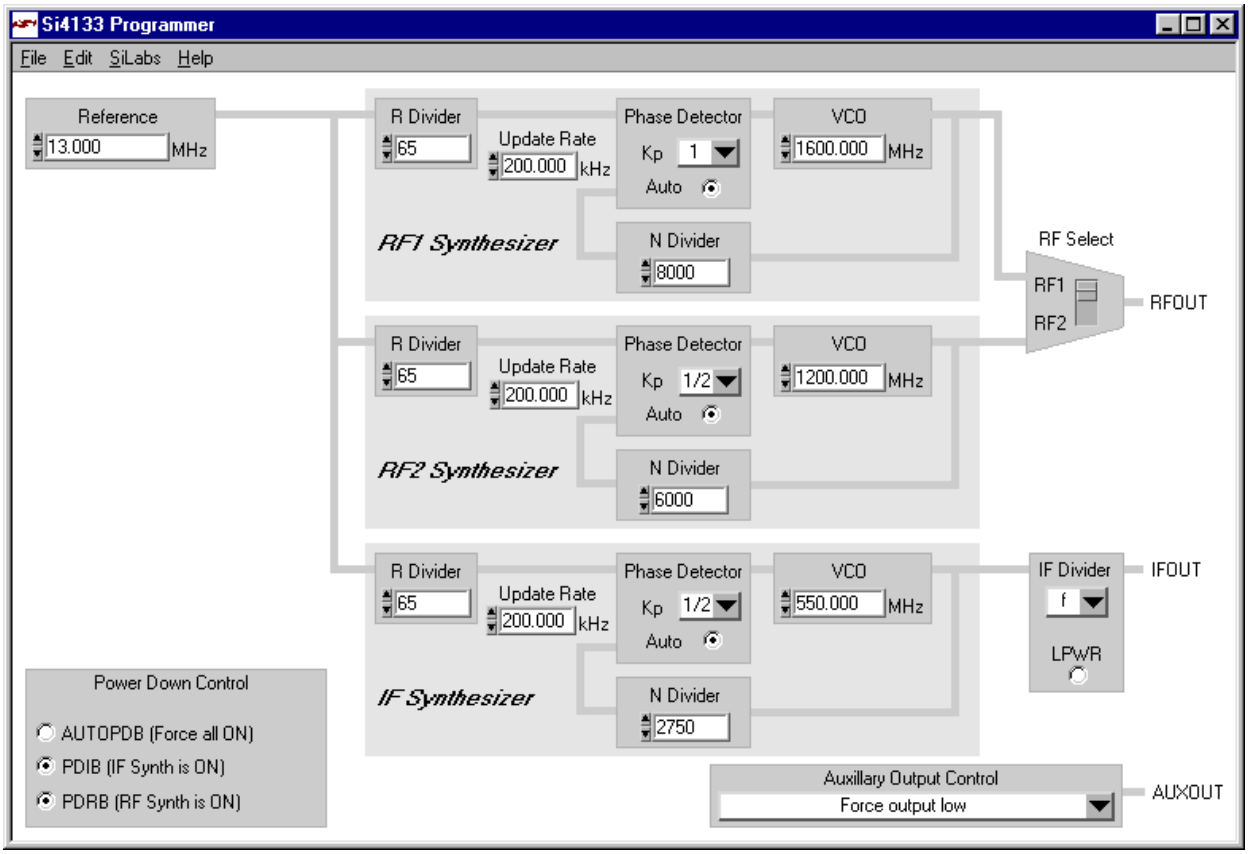


Figure 1. Evaluation Software

Controls

The various controls are described below.

Reference Divider, Reference Frequency, and Update Rate

The reference divider value sets the update rate of the phase detector for a given reference frequency. This value can be set by either using the R-Divider input, the Reference input, or the Update Rate input. All of these controls are linked to set the R Divider in the synthesizer. Writing to any of these registers for RF1 or RF2 will select the associated synthesizer at the RFOUT output.

The R-Divider input directly sets the R Divider of the synthesizer. Changes made to this value will then change the update rate and the synthesized frequency.

The Reference input changes all R Dividers to values such that the update rate and synthesized frequency remain at approximately the same value for the entered reference frequency. Note that this changes only the R Divider not the actual reference frequency of the on-board oscillator.

Changing the Update Rate input changes the R and N Dividers to maintain the same synthesized frequency for a given reference frequency.

Phase Detector

The phase detector value window sets the relative gain of the phase detector. Refer to the appropriate synthesizer data sheet for further information about setting of the phase detector gain.

The Auto K_P option will automatically select the best K_P for phase noise, settling time, and loop stability.

VCO and N Divider

The N Divider can be set by an integer in the N-Divider register or by a decimal frequency in the VCO window. Writing to either of these registers for RF1 or RF2 will select the associated synthesizer at the JRF1 connector. The N-Divider window writes directly to the N Divider of the synthesizer.

The values entered in the VCO register will cause the software to automatically compute and set the N register to generate the specified frequency.

RF Select

The RF Select toggle switch selects the RF1 or RF2 synthesizer output on the JRF1 connector. This control does not correspond to an actual control bit. Synthesizers are toggled by writing to the N Divider of the selected synthesizer. User applications should select the active synthesizer by writing to the N or R register as outlined in the appropriate synthesizer data sheet.

Auxiliary Output Control

Auxiliary Output Control selects the function of the AUXOUT pin. This pin can be used to monitor various functions internal to the synthesizer. Refer to the appropriate synthesizer data sheet for details.

This pin also performs the serial read function of the synthesizer registers by the PC. Serial data will appear at this pin if “Verify Device Writes” or if the VCO Tuning Meters are enabled in the SiLabs pull-down menu.

Power Down Control

The Power Down Control radio buttons select the various software power-down options of the frequency synthesizer IC. (See Figure 2.) The label for each radio button corresponds to the name of the control bit being programmed. See the appropriate synthesizer data sheet for a complete description of power control options.

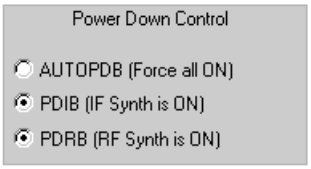


Figure 2. Power-Down Control Radio Buttons

AUTOPDB, *Force All On*, forces the reference amplifier, the RF synthesizers, and the IF synthesizer on. These synthesizers can be enabled independently of each other using PDIB and PDRB.

The hardware PWDNB input overrides all power-up settings selected in this window. The serial interface remains active when powered down.

Menus and Options

Menus and options are described below.

File Menu

The File menu allows register configurations to be saved and restored. By default, configurations are stored as .cfg files in the Configurations folder within the Si4133 Programmer folder. (See Figure 3.)

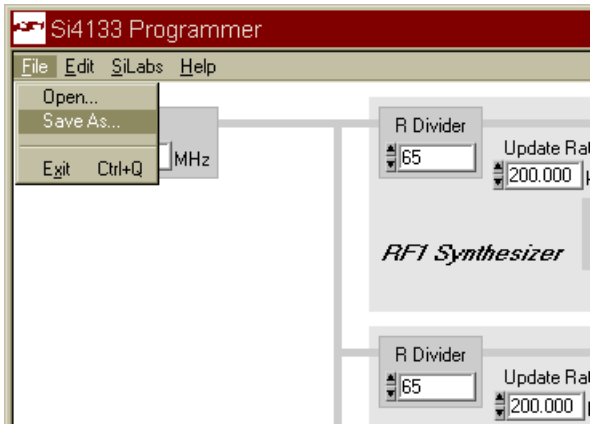


Figure 3. File Menu

The configuration files are text files and can be viewed and edited with a text editor such as Microsoft Notepad™ or Wordpad™.

Edit Menu

The Edit menu allows for copy and paste operations between input windows. (See Figure 4.)

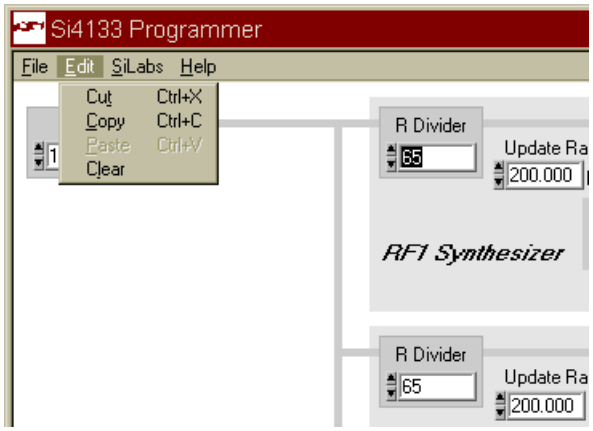


Figure 4. Edit Menu

SiLabs Menu

The SiLabs menu contains the controls specific to the Silicon Laboratories evaluation software and its hardware interface. (See Figure 5.)

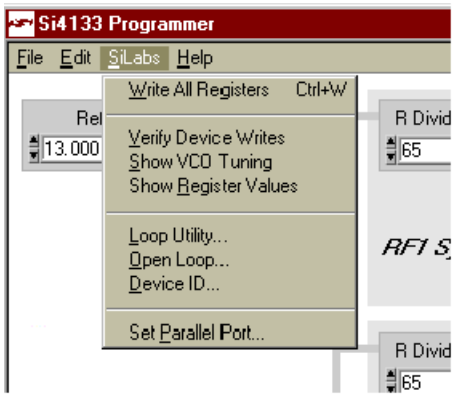


Figure 5. SiLabs Menu

Selecting *Write All Registers* refreshes all registers of the frequency synthesizer IC. This should be selected upon power up to ensure all registers are refreshed.

Selecting *Verify Device Writes* reads and verifies the content of the registers as they are written. If a discrepancy occurs, a pop-up window will show “Device Write Verification Failed.” (See Figure 6.)

Figure 6. Write Fail

The data is read from the frequency synthesizer to the PC through the AUXOUT port. Data read from this register temporarily overrides the function programmed to this pin.

Show VCO Tuning enables graphical, meter-type displays of the self-tuning results of each VCO. The VCO tuning meters are useful when selecting the values for external inductances or monitoring lock behavior. When the needle is at the extreme left of the display, the VCO is operating at the lower end of its frequency range. Similarly, when the needle is at the extreme right of the display, the VCO is operating at the upper end of its frequency range. (See Figure 7.)

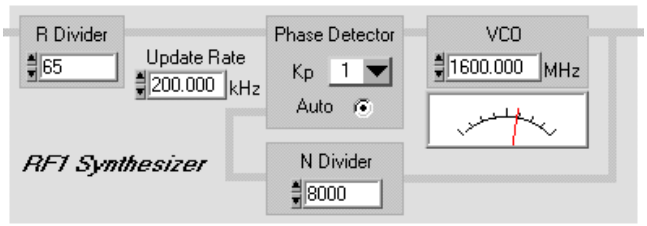


Figure 7. VCO Tuning

Detailed information on the operation and interpretation of the self-tuning algorithm is available in the appendix of the frequency synthesizer data sheet entitled, “Evaluating Self Tuning Results.”

The *Show Register Values* option enables a display of the contents of the synthesizer registers. (See Figure 8.) This is useful in computing register values for application software or for debugging. Refer to the Control Register section of the applicable synthesizer data sheet for definition of the values shown.

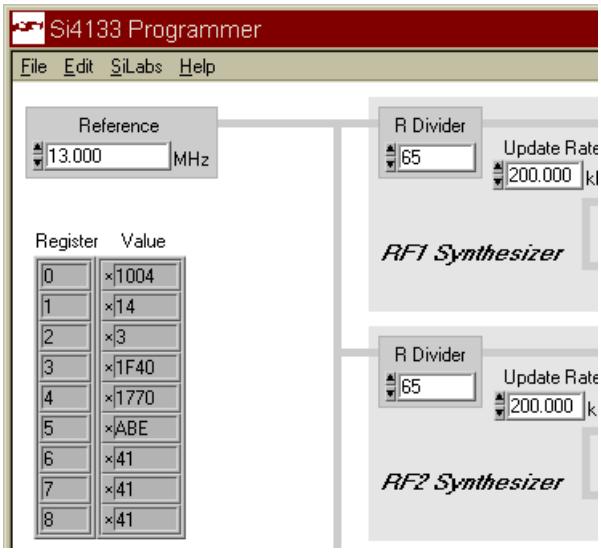


Figure 8. Show Registers

The *Loop Utility* allows the user to automatically toggle between two register settings as shown in Figure 9. Applications include power-up settling time and channel-to-channel settling time measurements. The GPO hardware port is also controlled through the Utility switch in this window to either power down the synthesizer through its hardware port or to trigger external test equipment to correspond to a register write.

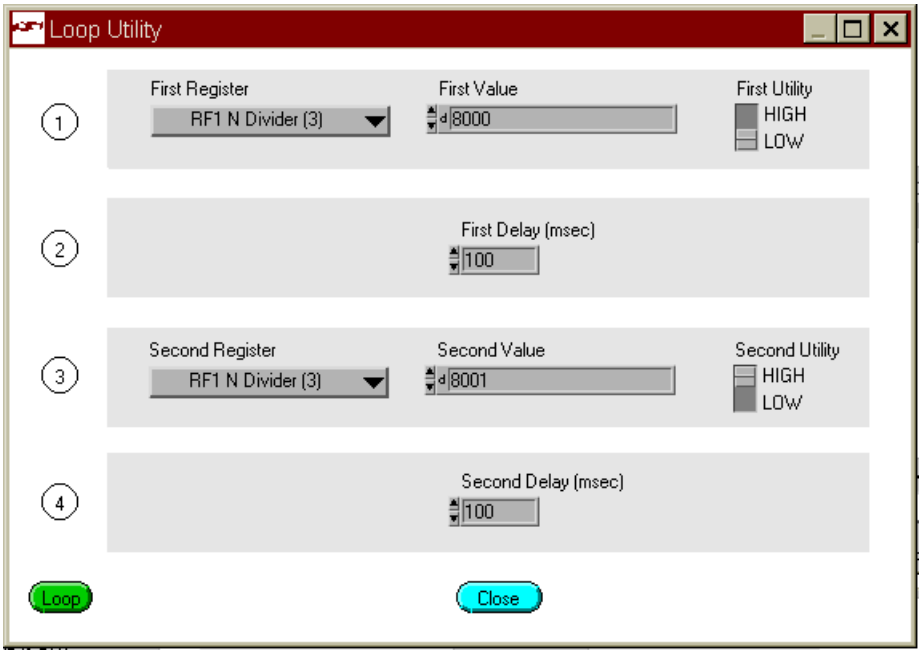


Figure 9. Loop Utility

The loop executes sequentially when the green Loop button is selected and repeats until the red Stop button is pressed. There are four steps. In the first, the register selected in the *First Register* pull-down box is written with the value in the *First Value* box. The GPO hardware signal on the evaluation board is set high or low dependent on the *First Utility* switch setting.

The second step is a delay, entered in milliseconds. The third and fourth steps are set similarly to the first and second.

The configuration shown in Figure 9 could be used to measure channel-to-channel settling time. Steps 1 and 2 set the N counter of the RF1 synthesizer to a given frequency, set the GPO utility signal low, and then pause for 100 milliseconds. Steps 3 and 4 then reprogram the N counter for a different frequency, set the GPO utility port high to trigger measurement equipment, and delay for another 100 ms. The loop repeats so that the measurement equipment can average over several channel changes. In this measurement, the evaluation board should have J2 and JP3 jumpered so that the GPO signal is routed to the PWDNB test point for connection to the test equipment trigger port and also to the PWDNB pin of the synthesizer.

The *Open Loop...* menu selection invokes the window shown in Figure 10. By setting the VCO to operate at its minimum and maximum frequencies, the center frequency can be calculated by averaging these two extremes.

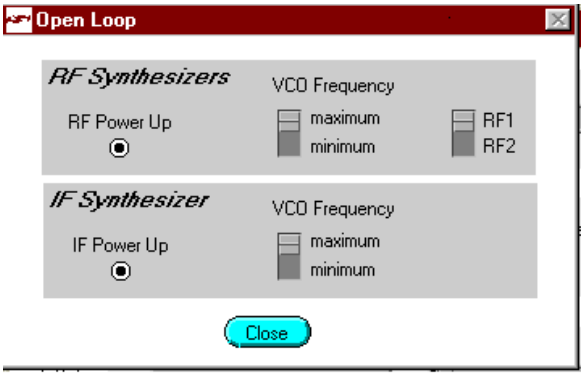


Figure 10. Open Loop Menu

Selecting *Device ID...* causes a pop-up window to appear with an internal device code displayed.

Selecting *Set Parallel Port* allows the user to select either LPT1 or LPT2 to control the evaluation board.

Help Menu

The version number of the software appears in Help About.

Contact Silicon Laboratories directly for evaluation software support.

Schematics and Layouts

Table 5. Guide to Schematics and Layouts

Evaluation Kit	Device	Schematic Figures	Layout Figures
Si4133-EVB	Si4133-BT	Figures 11 and 12	Figures 21 through 25
Si4133M-EVB	Si4133-BM	Figures 13 and 14	Figures 26 through 30
Si4133G-EVB	Si4133G-BT	Figures 11 and 12	Figures 21 through 25
Si4133GM-EVB	Si4133G-BM	Figures 13 and 14	Figures 26 through 30
Si4133GT2-EVB	Si4133G-XT2	Figures 11 and 12	Figures 21 through 25
Si4133GM2-EVB	Si4133G-XM2	Figures 13 and 14	Figures 26 through 30
Si4113GX5-EVB	Si4113GX5-BM	Figures 15 and 16	Figures 31 through 35
Si4114G-EVB	Si4114G-BM	Figures 15 and 16	Figures 31 through 35
Si4135M-EVB	Si4135-BM	Figures 17 and 18	Figures 36 through 40
Si4136-EVB	Si4136-BT	Figures 19 and 20	Figures 41 through 45

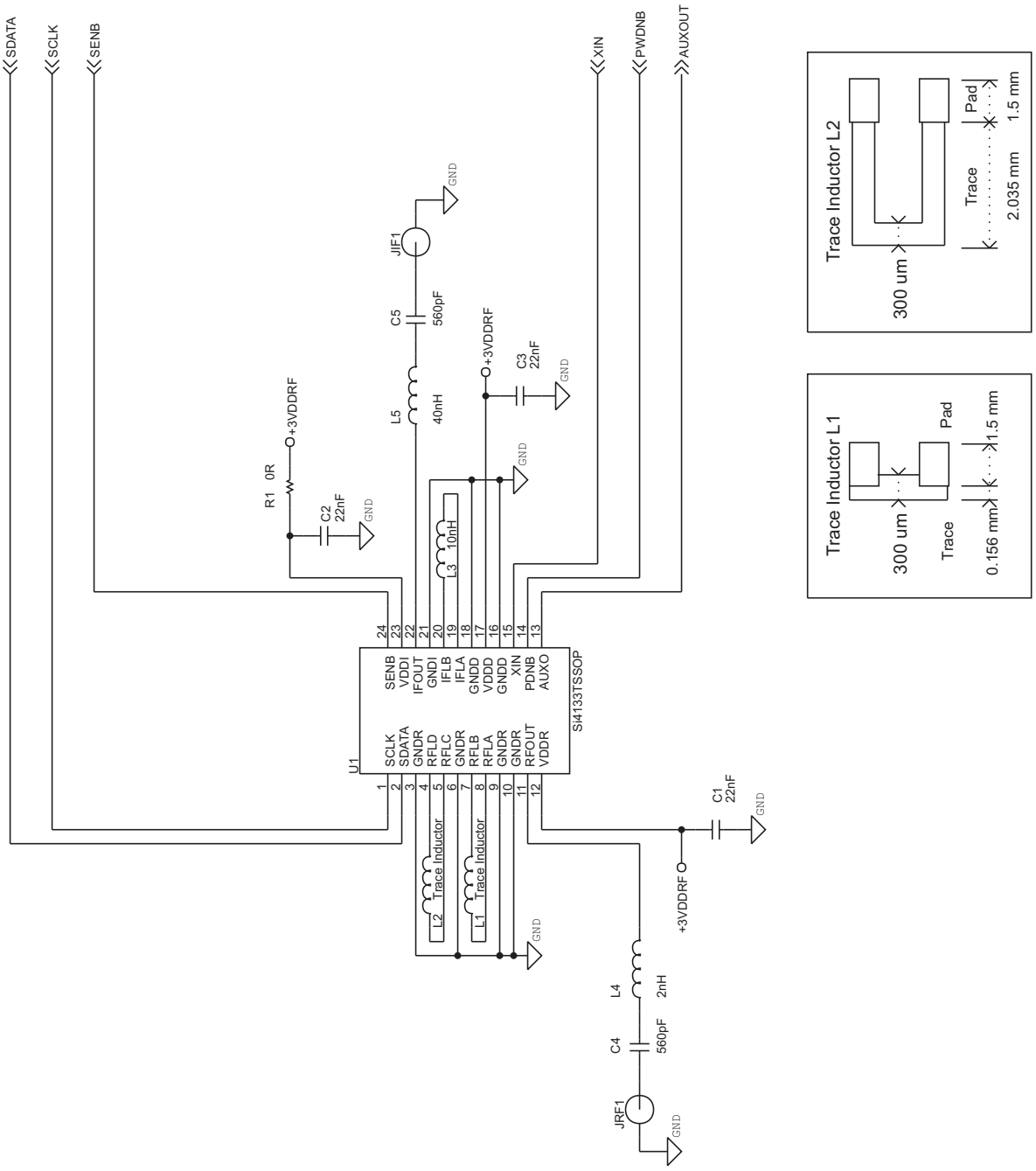


Figure 11. Si4133 TSSOP (1 of 2)

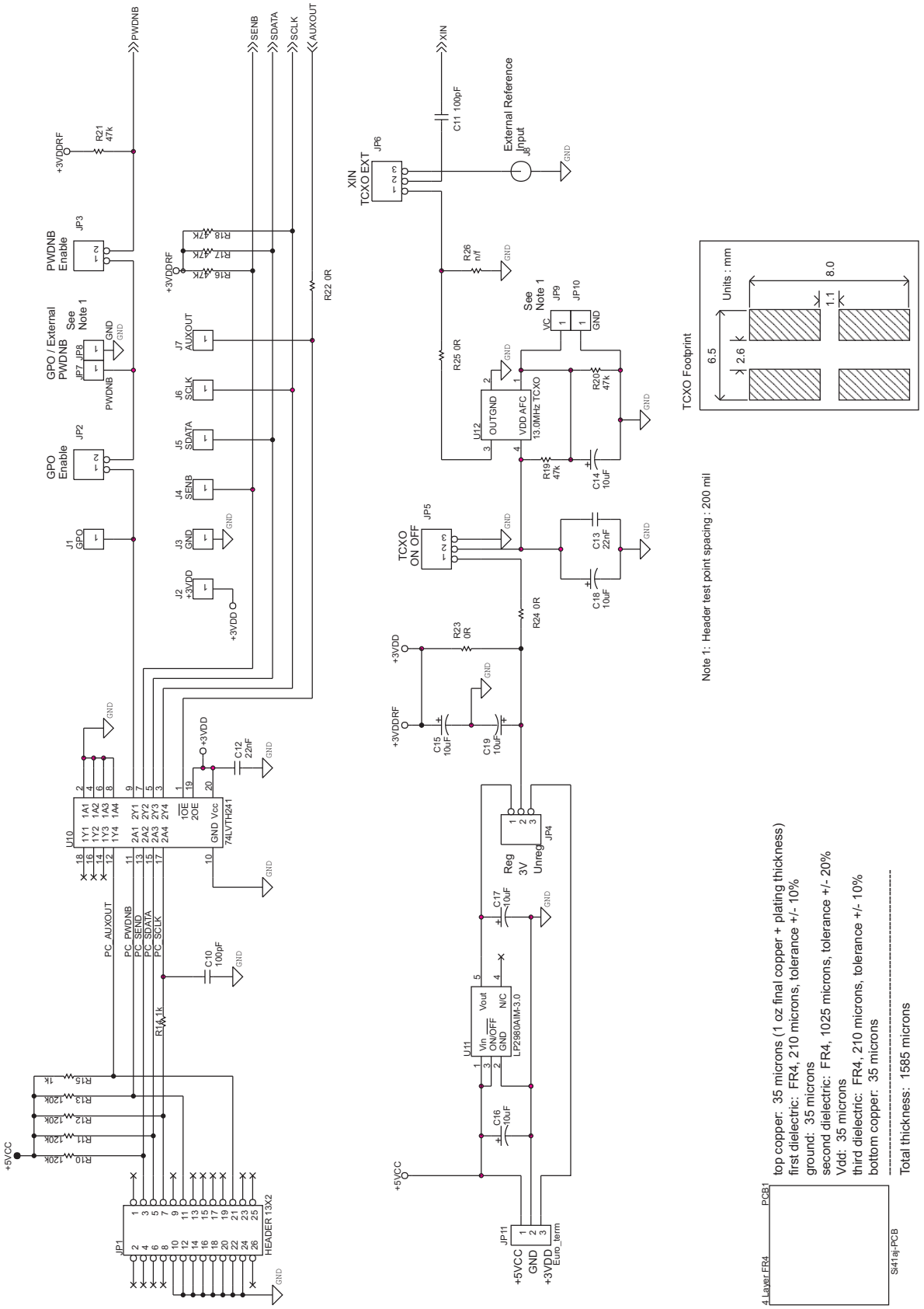


Figure 12. Si4133 TSSOP (2 of 2)

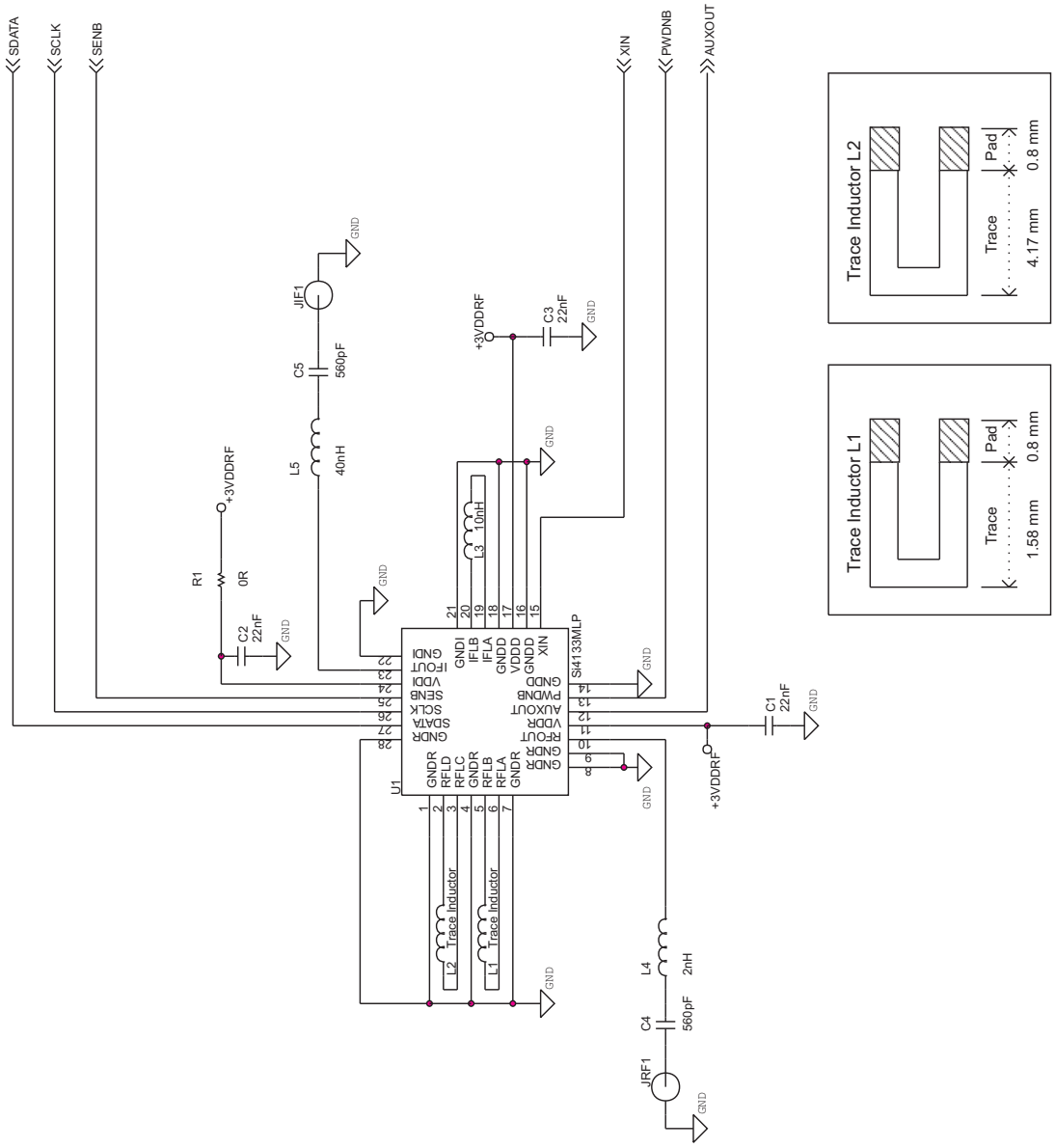


Figure 13. Si4133 MLP (1 of 2)

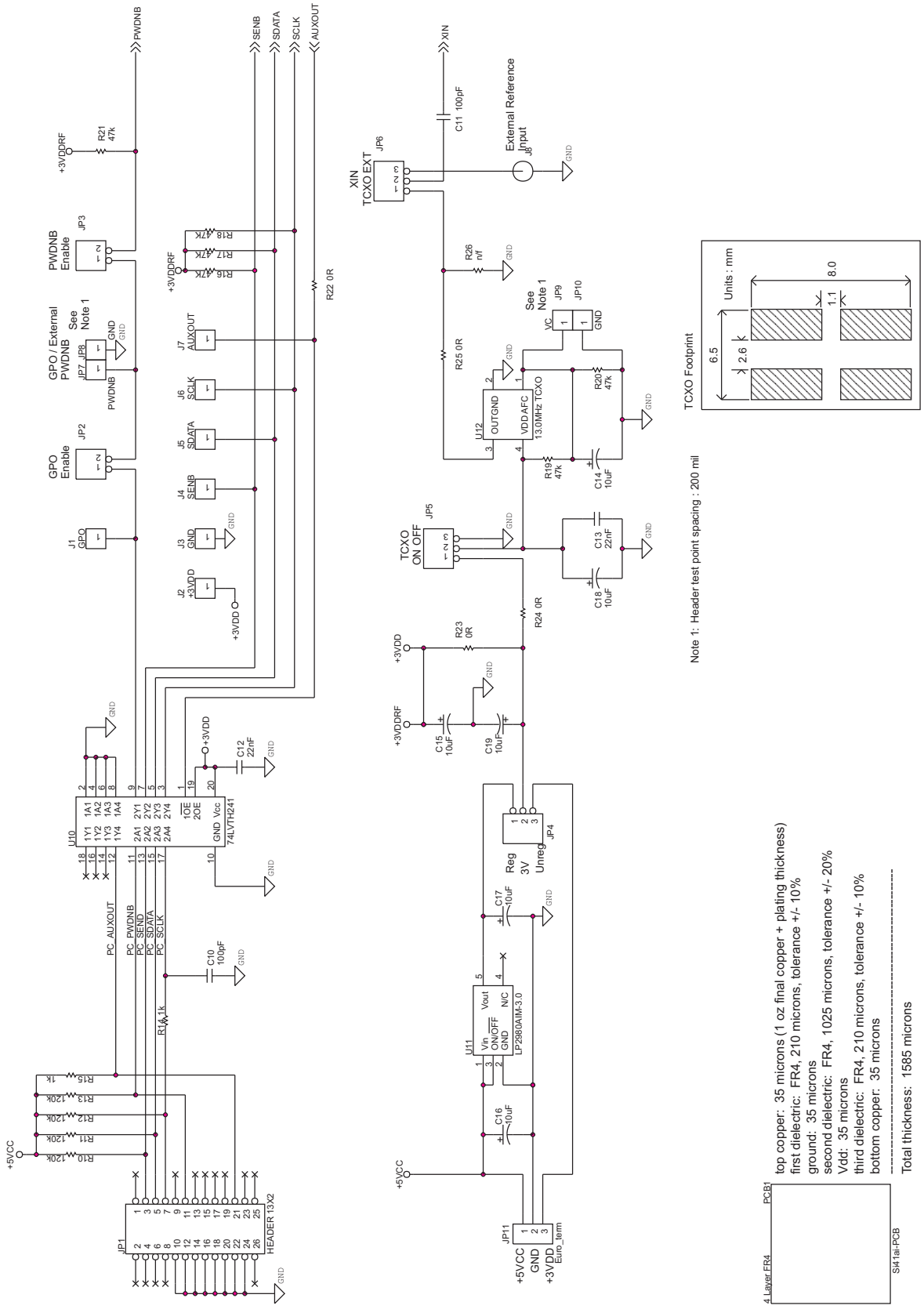


Figure 14. Si4133 MLP (2 of 2)

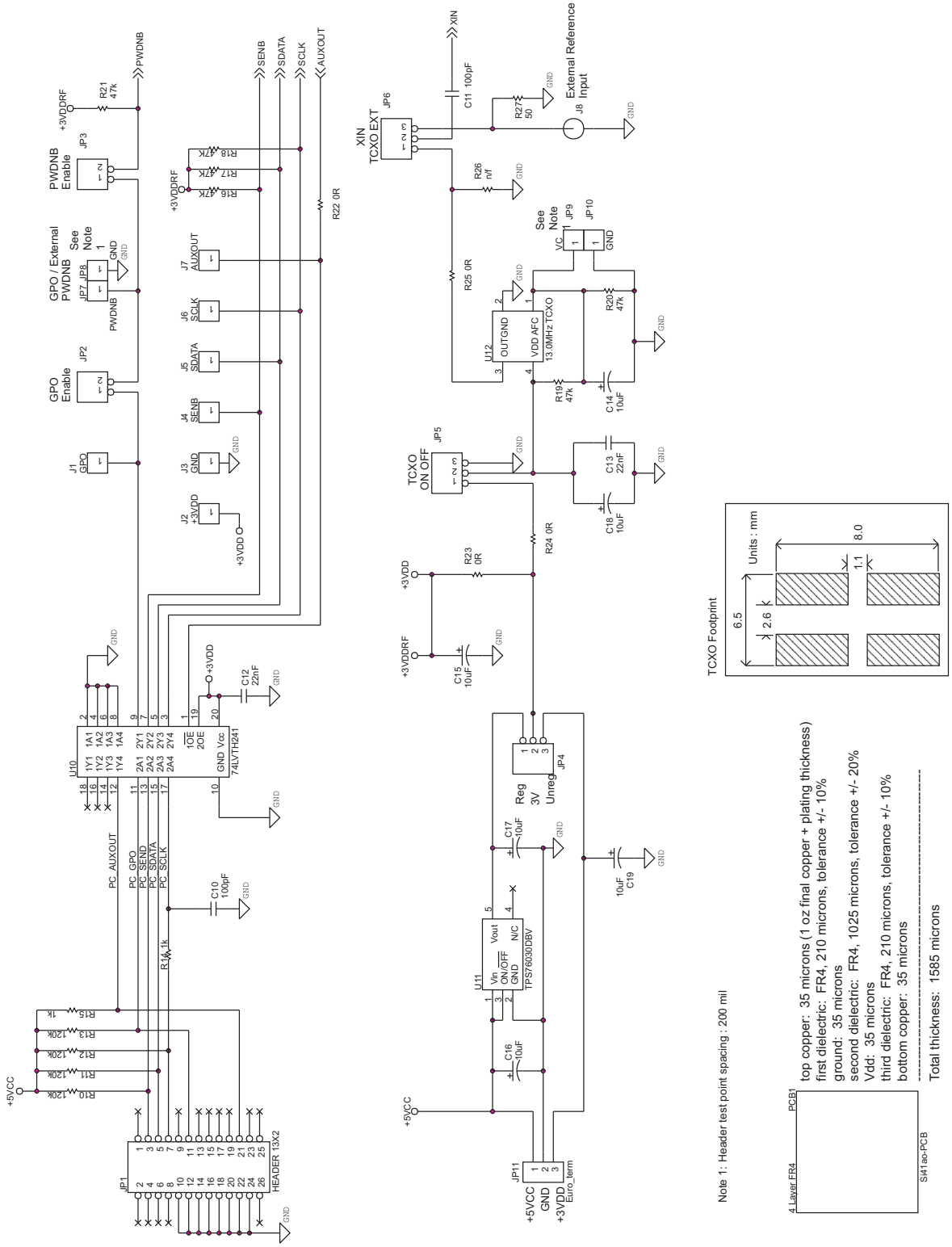


Figure 15. Si4113GX5 MLP (1 of 2)

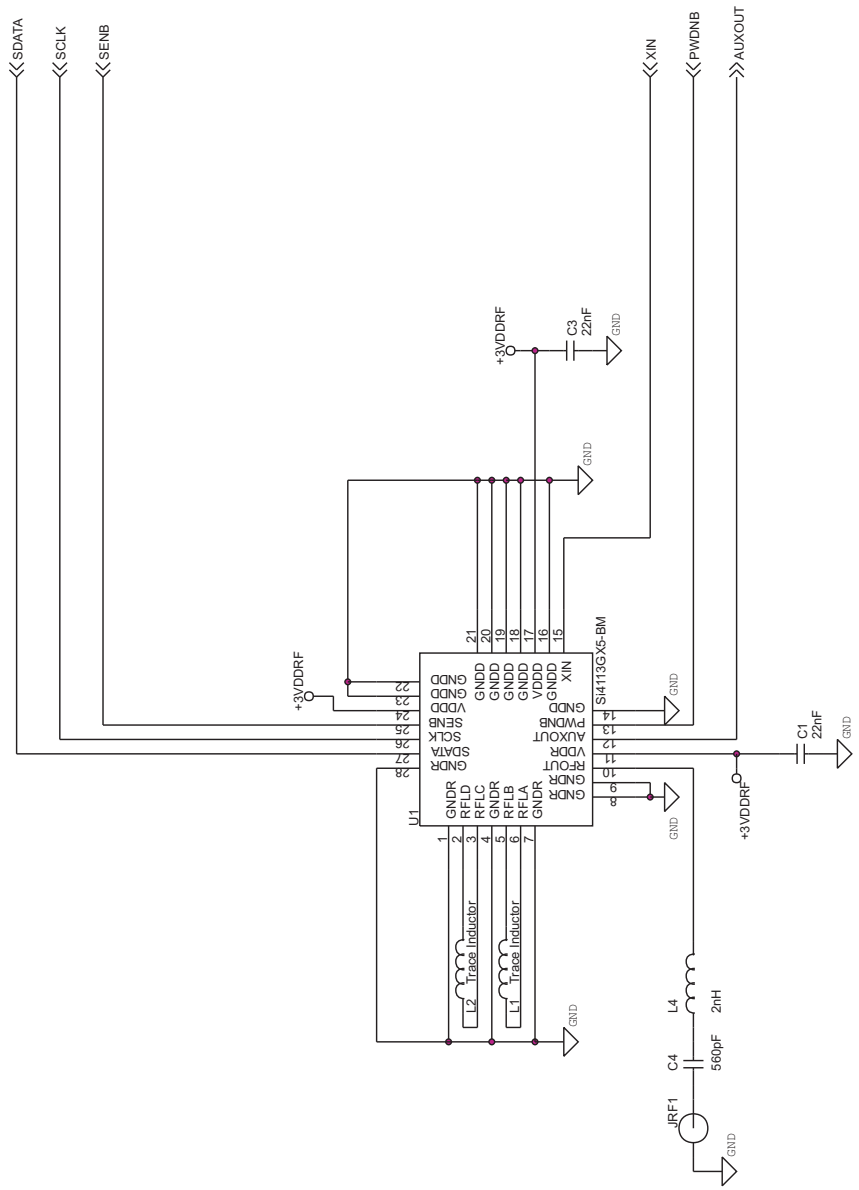


Figure 16. Si4113GX5 MLP (2 of 2)

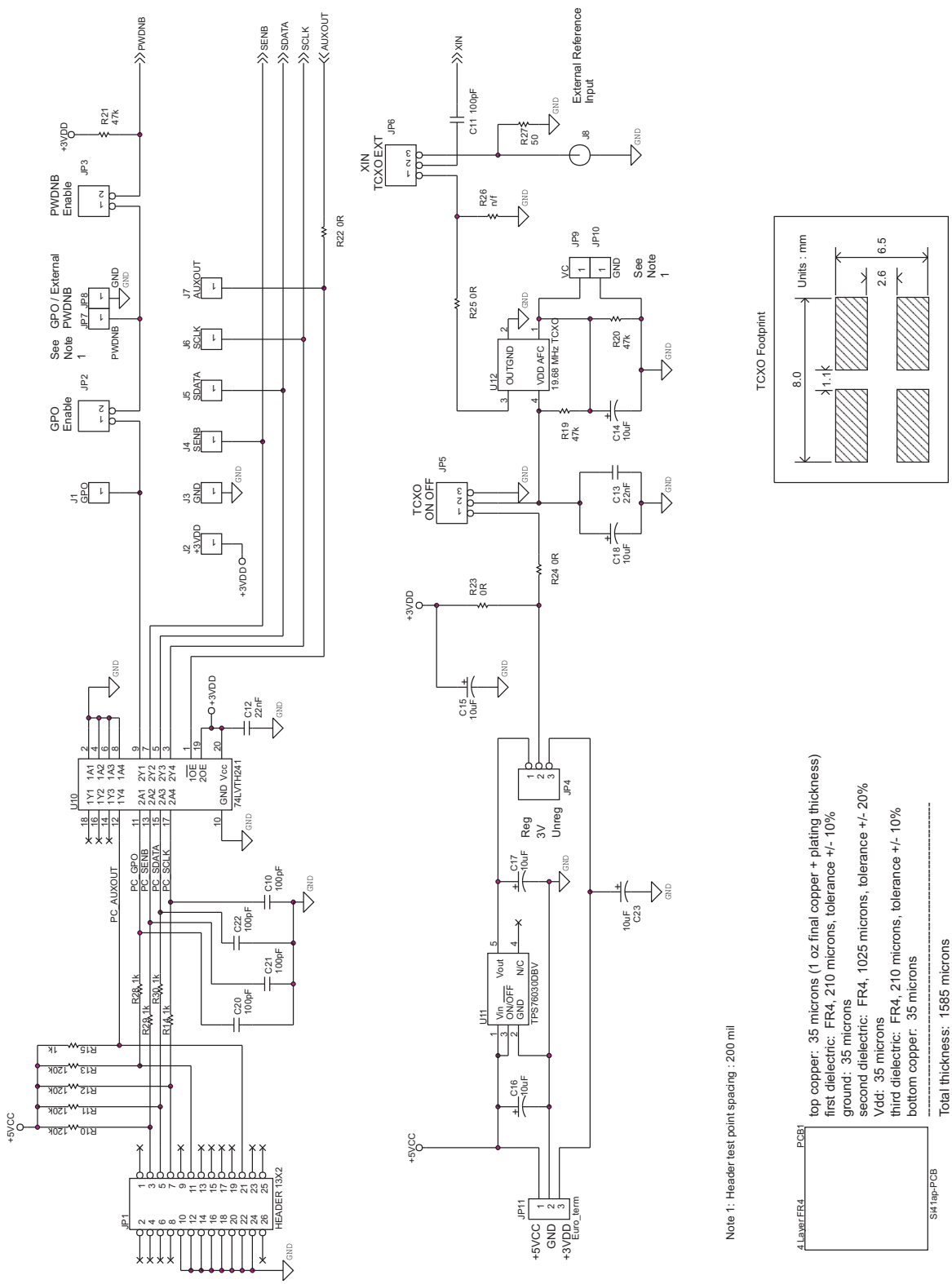


Figure 17. Si4135 MLP (1 of 2)

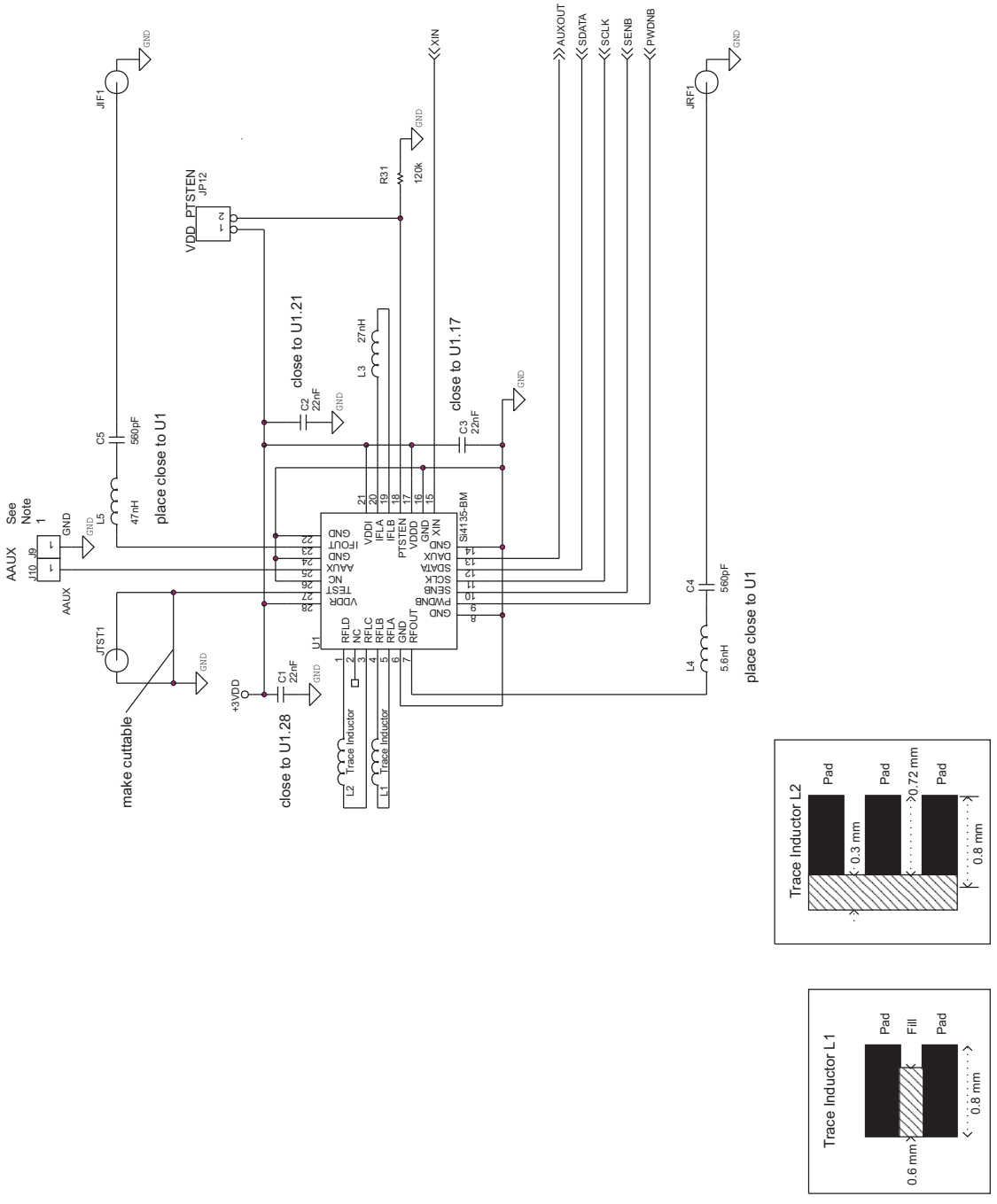


Figure 18. Si4135 MLP (2 of 2)

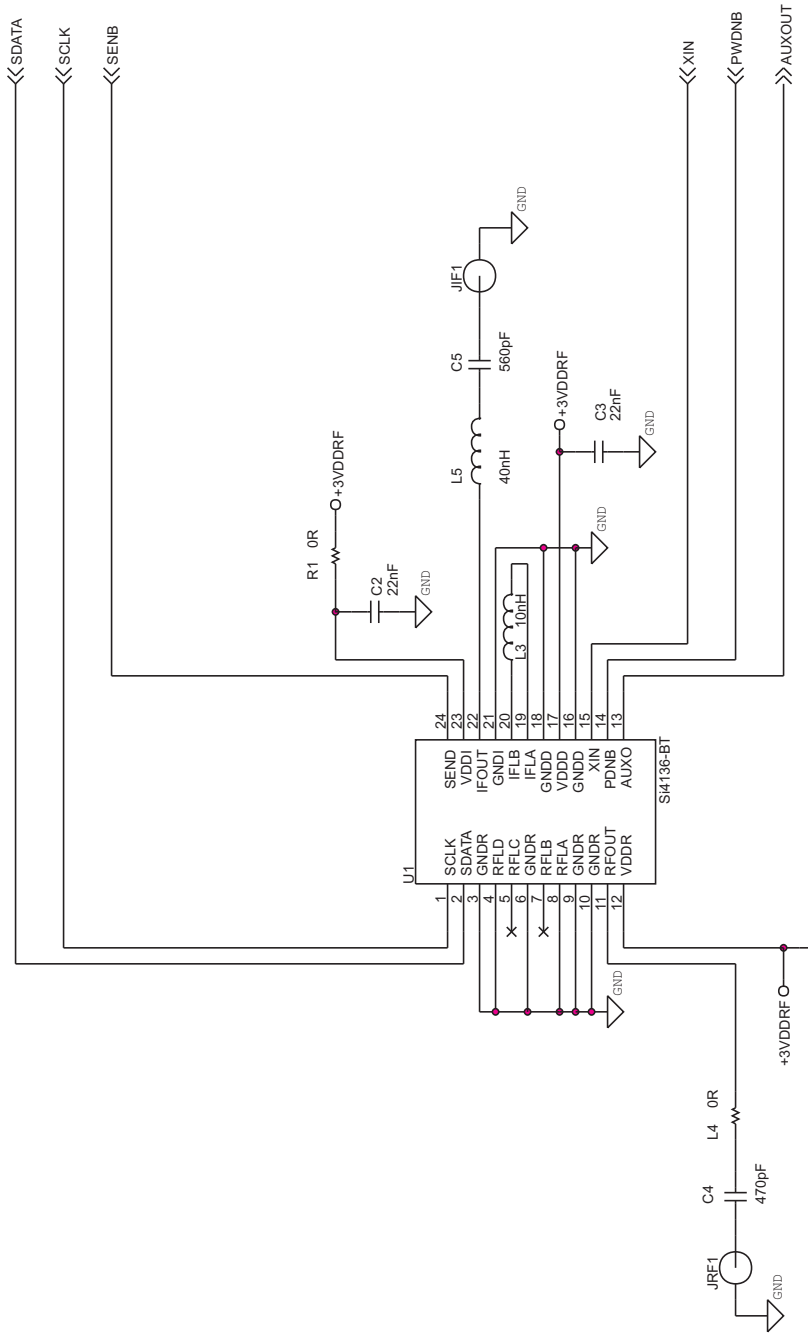


Figure 19. Si4136 TSSOP (1 of 2)

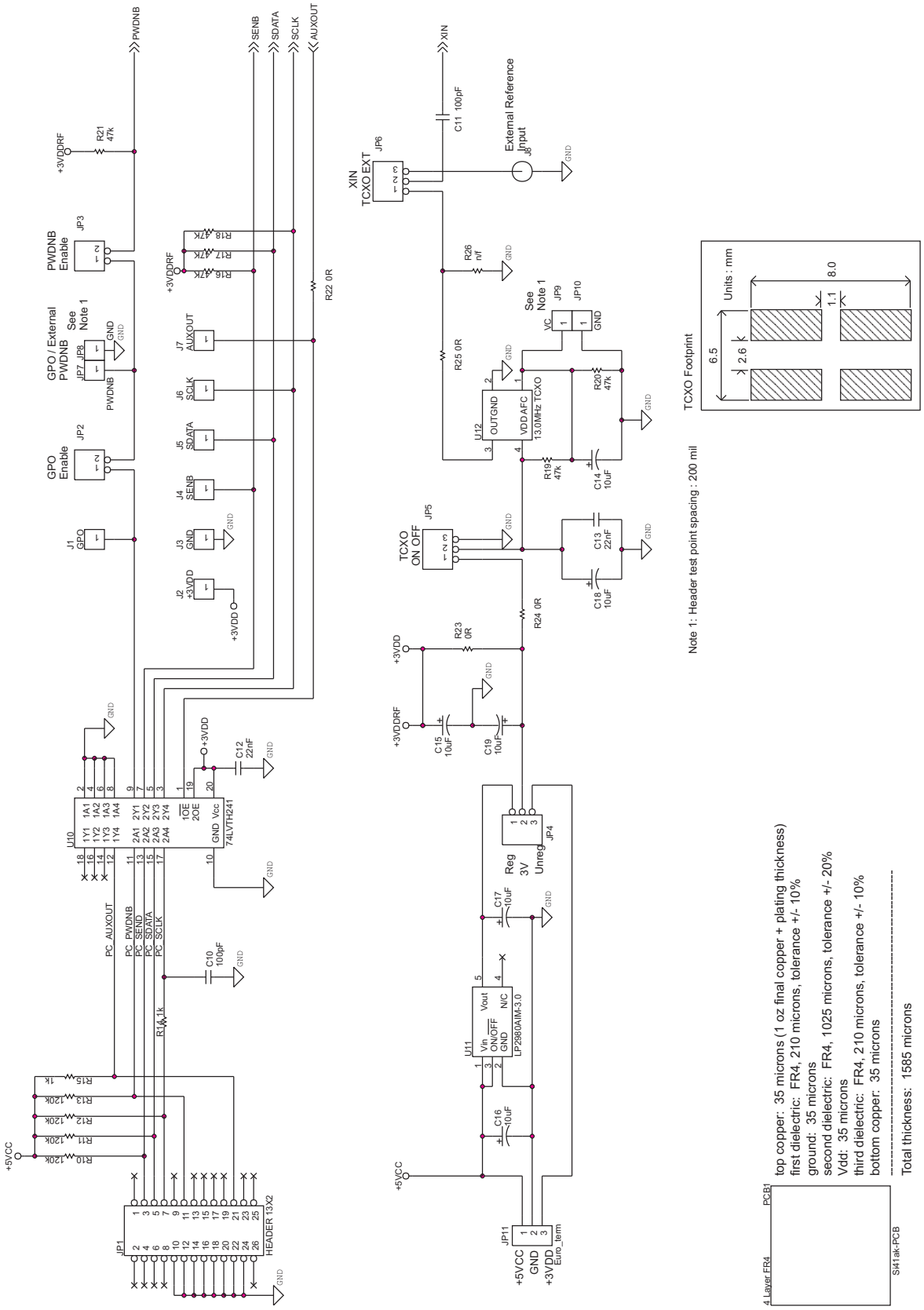


Figure 20. Si4136 TSSOP (2 of 2)

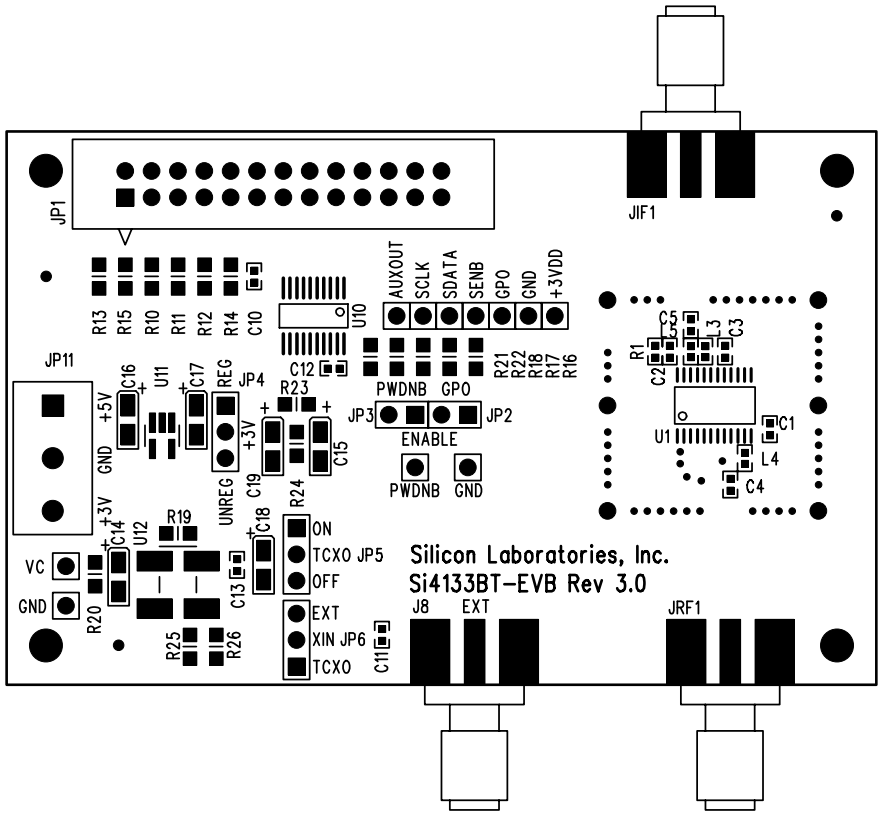


Figure 21. Si4133BT Silkscreen

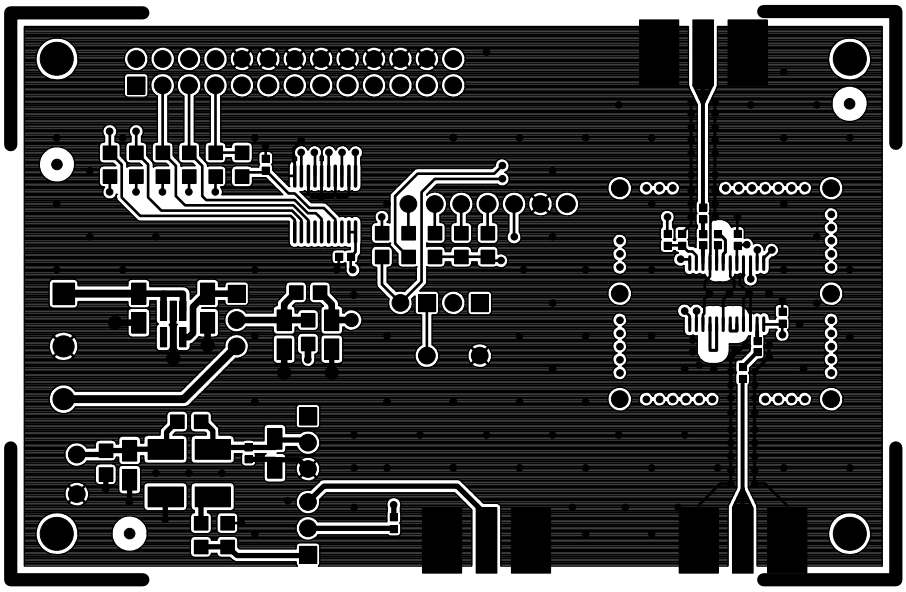


Figure 22. Si4133BT Component

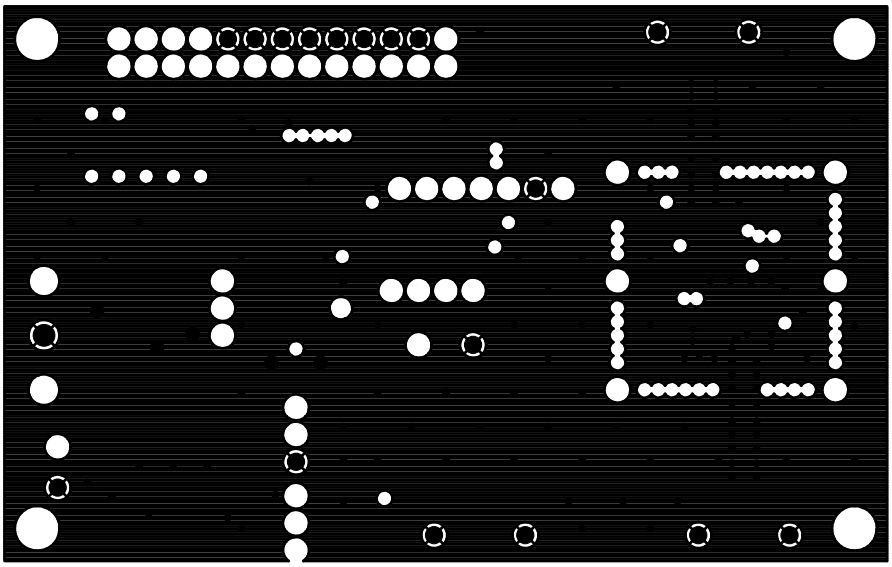


Figure 23. Si4133BT Ground

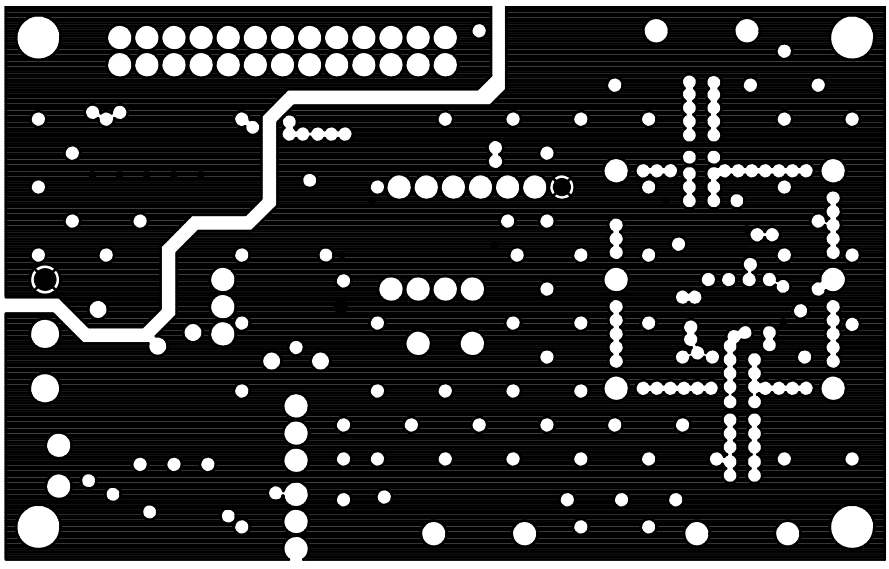


Figure 24. Si4133BT Power

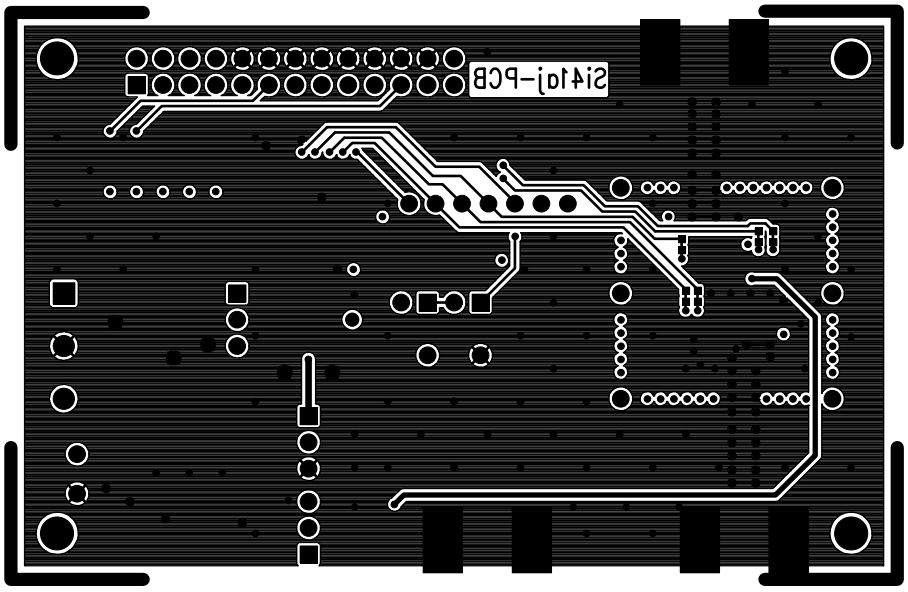


Figure 25. Si4133BT Solder

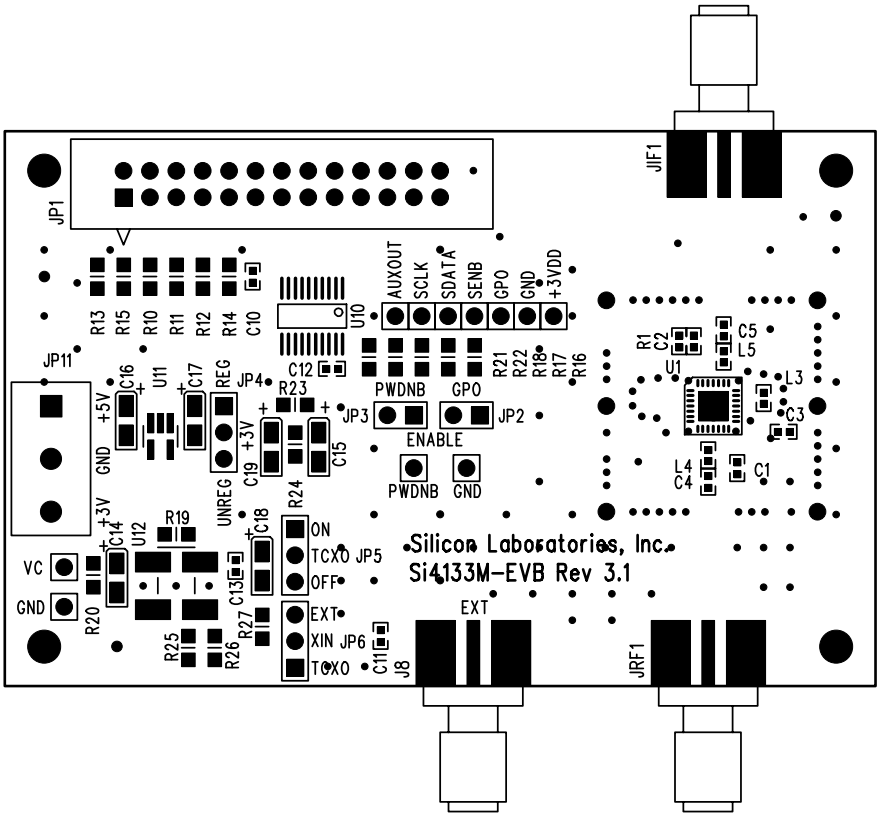


Figure 26. Si4133M Silkscreen

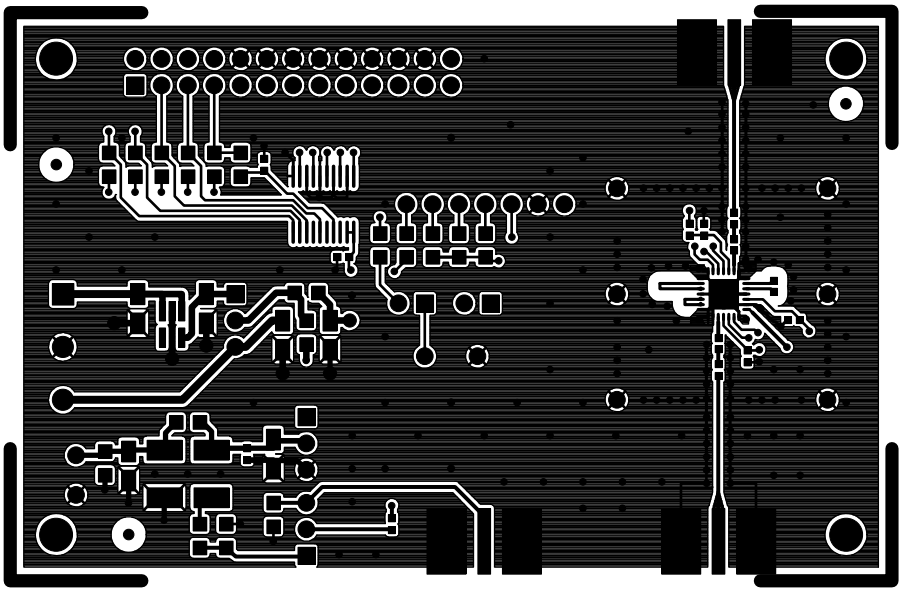


Figure 27. Si4133M Component

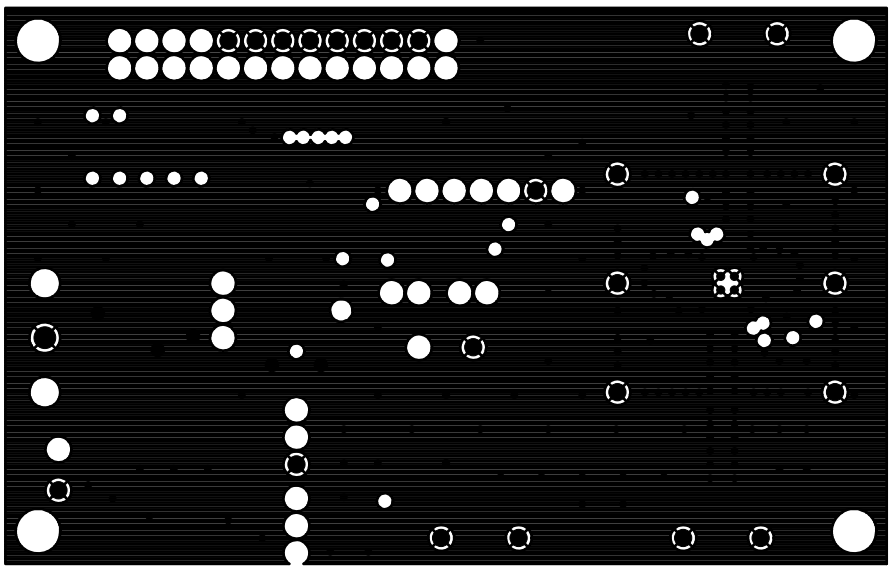


Figure 28. Si4133M Ground

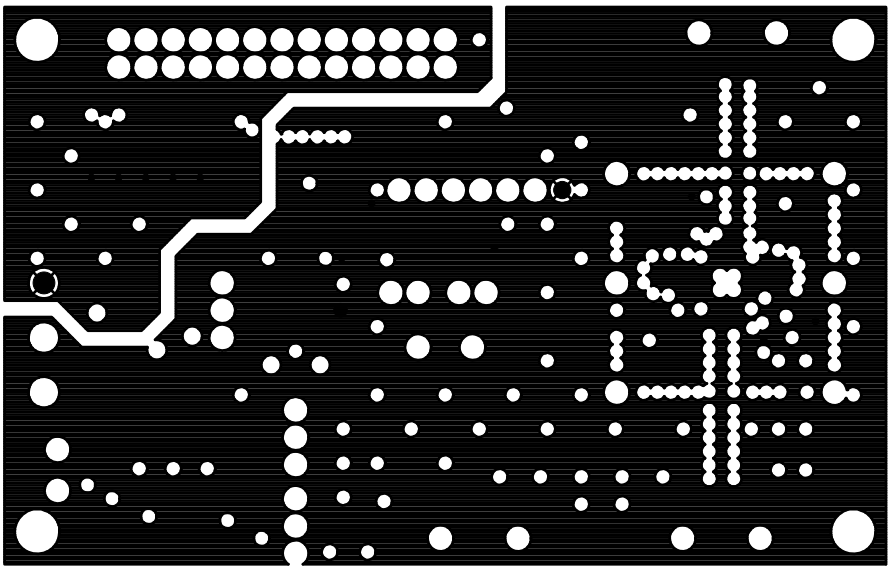


Figure 29. Si4133M Power

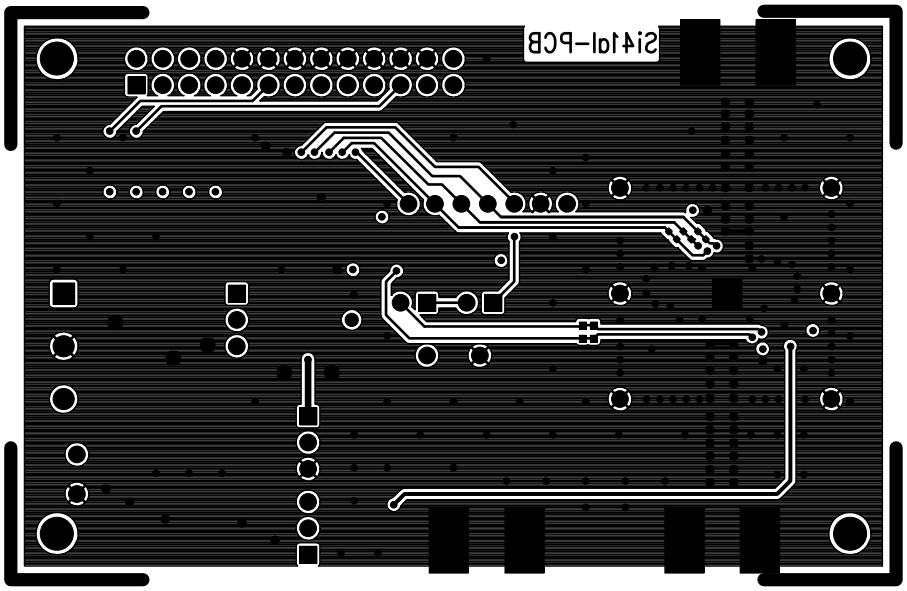


Figure 30. Si4133M Solder

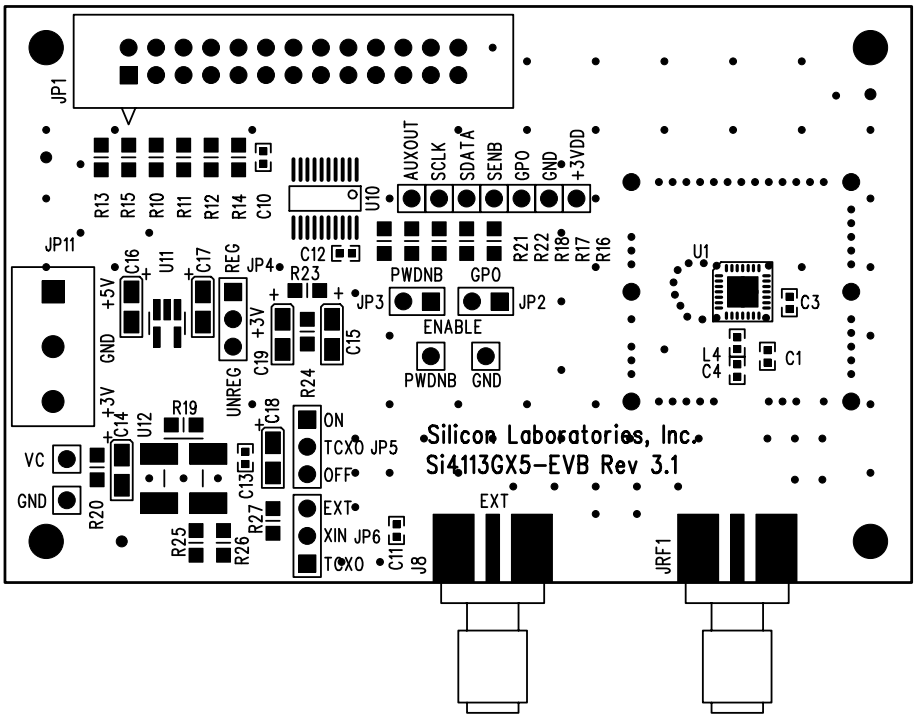


Figure 31. Si4113GX5-BM Silkscreen

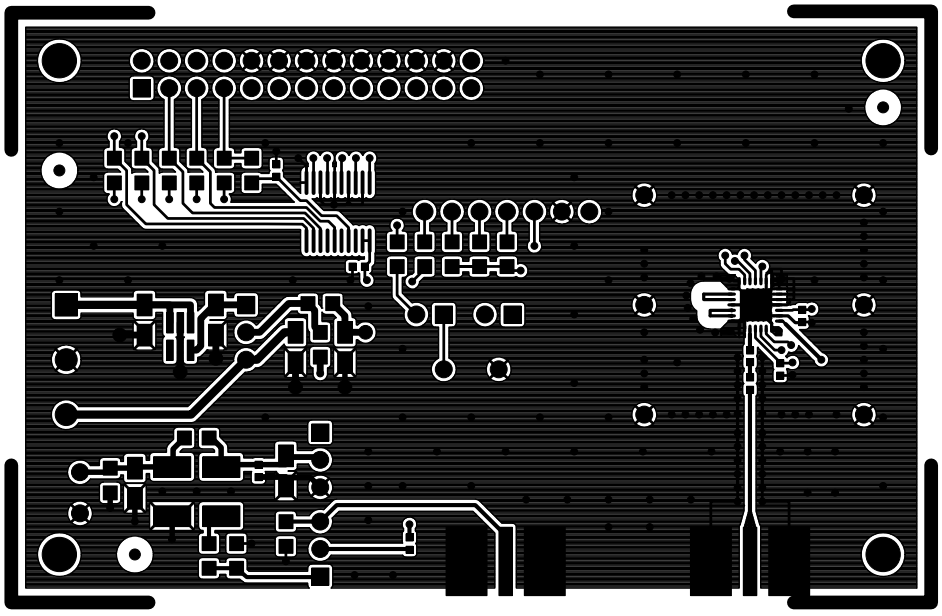


Figure 32. Si4113GX5-BM Component

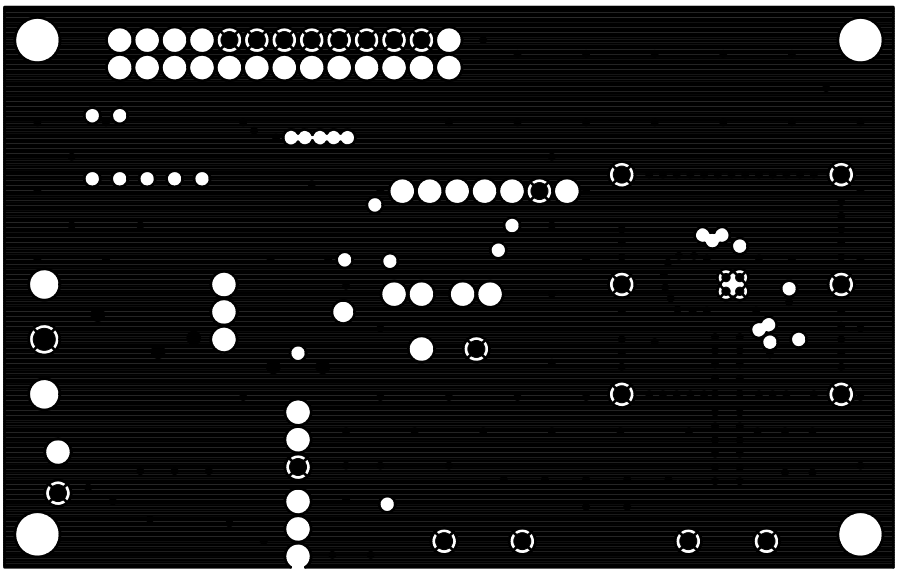


Figure 33. Si4113GX5-BM Ground

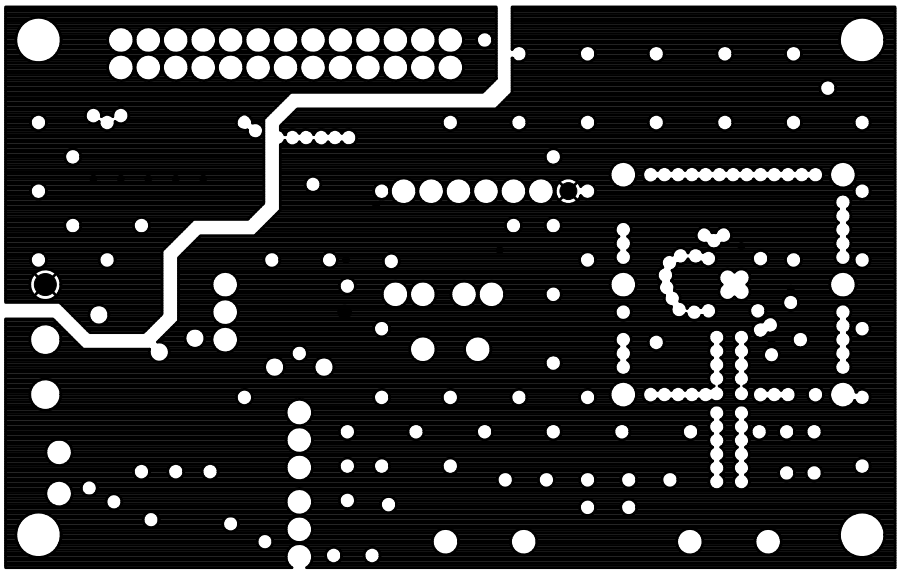


Figure 34. Si4113GX5-BM Power

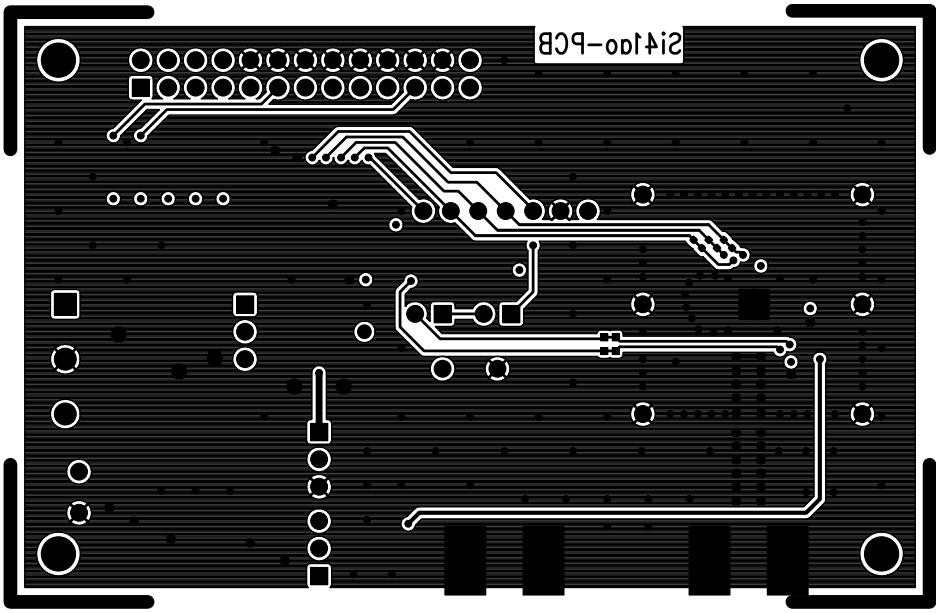


Figure 35. Si4113GX5-BM Solder

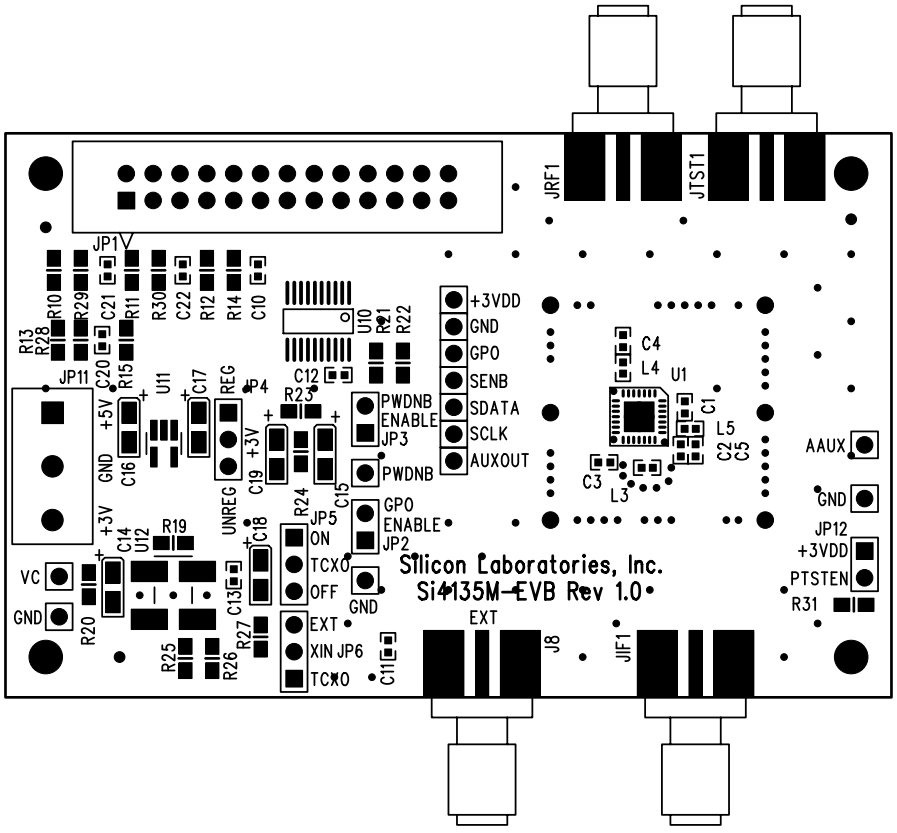


Figure 36. Si4135M Silkscreen

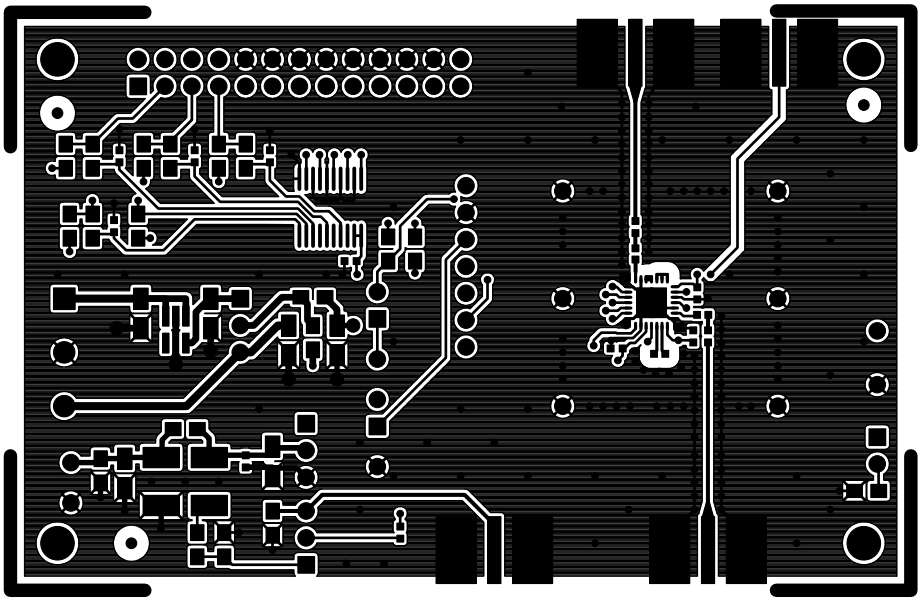


Figure 37. Si4135M Component

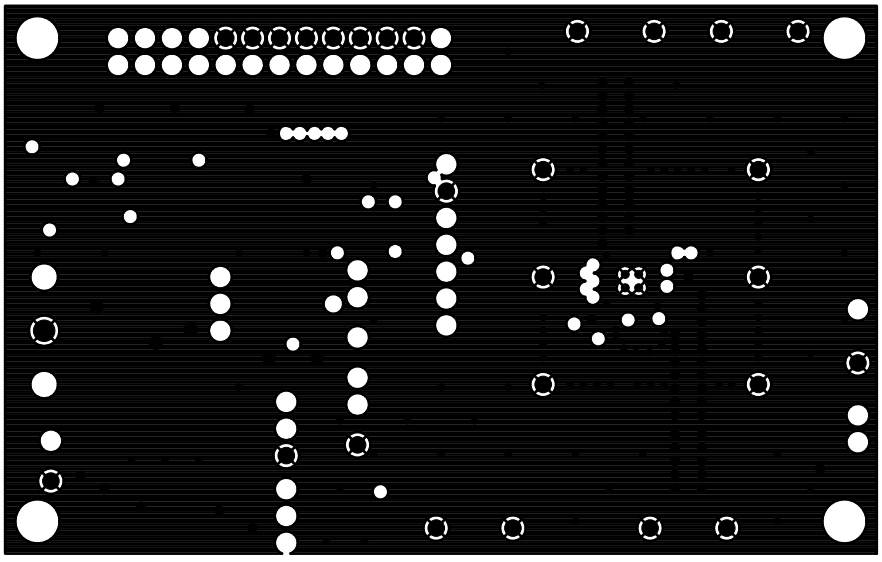


Figure 38. Si4135M Ground

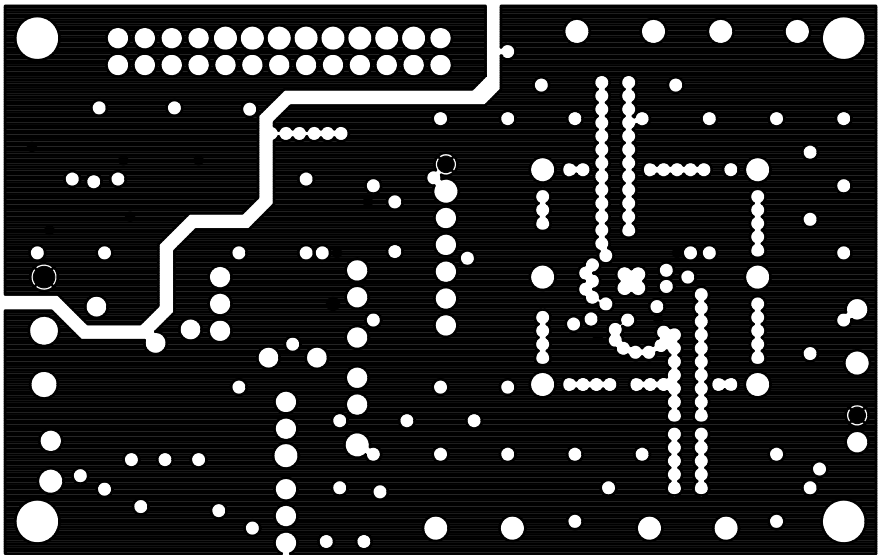


Figure 39. Si4135M Power

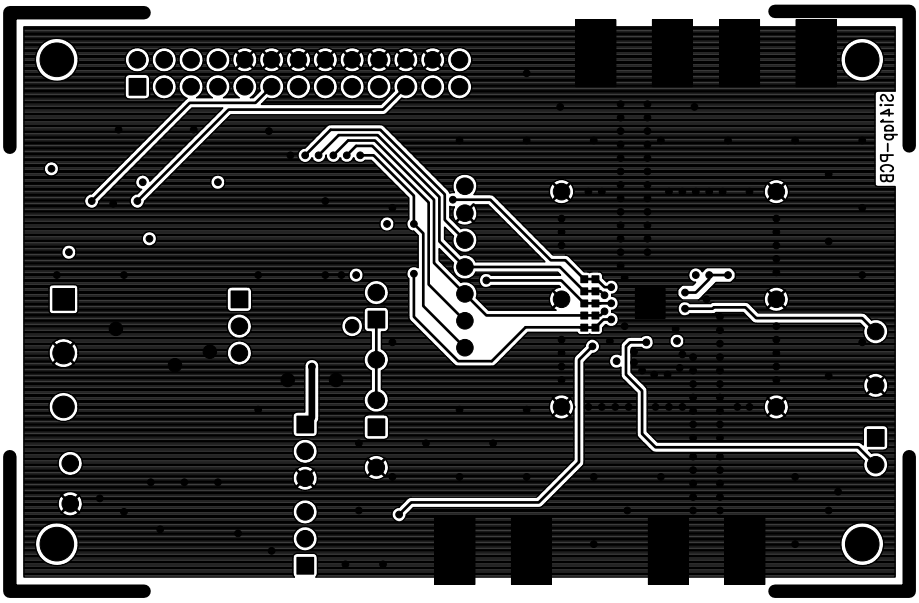


Figure 40. Si4135M Solder

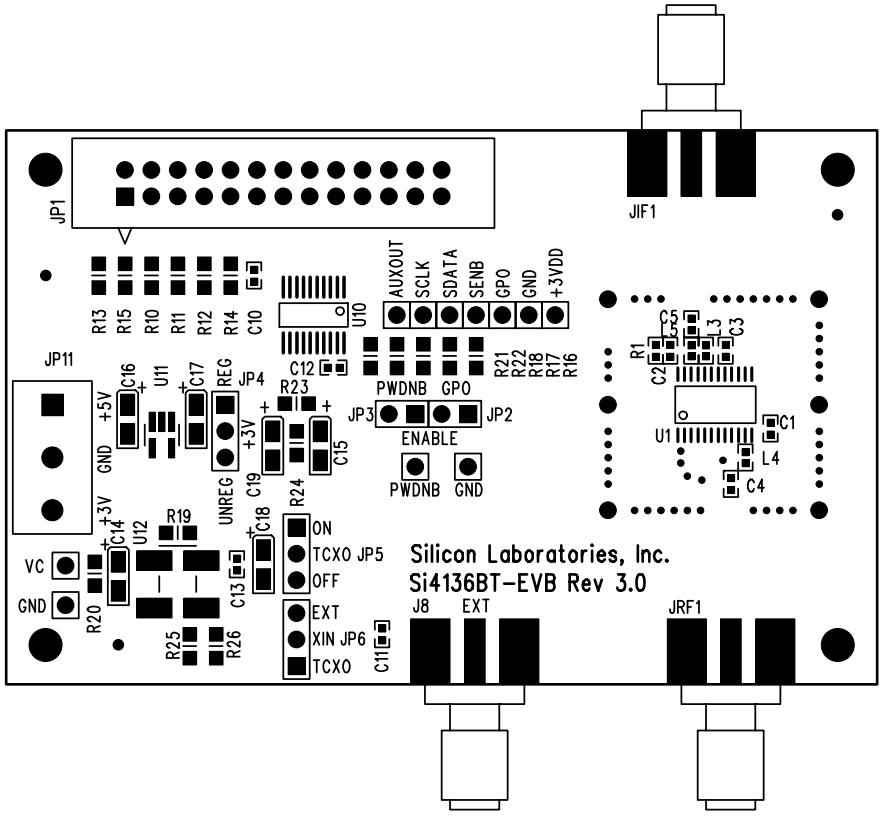


Figure 41. Si4136BT Silkscreen

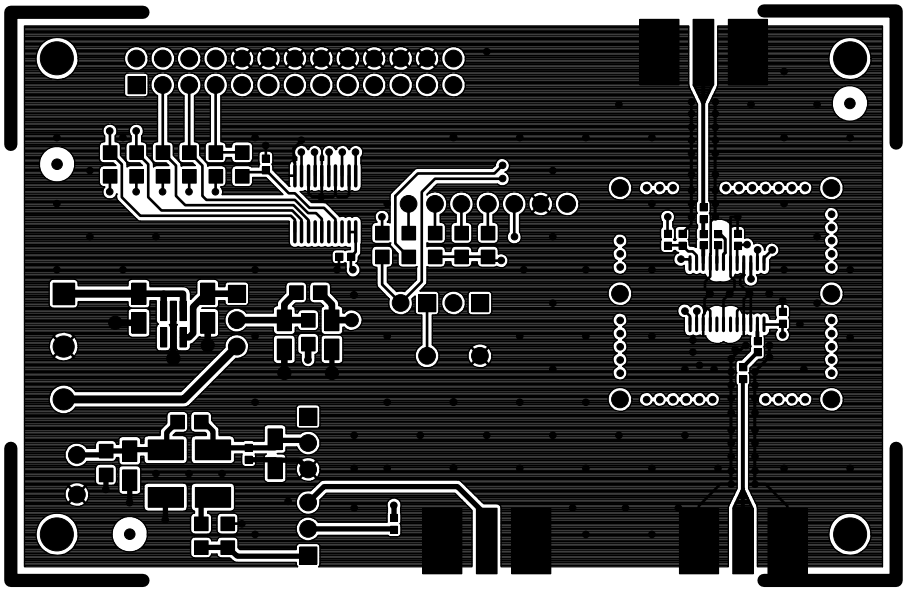


Figure 42. Si4136BT Component

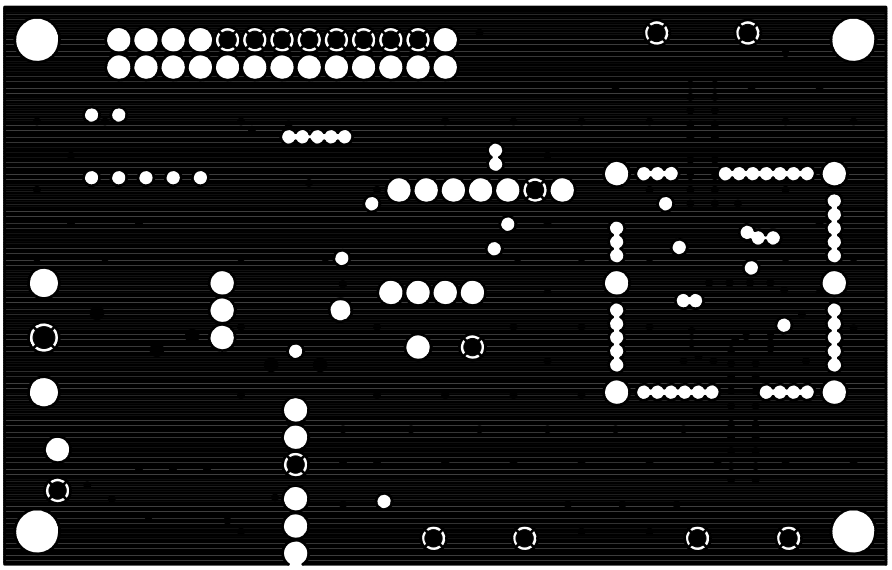


Figure 43. Si4136BT Ground

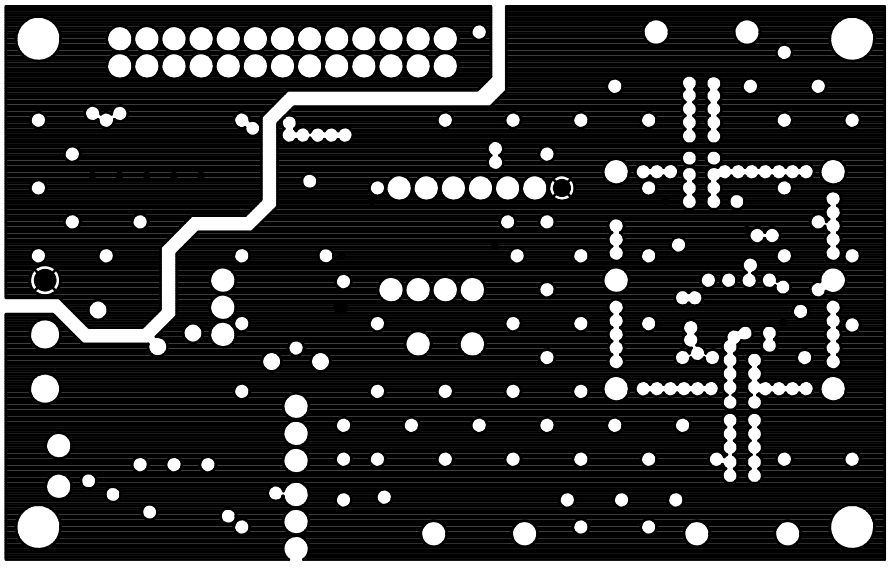


Figure 44. Si4136BT Power

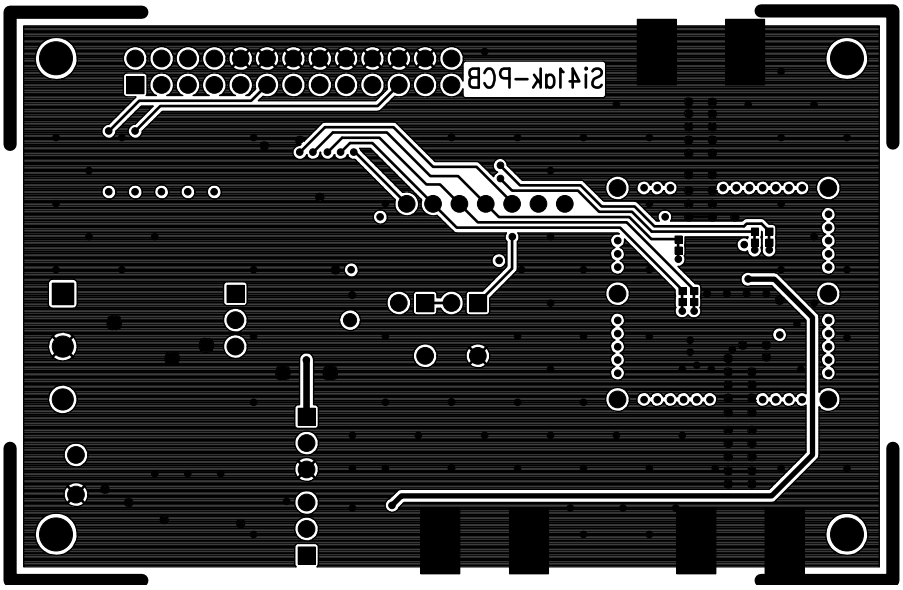


Figure 45. Si4136BT Solder

Bill of Materials

Reference	Part							
	Value	Dielectric	Tolerance	Working Voltage/ Power	Number	Vendor	Package	Note
C1,C2*,C3,C12,C13	22nF	X7R	20%	25V	C0402X7R250-223MNE	Venkel	0402	1
C4,C5 *	560pF	X7R	10%	50V	C0402X7R500-561KNE	Venkel	0402	1
C10,C11	100pF	COG	5%	50V	C0402COG500-101JNE	Venkel	0402	1
C14,C15,C16,C17,C18,C19	10uF	X7R	10%	10V	C1206X7R100-106KNE	Venkel	Case A	1
JRF1,JIF1*,J8	SMA_E	--	--	--	RA2EJ2-6G	Y-Connect	SMA_E	1
JP1	HEADER 13X2	--	--	--	13x2 pin Header with Shroud	Mouser	13x2_0.100_in	1
JP2,JP3	HEADER 2	--	--	--	68000-402	Berg	2x1 100 mil	1
JP4,JP5,JP6	HEADER 3	--	--	--	68000-402	Berg	3x1 100mil	1
JP7	PWDNB	--	--	--	040/SO1BK2F	Oxley	TP_1	1
JP8	GND	--	--	--	040/SO1BK2F	Oxley	TP_1	1
JP9	VC	--	--	--	not installed	--	TP_1	1
J3,JP10	GND	--	--	--	not installed	--	TP_1	1
JP11	Euro_term	--	--	--	MKDSN 1,5/3	Phoenix Contact	through_3	1
J1	GPO	--	--	--	not installed	--	TP_1	1
J2	+3VDD	--	--	--	not installed	--	TP_1	1
J4	SENB	--	--	--	not installed	--	TP_1	1
J5	SDATA	--	--	--	not installed	--	TP_1	1
J6	SCLK	--	--	--	not installed	--	TP_1	1
J7	AUXOUT	--	--	--	not installed	--	TP_1	1
L1	Trace Inductor	--	--	--	--	--	--	2-7
L2	Trace Inductor	--	--	--	--	--	--	2-8
L3	10nH	--	5%	100V	0402CS-10NXJBX	Coilcraft	0402	2-5, 8
L3	0R	--	--	.063W	CR0402-16W-000T	Venkel	0402	6-7
L4	2nH	--	5%	100V	0402CS-2N0XJBX	Coilcraft	0402	2-7, 9
L4	0R	--	--	.063W	CR0402-16W-000T	Venkel	0402	9
L5	40nH	--	5%	100V	0402CS-40NXJBX	Coilcraft	0402	2-8
R1	0R	--	--	.063W	CR0402-16W-000T	Venkel	0402	2-8
R10,R11,R12,R13	120k	--	5%	--	CR0805-10W-124JT	Venkel	0805	1
R14,R15	1k	--	1%	.125W	CR0805-10W-1001FT	Venkel	0805	1
R16,R17,R18,R19,R20,R21	47k	--	5%	--	CR0805-10W-473JT	Venkel	0805	1
R22,R23,R24,R25	0R	--	--	.1W	CR0805-10W-000T	Venkel	0805	1
R26	n/f	--	--	--	not installed	--	0805	1
U1	Si4133-BT	--	--	--	Si4133-BT	Silicon Labs	TSSOP-24	2
U1	Si4133-BM	--	--	--	Si4133-BM	Silicon Labs	MLP-28	3
U1	Si4133G-BT	--	--	--	Si4133G-BT	Silicon Labs	TSSOP-24	4
U1	Si4133G-BM	--	--	--	Si4133G-BM	Silicon Labs	MLP-28	5
U1	Si4133G-XT2	--	--	--	Si4133G-XT2	Silicon Labs	TSSOP-24	6
U1	Si4133G-XM2	--	--	--	Si4133G-XM2	Silicon Labs	MLP-28	7
U1	Si4136-BT	--	--	--	Si4136-BT	Silicon Labs	TSSOP-24	8
U1	Si4113G-X5	--	--	--	Si4113G-X5	Silicon Labs	MLP-28	9
U10	74LVTH241	--	--	--	SN74LVTH241PW	Texas Instruments	TSSOP-20	1
U11	TPS76030DBV	--	+/- .75%	16V	TPS76030DBV	Texas Instruments	5L-SOT-23	1
U12	13.0MHz TCXO	--	2.5ppm	3V	RTVY-174-13.0MHz	Raltron	TXCO	1

Notes:

- ***** Not used on the Si4113GX5-EVB.
- **1.** Used on all evaluation boards.
- **2.** Used on the Si4133-EVB.
- **3.** Used on the Si4133M-EVB.
- **4.** Used on the Si4133G-EVB.
- **5.** Used on the Si4133GM-EVB.
- **6.** Used on the Si4133GT2-EVB.
- **7.** Used on the Si4133GM2-EVB.
- **8.** Used on the Si4136-EVB.
- **9.** Used on the Si4113GX5-EVB.

Ordering Guide

Ordering Part Number	Description
Si4133 Family (TSSOP)	
Si4133-EVB	Evaluation Board with Si4133-BT (TSSOP) and Evaluation Kit (PC parallel port cable, evaluation software on CD-ROM, and documentation)
Si4123-EVB	Si4133-EVB with Si4123-BT Sample Kit
Si4122-EVB	Si4133-EVB with Si4122-BT Sample Kit
Si4113-EVB	Si4133-EVB with Si4113-BT Sample Kit
Si4112-EVB	Si4133-EVB with Si4112-BT Sample Kit
Si4133 Family (MLP)	
Si4133M-EVB	Evaluation Board with Si4133-BM (MLP) and Evaluation Kit
Si4123M-EVB	Si4133M-EVB with Si4123-BM Sample Kit
Si4122M-EVB	Si4133M-EVB with Si4122-BM Sample Kit
Si4113M-EVB	Si4133M-EVB with Si4113-BM Sample Kit
Si4112M-EVB	Si4133M-EVB with Si4112-BM Sample Kit
Si4133G Family (TSSOP)	
Si4133G-EVB	Evaluation Board with Si4133G-BT (TSSOP) and Evaluation Kit
Si4123G-EVB	Si4133G-EVB with Si4123G-BT Sample Kit
Si4122G-EVB	Si4133G-EVB with Si4122G-BT Sample Kit
Si4113G-EVB	Si4133G-EVB with Si4113G-BT Sample Kit
Si4112G-EVB	Si4133G-EVB with Si4112G-BT Sample Kit
Si4133G Family (MLP)	
Si4133GM-EVB	Evaluation Board with Si4133G-BM (MLP) and Evaluation Kit
Si4123GM-EVB	Si4133GM-EVB with Si4123G-BM Sample Kit
Si4122GM-EVB	Si4133GM-EVB with Si4122G-BM Sample Kit
Si4113GM-EVB	Si4133GM-EVB with Si4113G-BM Sample Kit
Si4112GM-EVB	Si4133GM-EVB with Si4112G-BM Sample Kit
Si4133G-XT2 (TSSOP)	
Si4133GT2-EVB	Evaluation Board with Si4133G-XT2 (TSSOP) and Evaluation Kit
Si4133G-XM2 (MLP)	
Si4133GM2-EVB	Evaluation Board with Si4133G-XM2 (MLP) and Evaluation Kit
Si4133G-X5 (MLP)	
Si4113GX5-EVB	Evaluation Board with Si4113GX5-BM (MLP) and Evaluation Kit
Si4135 (MLP)	
Si4135M-EVB	Evaluation Board with Si4135-BM (MLP) and Evaluation Kit

Document Change List

Revision 0.5 to Revision 0.6

- Removed references to Si4133W.

Notes:

Contact Information

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