I²C bus SERIAL INTERFACE REAL-TIME CLOCK IC WITH VOLTAGE MONITORING FUNCTION

RV5C387A

NO.EA-080-100928

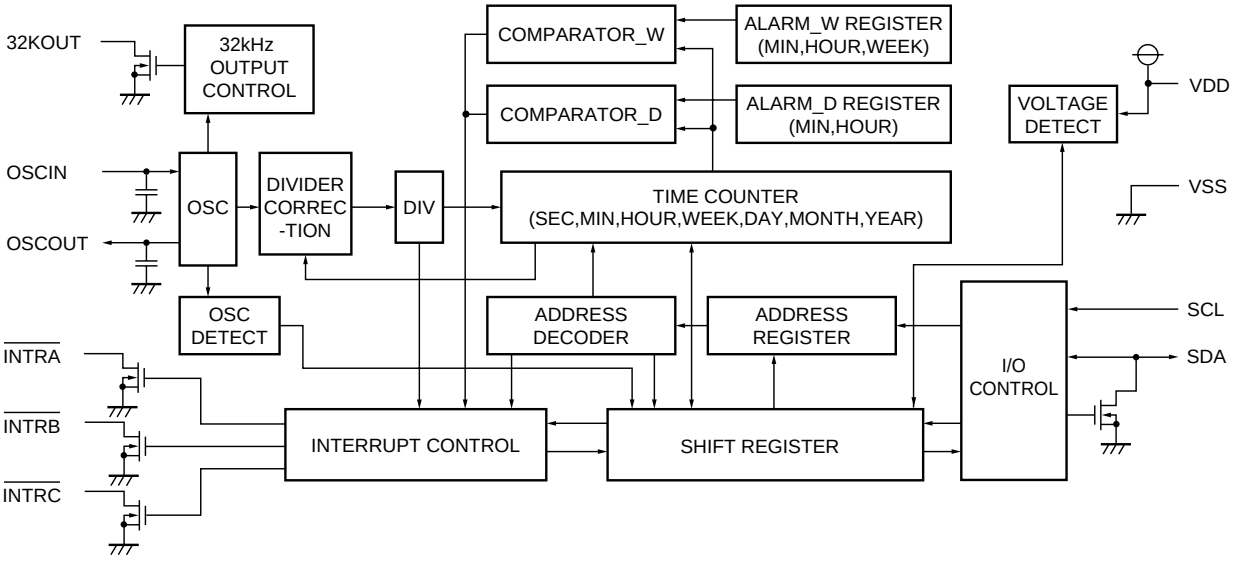
OUTLINE

The RV5C387A is a CMOS real-time clock IC connected to the CPU by two signal, SCL and SDA, and configured to perform serial transmission of time and calendar data to the CPU. The periodic interrupt circuit is configured to generate interrupt signals with six selectable interrupts ranging from 0.5 seconds to 1 month. The 2 alarm circuits generate interrupt signals at preset times. The oscillation circuit is driven under constant voltage so that fluctuations in oscillation frequency due to voltage are small and supply current is also small (TYP. 0.35µA for the RV5C387A at 3 volts). The oscillation halt sensing circuit can be used to judge the validity of internal data in such events as power-on. The supply voltage monitoring circuit is configured to record a drop in supply voltage below two selectable supply voltage monitoring threshold settings. The 32-kHz clock output function (Nch. open drain) is intended to output sub-clock pulses for the external microcomputer. The oscillation adjustment circuit is intended to adjust time counts with high precision by correcting deviations in the oscillation frequency of the crystal oscillator. The 32-kHz clock circuit can be disabled by certain register settings. This model comes in an ultra-compact 10-pin SSOP-G (with a height of 1.20mm and a pin pitch of 0.5mm).

FEATURES

- Timekeeping supply voltage ranging from 1.45 to 5.5 volts
- Low supply current: TYP. 0.35µA (MAX. 0.8µA) at 3 volts
- Only two signal lines (SCL, SDA) required for connection to the CPU.
  (I²C bus compatible, 400kHz at V_{DD}≥2.5V, address 7bits)
- Time counters (counting hours, minutes, and seconds) and calendar counters (counting years, months, days, and weeks) (in BCD format)
- 1900/2000 identification bit for Year 2000 compliance
- Interrupt circuit configured to generate interrupt signals (with interrupts ranging from 0.5 seconds to 1 month) to the CPU and provided with an interrupt flag and an interrupt halt circuit
- 2 alarm circuits (Alarm_W for week, hour, and minute alarm settings and Alarm_D for hour and minute alarm settings)
- 32-kHz clock circuit (Nch. open drain output)
- Oscillation halt sensing circuit which can be used to judge the validity of internal data
- Supply voltage monitoring circuit with two supply voltage monitoring threshold settings
- Automatic identification of leap years up to the year 2099
- Selectable 12-hour and 24-hour mode settings
- High precision oscillation adjustment circuit
- Built-in oscillation stabilization capacitors (C_G and C_D)
- CMOS process
- Ultra-compact 10-pin SSOP-G(with a height of 1.20mm and size 4.0mm×2.9mm)

BLOCK DIAGRAM

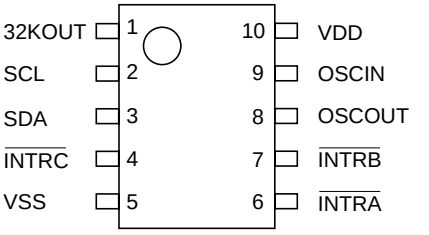


APPLICATIONS

- Communication devices (multi function phone, portable phone, PHS or pager)
- OA devices (fax, portable fax)
- Computer (desk-top and mobile PC, portable word-processor, PDA, electric note or video game)
- AV components (portable audio unit, video camera,camera, digital camera or remote controller)
- Home appliances (rice cooker, electric oven)
- Other (car navigation system, multi-function watch)

PIN CONFIGURATION

• 10-pin SSOP-G



PIN DESCRIPTIONS

Pin No.	Symbol	Item	Description
2	SCL	Serial Clock Line	This pin is used to input shift clock pulses to synchronize data input/output to and from the SDA pin with this clock. Allows a maximum input voltage of 5.5 volts regardless of supply voltage.
3	SDA	Serial Data Line	This pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCL pin. Allows a maximum input voltage of 5.5 volts regardless of supply voltage.
6	$\overline{\text{INTRA}}$	Interrupt Output A	This pin outputs periodic interrupt pulses to the CPU. This pin is off when power is activated from 0V. This pin functions as an Nch open drain output.
7	$\overline{\text{INTRB}}$	Interrupt Output B	This pin outputs alarm interrupt (ALARM_W) to the CPU. This pin is off when power is activated from 0V. This pin functions as an Nch open drain output.
4	$\overline{\text{INTRC}}$	Interrupt Output C	This pin outputs alarm interrupt (ALARM_D) to the CPU. This pin is off when power is activated from 0V. This pin functions as an Nch open drain output.
1	32KOUT	32-kHz Clock Output	The 32KOUT pin is used to output 32.768-kHz clock pulses. Enabled at power-on from 0 volts. Nch. open drain output. The RV5C387A is designed to be disable 32-kHz clock output in response to a command from the host computer.
9 8	OSCIN OSCOUT	Oscillatory Circuit Input/Output	The OSCIN and OSCOUT pins are used to connect the 32.768-kHz crystal oscillator (with all other oscillation circuit components built into the RV5C387A).
10 5	VDD VSS	Positive Power Supply Input Negative Power Supply Input	The VDD pin is connected to the power supply. The VSS pin is grounded.

ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply Voltage		–0.3 to +6.5	V
V_I	Input Voltage 2	SCL, SDA	–0.3 to +6.5	V
V_O	Output Voltage	SDA, $\overline{INTRA}$, $\overline{INTRB}$ $\overline{INTRC}$, 32KOUT	–0.3 to +6.5	V
P_D	Power Dissipation	Topt=25˚C	300	mW
Topt	Operating Temperature		–40 to +85	˚C
Tstg	Storage Temperature		–55 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(Vss=0V,Topt=–40 to +85˚C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Supply Voltage		2.0		5.5	V
V_{CLK}	Timekeeping Voltage		1.45		5.5	V
f_{XT}	Oscillation Frequency			32.768		kHz
V_{PUP}	Pull-up Voltage	SCL, SDA, $\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTRC}$, 32KOUT			5.5	V

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified : Vss=0V, V_{DD}=3V, Topt=–40 to +85°C

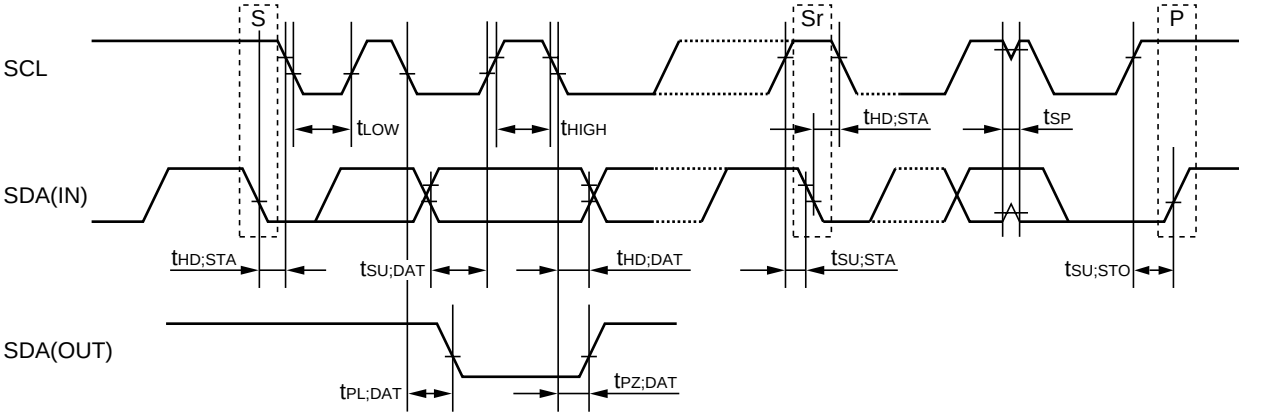
Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" Input Voltage	SCL,SDA	V_{DD}=2.5 to 5.5V	0.8V_{DD}		5.5	V
V_{IL}	"L" Input Voltage			–0.3		0.2V_{DD}	
I_{OL1}	"L" Output Current	32KOUT	V_{OL}=0.4V	0.5			mA
I_{OL2}		$\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTRC}$		1.0			
I_{OL3}		SDA		4.0			
I_{IL}	Input Leakage Current	SCL	V_I=5.5V or Vss V_{DD}=5.5V	–1		1	µA
I_{OZ}		SDA, $\overline{INTRA}$, $\overline{INTRB}$ $\overline{INTRC}$	Vo=5.5V or Vss V_{DD}=5.5V	–1		1	µA
I_{DD}		VDD	V_{DD}=3V, SCL=SDA=3V, Output=OPEN 32KOUT=OFF mode*1		0.35	0.8	µA
V_{DETH}	Supply Voltage Monitoring Voltage ("H")	VDD	Topt=–30 to +70°C	1.90	2.10	2.30	V
V_{DETL}	Supply Voltage Monitoring Voltage ("L")	VDD	Topt=–30 to +70°C	1.45	1.60	1.80	V
C_G	Internal Oscillation Capacitance 1	OSCIN			12		pF
C_D	Internal Oscillation Capacitance 2	OSCOUT			12		

*1) For standby current for outputting 32.768-kHz clock pulses from the 32KOUT pin, see "USAGES, 7. Typical Characteristics".

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified : V_{SS}=0V, Topt=–40 to +85°C
I/O conditions: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, V_{OL}=0.2×V_{DD}, C_L=50pF

Symbol	Item	Conditions	V_{DD}≥2.0V			V_{DD}≥2.5V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
f_{SLC}	SCL clock frequency				100			400	kHz
t_{LOW}	SCL clock “L” time		4.7			1.3			µs
t_{HIGH}	SCL clock “H” time		4.0			0.6			µs
$t_{HD;STA}$	Start condition hold time		4.0			0.6			µs
$t_{SU;STO}$	Stop condition setup time		4.0			0.6			µs
$t_{SU;STA}$	Start condition setup time		4.7			0.6			µs
$t_{SU;DAT}$	Data setup time		250			200			ns
$t_{HD;DAT}$	Data hold time		0			0			ns
$t_{PL;DAT}$	SDA “L” stable time after falling of SCL				2.0			0.9	µs
$t_{PZ;DAT}$	SDA off stable time after falling of SCL				2.0			0.9	µs
t_R	Rising time of SCL and SDA (input)				1000			300	ns
t_F	Falling time of SCL and SDA (input)				300			300	ns
t_{SP}	Spike width that can be removed with input filter				50			50	ns



S Start condition
P Stop condition
Sr Repeated start condition

*) For read/write timing, see “USAGES, 1.5 Considerations in Reading and Writing Time Data”.

GENERAL DESCRIPTION

1. Interface with CPU

The RV5C387A is connected to the CPU by two signal lines SCL and SDA, through which it reads and writes data from and to the CPU. Since the output of the I/O pin of SDA is open drain, data interfacing with a CPU different supply voltage is possible by applying pull-up resistors on the circuit board. The maximum clock frequency of 400kHz (at $V_{DD} \geq 2.5V$) of SCL enables data transfer in I^2C bus fast mode.

2. Clock and Calendar Function

The RV5C387A reads and writes time data from and to the CPU in units ranging from seconds to the last two digits of the calendar year. The calendar year will automatically be identified as a leap year when its last two digits are a multiple of 4. Also available is the 1900/2000 identification bit for Year 2000 compliance. Consequently, leap years up to the year 2099 can automatically be identified as such.

*) The year 2000 is a leap year while the year 2100 is not a leap year.

3. Alarm Function

The RV5C387A incorporates an alarm circuit configured to generate interrupt signals to the CPU for output from the $\overline{INTRB}$ or $\overline{INTRC}$ pin at preset times. The alarm circuit allows two types of alarm settings specified by the Alarm_W registers and the Alarm_D registers. The Alarm_W registers allow week, hour, and minute alarm settings including combinations of multiple day-of-week settings such as “Monday, Wednesday, and Friday” and “Saturday and Sunday”. The Alarm_D registers allow hour and minute alarm settings. The Alarm_W signal outputs from $\overline{INTRB}$ pin, and the Alarm_D signal outputs from $\overline{INTRC}$ pin. The current $\overline{INTRB}$ or $\overline{INTRC}$ pin conditions specified by these two registers can be checked from the CPU by using a polling function.

4. High-precision Oscillation Adjustment Function

The RV5C387A has built-in oscillation stabilization capacitors (C_G and C_D), which can be connected to an external crystal oscillator to configure an oscillation circuit. To correct deviations in the oscillation frequency of the crystal oscillator, the oscillation adjustment circuit is configured to allow correction of a time count gain or loss (up to ±1.5ppm at 25˚C) from the CPU within a maximum range of approximately ±189ppm in increments of approximately 3ppm. Such oscillation frequency adjustment in each system has the following advantages:

- Allows timekeeping with much higher precision than conventional real-time clocks while using a crysta l oscillator with a wide range of precision variations.
- Corrects seasonal frequency deviations through seasonal oscillation adjustment.
- Allows timekeeping with higher precision particularly in systems with a temperature sensing function through oscillation adjustment in tune with temperature fluctuations.

5. Oscillation Halt Sensing Function and Supply Voltage Monitoring Function

The RV5C387A incorporates an oscillation halt sensing circuit equipped with internal registers configured to record any past oscillation halt, thereby identifying whether they are powered on from 0 volts or battery backed-up. As such, the oscillation halt sensing circuit is useful for judging the validity of time data.
The RV5C387A also incorporates a supply voltage monitoring circuit equipped with internal registers configured to record any drop in supply voltage below a certain threshold value. Supply voltage monitoring threshold settings can be selected between 2.1 and 1.6 volts through internal register settings.
The oscillation halt sensing circuit is configured to confirm the established invalidation of time data in contrast to the supply voltage monitoring circuit intended to confirm the potential invalidation of time data. Further, the supply voltage monitoring circuit can be applied to battery supply voltage monitoring.

6. Periodic Interrupt Function

The RV5C387A incorporates a periodic interrupt circuit configured to generate periodic interrupt signals aside from interrupt signals generated by the alarm circuit for output from the $\overline{\text{INTRA}}$ pin. Periodic interrupt signals have five selectable frequency settings of 2Hz (once per 0.5 seconds), 1Hz (once per 1 second), 1/60Hz (once per 1 minute), 1/3600Hz (once per 1 hour), and monthly (the first day of every month). Further, periodic interrupt signals also have two selectable waveforms of a normal pulse form (with a frequency of 2Hz or 1Hz) and special form adapted to interruption from the CPU in the level mode (with second, minute, hour, and month interrupts). The register records of periodic interrupt signals can be monitored by using a polling function.

7. 32-kHz Clock Output Function

The RV5C387A incorporates a 32-kHz clock circuit configured to generate clock pulses with the oscillation frequency of a 32.768-kHz crystal oscillator for output from the 32KOUT pin. The 32KOUT pin is Nch. open drain output. The 32-kHz clock output can be disabled by certain register settings. But it cannot be disabled without manipulation of any two registers with different addresses, to prevent disabling in such events as the runaway of the CPU. The 32-kHz clock circuit is enabled at power-on.

FUNCTIONAL DESCRIPTIONS

1. Address Mapping

	Address				Register								
	A_3	A_2	A_1	A_0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Second Counter	–*2	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1
1	0	0	0	1	Minute Counter	–	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1
2	0	0	1	0	Hour Counter	–	–	H_{20} $P/\overline{A}$	H_{10}	H_8	H_4	H_2	H_1
3	0	0	1	1	Day-of-week Counter	–	–	–	–	–	W_4	W_2	W_1
4	0	1	0	0	Day-of-month Counter	–	–	D_{20}	D_{10}	D_8	D_4	D_2	D_1
5	0	1	0	1	Month Counter and Century Bit	$\overline{19}/20$	–	–	MO_{10}	MO_8	MO_4	MO_2	MO_1
6	0	1	1	0	Year Counter	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1
7	0	1	1	1	Oscillation Adjustment Register*3	–	F_6	F_5	F_4	F_3	F_2	F_1	F_0
8	1	0	0	0	Alarm_W (minute register)	–	WM_{40}	WM_{20}	WM_{10}	WM_8	WM_4	WM_2	WM_1
9	1	0	0	1	Alarm_W (hour register)	–	–	WH_{20} $WP/\overline{A}$	WH_{10}	WH_8	WH_4	WH_2	WH_1
A	1	0	1	0	Alarm_W (Day-of-week register)	–	WW_6	WW_5	WW_4	WW_3	WW_2	WW_1	WW_0
B	1	0	1	1	Alarm_D (minute register)	–	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1
C	1	1	0	0	Alarm_D (hour register)	–	–	DH_{20} $DP/\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1
D	1	1	0	1		–	–	–	–	–	–	–	–
E	1	1	1	0	Control Register 1*3	WALE	DALE	$\overline{12}/24$	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0
F	1	1	1	1	Control Register 2*3	VDSL	VDET	SCRATCH	XSTP	$\overline{CLEN1}$	CTFG	WAFG	DAFG

*1) All the data listed above accept both reading and writing.
*2) The data marked with "–" is invalid for writing and reset to 0 for reading.
*3) When the XSTP bit is set to 1 in control register 2, all the bits are reset to 0 in oscillation adjustment register 1, control register 1 and control register 2 excluding the XSTP bit.

2. Register Settings

2.1 Control Register 1 (at Address Eh)

D7	D6	D5	D4	D3	D2	D1	D0	
WALE	DALE	$\overline{12}$/24	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0	(For writing)
WALE	DALE	$\overline{12}$/24	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0	(For reading)
0	0	0	0	0	0	0	0	Default settings*[1]

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.1-1 WALE and DALE

Alarm_W Enable Bit and Alarm_D Enable Bit

WALE, DALE	Description	
0	Disabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers).	(Default setting)
1	Enabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers)	

2.1-2 $\overline{12}$/24

$\overline{12}$-/24-hour Mode Selection Bit

$\overline{12}$/24	Description	
0	Selecting the 12-hour mode with a.m. and p.m. indications.	(Default setting)
1	Selecting the 24-hour mode	

Setting the $\overline{12}$/24 bit to 0 and 1 specifies the 12-hour mode and the 24-hour mode, respectively.

Table of Time Digit Indications

24-hour mode	12-hour mode	24-hour mode	12-hour mode
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

*) Setting the $\overline{12}$/24 bit should precede writing time data.

2.1-3 $\overline{\text{CLEN2}}$

32-kHz Clock Output Bit 2

$\overline{\text{CLEN2}}$	Description	
0	Enabling the 32-kHz clock circuit	(Default setting)
1	Disabling the 32-kHz clock circuit	

For the RV5C387A, setting the $\overline{\text{CLEN2}}$ bit or the $\overline{\text{CLEN1}}$ bit (D3 in the control register 2) to 0, specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{\text{CLEN1}}$ and the $\overline{\text{CLEN2}}$ bit to 1 specifies disabling ("H") such output.

2.1-4 TEST

Test Bit

TEST	Description	
0	Normal operation mode	(Default setting)
1	Test mode	

The TEST bit is used only for testing in the factory and should normally be set to 0.

2.1-5 CT_2, CT_1, and CT_0

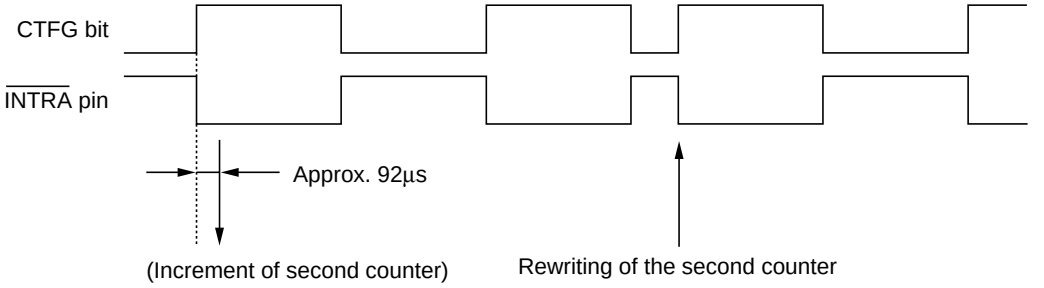
Periodic Interrupt Selection Bits

CT_2	CT_1	CT_0	Description		
			Waveform Mode	Interrupt Cycle and Fall Timing	
0	0	0	—	Off (“H”)	(Default setting)
0	0	1	—	Fixed at low (“L”)	
0	1	0	Pulse Mode	2Hz (Duty cycle of 50%)	
0	1	1	Pulse Mode	1Hz (Duty cycle of 50%)	
1	0	0	Level Mode	Once per 1 second (Synchronized with second counter increment)	
1	0	1	Level Mode	Once per minute (at 00 seconds of every minute)	
1	1	0	Level Mode	Once per hour (at 00 minutes and 00 seconds of every hour)	
1	1	1	Level Mode	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)	

1) Pulse Mode: 2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.
2) Level Mode: periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the second counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.
3) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20 seconds as follows:
   Pulse Mode: the “L” period of output pulses will increment or decrement by a maximum of ±3.784ms. For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.
   Level Mode: a periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784ms.

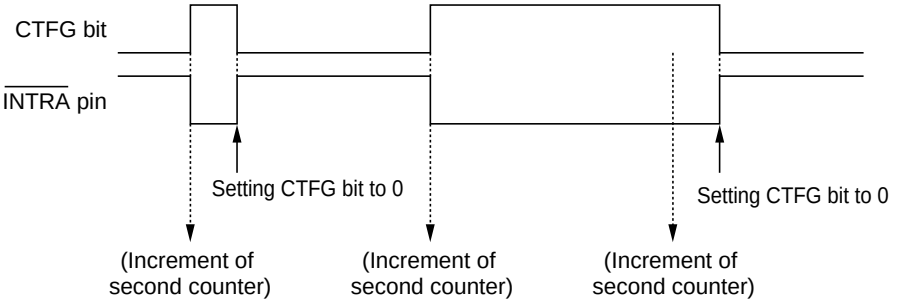
Relation Between the Mode Waveform and the CTFG Bit

• Pulse mode



*) In the pulse mode, the increment of the second counter is delayed by approximately 92µs from the falling edge of clock pulses. Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second. Rewriting the second counter will reset the other time counters of less than 1 second, driving the INTRA pin low.

• Level mode



2.2 Control Register 2 (at Address Fh)

D7	D6	D5	D4	D3	D2	D1	D0	
VDSL	VDET	SCRATCH	XSTP	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For write operation)
VDSL	VDET	SCRATCH	XSTP	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For read operation)
0	0	0	1	0	0	0	0	Default setting*[1]

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.2-1 VDSL

Supply Voltage Monitoring Threshold Selection Bit

VDSL	Description	
0	Selecting the supply voltage monitoring threshold setting of 2.1 volts.	(Default setting)
1	Selecting the supply voltage monitoring threshold setting of 1.6 volts.	

The VDSL bit is intended to select the supply voltage monitoring threshold settings.

2.2-2 VDET

Supply Voltage Monitoring Result Indication Bit

VDET	Description	
0	Indicating supply voltage above the supply voltage monitoring threshold settings.	(Default setting)
1	Indicating supply voltage below the supply voltage monitoring threshold settings.	

Once the VDET bit is set to 1, the supply voltage monitoring circuit will be disabled while the VDET bit will hold the setting of 1. The VDET bit accepts only the writing of 0, which restarts the supply voltage monitoring circuit. Conversely, setting the VDET bit to 1 causes no event.

2.2-3 SCRATCH

Scratch Bit

SCRATCH	Description	
0		(default settings)
1		

The SCRATCH bit is intended for scratching and accepts the reading and writing of 0 and 1. The SCRATCH bit will be set to 0 when the XSTP bit is set to 1 in the control register 2.

2.2-4 XSTP

Oscillation Halt Sensing Bit

XSTP	Description	
0	Sensing a normal condition of oscillation	
1	Sensing a halt of oscillation	(Default setting)

The XSTP bit is for sensing a halt in the oscillation of the crystal oscillator. The oscillation halt sensing circuit operates only when the CE pin is "L".

- The XSTP bit will be set to 1 once a halt in the oscillation of the crystal oscillator is caused by such events as power-on from 0 volts and a drop in supply voltage. The XSTP bit will hold the setting of 1 even after the restart of oscillation. As such, the XSTP bit can be applied to judge the validity of clock and calendar data after power-on or a drop in supply voltage.
- When the XSTP bit is set to 1, all bits will be reset to 0 in the oscillation adjustment register, control register 1, and control register 2, stopping the output from the $\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$, $\overline{\text{INTRC}}$ pin and starting the output of 32.768-kHz clock pulses from the 32KOUT pin.
- The XSTP bit accepts only the writing of 0, which restarts the oscillation halt sensing circuit. Conversely, setting the XSTP bit to 1 causes no event.

2.2-5 $\overline{\text{CLEN1}}$

32-kHz Clock Output Bit 1

$\overline{\text{CLEN1}}$	Description	
0	Enabling the 32-kHz clock output	(Default setting)
1	Disabling the 32-kHz clock output	

Setting the $\overline{\text{CLEN1}}$ bit or the $\overline{\text{CLEN2}}$ bit (D4 in control register 1) to 0, specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{\text{CLEN1}}$ bit and the $\overline{\text{CLEN2}}$ bit to 1 specifies disabling ("L") such output.

2.2-6 CTFG

Periodic Interrupt Flag Bit

CTFG	Description
0	Periodic interrupt output "H" (OFF)
1	Periodic interrupt output "L" (ON)

(Default setting)

The CTFG bit is set to 1 when the periodic interrupt signals are output from the $\overline{\text{INTRA}}$ pin ("L"). The CTFG bit accepts only the writing of 0 in the level mode, which disables ("H") the $\overline{\text{INTRA}}$ pin until it is enabled ("L") again in the next interrupt cycle. Conversely, setting the CTFG bit to 1 causes no event.

2.2-7 WAFG and DAFG

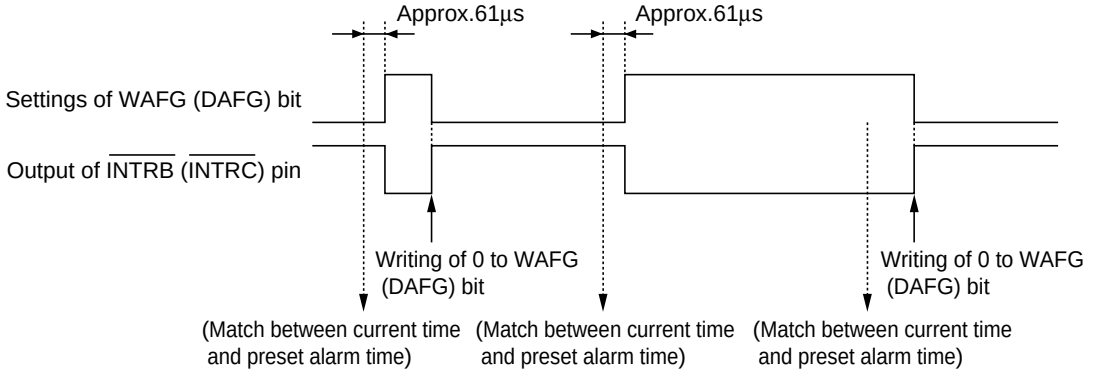
Alarm_W Flag Bit and Alarm_D Flag Bit

WAFG, DAFG	Description
0	Indicating a mismatch between current time and preset alarm time
1	Indicating a match between current time and preset alarm time

(Default setting)

The WAFG and DAFG bits are valid only when the WALE and DALE bits have the setting of 1, which is caused approximately 61µs after any match between current time and preset alarm time specified by the Alarm_W registers and the Alarm_D registers. The WAFG and DAFG bits accept only the writing of 0, which disables ("H") the $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ pin until it is enabled ("L") again at the next preset alarm time. Conversely, setting the WAFG and DAFG bits to 1 causes no event. The WAFG and DAFG bits will have the reading of 0 when the alarm interrupt circuit is disabled with the WALE and DALE bits set to 0. The settings of the WAFG and DAFG bits are synchronized with the output of the $\overline{\text{INTRB}}$ and $\overline{\text{INTRC}}$ pins as shown in the timing chart below.

Output Relationships Between the WAFG or DAFG Bit and $\overline{\text{INTRB}}$, $\overline{\text{INTRC}}$



2.3 Time Counters (at Addresses 0h to 2h)

- Time digit display (BCD format) as follows:
  The second digits range from 00 to 59 and are carried to the minute digit in transition from 59 to 00.
  The minute digits range from 00 to 59 and are carried to the hour digits in transition from 59 to 00.
  The hour digits range as shown in "2.1-2 $\overline{12}$/24: $\overline{12}$-/ 24-hour Mode Selection Bit" and are carried to the day-of-month and day-of-week digits in transition from PM11 to AM12 or from 23 to 00.
- Any writing to the second counter resets divider units of less than 1 second.
- Any carry from lower digits with the writing of non-existent time may cause the time counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent time data.

2.3-1 Second Counter (at Address 0h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For writing)
0	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.3-2 Minute Counter (at Address 1h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For writing)
0	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.3-3 Hour Counter (at Address 2h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	P/$\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For writing)
0	0	P/$\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.4 Day-of-week Counter (at Address 3h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	—	—	—	W_4	W_2	W_1	(For writing)
0	0	0	0	0	W_4	W_2	W_1	(For reading)
0	0	0	0	0	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

- The day-of-week counter is incremented by 1 when the day-of-week digits are carried to the day-of-month digits.
- Day-of-week display (incremented in septimal notation):
  $(W_4, W_2, W_1) = (0, 0, 0) \rightarrow (0, 0, 1) \rightarrow \cdots \rightarrow (1, 1, 0) \rightarrow (0, 0, 0)$
- Correspondences between days of the week and the day-of-week digits are user-definable (e.g. Sunday = 0, 0, 0)
- The writing of (1, 1, 1) to (W_4, W_2, W_1) is prohibited except when days of the week are unused.

2.5 Calendar Counters (at Addresses 4h to 6h)

- The calendar counters are configured to display the calendar digits in BCD format by using the automatic calendar function as follows:

  The day-of-month digits (D_{20} to D_1) range from 1 to 31 for January, March, May, July, August, October, and December; from 1 to 30 for April, June, September, and November; from 1 to 29 for February in leap years; from 1 to 28 for February in ordinary years.

  The day-of-month digits are carried to the month digits in reversion from the last day of the month to 1. The month digits (MO_{10} to MO_1) range from 1 to 12 and are carried to the year digits in reversion from 12 to 1.

  The year digits (Y_{80} to Y_1) range from 00 to 99 (00, 04, 08, ··· , 92, and 96 in leap years) and are carried to the $\overline{19}/20$ digits in reversion from 99 to 00.

  The $\overline{19}/20$ digits cycle between 0 and 1 in reversion from 99 to 00 in the year digits.
- Any carry from lower digits with the writing of non-existent calendar data may cause the calendar counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent calendar data.

2.5-1 Day-of-month Counter (at Address 4h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For writing)
0	0	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.5-2 Month Counter + Century Bit (at Address 5h)

D7	D6	D5	D4	D3	D2	D1	D0	
$\overline{19}/20$	—	—	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For writing)
$\overline{19}/20$	0	0	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For reading)
Indefinite	0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.5-3 Year Counter (at Address 6h)

D7	D6	D5	D4	D3	D2	D1	D0	
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For writing)
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For reading)
Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.6 Oscillation Adjustment Register (at Address 7h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For writing)
0	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For reading)
0	0	0	0	0	0	0	0	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.6-1 F_6 to F_0

The oscillation adjustment circuit is configured to change time counts of 1 second on the basis of the settings of the oscillation adjustment register when the second digits read 00, 20, or 40 seconds. Normally, the second counter is incremented once per 32768 32.768-kHz clock pulses generated by the crystal oscillator. Writing to the F_6 to F_0 bits activates the oscillation adjustment circuit.

- The oscillation adjustment circuit will not operate with the same timing (00, 20, or 40 seconds) as the timing of writing to the oscillation adjustment register.
- The F_6 bit setting of 0 causes an increment of time counts by $((F_5, F_4, F_3, F_2, F_1, F_0) - 1) \times 2$.
  The F_6 bit setting of 1 causes a decrement of time counts by $((\overline{F_5}, \overline{F_4}, \overline{F_3}, \overline{F_2}, \overline{F_1}, \overline{F_0}) + 1) \times 2$.
  The settings of "*, 0, 0, 0, 0, 0, *" ("*" representing either "0" or "1") in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause neither an increment nor decrement of time counts.

Example:

When the second digits read 00, 20, or 40, the settings of "0, 0, 0, 0, 1, 1, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause an increment of the current time counts of 32768 by $(7-1) \times 2$ to 32780 (a current time count loss). When the second digits read 00, 20, or 40, the settings of "0, 0, 0, 0, 0, 0, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause neither an increment nor a decrement of the current time counts of 32768.

When the second digits read 00, 20, or 40, the settings of "1, 1, 1, 1, 1, 1, 0" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause a decrement of the current time counts of 32768 by $(-2) \times 2$ to 32764 (a current time count gain).

An increase of two clock pulses once per 20 seconds causes a time count loss of approximately 3ppm (2 / (32768 × 20=3.051ppm). Conversely, a decrease of two clock pulses once per 20 seconds causes a time count gain of 3ppm. Consequently, deviations in time counts can be corrected with a precision of ±1.5ppm. Note that the oscillation adjustment circuit is configured to correct deviations in time counts and not the oscillation frequency of the 32.768-kHz clock pulses. For further details, see "USAGE, 2.4 Oscillation Adjustment Circuit".

2.7 Alarm_W Registers (at Addresses 8h to Ah)

2.7-1 Alarm_W Minute Register (at Address 8h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	WM_{40}	WM_{20}	WM_{10}	WM_{8}	WM_{4}	WM_{2}	WM_{1}	(For writing)
0	WM_{40}	WM_{20}	WM_{10}	WM_{8}	WM_{4}	WM_{2}	WM_{1}	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.7-2 Alarm_W Hour Register (at Address 9h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	WH_{20},WP/$\overline{A}$	WH_{10}	WH_{8}	WH_{4}	WH_{2}	WH_{1}	(For writing)
0	0	WH_{20},WP/$\overline{A}$	WH_{10}	WH_{8}	WH_{4}	WH_{2}	WH_{1}	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.7-3 Alarm_W Day-of-week Register (at Address Ah)

D7	D6	D5	D4	D3	D2	D1	D0	
—	WW_{6}	WW_{5}	WW_{4}	WW_{3}	WW_{2}	WW_{1}	WW_{0}	(For writing)
0	WW_{6}	WW_{5}	WW_{4}	WW_{3}	WW_{2}	WW_{1}	WW_{0}	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

- The D5 bit of the Alarm_W hour register represents WP/$\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.). and WH_{20} when the 24-hour mode is selected (tens in the hour digits).
- The Alarm_W registers should not have any non-existent alarm time settings. (Note that any mismatch between current time and preset alarm time specified by the Alarm_W registers may disable the alarm circuit.)
- When the 12-hour mode is selected, the hour digits read 12 and 32 for 0 a.m. and 0 p.m., respectively (see "2.1-2 $\overline{12}$/24: $\overline{12}$-/24-hour Mode Selection Bit").
- WW_{0} to WW_{6} correspond to W_{4}, W_{2}, and W_{1} of the day-of-week counter with settings ranging from (0, 0, 0) to (1, 1, 0).
- WW_{0} to WW_{6} with respective settings of 0 disable the outputs of the Alarm_W registers.

Example of Alarm Time Setting

Preset alarm time	Day-of-week							12-hour mode				24-hour mode			
	Sun. WW_0	Mon. WW_1	Tue. WW_2	Wed. WW_3	Thu. WW_4	Fri. WW_5	Sat. WW_6	10-hour	1-hour	10-min	1-min	10-hour	1-hour	10-min	1-min
00:00 a.m. on all days	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 a.m. on all days	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 a.m. on all days	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 p.m. on Mondays to Fridays	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 p.m. on Sundays	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 p.m. on Mondays, Wednesdays, and Fridays	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Note that the correspondence between WW_0 to WW_6 and the days of the week shown in the above table is only an example and not mandatory.

2.8 Alarm_D Registers (at Addresses Bh to Ch)

2.8-1 Alarm_D Minute Register (at Address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
—	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1	(For writing)
0	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.8-2 Alarm_D Hour Register (at Address Ch)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	DH_{20},DP/$\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1	(For writing)
0	0	DH_{20},DP/$\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

- The D5 bit represents DP/$\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.). and DH_{20} when the 24-hour mode is selected (tens in the hour digits).
- The Alarm_D registers should not have any non-existent alarm time settings. (Note that any mismatch between current time and preset alarm time specified by the Alarm_D registers may disable the alarm circuit.)
- When the 12-hour mode is selected, the hour digits read 12 and 32 for 0 a.m. and 0 p.m., respectively (see "2.1-2 $\overline{12}$/24: $\overline{12}$-/24-hour Mode Selection Bit").

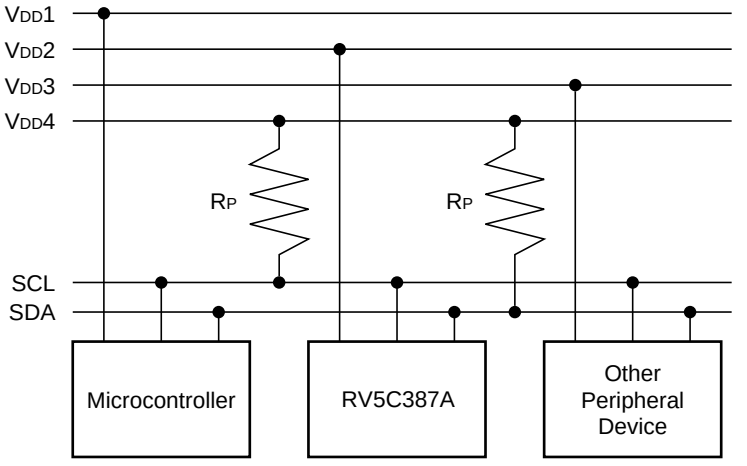
USAGES

1. Interfacing with the CPU

The RV5C387A employs the I^2C bus system to be connected to the CPU via 2-wires. Connection and transfer system of I^2C bus are described in the following sections.

1.1 Connection of I^2C bus

2-wires, SCL and SDA which are connected to I^2C bus are used for transmit clock pulses and data respectively.
All ICs that are connected to these lines are designed that will be not be clamped when a voltage beyond supply voltage is applied to input or output pins. Open drain pins are used for output. This construction allows communication of signals between ICs with different supply voltages by adding a pull-up resistor to each signal line as shown in the figure below. Each IC is designed not to affect SCL and SDA signal lines when power to each of these is turned off separately.



∗1) For data interface, the following conditions must be met:
$V_{DD4} \geq V_{DD1}$
$V_{DD4} \geq V_{DD2}$
$V_{DD4} \geq V_{DD3}$
∗2) When the master is one, the micro controller is ready for driving SCL to "H" and R_P of SCL may not be required.

Cautions on Determining R_P Resistance

(1) Voltage drop at R_P due to sum of input current or output current at off conditions on each IC pin connected to the I^2C bus shall be adequately small.
(2) Rising time of each signal shall be kept short even when all capacity of the bus is driven.
(3) Current consumed in I^2C bus is small compared to the consumption current permitted for the entire system.

When all ICs connected to I^2C bus are CMOS type, condition (1) may usually be ignored since input current and off state output current is extremely small for the many CMOS type ICs.
Thus the maximum resistance of R_P may be determined based on (2) while the minimum on (3) in most cases.

In actual cases a resistor may be place between the bus and input/output pins of each IC to improve noise margins in which case the R_P minimum value may be determined by the resistance.

Consumption current in the bus to review (3) above may be expressed by the formula below:

$$\text{Bus consumption current} \fallingdotseq \frac{(\text{Sum of input current and off state output current of all devices in stand-by mode}) \times \text{Bus stand-by duration}}{\text{Bus stand-by duration} + \text{bus operation duration}}$$

$$+ \frac{\text{Supply voltage} \times \text{bus operation duration} \times 2}{R_P \text{ resistance} \times 2 \times (\text{bus stand-by duration} + \text{bus operation duration})}$$

$$+ \text{supply voltage} \times \text{bus capacity} \times \text{charging/discharging times per unit time}$$

Operation of "× 2" in the second member denominator in the above formula is derived from assumption that "L" duration of SDA and SCL pins are the half of bus operation duration. "× 2" in the numerator of the same member is because there are two pins of SDA and SCL. The third member, (charging/discharging times per unit time) means number of transition from "H" to "L" of the signal line.

Calculation example is shown below:

Pull-up resistor (R_P)=10kΩ, Bus capacity=50pF (both for SCL and SDA), V_{DD}=3V
In as system with sum of input current and off state output current of each pin=0.1μA, I^2C bus is used for 10ms every second while the rest of 990ms is in the stand-by mode. In this mode number of transitions of the SCL pin from "H" to "L" state is 100 while SDA 50, every second.

$$\text{Bus consumption current} \fallingdotseq \frac{0.1\mu A \times 990ms}{990ms + 10ms}$$

$$+ \frac{3V \times 10ms \times 2}{10k\Omega \times 2 \times (990ms + 10ms)}$$

$$+ 3V \times 50pF \times (100 + 50)$$

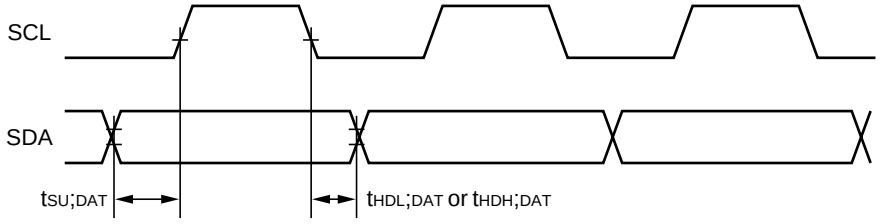
$$= 0.099\mu A + 3.0\mu A + 0.0225\mu A = 3.12\mu A$$

Generally, the second member of the above formula is larger enough than the first and the third members, bus consumption current may be determined by the second member in many cases.

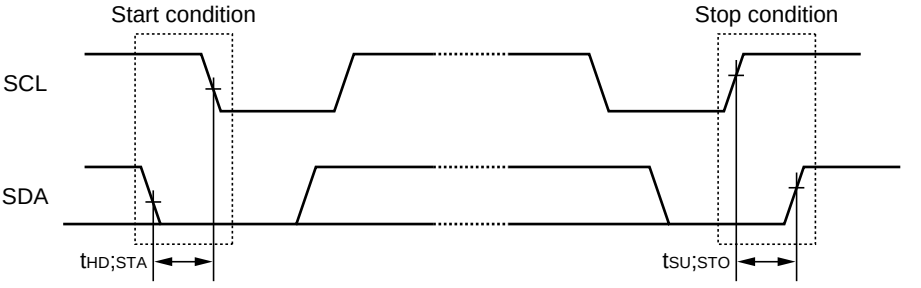
1.2 Transmission System of I^2C bus

1.2-1 Start and stop conditions

In I^2C bus, SDA must be kept at a certain state while SCL is at the "H" state as shown below during data transmission.



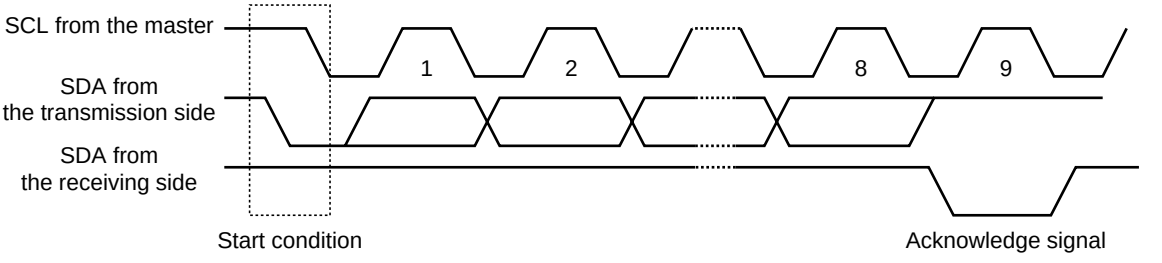
The SCL and SDA pins are at the "H" level when no data transmission is made. Changing the SDA from "H" to "L" when the SCL is "H" activates the start condition and access is started. Changing the SDA from "L" to "H" when the SCL is "H" activates stop condition and accessing stopped. Generation of start and stop conditions are always made by the master (see the figure below).



1.2-2 Data transmission and its acknowledge

After start condition is entered, data is transmitted by 1byte (8bits). Any bytes of data may be serially transmitted. The receiving side will send an acknowledge signal to the transmission side each time 8bit data is transmitted.

The acknowledge signal is sent immediately after falling to "L" of SCL8bit clock pulses of data transmission, by releasing the SDA by the transmission side that has asserted the bus at that time and by turning the SDA to "L" by the receiving side. When transmission of 1byte data next to preceding 1byte of data is received the receiving side releases the SDA pin at falling edge of the SCL9bit of clock pulses or when the receiving side switches to the transmission side it starts data transmission. When the master is the receiving side, it generates no acknowledge signal after the last 1byte of data from the slave to tell the transmitter that data transmission has completed when the slave side (transmission side) continues to release the SDA pin so that the master will be able to generate stop condition.

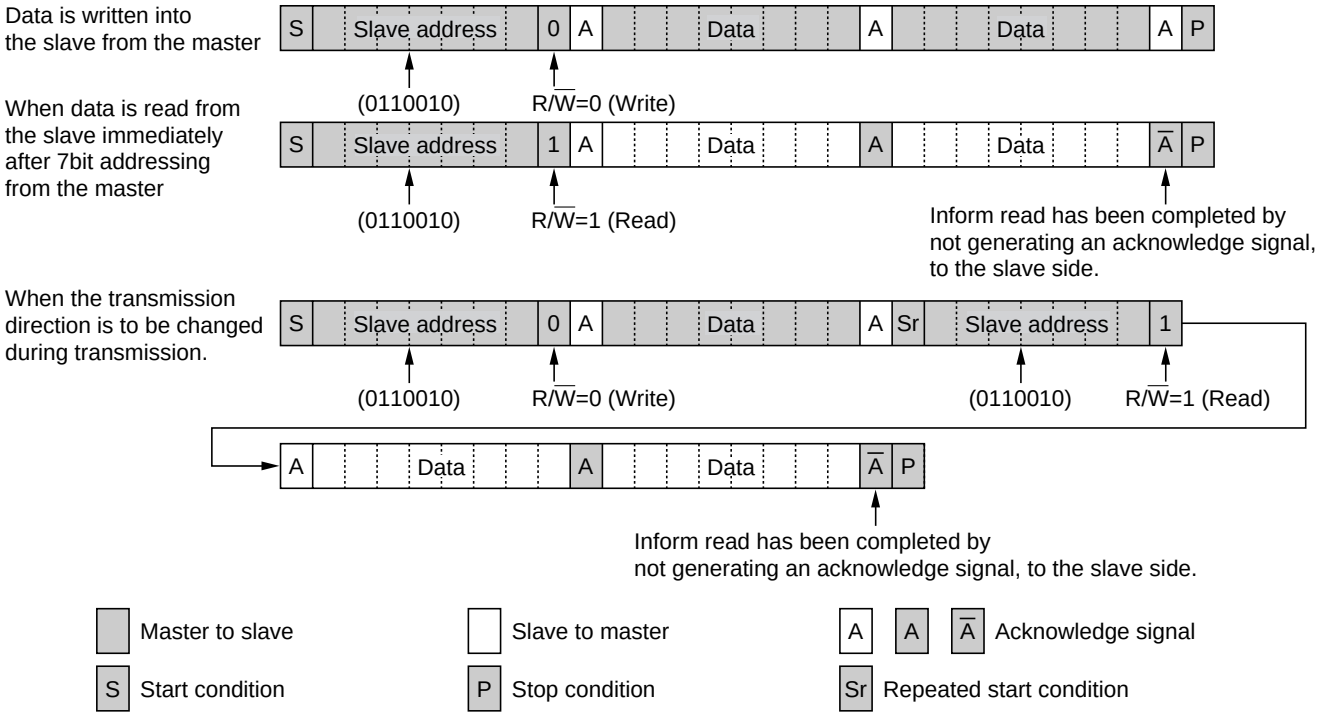


1.2-3 Data transmission format in I^2C bus

I^2C bus generates no CE signals. In place of it each device has a 7bit slave address allocated. The first 1byte is allocated to this 7bit of slave address and to the command (R/$\overline{W}$) for which data transmission direction is designated by the data transmission thereafter. 7bit address is sequentially transmitted from the MSB and 2 and after bytes are read, when 8bit is "H" and write when "L".

The slave address of the RV5C387A is specified at (0110010).

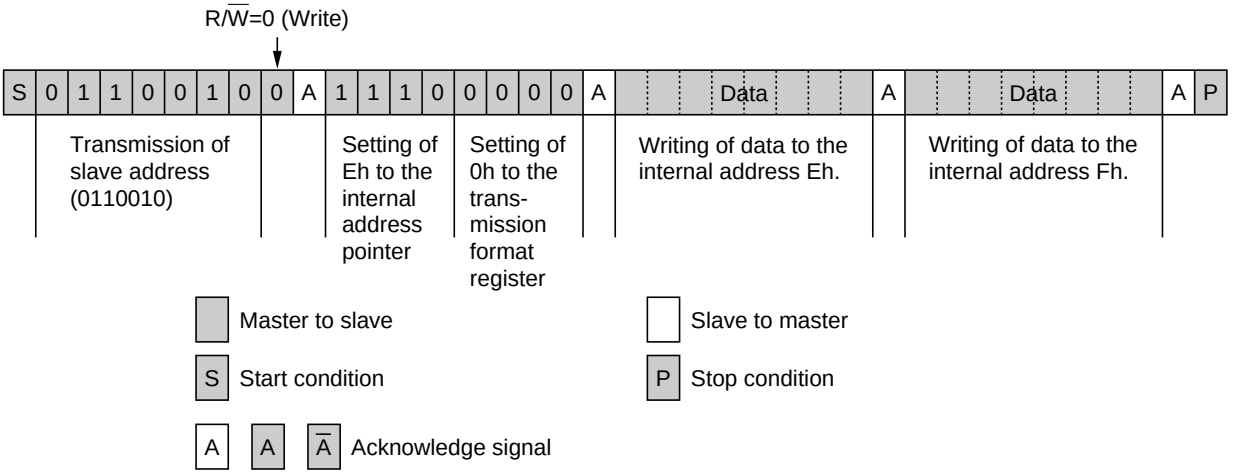
At the end of data transmission/receiving stop condition is generated to complete transmission. However, if start condition is generated without generating stop condition, repeated start condition is met and transmission/receiving data may be continued by setting the slave address again. Use this procedures when the transmission direction needs to be changed during one transmission.



1.2-4 Data transmission write format in the RV5C387A

Although the I^2C bus standard defines a transmission format for the slave address allocated for each IC, transmission method of address information in IC is not defined. The RV5C387A transmits data the internal address pointer (4bit) and the transmission format register (4bit) at the 1byte next to one which transmitted a slave address and a write command. For write operation only one transmission format is available and (0000) is set to the transmission format register. The 3byte transmits data to the address specified by the internal address pointer written to the 2byte. Internal address pointer settings are automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h on transmitting the next byte.

Example of data writing (When writing to internal address Eh to Fh)

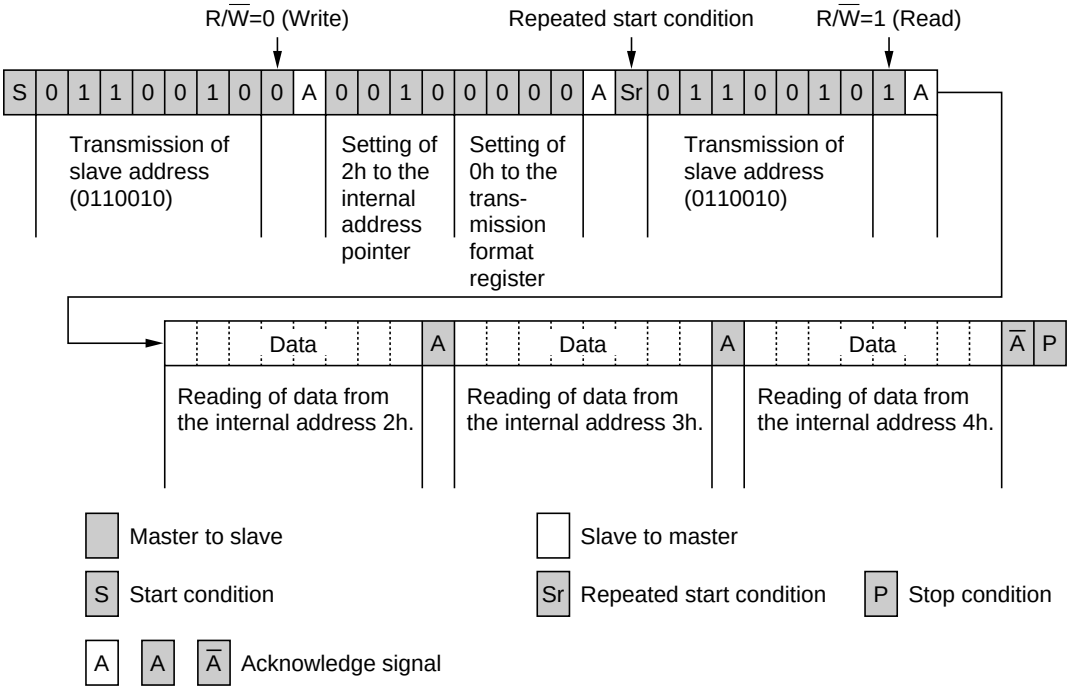


1.2-5 Data transmission read format of the RV5C387A

The RV5C387A allows the following three readout methods of data from an internal register.

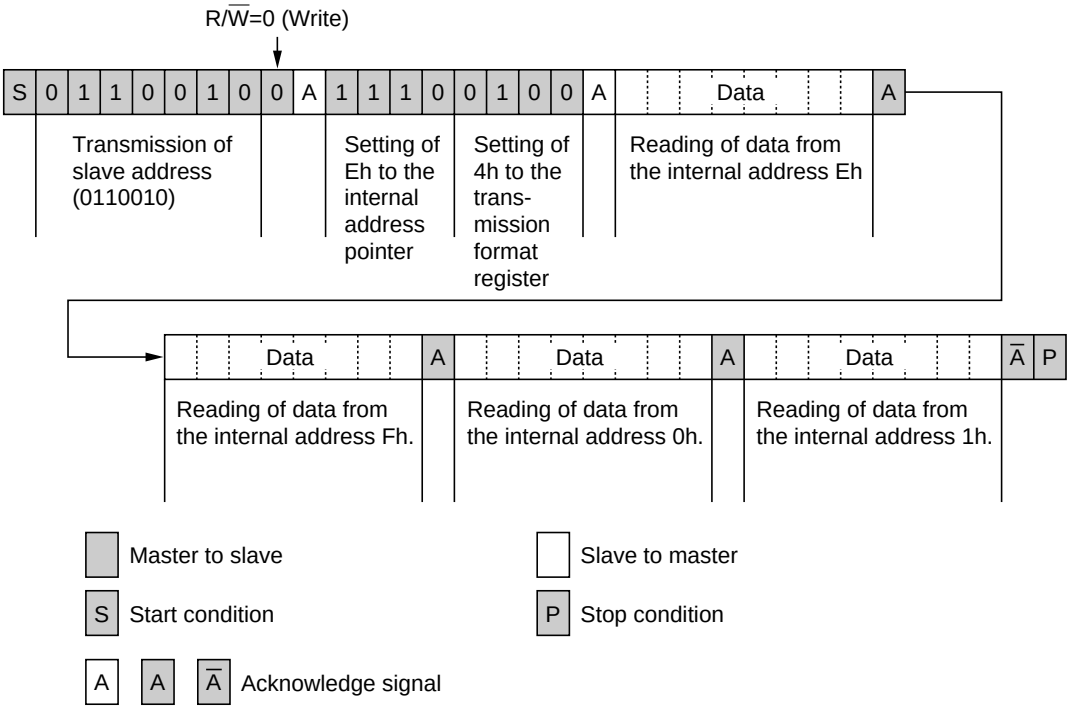
1) The first method to reading data from the internal register is to specify an internal address by setting the internal address pointer and the transmission format register described 1.2-4, generate the repeated start condition (see section 1.2-3) to change the data transmission direction to perform reading. The internal address pointer is set to Fh when the stop condition is met. Therefore, this method of reading allows no insertion of the stop condition before the repeated start condition. Set 0h to the transmission format register.

Example 1 of data read (when data is read from 2h to 4h)



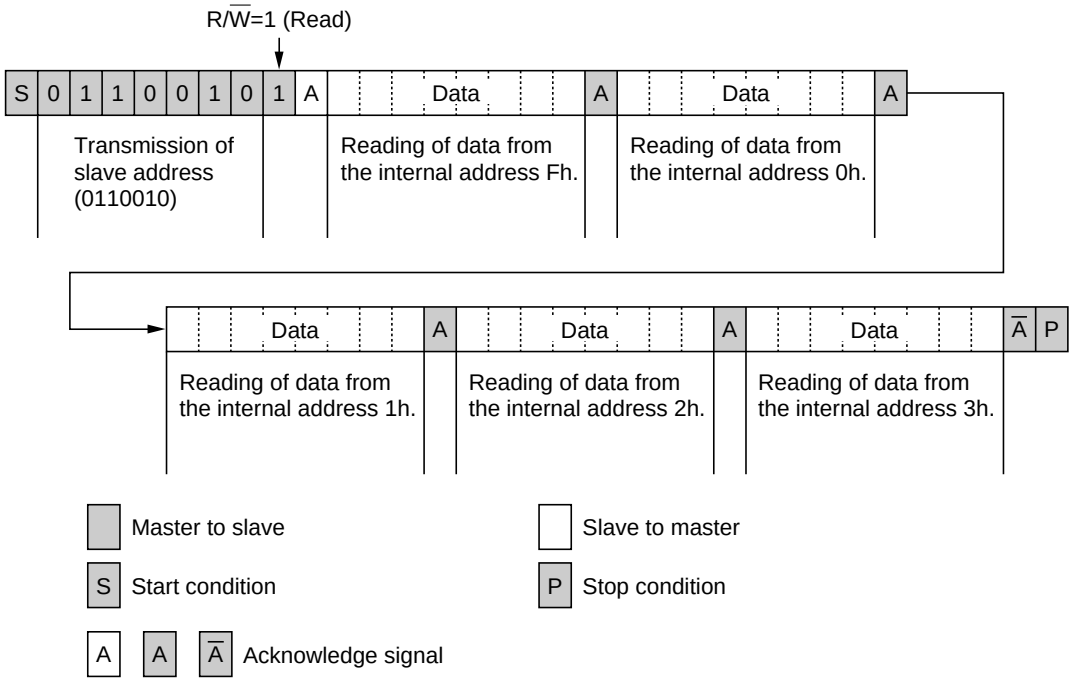
2) The second method to reading data from the internal register is to start reading immediately after writing to the internal address pointer and the transmission format register. Although this method is not based on the I^2C bus standard in a strict sense it still effective to shorten read time to ease load to the master. Set 4h to the transmission format register when this method is used.

Example 2 of data read (when data is read from internal addresses Eh to 1h).



3) The third method to reading data from the internal register is to start reading immediately after writing to the slave address and the R/$\overline{W}$ bit. Since the internal address pointer is set to Fh by default as described in 1), this method is only effective when reading is started from the internal address Fh.

Example 3 of data read (when data is read from internal addresses Fh to 3h).



1.2-6 Data transmission under special condition

The RV5C387A holds the clock tentatively for duration from start condition to stop condition to avoid invalid read or write clock on carrying clock. When clock is carried during this period, which will be adjusted within approx. 61µs from stop condition. To prevent invalid read or write clock shall be made during one transmission operation (from start condition to stop condition). When 0.5 to 1.0 second elapses after start condition any access to the RV5C387A is automatically released to release tentative hold of the clock, set Fh to the address pointer, and access from the CPU is forced to be terminated (the same action as made stop condition is received: automatic resume function from the I^2C bus interface). Therefore, one access must be completed within 0.5 seconds. The automatic resume function prevents delay in clock even if the SCL is stopped from sudden failure of the system during clock read operation.

Also a second start condition after the first condition and before the stop condition is regarded as the "repeated start condition." Therefore, when 0.5 to 1.0 seconds passed after the first start condition, access to the RV5C387A is automatically released.

If access is tried after automatic resume function is activated, no acknowledge signal will be output for writing while FFh will be output for reading.

Access to the Real-time Clock

1) No stop condition shall be generated until clock read/write is started and completed.
2) One cycle read/write operation shall be completed within 0.5 seconds.
3) Do not make Start Condition within 61µs from Stop Condition. When clock is carried during the access, which will be adjusted within approx. 61µs from Stop Condition.

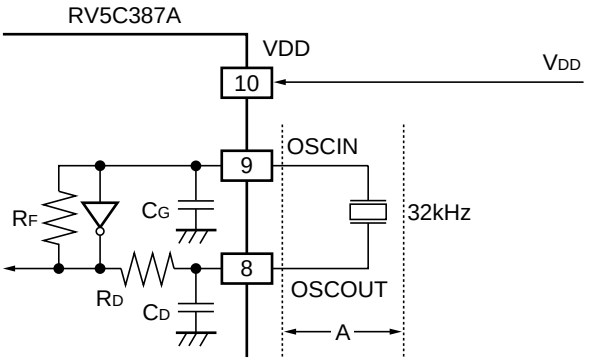
The user shall always be able to access the real-time clock as long as these three conditions are met.

Bad example of reading from seconds to hours (invalid read)
(Start condition) → (Read of seconds) → (Read of minutes) → (Stop condition) → (Start condition) → (Read of hour) → (Stop condition)

Assuming read was started at 05:59:59 P.M. and while reading seconds and minutes the time advanced to 06:00:00 P.M. At this time second digit is hold so the read as 05:59:59. Then the RV5C387A confirms (Stop condition) and carries second digit being hold and the time changes to 06:00:00 P.M. Then, when the hour digit is read, it changes to 6. The wrong results of 06:59:59 will be read.

2. Configuration of Oscillation Circuit and Correction of Time Count Deviations

2.1 Configuration of Oscillating Circuit



Typical externally-equipped element
X'tal: 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)

Standard values of internal elements
R_F=15MΩ TYP.
R_D=120kΩ TYP.
C_G, C_D=12pF TYP.

The oscillation circuit is driven at a constant voltage of approximately 1.2 volts relative to the level of the V_{SS} pin input. As such, it is configured to generate an oscillating waveform with a peak-to-peak voltage on the order of 1.2 volts on the positive side of the V_{SS} pin input.

Considerations in Handling Crystal Oscillators

Generally, crystal oscillators have basic characteristics including an equivalent series resistance (R_1) indicating the ease of their oscillation and a load capacitance (C_L) indicating the degree of their center frequency. Particularly, crystal oscillators intended for use with the RV5C387A are recommended to have a typical R_1 value of 30kΩ and a typical C_L value of 6 to 8pF. To confirm these recommended values, contact the manufacturers of crystal oscillators intended for use with these particular models.

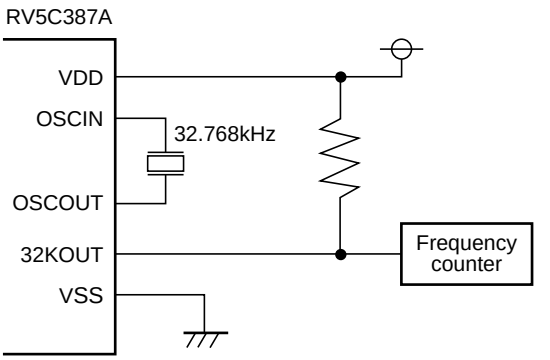
Considerations in Installing Components around the Oscillation Circuit

1) Install the crystal oscillator in the closest possible vicinity to the real-time clock ICs.
2) Avoid laying any signal lines or power lines in the vicinity of the oscillation circuit (particularly in the area marked "←A→" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN and OSCOUT pins and the printed circuit board.
4) Avoid using any long parallel lines to wire the OSCIN and OSCOUT pins.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) For external input of 32.768-kHz clock pulses to the OSCIN pin:
   DC coupling: Prohibited due to an input level mismatch.
   AC coupling: Permissible except that the oscillation halt sensing circuit does not guarantee perfect operation because it may cause sensing errors due to such factors as noise.
2) To maintain stable characteristics of the crystal oscillator, avoid driving any other IC through 32.768-kHz clock pulses output from the OSCOUT pin.

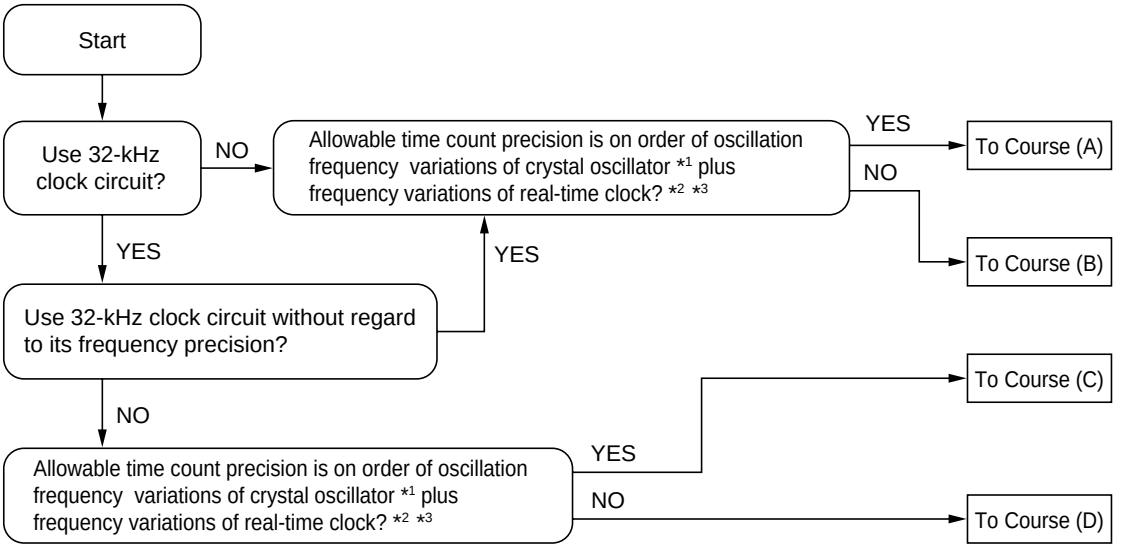
2.2 Measurement of Oscillation Frequency



*1) The RV5C387A is configured to generate 32.768-kHz clock pulses for output from the 32KOUT pin at power-on conditionally on setting the XSTP bit to 1 in the control register 2.
*2) A frequency counter with 6 (more preferably 7) or more digits on the order of 1ppm is recommended for use in the measurement of the oscillation frequency of the oscillation circuit.
*3) The 32KOUT pin should be connected to the VDD pin with a pull-up resistor.

2.3 Adjustment of Oscillation Frequency

The oscillation frequency of the oscillation circuit can be adjusted by varying procedures depending on the usage of the RV5C387A in the system into which they are to be built and on the allowable degree of time count errors. The flow chart below serves as a guide to selecting an optimum oscillation frequency adjustment procedure for the relevant system.



*1) Generally, crystal oscillators for commercial use are classified in terms of their center frequency depending on their load capacitance (C_L) and further divided into ranks on the order of ±10, ±20, and ±50ppm depending on the degree of their oscillation frequency variations.
*2) Basically, the RV5C387A is configured to cause frequency variations on the order of ±5 to ±10ppm at normal temperature.
*3) Time count precision as referred to in the above flow chart is applicable to normal temperature and actually affected by the temperature characteristics and other properties of crystal oscillators.

Course (A)

When the time count precision of each real-time clock is not to be adjusted, the crystal oscillator intended for use with that real-time clock may have any C_L value requiring no presetting. The crystal oscillator may be subject to frequency variations which are selectable within the allowable range of time count precision. Several crystal oscillators and real-time clocks should be used to find the center frequency of the crystal oscillators by the method described in "2.2 Measurement of Oscillation Frequency" and then calculate an appropriate oscillation adjustment value by the method described in "2.4 Oscillation Adjustment Circuit" for writing this value to the RV5C387A.

Course (B)

When the time count precision of each real-time clock is to be adjusted within the oscillation frequency variations of the crystal oscillator plus the frequency variations of the real-time clock ICs, it becomes necessary to correct deviations in the time count of each real-time clock by the method described in "2.4 Oscillation Adjustment Circuit". Such oscillation adjustment provides crystal oscillators with a wider range of allowable settings of their oscillation frequency variations and their C_L values. The real-time clock IC and the crystal oscillator intended for use with that real-time clock IC should be used to find the center frequency of the crystal oscillator by the method described in "2.2 Measurement of Oscillation Frequency" and then confirm the center frequency thus found to fall within the range adjustable by the oscillation adjustment circuit before adjusting the oscillation frequency of the oscillation circuit. At normal temperature, the oscillation frequency of the oscillator circuit can be adjusted by up to approximately ±1.5ppm.

Course (C)

Course (C) together with Course (D) requires adjusting the time count precision of each real-time clock as well as the frequency of 32.768-kHz clock pulses output from the 32KOUT pin. Normally, the oscillation frequency of the crystal oscillator intended for use with the real-time clocks should be adjusted by adjusting the oscillation stabilizing capacitors C_G and C_D connected to both ends of the crystal oscillator. The RV5C387A, which incorporates the C_G and the C_D, require adjusting the oscillation frequency of the crystal oscillator through its C_L value.

Generally, the relationship between the C_L value and the C_G and C_D values can be represented by the following equation:

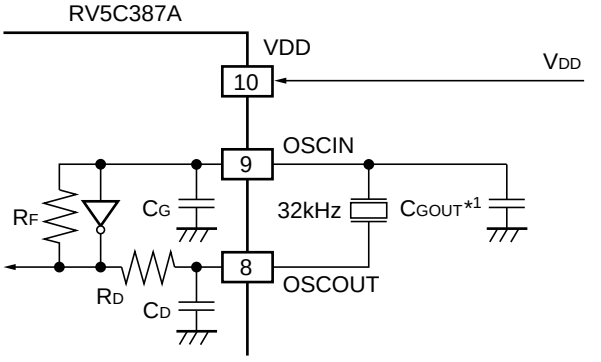
$$C_L = \frac{C_G \times C_D}{C_G + C_D} + C_S$$

where "C_S" represents the floating capacity of the printed circuit board

The crystal oscillator intended for use with the RV5C387A is recommended to have the C_L value on the order of 6 to 8pF. Its oscillation frequency should be measured by the method described in "2.2 Measurement of Oscillation Frequency". Any crystal oscillator found to have an excessively high or low oscillation frequency (causing a time count gain or loss, respectively) should be replaced with another one having a smaller and greater C_L value, respectively until another one having an optimum C_L value is selected. In this case, the bit settings disabling the oscillation adjustment circuit (see "2.4 Oscillation Adjustment Circuit") should be written to the oscillation adjustment register.

Another advisable way to select a crystal oscillator having an optimum C_L value is to contact the manufacturer of the crystal oscillator intended for use with the RV5C387A.
Incidentally, the high oscillation frequency of the crystal oscillator can also be adjusted by adding an external oscillation stabilization capacitor C_{GOUT} as illustrated in the diagram below.

∗1) The C_{GOUT} should have a capacitance ranging from 0 to 15pF.



Course (D)
It is necessary to select the crystal oscillator in the same manner as in Course (C) as well as correct errors in the time count of each real-time clock in the same manner as in Course (B) by the method described in "2.4 Oscillation Adjustment Circuit".

2.4 Oscillation Adjustment Circuit

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision by varying the number of 1-second clock pulses once per 20 seconds. When such oscillation adjustment is not to be made, the oscillation adjustment circuit can be disabled by writing the settings of "∗, 0, 0, 0, 0, 0, ∗" ("∗" representing "0" or "1") to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment circuit. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated by the equation below for writing to the oscillation adjustment circuit.

2.4-1 When Oscillation Frequency *1 is Higher than Target Frequency *2 (There is a Time Count Gain)

$$\text{Oscillation adjustment value}^{*3} = \frac{(\text{Oscillation frequency} - \text{Target frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

∗1) Oscillation frequency: Frequency of clock pulses output from the 32KOUT pin at normal temperature in the manner described in "2.2 Measurement of Oscillation Frequency".

∗2) Target frequency: Desired frequency to be set. Generally, a 32.768-kHz crystal oscillator has such temperature characteristics as to have the highest oscillation frequency at normal temperature. Consequently, the crystal oscillator is recommended to have target frequency settings on the order of 32.768 to 32.76810kHz (+3.05ppm relative to 32.768kHz). Note that the target frequency differs depending on the environment or location where the equipment incorporating the real-time clocks is expected to be operated.

∗3) Oscillation adjustment value: Value that is to be finally written to the F_0 to F_6 bits in the oscillation adjustment register and is represented in 7-bit coded decimal notation.

2.4-2 When Oscillation Frequency is Equal to Target Frequency (There is Neither a Time Count Gain nor a Time Count Loss)

Writing the oscillation adjustment value setting of "0", "+1", "–64", or "–63" to the oscillation adjustment register disables the oscillation adjustment circuit.

2.4-3 When Oscillation Frequency is Lower than Target Frequency (There is a Time Count Loss)

$$\text{Oscillation adjustment value}^{*3} = \frac{(\text{Oscillation frequency} - \text{Target frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10$$

Oscillation adjustment value calculations are exemplified below.

(1) For an oscillation frequency of 32768.85Hz and a target frequency of 32768.05Hz:

Oscillation adjustment value = $(32768.85 - 32768.05 + 0.1) / (32768.85 \times 3.051 \times 10^{-6}) \fallingdotseq (32768.85 - 32768.05) \times 10 + 1$

$= 9.001 \fallingdotseq 9$

In this instance, write the settings of "0, 0, 0, 1, 0, 0, 1" to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

(2) For an oscillation frequency of 32763.95Hz and a target frequency of 32768.05Hz:

Oscillation adjustment value = $(32763.95 - 32768.05) / (32763.95 \times 3.051 \times 10^{-6}) = (32763.95 - 32768.05) \times 10$

$= -41.015 \fallingdotseq -41$

To represent an oscillation adjustment value of –41 in 7-bit coded decimal notation, subtract 41(29h) from 128(80h) to obtain 57h. In this instance, write the settings of "1, 0, 1, 0, 1, 1, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register. Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

Oscillation adjustment involves an adjustment differential of approximately ±1.5ppm from the target frequency at normal temperature.

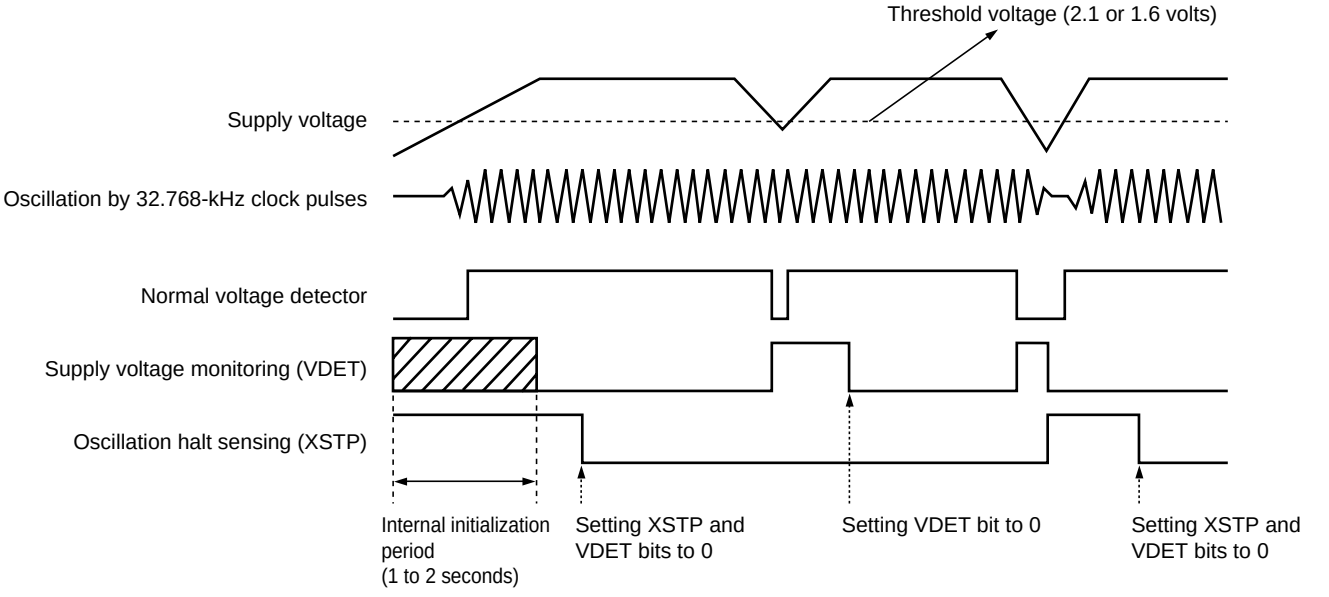
Notes

1) Oscillation adjustment does not affect the frequency of 32.768-kHz clock pulses output from the 32KOUT pin.
2) Oscillation adjustment value range: When the oscillation frequency is higher than the target frequency (causing a time count gain), an appropriate time count gain ranges from –3.05ppm to –189.2ppm with the settings of "0, 0, 0, 0, 0, 1, 0" to "0, 1, 1, 1, 1, 1, 1" written to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register, thus allowing correction of a time count gain of up to +189.2ppm.
   Conversely, when the oscillation frequency is lower than the target frequency (causing a time count loss), an appropriate time count gain ranges from +3.05ppm to +189.2ppm with the settings of "1, 1, 1, 1, 1, 1, 1" to "1, 0, 0, 0, 0, 1, 0" written to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register, thus allowing correction of a time count loss of up to –189.2ppm.

3. Oscillation Halt Sensing and Supply Voltage Monitoring

The oscillation halt sensing circuit is configured to record a halt in the oscillation of 32.768-kHz clock pulses. The supply voltage monitoring circuit is configured to record a drop in supply voltage below a threshold voltage of 2.1 or 1.6 volts. For these functions, the real-time clock has two flag bits (ie. the XSTP bit for the former and the VDET bit for the latter) in which 1 is set once and this setting is maintained until 0 is written.
When the XSTP bit is set to 1 for the oscillation halt sensing circuit, the VDET bit is reset to 0 for the supply voltage monitoring circuit. The relationship between the XSTP and VDET bits is shown in the table below.

XSTP	VDET	Conditions of supply voltage and oscillation
0	0	No drop in supply voltage below threshold voltage and no halt in oscillation
0	1	Drop in supply voltage below threshold voltage and no halt in oscillation
1	*	Halt on oscillation



When the XSTP bit is set to 1 in the control register 2, the F_6 to F_0, WALE, DALE, $\overline{CLEN2}$, $\overline{12}/24$, TEST, CT_2, CT_1, CT_0, VDSL, VDET, SCRATCH, $\overline{CLEN1}$, CTFG, WAFG, and DAFG bits are reset to 0 in the oscillation adjustment register, the control register 1, and the control register 2. The XSTP bit is also set to 1 at power-on from 0 volts. Note that the XSTP bit may be locked to 0 and the internal register broken upon instantaneous power-down.

Considerations in Using Oscillation Halt Sensing Circuit

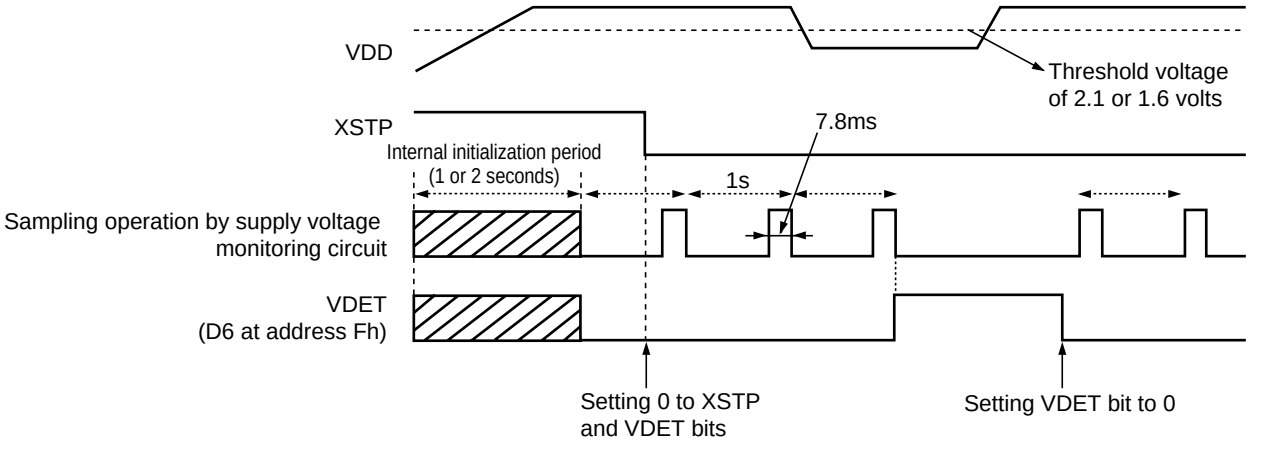
Be sure to prevent the oscillation halt sensing circuit from malfunctioning by preventing the following:

1) Instantaneous power-down on the V_{DD}
2) Condensation on the crystal oscillator
3) On-board noise to the crystal oscillator
4) Applying to individual pins voltage exceeding their respective maximum ratings

In particular, note that the XSTP bit may fail to be set to 1 in the presence of any applied supply voltage as illustrated below in such events as backup battery installation. Further, give special considerations to prevent excessive chattering to pewer supply.

< Supply Voltage Sensing Circuit >

The supply voltage monitoring circuit is configured to conduct a sampling operation during an interval of 7.8ms per second to check for a drop in supply voltage below a threshold voltage of 2.1 or 1.6 volts for the VDSL bit setting of 0 (the default setting) or 1, respectively, in the control register 2, thus minimizing supply current requirements as illustrated in the timing chart below. This circuit suspends a sampling operation once the VDET bit is set to 1 in the control register 2



4. Alarm and Periodic Interrupt

The RV5C387A incorporates the alarm circuit and the periodic interrupt circuit that are configured to generate alarm signals and periodic interrupt signals, respectively, for output from the $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ pin as described below.

1) Alarm Circuit
   The alarm interrupt circuit is configured to generate alarm signals for output from the $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$, which is driven low (enabled) upon the occurrence of a match between current time read by the time counters (the day-of-week, hour, and minute counters) and alarm time preset by the alarm registers (the Alarm_W registers intended for the day-of-week, hour, and minute digit settings and the Alarm_D registers intended for the hour and minute digit settings). The Alarm_W is output form the $\overline{\text{INTRB}}$ pin, and the Alarm_D is output from $\overline{\text{INTRC}}$ pin.

2) Periodic Interrupt Circuit
   The periodic interrupt circuit is configured to generate either clock pulses in the pulse mode or interrupt signals in the level mode for output from the $\overline{\text{INTRA}}$ pin depending on the CT_2, CT_1, and CT_0 bit settings in the control register 1.

The above two types of interrupt signals are monitored by the flag bits (i.e. the WAFG, DAFG, and CTFG bits in the control register 2) and enabled or disabled by the enable bits (i.e. the WALE, DALE, CT_2, CT_1, and CT_0 bits in the control register 1) as listed in the table below.

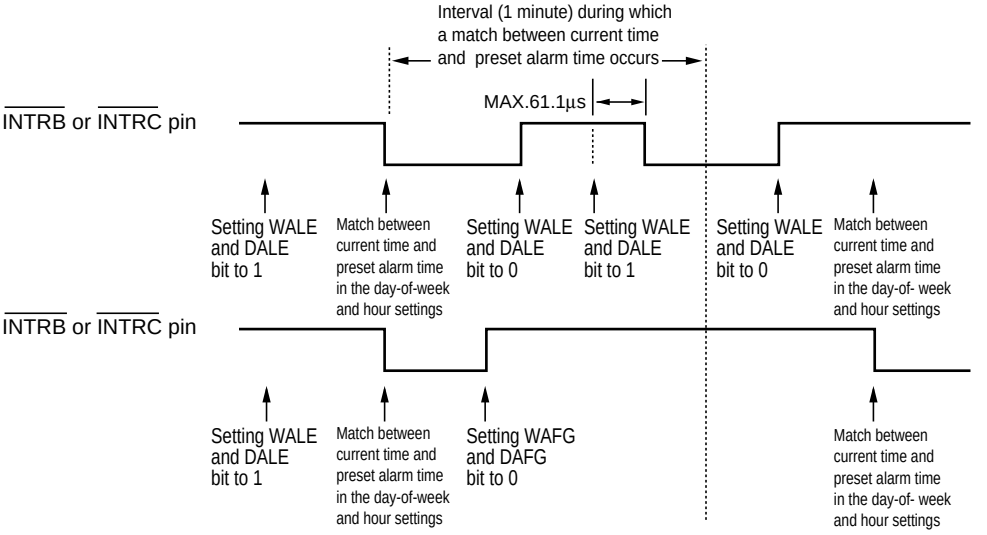
	Flag Bits	Enable Bits	Output Pin
Alarm signals (under control of Alarm_W registers)	WAFG bit (D1 at address Fh)	WALE bit (D7 at address Eh)	$\overline{\text{INTRB}}$
Alarm signals (under control of Alarm_D registers)	DALE bit (D0 at address Fh)	DALE bit (D6 at address Eh)	$\overline{\text{INTRC}}$
Periodic interrupt signals	CTFG bit (D2 of Internal Address Fh)	CT2, CT1, and CT0 bits (D2 to D0 at address Eh) (these bit settings of 0 disable the periodic interrupt circuit)	$\overline{\text{INTRA}}$

· At power-on, when the WALE, DALE, CT_2, CT_1, and CT_0 bits are set to 0 in the control register 1, the $\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ pin is driven high (disabled).

4.1 Alarm Interrupt

The alarm circuit is controlled by the enable bits (i.e. the WALE and DALE bits in the control register 1) and the flag bits (i.e. the WAFG and DAFG bits in the control register 2). The enable bits can be used to enable this circuit when set to 1 and to disable it when set to 0. When intended for reading, the flag bits can be used to monitor alarm interrupt signals. When intended for writing, the flag bits will cause no event when set to 1 and will drive high (disable) the alarm circuit when set to 0.
The enable bits will not be affected even when the flag bits are set to 0. In this event, therefore, the alarm circuit will continue to function until it is driven low (enabled) upon the next occurrence of a match between current time and preset alarm time.

The alarm function can be set by presetting desired alarm time in the alarm registers (the Alarm_W registers for the day-of-week digit settings and both the Alarm_W registers and the Alarm_D registers for the hour and minute digit settings) with the WALE and DALE bits once set to 0 and then to 1 in the control register 1. Note that the WALE and DALE bits should be once set to 0 in order to disable the alarm circuit upon the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm function.



4.2 Periodic Interrupt

Setting of the periodic selection bits (CT_2 to CT_0) enables periodic interrupt to the CPU. There are two waveform modes: pulse mode and level mode. In the pulse mode, the output has a waveform duty cycle of around 50%. In the level mode, the output is cyclically driven low and, when the CTFG bit is set to 0, the output is set to high (OFF).

Waveform Mode, Cycle and Falling Timing

CT_2	CT_1	CT_0	Description		
			Waveform Mode	Interrupt Cycle and Fall Timing	
0	0	0	—	Off (“H”)	(Default setting)
0	0	1	—	Fixed at low (“L”)	
0	1	0	Pulse Mode*1	2Hz (Duty cycle of 50%)	
0	1	1	Pulse Mode*1	1Hz (Duty cycle of 50%)	
1	0	0	Level Mode*2	Once per 1 second (Synchronized with second counter increment)	
1	0	1	Level Mode*2	Once per minute (at 00 seconds of every minute)	
1	1	0	Level Mode*2	Once per hour (at 00 minutes and 00 seconds of every hour)	
1	1	1	Level Mode*2	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)	

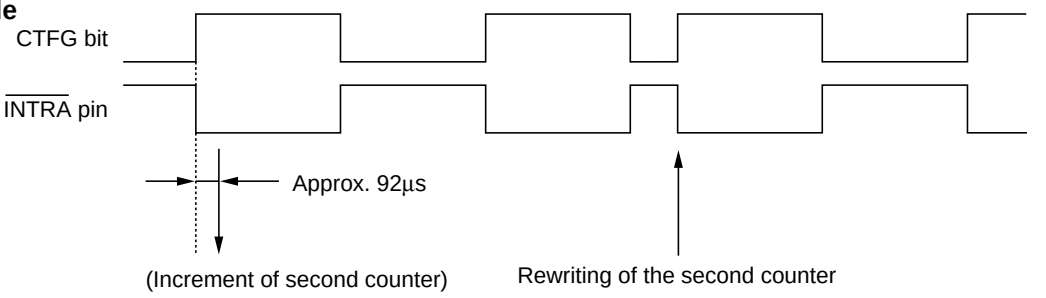
1) Pulse Mode: 2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.

2) Level Mode: periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the second counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.

3) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20 seconds as follows:
   Pulse Mode: the “L” period of output pulses will increment or decrement by a maximum of ±3.784ms. For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%
   Level Mode: a periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784ms.

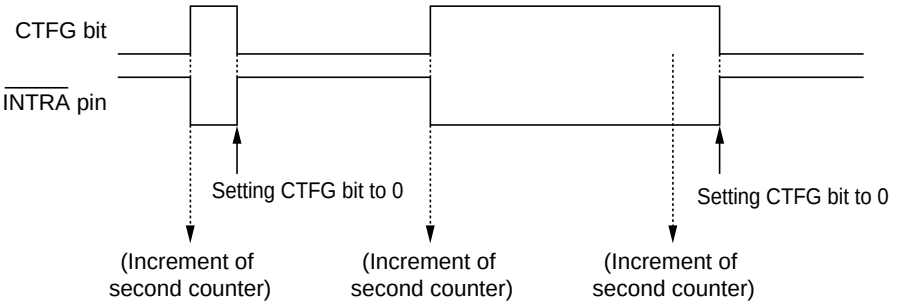
Relation Between the Mode Waveform and the CTFG Bit

• Pulse Mode



*) In the pulse mode, the increment of the second counter is delayed by approximately 92 µs from the falling edge of clock pulses. Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second. Rewriting the second counter will reset the other time counters of less than 1 second, driving the INTRA pin low.

• Level Mode

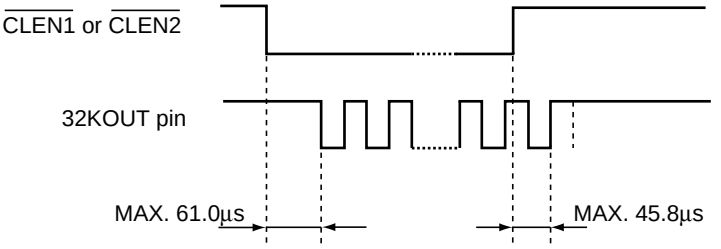


5. 32-kHz Clock Output

32.768-kHz clock pulses are output from the 32KOUT pin when either the CLEN1 bit in the control register 2 or the CLEN2 bit in the control register 1 is set to 0. If the conditions described above are not satisfied, the output is set to high.

CLEN1 (D3 at Address Fh)	**CLEN2 (D4 at Address Eh)**	**32KOUT pin output (Nch Open Drain output)**
1	1	OFF("H")
0 (Default)	*	Clock pulses
*	0 (Default)	

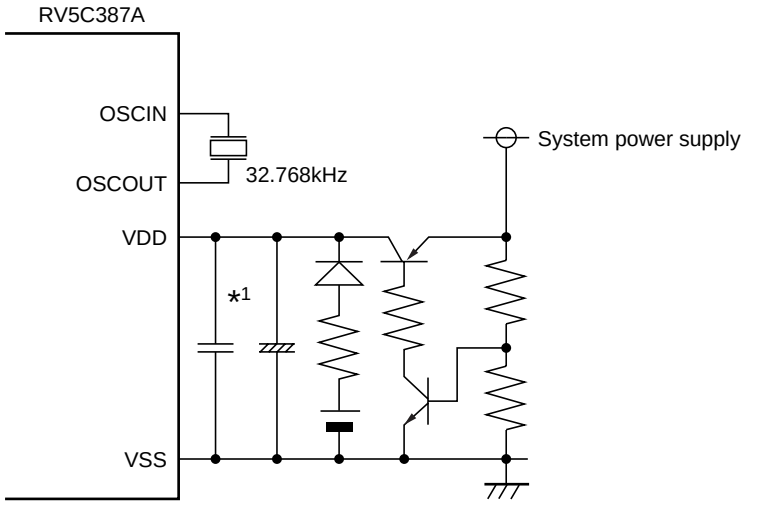
The 32KOUT pin output is synchronized with the CLEN1, CLEN2 bit, settings as illustrated in the timing chart below.



6. Typical Applications

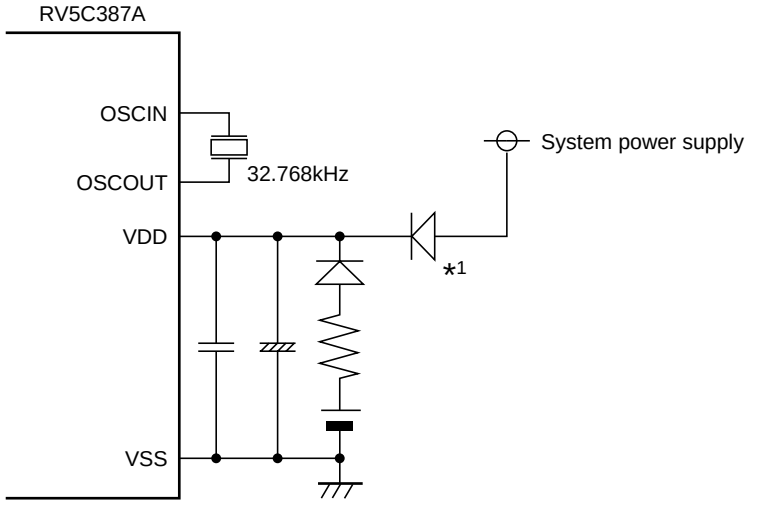
6.1 Typical Power Circuit Configurations

Sample circuit configuration 1



*1) Install bypass capacitors for high-frequency and low-frequency applications in parallel in close vicinity to the RV5C387A .

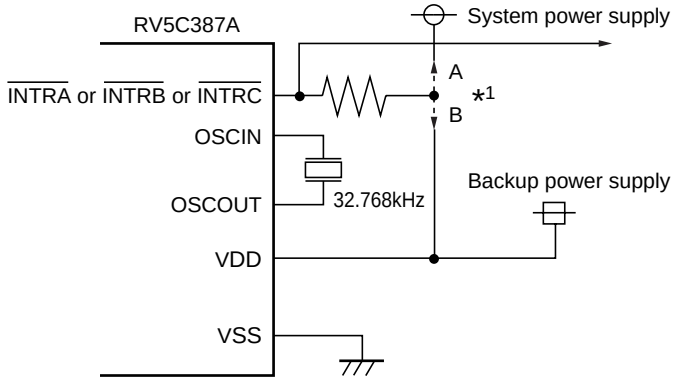
Sample circuit configuration 2



*1) Connection in the example shown left may not affect the RV5C387A since it is designed to be operational even when the pin voltage exceeds VDD.

6.2 Connection of $\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ Pin

The $\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ pin follows the N-channel open drain output logic and contains no protective diode on the power supply side. As such, it can be connected to a pull-up resistor of up to 5.5 volts regardless of supply voltage.

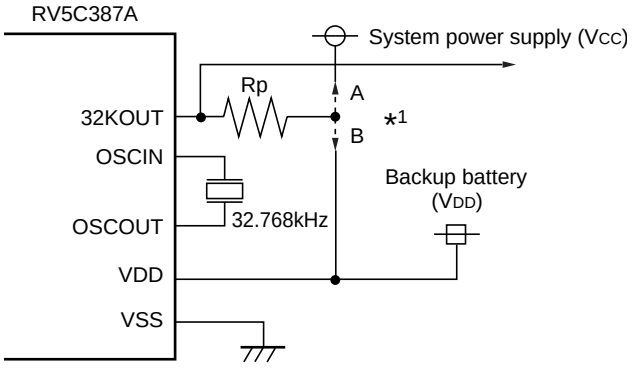


*1) Depending on whether the $\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$ or $\overline{\text{INTRC}}$ pin is to be used during battery backup, it should be connected to a pull-up resistor at the following different positions:
1) Position A in the left diagram when it is not to be used during battery backup.
2) Position B in the left diagram when it is to be used during battery backup.

6.3 Connection of 32KOUT Pin

The 32KOUT pin follows the Nch. open drain output and contains no protective diode on the power supply side. As such, it can be connected to a device with a supply voltage of up to 5.5 volts regardless of supply voltage, provided that such connection involves considerations for the supply current requirements of a pull-up resistor, which can be roughly calculated by the following equation:

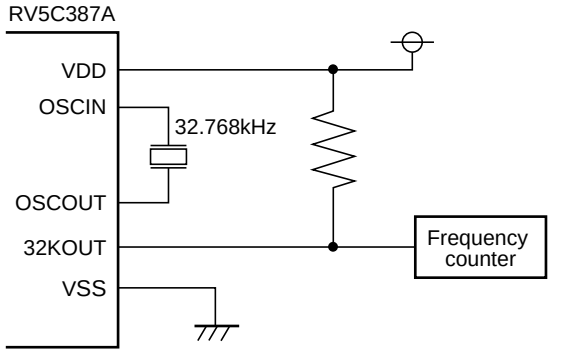
$$I = 0.5 \times (V_{DD} \text{ or } V_{CC}) / Rp$$



*1) Depending on whether the 32KOUT pin is to be used during battery backup, it should be connected to a pull-up resistor at the following different positions:
1) Position A in the left diagram when it is not to be used during battery backup.
2) Position B in the left diagram when it is to be used during battery backup.

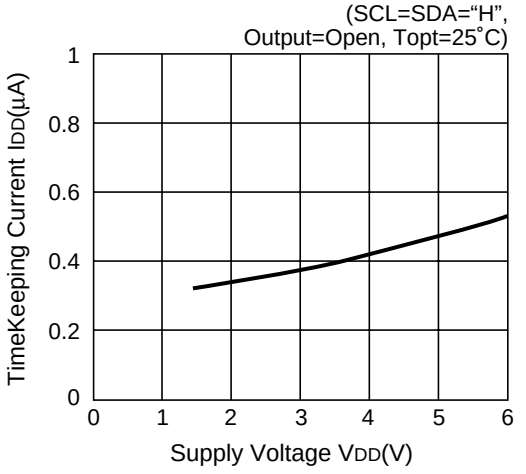
7. Typical Characteristics

• Test Circuit

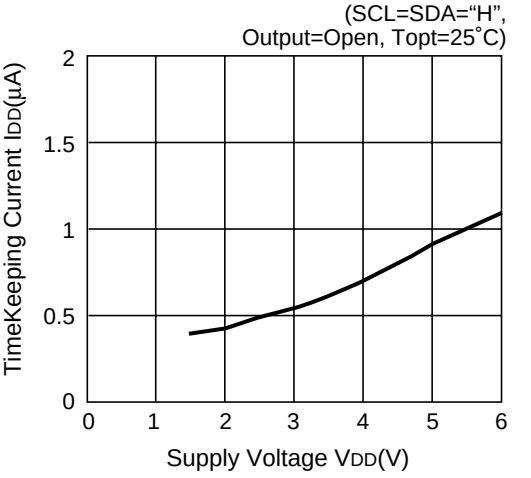


X'tal : 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)
Topt : 25°C
Output Pins: open

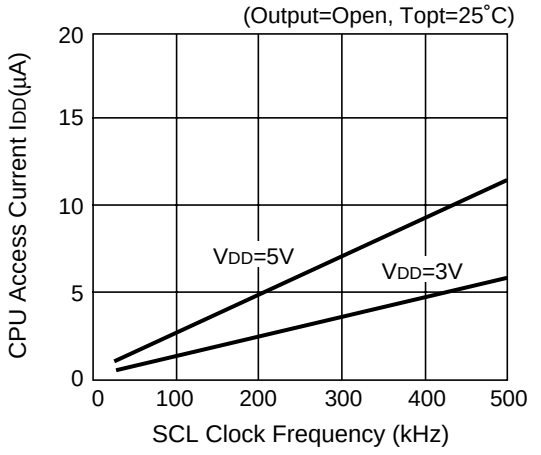
7.1 Timekeeping Current vs. Supply Voltage (with no 32-kHz clock output)



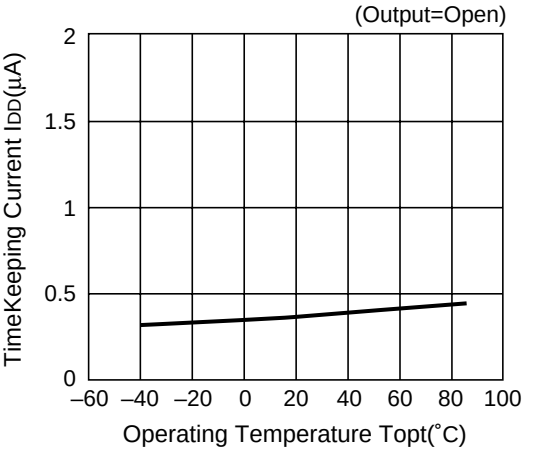
7.2 Timekeeping Current vs. Supply Voltage (with 32-kHz clock output)



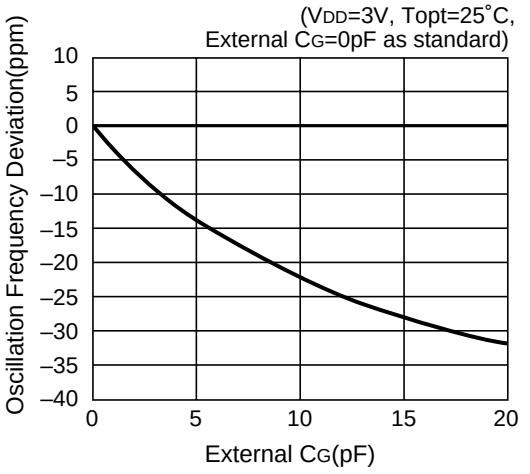
7.3 CPU Access Current vs. SCLK Clock Frequency



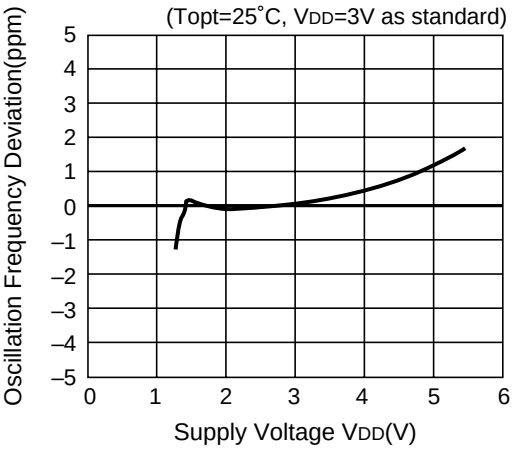
7.4 Timekeeping Current vs. Operating Temperature (with no 32-kHz clock output)



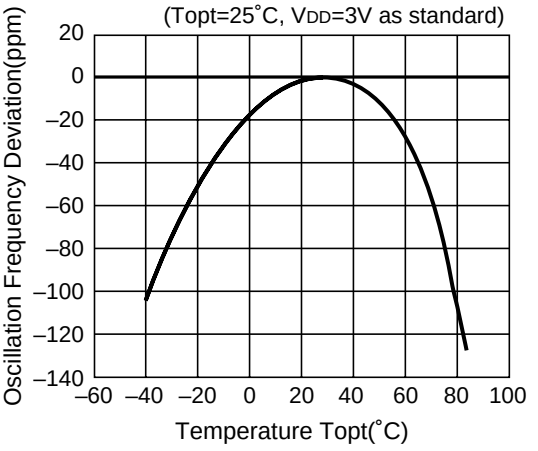
7.5 Oscillation Frequency Deviation vs. External C_G



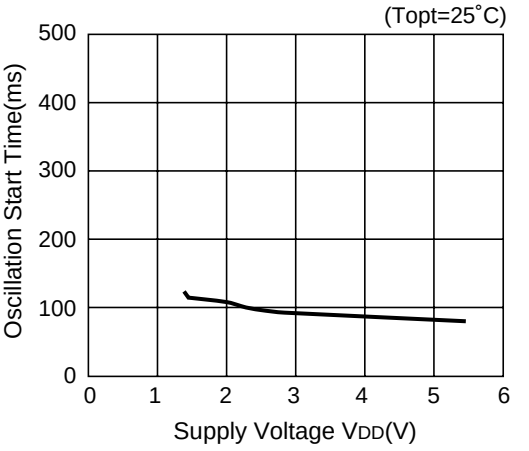
7.6 Oscillation Frequency Deviation vs. Supply Voltage



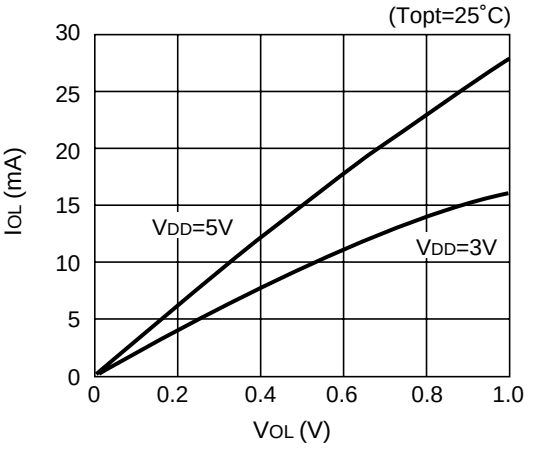
7.7 Oscillation Frequency Deviation vs. Operating Temperature



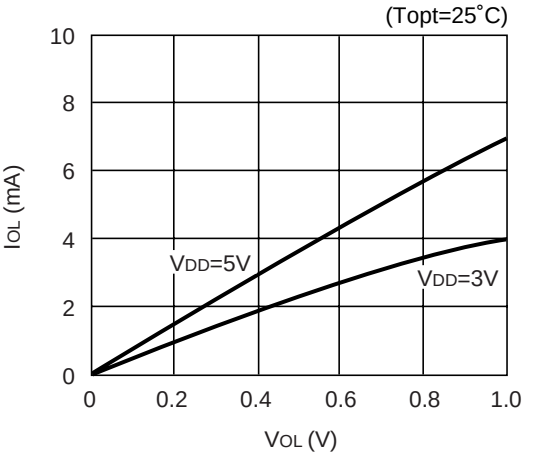
7.8 Oscillation Start Time vs. Supply Voltage



7.9 V_{OL} vs. I_{OL} (INTRA, INTRB, INTRC Pin)

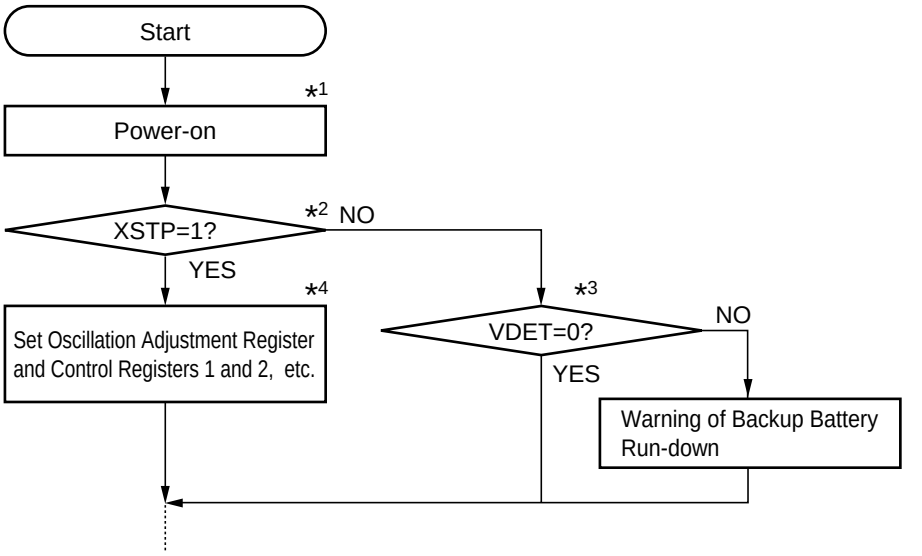


7.10 V_{OL} vs. I_{OL} (32KOUT Pin)



8. Typical Software-based Operations

8.1 Initialization at Power-on



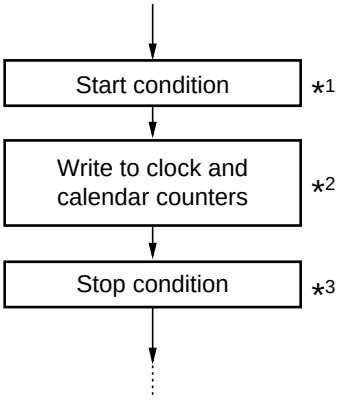
*1) After power-on from 0 volts, the start of oscillation and the process of internal initialization require a time span on the order of 1 to 2 seconds, so that access should be done after the lapse of this time span or more.

*2) The XSTP bit setting of 0 in the control register 1 indicates power-on from backup battery and not from 0 volt. The XSTP bit may fail to be set to 1 in the presence of any excessive chattering in power supply in such events as installing backup battery. Should there be any possibility of this failure occurring, it is recommended to initialize the RV5C387A regardless of the current XSTP bit setting. For further details, see "3. Oscillation Halt Sensing and Supply Voltage Monitoring".

*3) This step is not required when the supply voltage monitoring circuit is not used.

*4) This step involves ordinary initialization including the oscillation adjustment register and interrupt cycle settings.

8.2 Writing of Time and Calendar Data



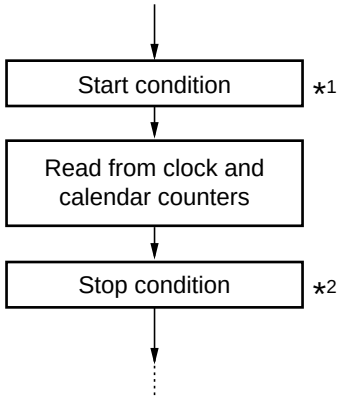
*1) When writing to clock and calendar counters, do not insert stop condition until all times from second to year have been written to prevent error in writing time. (Detailed in "1.2-6 Data transmission under special condition".

*2) Any writing to the second counter will reset divider units lower than the second digits.

*3) Take care so that process from start condition to stop condition will be complete within 0.5sec. (Detailed in "1.2-6 Data transmission under special condition".
The RV5C387A may also be initialized not at power-on but in the process of writing time and calendar data.

8.3 Reading Time and Calendar Data

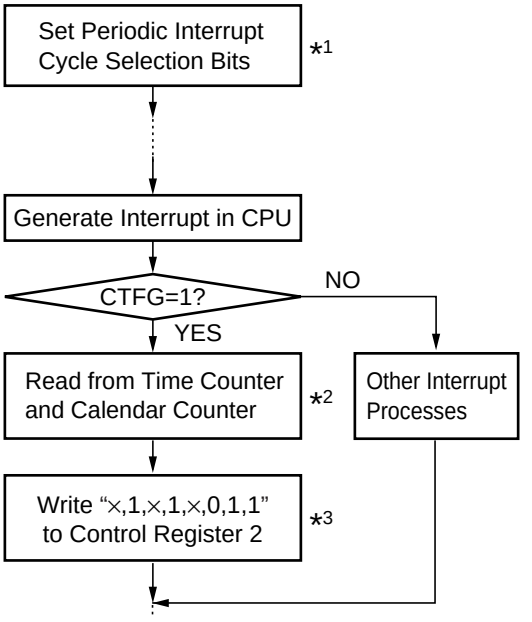
8.3-1 Ordinary Process of Reading Time and Calendar Data



*1) When reading from clock and calendar counters, do not insert stop condition until all times from second to year have been read to prevent error in reading time. (Detailed in "1.2-6 Data transmission under special condition".

*2) Take care so that process from start condition to stop condition will be complete within 0.5sec. (Detailed in "1.2-6 Data transmission under special condition".

8.3-2 Basic Process of Reading Time and Calendar Data Synchronized with Periodic Interrupt



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

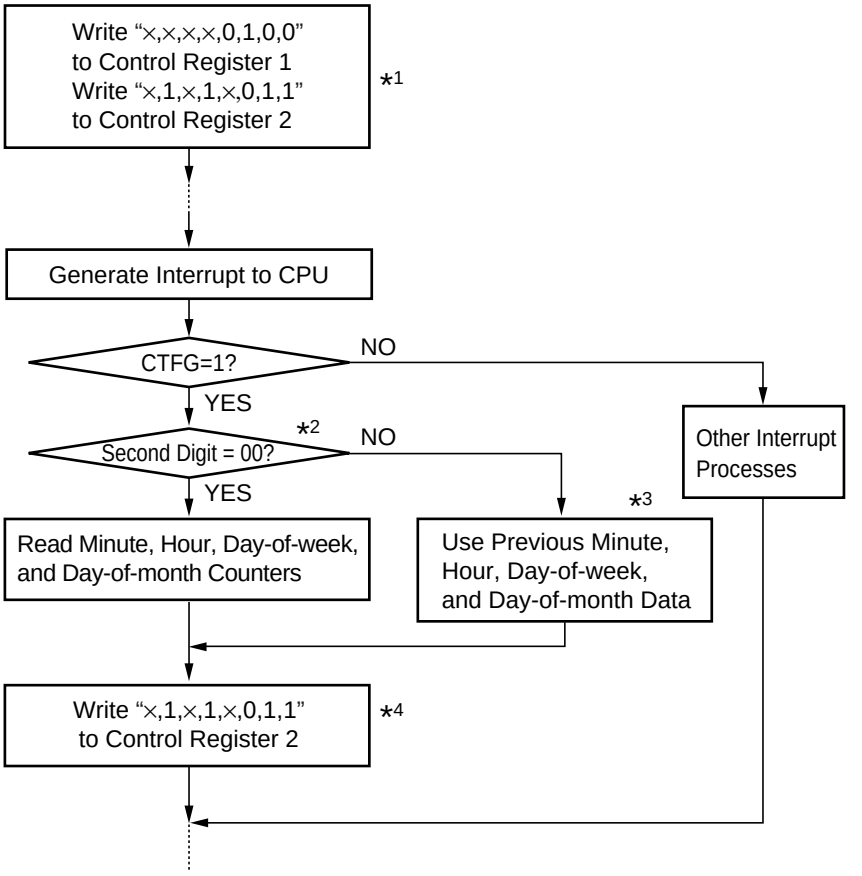
*2) This step must be completed within 0.5 second.

*3) This step is intended to set the CTFG bit to 0 in the Control Register 2 to cancel an interrupt to the CPU.

8.3-3 Applied Process of Reading Time and Calendar Data Synchronized with Periodic Interrupt

Time data need not be read from all the time counters when used for such ordinary purposes as time count indication. This applied process can be used to read time and calendar data with substantial reductions in the load involved in such reading.

For Time Indication in "Day-of-month, Day-of-week, Hour, Minute, and Second" Format:



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

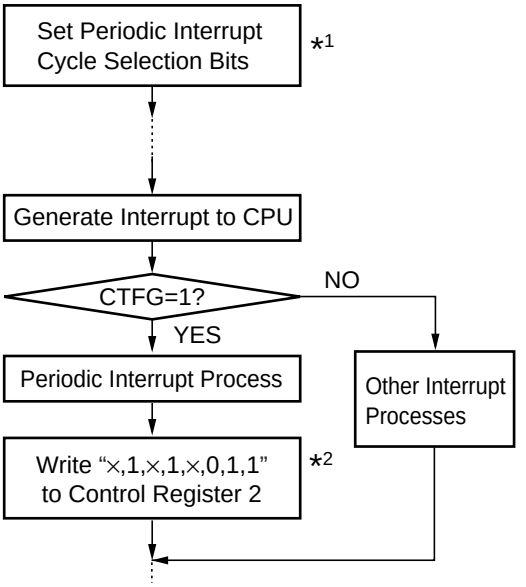
*2) This step must be completed within 0.5sec.

*3) This step is intended to read time data from all the time counters only in the first session of reading time data after writing time data.

*4) This step is intended to set the CTFG bit to 0 in the control register 2 to cancel an interrupt to the CPU.

8.4 Interrupt Process

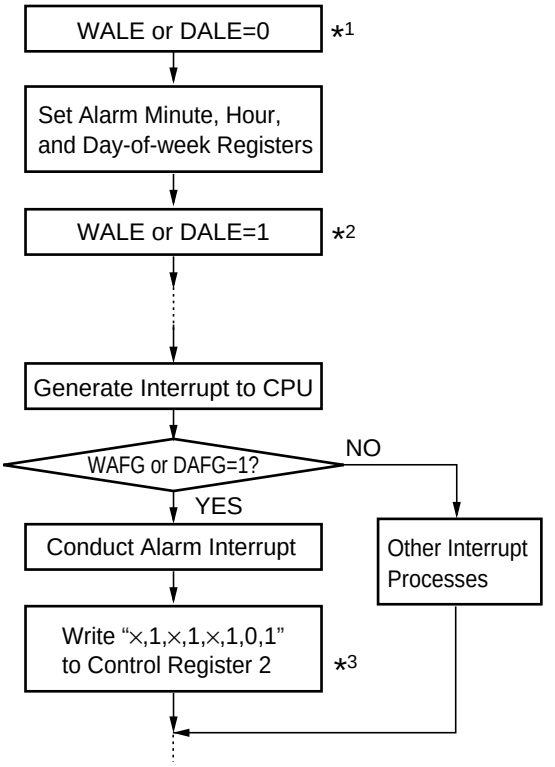
8.4-1 Periodic Interrupt



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

*2) This step is intended to set the CTFG bit to 0 in the control register 2 to cancel an interrupt to the CPU.

8.4-2 Alarm Interrupt



*1) This step is intended to once disable the alarm interrupt circuit by setting the WALE and DALE bits to 0 in anticipation of the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm interrupt function.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

*3) This step is intended to once cancel the alarm interrupt function by writing the settings of "×,1,×,1,×,1,0,1" and "×,1,×,1,×,1,1,0" to the Alarm_W registers and the Alarm_D registers, respectively.

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