### Power Management IC for Automotive Microcontroller

# Buck-Boost Switching Regulator + LDO + Step-down Switching Regulator + Reset + Watch Dog Timer

## BD39001EKV-C

### General Description

BD39001EKV-C is a power management IC with buck-boost switching regulator controller (DC / DC1), secondary step-down switching regulator (DC / DC2), LDO, reset and WDT.
The BD39001EKV-C includes protection circuits, such as Under voltage, Over voltage, Over current and TSD.

### Features

- AEC-Q100 Qualified(Note 1)
- Automatically controlled buck-boost switching regulator with 40 V rated $V_{CC}$, DC / DC2 and LDO input
- 3.3 V fixed output secondary step-down switching regulator with built-in FET
- 5 V fixed output secondary LDO
- Configurable Sequence control
- Over Current protection
  DC / DC1: Adjustable voltage with external resistors
  DC / DC2: Integrated
  LDO: Integrated
- Over voltage / Under voltage detection
- Reset for LDO and DC / DC2
- Window Watchdog Timer
- HTQFP48V package
  (Note 1: Grade 1)

### Applications

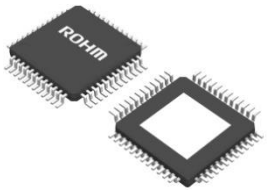
- Microcontroller for Automotive

### Key Specifications

- Input voltage range 4.0 V to 30 V
  (Startup voltage needs to be above 4.5V.)
- Output voltage
  - Buck-Boost DC / DC1 FB Voltage 0.8 V
  - Secondary DC / DC2 3.3 V
  - Secondary LDO 5.0 V
- Reference voltage accuracy
  - Buck-Boost DC / DC1 FB Voltage ±2 %
  - Secondary DC / DC2 ±2 %
  - Secondary LDO ±2 %
- Oscillation frequency 200 to 550 kHz
- Max output current
  - Secondary Buck DC / DC2 900 mA
  - Secondary LDO 600 mA
- Stand-by Current 0 μA (Typ)
- Operating temperature range -40 °C to 125 °C
- AEC-Q100 Qualified

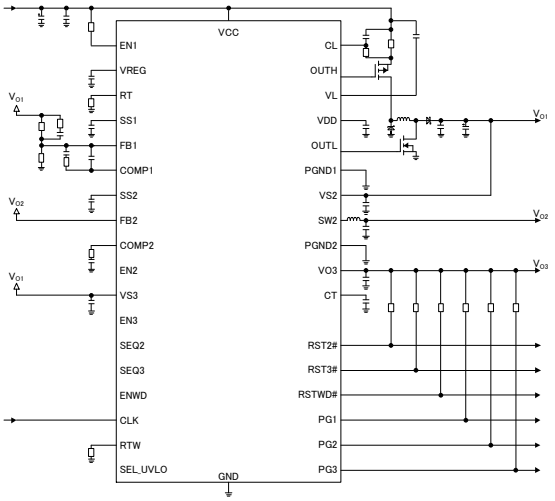
### Package

| | W (Typ) × D (Typ) × H (Max) |
|---|---|
| HTQFP48V | 9.00 mm × 9.00 mm × 1.00 mm |



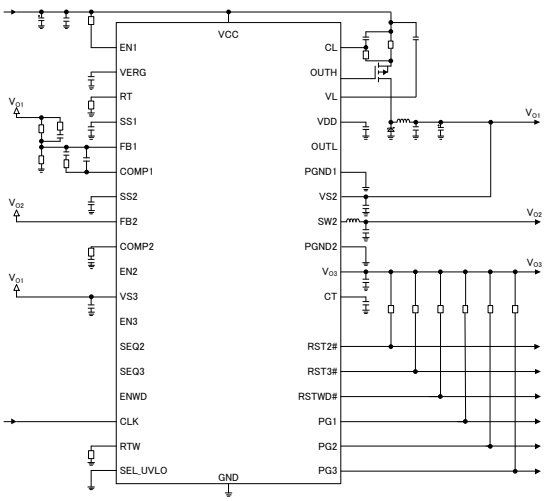

### Typical Application Circuit

Simplified Circuit1




Buck-Boost Switching Regulator
+ Secondary Switching Regulator
+ Secondary LDO

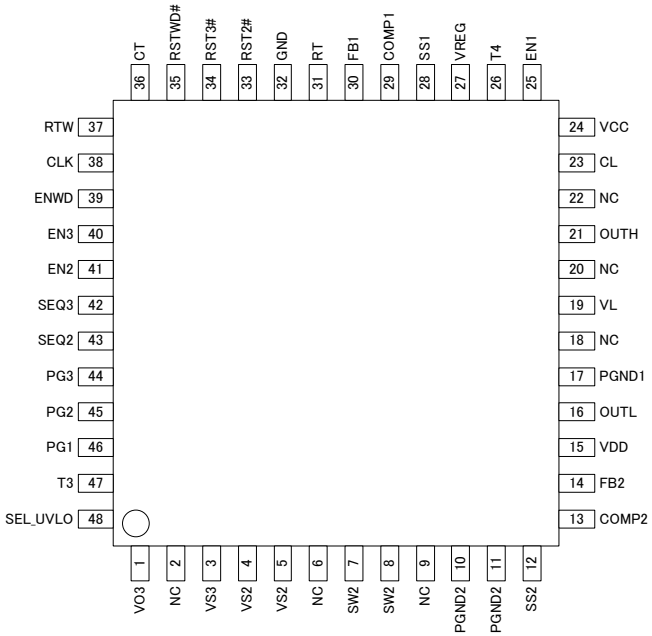
Simplified Circuit2




Buck Switching Regulator
+ Secondary Switching Regulator
+ Secondary LDO

## Pin Configuration

(TOP VIEW)

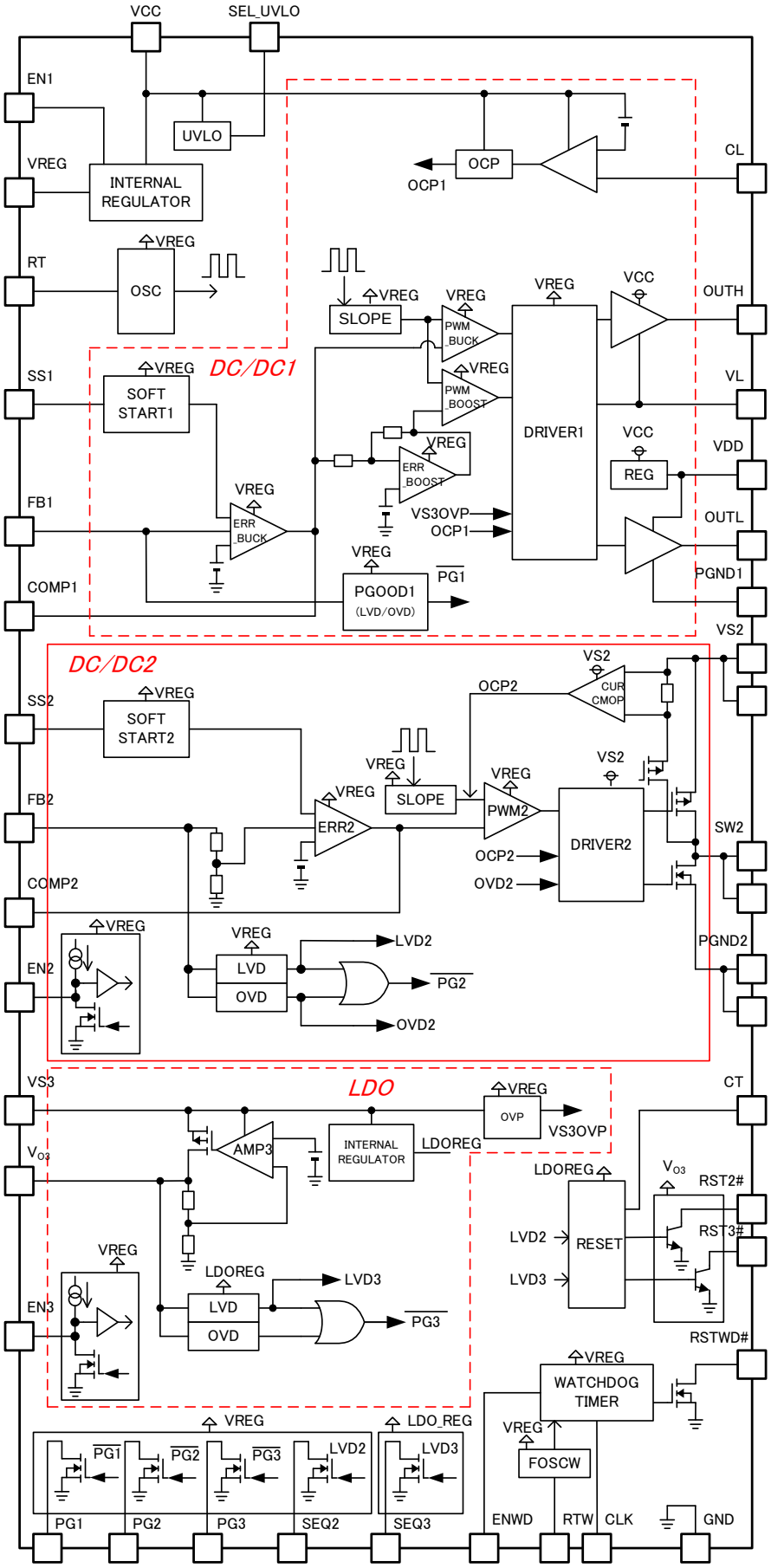



## Pin Description

| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
|---|---|---|---|---|---|
| 1 | VO3 | 5 V Output | 25 | EN1 | Output ON / OFF |
| 2 | N.C. | Not connected | 26 | T4 (Note 1) | Test pin |
| 3 | VS3 | Supply Voltage Input for LDO | 27 | VREG | Internal power supply |
| 4 | VS2 | Supply Voltage Input for DC / DC2 | 28 | SS1 | Soft start time setting for DC / DC1 |
| 5 | VS2 | Supply Voltage Input for DC / DC2 | 29 | COMP1 | Error-amp output for DC / DC1 |
| 6 | N.C. | Not connected | 30 | FB1 | Feedback for DC / DC1 |
| 7 | SW2 | DC / DC2 SW pin | 31 | RT | Frequency setting |
| 8 | SW2 | DC / DC2 SW pin | 32 | GND | Ground |
| 9 | N.C. | Not connected | 33 | RST2# | Reset Output for DC / DC2 |
| 10 | PGND2 | Power Ground | 34 | RST3# | Reset Output for LDO |
| 11 | PGND2 | Power Ground | 35 | RSTWD# | Reset Output for WDT |
| 12 | SS2 | Soft start time setting for DC / DC2 | 36 | CT | Reset Delay |
| 13 | COMP2 | Error-amp output for DC / DC2 | 37 | RTW | Frequency setting for WDT |
| 14 | FB2 | Feedback for DC / DC2 | 38 | CLK | Clock input |
| 15 | VDD | N-channel MOSFET drive supply | 39 | ENWD | WDT ON / OFF |
| 16 | OUTL | N-channel MOSFET drive | 40 | EN3 | Output ON / OFF for LDO |
| 17 | PGND1 | Power Ground | 41 | EN2 | Output ON / OFF for DC / DC2 |
| 18 | N.C. | Not connected | 42 | SEQ3 | Sequence setting for LDO |
| 19 | VL | Pch FET gate clamp for DC / DC1 | 43 | SEQ2 | Sequence setting for DC / DC2 |
| 20 | N.C. | Not connected | 44 | PG3 | Power good output for LDO |
| 21 | OUTH | N-channel MOSFET drive | 45 | PG2 | Power good output for DC / DC2 |
| 22 | N.C. | Not connected | 46 | PG1 | Power good output for DC / DC1 |
| 23 | CL | Overcurrent detection setting for DC / DC1 | 47 | T3 (Note 1) | Test pin |
| 24 | VCC | Supply Voltage Input | 48 | SEL_UVLO | Select Pin for VCC UVLO |

(Note 1) Short with GND

## Block Diagram



## Absolute Maximum Ratings

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| VCC Voltage (Note 1) | $V_{CC}$ | 40 | V |
| VS2 Voltage (Note 1) | $V_{S2}$ | 40 | V |
| VS3 Voltage (Note 1) | $V_{S3}$ | 40 | V |
| CL Voltage | $V_{CL}$ | VCC | V |
| EN1 Voltage | $V_{EN1}$ | VCC | V |
| VREG Voltage | $V_{REG}$ | 7 | V |
| VDD Voltage | $V_{DD}$ | 7 | V |
| SS1, SS2 Voltage | $V_{SS1}$, $V_{SS2}$ | VREG | V |
| RST2#, RST3#, RSTWD# | $V_{RST2\#}$, $V_{RST3\#}$, $V_{RSTWD\#}$ | 7 | V |
| CLK, RTW, CT, ENWD | $V_{CLK}$, $V_{RTW}$, $V_{CT}$, $V_{ENWD}$ | 7 | V |
| PG1, PG2, PG3 | $V_{PG1}$, $V_{PG2}$, $V_{PG3}$ | 7 | V |
| EN2, EN3 | $V_{EN2}$, $V_{EN3}$ | VREG | V |
| SEQ2, SEQ3 | $V_{SEQ2}$, $V_{SEQ3}$ | 7 | V |
| Power Dissipation (Note 2) | Pd | 5.00 | W |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Junction Temperature | Tjmax | 150 | °C |

(Note 1) Pd should not be exceeded.
(Note 2) If mounted on a standard ROHM 4 layer PCB (copper foil area: 70 mm × 70 mm) (Standard ROHM PCB size: 70mm × 70 mm ×1.6mm)
Reduce by 9.6 mW / °C (Ta ≥ 25 °C)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Rating

| Parameter | Symbol | Maximum ratings | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Voltage Power Supply | $V_{CC}$ (Buck Boost mode) | 4 (Note 1) | 30 | V |
| | $V_{CC}$ (Buck mode) | 6 | 30 | V |
| | $V_{S2}$ | 5 | 10 | V |
| | $V_{S3}$ | 5 | 10 | V |
| Oscillation Frequency | $F_{OSC}$ | 200 | 550 | kHz |
| WDT Oscillation Frequency | $F_{OSCW}$ | 50 | 250 | kHz |
| OUTH Current Ability | $I_{OUTH}$ | - | 1.5 | A |
| OUTL Current Ability | $I_{OUTL}$ | - | 1.5 | A |
| SW2 Current Ability | $I_{SW2}$ | - | 900 (Note 2) | mA |
| $V_{O3}$ Current Ability | $I_{VO3}$ | - | 600 (Note 2) | mA |
| Operating Temperature Range | Topr | -40 | +125 | °C |

(Note 1) Initial startup is over 4.5 V
(Note 2) Pd should not be exceeded.

### Electrical Characteristic

(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ $V_{CC}$ ≤ 30 V, 5 V ≤ $V_{S2}$ ≤ 10 V, 5 V ≤ $V_{S3}$ ≤ 10 V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| **All** | | | | | | |
| Standby Current 1 | $I_{STB1}$ | - | 0 | 10 | μA | Ta = 25 °C |
| Standby Current 2 | $I_{STB2}$ | - | - | 30 | μA | Ta = 125 °C |
| Circuit Current | $I_{VCC}$ | 5 | 8 | 12 | mA | $R_{RT}$ = 33 kΩ, $V_{FB1}$ = 1.0 V |
| Oscillation Frequency | $F_{OSC}$ | 315 | 350 | 385 | kHz | $R_{RT}$ = 33 kΩ |
| VREG Output Voltage | $V_{REG}$ | 3.0 | 3.5 | 4.0 | V | |
| VDD Output Voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V | $V_{CC}$ = 12 V |
| UVLO_VCC Detection Voltage 1 | $V_{UVLOVCC1}$ | 3.30 | 3.60 | 3.90 | V | SEL_UVLO = OPEN |
| UVLO_VCC Release Voltage 1 | $V_{UVVCCRE1}$ | 3.50 | 4.00 | 4.50 | V | SEL_UVLO = OPEN |
| UVLO_VCC Hysteresis Voltage 1 | $V_{UVVCCHYS1}$ | 200 | 400 | 600 | mV | SEL_UVLO = OPEN |
| UVLO_VCC Detection Voltage 2 | $V_{UVLOVCC2}$ | 5.27 | 5.58 | 5.89 | V | SEL_UVLO = GND |
| UVLO_VCC Release Voltage 2 | $V_{UVVCCRE2}$ | 5.35 | 5.67 | 6.0 | V | SEL_UVLO = GND |
| UVLO_VCC Hysteresis Voltage 2 | $V_{UVVCCHYS2}$ | 50 | 75 | - | mV | SEL_UVLO = GND |
| EN1 L Voltage | $V_{EN1L}$ | - | - | 0.5 | V | |
| EN1 H Voltage | $V_{EN1H}$ | 2.5 | - | - | V | |
| EN1 Input Resistance | $R_{EN1}$ | 180 | 375 | 570 | kΩ | $V_{EN1}$ = 5 V |
| SEL_UVLO Threshold | $V_{SEL\_UVLO}$ | - | $V_{REG}$ / 2 | - | V | |
| SEL_UVLO Output Current | $I_{SEL\_UVLO}$ | 5 | 14 | 23 | μA | $V_{SEL\_UVLO}$ = 0V |
| **DC / DC1 (Buck - Boost DC / DC Controller)** | | | | | | |
| FB1 Voltage | VREF08 | 0.784 | 0.800 | 0.816 | V | FB1 = COMP1 |
| FB1 Input Bias Current | $I_{FB1}$ | -1 | 0 | +1 | μA | $V_{FB1}$ = 0.8 V |
| Soft Start Quick Charge Current | $I_{SS0}$ | 55 | 110 | 165 | μA | |
| Soft Start Charge Current | $I_{SS1}$ | 5 | 10 | 15 | μA | |
| Soft Start selected Voltage | $V_{SS0}$ | 0.3 | 0.7 | 1.5 | V | |
| Soft Start End Voltage 1 | $V_{SS1}$ | - | $V_{SS0}$+ $V_{REF08}$ | - | V | |
| Soft Start Cramp Voltage | $V_{SSCL1}$ | 2.2 | 2.8 | 3.3 | V | SS1 = OPEN |
| VCC - VL Voltage | $V_L$ | 8 | 10 | 12 | V | $V_{CC}$ ≥ 12 V, $V_{CC}$ - $V_{VL}$ |
| Hi - Side OUTH ON - Resistance | $R_{ONHH}$ | - | 1.7 | - | Ω | $V_{CC}$ = 12 V, OUTH - VCC |
| Lo - Side OUTH ON - Resistance1 | $R_{ONHL1}$ | - | 3 | - | Ω | $V_{CC}$ = 12 V, OUTH - VL |
| Lo - Side OUTH ON - Resistance2 | $R_{ONHL2}$ | - | - | 30 | Ω | $V_{CC}$ = 4 V, OUTH - PGND |
| Hi - Side OUTL ON - Resistance | $R_{ONLH}$ | - | 18 | - | Ω | $V_{CC}$ = 12 V |
| Lo - Side OUTL ON - Resistance | $R_{ONLL}$ | - | 22 | - | Ω | $V_{CC}$ = 12 V |
| Over current detection CL voltage (Low) | $V_{CL\_L}$ | 86 | 100 | 114 | mV | $V_{CC}$ - $V_{CL}$, $V_{CC}$ = 12 V |
| Over current detection CL voltage (High) | $V_{CL\_H}$ | 172 | 200 | 228 | mV | $V_{CC}$ - $V_{CL}$, $V_{CC}$ = 12 V |
| Maximum ON Duty (OUTL) | $T_{ON}$ | - | 92 | - | % | $F_{OSC}$ = 550 kHz |

## Electrical Characteristic

(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ $V_{CC}$ ≤ 30 V, 5 V ≤ $V_{S2}$ ≤ 10 V, 5 V ≤ $V_{S3}$ ≤ 10 V)

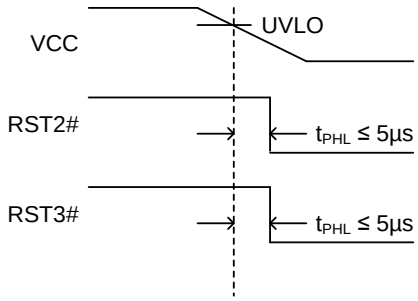
| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| **DC / DC2 (Secondary DC / DC)** | | | | | | |
| Output Voltage 2 | $V_{O2}$ | 3.23 | 3.30 | 3.37 | V | |
| Under voltage detection voltage | $V_{RST2}$ | 3.00 | 3.07 | 3.14 | V | |
| Under voltage hysteresis voltage | $V_{RSTH2}$ | 20 | - | 80 | mV | |
| Soft Start Charge Current | $I_{SS2}$ | 5 | 10 | 15 | µA | $V_{SS2}$ = 0.2 V |
| Soft Start end voltage 2 | $V_{SS2}$ | 0.6 | 0.8 | 1.0 | V | |
| SW2 ON - Resistance H | $R_{ONH2}$ | - | 0.3 | 0.6 | Ω | |
| SW2 ON - Resistance L | $R_{ONL2}$ | - | 0.3 | 0.6 | Ω | |
| EN2 L Voltage | $V_{EN2L}$ | - | - | 0.6 | V | |
| EN2 H Voltage | $V_{EN2H}$ | 1.0 | - | - | V | |
| EN2 Charge Current | $I_{EN2}$ | 4 | 8 | 12 | µA | $V_{EN2}$ = 0.2 V |
| UVLO_VS2 Detection Voltage | $V_{UVLOVS2}$ | 3.5 | 3.9 | 4.3 | V | |
| UVLO_VS2 Hysteresis Voltage | $V_{UVVS2HYS}$ | 0.2 | 0.35 | 0.5 | V | |
| **LDO (5.0 V Output LDO)** | | | | | | |
| Output Voltage 3 | $V_{O3}$ | 4.90 | 5.00 | 5.10 | V | 6.0 V ≤ $V_{S3}$ ≤ 10 V,<br>5 mA ≤ $I_{VO3}$ ≤ 600 mA |
| Drop Voltage | $\Delta V_{O3}$ | - | - | 0.6 | V | $V_{S3}$ = 4.65 V, $I_{VO3}$ = 600 mA |
| Under voltage detection voltage | $V_{RST3}$ | 4.50 | 4.625 | 4.75 | V | |
| Under voltage hysteresis voltage | $V_{RSTH3}$ | 30 | - | 150 | mV | |
| VCC UVLO - LDO LVD difference voltage | $\Delta V_{LVD3}$ | 0.7 | 0.9 | 1.5 | V | $V_{UVLOVVCC2}$ - $V_{RST3}$ |
| EN3 L Voltage | $V_{EN3L}$ | - | - | 0.6 | V | |
| EN3 H Voltage | $V_{EN3H}$ | 1.0 | - | - | V | |
| EN3 Charge Current | $I_{EN3}$ | 4 | 8 | 12 | µA | $V_{EN3}$ = 0.2 V |
| UVLO_VS3 Detection Voltage | $V_{UVLOVS3}$ | 3.5 | 3.9 | 4.3 | V | |
| UVLO_VS3 Hysteresis Voltage | $V_{UVVS3HYS}$ | 0.2 | 0.35 | 0.5 | V | |
| VS3 Over voltage detection voltage | $V_{OVVS}$ | 12.5 | 14 | 15.5 | V | |
| **RST2#, RST3#, RSTWD#** | | | | | | |
| Reset Delay Time | $t_{RST}$ | 30 | 56 | 160 | ms | $C_{CT}$ = 0.47 µF |
| Reset L Voltage 1 | $V_{RSTL1}$ | - | - | 0.25 | V | $V_{O3}$ = 1.0 V, $I_{RST}$ = 100 µA |
| Reset L Voltage 2 | $V_{RSTL2}$ | - | - | 0.4 | V | $I_{RST}$ = 1 mA |
| Reset Response Time | $t_{PHL}$ | - | - | 5 | µs | RST# pull up resistance 4.7 kΩ |
| WDT Oscillation Frequency | $F_{OSCW}$ | 75 | 100 | 125 | kHz | $R_{TW}$ = 51 kΩ |
| CLK FAST NG Threshold | $t_{WF}$ | $\frac{507}{F_{OSCW}}$ | $\frac{512}{F_{OSCW}}$ | $\frac{517}{F_{OSCW}}$ | s | |
| CLK SLOW NG Threshold | $t_{WS}$ | $\frac{6635}{F_{OSCW}}$ | $\frac{6655}{F_{OSCW}}$ | $\frac{6675}{F_{OSCW}}$ | s | |
| WDT Reset Time | $t_{WRES}$ | $\frac{123}{F_{OSCW}}$ | $\frac{128}{F_{OSCW}}$ | $\frac{133}{F_{OSCW}}$ | s | |
| CLK L Voltage | $V_{CLKL}$ | - | - | 0.8 | V | |
| CLK H Voltage | $V_{CLKH}$ | 2.0 | - | - | V | |
| ENWD L Voltage | $V_{ENWDL}$ | - | - | 0.8 | V | |
| ENWD H Voltage | $V_{ENWDH}$ | 2.0 | - | - | V | |
| RSTWD ON Resistance | $R_{RSTWD}$ | 50 | 100 | 200 | Ω | $I_{RSTWD}$ = 100 µA |
| CLK Input Current | $I_{CLK}$ | 10 | 22 | 55 | µA | $V_{CLK}$ = 5 V |
| ENWD Input Current | $I_{ENWD}$ | 5 | 11 | 28 | µA | $V_{ENWD}$ = 5 V |
| RST Leak Current | $I_{LRST}$ | - | - | 10 | µA | $V_{RST}$ = 5V |
| RSTWD Leak Current | $I_{LRSTWD}$ | - | - | 10 | µA | $V_{RSTWD}$ = 5V |

### Electrical Characteristic

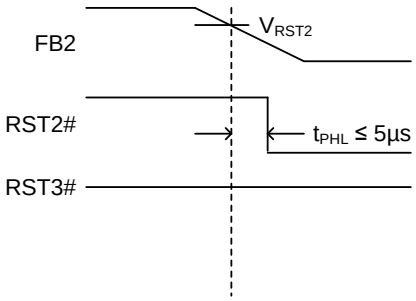
(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ $V_{CC}$ ≤ 30 V, 5 V ≤ $V_{S2}$ ≤ 10 V, 5 V ≤ $V_{S3}$ ≤ 10 V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| **PG1, PG2, PG3** | | | | | | |
| PG ON - Resistance | $R_{PG1}$<br>$R_{PG2}$<br>$R_{PG3}$ | 0.5 | 1.0 | 2.0 | kΩ | |
| PG1 Under Voltage Detection voltage | $V_{LVPG1}$ | 0.62 | 0.67 | 0.72 | V | $V_{FB1}$ Voltage |
| PG1 Under Voltage Hysteresis | $V_{LVPH1}$ | 20 | - | 100 | mV | $V_{FB1}$ Voltage |
| PG1 Over Voltage Detection Voltage | $V_{OVPG1}$ | 0.88 | 0.94 | 1.00 | V | $V_{FB1}$ Voltage |
| PG1 Over Voltage Hysteresis | $V_{OVPH1}$ | 20 | - | 100 | mV | $V_{FB1}$ Voltage |
| PG2 Under Voltage Detection Voltage | $V_{LVPG2}$ | 3.00 | 3.07 | 3.14 | V | $V_{FB2}$ Voltage |
| PG2 Under Voltage Hysteresis | $V_{LVPH2}$ | 20 | - | 80 | mV | $V_{FB2}$ Voltage |
| PG2 Over Voltage Detection Voltage | $V_{OVPG2}$ | 3.45 | 3.53 | 3.60 | V | $V_{FB2}$ Voltage |
| PG2 Over Voltage Hysteresis | $V_{OVPH2}$ | 20 | - | 80 | mV | $V_{FB2}$ Voltage |
| PG3 Under Voltage Detection Voltage | $V_{LVPG3}$ | 4.50 | 4.625 | 4.75 | V | $V_{O3}$ Voltage |
| PG3 Under Voltage Hysteresis | $V_{LVPH3}$ | 30 | - | 150 | mV | $V_{O3}$ Voltage |
| PG3 Over Voltage Detection Voltage | $V_{OVPG3}$ | 5.25 | 5.38 | 5.50 | V | $V_{O3}$ Voltage |
| PG3 Over Voltage Hysteresis | $V_{OVPH3}$ | 30 | - | 150 | mV | $V_{O3}$ Voltage |
| PG Leak Current | $I_{LPG}$ | - | - | 10 | μA | $V_{PG}$ = 5V |
| **SEQ 2, SEQ 3** | | | | | | |
| SEQ2 ON Resistance | $R_{SEQ2}$ | 0.5 | 1.0 | 2.0 | kΩ | $I_{SEQ2}$ = 100 μA |
| SEQ3 ON Resistance | $R_{SEQ3}$ | 0.5 | 1.0 | 2.0 | kΩ | $I_{SEQ3}$ = 100 μA |
| SEQ Leak Current | $I_{LSEQ}$ | - | - | 10 | μA | $V_{SEQ}$ = 5V |

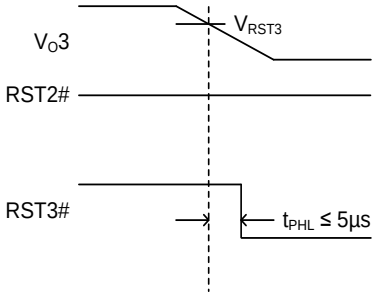
### Reset response time ($t_{PHL}$)




UVLO, RST# Delay time




FB2, RST2# Delay time




VO3, RST3# Delay time

**Typical Performance Curves**

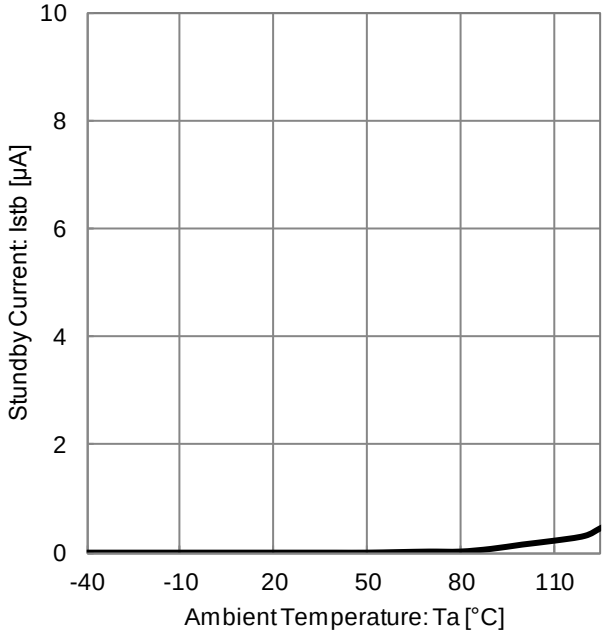



Figure 1. Standby Current vs. Temperature

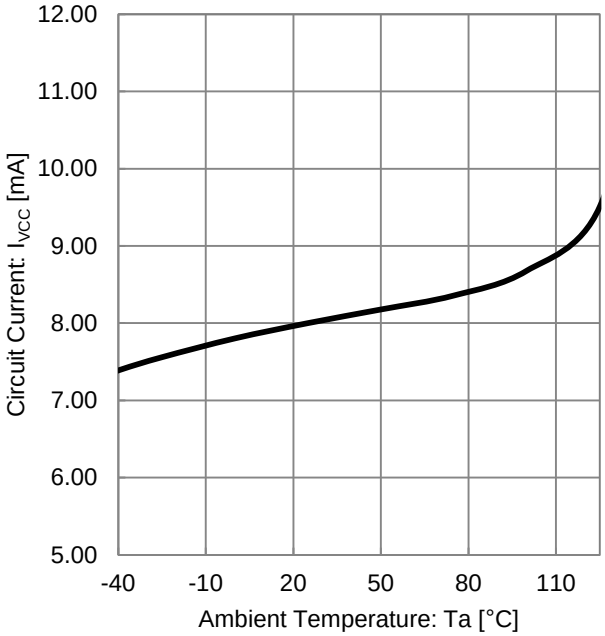



Figure 2. Circuit Current vs. Temperature

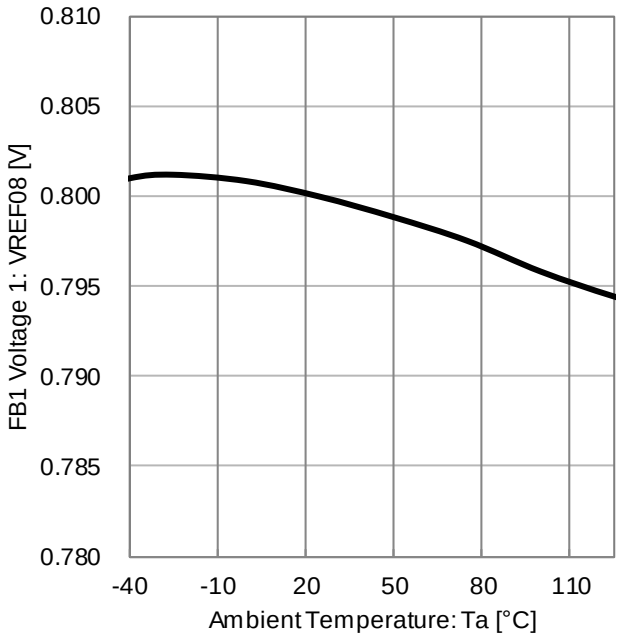



Figure 3. FB1 Voltage vs. Temperature

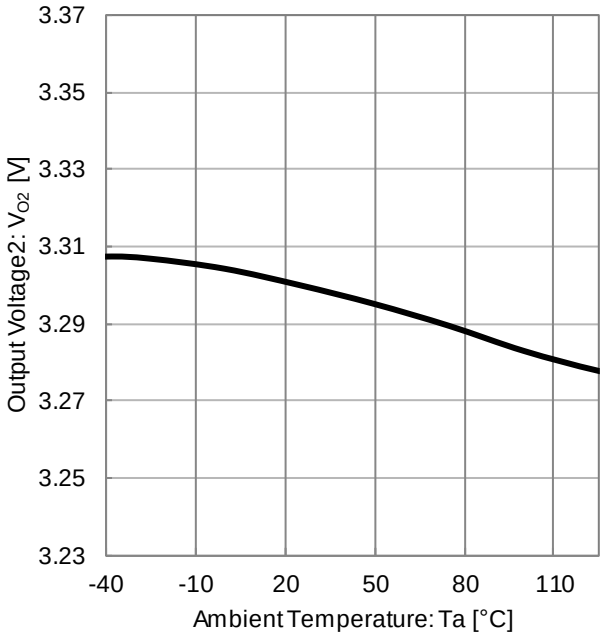



Figure 4. Output Voltage2 vs. Temperature

**Typical Performance Curves**

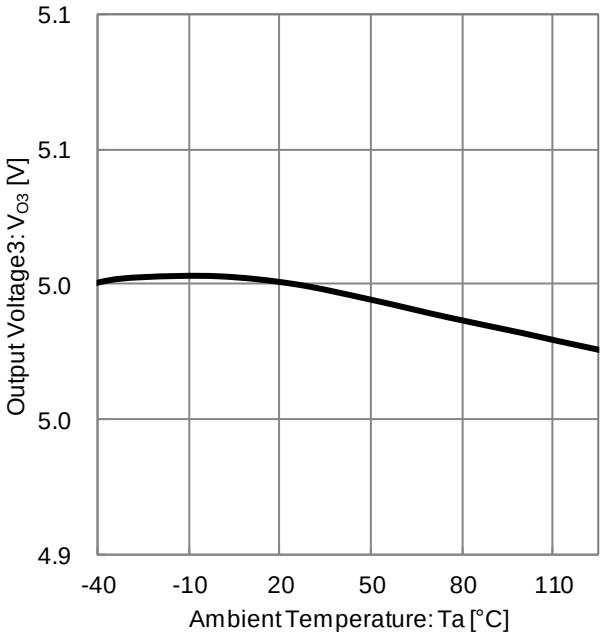



Figure 5. Output Voltage3 vs. Temperature

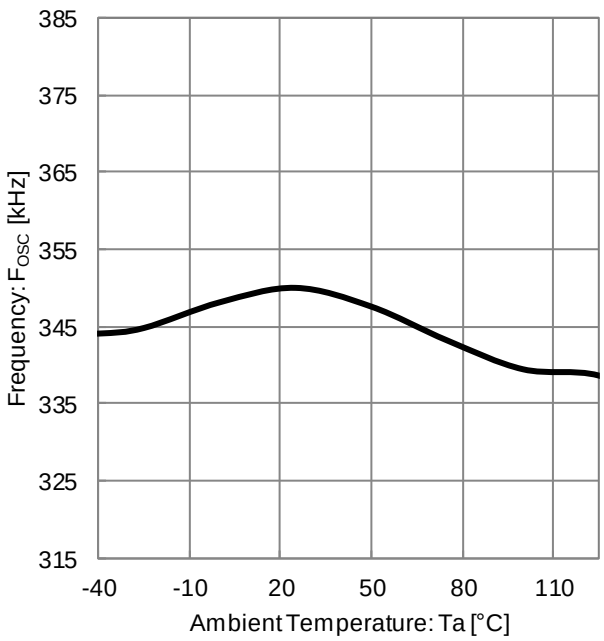



Figure 6. Frequency vs. Temperature

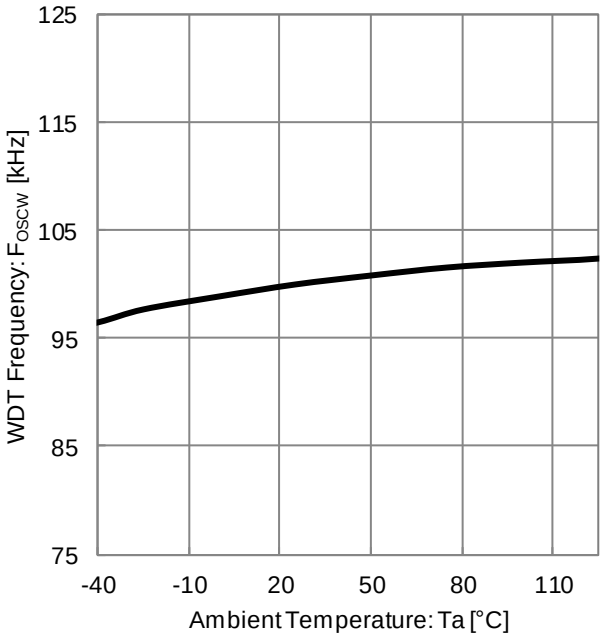



Figure 7. WDT Frequency vs. Temperature

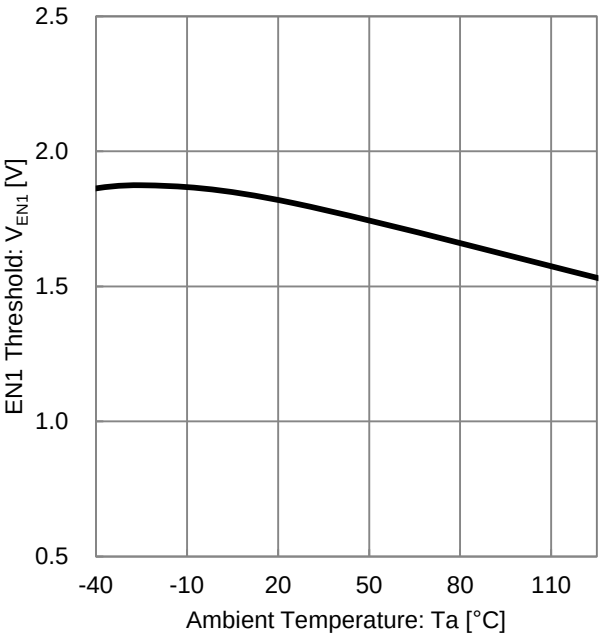



Figure 8. EN1 Threshold vs. Temperature

**Typical Performance Curves**

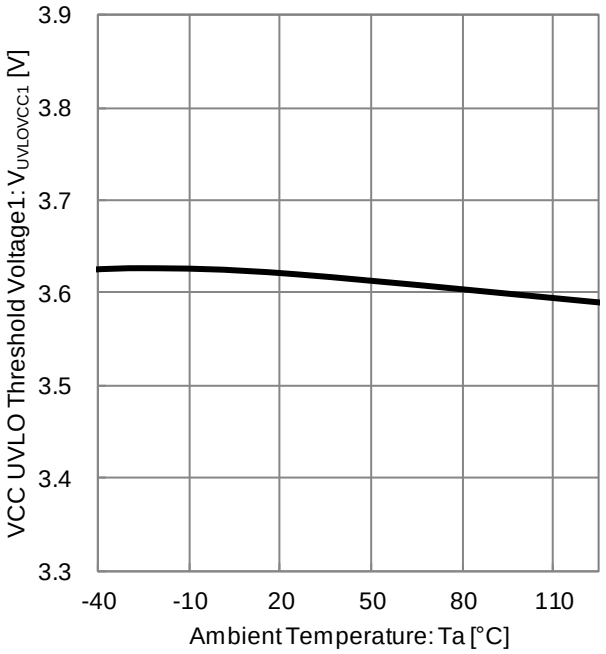



Figure 9. VCC UVLO Threshold Voltage1 vs. Temperature

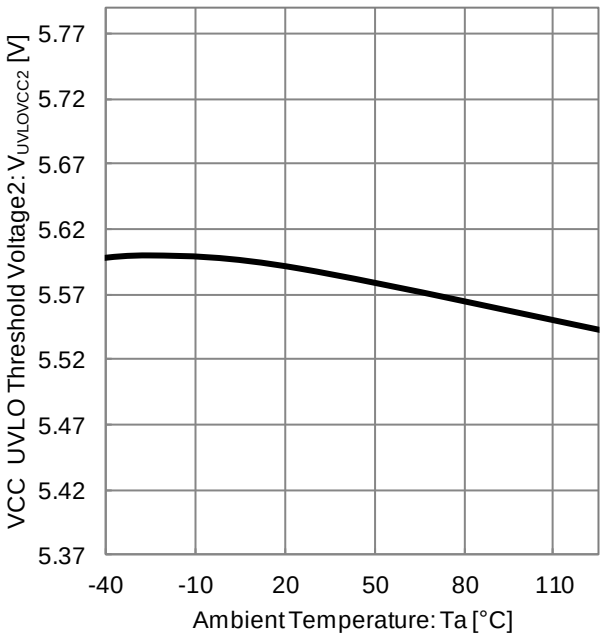



Figure 10. VCC UVLO Threshold Voltage2 vs. Temperature

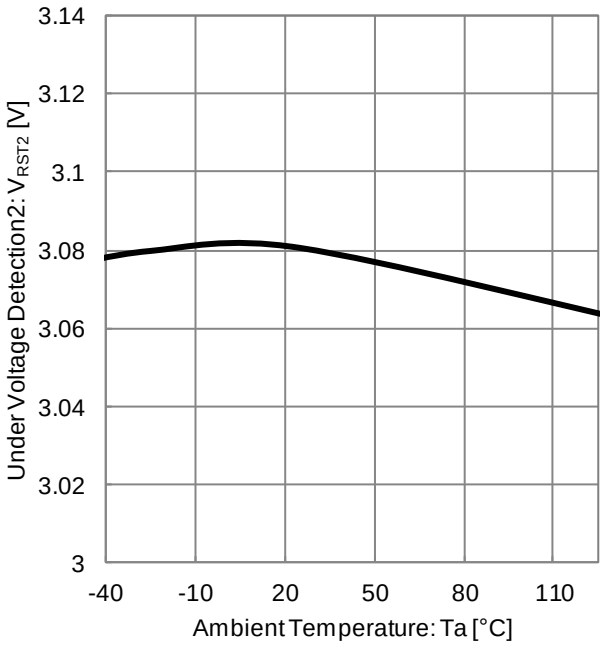



Figure 11. Under Voltage Detection2 vs. Temperature

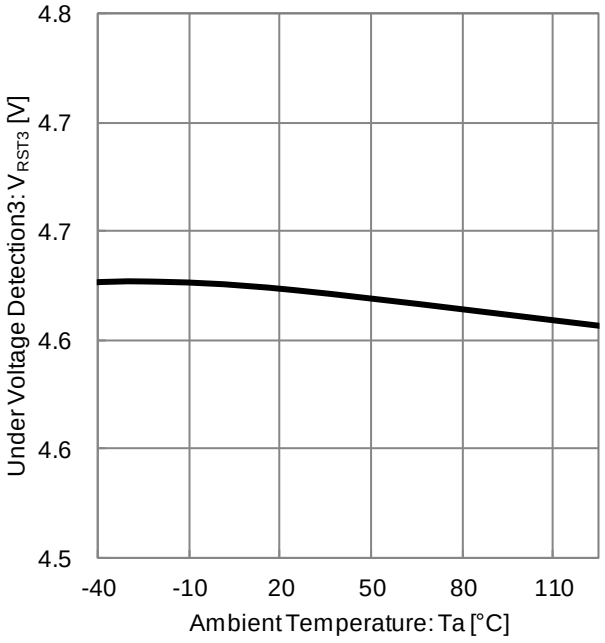



Figure 12. Under Voltage Detection3 vs. Temperature

**Typical Performance Curves**

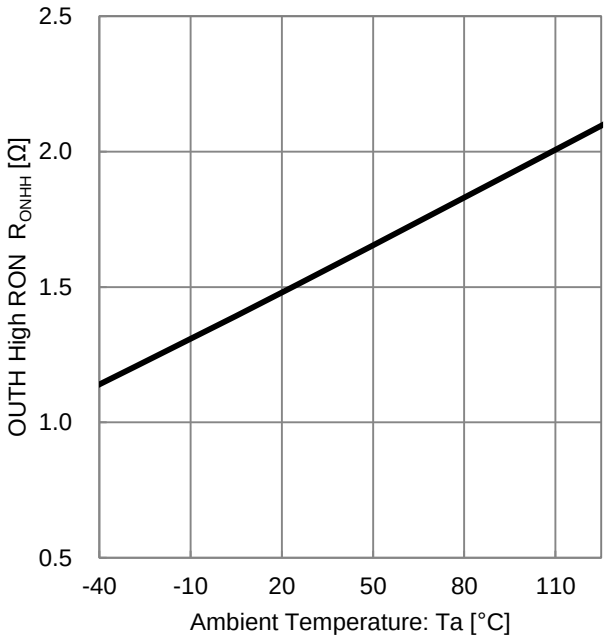



Figure 13. OUTH High RON vs. Temperature

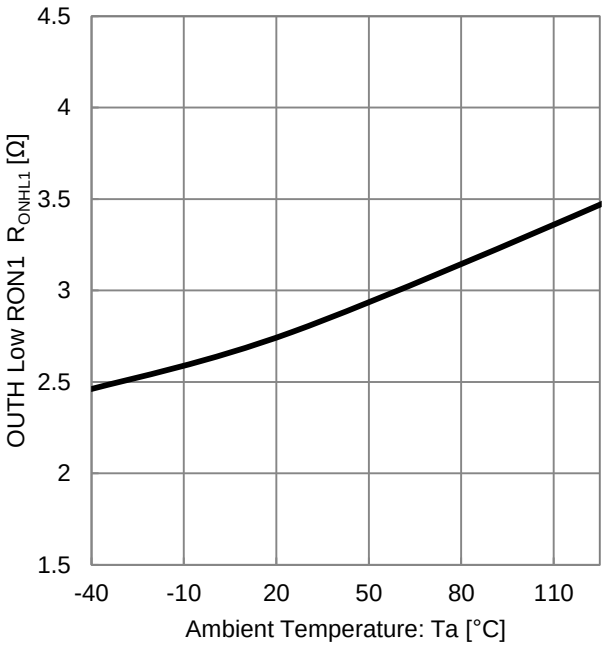



Figure 14. OUTH Low RON1 vs. Temperature

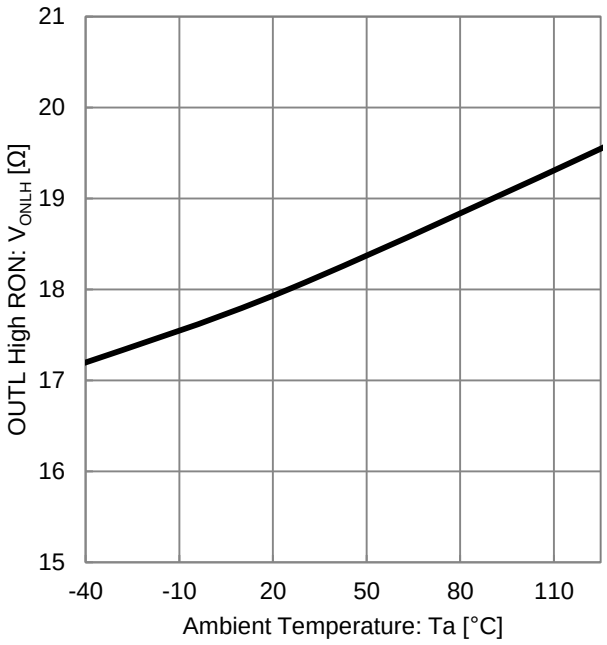



Figure 15. OUTL High RON vs. Temperature

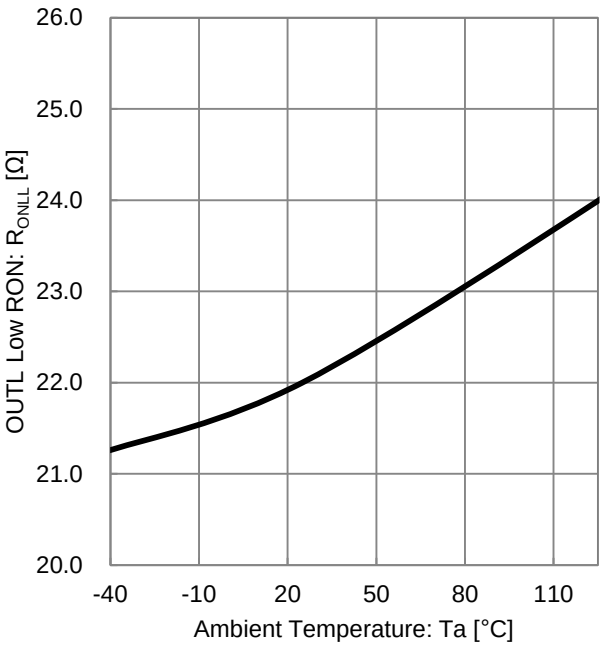



Figure 16. OUTL Low RON vs. Temperature

### Typical Performance Curves

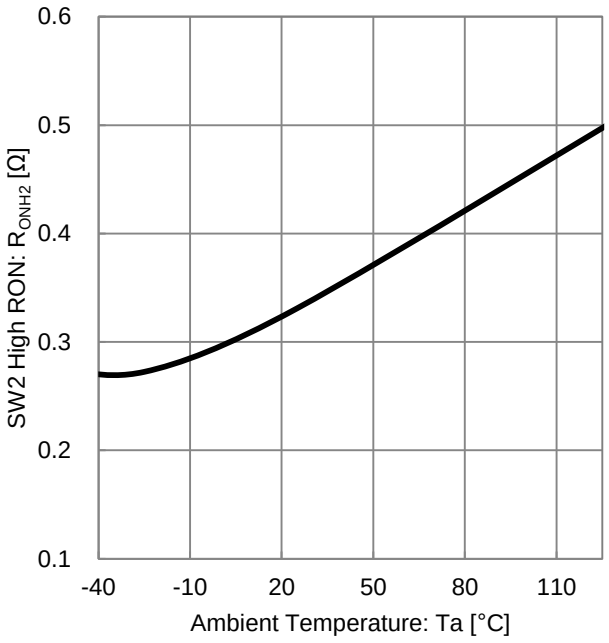



Figure 17. SW2 High RON vs. Temperature

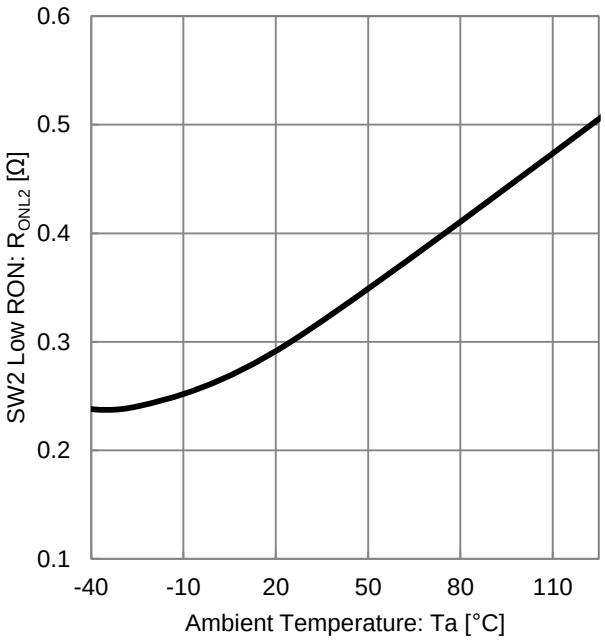



Figure 18. SW2 Low RON vs. Temperature

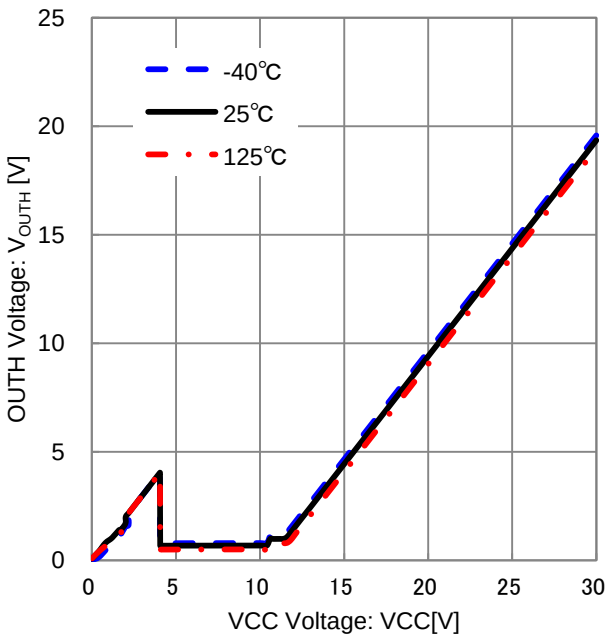



Figure 19. OUTH Voltage vs. VCC

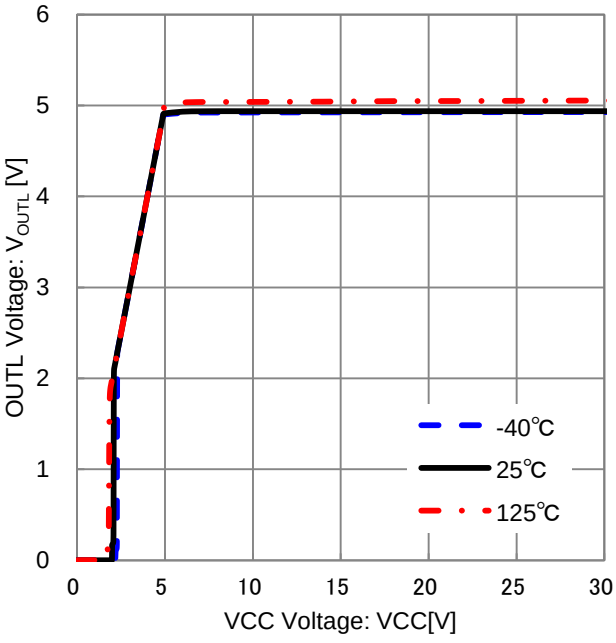



Figure 20. OUTL Voltage vs. VCC

## Description of Blocks

■ Under Voltage Lockout circuit (VCC_UVLO)
This is a Low Voltage Error Prevention Circuit.
In case of SEL_UVLO = OPEN, if the VCC drops below 3.6 V (Typ), the VCC_UVLO is activated and the output circuit shuts down. In case of SEL_UVLO = GND, if the VCC drops below 5.58 V (Typ), the VCC_UVLO is activated and the output circuit shuts down. When Vcc power supply off, Vcc voltage drop down low enough and make UVLO detect function, then the voltage of OUTH is same as VCC and OUTL is same as VDD.

■ Thermal Shut Down (TSD)
The TSD protects the device from overheating.
If the chip temperature (Tj) reaches 175 °C (Typ), the circuit shuts down

■ Oscillation Frequency (OSC)
The oscillator frequency is fixed by RT pull-down resistance value. Switching frequency of DC / DC1 and DC / DC2 are as same as OSC, but with a 180 °C difference in phase angle.

■ Over Voltage Detection (OVD)
If DC / DC1, DC / DC2 and LDO output voltage exceed OVD, each PGOOD Pin turns Low.
DC / DC1 OVD monitors FB1 voltage, DC / DC2 OVD monitors FB2 voltage and LDO OVD monitors $V_{O3}$ voltage.
PGOOD pin is an open drain output. And the pull up resistor should be connected to PGOOD for using this function.

■ Low Voltage Detection (LVD)
If DC / DC1, DC / DC2 and LDO output voltage below LVD, each PGOOD Pin turns Low.
DC / DC1 LVD monitors FB1 voltage, DC / DC2 LVD monitors FB2 voltage and LDO LVD monitors $V_{O3}$ voltage.
PGOOD pin is an open drain output, and the pull up resistor should be connected to PGOOD for using this function.

■ Under Voltage Lockout (VS_UVLO)
VS_UVLO prevents Error function at low VS voltage.
If the VS2 or VS3 drops below 3.9 V (Typ), the VS_UVLO is activated and the DC / DC2 or LDO is turned off.

■ Over Current Protection (OCP1_L, OCP1_H)
DC / DC1 has two levels over current protection with different control system as shown below.

1) OCP1 low level operations
In case the voltage between VCC and CL exceeds 100 mV (Typ), OCP1 (low level operation) is activated and the switching pulse width of OUTH and the switching pulse width of OUTL are limited. Also, if this pulse limited status continues during 256 clock times where the FB1 pin voltage drops below the under voltage detection level, the SS1 pin capacitor is discharged and the output is turned OFF during 8192 clock times.
During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 pin is recharged. The clk is the same frequency as OSC.

2) OCP1 high level operations
In case the inter VCC - CL pin voltage exceeds 200 mV (Typ), the chip goes into OCP1 high level operations, the SS1 pin capacitor is discharged and the output is turned OFF for 8192 clk. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 pin is recharged. clk and OSC has the same frequency.

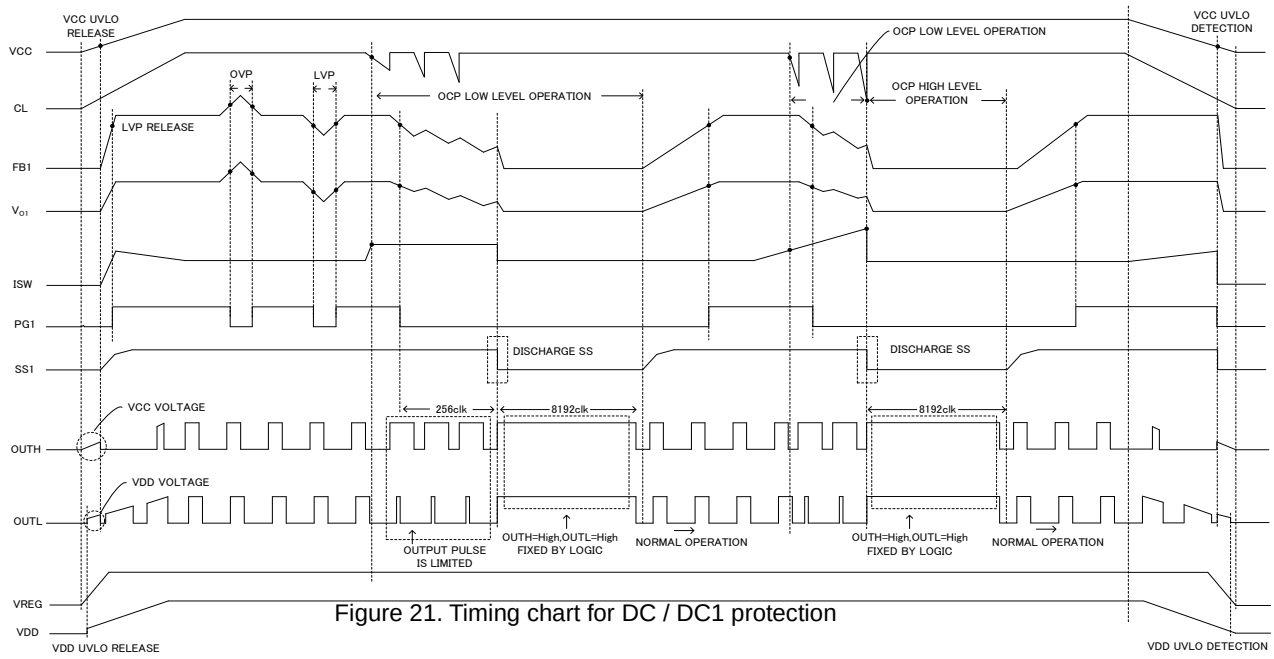



Figure 21. Timing chart for DC / DC1 protection

・DC / DC2

If output current of SW2 exceeds OCP, SW2 ON duty is limited and the output voltage is lowered.
If FB2 voltage is below SCP and after 256 clk, DC / DC2 is turned off. After 256 clk, DC / DC2 return to normal operation. The clk is the same frequency as OSC.

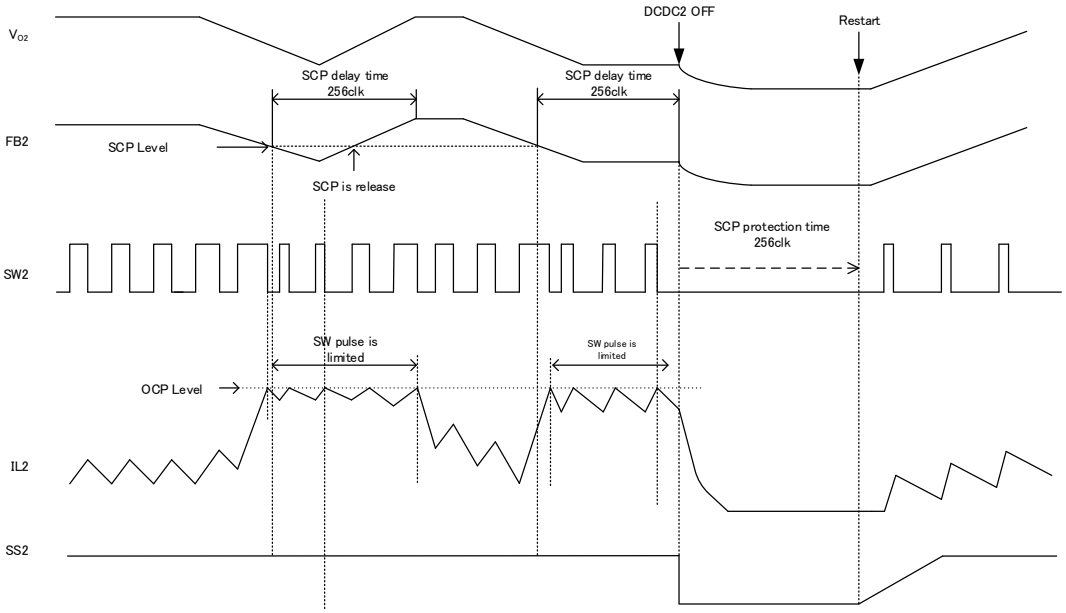
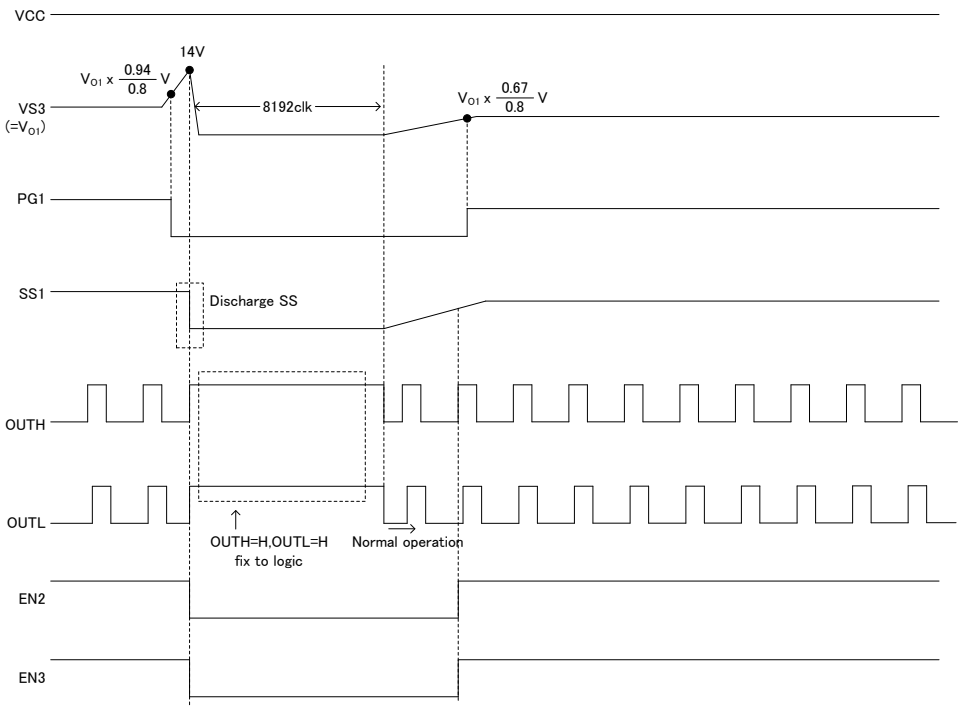



Figure 22. DC / DC2 Over current protection

・If the output current of LDO exceed OCP, the output current is limited and the output voltage is lowered. (fold-back OCP)

■ Over Voltage Protection (VS3 OVP)

・In case the VS3 voltage exceeds 14 V (Typ), the chip goes into VS3 OVP, the SS1 capacitor is discharged and the output is turned OFF for 8192 clock. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 is recharged. The clk is the same frequency as OSC.




All numerical values are Typical.

Figure 23. VS3 Over voltage protection

■ RST#, RSTWD# pin

In case of ENWD = L, RSTWD# voltage is pull up voltage.
In case of ENWD = H, WDT operation starts. If WDT is in abnormal condition, RSTWD# outputs 'L'.
If $V_{O2}$ or $V_{O3}$ voltage is below the LVD, reset voltage (RST#) output is low.
If both of $V_{O2}$ and $V_{O3}$ exceed the reset release voltage, CT is charged. After tPOR, reset voltage outputs high.

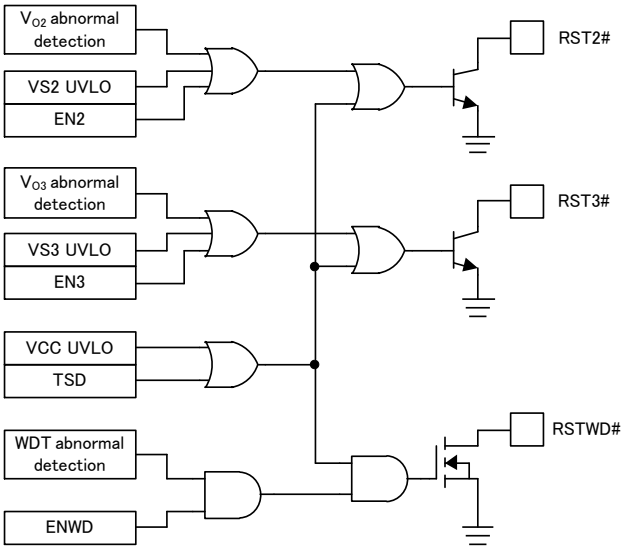



Figure 24. RST#, RSTWD# Logic Circuit

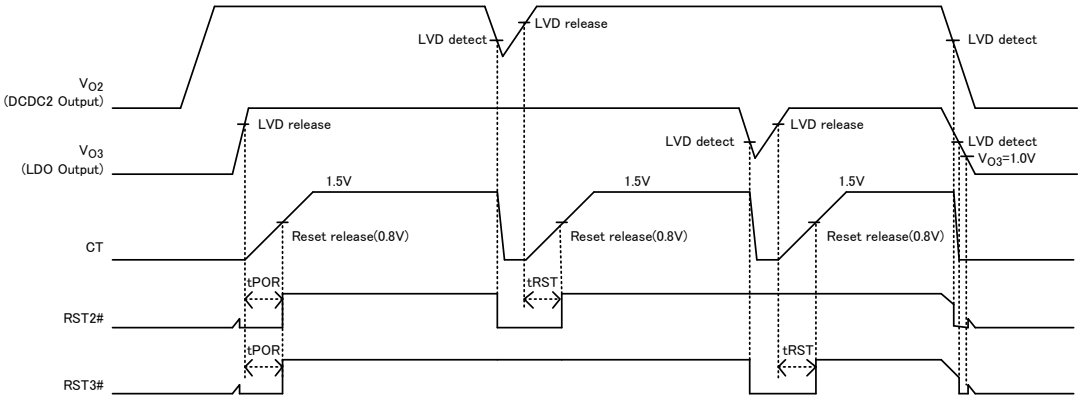



Figure 25. RST2#, RST3# Timing Chart

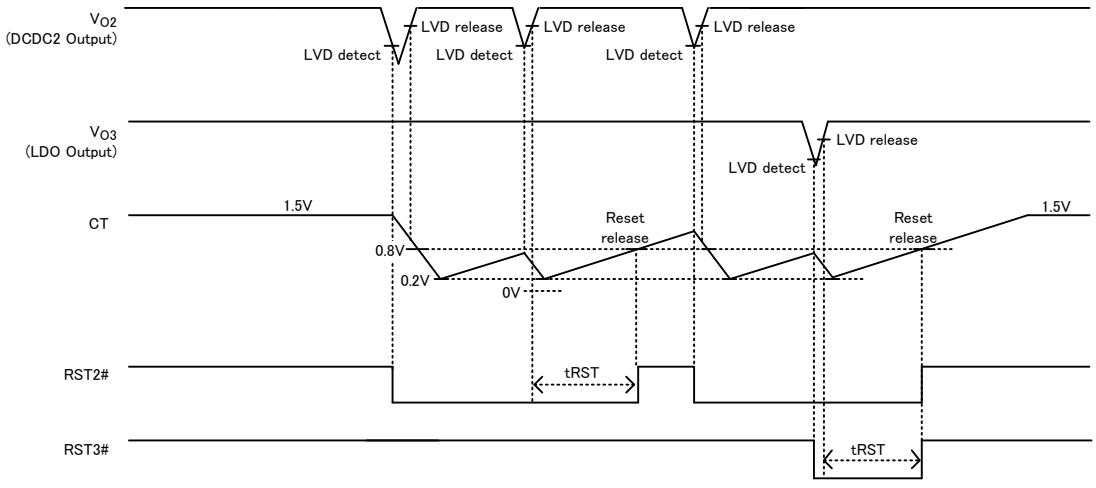



Figure 26. Timing chart (detection of LVD between reset)

■ Oscillator for Watch Dog Timer (FOSCW)

This block creates a reference frequency of the Watch Dog Timer. The oscillation frequency is determined by the RTW resistance. The oscillation frequency can be set in the range of 50 kHz to 250 kHz.

■ WATCH DOG TIMER

Microcontroller (μC) operation is monitored with CLK pin. Window watch dog timer is included to enhance the assurance of the system. WDT starts operating when ENWD becomes high. CLK pin voltage must be Low when ENWD switches to High.

WDT monitors both edges of CLK pin (rising edge and falling edge). If width of both edges are shorter than Fast NG or longer than Slow NG, $R_{STWD}$ turns low for a WDT reset time ($t_{WRES}$). Since the width of Fast NG and Slow NG depends on a number of $F_{OSCW}$, Fast NG and Slow NG are variable by frequency of $F_{OSCW}$. If $F_{OSCW}$ is unusual (ex. RTW is short to ground), $R_{STWD}$ turns low. In case of using RSTWD, pull-up resister is needed because RSTWD is an open drain.

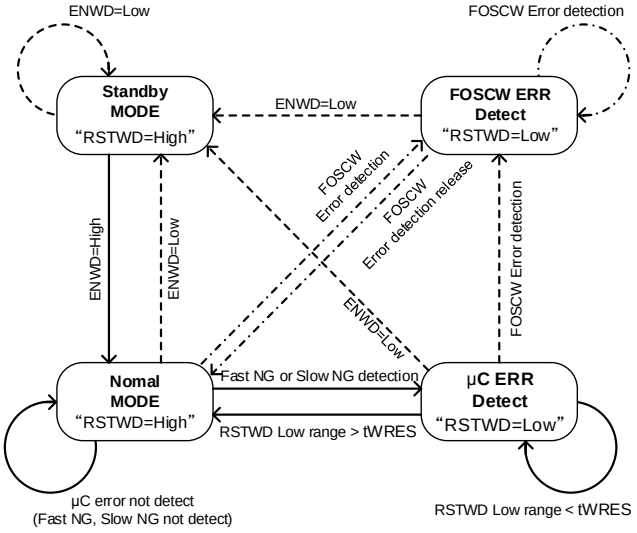
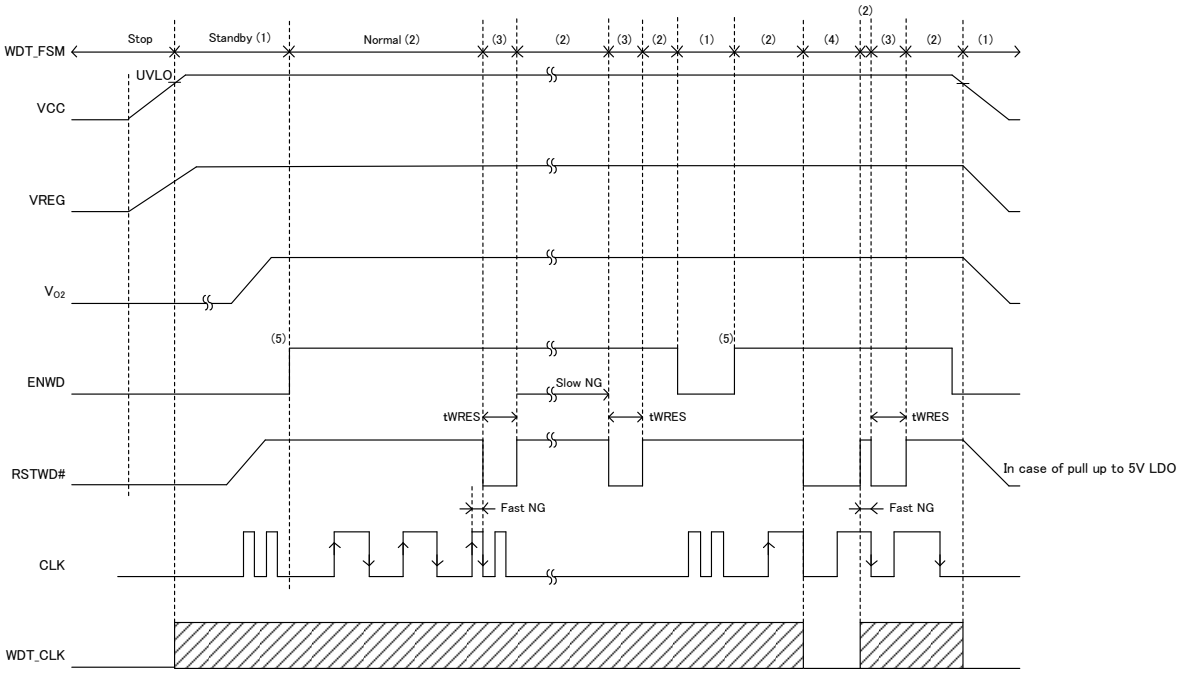



Figure 27. Witch Dog Timer State Change Diagram (WDT FSM)




(1): Standby Mode, (2): Normal Mode, (3): Microcontroller Error Detect, (4): OSC_WDT Error Detect (See Figure 27 WDT FSM)
(5): When ENWD is changed Low to High, it is necessary that CLK is Low.

Figure 28. WDT Timing Chart

### External Components Selection

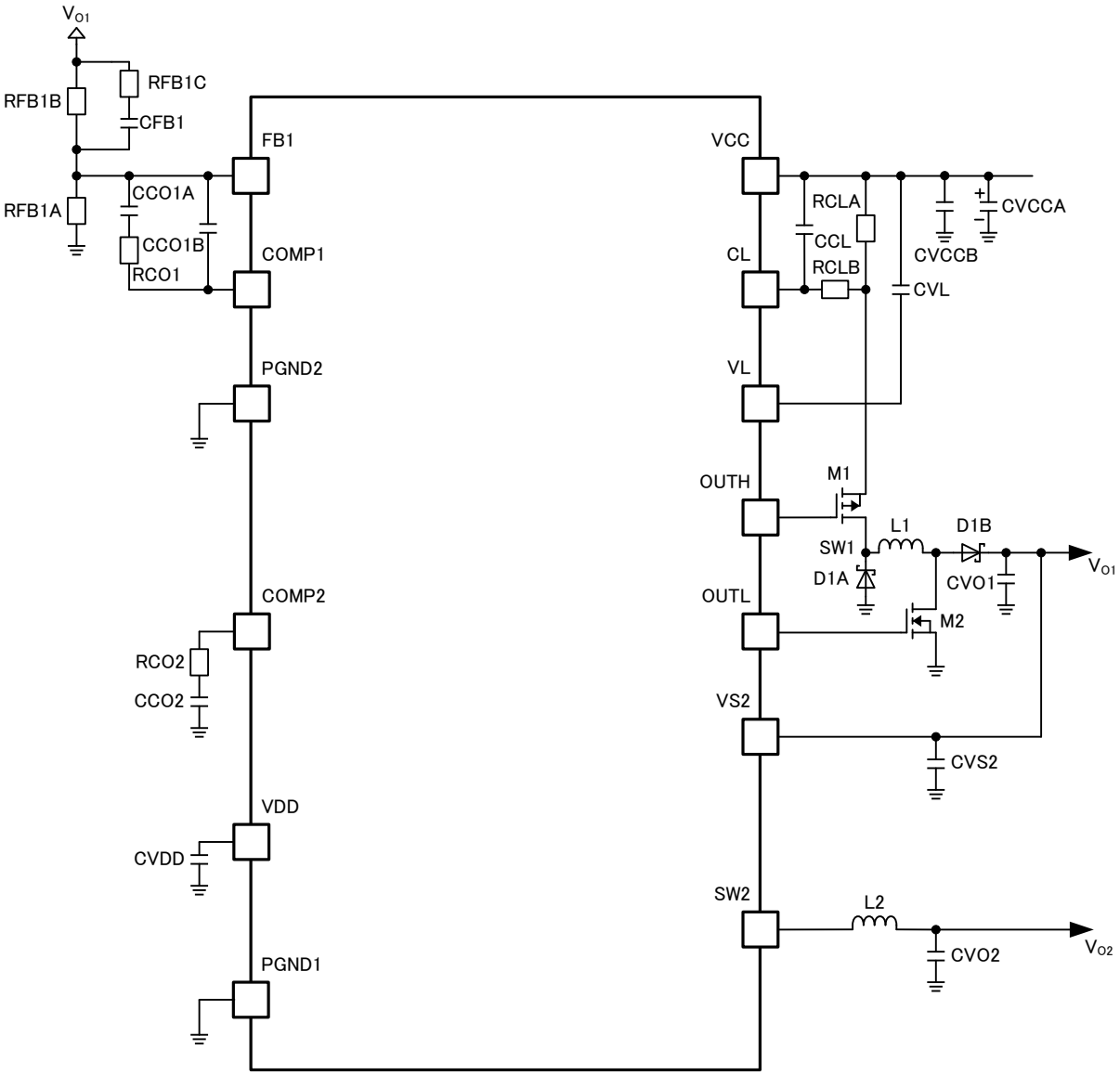



Figure 29. Application Example 1

(1) Buck mode ($V_{CC}$>>$V_{O1}$)
In case the input voltage is high compared to the output voltage, the chip will go into buck mode, resulting OUTH to repeatedly switch between H and L and that the OUTL will go to L (= OFF).
This operation is the same as that of standard step-down switching regulators.
Shown below are the OUTH and OUTL waveforms on the right.
ON duty of PMOS ($D_{pon}$), VCC and $V_{O1}$ are shown in the following equation.

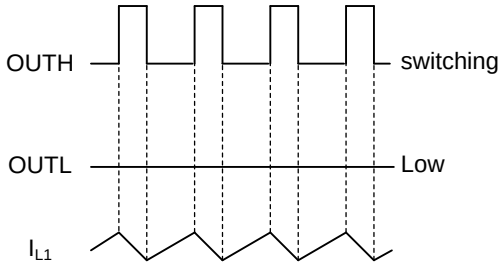



Figure 30

$$V_{cc} \times D_{pon} = V_{O1} \quad \text{(eq. 1)}$$

(2) Buck-Boost mode ($V_{CC}$ ≈ $V_{O1}$)
In case the input voltage is close to the output voltage, the chip will go into buck-boost mode, resulting both the OUTH and OUTL to repeatedly switch between H and L. Concerning the OUTH, OUTL timing, the chip internally controls where the following sequence is upheld; when OUTH: H → L, OUTL: H → L.
Shown below are the OUTH and OUTL waveforms.

① $V_{CC}$ > $V_{O1}$

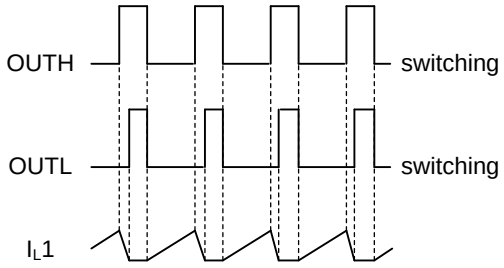



Figure 31

② $V_{CC}$ < $V_{O1}$

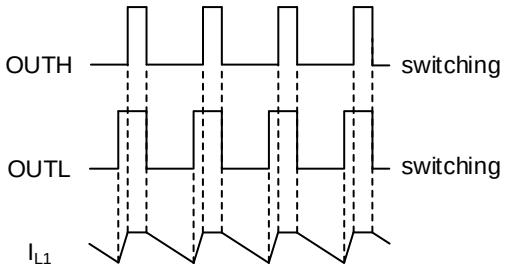



Figure 32

*The timing excludes the SW delay

The relationship between ON duty of PMOS ($D_{pon}$), ON duty of NMOS ($D_{non}$), $V_{CC}$ and $V_{O1}$ is shown in the following equation.

$$\frac{V_{cc} \times D_{pon}}{(1-D_{non})} = V_{O1} \quad \text{(eq. 2)}$$

The calculation formula of $D_{pon}$ and $D_{non}$ are shown in page 20.

(3) Boost mode ($V_{CC}$ << $V_{O1}$)
In case the input voltage is low compared to the output voltage, the chip will go into boost mode, resulting OUTH to go to L (= ON) and OUTL will repeatedly switch between H and L. This operation is the same as that of standard step-up switching regulators.
Max duty of OUTL is limited by internal circuit.
ON duty of NMOS ($D_{non}$), $V_{CC}$ and $V_{O1}$ are shown in the following equation.

$$V_{O1} \times (1 - D_{non}) = V_{cc} \quad \text{(eq. 3)}$$

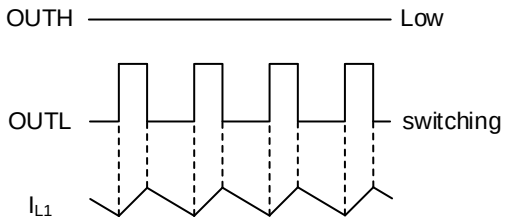



Figure 33

(4) Voltage for Mode Switching and Duty Control

In the event of mode switching from Boost to Buck-Boost or vice versa, mode switching input voltage is dependent on output voltage, the gain of inverting amplifier and the cross duty. The general description is shown below.

The duty of OUTH is controlled by output of error amp (COMP1) and SLOPE voltage.
Also, OUTL duty is controlled by the output voltage of the inverting amplifier in chip (BOOSTCOMP) and SLOPE voltage.
In case VCC = $V_{O1}$, COMP1 voltage becomes equal to BOOSTCOMP voltage, and switching control timing of OUTH and OUTL becomes identical accordingly.

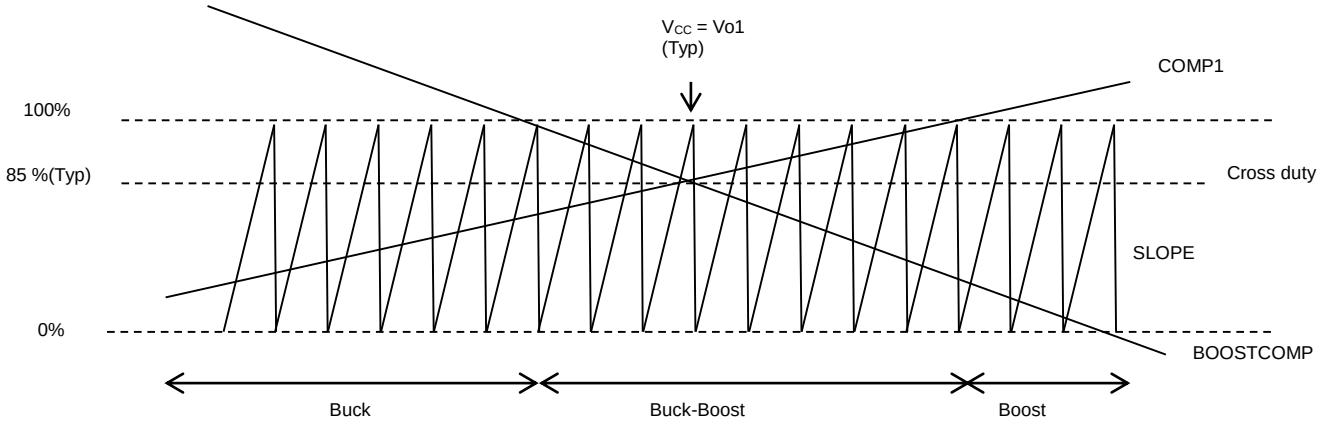



Figure 34. Buck-Boost operation controlled by COMP1, BOOSTCOMP and SLOPE voltage

ON duty of PMOS in this condition is called the cross duty (Dx = 0.85, Typ). $D_{pon}$ and $D_{non}$ can be calculated by the following equation, assuming the gain of the inverting amplifier as A (1.5, Typ).

$$D_{non} = 1 - D_X + A(D_{pon} - D_X)$$

$$= 1.5D_{pon} - 1.125 \quad \text{(Note 1)} \quad \text{(eq. 4)}$$

From eq.3, eq.4 and $D_{pon}$ = 1, the input voltage at transition between buck - boost and boost mode is calculated as follows;

$$V_{CC} = \{D_X - A(1 - D_X)\}V_{O1}$$

$$= 0.625 \times V_{O1} \quad \text{(Note 1)} \quad \text{(eq. 5)}$$

Also, from eq.1, eq.4 and $D_{non}$ = 0, the input voltage at transition between buck - boost and buck mode is calculated as follows;

$$V_{CC} = \frac{V_{O1} \times A}{\{(1+A)D_X - 1\}} = 1.333 \times V_{O1} \text{ (Note 1)}$$

Be sure to confirm Dx and A value under the actual application because these parameters vary depending on conditions of use and external components selected.
Dx varies with oscillating frequency shown in Figure 35.
In addition, 'A' value can be calculated by $D_{non}$ / $D_{pon}$.

(Note 1) A = 1.5 (Typ), Dx = 0.85 (Typ)

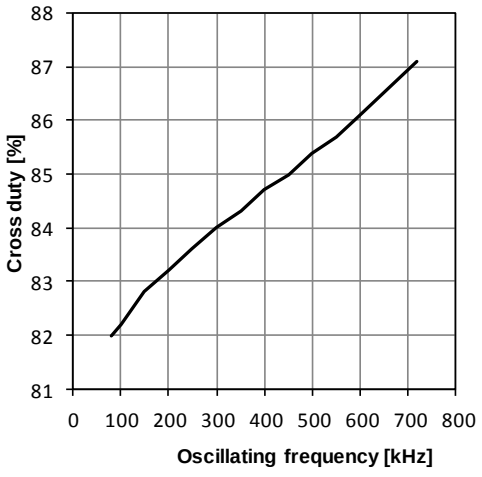



Figure 35. Cross duty vs. frequency characteristics

1. Setting the output L1, L2 value (DC / DC1, DC / DC 2)

It is necessary to use LC filter. The use of a big inductor helps lower the inductor ripple current and output ripple voltage, even though cost is higher and the size is bigger.
The inductance is shown in the following equation.
The coil value significantly influences the output ripple current. Thus, as seen bellow, the larger coil and the higher switching frequency, the lower ripple current it becomes. The optimal output ripple current setting is 30 % of maximum current.

・DC / DC1 (at Buck - Boost)

| Buck mode | Buck-Boost mode | | Boost mode |
|---|---|---|---|
| | VCC > $V_{O1}$ | VCC < $V_{O1}$ | |
| $\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times V_{O1}}{L1 \times V_{CC} \times f}$ | $\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times D_{pon}}{L1 \times f}$ | $\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times D_{noff}}{L1 \times f}$ | $\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times V_{CC}}{L1 \times V_{O1} \times f}$ |
| $\overline{I_{L1}} = I_{O1}$ | $\overline{I_{L1}} = \frac{I_{O1}}{D_{noff}}$ | | |

$\Delta I_L$: Ripple current, $\overline{I}_L$: Average coil current, f: Oscillating frequency

$D_{pon}$: $$\text{PMOS ON } duty = V_{O1} \times Dx\,(1+A) \,/\, (V_{CC} + A \times V_{O1}) = 2.13 \times V_{O1} \,/\, (V_{CC} + 1.5 \times V_{O1}) \quad (Typ)$$

$D_{noff}$: $$\text{NMOS OFF } duty = (1+A) \times Dx - A \times Dpon = 2.13 - 1.5 \times Dpon \quad (Typ)$$

・DC / DC1 (at Buck)

$$\Delta I_{L1} = \frac{(V_{CC(MAX)} - V_{O1}) \times V_{O1}}{V_{CC(MAX)} \times f_{SW} \times L1}$$

($V_{CC\,(MAX)}$: Maximum input voltage, $\Delta I_{L1}$: Inductor ripple current, $V_{O1}$: Output voltage 1, $f_{SW}$: Oscillating frequency)

・DC / DC2 (at Boost)

$$\Delta I_{L2} = \frac{(V_{S2(MAX)} - V_{O2}) \times V_{O2}}{V_{S2(MAX)} \times f_{SW} \times L2}$$

($V_{S2\,(MAX)}$: Maximum input voltage, $\Delta I_{L2}$: Inductor ripple current, $V_{O2}$: Output voltage 2, $f_{SW}$: Oscillating frequency)

An output current in excess of the coil current rating will cause magnetic saturation to the coil and decrease efficiency.
The following equation shows the peak current $I_{LMAX}$ assuming the efficiency as η.
It is recommended to secure sufficient margin to ensure that the peak current does not exceed the coil current rating.

$$I_{LMAX} = \frac{1}{\eta}\left(\overline{I_L} + \frac{\Delta I_L}{2}\right)$$

Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

When load current is low, DC / DC1 operates discontinuously so set $\Delta I_L$ in a way it operates continuously ($I_{L1}$ keeps continuously flowing).
The condition of continuous operation is shown in the following equation.

・DC / DC1

$$I_{O1} > \frac{(V_{CC} - V_{O1}) \times V_{O1}}{2 \times V_{CC} \times f_{SW} \times L1}$$

($I_{O1}$: Load current)

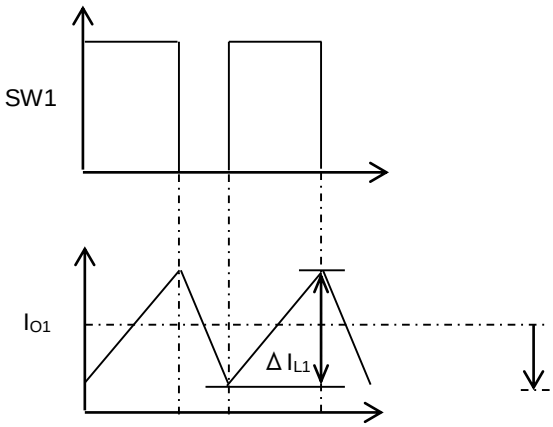



Figure 36. Continuous operation

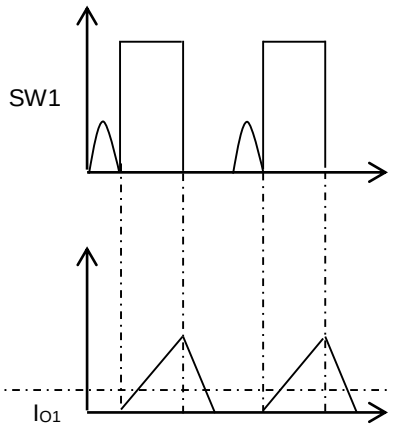



Figure 37. Discontinuous operation

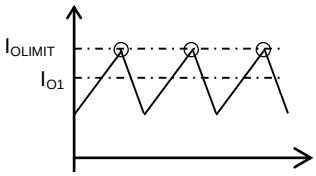



Figure 38. Over current detection

Shielded type inductor (closed magnetic circuit) is recommended. Open magnetic circuit type inductor can be used for low cost applications if noise is not of concern. But in this case, there is magnetic field radiation between the parts and thus keep enough spacing between the parts.

For ferrite core inductor type, please note that magnetic saturation may occur. Saturation needs to be avoided at all times. Precautions must be taken into account on the given provisions of the current rating because it differs according to each manufacturer.

Please confirm the rated current at the maximum ambient temperature of the application to the coil manufacturer.

2. Setting the output capacitor $C_{VO1}$, $C_{VO2}$ value (DC / DC1, DC / DC 2)

The maximum output current is limited by the over current protect operation current as shown in below equation.

$$I_{O(MAX)} = I_{LIMIT(MIN)} - \frac{\Delta I_L}{2}$$

$I_{O\ (MAX)}$: Maximum output current, $I_{LIMIT\ (MIN)}$: Minimum over current protect operation level (0.9 A) (1ch is external set)
When the $\Delta I_L$ is low, the Inductor core loss (iron loss), the loss due to ESR of the output capacitor and the $\Delta V_{PP}$ will become low. $\Delta V_{PP}$ is expressed as follows:

| Buck mode | Boost mode |
|---|---|
| $\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{8 \times C_{VO} \times f_{SW}}$ | $\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{I_O}{C_{VO} \times f_{SW}} \times \frac{V_O - V_{CC}}{V_O}$ |

(*ESR*: Output capacitor equivalence series resistance, $C_O$: Output capacitor volume)

By using small ESR capacitor, $\Delta V_{PP}$ voltage level can be lowered. The benefit of ceramics capacitor is low ESR and small form factor.

The frequency characteristic of ESR from the datasheet of the manufacturer should be confirmed. Choose the ceramic capacitor which exhibits low ESR in the switching frequency range that is used On the other hand, DC biasing characteristics of the ceramic capacitor is significant so it needs to be carefully examined. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R or better, is recommended.

Because the voltage rating of ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, select electrolytic capacitor.

When using electrolytic capacitors, the voltage rating should be 1.2 times or more than the output voltage. Electrolytic capacitors have a high voltage rating, large capacity, small amount of DC biasing characteristic, and are generally inexpensive. Because typical failure mode is OPEN, it is effective to use electrolytic capacitor for applications where high reliability is required such as automotive. On the other hand, disadvantages are relatively high ESR and capacitance value drop at low temperatures. In this case, please take note that $\Delta V_{PP}$ may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor.

When it comes to the capacitance $C_O$, the value needs to be less than the value calculated by the equations below.

・DC / DC 1

$$C_{O1\ (MAX)} = \frac{0.5\,ms \times (I_{L1imit\ (MIN)} - I_{O1\ (MAX)})}{V_{O1}}$$

・DC / DC 2

$$C_{O2\ (MAX)} = \frac{0.4\,ms \times (I_{L2imit\ (MIN)} - I_{O2\ (MAX)})}{V_{O2}}$$

($I_{LIMIT\ (MIN)}$: Minimum over current protect operation current (1ch is external set). 2ch = 0.9 A.
Soft start Min time DC / DC1: 0.5 ms, DC / DC2: 0.4 ms, Soft start setting refer to page 34)

Boot failure may occur if the capacitance value exceeds the limits explained above. If the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup, and the output may not start.
Please confirm this on the actual circuit.

Capacitance values are critical parameter to determine the LC oscillation frequency. Transient response and loop stability are dependent on the $C_{VO}$. Please select after confirming the setting of the phase compensation circuit.

3. Setting the input capacitor $C_{VCCA}$ / $C_{VCCB}$, $C_{VS2}$ value (VCC, VS2)

Input capacitors reduce the power output impedance that is connected to VCC. Two types of capacitors are needed for input capacitor, i.e., decoupling capacitor $C_{VCCB}$ and bulk capacitor $C_{VCCA}$. The decoupling capacitors of VCC and VS2 need to be 1 µF to 10 µF ceramics. More than 22 µF are necessary for the bulk capacitor of VCC. The ceramic capacitors are most effective when placed as close to VCC and VS2 as possible. At VCC, the ceramic capacitors need to be placed between VCC and GND and close to PMOS and the ground of schottky barrier diode. At VS2, the ceramic capacitor needs to be placed between VS2 and GND. Voltage rating is recommended to be more than 1.2 times the maximum input voltage and twice the normal input voltage.

The bulk capacitor prevents line voltage drop and serves as a backup power supply to maintain the input voltage. The low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the capacitance value which best fits to each application. In case impedance of input side is high such as long wiring between the power supply and VCC, input voltage gets unstable when output impedance of the power supply increases resulting in oscillation or degraded ripple rejection characteristics. Large capacitor is needed in this case. It is necessary to verify that the output does not turn off in the event of Vcc drop due to transient in the actual circuit.
Make sure not to exceed the rated ripple current of the capacitor in this case. The RMS of the input ripple current can be obtained from the following equation.

・DC / DC 1

$$I_{CVCCB\,(RMS)} = I_{O1} \times \frac{\sqrt{V_{O1}\,(V_{CC} - V_{O1})}}{V_{CC}}$$

($I_{CVCCB\,(RMS)}$: Input ripple current RMS value)

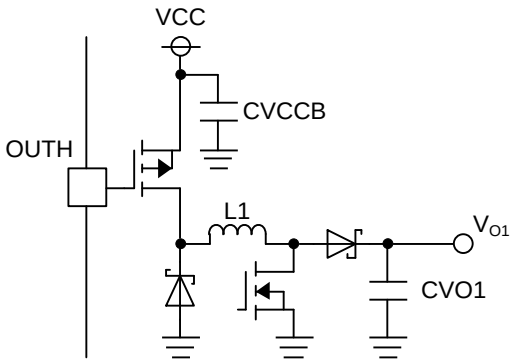



Figure 39. VCC pin

・DC / DC 2

$$I_{CVS2\,(RMS)} = I_{O2} \times \frac{\sqrt{V_{O2}\,(V_{S2} - V_{O2})}}{V_{S2}}$$

($I_{CVS2\,(RMS)}$: Input ripple current RMS value)

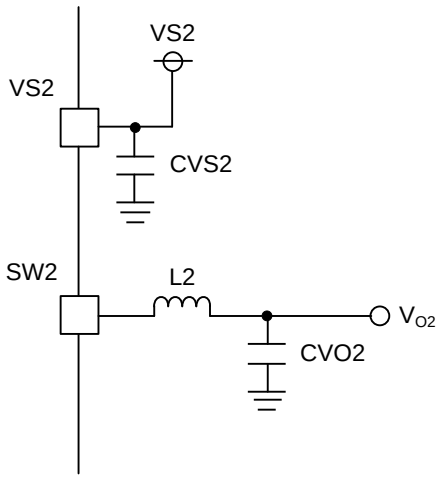



Figure 40. VS2 pin

In automotive and other applications requiring high reliability, it is recommended that capacitors are connected in parallel to reduce the risk of electrolytic capacitors drying out. In case of ceramic capacitors, it is recommended make it two in series and two in parallel structures to reduce the risk of destruction due to short circuit event. Currently capacitors containing two in series or two in parallel in one package are available in the market so please contact suppliers.

4. Setting the input capacitor $C_{VS3}$ value

Place a capacitor which is greater than 0.1 µF between VS3 and GND. Select the capacitor considering filter circuit for power supply and VS3. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor. Capacitors that have good voltage and temperature characteristics are recommended.

5. Setting the output capacitor $C_{VREG}$ value

Place a capacitor between the VREG pin and GND to avoid oscillation. 0.47 µF or greater capacitance is recommended. $C_{VREG}$ can be electrolytic capacitor or ceramic capacitor. Secure the capacitance of 0.47 µF or greater in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.

6. Setting the output capacitor $C_{VDD}$ value

Place a capacitor between VDD and GND. The capacitance needs to be 0.01 µF or greater (OUTL = open) and1 µF or greater (OUTL in use). $C_{VDD}$ can be electrolytic or ceramic. Secure high enough capacitance in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.

7. Setting the internal drive circuit supply capacitor $C_{VL}$ value

Add the capacitor greater than 0.1 µF between VCC and VL. Select the capacitor considering the filter circuit for power supply and VL. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor.

8. Setting output voltage ($V_{O1}$)

$V_{O2}$ and $V_{O3}$ are fixed output while $V_{O1}$ is adjustable.
$V_{O1}$ output voltage is determined by the following equation.

$$V_{O1} = 0.8 \times \frac{R_{FB1A} + R_{FB1B}}{R_{FB1A}}$$

Please set feedback resistor RFB1A below 30 kΩ to reduce the error margin by the bias current. In addition, since power efficiency is reduced when RFB1A + RFB1B is small, please set the current flowing through the feedback resistor small enough as compared to the output current $I_{O1}$.

9. Selection of the MOSFET (M1, M2)

In case of Buck-Boost DC / DC, DC / DC1 needs 2 external MOSFET (PMOS = M1 and NMOS = M2). In case of Buck DC / DC, DC / DC1 needs 1 external MOSFET (PMOS). Key parameters in choosing MOSFET are voltage and current rating.

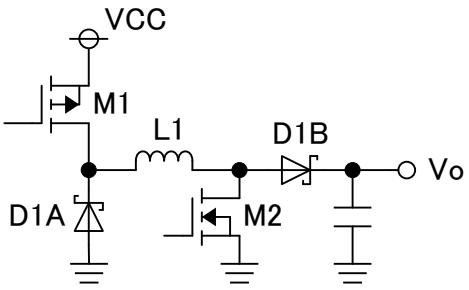



Figure 41. Select MOSFET

( i ) PMOS

- $V_{ds}$ maximum rating > VCC
- $V_{gs}$ maximum rating > Lower value of 13 V or VCC

  * The voltage between VCC - VL is kept at 10 V (Typ), 12 V (Max).
    VL become 0 V when VCC become less than 10.3 V (Typ)
- Allowable current > coil peak current $I_{LMAX}$

  * A value above the over current protection setting is recommended.
  * Choosing a low ON Resistance FET results in high efficiency.

( ii ) NMOS

- $V_{ds}$ maximum rating > $V_O$
- $V_{gs}$ maximum rating > $V_{DD}$
- Allowable current > Coil peak current $I_{LMAX}$

  * A value above the over current protection setting is recommended.
  * Choosing a low ON Resistance FET results in high efficiency.

10. Selection of the schottky barrier diode

The diode D1A needs to be low Vf and fast Trr. Key parameters in the diode selection are average rectified current and DC reverse voltage. Average rectified current $I_{F\,(AVG)}$ can be obtained from the following equation:

$$I_{F\,(AVG)} = I_{O1\,(MAX)} \times \frac{V_{CC\,(MAX)} - V_{O1}}{V_{CC\,(MAX)}}$$

($I_{F\,(AVG)}$: Average rectified current)

The absolute maximum rating of the average rectified current in D1A needs to be 1.2 times or greater than the $I_{F\,(AVG)}$.
The absolute maximum rating of the DC reverse voltage in D1A needs to be 1.2 times or greater than the maximum input voltage.
The DIA and DIB's diode power loss can be obtained by the following equation:

$$P_{D1A} = I_{o1\,(MAX)} \times \frac{V_{CC\,(MAX)} - V_{O1}}{V_{CC\,(MAX)}} \times VF \qquad P_{D1B} = I_{o1\,(MAX)} \times VF$$

(*VF*: Forward voltage of $I_{O1\,(MAX)}$)

Selecting D1A and D1B diode that have low forward voltage and fast reverse recovery time will help achieve a high efficiency. Select a diode with 0.6 V or lower forward voltage. The use of the diode greater than 0.6 V forward voltage may cause inner element destruction so care has to be taken. The reverse recovery time of the schottky barrier diode is so short and thus its switching loss is ignorable. If the diode needs to withstand the event of output short-circuit, absolute maximum ratings and power dissipation need to be even higher. The maximum rated current needs to be approximately 1.5 times of the over current detection value. The D1A and D1B's diode power loss at the event of output short-circuit can be obtained by the following equation.

$$P_{Di\,(SHORT)} = I_{LIMI\,T\,(MAX)} \times VF$$

($I_{LIMIT\,(MAX)}$: $V_{O1}$ Maximum over current protect operation current)

11. Setting the oscillation frequency (DC / DC1, DC / DC2)

The internal oscillation frequency can be set by changing the resistance value connected to RT pin. Frequency can be set in the range of 250 kHz to 550 kHz. The following table shows the resistance value and its corresponding oscillation frequency. Switching may stop if the oscillation frequency is set outside of the recommended frequency range and thus normal operation is not guaranteed in such case.

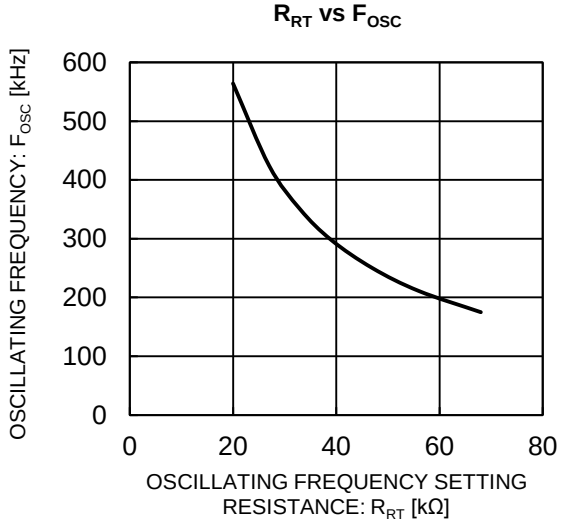



Figure 42. RT resistance vs. oscillation frequency

| $R_{RT}$ [kΩ] | $F_{OSC}$ [kHz] |
|---|---|
| 20 | 564 |
| 27 | 424 |
| 33 | 350 |
| 39 | 298 |
| 47 | 250 |
| 56 | 211 |
| 68 | 175 |

*The oscillation frequency graph is typical. A certain variation exists in actual usage.

12. Setting the phase compensation circuit (DC / DC1)

Circuit stability and transient response characteristics are determined by phase compensation. In order to get negative feedback stability, set phase lag when gain 1 (0 dB) equal to or less than 135 ° (greater than 45 ° phase margin).
Good frequency response can be realized by setting higher zero crossing frequency fc (frequency at 0 dB gain) of the total gain. However, speed and stability are in trade-off relationship. Moreover, DC / DC converter application is sampled by switching frequency and the gain of the switching frequency needs to be suppressed. In order to do so, zero crossing frequency needs to be set equal to or lower than 1 / 10 of the switching frequency.

To improve the responsiveness, switching frequency needs to be raised. It is recommended to draw a Bode plot using the transfer function of control loop in order to get a frequency response necessary. Please confirm the frequency characteristics of the total gain by combining the below three transfer functions.

$$G_{LC} = \frac{1 + \frac{s}{2\pi \times f_{ESR}}}{1 + \frac{s}{Q \times 2\pi \times f_{LC}} + \left(\frac{s}{2\pi \times f_{LC}}\right)^2} \quad \cdots \text{(a)}$$

$$G_{FB1} = \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{Z2}}\right)}{s \times R_{FB1B} \times C_{CO1A} \times \left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad \cdots \text{(b)}$$

$$G_{PWM} = \frac{V_{CC}}{\Delta V_{RAMP}} \quad \cdots \text{(c)}$$

*($G_{LC}$*: transfer function of LC resonance, *$G_{FB}$*: transfer function of phase compensation,
*$G_{PWM}$*: transfer function of PWM, *$\Delta V_{RAMP}$*: 0.4 V, *Q*: LC quality factor)

Since DC / DC1 of the BD39001EKV-C is voltage mode, it is possible to add 2-pole and 2-zero compensation as follows. The frequency of zero and pole is determined by the following equations:

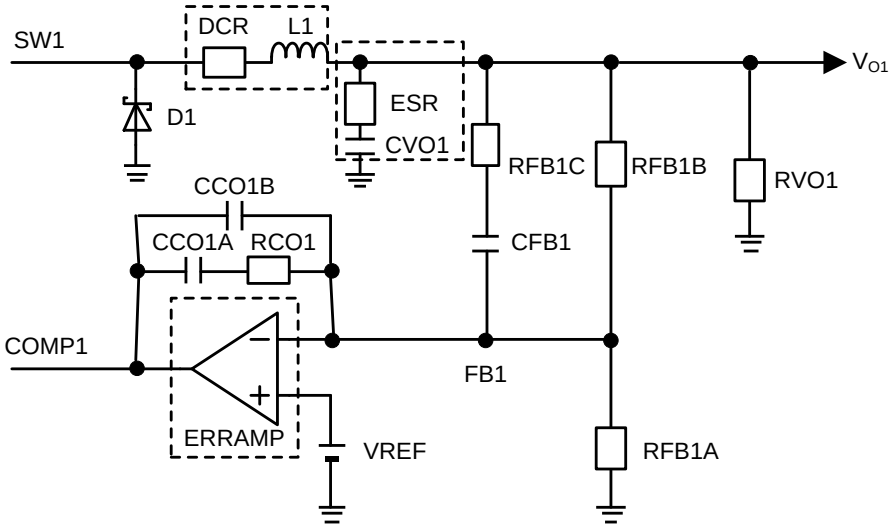



Figure 43. Phase compensation circuit (DC / DC1)

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{R_{VO1}+DCR+R_{ON}}{L1 \times C_{VO1}\,(R_{VO1}+ESR)}} \quad \cdots \text{(d)}$$

$$f_{ESR} = \frac{1}{2\pi \times \mathrm{ESR} \times C_{VO1}} \quad \cdots \text{(e)}$$

$$f_{Z1} = \frac{1}{2\pi \times R_{CO1} \times C_{CO1A}} \quad \cdots \text{(f)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{FB1B}+R_{FB1C}) \times C_{FB1}} \quad \cdots \text{(g)}$$

$$f_{P1} = \frac{C_{CO1A}+C_{CO1B}}{2\pi \times R_{CO1} \times C_{CO1A} \times C_{C01B}} \quad \cdots \text{(h)}$$

$$\mathrm{f}_{P2} = \frac{1}{2\pi \times R_{FB1C} \times C_{FB1}} \quad \cdots \text{(i)}$$

(*DCR*: Inductor DC resistance, $R_O$: Load resistance, $R_{ON}$: MOS FET ON resistance)

The frequency characteristics are optimized by placing pole and zero at most appropriate frequencies. The estimate is as follows.

$$0.2 \times f_{LC} \leq f_{Z1} \leq f_{LC} \quad \cdots \text{(j)}$$

$$0.5 \times f_{LC} \leq f_{Z2} \leq f_{LC} \times 2 \quad \cdots \text{(k)}$$

$$f_{P1} \approx f_C \times 5 = f_{SW} \times 0.5 \quad \cdots \text{(l)}$$

$$f_{P2} \approx f_{ESR} \quad \cdots \text{(m)}$$

(*fc*: Zero cross frequency、$f_{SW}$: DCDC1 switching frequency)

The phase compensation set as explained can cancel out the second order lag (-180 ˚) caused by LC resonance.
If $f_{ESR}$ is positioned higher than DC / DC switching frequency such as using low ESR ceramic for output cap, $f_{P2}$ is not necessary.
If LC filter Q (quality factor) is high, the gain has peak and phase rotates too fast resulting in not enough phase margin. In such case, set $f_{Z1}$ and $f_{Z2}$ as close to $f_{LC}$ as possible. Q (quality factor) is calculated by following equation:

$$\mathrm{Q} = \frac{\sqrt{L1 \times C_{VO1} \times R_{VO1}\,(R_{VO1}+ESR)}}{L1+C_{VO1} \times R_{VO1} \times ESR} \quad \cdots \text{(n)}$$

$$\approx R_{VO1} \times \sqrt{\frac{C_{VO1}}{L1}} \quad \cdots \text{(o)}$$

13. Phase compensation circuit (DC / DC2)

DC / DC2 is current mode control and is 2-pole and 1-zero system. It has two poles formed by error amp and output load and one zero added by phase compensation. The appropriate pole point and zero point placement results in good transient response and stability. Generic Bode plot of DC / DC converters is shown below. At point (a), gain starts falling due to the pole formed by output impedance of error amp and $C_{CO2}$ capacitance. After that, in order to cancel out the pole formed by output load, insert zero formed by $R_{CO2}$ and $C_{CO2}$ and offset the fluctuation of gain and phase before reaching out to point (b).

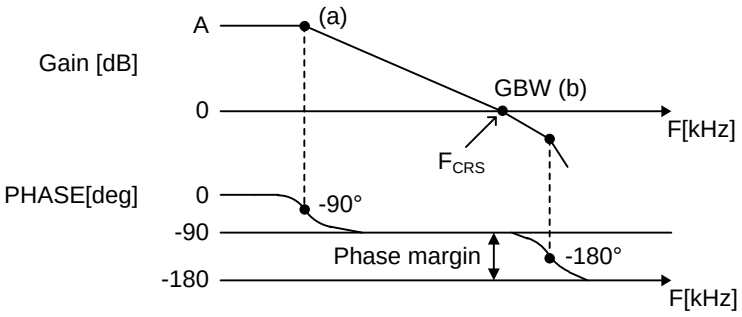



Figure 44. Phase compensation level

External component values are determined in this way. The $R_{CO2}$ determines the cross over frequency $F_{CRS}$, i.e., the frequency at which DC / DC total gain falls down to 0 dB. When $F_{CRS}$ is set high, good transient response is expected but stability is sacrificed on the other hand. When $F_{CRS}$ is set low, good stability is expected but transient response is sacrificed on the other hand.
In this example, component value is set in a way $F_{CRS}$ is 1 / 5 to 1 / 10 of the switching frequency.

(i) $R_{CO2}$ for Phase compensation
Phase compensation resistor $R_{CMP}$ can be obtained by the following equation.

$$R_{CO2} = \frac{2\pi \times V_{O2} \times F_{CRS} \times C_{VO2}}{0.8 \times G_{NP} \times G_{MA}} \quad (\Omega)$$

$V_{O2}$: Output voltage, $F_{CRS}$: Cross over frequency, $C_{VO2}$: Output capacitor, $V_{FB2}$: Feedback reference voltage (0.8 V (Typ)), $G_{MP}$: Current sense gain (16.7 A / V (Typ)), $G_{MA}$: Error amp trans-conductance (220 uA / V (Typ))

(ii) $C_{CO2}$ for Phase compensation

Phase compensation capacitor $C_{CO2}$ can be obtained by the following equation.

$$C_{CO2} = \frac{V_{O2} \times C_{VO2}}{I_{O2} \times R_{CO2}} \quad \text{(F)}$$

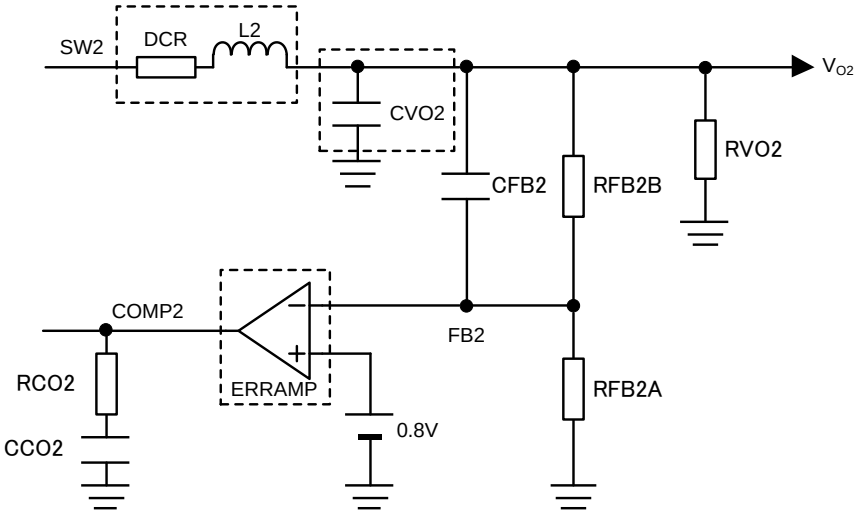



Figure 45. Phase compensation circuit (DC / DC2)

However these are simple equation and thus adjustment of the value using the actual product may be necessary for optimization. Also compensation characteristics are influenced by PCB layout and load conditions and thus thorough evaluation using the production intent unit is recommended.

14. Phase compensation circuit (DC / DC1, DC / DC2)

The way to start designing phase compensation circuit is as explained. Create a Bode plot and check if targeted frequency characteristics are met. The frequency characteristics pretty much fluctuate depending on PCB layout, type of components used and operating conditions. For instance, using electrolytic capacitor for output stability may cause the shift of LC resonance resulting in oscillation due to the capacitance drop at low temp and relevant ESR increase. For phase compensation, temperature compensating type capacitor is recommended. Make sure to check stability and responsiveness in actual product.

Frequency characteristics are checked by gain phase analyzer or FRA. Ask each vendor for measurement method. Even you such measurement equipment is unavailable, phase margin can be estimated from transient load response. Monitor how the output waveform fluctuates when changing from no load to maximum load. If the output fluctuation is significant, response time is slow. If the ringing is frequent, phase margin is not enough. Twice or less ringing is appropriate. The phase margin however cannot be quantified in this check method.

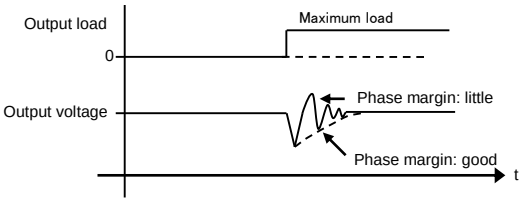
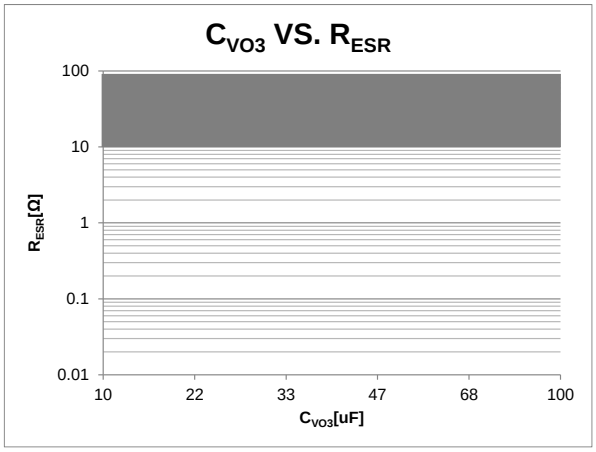



Figure 46. Load response

15. Phase compensation circuit (LDO3)

VO3 pin capacitor

The capacitor must be added between VO3 pin and GND in order to stop from having it Oscillated and the recommended Capacitance value is more than 10uF. In accordance to graph shown in below, either Electrolytic or Ceramic Capacitor can be used. Please ensure to select the Capacitor higher than 10uF in the range of voltage and temperature to be used at.
There is possibility of oscillation when capacitance value changes due to change of temperature. When selecting a ceramic capacitor, X7R or higher is recommended which is good in temperature characteristic and has excellent DC bias characteristic. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.




○Condition
$V_{CC}$ = 12 V
$V_{S3}$ = 6.5 V
0 mA ≤ $I_{O3}$ ≤ 600 mA
10 µF ≤ $C_{VO3}$ ≤ 100 µF

Figure 47. Output capacitor value $C_{VO3}$ vs Output capacitor $R_{ESR}$

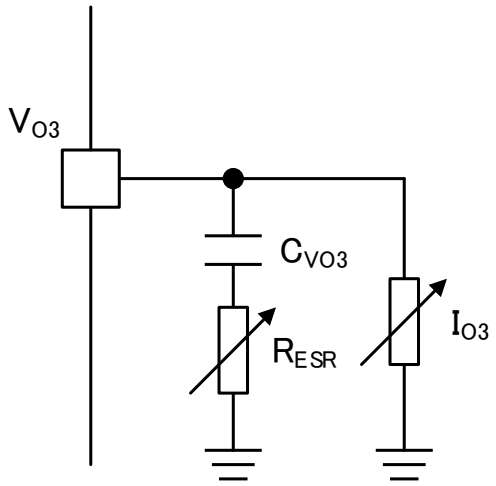



Figure 48. Output capacitor and ESR measurement circuit

16. Over Current Protection (OCP) Function (DCDC1)

Once coil current that flows through OCP sensing resistor $R_{CL}$ exceeds OCP detection level, OCP starts functioning. The setting method is shown below.

Selecting OCP sensing resistor - $R_{CL}$

In the state of OCP detection, the relation of coil current-$I_{L(OCP)}$, load current-$I_{O(OCP)}$ and current sensing resistor-$R_{CL}$ are shown in the following form. The VCC value that used to calculate $I_{L(OCP)}$ is the minimum or the maximum value of VCC, whichever can finally generate the maximum $I_{L(OCP)}$ value.

| BUCK MODE | BUCK-BOOST MODE | | BOOST MODE |
|---|---|---|---|
| $V_{CC} \geq 1.333 \times Vo$ | $1.333 \times Vo > V_{CC} \geq 0.625 \times Vo$ | | $V_{CC} < 0.625 \times Vo$ |
| $R_{CL} = \frac{0.1}{I_{L(OCP)}}$ | | | |
| $I_{L(OCP)} = I_{O(OCP)} + \frac{\Delta I_L}{2}$ | $I_{L(OCP)} = \frac{Vo \times I_{O(OCP)}}{VCC \times \eta} + \frac{\Delta I_L}{2}$ | | |
| $\Delta I_L = \frac{(VCC - Vo) \times Vo}{VCC \times fsw \times L}$ | $V_{CC} > Vo$<br>$\Delta I_L = \frac{(VCC - Vo) \times Dpon}{L \times fsw}$<br>$= \frac{(VCC - Vo) \times 2.13 \times Vo}{L \times fsw \times (VCC + 1.5 \times Vo)}$ | $V_{CC} < Vo$<br>$\Delta I_L = \frac{(Vo - VCC) \times Dnoff}{L \times fsw}$<br>$= \frac{(Vo - VCC) \times 2.13 \times VCC}{L \times fsw \times (VCC + 1.5 \times Vo)}$ | $\Delta I_L = \frac{(Vo - VCC) \times VCC}{Vo \times L \times fsw}$ |

$V_{CC}$: minimum or maximum voltage of VCC, $V_O$: output voltage, $f_{SW}$: switching frequency, L: inductance value
η: efficiency (It is necessary to measure on real board, as an reference:80%~90%)

In Figure 49 (BUCK-BOOST MODE) and Figure 50 (BUCK MODE), the reason of OCPH detection were considered Schottky diode break down and SW1 short to GND.

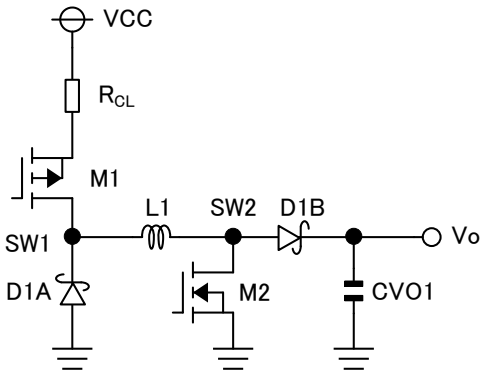



Figure 49. BUCK-BOOST Mode OCPH Detection

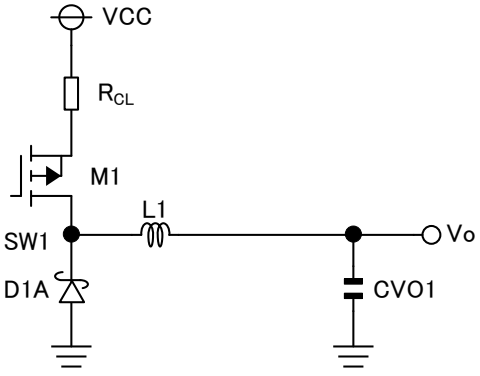



Figure 50. BUCK Mode OCPH Detection

① BUCK DCDC Application

When PchFET ON, once coil current × OCP sensing resistor $R_{CL}$ exceed VCCCL-CL voltage (100mV Typ), OCPL detection start working. In the condition of OCPL detect, on pulse width of PchFET be fixed, output voltage Vo decreases. If FB voltage lower than SCP detection level and continue 256clks, PchFET OFF, COMP and SS are discharged forcibly. After 8192clks, IC turn back to normal operation and SS be recharged again. (Figure 51) In addition, If VCCCL-CL voltage decrease to less than 100mV (Typ) within 256 clks, IC turns back to normal operation immediately. (Figure 52) Additionally, when VCCCL-CL voltage exceeds 200mV (Typ), OCPH detection start working, meanwhile PchFET OFF, COMP and SS are discharged forcibly. After 8192clks, IC turn back to normal operation and SS be recharged.

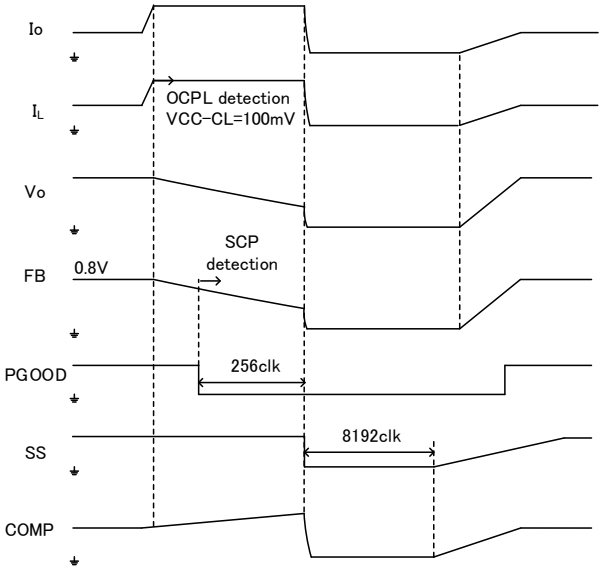



Figure 51. OCPL Detection・Release

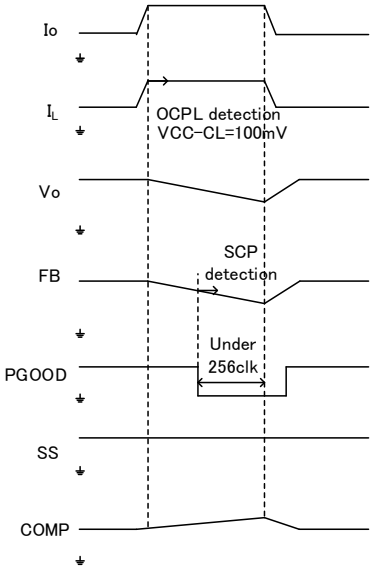



Figure 52. OCPL Detection

② BUCK-BOOST DCDC Application

In BUCK-BOOST DCDC Application, OCPL and OCPH function waves are as same as BUCK DCDC Application. (Refer to Figure 21) However, an exception rarely occurs - load current over OCPL detect current in a moment and turn to normal level within 256clks, but SS still be discharged. Please refer to the detail in the following section.

Once OCPL detected, Vo voltage decreases at first. Then Vo have the trend of increasing output voltage that been set as target output t in advance, so that DCDC come into BUCK-BOOST MODE and COMP voltage rise up. Finally, ON pulse width of NchFET is extended. Because coil current increases is depending on several essential factor (Input and output, frequency condition, load applying waveform, reply properties), the following 2 phenomenon related to OCPL is rarely occurs and could be automatically recover after Vo drop to 0V.

(1) VCCCL-CL voltage exceeds 200mV within OCPL 256clks' on pulse width limitation period.

(2) Even if load current decreases after OCPL detected, coil current keep increasing and an OCPL detection state won't stop until SS discharged.

The setting resistance of the OCP is from 1.2 times to 1.5 times of the rush current. Please check on application board.

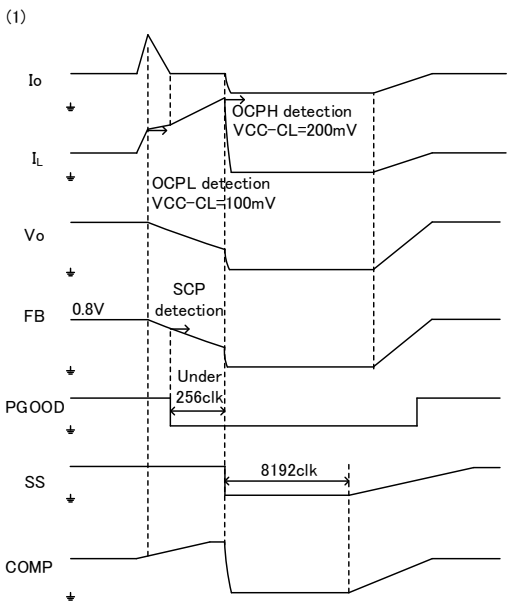



Figure 53. OCPH Detection・Release

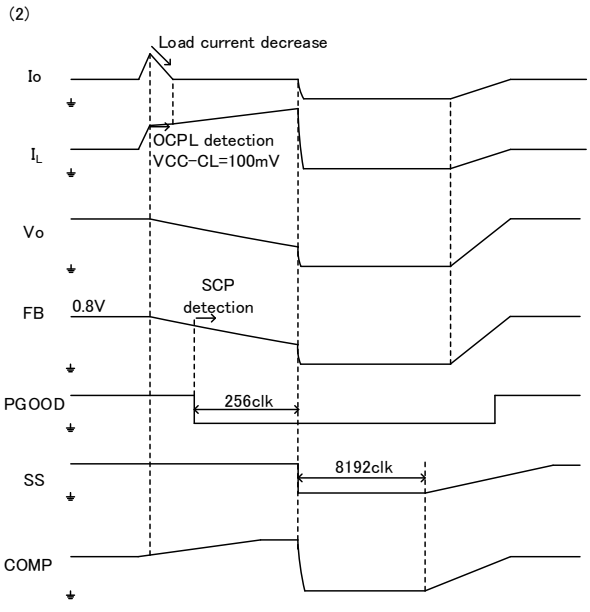



Figure 54. OCPL Detection・Release

17. Provision of Capacitor connected to CL terminal

The capacitor (CCL) and resistor (RCLB) connected to CL pin are the CR noise filter for preventing OCP error detection.

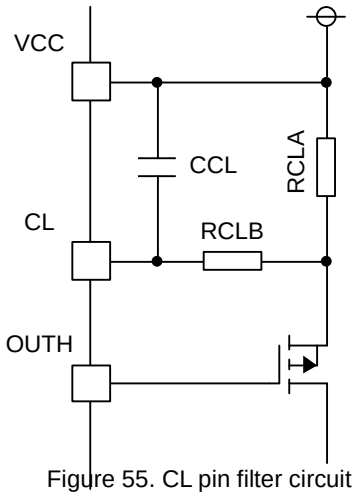



Figure 55. CL pin filter circuit

For the constant setting of filter, since noise depends on circuit and board pattern, there is no fixed rule. But, please try reducing cut-off frequency of CR filter without deteriorating ON pulse waveform that requires detecting current sense.
Pulse width≈ ($V_{O1}$ / $V_{CC}$) × (1 / $F_{OSC}$)
(The rough estimate setting is $R_{CLB}$ = 10kΩ, $C_{CL}$ = 0.1μF)

18. Soft Start setting

The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at start up.
Setting of soft start time is shown in the following equation.

・DC / DC1

$$T_{SS1} = \frac{V_{SS0} \times C_{SS1}}{I_{SS0}} + \frac{V_{REF08} \times C_{SS1}}{I_{SS1}} \geq 0.5ms$$

In addition, Please take SS1 discharge time ($T_{SS1DIS}$) into account, when start up this IC with VCC_UVLO function or EN pin. If SS1 is not finish discharge, it is possible that this IC can't do re-start.

$$T_{SS1dis} \geq C_{SS1} \times 2.2 \times 10^3$$

(For example: If $C_{ss1} = 33nF$, $T_{SS1dis} = 72.6\mu s$)

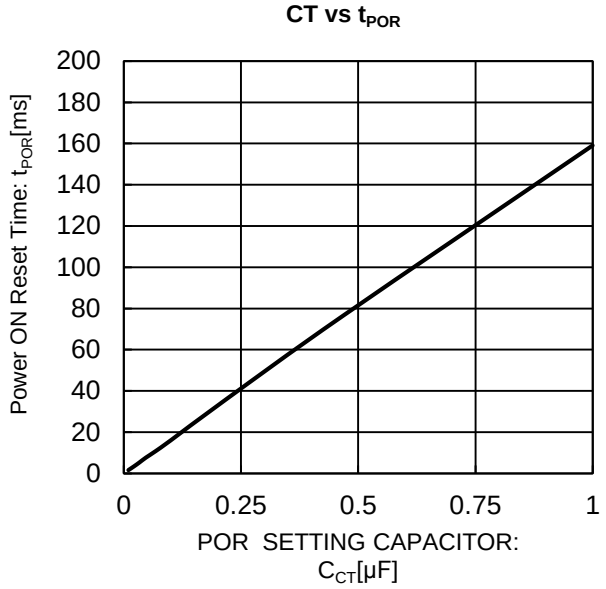
・DC / DC2

$$T_{SS2} = \frac{V_{SS2} \times C_{SS2}}{I_{SS2}} \geq 0.4ms$$

19. Setting the CT power on reset time

Power reset setting time can be set by the capacitor connected to CT
Capacitance can be chosen from 0.01 μF to 1 μF range or have CT terminal OPEN.
If setting is made out of its range, chattering may occur at Reset output.
CT operation is changed by the time of error detection. See page 15, Figure 26 for detail.

(1) CT pin starts 0 V



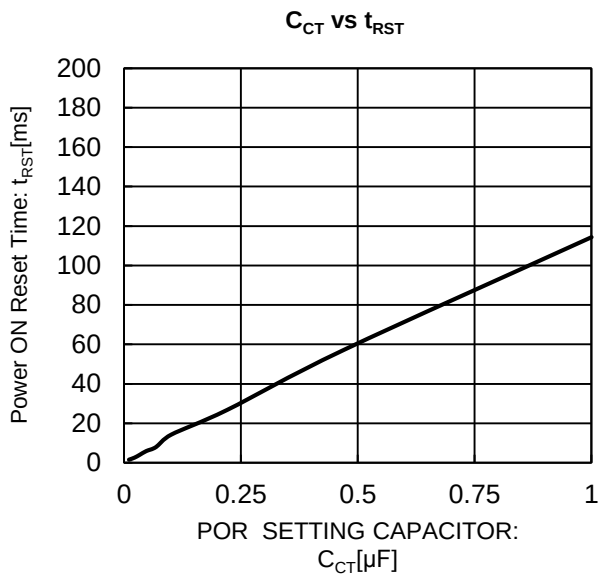

| $C_{CT}$ [μF] | $t_{POR}$ [ms] |
|---|---|
| 0.001 | 0.167 |
| 0.0082 | 1.09 |
| 0.01 | 1.62 |
| 0.022 | 3.46 |
| 0.033 | 5.24 |
| 0.047 | 7.64 |
| 0.068 | 10.8 |
| 0.1 | 16 |
| 0.22 | 36.2 |
| 0.47 | 76.8 |
| 1 | 159 |

Figure 56. Power ON Reset time1 ($V_{CT}$ = 0 V to 0.8 V(Typ))

$$t = CV/I$$

(C: CT pin capacitance value, V: Reset release voltage 0.8V, I: Charge current value 5μA)

(2) CT pin starts 0.2 V




| $C_{CT}$ [μF] | $t_{RST}$ [ms] |
|---|---|
| 0.001 | 0.16 |
| 0.0082 | 0.826 |
| 0.01 | 1.452 |
| 0.022 | 2.51 |
| 0.033 | 3.93 |
| 0.047 | 5.82 |
| 0.068 | 7.9 |
| 0.1 | 14.12 |
| 0.22 | 26.7 |
| 0.47 | 57.2 |
| 1 | 114.4 |

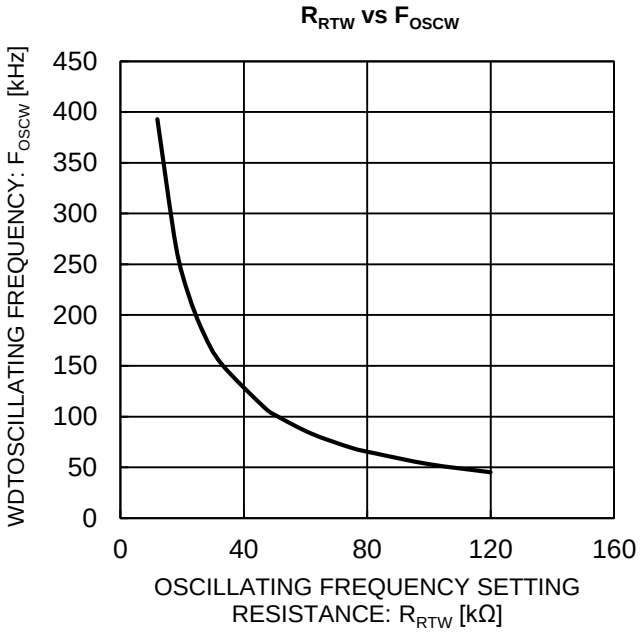
Figure 57. Power ON Reset time2 ($V_{CT}$ = 0.2 V (Typ) to 0.8 V(Typ))

$$t = C(V_1 - V_2)/I$$

(C: CT pin capacitance value, $V_1$: Reset release voltage 0.8V, $V_2$: CT pin voltage 0.2V, I: Charge current value 5μA)

20. Setting the WDT oscillation frequency

WDT oscillation frequency can be set by resistance value connected to RTW. Possible setting range is 50 kHz to 250 kHz and the relation between resistance value and oscillation frequency is decided as shown below.
It is possible that the WDT stops at outside these range and its operation is not guaranteed.

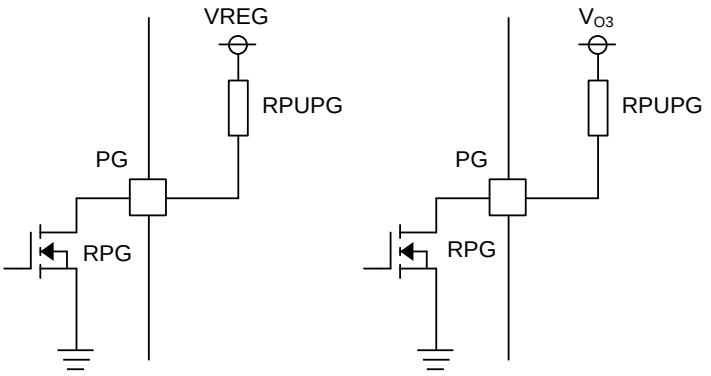



| $R_{RTW}$ [kΩ] | $F_{OSCW}$ [kHz] |
|---|---|
| 18 | 268 |
| 22 | 221 |
| 27 | 182 |
| 33 | 151 |
| 47 | 108 |
| 51 | 100 |
| 62 | 83 |
| 75 | 69 |
| 82 | 64 |
| 100 | 53 |
| 120 | 45 |

*This oscillation frequency graph is typical value
Tolerance needs to be put into consideration.

Figure 58. WDT oscillation frequency characteristics

21. Recommend value of external pull - up resistance




PG pin ON resistance (PPUPG)
Min = 0.5 kΩ, Typ = 1.0 kΩ, Max = 2.0 kΩ

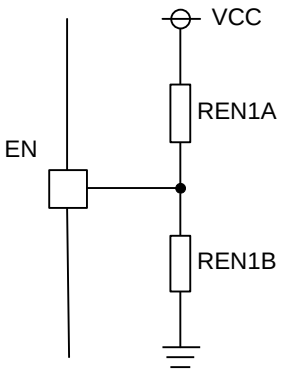
$$\frac{R_{PG}}{R_{PG}+R_{PUPG}} \times V_{O3} > V_{PG} \quad \text{(V)}$$

Please set the Resistance value considering H threshold of PG pin.

Figure 59

22. Provision of EN1 pull -up resistance

Because "H" threshold of EN1 is Min 2.5 V, please design as the below equation is able to work.




$$\frac{R_{EN1B}}{R_{EN1B}+R_{EN1A}} \times V_{CC} > 2.5 \quad \text{(V)}$$

(188 kΩ ≤ $R_{EN1B}$ ≤ 750 kΩ)

Figure 60

### Application Examples

*There are many factors (Board layout, variation of the part, etc.) that can affect the characteristics.
Please verify and confirm using practical applications.
*No connection (N.C) pin should not be connected to any other lines.
*Be sure to connect the TEST pin to ground.
* If EN1 pin is connected to VCC pin, please insert resistance between the pins.

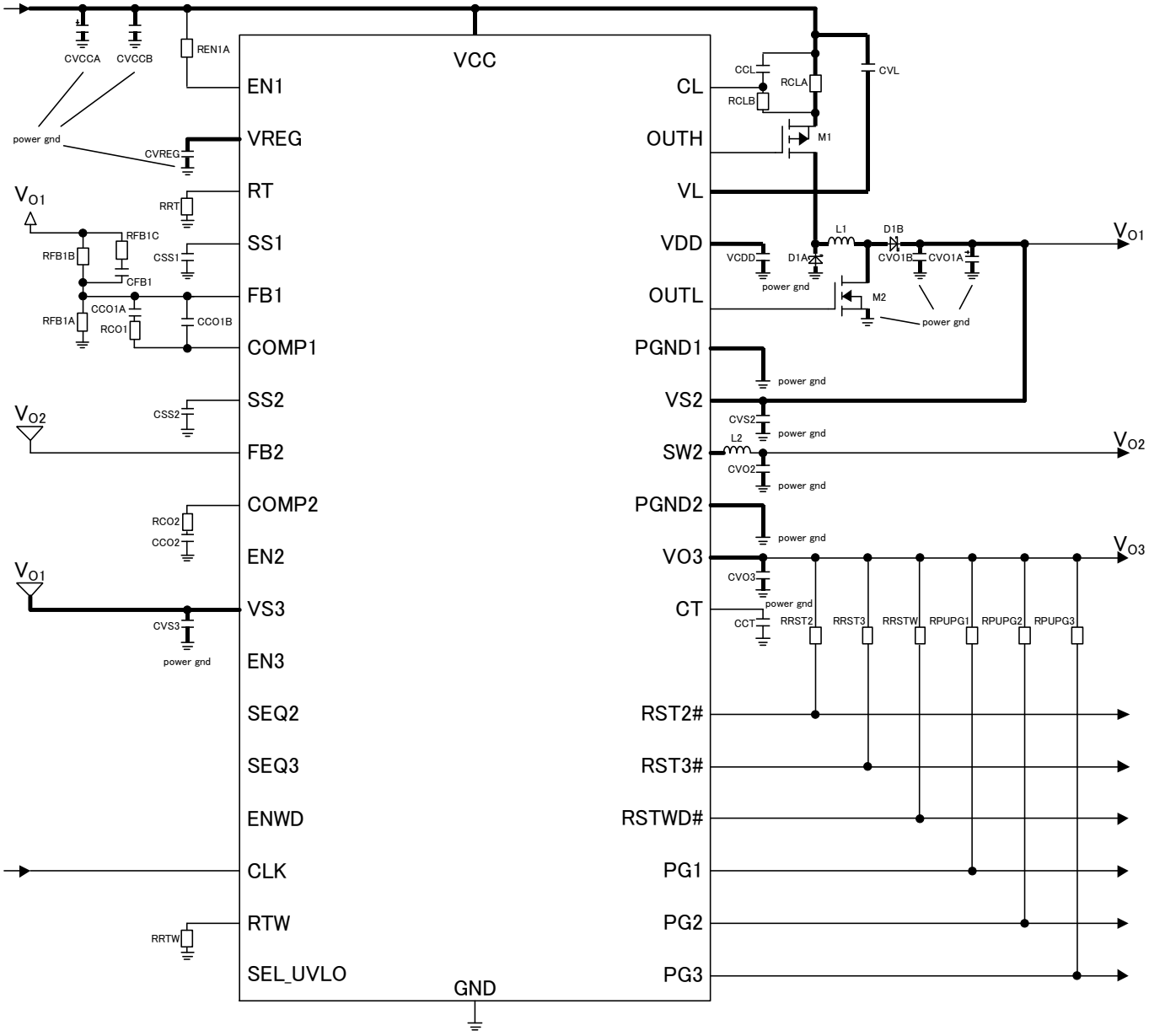



Figure 61. Application Example 2 (DC / DC1 Buck - Boost)

### Application Examples

*There are many factors (Board layout, variation of the part, etc.) that can affect the characteristics.
Please verify and confirm using practical applications.
*No connection (N.C) pin should not be connected to any other lines.
*Be sure to connect the TEST pin to ground.
* If EN1 pin is connected to VCC pin, please insert resistance between the pins.

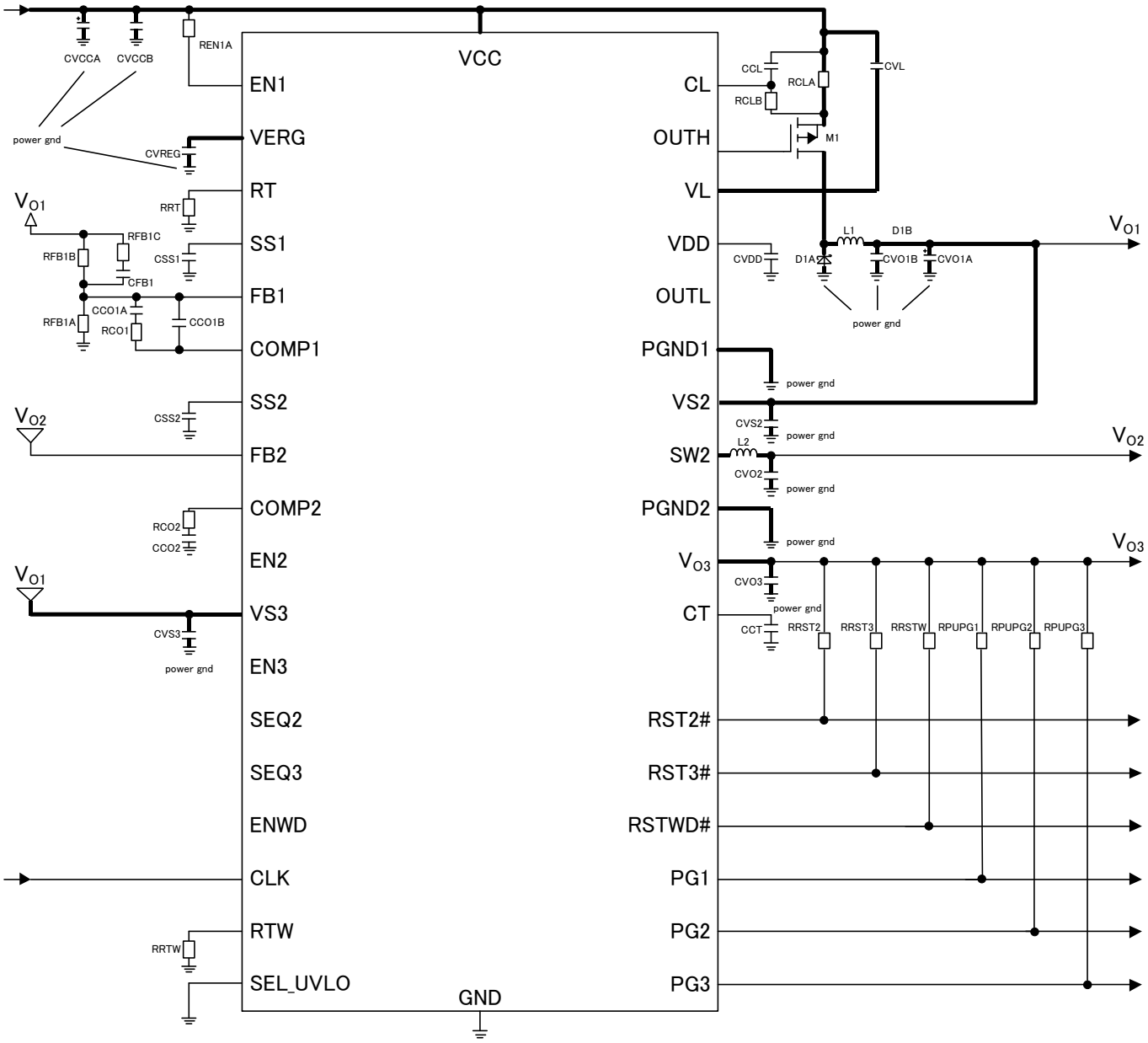



Figure 62. Application Example 3 (DC / DC1 Buck)

**Example of Constant Setting (DC / DC1 Buck Mode)**

| Name | Value | | Parts No. | Size Code | Maker | Note |
|---|---|---|---|---|---|---|
| IC | - | - | BD39001EKV-C | 10 × 10 mm | ROHM | |
| REN1A | 150 | kΩ | MCR03 | 1608 | ROHM | |
| RRT | 33 | kΩ | MCR03 | 1608 | ROHM | |
| RFB1A | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RFB1B | 68 | kΩ | MCR03 | 1608 | ROHM | |
| RFB1C | 1.6 | kΩ | MCR03 | 1608 | ROHM | At Buck-Boost: 0.1 kΩ |
| RCO1 | 36 | kΩ | MCR03 | 1608 | ROHM | At Buck-Boost: 4.7 kΩ |
| RCO2 | 20 | kΩ | MCR03 | 1608 | ROHM | |
| RRTW | 51 | kΩ | MCR03 | 1608 | ROHM | |
| RCLA | 110 | mΩ | MCR10 | 2012 | ROHM | |
| RCLB | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RRST2 | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RRST3 | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RRSTW | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RPUPG1 | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RPUPG2 | 10 | kΩ | MCR03 | 1608 | ROHM | |
| RPUPG3 | 10 | kΩ | MCR03 | 1608 | ROHM | |
| CVCCA | 47 | µF | Electrolytic capacitor | - | - | |
| CVCCB | 2.2 | µF | GCM | 1608 | murata | |
| CVREG | 1 | µF | GCM | 1608 | murata | |
| CVDD | 0.1 | µF | GCM | 1608 | murata | At Buck-Boost: 1 µF |
| CSS1 | 0.033 | µF | GCM | 1608 | murata | |
| CFB1 | 820 | pF | GCM | 1608 | murata | At Buck-Boost: 2200 pF |
| CSS2 | 0.047 | µF | GCM | 1608 | murata | |
| CCO1A | 2200 | pF | GCM | 1608 | murata | At Buck-Boost: 47000 pF |
| CCO1B | 33 | pF | GCM | 1608 | murata | At Buck-Boost: 100 pF |
| CCO2 | 2200 | pF | GCM | 1608 | murata | |
| CVS3 | 1 | µF | GCM | 1608 | murata | |
| CCL | 0.1 | µF | GCM | 1608 | murata | |
| CVL | 0.1 | µF | GCM | 1608 | murata | |
| CVO1A | 100 | µF | Hybrid capacitor | - | - | At Buck-Boost: 47 µF |
| CVO1B | OPEN | | - | - | - | At Buck-Boost: 44 µF |
| CVS2 | 4.7 | µF | GCM | 2012 | murata | |
| CVO2 | 100 | µF | Hybrid capacitor | - | - | |
| CVO3 | 10 | µF | GCM | 3216 | murata | |
| CCT | 0.1 | µF | GCM | 1608 | murata | |
| L1 | 47 | µH | CLF12577NIT-470M-D | 12.5 × 12.8 mm | TDK | |
| L2 | 10 | µH | CLF6045NIT-100M-D | 6 × 6.3 mm | TDK | |
| D1A | SBD | | RB050L-40DD | 2.6 × 5.0 mm | ROHM | |
| D1B | SBD | | RB050L-40DD | 2.6 × 5.0 mm | ROHM | Only Buck-Boost |
| M1 | pchFET | | RSD046P05FRA | 6.5 × 9.5 mm | ROHM | |
| M2 | nchFET | | RSD080N06FRA | 6.5 × 9.5 mm | ROHM | Only Buck-Boost |

**Notes for pattern layout of PCB**

1) Design the wirings shown in bold line as short as possible.
2) Place the input ceramic capacitor CVCCB as close to M1 as possible.
3) Place the RRT and RRTW as close to GND pin as possible.
4) Place the RFB1A and RFB1B as close to FB1 pin as possible and provide the shortest wiring from FB1 pin.
5) Place the RFB1A, RFB1B and FB2 as far away from L1 and L2 as possible.
6) Separate power GND and signal GND so that SW noise doesn't affect the signal GND.

Sequence function

DC / DC2 and LDO output sequence can be set with EN2, EN3, SEQ2 and SEQ3 pin.

Ex. 1) EN2, EN3, SEQ2 and SEQ3 pins are open

DC / DC1→LDO and DC / DC2 start at once.

LVD2 Release Voltage = Under voltage detection voltage (VRST2) + Under voltage hysteresis voltage (VRSTH2).

LVD3 Release Voltage = Under voltage detection voltage (VRST3) + Under voltage hysteresis voltage (VRSTH3).

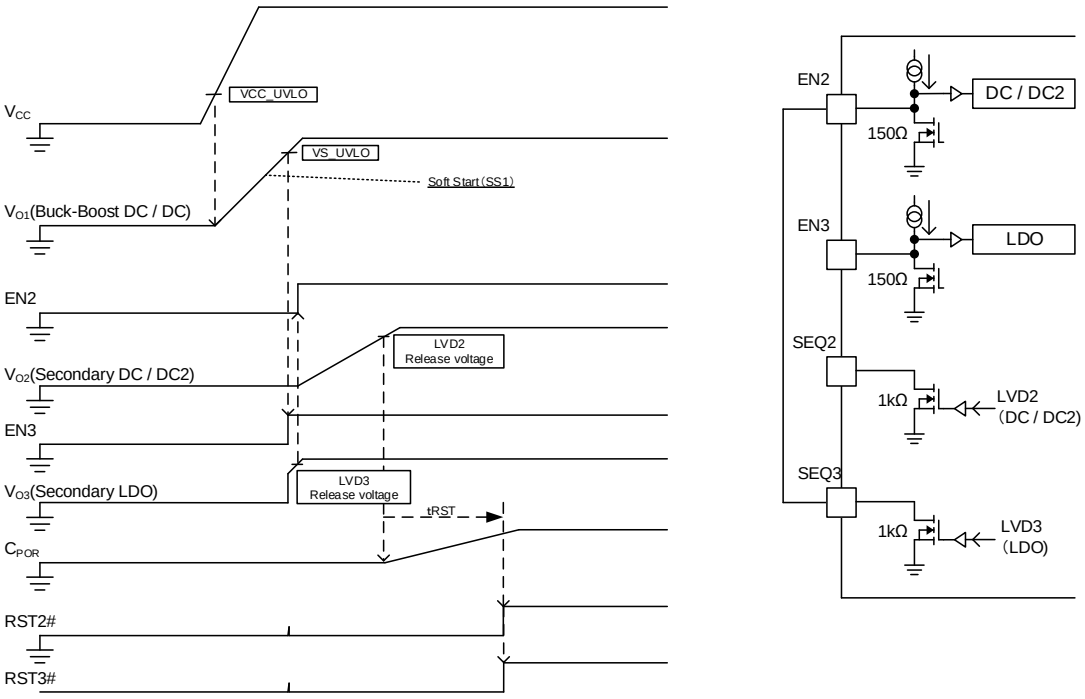



Figure 63. Start sequence example 1

Ex. 2) Condenser connects to EN pin

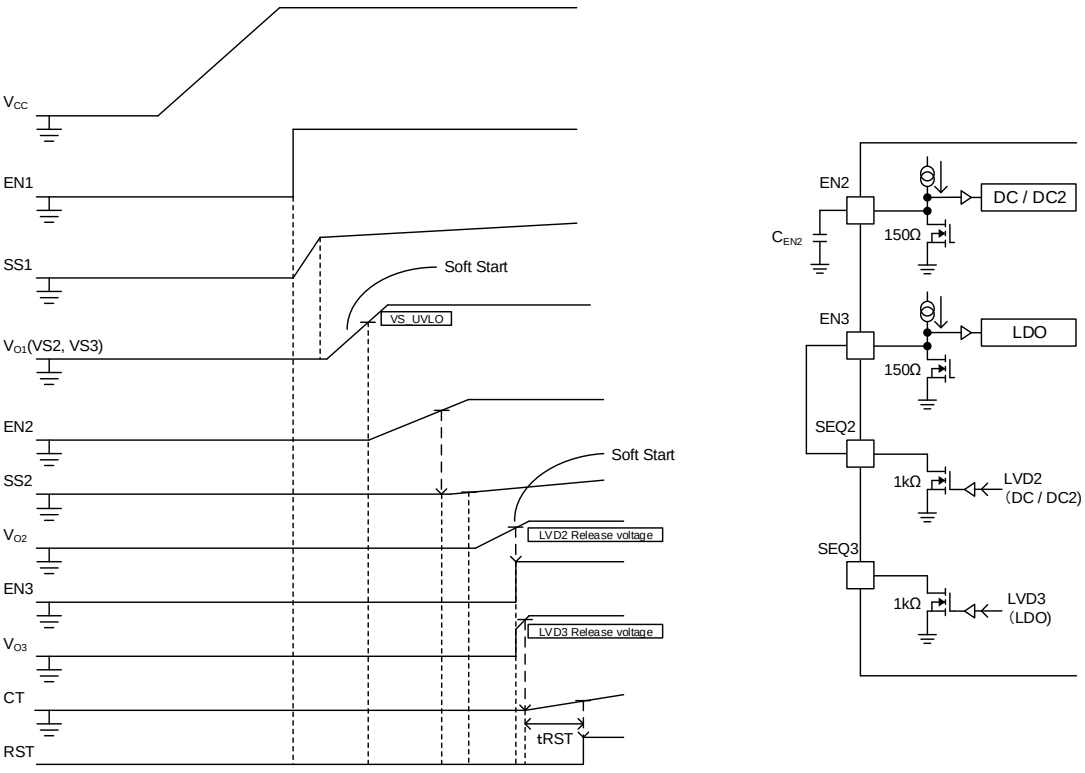



Figure 64. Start sequence example 2

**Power Dissipation**

Maximum Junction Temperature Tj is 150 °C. If the junction temperature reaches 175 °C or higher, the circuit will be shut down. Please make sure that the junction temperature must not exceed 150C at all time.

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. Ambient temperature Ta is less than 125 °C.
2. Tj is less than 150 °C.

Temperature Tj can be calculated by two ways as below.

1. To obtain Tj from the IC surface temperature Tc in actual use

$$Tj = TC + \theta jc \times P_{TOTAL}$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta ja \times P_{TOTAL}$$

The heat loss of the IC ($P_{TOTAL}$) is calculated by the equation below.

$$P_{TOTAL} = P_1 + P_2 + P_3$$

・DC / DC1

$$P_1 = V_{CC} \times I_{CC}$$

・DC / DC2

$$P_2 = \left\{R_{onH2} \times {I_{O2}}^2 \times \left(\frac{V_{O2}}{V_{S2}}\right)\right\} + \left\{R_{onL2} \times {I_{O2}}^2 \times \frac{V_{S2} - V_{O2}}{V_{S2} - Toff2)}\right\}$$

$$+ \{Vf \times I_{O2} \times (Toff2 \times f)\} + \left(Tr2 \times V_{S2} \times I_{O2} \times \frac{f}{2}\right)$$

$$+ (Tf2 \times VS2 \times I_{O2} \times f/2)$$

・LDO

$$P_3 = (V_{S3} - V_{O3}) \times I_{O3} + V_{S3} \times I_{CC3}$$

・DC / DC2

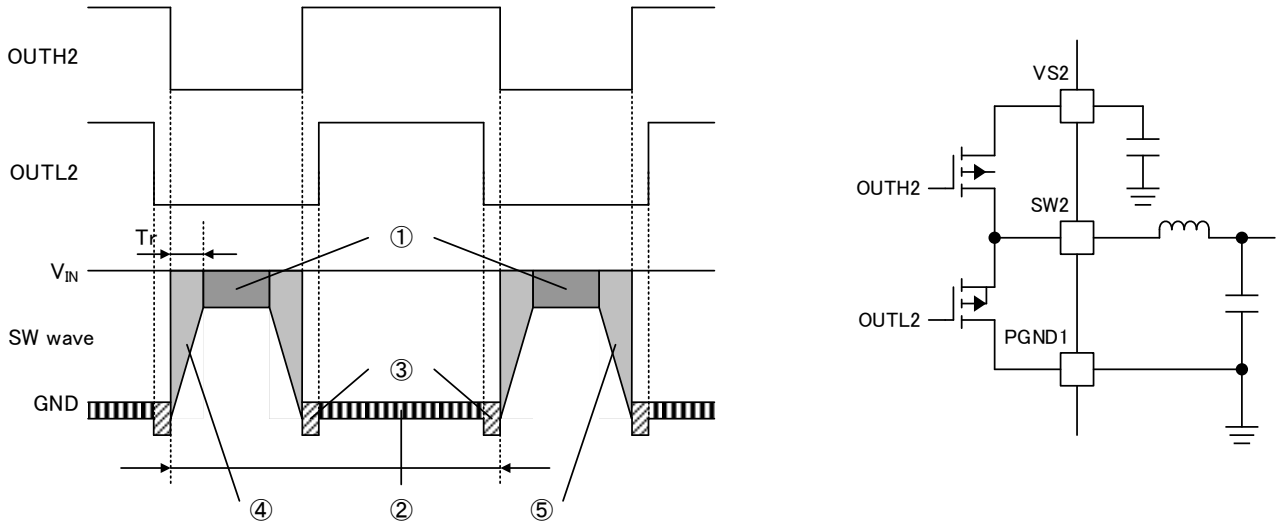



Figure 65. SW2 wave and circuit

①The loss of ON Duty $R_{onH2} \times I_{O2} \times I_{O2} \times \frac{V_{O2}}{V_{S2}}$

②The loss of OFF Duty $R_{onL2} \times I_{O2} \times I_{O2} \times \frac{V_{S2} - V_{O2}}{V_{S2} - \mathrm{Toff2} \times \mathrm{f}}$

③The loss of OFF / OFF $\mathrm{Vf} \times I_{O2} \times (\mathrm{Toff2} \times \mathrm{f})$

④The loss of $Tr_2$ $\mathrm{Tr2} \times V_{S2} \times I_{O2} \times \frac{f}{2}$

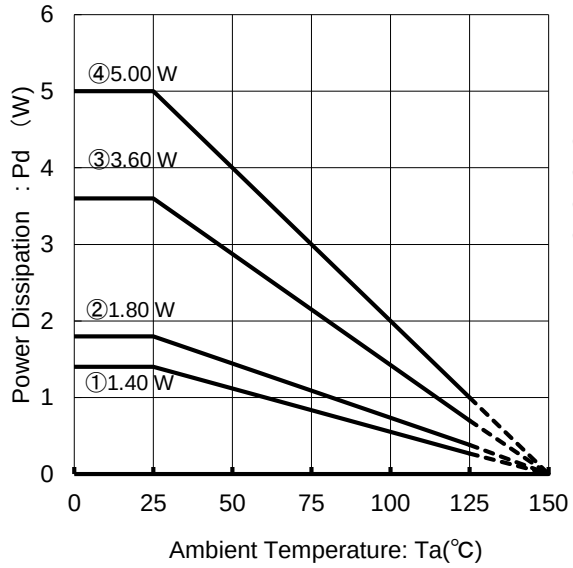
⑤The loss of $Tf_2$ $\mathrm{Tf2} \times V_{S2} \times I_{O2} \times \frac{f}{2}$

$R_{ONH2}$: ON resistor of internal Pch-PowTr
$R_{ONL2}$: ON resistor of internal Nch-PowTr
$V_{O1}$: DC / DC1 output voltage
$V_{O2}$: DC / DC2 output voltage
$V_{O3}$: LDO output voltage
$V_{CC}$: Input voltage (VS2 = $V_{O1}$, VS3 = $V_{O1}$)
$Io_2$: DC / DC2 output current
$Io_3$: LDO output current
$I_{VCC}$: circuit current (see page 5)
$I_{CC3}$: VS3 circuit current (About 1mA)
Vf: Internal Nch-PowTr's body diode (About 1.3 V)
$Tr_2$: Switching rise time (About15 ns)
$Tf_2$: Switching fall time (About15 ns)
Toff2: DC / DC2 dead time (About 65 ns)
f: Oscillation frequency

See the thermal derating characteristics (Figure 66) if the device used over the ambient temperature Ta = 25 °C.
The characteristics of IC largely depend on temperature, and IC must be used at maximum junction temperature (Tjmax) or lower. Even if the ambient temperature is 25 °C, there is a possibility junction temperature gets high as consequence of input voltage and load current. IC must be used within power dissipation Pd.

Thermal resistance value θja is varied by the number of the layer and copper foil area of the PCB.
See Figure 66 for the thermal design.

### Thermal Derating Characteristics



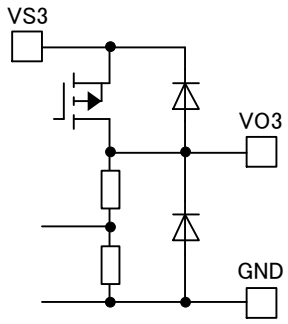
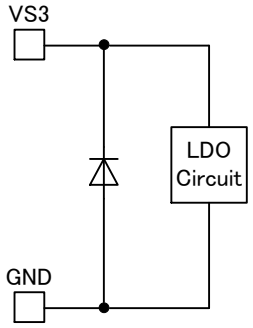
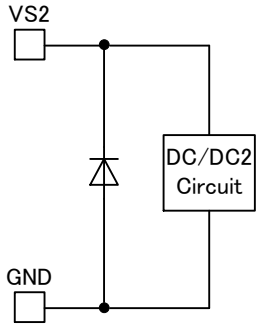
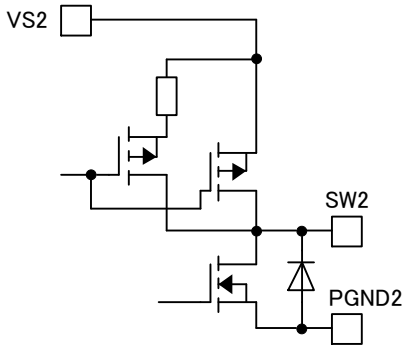
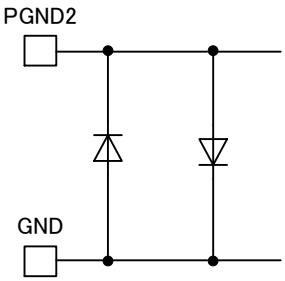
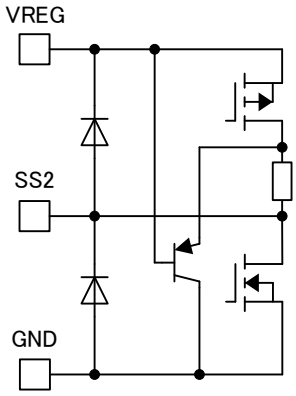
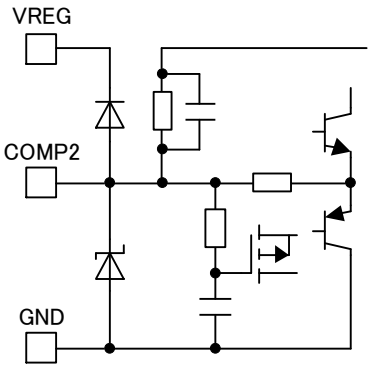
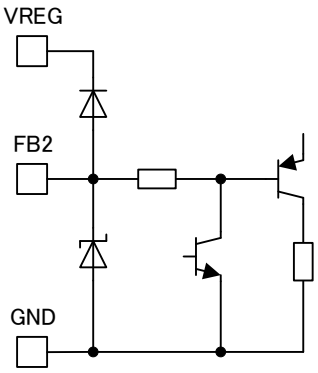
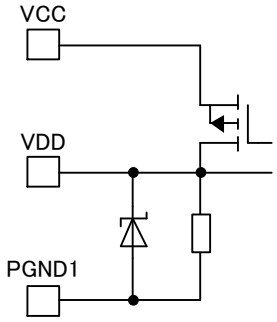
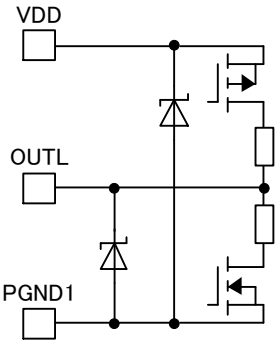
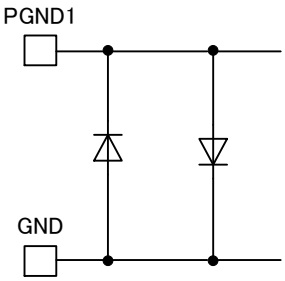
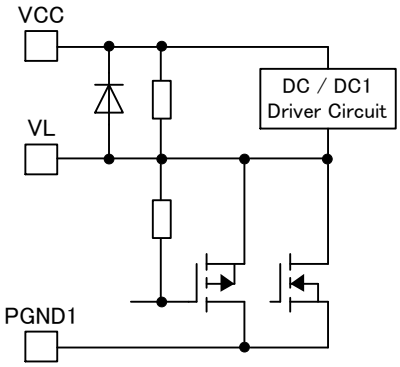

IC mounted on ROHM standard board
・Board size: 70 mm × 70 mm × 1.6 mm
・PCB and back metal are connected by soldering

①1 layer board 70 × 70 × 1.6 mm (copper foil area 0 mm × 0 mm)
②2 layer board 70 × 70 × 1.6 mm (copper foil 15 mm × 15 mm)
③2 layer board 70 × 70 × 1.6 mm (copper foil 70 mm × 70 mm)
④4 layer board 70 × 70 × 1.6 mm (copper foil 70 mm × 70 mm)

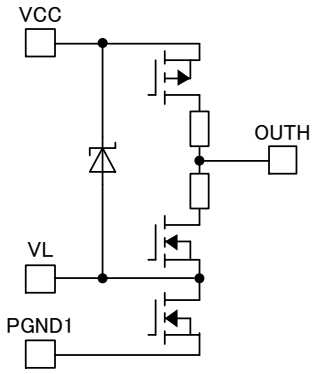
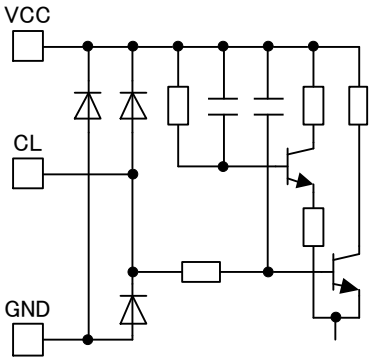
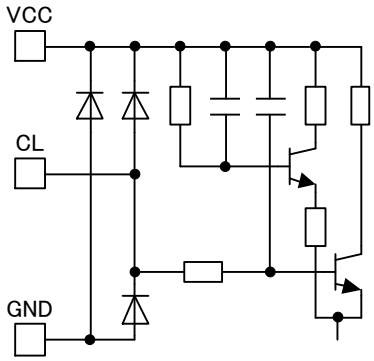
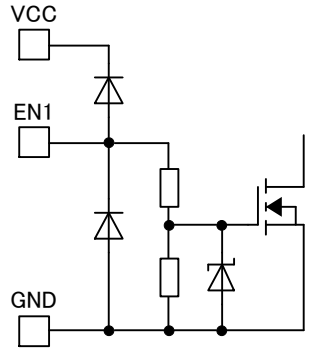
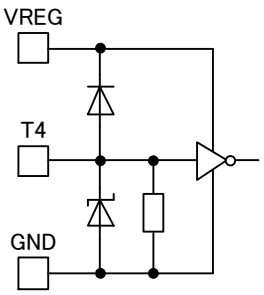
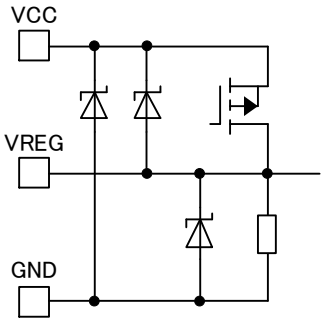
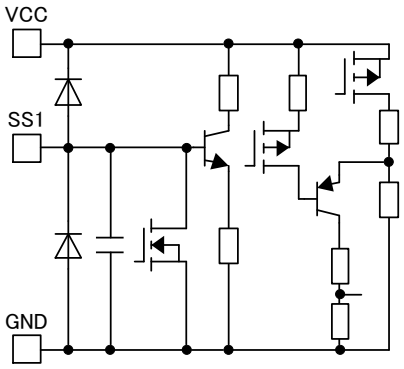
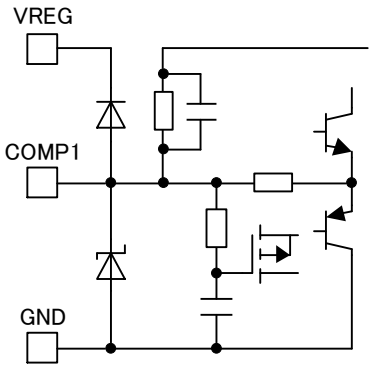
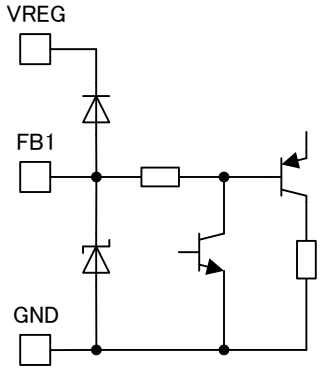
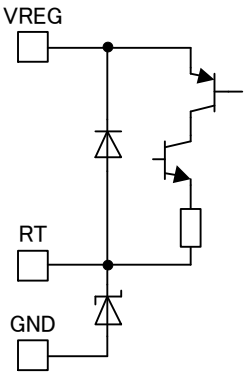
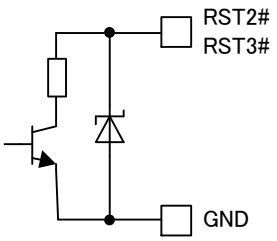
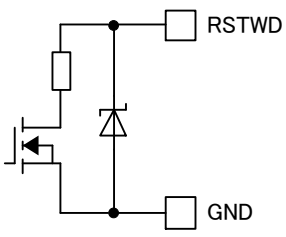
Board①: θja = 89.3 °C / W
Board②: θja = 69.4 °C / W
Board③: θja = 34.7 °C / W
Board④: θja = 25.0 °C / W

Figure 66. Package data of HTQFP48V (Reference data)

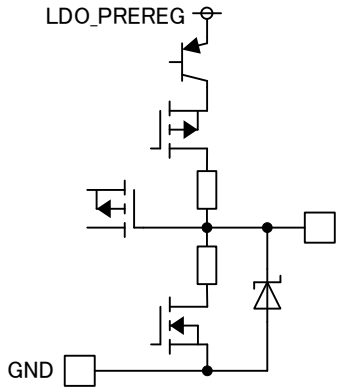
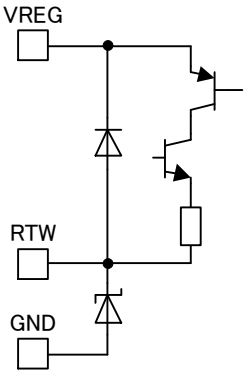
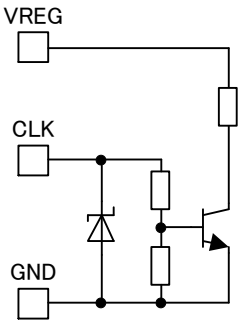
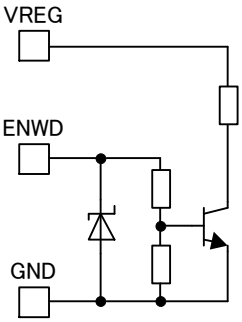
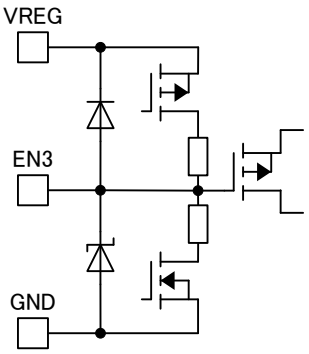
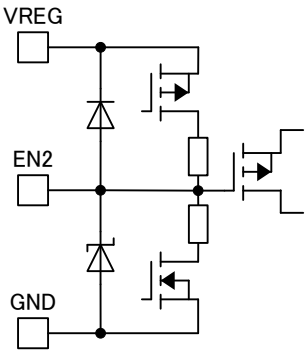
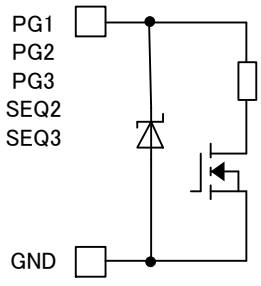
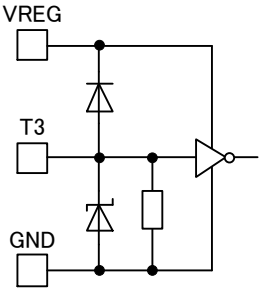
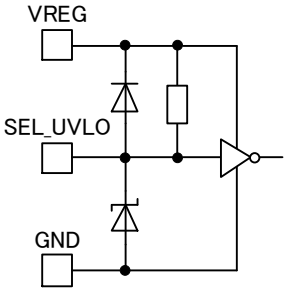
**I / O Equivalence Circuit**

| 1. VO3 | 3. VS3 | 4, 5. VS2 |
|---|---|---|
|  |  |  |
| 7, 8. SW2 | 10, 11. PGND2 | 12. SS2 |
|  |  |  |
| 13. COMP2 | 14. FB2 | 15. VDD |
|  |  |  |
| 16. OUTL | 17. PGND1 | 19. VL |
|  |  |  |

**I / O Equivalence Circuit**

| 21. OUTH | 23. CL | 24. VCC |
|---|---|---|
|  |  |  |
| 25. EN1 | 26. T4 | 27. VREG |
|  |  |  |
| 28. SS1 | 29. COMP1 | 30. FB1 |
|  |  |  |
| 31. RT | 33, 34<br>RST2#, RST3# | 35. RSTWD# |
|  |  |  |

**I / O Equivalence Circuit**

| 36. CT | 37. RTW | 38. CLK |
|---|---|---|
|  |  |  |
| 39. ENWD | 40. EN3 | 41. EN2 |
|  |  |  |
| 42, 43, 44, 45, 46<br>SEQ3, SEQ2, PG3, PG2, PG1 | 47. T3 | 48. SEL_UVLO |
|  |  |  |

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Please make sure to have protection against reverse polarity, such as putting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Power supply line must be low impedance on the PCB. The power supply of digital and analog must be separated (even if the electrical potentials are the same) to prevent analog circuit from having digital noise by common impedance of line pattern (ground line must be designed in the same way)
   Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that ground pin must have the lowest electrical potential at all time even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately, but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground voltage caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd is specified at the condition of 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size or copper area to prevent the IC from exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the specified characteristics can be approximately obtained. The electrical characteristics are guaranteed under the specified conditions.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To protect IC from static discharge damage, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Make sure that there is nothing between the pins, such as no metal particles, no water droplets (in very humid environment) and unintentional solder bridge deposited.

**10. Unused Input Pins**

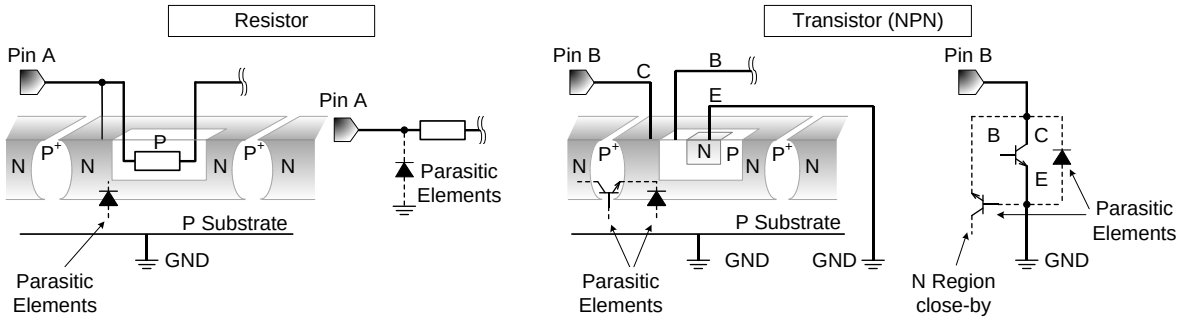
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If input pins left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**11. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.




In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**12. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant with the consideration of the capacitance charge with temperature and the decrease in nominal capacitance due to DC bias and others.

**13. Thermal Shutdown Circuit (TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period of time, the junction temperature (Tj) rises, and TSD activated, which turns off all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Under no circumstances, TSD circuit should not be used for any purpose other than protecting the IC from exceeding the maximum rating.

**14. Over Current Protection Circuit (OCP)**

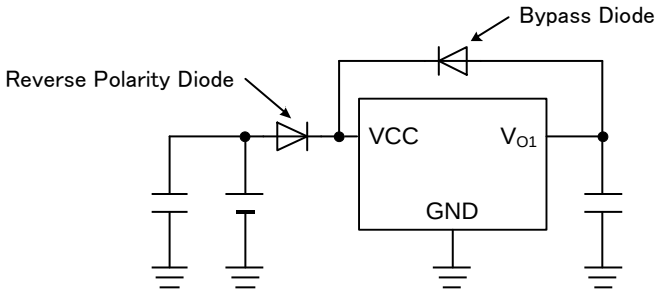
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is designed to avoid IC damaged from sudden and unexpected incidents, so should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

**15. Power input at shutdown**

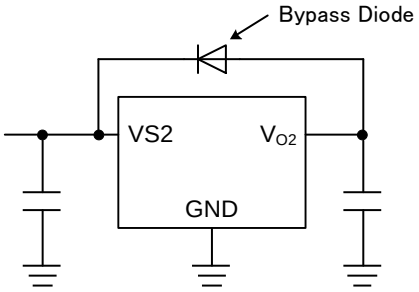
If VCC starts up in rapid period of time at shutdown (EN1 = OFF), VREG voltage may be output, which causes the IC to malfunction. Therefore, set the VCC rise time at 40V/ms or shorter.

### 16. Reverse Polarity and Surge voltage

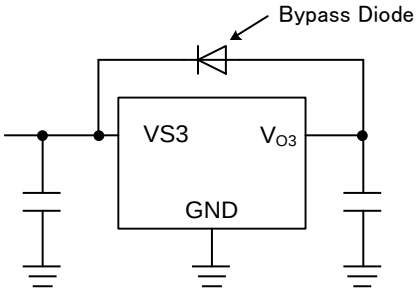
- If the VCC and pin potential are reversed, internal circuit or element may be damaged (example: VCC is shorted to GND while external capacitor changed) Putting diode for reverse protection in series of VCC or putting bypass diode between VCC is recommended.



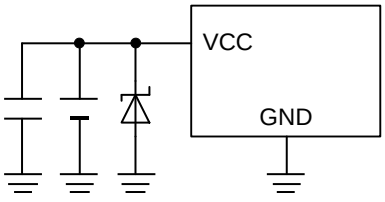

- If the VS2 and pin potential are reversed, internal circuit or element may be damaged (example: VCC is shorted to GND while external capacitor changed) Putting diode for reverse protection in series of VCC or putting bypass diode between VCC is recommended.



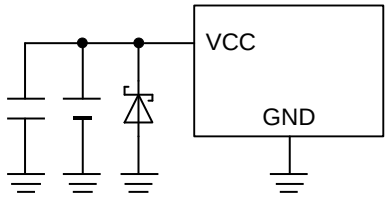

- If the VS3 and pin potential are reversed, internal circuit or element may be damaged (example: VCC is shorted to GND while external capacitor changed) Putting diode for reverse protection in series of VCC or putting bypass diode between VCC is recommended



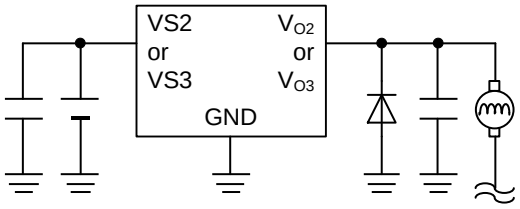

- Applying positive surge to the VCC
  If there is apossibility a surge exceeding the rating be applied to VCC, please put a power zener diode between VCC and GND.



- Applying negative surge to the VCC
  If there is a possibility VCC gets lower than GND, please put a schottky diode between VCC and GND.

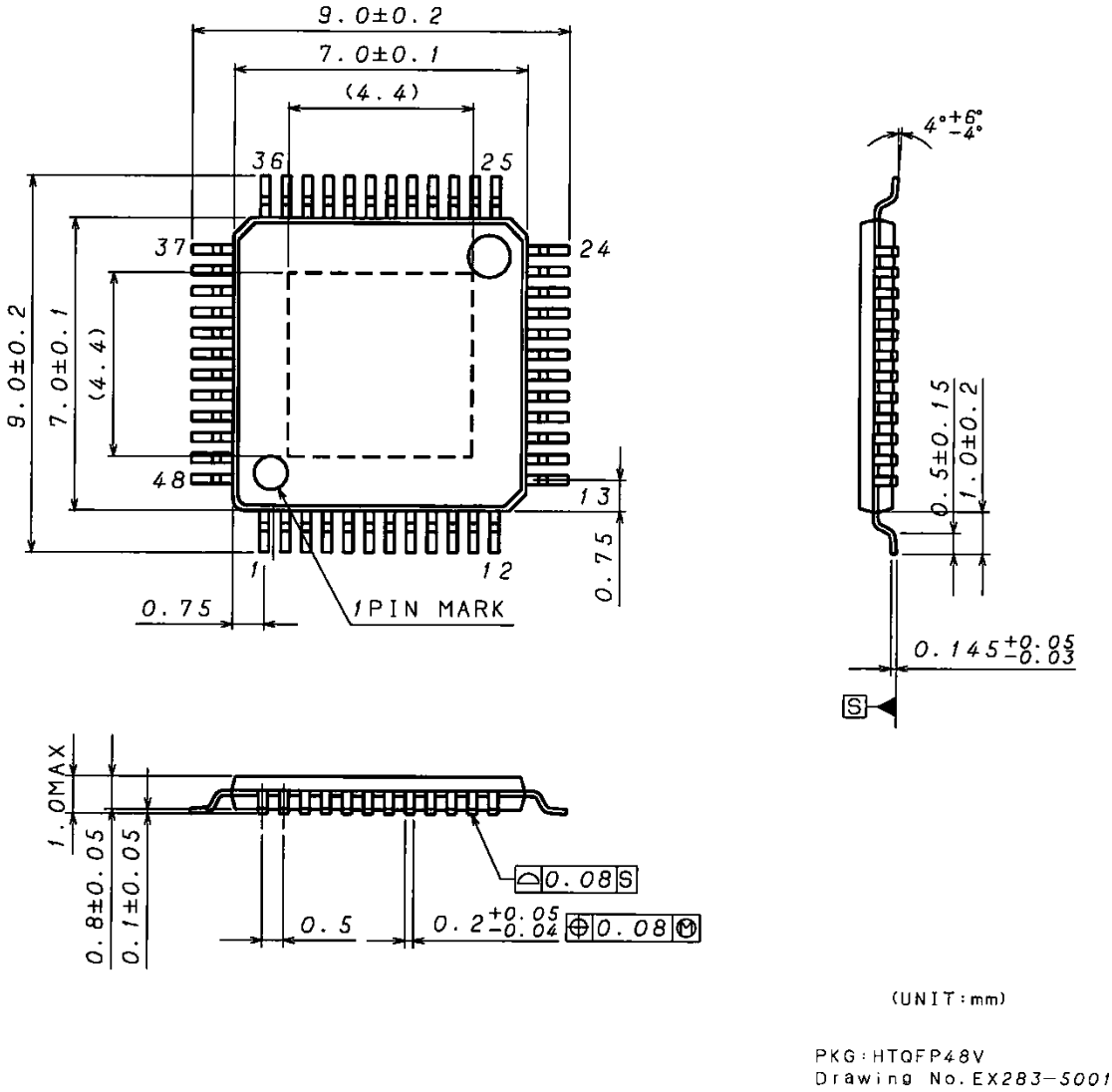



- Protection Diode
  If there is a possibility large inductive load is connected to the output pin (VO2 or VO3) resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.



**Physical Dimension, Tape and Reel Information**

| Package Name | HTQFP48V |
|---|---|

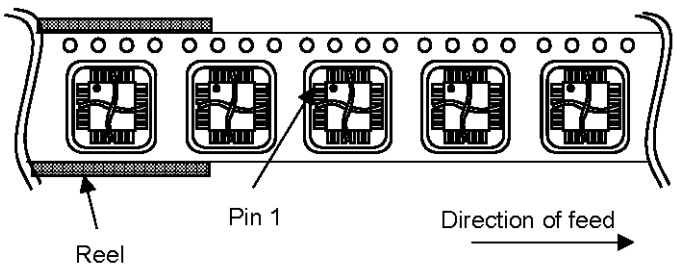



(UNIT:mm)

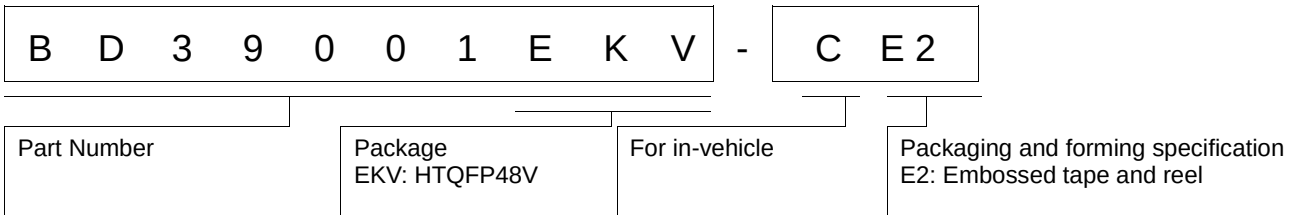
PKG:HTQFP48V
Drawing No.EX283-5001

< Tape and Reel Information >

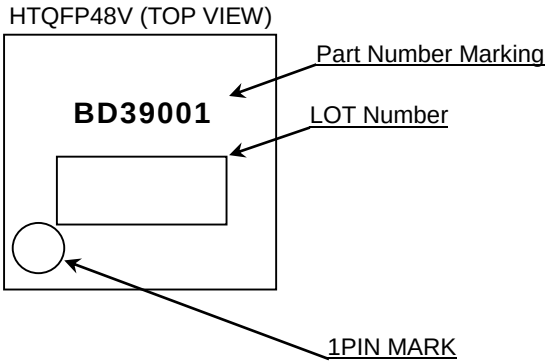
| | |
|---|---|
| Tape | Embossed carrier tape with dry pack |
| Quantity | 1500pcs |
| Direction of feed | E2<br>The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |



### Ordering Information




### Marking Diagram



**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 2014.02.12 | 001 | New Release |
| 2017.03.23 | 002 | P.6: at Electrical Characteristic, add four item.<br>(CLK Input Current, ENWD Input Current,<br>RST Leak Current and RSTWD Leak Current )<br>P.32 to 33: add “16. Over Current Protection Function“.<br>P.34: at 18. Soft Start Setting, add the discharge time of SS1.<br>The other: It revises errors. |

# Notice

## Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

## Precaution Regarding Intellectual Property Rights

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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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