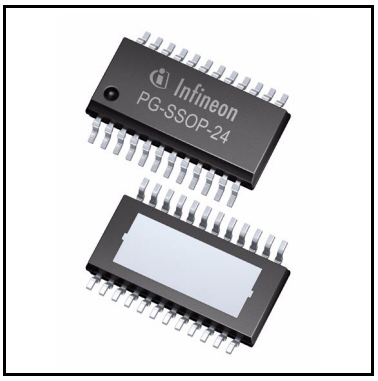
# TLE8080EM

## Engine Management IC for Small Engines




## 1 Overview

### Features

- Supply 5V (+/-2%), 250 mA
- K-line transceiver (ISO 9141)
- Serial Peripheral Interface (SPI)
- 4 low side driver for inductive loads with overtemperature and overcurrent protection and open load/short to GND in off diagnosis:
  - 2 low side switches with maximum operation of 2.6A
  - 2 low side switches with maximum operation of 350mA
- 1 low side driver for resistive loads with maximum operation current of 3A including overtemperature and overcurrent protection
- Configurable variable reluctance sensor interface
- Reset output and 5V undervoltage detection
- Watchdog
- Green Product (RoHS compliant)
- AEC Qualified

### Description

The TLE8080EM is an engine management IC based on Infineon Smart Power Technology (SPT). It is protected by embedded protection functions and integrates a power supply, K-line, SPI, variable reluctance sensor interface and power stages to drive different loads in an engine management system. It provides a compact and cost optimized solution for engine management systems. It is very suitable for one cylinder motorcycle engine management systems.

### TLE8080-2EM and TLE8080-3EM

TLE8080-2EM differs from the main version in parameters “V5DD Reset Threshold for TLE8080-2EM and TLE8080-3EM” and “Power On Reset Delay Time for TLE8080-2EM” in Chapter 5.4.

TLE8080-3EM differs from the main version in parameter “V5DD Reset Threshold for TLE8080-2EM and TLE8080-3EM” in Chapter 5.4.

| Type | Package | Marking |
|---|---|---|
| TLE8080EM | PG-SSOP24 | TLE8080EM |
| TLE8080-2EM | PG-SSOP24 | TLE8080-2EM |
| TLE8080-3EM | PG-SSOP24 | TLE8080-3EM |

# Table of Contents

# 2 Block Diagram

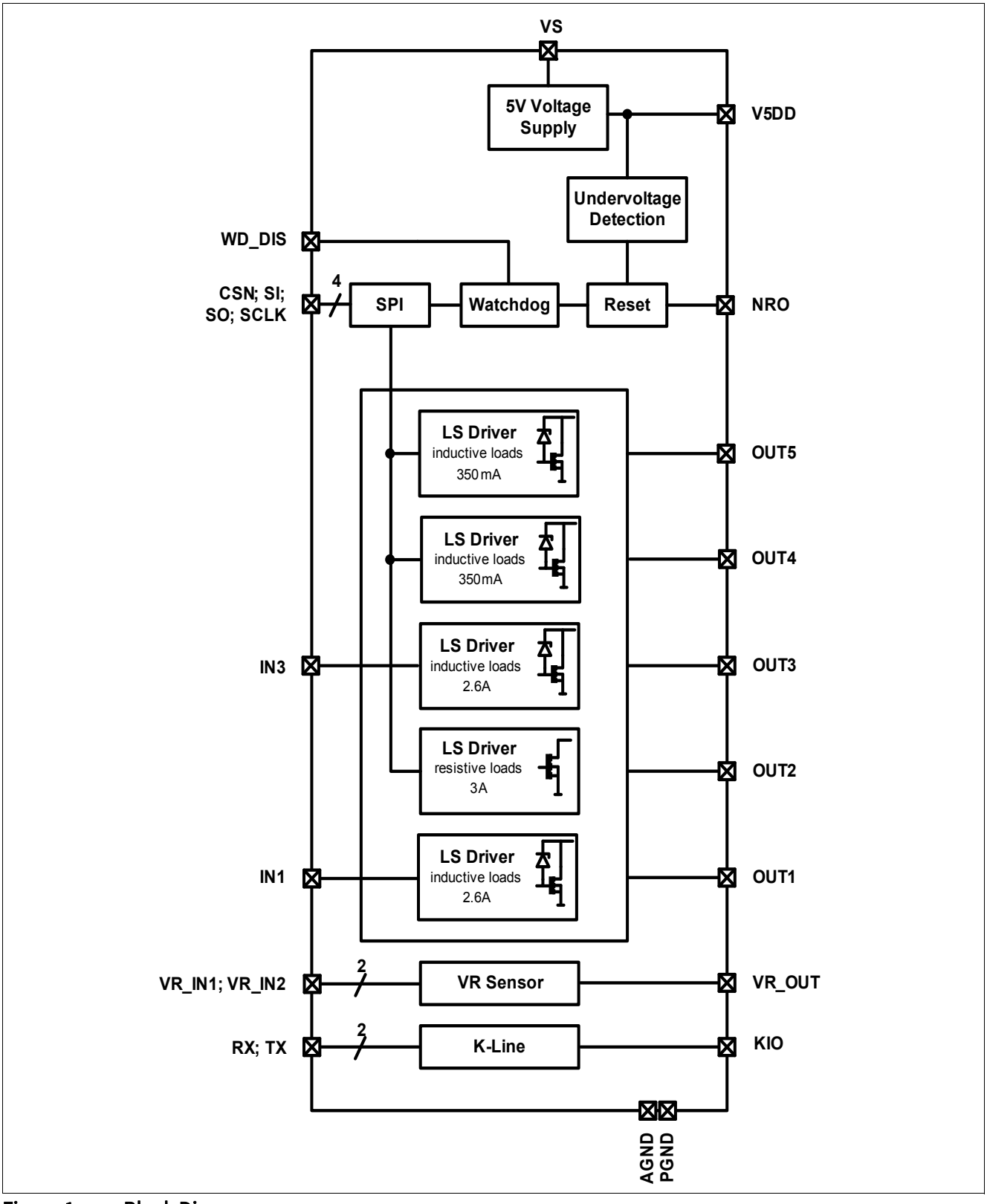



Figure 1 Block Diagram

# 3 Pin Configuration

## 3.1 Pin Assignment

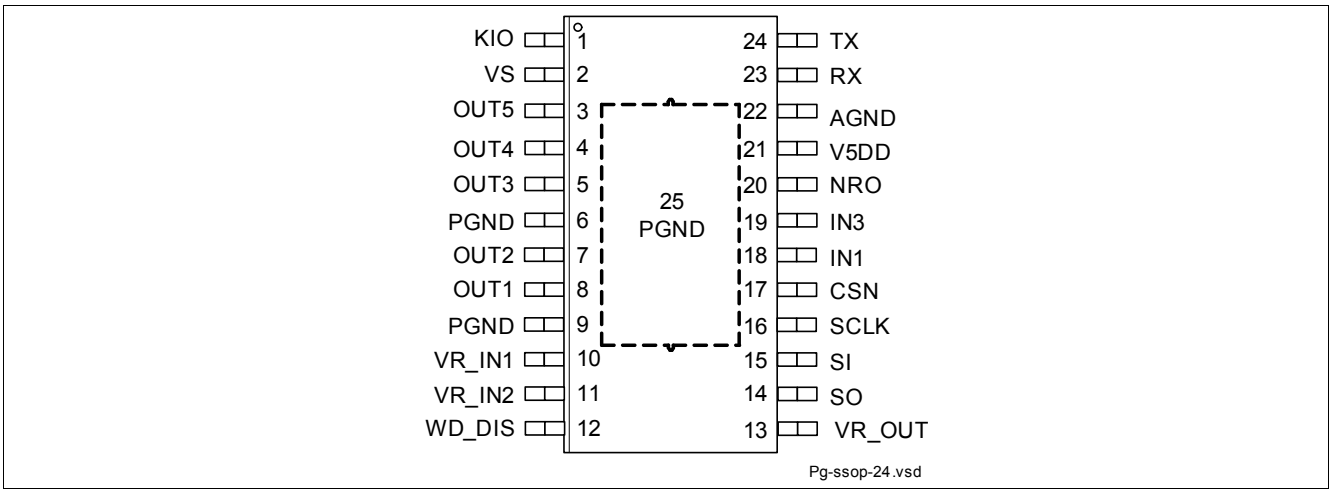



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | KIO | **K-Line Bus Connection** |
| 2 | VS | **Battery Voltage:** Block to AGND directly at the IC with min. 100nF ceramic capacitor |
| 3 | OUT5 | **Output Channel 5** |
| 4 | OUT4 | **Output Channel 4** |
| 5 | OUT3 | **Output Channel 3** |
| 6 | PGND | **Power Ground:** internally connected to pin 9, connect externally to pin 9 |
| 7 | OUT2 | **Output Channel 2** |
| 8 | OUT1 | **Output Channel 1** |
| 9 | PGND | **Power Ground:** internally connected to pin 6, connect externally to pin 6 |
| 10 | VR_IN1 | **VR Sensor Interface Input 1** |
| 11 | VR_IN2 | **VR Sensor Interface Input 2** |
| 12 | WD_DIS | **Watchdog Disable:** high active; internal pull down |
| 13 | VR_OUT | **VR Sensor Output** |
| 14 | SO | **SPI Slave Output:** high impedance |
| 15 | SI | **SPI Slave Input:** internal pull down |
| 16 | SCLK | **SPI Clock Input:** internal pull down |
| 17 | CSN | **SPI Chip Select Input:** low active; internal pull up |
| 18 | IN1 | **Control Input Channel 1:** internal pull down |

## Pin Configuration

| Pin | Symbol | Function |
|---|---|---|
| 19 | IN3 | **Control Input Channel 3:** internal pull down |
| 20 | NRO | **Reset Output:** low active, open drain |
| 21 | V5DD | **5V Supply Output:** connected to external blocking capacitor |
| 22 | AGND | **Analog Ground:** connected to system logic ground |
| 23 | RX | **K-Line Receive Output:** logic output of data received from the K-Line bus KIO |
| 24 | TX | **K-Line Transmit Input:** logic level input for data to be transmitted on the K-Line bus KIO; internal pull up |
| 25 | Exposed Pad | **Substrate Connection:** must be connected to PGND externally on PCB |

# 4 General Product Characteristics

**Table 1 Absolute Maximum Ratings [1)]**

$T_j$ = -40°C to +150°C: All voltages with respect to ground unless otherwise specified. Positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Supply Voltage VS | $V_{VS}$ | -0.3 | – | 40 | V | – | P_4.1.1 |
| Supply Voltage V5DD | $V_{V5DD}$ | -0.3 | – | 5.5 | V | – | P_4.1.2 |
| Input Voltage on Pins IN1, IN3, SCLK, SI, WD_DIS | $V_x$ | -0.3 | – | 5.5 | V | – | P_4.1.3 a |
| Input Voltage on Pins CSN, TX | $V_x$ | -0.3 | – | V5DD +0.3V | V | – | P_4.1.3 b |
| Input Voltage VR_IN1, VR_IN2 | $V_{VR\_IN1/2}$ | -0.3 | – | 5.5 | V | see also 4.2.1 and 4.2.2 | P_4.1.4 |
| DC Voltage on Pins OUT1-5 | $V_x$ | -0.3 | – | 30 | V | respect to PGND all channels are switched off | P_4.1.5 |
| DC Voltage on Pins VR_OUT, SO, RX, NRO | $V_x$ | -0.3 | – | 5.5 | V | $I_x$ < 1mA | P_4.1.6 |
| DC Voltage AGND to PGND | $V_x$ | -0.3 | – | 0.3 | V | | P_4.1.7 |
| DC Voltage on Pin KIO | $V_{KIO}$ | -0.3 | – | 35 | V | respect to PGND KIO is switched off | P_4.1.8 |
| **Currents** | | | | | | | |
| Input Current between VR_IN1 and VR_IN2 | $I_{VR\_IN1,VR\_IN2}$ | -- | – | 50 | mA | – | P_4.2.1 |
| Input Current VR_IN1, VR_IN2 to GND | $I_{VR\_IN1/2,GND}$ | -- | – | 10 | mA | – | P_4.2.2 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.3.1 |
| Storage Temperature | $T_{stg}$ | -55 | – | 150 | °C | – | P_4.3.2 |
| **ESD Susceptibility** | | | | | | | |
| ESD Resistivity all Pins to GND | $V_{ESD}$ | -2 | – | 2 | kV | HBM [2)] | P_4.4.1 |
| ESD Resistivity all Pins to GND | $V_{ESD}$ | -500 | – | 500 | V | CDM [3)] | P_4.4.2 |
| ESD Resistivity Pin 1, 12, 13, 24 (corner pins) to GND | $V_{ESD1,19,20,36}$ | -750 | – | 750 | V | CDM [3)] | P_4.4.3 |

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to EIA/JESD 22-A114B.
3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1.

### Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

**Table 2 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply Voltage | $V_S$ | 6 | – | 18 | V | – | P_4.5.1 |
| Junction Temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.5.2 |

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

**Table 3 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Case | RthJC | – | 7 | – | K/W | 1) | P_4.6.1 |
| Junction to Ambient | RthJA | – | 29 | – | K/W | 1) 2) | P_4.6.2 |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

# 5 5V Supply, Reset and Supervision

## 5.1 5V Supply

The TLE8080EM integrates a voltage regulator for load currents up to 250mA. The input voltage at VS is regulated to 5V on V5DD with a precision of ±2%. The design allows to achieve stable operation even with ceramic output capacitors down to 470nF. It is protected against overload, short circuit, and over temperature conditions. For low drop operation, a charge pump is implemented.

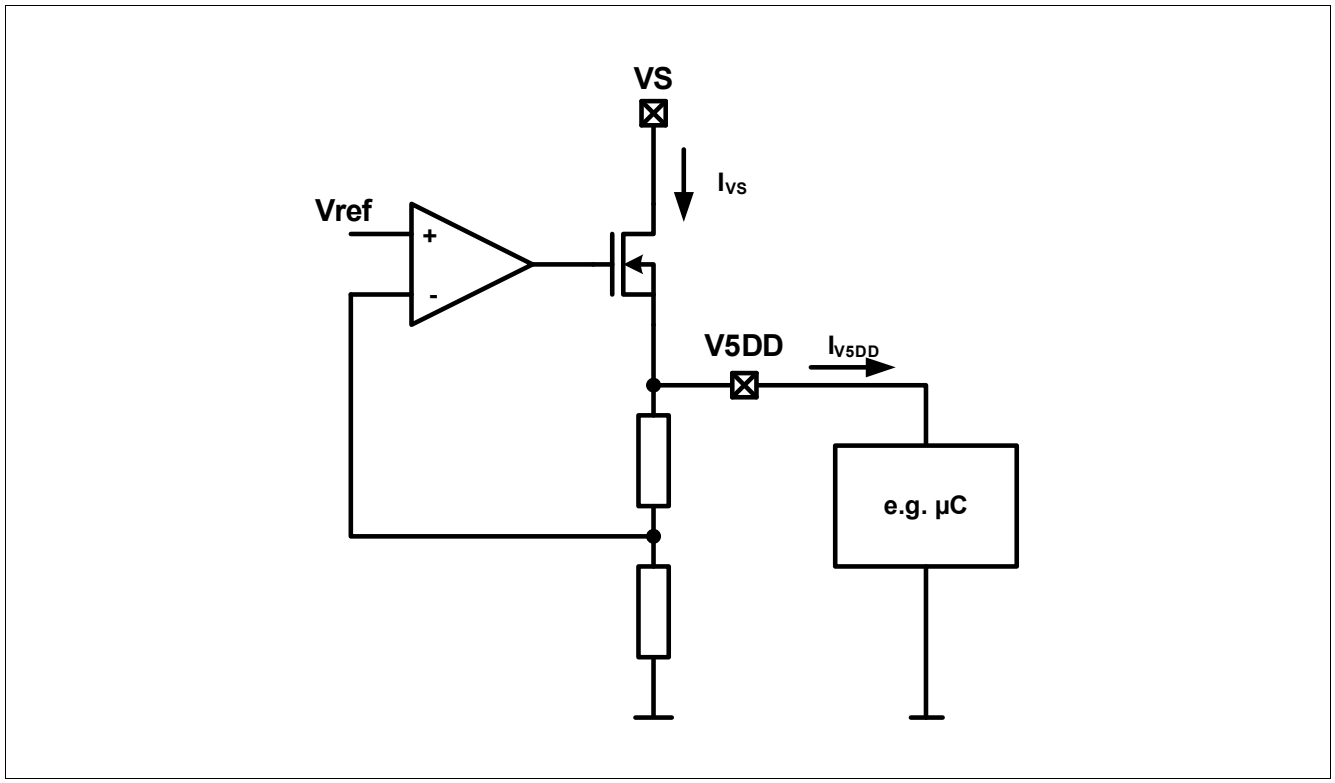



Figure 3 5V Supply

## 5.2 Power On Reset and Reset Output

The reset output NRO is an open drain output. When the level of $V_{V5DD}$ reaches the reset threshold ($V_{RT}$) (increasing voltage $V_{V5DD}$) the signal at NRO remains low for the power-up reset delay time ($t_{RD}$). The reset function and timing is illustrated in Figure 4. The reset reaction time ($t_{RR}$ ) avoids wrong triggering caused by short “glitches” on the V5DD-line. In case of V5DD power down (decreasing voltage; $V_{V5DD} < V_{RT}$ for $t < t_{RR}$ ) a logic low signal is generated at the pin NRO to reset an external micro controller. The level of the reset threshold for increasing $V_{V5DD}$ is for the hysteresis ($V_{RH}$) higher than the level for decreasing $V_{V5DD}$.

With an active reset all power stages and the K-Line output are disabled and SPI commands are ignored.

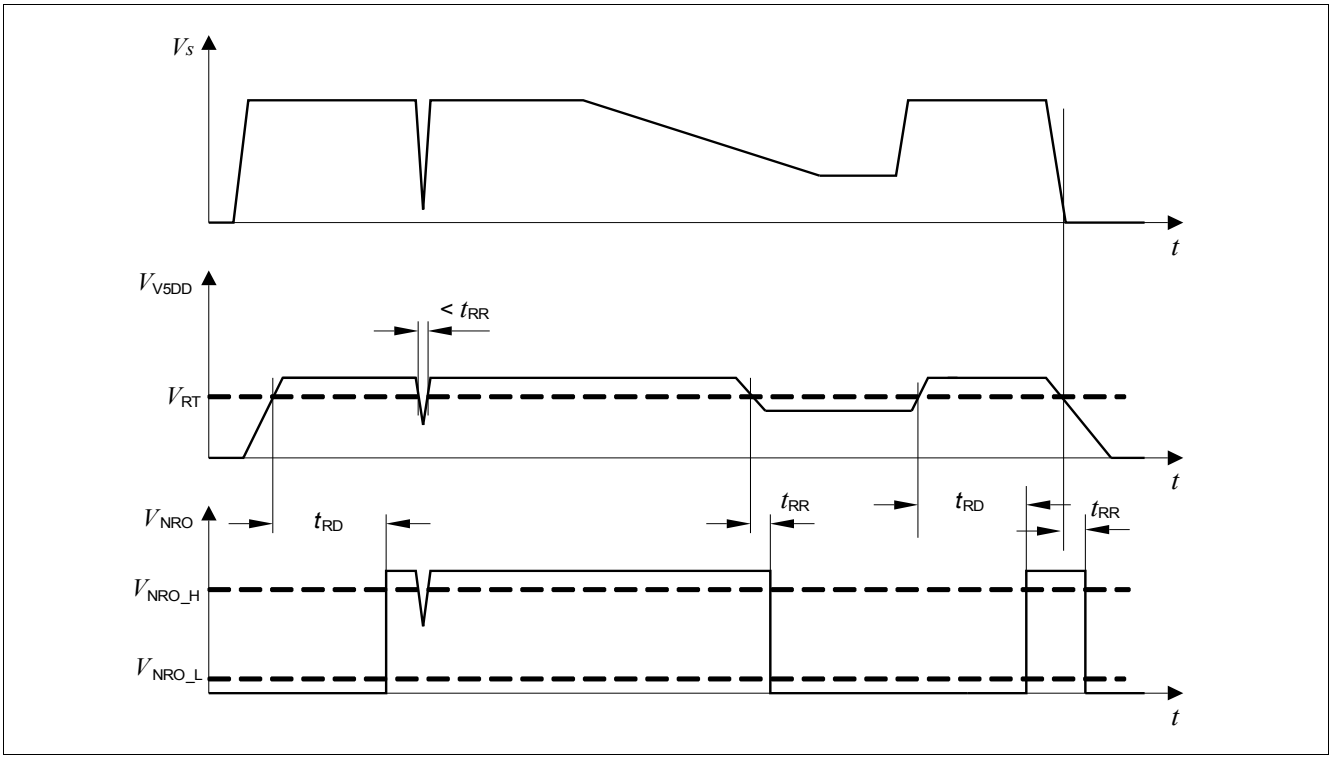



**Figure 4 Reset Timing Diagram**

## 5.3 Watchdog Operation

The TLE8080EM integrates a watchdog function which monitors the correct SPI communication with the micro controller. A watchdog disable pin ( WD_DIS ) with an internal pull down current source is implemented. With a high level the watchdog function is disabled.

For enabled watchdog function after power-up reset delay time ( $t_{RD}$ ), valid SPI communication from the micro controller must occur within the watchdog period ( $t_{WP}$ ) specified in the electrical characteristics. A restart of the watchdog period is done with a low to high transition of the CSN pin of a valid transmission of a 16 bit message.

A reset is generated (NRO goes LOW) for the time ( $t_{WR}$ ) if there is no restart during the watchdog period as shown in **Figure 5**.

Status after watchdog overflow:

- all outputs are switched off
- SPI registers are not influenced
- Watchdog Time Out bit in SPI status register is set
- first answer to SPI communication is the content of the status register

Switching of Outputs and reset of Watchdog Time Out Bit after watchdog overflow:

- Outputs 1 and 3 will be switched on with an positive edge at IN1 respectively IN3
- Outputs 2, 4 and 5 will be switched on with a write command to CMD register
- the watchdog time out bit will be reset with the rising edge of CSN of the first read command of the status register

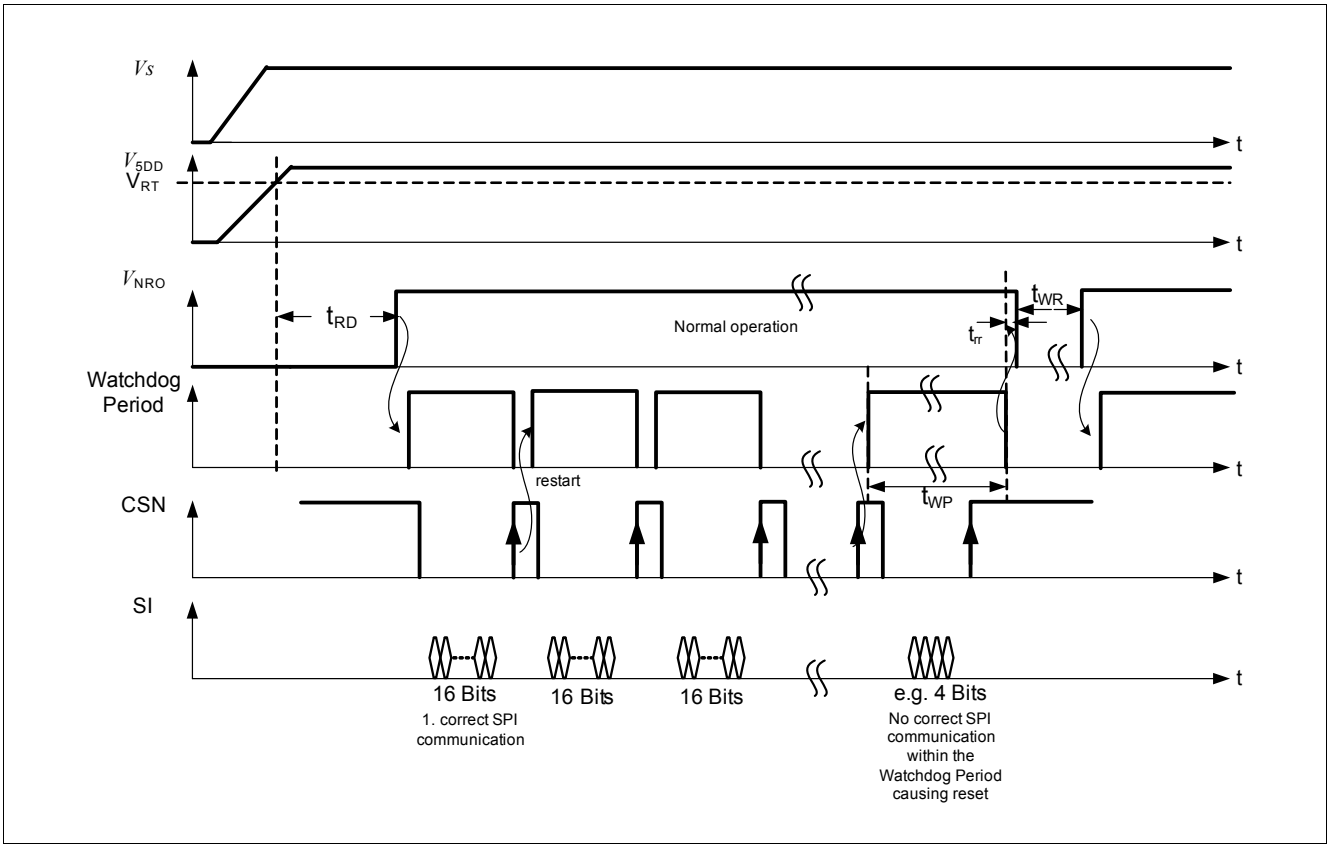



**Figure 5 Watchdog Timing Diagram**

## 5.4 Electrical Characteristics 5V Supply, Reset and Supervision

**Table 4 Electrical Characteristics: 5V Supply, Reset and Supervision**

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **5V Supply** | | | | | | | |
| Output Voltage | $V_{V5DD}$ | 4.9 | 5 | 5.1 | V | 0 mA < $I_{V5DD}$ < 250mA, 6V < $V_S$ < 18V | P_5.1.1 |
| Output Current Limitation | $I_{V5DD}$ | 250 | – | 650 | mA | $V_{V5DD}$ = 0V | P_5.1.2 |
| Load Regulation | $\Delta V_{V5DD, Lo}$ | – | – | 50 | mV | 1 mA < $I_{V5DD}$ < 250mA | P_5.1.3 |
| Line Regulation | $\Delta V_{V5DD, Li}$ | – | – | 10 | mV | $I_{V5DD}$ = 1mA, 10V < $V_S$ < 18V | P_5.1.4 |
| Power Supply Rejection | *PSRR* | – | 60 | – | dB | $f$ = 100Hz, $V_{S, ripple}$ = 0.5 Vpp [1] | P_5.1.5 |
| Output Capacitor | $C_{V5DD}$ | 470 | – | – | nF | [1] | P_5.1.6 |
| Output Capacitor ESR | $ESR(C_{V5DD})$ | – | – | 10 | Ω | [1] | P_5.1.7 |
| Current Consumption | $I_{VS}$ | – | 5.5 | 8 | mA | $I_{V5DD}$= 0mA, all channels and K-Line off | P_5.1.8 |
| Low Drop Voltage | $V_{V5DD}$ | 4.8 | – | 5 | V | $I_{V5DD}$ = 1mA $V_S$ =5V | P_5.1.9 |
| | | 4.15 | – | 5 | V | $I_{V5DD}$ = 250mA $V_S$ = 5V, after device ramp-up ($V_S$ > 9V) | P_5.1.10 a |
| | | 4.8 | – | - | V | $I_{V5DD}$ ≤ 250mA $V_S$ = 5.5 V, after device ramp-up ($V_S$ > 9V) [1] | P_5.1.10 b |
| **Over Temperature Protection** | | | | | | | |
| Over Temperature Threshold | $T_{OT}$ | 150 | – | 200 | °C | [1] | P_5.2.1 |
| Over Temperature Hysteresis | $T_{OT,Hys}$ | – | 20 | – | °C | [1] | P_5.2.2 |

**Table 4 Electrical Characteristics: 5V Supply, Reset and Supervision** (cont'd)

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Under Voltage Detection** | | | | | | | |
| V5DD Reset Threshold for TLE8080EM | $V_{RT}$ | 4.00 | 4.25 | 4.50 | V | $V_{V5DD}$ decreasing, only at version TLE8080EM | P_5.3.1 |
| Reset Hysteresis | $V_{RH}$ | 10 | – | 150 | mV | | P_5.3.2 |
| V5DD Reset Threshold for TLE8080-2EM and TLE8080-3EM | $V_{RT}$ | 3.4 | 3.65 | 3.9 | V | $V_{V5DD}$ decreasing, only at versions TLE8080-2EM and TLE8080-3EM | P_5.3.3 |
| **Power On Reset** | | | | | | | |
| Power On Reset Delay Time for TLE8080EM and TLE8080-3EM | $t_{RD}$ | 10 | 15 | 20 | ms | only at versions TLE8080EM and TLE8080-3EM | P_5.4.1 |
| Power On Reset Delay Time for TLE8080-2EM | $t_{RD}$ | 30 | 40 | 50 | ms | only at version TLE8080-2EM | P_5.4.2 |
| Reset Reaction Time | $t_{RR}$ | 10 | 15 | 20 | µs | | P_5.4.3 |
| **Reset Output NRO** | | | | | | | |
| Low Level Output Voltage | $V_{NRO,L}$ | – | – | 1.1 | V | $I_{NRO}$ = 1mA | P_5.5.1 |
| **Watchdog** | | | | | | | |
| Watchdog Period | $t_{WP}$ | 50 | 60 | 70 | ms | | P_5.6.1 |
| Watchdog Reset Time | $t_{WR}$ | 120 | 240 | 360 | µs | | P_5.6.2 |
| **Input Characteristics WD_DIS** | | | | | | | |
| Low Level Input Voltage | $V_{WD\_DIS,L}$ | – | – | 1 | V | | P_5.7.1 |
| High Level Input Voltage | $V_{WD\_DIS,H}$ | 2 | – | – | V | | P_5.7.2 |
| Pull Down Current | $I_{WD\_DIS,pd}$ | 20 | 50 | 100 | µA | at $V_{IN}$ = 5V | P_5.7.3 |
| Pull Down Current | $I_{WD\_DIS,pd}$ | 2.4 | – | – | µA | at $V_{IN}$ = 0.6V | P_5.7.4 |
| Hysteresis | $V_{WD\_DIS,Hys}$ | 30 | | 250 | mV | | P_5.7.5 |

1) Not subject to production test, specified by design.

# 6 Power Stages

## 6.1 Low Side Switches

The power stages are built by N-channel power MOSFET transistors. The channels are universal multi channel switches, but are mostly suitable to be used in engine management systems. Within an engine management system, the best fit of the channels to the typical loads is:

- Channel 1 and 3 for injector valves or similar sized solenoids with a maximum operation current requirement of 2.6A
- Channel 2 for malfunction indication lamps or other resistive loads with a maximum current requirement of 3A
- Channel 4 and 5 for relays or other inductive loads with a maximum current requirement of 350mA

The channels are switched off while reset is active (pin NRO is low). After an power on reset the channels will be switched on with a positive edge at IN1 respectively IN3 or with a switch on command over SPI.

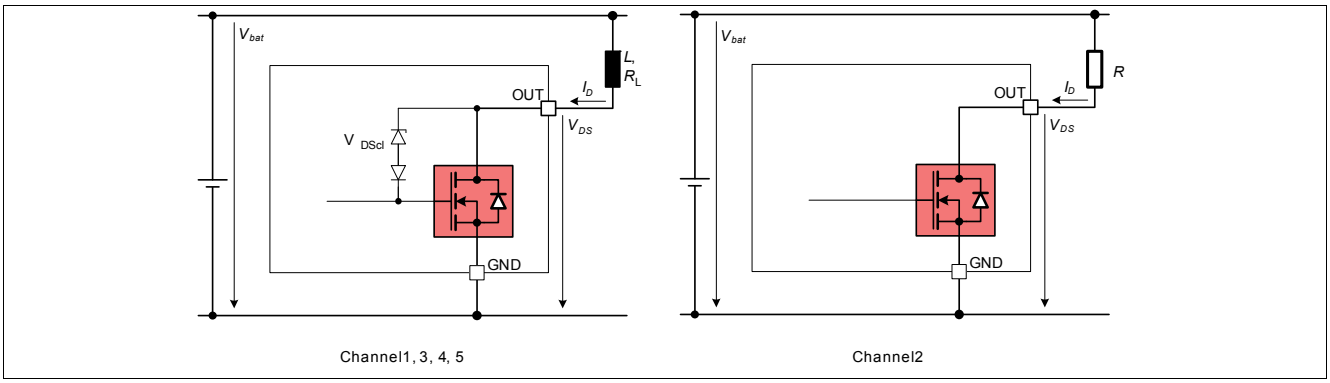



**Figure 6 Low Side Switches**

In Table 5 the control concept, typical loads, the implemented protection and monitor functions are illustrated.

**Table 5 Overview Diagnosis Function**

| Channel | Control | Recommended Load | Over Temperature | Over Current | Open Load/ Short to GND |
|---|---|---|---|---|---|
| 1 | Pin IN1 | Injector Valve | x | Latch 1) | x |
| 2 | SPI CMD Register Bit 0 | MIL (max. 3W) | x | repetitive switching; off time $t_{oc,off}$ 1) | – |
| 3 | Pin IN3 | Valve | x | Latch 1) | x |
| 4 | SPI CMD Register Bit 1 | Relay | one temperature sensor for channel 4 and channel 5 | Latch 1) | x |
| 5 | SPI CMD Register Bit 2 | Relay | one temperature sensor for channel 4 and channel 5 | Latch 1) | x |

1) Reset behavior of the diagnosis bits see Chapter 8.2.

In overcurrent condition the affected channel will be switched off. There are two different implementations for switching on again after an over current event.

For channels 1, 3, 4 and 5 the switch off state is latched. The input pins IN1, IN3 must be set to low to reset the latch before the channel can be switched on again.
For channels 4 and 5 the over current status is reset with a write command to the CMD register after a Diagnosis Read Command has been sent. The switching state is according to the status of bit 1 and 2.

Channel 2 will be switched off and after $t_{oc\_off}$ = 5ms typically the channel will be switched on again automatically. The result is repetitive switching with a fixed off time of $t_{oc,off}$. The overcurrent status of channel 2 is internally latched. For releasing the over current diagnosis bit after over current condition, channel 2 must stay switched on for at least $t_{oc,St}$.

The bits 0 to 4 in the Stat register reflect the actual switching status of the channels. For detailed description see Chapter 8.2.2.
All the channels are protected from over temperature. In an overtemperature situation the affected channel will be switched off. The channel will restart operation if the junction temperature decreases by thermal shutdown hysteresis $T_{OT,Hys}$. Channels 4 and 5 are using a common temperature sensor. Therefore, the two channels are switched together during over temperature.

For channels 1, 3, 4 and 5 an open load/short to GND in off detection with a pull down current source (active in off) and a comparator is implemented. In case of switch off and the output voltage is below the open load detection threshold ($V_{outx} < V_{ol,th}$), the open load in off timer is started. After the open load in off delay time $t_{ol,d}$ , the open load is detected (timing see Figure 9 and Figure 10).

The diagnosis status of the channels is monitored in the SPI Diagnosis Register DIAG (see Chapter 8.2).

## 6.2 Electrical Characteristics Low Side Switches

**Table 6 Electrical Characteristics: Power Stage**

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Output Channel 1 and 3** | | | | | | | |
| On Resistance | $R_{OUTx\_on}$ | – | 0.6 | 0.7 | Ω | $I_{OUTx\_nom}$ = 1.3A, $T_j$ = 150°C | P_6.1.1 |
| Output Clamping Voltage | $V_{OUTx\_cl}$ | 30 | 35 | 40 | V | $I_{OUTx}$ = 0.02A | P_6.1.2 |
| Over-current Switch Off Threshold | $I_{OUTx\_oc}$ | 2.6 | – | 5 | A | | P_6.1.3 |
| Over-current Switch Off Filter Time | $t_{oc,f}$ | 0.5 | – | 3 | µs | | P_6.1.4 |
| Over Temperature Switch Off | $T_{OT}$ | 150 | – | 200 | °C | | P_6.1.5 |
| Over Temperature Hysteresis | $T_{OT,Hys}$ | – | 20 | – | °C | | P_6.1.6 |
| Open Load in Off Detection Threshold | $V_{ol,th}$ | 2 | 2.8 | 3.2 | V | | P_6.1.7 |
| Open Load in Off Pull Down Diagnosis Current | $I_{ol}$ | 50 | 100 | 150 | µA | $V_{OUTx}$ = 13.5V | P_6.1.8 |
| Open Load in Off Diagnosis Delay Time | $t_{ol,d}$ | 100 | – | 200 | µs | | P_6.1.9 |
| Turn On Delay Time | $t_{d,ON}$ | – | 0.25 | 1 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load [1] | P_6.1.10 |
| Turn Off Delay Time | $t_{d,OFF}$ | – | 0.9 | 1.5 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load [1] | P_6.1.11 |
| Turn On Time | $t_{s,ON}$ | – | 0.6 | 1.2 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load [1] | P_6.1.12 |
| Turn Off Time | $t_{s,OFF}$ | – | 0.6 | 1.2 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load [1] | P_6.1.13 |
| Output Leakage Current in Off Mode | $I_{OUTx\_off}$ | – | – | 3 | µA | $V_{OUTx}$ = 13.5V, $T_j$ = 150°C [2] | P_6.1.14 |
| **Output Channel 2** | | | | | | | |
| On Resistance | $R_{OUTx\_on}$ | – | 1.1 | 1.2 | Ω | $I_{OUTx\_nom}$ = 0.3A, $T_j$ = 150°C | P_6.2.1 |
| Over-current Switch Off Threshold | $I_{OUTx\_oc}$ | 3 | – | 6.5 | A | | P_6.2.2 |
| Over-current Switch Off Filter Time | $t_{oc,f}$ | 0.5 | – | 3 | µs | | P_6.2.3 |
| Over-current Switch Off Time | $t_{oc,off}$ | 3 | – | 8 | ms | | P_6.2.4 |
| Over-current Status Time | $t_{oc,St}$ | 1 | – | 12 | ms | | P_6.2.5 |
| Over Temperature Switch Off | $T_{OT}$ | 150 | – | 200 | °C | | P_6.2.6 |

**Table 6 Electrical Characteristics: Power Stage** (cont'd)

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Over Temperature Hysteresis | $T_{OT,Hys}$ | – | 20 | – | °C | | P_6.2.7 |
| Turn On Delay Time | $t_{d,ON}$ | – | 0.6 | 1.2 | µs | $V_{OUTx}$ = 13.5, $I_{OUTx}$ = 1.3A, resistive load 1) | P_6.2.8 |
| Turn Off Delay Time | $t_{d,OFF}$ | – | 0.7 | 1.5 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load 1) | P_6.2.9 |
| Turn On Time | $t_{s,ON}$ | – | 0.4 | 1 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load 1) | P_6.2.10 |
| Turn Off Time | $t_{s,OFF}$ | – | 0.4 | 1 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 1.3A, resistive load 1) | P_6.2.11 |
| Output Leakage Current in Off Mode | $I_{OUTx\_off}$ | – | – | 3 | µA | $V_{OUTx}$ = 13.5V, $T_j$ = 150°C | P_6.2.12 |
| **Output Channel 4 and 5** | | | | | | | |
| On Resistance | $R_{OUTx\_on}$ | – | 3.3 | 3.6 | Ω | $I_{OUTx\_nom}$ = 0.3A, $T_j$ = 150°C | P_6.3.1 |
| Output Clamping Voltage | $V_{OUTx\_cl}$ | 30 | 35 | 40 | V | $I_{OUTx}$ = 0.02A | P_6.3.2 |
| Over-current Switch Off Threshold | $I_{OUTx\_oc}$ | 350 | – | 600 | mA | | P_6.3.3 |
| Over-current Switch Off Filter Time | $t_{oc,f}$ | 0.8 | – | 2.4 | µs | | P_6.3.4 |
| Over Temperature Switch Off | $T_{OT}$ | 150 | – | 200 | °C | | P_6.3.5 |
| Over Temperature Hysteresis | $T_{OT,Hys}$ | – | 20 | – | °C | | P_6.3.6 |
| Open Load in Off Detection Threshold | $V_{ol,th}$ | 2 | 2.8 | 3.2 | V | | P_6.3.7 |
| Open Load in Off Pull Down Diagnosis Current | $I_{ol}$ | 50 | 100 | 150 | µA | $V_{OUTx}$ = 13.5V | P_6.3.8 |
| Open Load in Off Diagnosis Delay Time | $t_{ol,d}$ | 100 | – | 200 | µs | | P_6.3.9 |
| Turn On Delay Time | $t_{d,ON}$ | – | 0.5 | 1.2 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 0.3A, resistive load1) | P_6.3.10 |
| Turn Off Delay Time | $t_{d,OFF}$ | – | 0.7 | 1.5 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 0.3A, resistive load1) | P_6.3.11 |
| Turn On Time | $t_{s,ON}$ | – | 0.1 | 0.8 | µs | $V_{OUTx}$ = 13.5V $I_{OUTx}$ = 0.3A, resistive load1) | P_6.3.12 |

**Table 6 Electrical Characteristics: Power Stage** (cont'd)

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Turn Off Time | $t_{s,OFF}$ | – | 0.1 | 0.8 | µs | $V_{OUTx}$ = 13.5V, $I_{OUTx}$ = 0.3A, resistive load 1) | P_6.3.13 |
| Output Leakage Current in Off Mode | $I_{OUTx\_off}$ | – | – | 2 | µA | $V_{OUTx}$ = 13.5V, $T_j$ = 150°C 2) | P_6.3.14 |
| **Input Characteristic IN1 and IN3** | | | | | | | |
| Low Level Input Voltage | $V_{IN,L}$ | – | – | 1 | V | | P_6.4.1 |
| High Level Input Voltage | $V_{IN,H}$ | 2 | – | – | V | | P_6.4.2 |
| Input Voltage Hysteresis | $V_{IN,Hys}$ | 50 | 110 | 250 | mV | | P_6.4.3 |
| Pull Down Current | $I_{IN,PD}$ | 20 | 50 | 100 | µA | $V_{IN}$ = 5V | P_6.4.4 |
| Pull Down Current | $I_{IN,PD}$ | 2.4 | – | – | µA | $V_{IN}$ = 0.6V | P_6.4.5 |

1) definition of timing see Figure 7 or Figure 8.

2) in OFF mode open load diagnosis pull down current active.

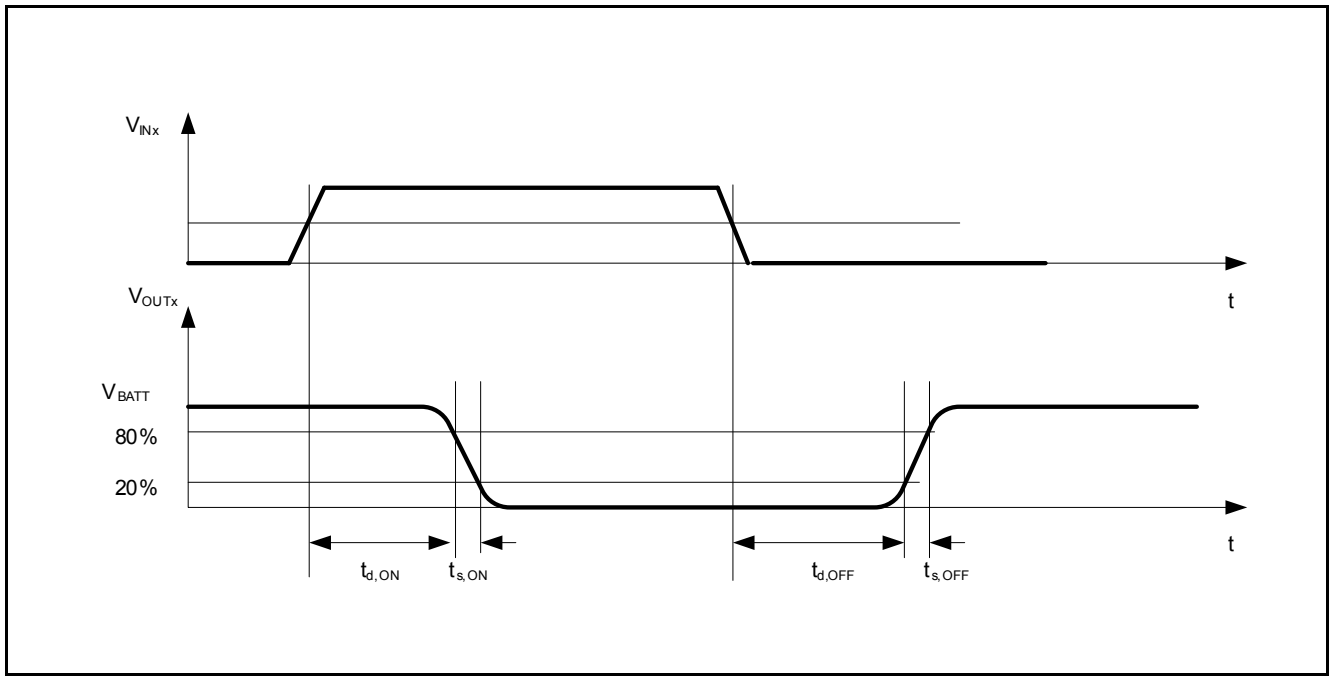



**Figure 7 Timing Low Side Switches Channel 1 and 3**

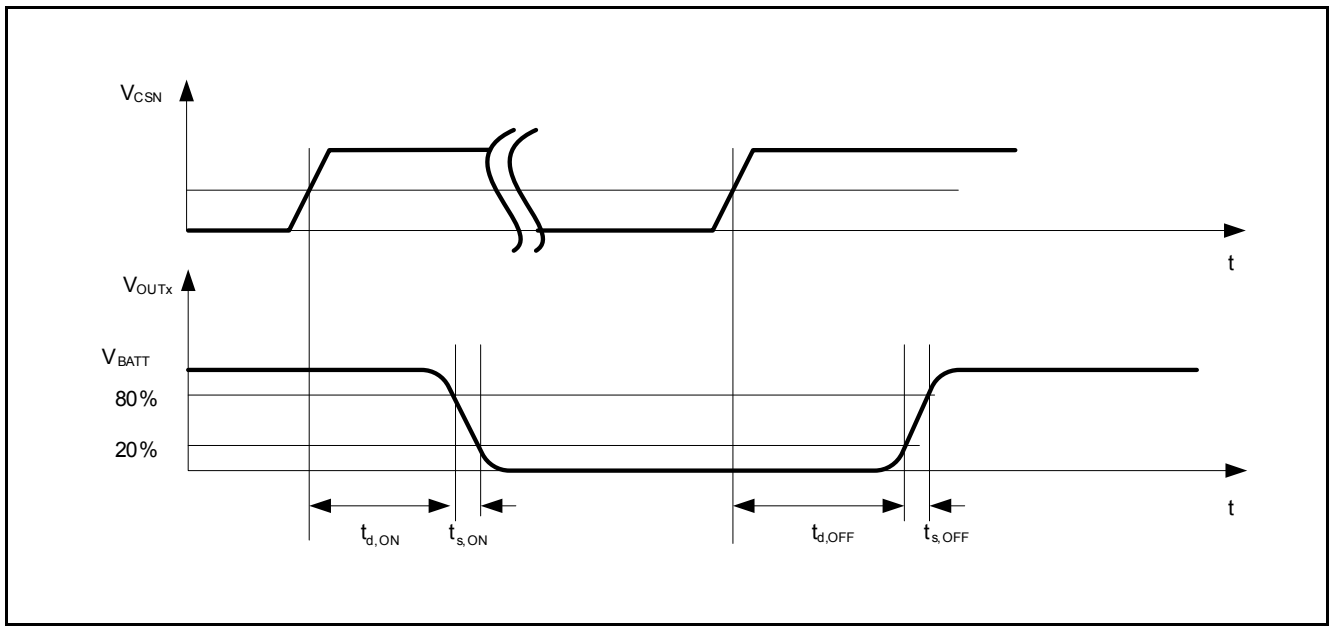



Figure 8 Timing Low Side Switches Channel 2, 4 and 5

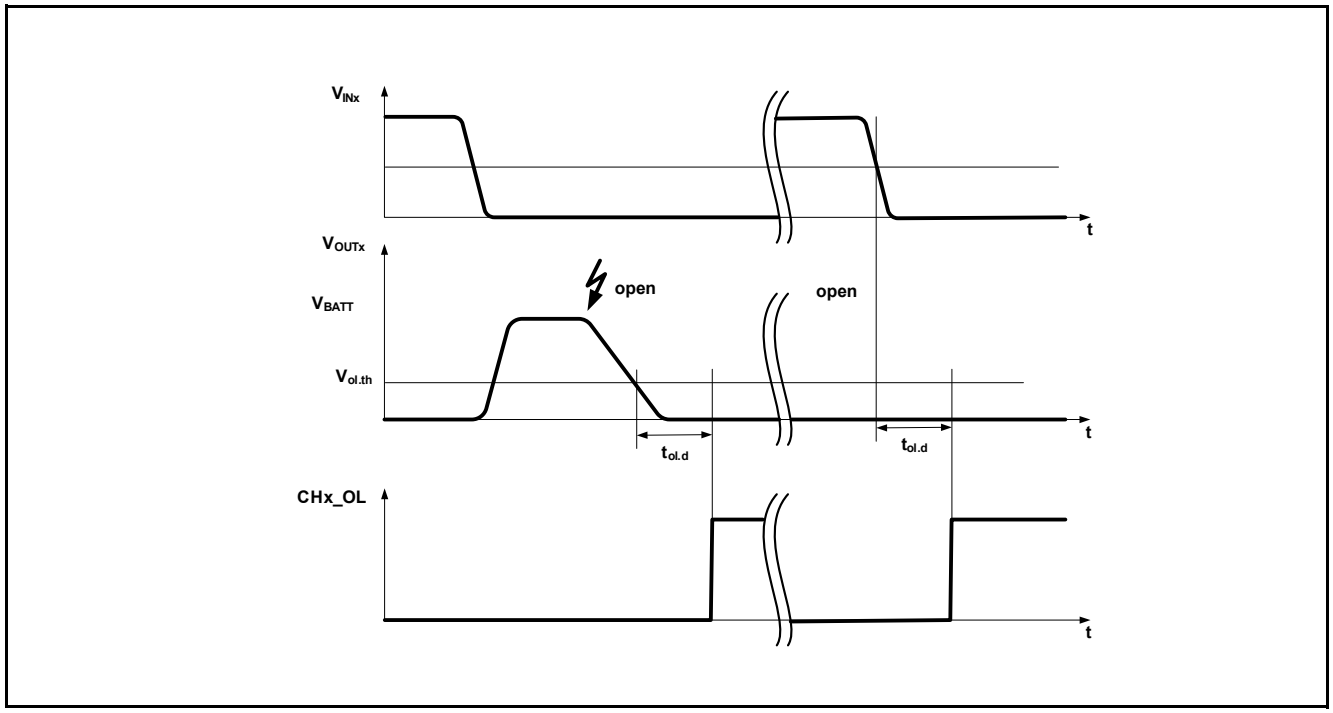



Figure 9 Timing Open Load/Short to GND in Off Detection Channel 1 and 3

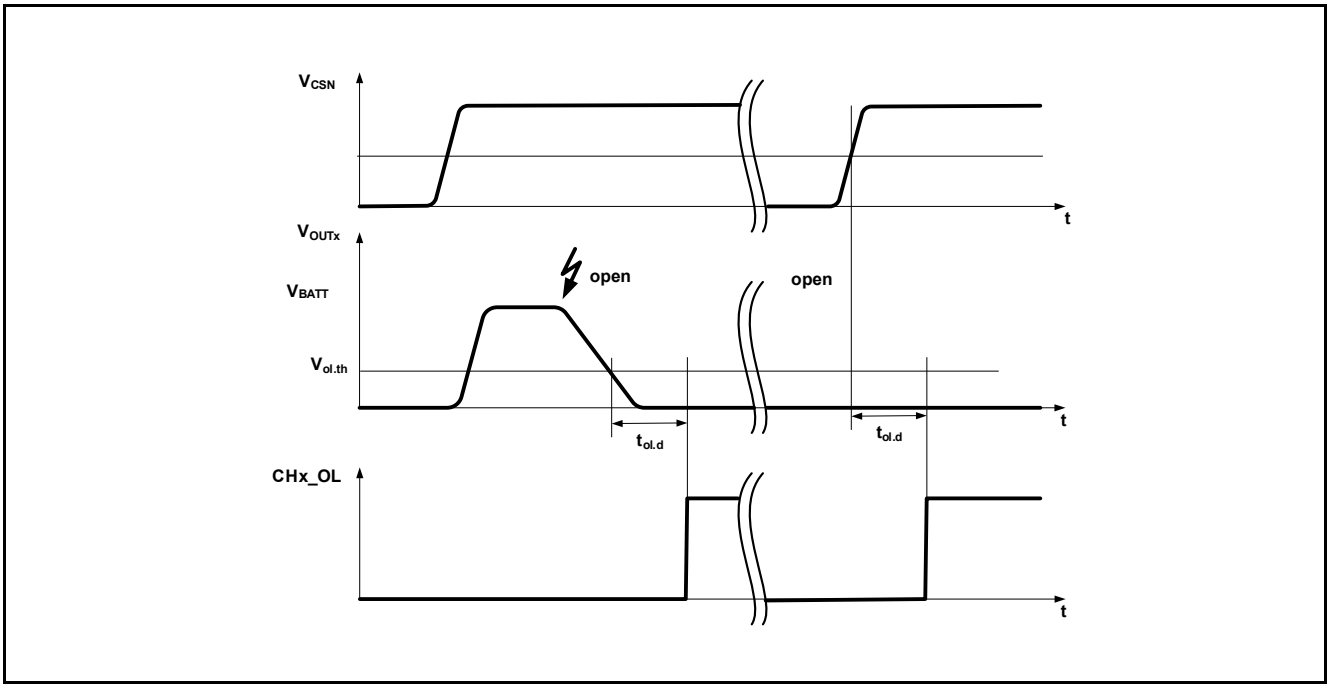



Figure 10 Timing Open Load/Short to GND in Off Detection Channel 2, 4 and 5

# 7 Variable Reluctance Sensor ( VRS ) Interface

The variable reluctance (VR) sensor interface converts an output signal of a VR sensor into a logic level signal suited for µC 5V input ports. The voltage difference between the two input pins, VR_IN1 and VR_IN2, which are connected to the two output pins of the VR sensor, is detected and the output pin VR_OUT is switched depending on the sign of the voltage difference (see Figure 12 ). The amplitude of the VR sensor signal is limited by an internal clamping circuit to avoid damage of the device due to over voltage caused by the VR sensor signal.

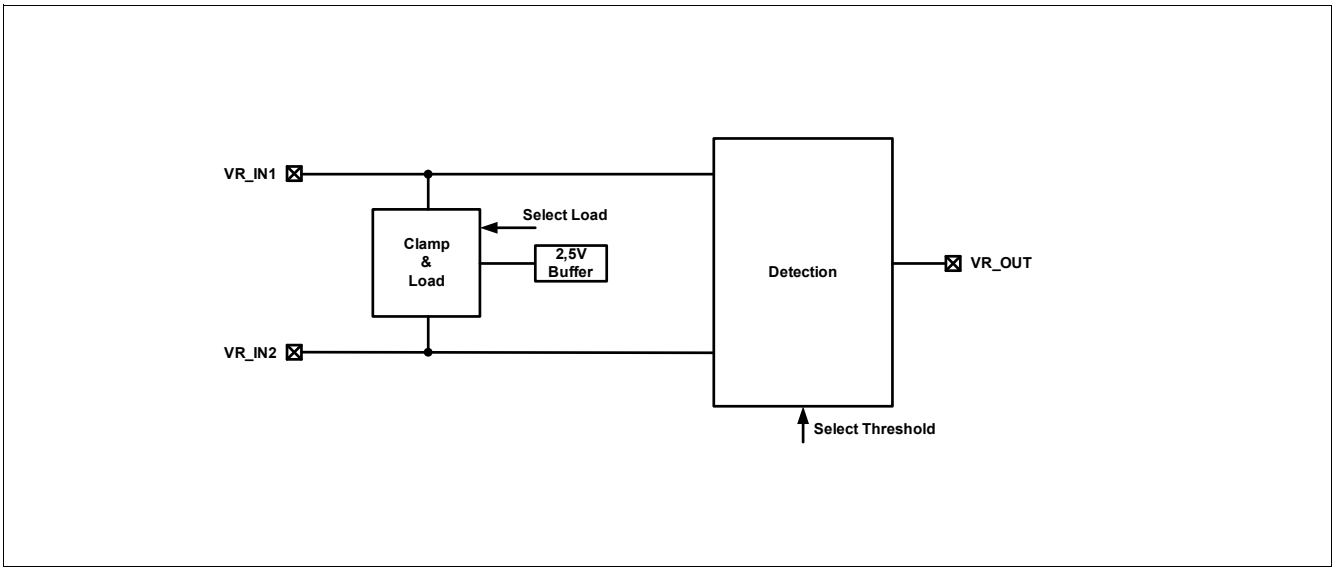



Figure 11 VR Sensor Interface Block Diagram

## 7.1 Electrical Characteristics VR Sensor Interface

**Table 7 Electrical Characteristics: VR Sensor Interface**

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input Characteristics:** | | | | | | | |
| Positive VR Sensor Interface Detection Threshold | $V_{VR,th\_pos}$ | -30 | 0 | 30 | mV | | P_7.1.1 |
| Negative VR Sensor Interface Detection Threshold | $V_{VR,th\_neg}$ | -80 | -50 | -20 | mV | CMD Register: VR_T[1:0] = “00” Reset State | P_7.1.2 |
| Negative VR Sensor Interface Detection Threshold | | -130 | -100 | -70 | mV | CMD Register: VR_T[1:0] = “01” | P_7.1.3 |
| Negative VR Sensor Interface Detection Threshold | | -550 | -500 | -450 | mV | CMD Register: VR_T[1:0] = “10” | P_7.1.4 |
| Negative VR Sensor Interface Detection Threshold | | -1.1 | -1 | -0.9 | V | CMD Register: VR_T[1:0] = “11” | P_7.1.5 |
| VR Sensor Interface Load Selection | $R_{VR,Load}$ | 30 | 75 | 120 | kΩ | $T_j$ = 25°C, CMD Register: VR_L[1:0] = “00” Reset State | P_7.1.6 |
| | | | 90 | | kΩ | $T_j$ = -40°C, CMD Register: VR_L[1:0] = “00” Reset State | |
| | | | 60 | | kΩ | $T_j$ = 150°C, CMD Register: VR_L[1:0] = “00” Reset State | |
| VR Sensor Interface Load Selection | | 3 | 4.5 | 8 | kΩ | CMD Register: VR_L[1:0] = “01” | P_7.1.7 |
| VR Sensor Interface Load Selection | | 1.5 | 2.2 | 3.3 | kΩ | CMD Register: VR_L[1:0] = “10” | P_7.1.8 |
| VR Sensor Interface Load Selection | | 0.7 | 1.2 | 1.9 | kΩ | CMD Register: VR_L[1:0] = “11” | P_7.1.9 |
| VR Sensor Interface Input Clamping Current | $I_{VR,clamp}$ | – | – | ±50 | mA | | P_7.1.10 |
| VR Sensor Interface Input Clamping Voltage | $V_{VR,clamp}$ | ±2.5 | ±3 | ±3.5 | V | $I_{VR,clamp}$ = ±50mA | P_7.1.11 |

**Table 7 Electrical Characteristics: VR Sensor Interface** (cont'd)

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Output Characteristics:** | | | | | | | |
| Low Level Output Voltage | $V_{VR\_OUT,L}$ | – | – | 0.3 | V | $I_{VR\_OUT}$ = 100µA | P_7.2.1 |
| High Level Output Voltage | $V_{VR\_OUT,H}$ | V5DD -0.3 | – | – | V | $I_{VR\_OUT}$ = -100µA | P_7.2.2 |
| **Transfer Characteristics:** | | | | | | | |
| Delay Time Input to VR_OUT falling edge | $t_{dr}$ | 1 | 1.5 | 2.5 | µs | | P_7.3.1 |
| Delay Time Input to VR_OUT rising edge | $t_{df}$ | 1 | 1.5 | 2.5 | µs | | P_7.3.2 |

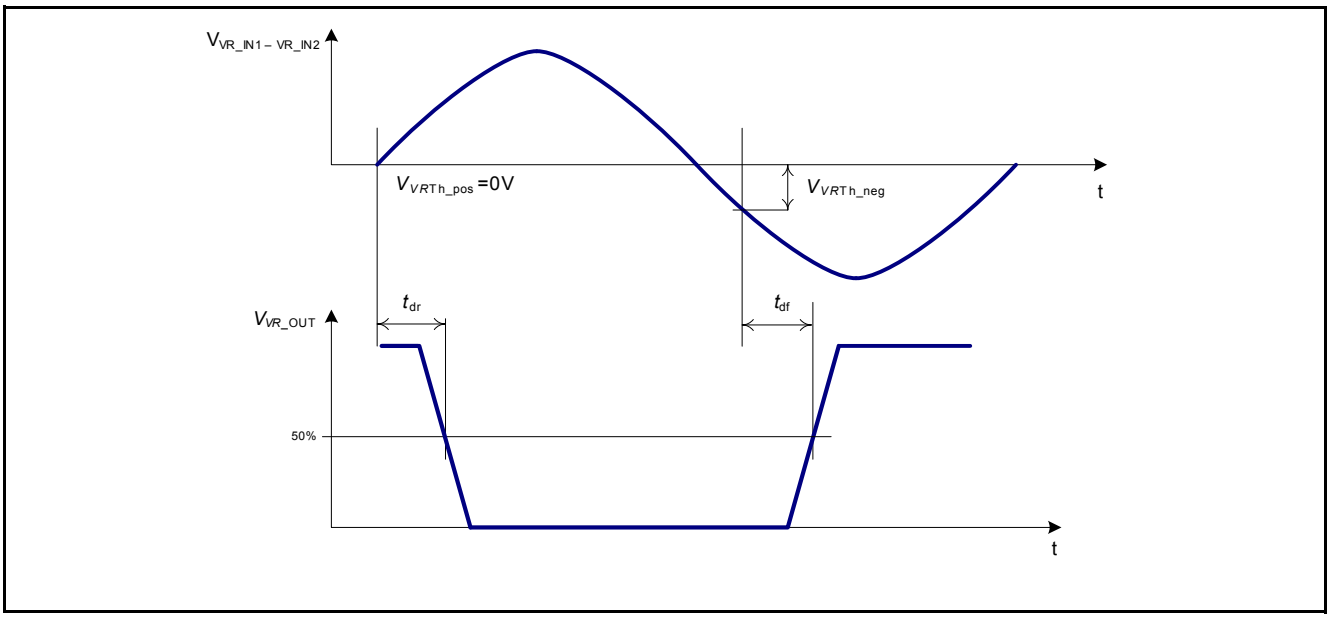



**Figure 12 Timing Characteristics of the VR Sensor Interface**

# 8 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).
The SPI is a 16 bit full duplex synchronous serial slave interface, which uses four lines: SI, SO, SCLK and CSN.

## 8.1 SPI Signal Description

**CSN - Chip Select:**
The system micro controller selects the IC by means of the CSN pin. Whenever the pin is in low state, data transfer can take place. As long as CSN is in high state, all signals at the SCLK and SI pins are ignored and SO is forced to high impedance.

CSN - High to Low Transition:
SO changes from high impedance to high or low state depending on the Status Flag (see Chapter 8.2).

CSN - Low to High Transition:
End of transmission, the validation check of the communication is done (number of bits and valid command) and valid commands are executed.

**SCLK - Serial Clock:**
This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select CSN makes any transition.

**SI - Serial Input:**
Serial input data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read on the falling edge of SCLK. Please refer to Section 8.2 for further information.

**SO - Serial Output:**
Data is shifted out serially at this pin, the MSB first. SO is in high impedance until the CSN pin goes to low. The output level before the first rising edge of SCLK depends on the status flag. New data will appear at the SO pin following the rising edge of SCLK. Please refer to Section 8.2 for further information.

## 8.2 SPI Protocol

The principle of the SPI communication is shown in Figure 13. The message from the micro controller must be sent MSB first. The data from the SO pin is sent MSB first. The TLE8080EM samples data from the SI pin on the falling edge of SCLK and shifts data out of the SO pin on the rising edge of SCLK. Each access must be terminated by a rising edge of CSN.

All SPI messages must be exactly 16-bits long, otherwise the SPI message is discarded.
There is a one message delay in the response to each message (i.e. the response for message N will be returned during message N+1).

The SPI protocol of the TLE8080EM provides three registers. The control register, the diagnosis, and the status register. The control register contains the set up bits for the VR sensor interface and the control bits of channels 2, 4 and 5. The diagnosis register contains the diagnosis bits of the five low side switches. The status register contains the status bits of the five low side switches, the watchdog status bit, and the watchdog time out bit. After power-on reset, all register bits are set to reset state (see Chapter 8.2.1).

There are four ways of valid access:

- Write access to the command register: the answer is 1 for the R/W bit, 00 for the address and the content of the register
- Read access to the command register: the answer is 0 for the R/W bit, 00 for the address and the content of the register
- Read access to the diagnosis register: the answer is 0 for the R/W bit, 01 for the address and the content of the register
- Read access to the status register: the answer is 0 for the R/W bit, 10 for the address and the content of the register

Any other access is recognized as an invalid message.

Status Flag Indication: after the falling edge of CSN and before the first rising edge of SCLK, the level of the SO indicates the status of the diagnosis register:

- SO = “0”: no error condition detected; all diagnosis register bits are “0”
- SO = “1”: one or more error conditions are detected; one or more diagnosis register bits are “1”

With this feature during every SPI communication a check of the diagnosis status can be done without additional read access of the diagnosis register.

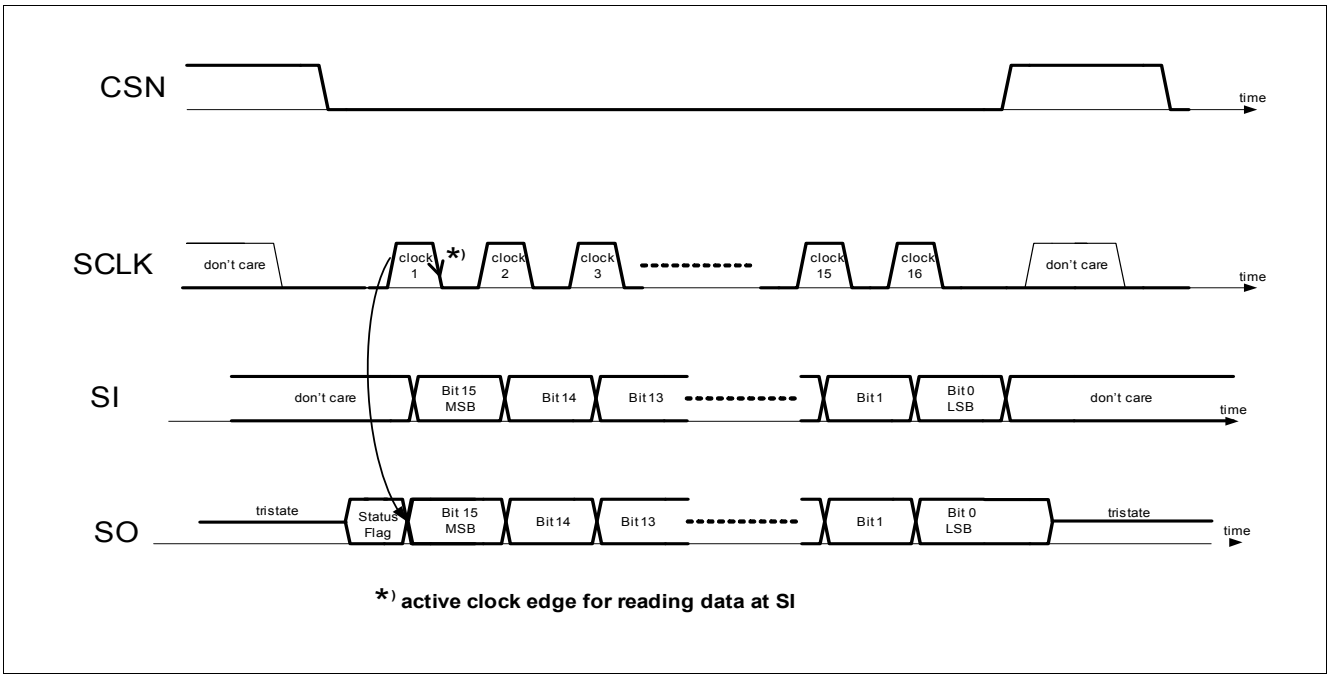



**Figure 13 SPI Protocol**

SPI Answers:

- during power on reset: SPI commands are ignored, SO is always low
- after power on reset: the content of the command register is transmitted with the next SPI transmission
- during watchdog reset: SPI commands are ignored, SO has the value of the status flag
- after watchdog overflow: the content of the status register is transmitted with the first SPI transmission after the low to high transition of NRO

- after a read or write command: the content of the selected register is transmitted with the next SPI transmission
- after an invalid communication: the content of the diagnosis register is transmitted with the next SPI transmission

### 8.2.1 SPI Register

**Overview**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$/W | AD1 | AD0 | | | | | | | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| AD1:AD0 | [14:13] | w | **Address Bits:**<br>$00_B$ Control Register<br>$01_B$ Diagnosis Register<br>$10_B$ Status Register |
| $\overline{R}$/W | 15 | w | **Read - Write Bit:**<br>$0_B$ Read Access<br>$1_B$ Write Access |

**CMD Register**

**Command Register (Identifier x00x xxxx xxxx xxxx$_B$)** **Reset Value: $0_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$/W | AD1 | AD0 | VR_T1 | VR_T0 | VR_L1 | VR_L0 | | | | | | | CTR5 | CTR4 | CTR2 |
| | | | rw | rw | rw | rw | | | | | | | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| CTR2 | 0 | rw | **Control Bit Channel 2:**<br>$0_B$ Channel 2 is switched off (Reset State)<br>$1_B$ Channel 2 is switched on |
| CTR4 | 1 | rw | **Control Bit Channel 4:**<br>$0_B$ Channel 4 is switched off (Reset State)<br>$1_B$ Channel 4 is switched on |
| CTR5 | 2 | rw | **Control Bit Channel 5:**<br>$0_B$ Channel 5 is switched off (Reset State)<br>$1_B$ Channel 5 is switched on |

| Field | Bits | Type | Description |
|---|---|---|---|
| VR_L1: VR_L0 | [10:9] | rw | **Load Register of VR Interface:**<br>( c.f. VR Sensor Interface Load Selection )<br>$00_B$ $R_{Load}$ = 75kΩ (Reset State)<br>$01_B$ $R_{Load}$ = 4.5kΩ<br>$10_B$ $R_{Load}$ = 2.2kΩ<br>$11_B$ $R_{Load}$ = 1.2kΩ |
| VR_T1: VR_T0 | [12:11] | rw | **Threshold Register of VR Interface:**<br>$00_B$ -50mV (Reset State)<br>$01_B$ -100mV<br>$10_B$ -500mV<br>$11_B$ -1V |

### Diag Register

**Diagnosis Register (Identifier x01x xxxx xxxx xxxx$_B$)** **Reset Value: $0_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$/W | AD1 | AD0 | CH45_OT | CH5_OC | CH5_OL | CH4_OC | CH4_OL | CH3_OT | CH3_OC | CH3_OL | CH2_OT | CH2_OC | CH1_OT | CH1_OC | CH1_OL |
| | | | r | r | r | r | r | r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| CH1_OL | 0 | r | **Open Load Diagnosis Bit of Channel 1:**<br>$0_B$ no open load in off detected (Reset State)<br>$1_B$ open load in off detected |
| CH1_OC | 1 | r | **Over Current Diagnosis Bit of Channel 1:**<br>$0_B$ no over current detected (Reset State)<br>$1_B$ over current detected |
| CH1_OT | 2 | r | **Over Temperature Diagnosis Bit of Channel 1:**<br>$0_B$ no over temperature detected (Reset State)<br>$1_B$ over temperature detected |
| CH2_OC | 3 | r | **Over Current Diagnosis Bit of Channel 2:**<br>$0_B$ no over current detected (Reset State)<br>$1_B$ over current detected |
| CH2_OT | 4 | r | **Over Temperature Diagnosis Bit of Channel 2:**<br>$0_B$ no over temperature detected (Reset State)<br>$1_B$ over temperature detected |
| CH3_OL | 5 | r | **Open Load Diagnosis Bit of Channel 3:**<br>$0_B$ no open load in off detected (Reset State)<br>$1_B$ open load in off detected |
| CH3_OC | 6 | r | **Over Current Diagnosis Bit of Channel 3:**<br>$0_B$ no over current detected (Reset State)<br>$1_B$ over current detected |

| Field | Bits | Type | Description |
|---|---|---|---|
| CH3_OT | 7 | r | **Over Temperature Diagnosis Bit of Channel 3:**<br>$0_B$ no over temperature detected (Reset State)<br>$1_B$ over temperature detected |
| CH4_OL | 8 | r | **Open Load Diagnosis Bit of Channel 4:**<br>$0_B$ no open load in off detected (Reset State)<br>$1_B$ open load in off detected |
| CH4_OC | 9 | r | **Over Current Diagnosis Bit of Channel 4:**<br>$0_B$ no over current detected (Reset State)<br>$1_B$ over current detected |
| CH5_OL | 10 | r | **Open Load Diagnosis Bit of Channel 5:**<br>$0_B$ no open load in off detected (Reset State)<br>$1_B$ open load in off detected |
| CH5_OC | 11 | r | **Over Current Diagnosis Bit of Channel 5:**<br>$0_B$ no over current detected (Reset State)<br>$1_B$ over current detected |
| CH45_OT | 12 | r | **Over Temperature Diagnosis Bit of Channel 4 and 5:**<br>$0_B$ no over temperature detected (Reset State)<br>$1_B$ over temperature detected |

### Stat Register

**Status Register (Identifier x10x xxxx xxxx xxxx$_B$)** **Reset Value: $0_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{R}$/W | AD1 | AD0 | WD_DIS | WD_TO | | | | | | | ST5 | ST4 | ST3 | ST2 | ST1 |
| | | | r | r | | | | | | | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| ST1 | 0 | r | **Status Bit Channel 1:**<br>$0_B$ Channel 1 is switched off (Reset State)<br>$1_B$ Channel 1 is switched on |
| ST2 | 1 | r | **Status Bit Channel 2:**<br>$0_B$ Channel 2 is switched off (Reset State)<br>$1_B$ Channel 2 is switched on |
| ST3 | 2 | r | **Status Bit Channel 3:**<br>$0_B$ Channel 3 is switched off (Reset State)<br>$1_B$ Channel 3 is switched on |
| ST4 | 3 | r | **Status Bit Channel 4:**<br>$0_B$ Channel 4 is switched off (Reset State)<br>$1_B$ Channel 4 is switched on |
| ST5 | 4 | r | **Status Bit Channel 5:**<br>$0_B$ Channel 5 is switched off (Reset State)<br>$1_B$ Channel 5 is switched on |

| Field | Bits | Type | Description |
|---|---|---|---|
| **WD_TO** | 11 | r | **Watchdog Time Out Bit:**<br>$0_B$ no watchdog time out<br>$1_B$ watchdog time out occurred |
| **WD_DIS** | 12 | r | **Watchdog Status Bit:**<br>$0_B$ Watchdog enabled ($V_{WD\_DIS}$ = 0V)<br>$1_B$ Watchdog disabled ($V_{WD\_DIS}$ = 5V) |

### 8.2.2 Set and Reset of Diagnosis Register Bits

Set of the over current diagnosis bits of channels 1, 3, 4 and 5:

The over current diagnosis bits of channels 1, 3, 4 and 5 are set asynchronously of the internal clock with the output signal of the detection circuit (details see Chapter 6.1).

Reset of the over current diagnosis bits of channels 1 and 3:

- Diagnosis register was read out:
  - input pin INx remains high: **no reset** of the over current diagnosis bit, the channel remains switched off
  - input pin INx transition from high to low: the over current diagnosis bit is **reset,** the channel could be switched on again
- Diagnosis register was not read out
  - channel remains **switched off and no reset** of the over current diagnosis bit is done
  - input pin INx is low: with the next read access of the diagnosis register the diagnosis bits are reset

Reset of the over current diagnosis bits of channels 4 and 5:

- Diagnosis register was not read out
  - channel remains **switched off and no reset** of the over current diagnosis bit is done
- Diagnosis register was read out:
  - SPI command register write command is not sent: **no reset** of the over current diagnosis bit, the channel remains switched off
  - SPI command register write command is sent: the over current diagnosis bit is **reset,** the channel will be switched according the status of the control bit

Set and Reset of the over current diagnosis bit of channel 2:

The over current diagnosis register bit for channel 2 is set asynchronously of the internal clock with the output signal of the detection circuit. With this signal the output is switched off and the counter for the off time $t_{oc,off}$ of the repetitive switching cycle starts. After $t_{oc,off}$ the channel will be switched on again. With an remaining over current condition the channel will be switched on repetitively. This internal overcurrent status of the channel is latched internally. The internal over current status is reset in two situations.

- over current condition exists no longer: the internal over current status is reset after the time $t_{oc,St}$
- over current condition remains and the channel is switched off: the internal over current status is reset after the time $t_{oc,off}$

The reset of the over current diagnosis register bit for channel 2 is related to the internal over current status. In Figure 14 and Figure 15 the behavior of the diagnosis with temporary and permanent over current condition is drawn.

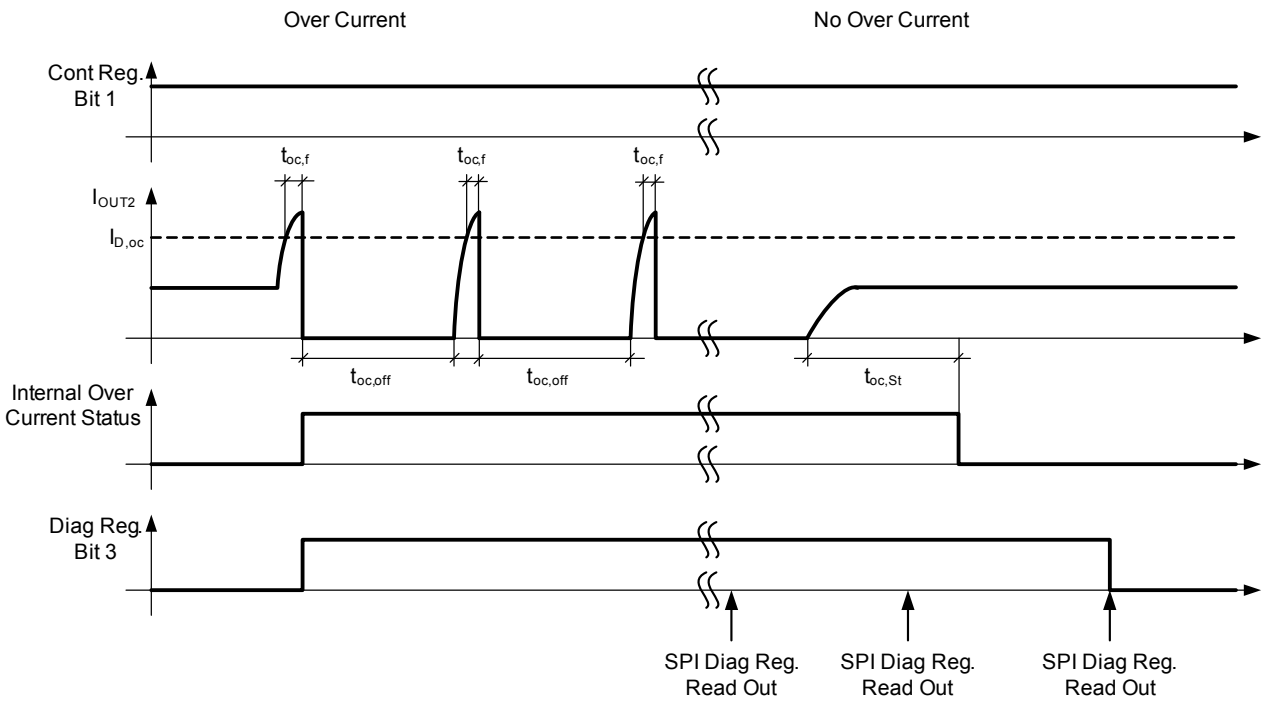



**Figure 14 Behavior of diagnosis with temporary over current condition at channel 2**

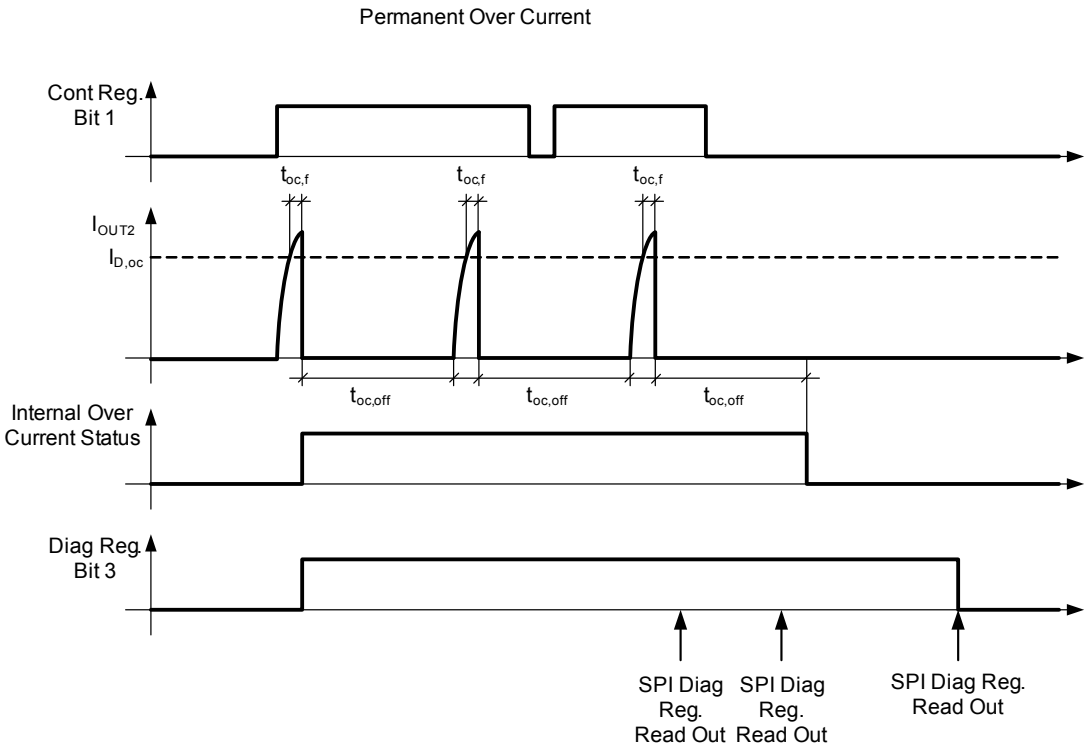



**Figure 15 Behavior if diagnosis with permanent over current condition at channel 2**

Reset of the over temperature diagnosis bits:

The over temperature diagnosis bits will be reset with read access of the diagnosis register if no over temperature condition is detected.

Reset of the open load in off diagnosis bits:

The open load in off diagnosis bits will be reset with read access of the diagnosis register if no open load condition is detected.

## 8.3 Electrical Characteristics SPI

**Table 8 Electrical Characteristics: SPI**

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input Characteristics (CSN, SCLK, SI):** | | | | | | | |
| Low Level Input Voltage | $V_{x,L}$ | – | – | 1 | V | | P_8.1.1 |
| High Level Input Voltage | $V_{x,H}$ | 2 | – | – | V | | P_8.1.2 |
| Hysteresis | $V_{x,Hys}$ | 50 | | 250 | mV | | |
| Pull Up Current CSN | $I_{x,pu}$ | -25 | -50 | -100 | µA | at $V_{IN}$ = 0V | P_8.1.3 |
| Pull Up Current CSN | $I_{x.pu}$ | -25 | – | – | µA | at $V_{IN}$ = $V_{V5DD}$ - 0.6V | P_8.1.4 |
| Pull Down Current SCLK, SI | $I_{x,pu}$ | 20 | 50 | 100 | µA | at $V_{IN}$ = $V_{V5DD}$ | P_8.1.5 |
| Pull Down Current SCLK, SI | $I_{x.pu}$ | 2.4 | – | – | µA | at $V_{IN}$ = 0.6V | P_8.1.6 |
| **Output Characteristics (SO):** | | | | | | | |
| Low Level Output Voltage | $V_{So,L}$ | – | – | 0.4 | V | $I_x$ = 100µA | P_8.2.1 |
| High Level Output Voltage | $V_{SO,H}$ | V5DD -0.4 | – | – | V | $I_x$ = -100µA | P_8.2.2 |
| Output High Impedance Leakage Current | $I_{SO,TRI}$ | -3 | – | 3 | µA | 0V < $V_{SO}$ < 5V | P_8.2.3 |
| **Timings:** | | | | | | | |
| Lead Time | $t_1$ | 210 | – | – | ns | CSN falling to SCLK rising | P_8.3.1 |
| Lag Time | $t_2$ | 75 | – | – | ns | SCLK falling to CSN rising | P_8.3.2 |
| CSN High Time | $t_3$ | 550 | – | – | ns | CSN rising to CSN falling | P_8.3.3 |
| Period of SCLK | $t_4$ | 200 | – | – | ns | | P_8.3.4 |
| SCLK to CSN Set Up Time | $t_5$ | 10 | – | – | ns | SCLK falling to CSN falling | P_8.3.5 |
| SCLK Low Time | $t_7$ | 60 | – | – | ns | | P_8.3.6 |
| CSN to SCLK Hold Time | $t_8$ | 15 | – | – | ns | CSN rising to SCLK rising | P_8.3.7 |
| SI Set Up Time | $t_9$ | 30 | – | – | ns | SI set up time to SCLK falling | P_8.3.8 |
| SI Hold Up Time | $t_{10}$ | 30 | – | – | ns | SI holdup time after SCLK falling | P_8.3.9 |
| SO Enable Time | $t_{11}$ | – | – | 165 | ns | CSN falling to SO active | P_8.3.10 |
| SO Valid Time | $t_{12}$ | – | – | 120 | ns | SO data valid after SCLK rising | P_8.3.11 |
| SO Disable Time | $t_{13}$ | – | – | 165 | ns | SO high impedance after CSN rising | P_8.3.12 |
| Number of Clock Pulses while CSN = low | | 16 | – | 16 | pulses | | P_8.3.13 |

**Table 8 Electrical Characteristics: SPI** (cont'd)

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SO Rise Time | $t_{SO\_rise}$ | – | – | 75 | ns | 20% to 80%, $C_{load}$=1.6pF | P_8.3.14 |
| SO Fall Time | $t_{SO\_fall}$ | – | – | 75 | ns | 80% to 20% $C_{load}$=1.6pF | P_8.3.15 |

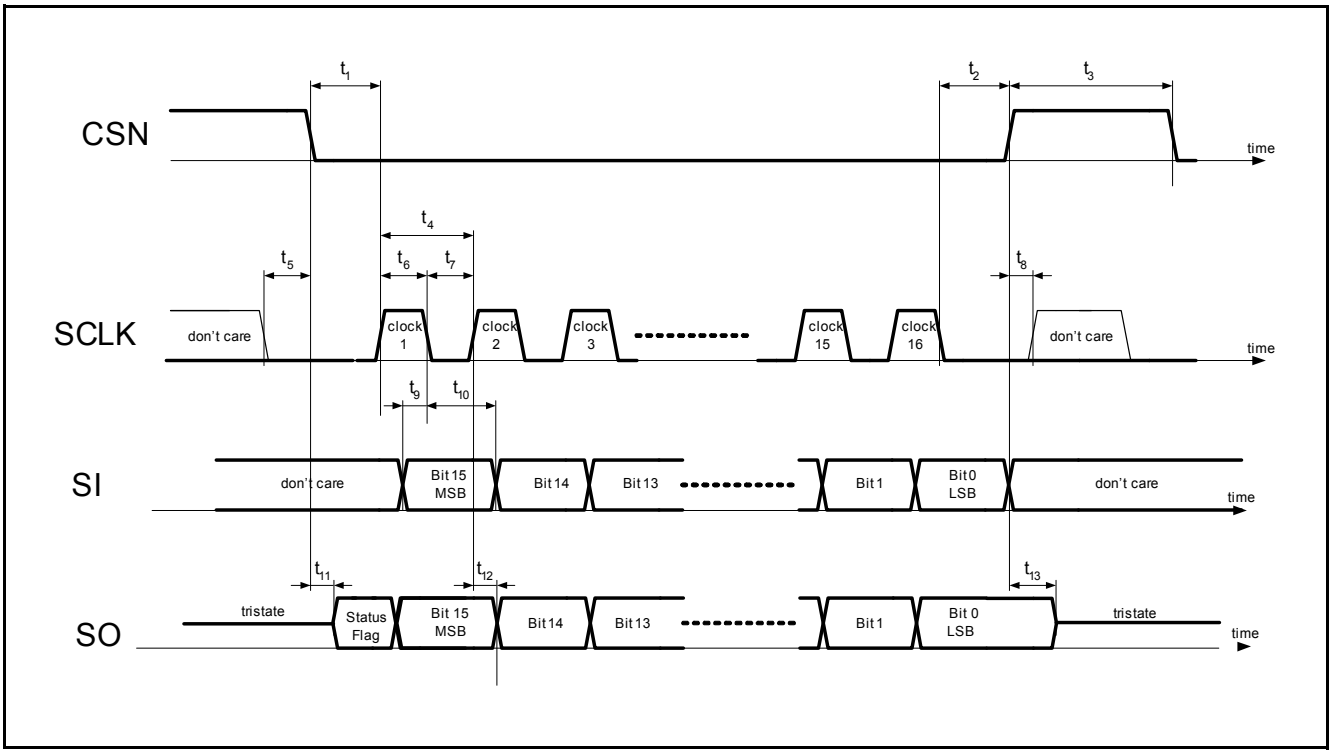



**Figure 16 SPI Timing Diagram**

# 9 K-Line

## 9.1 K-Line

The K-Line module is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing. It is designed to interface vehicles via the special ISO K-Line and meets the ISO standard 9141. The device's K-Line bus driver's output is protected against bus shorts.

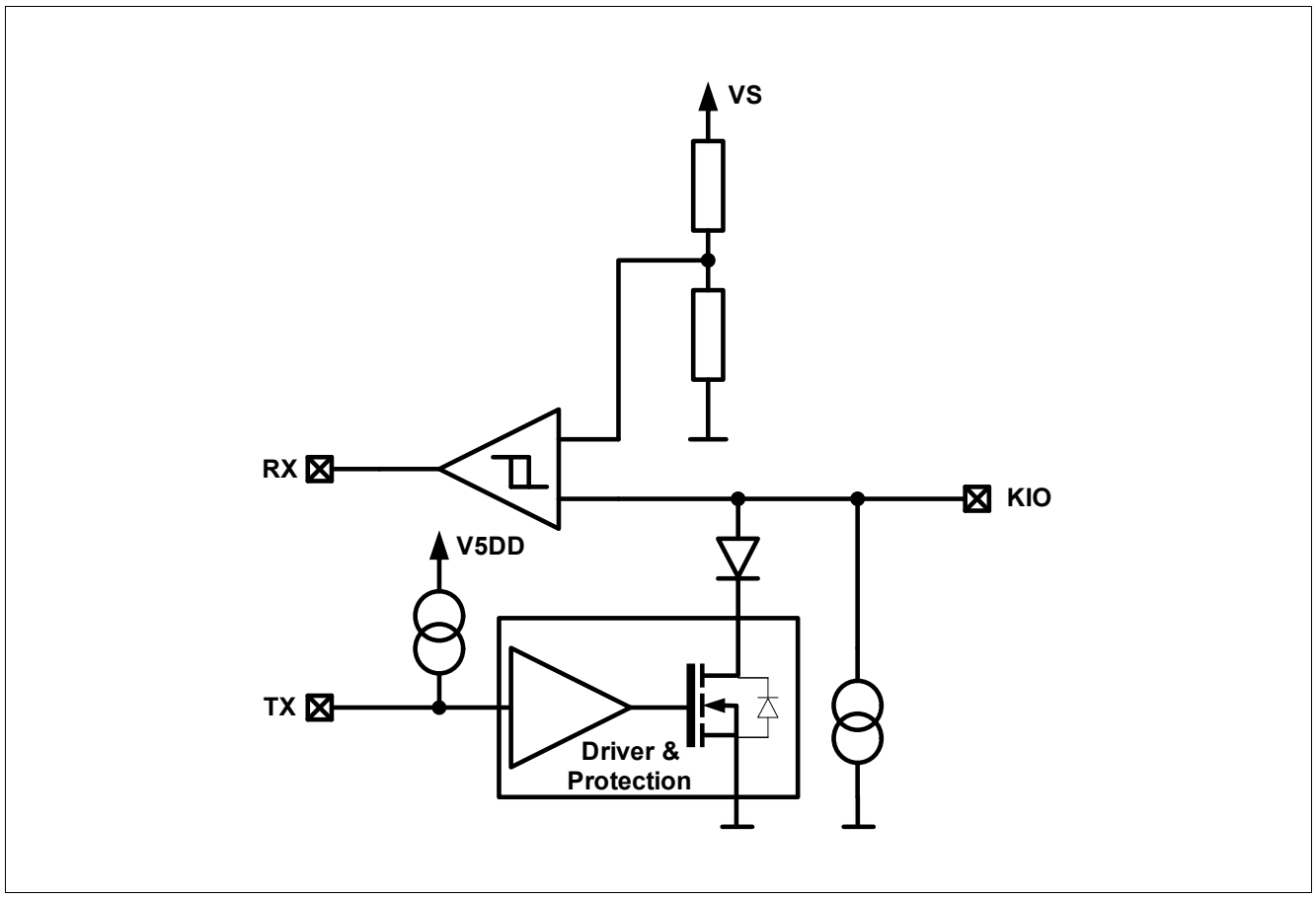



Figure 17 K-Line Block Diagram

## 9.2 Electrical Characteristics K-Line

**Table 9 Electrical Characteristics: K-Line**

$V_S$ = 13.5 V, $T_j$ = -40°C to +150°C: All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Output RX** | | | | | | | |
| Low Level Output Voltage | $V_{RX,L}$ | – | – | 0.4 | V | $I_{RX}$ = 100µA | P_9.1.1 |
| High Level Output Voltage | $V_{RX,H}$ | V5DD-0.4 | – | – | V | $I_{RX}$ = -100µA | P_9.1.2 |
| **Input TX** | | | | | | | |
| Low Level Input Voltage | $V_{TX,L}$ | – | – | 1 | V | | P_9.2.1 |
| High Level Input Voltage | $V_{TX,H}$ | 3.2 | – | – | V | | P_9.2.2 |
| Hysteresis | $V_{TX,Hys}$ | 280 | 500 | 700 | mV | | P_9.2.3 |
| Pull Up Current | $I_{PU\_L}$ | -70 | -100 | -150 | µA | at $V_{TX}$ = 0V | P_9.2.4 |
| Pull Up Current | $I_{PU\_L}$ | -30 | – | – | µA | at $V_{TX}$ = $V_{V5DD}$ - 0.6V | P_9.2.5 |
| **K-Line Bus Driver Input/Output KIO** | | | | | | | |
| Low Level Output Voltage | $V_{KIO,O,L}$ | – | – | 1.4 | V | TX = low, $R_{KIO}$= 480Ω | P_9.3.1 |
| Current Limitation | $I_{KIO(lim)}$ | 40 | – | 140 | mA | | P_9.3.2 |
| Low Level Input Voltage | $V_{KIO,I,L}$ | – | – | 0.4*VS | V | | P_9.3.3 |
| High Level Input Voltage | $V_{KIO,I,H}$ | 0.6*VS | – | – | V | | P_9.3.4 |
| Hysteresis | $V_{KIO,I,Hys}$ | 0.02 *VS | – | 0.175 *VS | V | | P_9.3.5 |
| Pull Down Current | $I_{KIO,pd}$ | 5 | 10 | 15 | µA | | P_9.3.6 |
| **Transfer Characteristics** $C_{RX}$ = 25pF; $R_{KIO}$ = 540Ω; $C_{KIO}$ ≤ 1.3nF | | | | | | | |
| Receive Frequency | $f_{KIO,rec}$ | – | – | 500 | kHz | $C_{KIO}$ = 0pF | P_9.4.1 |
| Transmit Frequency | $f_{KIO,tran}$ | – | – | 100 | kHz | | P_9.4.2 |
| Delay Time KIO -> RX rising edge[1)] | $t_{drR}$ | 0.05 | – | 0.5 | µs | $C_{RX,load}$ = 1.6pF | P_9.4.3 |
| Delay Time KIO -> RX falling edge[1)] | $t_{dfR}$ | 0.05 | – | 0.5 | µs | $C_{RX,load}$ = 1.6pF | P_9.4.4 |
| Delay Time TX -> KIO rising edge[1)2)] | $t_{drT}$ | 0.05 | – | 0.5 | µs | $C_{KIO,load}$ = 1.6pF | P_9.4.5 |
| Delay Time TX -> KIO falling edge[1)] | $t_{dfT}$ | 0.05 | – | 0.5 | µs | $C_{KIO,load}$ = 1.6pF | P_9.4.6 |

1) For definition see Figure 18.

2) Not subject of production test, behavior defined by external devices.

## K-Line

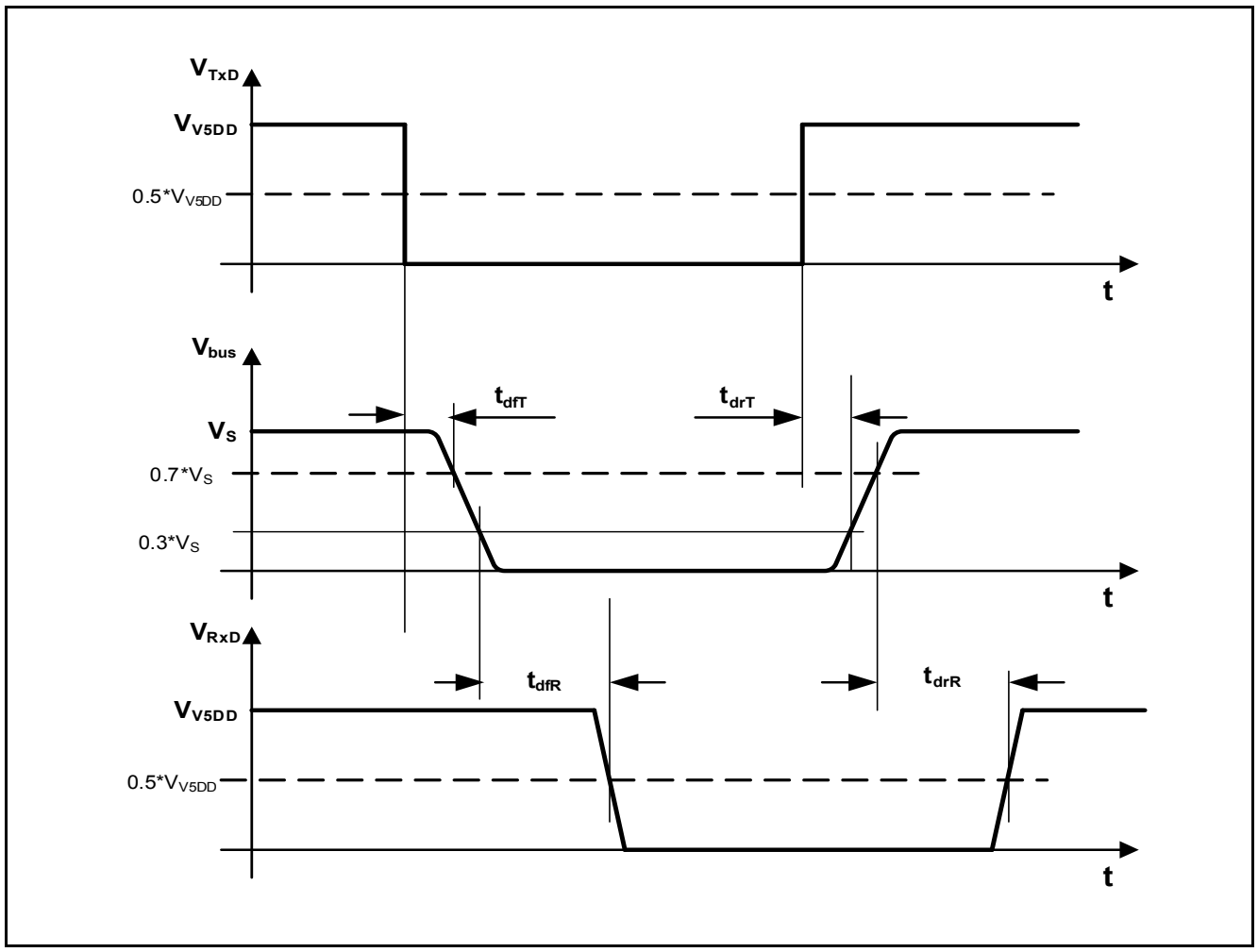



Figure 18 K-Line Transfer Characteristics

# 10 Package Outlines

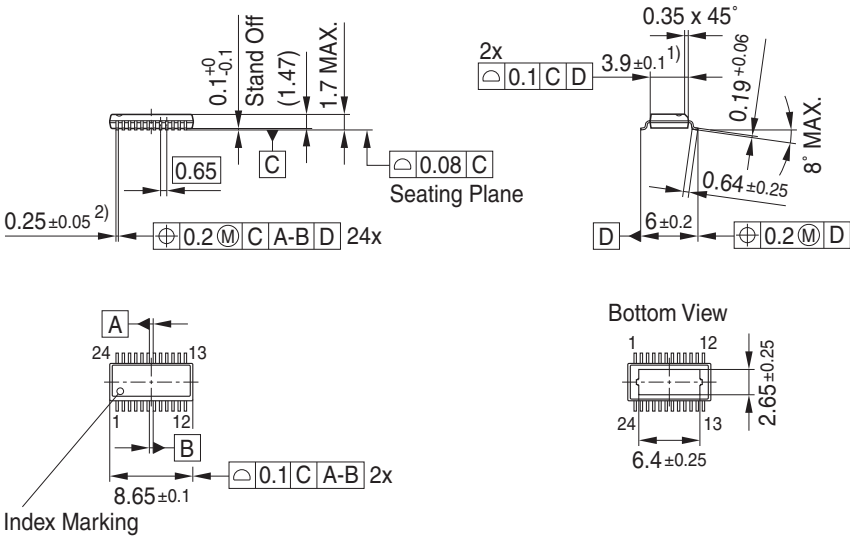



**Figure 19 PG-SSOP24**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products, and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
**http://www.infineon.com/packages**.

Dimensions in mm

# 11 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2012-09-12 | Data Sheet. |
| 1.1 | 2012-12-19 | Parameter “Reset Reaction Time” on Page 12 increased. |
| 1.2 | 2016-10-26 | Added variant TLE8080-3EM. |
| | | Parameter “Low Drop Voltage” on Page 11 is spilt in P_5.1.10 a and P_5.1.10 b. |
| | | Removed “50%” indicator for VCSN signals in Figure 7, Figure 8, Figure 9 and Figure 10. |
| | | Removed pin “KIO” from P_4.1.5 in Table 1 as covered by P_4.1.8. |
| | | Added “after a Diagnosis Read has been performed” to description of channel 4 and 5 over current status reset behavior. |
| | | Editorial changes. |

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