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FDMS8090

PowerTrench® Symmetrical Dual 100 V N-Channel MOSFET

Features

- Max $r_{DS(on)}$ = 13 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $r_{DS(on)}$ = 20 mΩ at $V_{GS} = 6$ V, $I_D = 8$ A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- 100% UIL tested
- RoHS Compliant

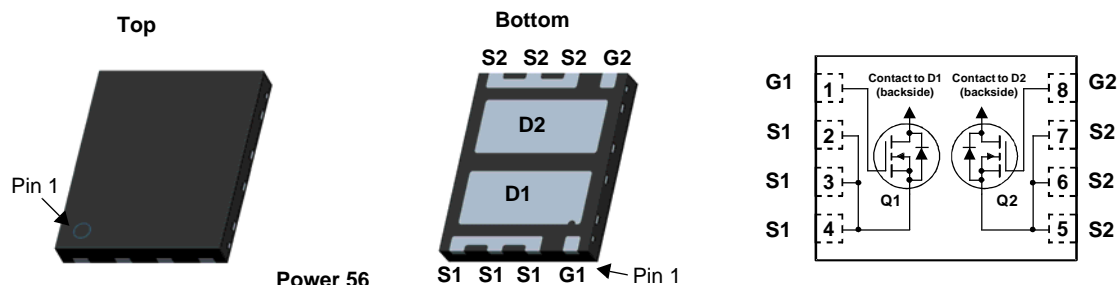


General Description

This device includes two fast switching (Qgd minimized) 100V N-Channel MOSFETs in a dual Power 56 (5 mm X 6 mm MLP) package. The package is enhanced for exceptional thermal performance.

Applications

- Bridge Topologies
- Synchronous Rectifier Pair
- Motor Drives



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous $T_C = 25$ °C	40	A
	-Continuous $T_A = 25$ °C (Note 1a)	10	
	-Pulsed (Note 4)	120	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	253	mJ
P_D	Power Dissipation $T_C = 25$ °C	59	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8090	FDMS8090	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		70		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$		11	13	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 8\ \text{A}$		15	20	
		$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$, $T_J = 125^\circ\text{C}$		18	20	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 10\ \text{A}$		24		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		1285	1800	pF
C_{oss}	Output Capacitance			301	400	pF
C_{rss}	Reverse Transfer Capacitance			16	28	pF
R_g	Gate Resistance		0.1	1.7	3.5	Ω

Switching Characteristics

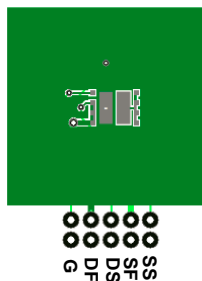
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		10.6	21	ns
t_r	Rise Time			4.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17.4	31	ns
t_f	Fall Time			4	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V}$, $I_D = 10\ \text{A}$	19	27	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		10	15	nC
Q_{gs}	Gate to Source Charge			6.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.1		nC

Drain-Source Diode Characteristics

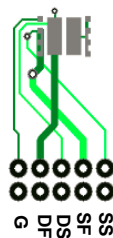
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2\ \text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\ \text{V}$, $I_S = 10\ \text{A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 10\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		49	78	ns
Q_{rr}	Reverse Recovery Charge			54	86	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. $138^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
3. E_{AS} of 253 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\ \text{mH}$, $I_{AS} = 13\ \text{A}$, $V_{DD} = 100\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% test at $L = 0.3\ \text{mH}$, $I_{AS} = 29\ \text{A}$.
4. Pulsed I_D limited by junction temperature, $t_d \leq 10\ \mu\text{s}$. Please refer to SOA curve for more details.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

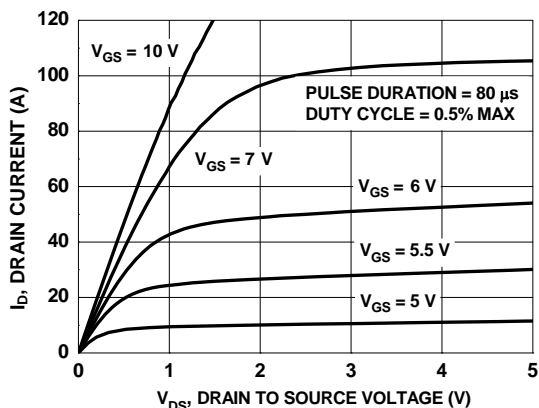


Figure 1. On Region Characteristics

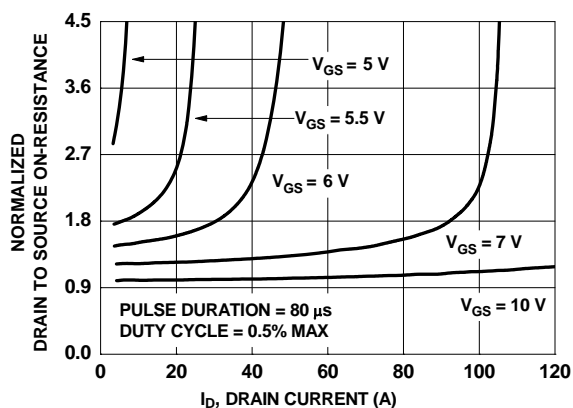


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

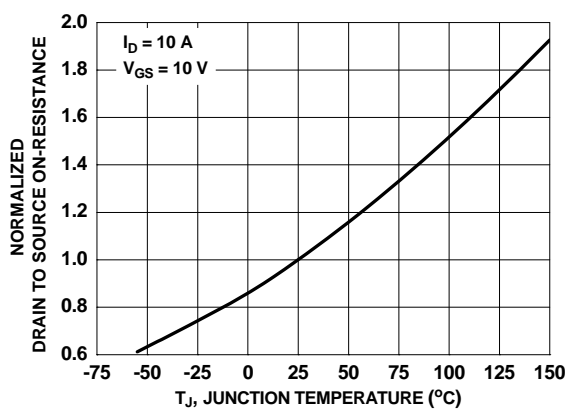


Figure 3. Normalized On Resistance vs Junction Temperature

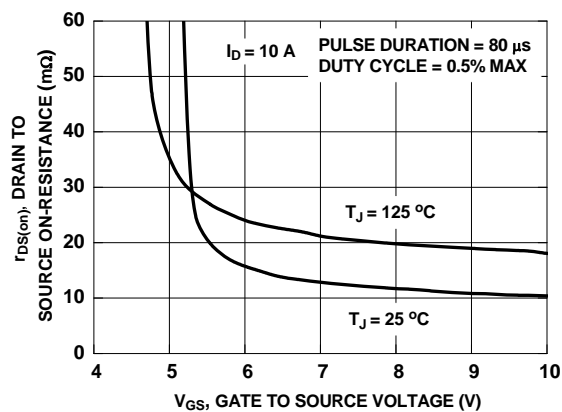


Figure 4. On-Resistance vs Gate to Source Voltage

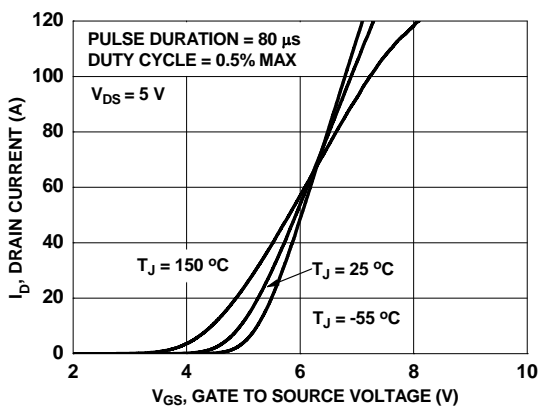


Figure 5. Transfer Characteristics

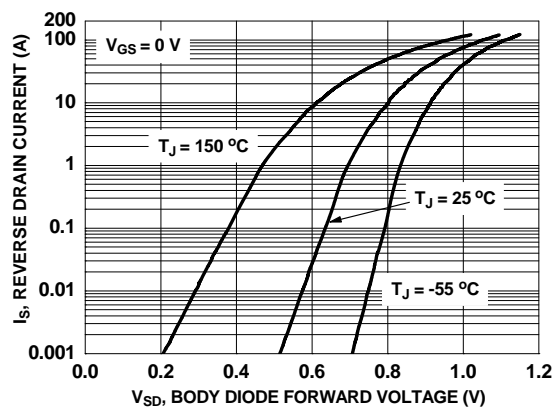


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

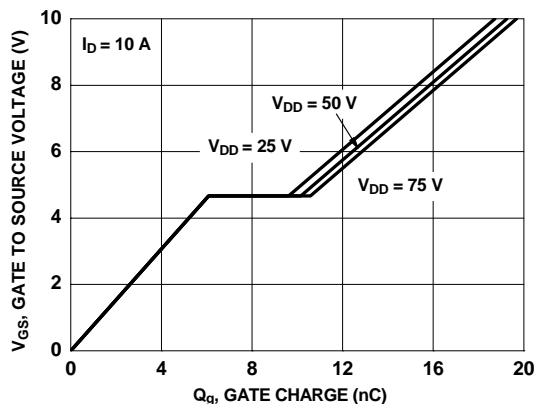


Figure 7. Gate Charge Characteristics

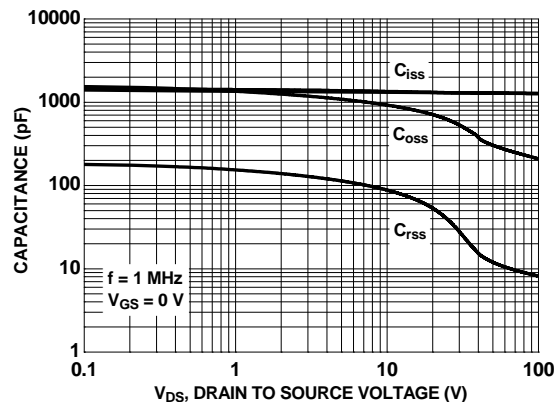


Figure 8. Capacitance vs Drain to Source Voltage

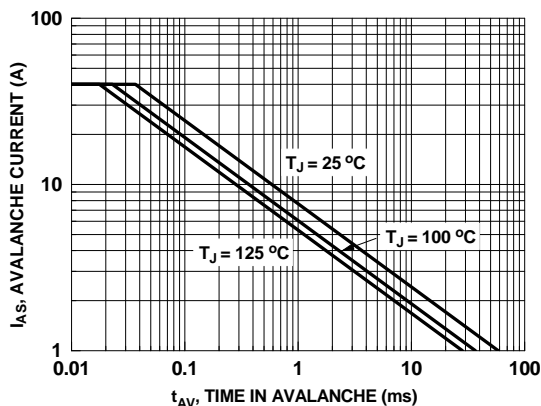


Figure 9. Unclamped Inductive Switching Capability

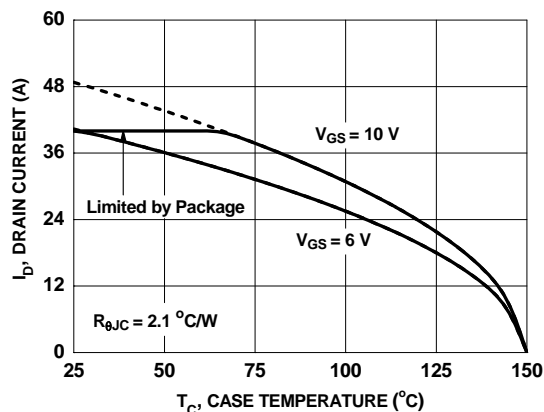


Figure 10. Maximum Continuous Drain Current vs Case Temperature

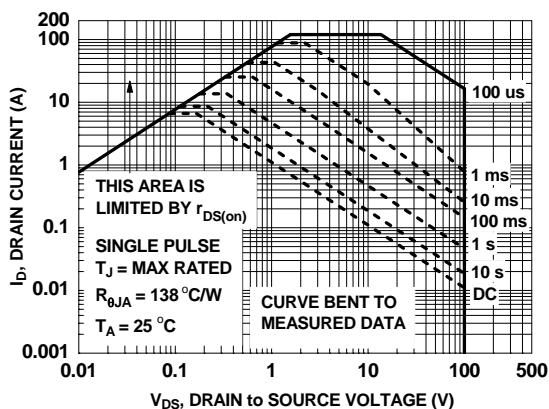


Figure 11. Forward Bias Safe Operating Area

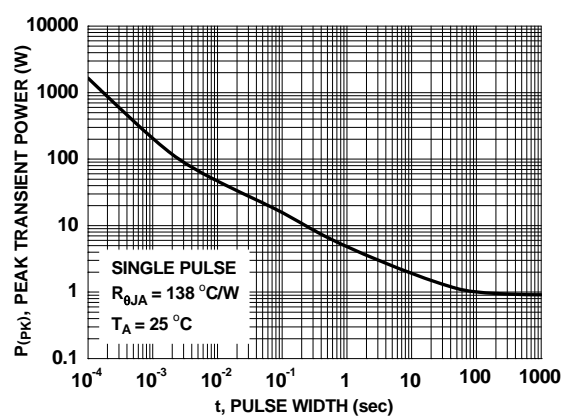
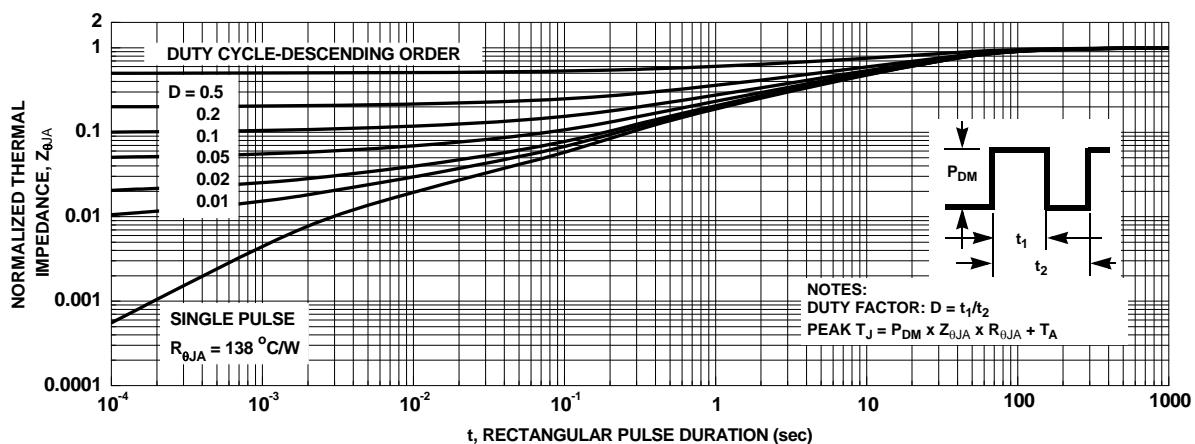
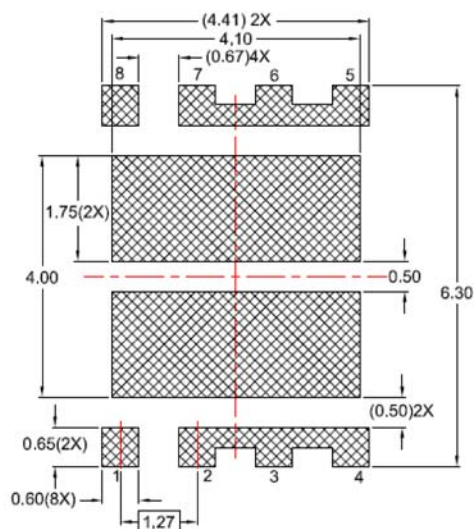


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted







RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- E. DRAWING FILENAME: MKT-MLP08Zrev1.

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