

# MC74HCT374A

## Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT374A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT374A is identical in pinout to the LS374.

Data meeting the setup and hold time is clocked to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT374A is identical in function to the HCT574A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT534A, which has inverting outputs.

#### Features

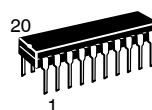
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 276 FETs or 69 Equivalent Gates
- Improvements over HCT374
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity
- These Devices are Pb-Free and are RoHS Compliant



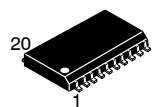
ON Semiconductor®

<http://onsemi.com>

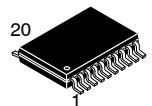
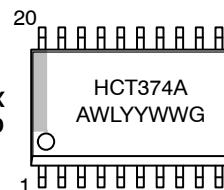
#### MARKING DIAGRAMS



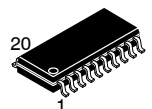
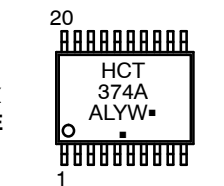
PDIP-20  
N SUFFIX  
CASE 738



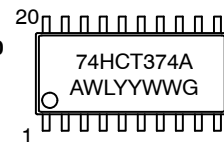
SOIC-20  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E



SOEIAJ-20  
F SUFFIX  
CASE 967



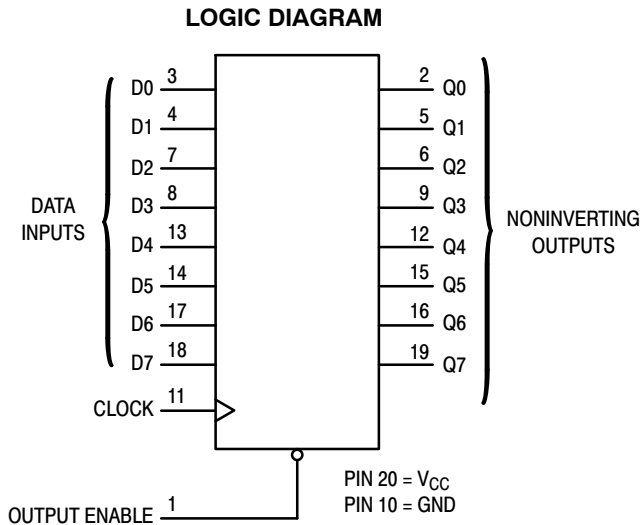
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HCT374A



**PIN ASSIGNMENT**

|               |     |    |                 |
|---------------|-----|----|-----------------|
| OUTPUT ENABLE | 1 ● | 20 | V <sub>CC</sub> |
| Q0            | 2   | 19 | Q7              |
| D0            | 3   | 18 | D7              |
| D1            | 4   | 17 | D6              |
| Q1            | 5   | 16 | Q6              |
| Q2            | 6   | 15 | Q5              |
| D2            | 7   | 14 | D5              |
| D3            | 8   | 13 | D4              |
| Q3            | 9   | 12 | Q4              |
| GND           | 10  | 11 | CLOCK           |

**FUNCTION TABLE**

| Output Enable | Inputs |   | Output    |
|---------------|--------|---|-----------|
|               | Clock  | D | Q         |
| L             |        | H | H         |
| L             |        | L | L         |
| L             | L, H,  | X | No Change |
| H             | X      | X | Z         |

X = don't care  
Z = high impedance

| Design Criteria                 | Value | Units |
|---------------------------------|-------|-------|
| Internal Gate Count*            | 69    | ea.   |
| Internal Gate Propagation Delay | 1.5   | ns    |
| Internal Gate Power Dissipation | 5.0   | μW    |
| Speed Power Product             | .0075 | pJ    |

\*Equivalent to a two-input NAND gate.

## ORDERING INFORMATION

| Device           | Package                | Shipping†         |
|------------------|------------------------|-------------------|
| MC74HCT374ANG    | PDIP-20<br>(Pb-Free)   | 1440 Units / Box  |
| MC74HCT374ADWG   | SOIC-20<br>(Pb-Free)   | 38 Units / Rail   |
| MC74HCT374ADWR2G | SOIC-20<br>(Pb-Free)   | 1000 Units / Reel |
| MC74HCT374ADTR2G | TSSOP-20*              | 2500 Units / Reel |
| MC74HCT374AFELG  | SOEIAJ-20<br>(Pb-Free) | 2000 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HCT374A

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin   | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin  | $\pm 35$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins  | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†            | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC, SSOP or TSSOP Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time (Figure 1)                  | 0    | 500      | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions   | $V_{CC}$<br>V | Guaranteed Limit |               |         | Unit |
|-----------------|--|---|---------------|------------------|---------------|---------|------|
|                 |  |   |               | - 55 to<br>25°C  | ≤ 85°C        | ≤ 125°C |      |
| $V_{IH}$        | Minimum High-Level Input Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 4.5           | 2.0              | 2.0           | 2.0     | V    |
|                 |  |   | 5.5           | 2.0              | 2.0           | 2.0     |      |
| $V_{IL}$        | Maximum Low-Level Input Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 4.5           | 0.8              | 0.8           | 0.8     | V    |
|                 |  |   | 5.5           | 0.8              | 0.8           | 0.8     |      |
| $V_{OH}$        | Minimum High-Level Output Voltage              | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 4.5           | 4.4              | 4.4           | 4.4     | V    |
|                 |  |   | 5.5           | 5.4              | 5.4           | 5.4     |      |
| $V_{OL}$        | Maximum Low-Level Output Voltage               | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 6.0 \text{ mA}$   | 4.5           | 3.98             | 3.84          | 3.7     | V    |
|                 |  |   | 5.5           | 0.1              | 0.1           | 0.1     |      |
| $I_{in}$        | Maximum Input Leakage Current                  | $V_{in} = V_{CC} \text{ or } GND$   | 4.5           | 0.1              | 0.1           | 0.1     | μA   |
|                 |  |   | 5.5           | 0.1              | 0.1           | 0.1     |      |
| $I_{OZ}$        | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>$V_{in} = V_{IL} \text{ or } V_{IH}$<br>$V_{out} = V_{CC} \text{ or } GND$                    | 4.5           | ± 0.1            | ± 1.0         | ± 1.0   | μA   |
|                 |  |   | 5.5           | ± 0.5            | ± 5.0         | ± 10    |      |
| $I_{CC}$        | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or } GND$<br>$I_{out} = 0 \mu\text{A}$  | 4.5           | 4.0              | 40            | 160     | μA   |
|                 |  |   | 5.5           | 4.0              | 40            | 160     |      |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current            | $V_{in} = 2.4 \text{ V, Any One Input}$<br>$V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$<br>$I_{out} = 0 \mu\text{A}$ | 5.5           | ≥ -55°C          | 25°C to 125°C |         | mA   |
|                 |  |   |               | 2.9              | 2.4           |         |      |

1. Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

| Symbol                   | Parameter  | Guaranteed Limit |        |         | Unit |
|--------------------------|--|------------------|--------|---------|------|
|                          |  | - 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| $f_{\max}$               | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 4)              | 30               | 24     | 20      | MHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Clock to Q<br>(Figures 1 and 4)                 | 31               | 39     | 47      | ns   |
| $t_{PLZ}$ ,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Q<br>(Figures 2 and 5)         | 30               | 38     | 45      | ns   |
| $t_{PZL}$ ,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to Q<br>(Figures 2 and 5)         | 30               | 38     | 45      | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 4)            | 12               | 15     | 18      | ns   |
| $C_{in}$                 | Maximum Input Capacitance  | 10               | 10     | 10      | pF   |
| $C_{out}$                | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | 15               | 15     | 15      | pF   |

| Symbol   | Parameter                                      | Typical @ 25°C, $V_{CC} = 5.0\text{ V}$ |  |  | Unit |
|----------|--|---|--|--|------|
|          |  | 65                                      |  |  |      |
| $C_{PD}$ | Power Dissipation Capacitance (Per Flip-Flop)* |   |  |  | pF   |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## TIMING REQUIREMENTS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , Input $t_r = t_f = 6.0\text{ ns}$ )

| Symbol        | Parameter                                       | Guaranteed Limit |        |         | Unit |
|---------------|---|------------------|--------|---------|------|
|               |   | - 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| $t_{su}$      | Minimum Setup Time, Data to Clock<br>(Figure 3) | 12               | 15     | 18      | ns   |
| $t_h$         | Minimum Hold Time, Clock to Data<br>(Figure 3)  | 5.0              | 5.0    | 5.0     | ns   |
| $t_w$         | Minimum Pulse Width, Clock<br>(Figure 1)        | 12               | 15     | 18      | ns   |
| $t_r$ , $t_f$ | Maximum Input Rise and Fall Times<br>(Figure 1) | 500              | 500    | 500     | ns   |

# MC74HCT374A

## SWITCHING WAVEFORMS

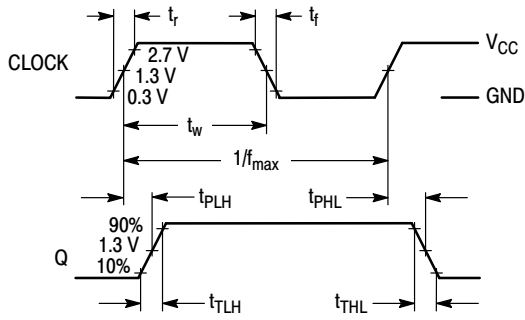


Figure 1.

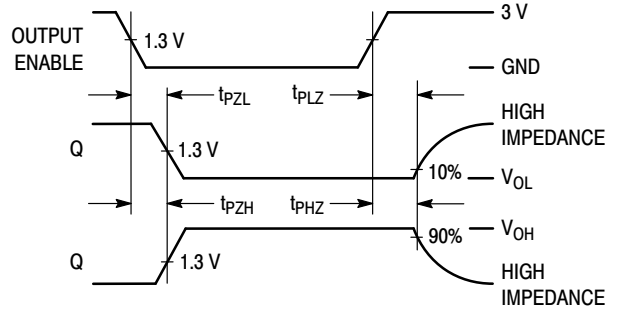


Figure 2.

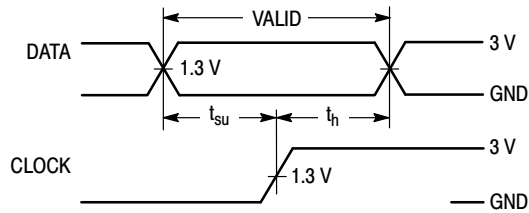
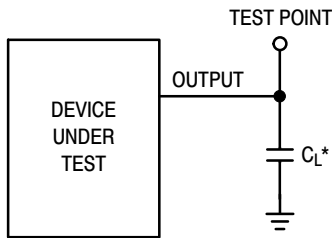


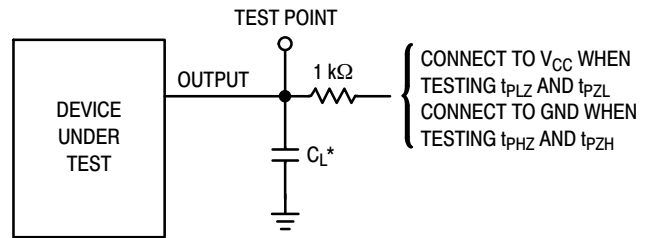
Figure 3.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

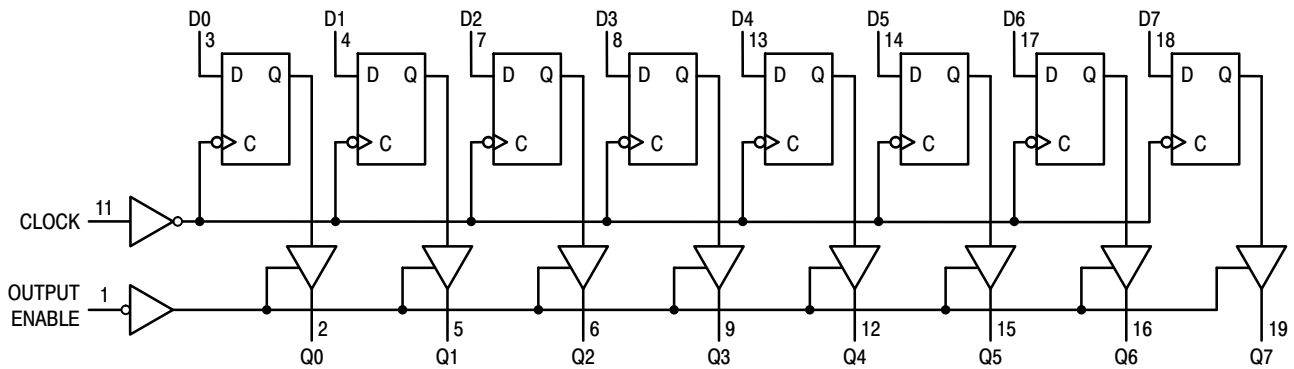
Figure 4.



\*Includes all probe and jig capacitance

Figure 5.

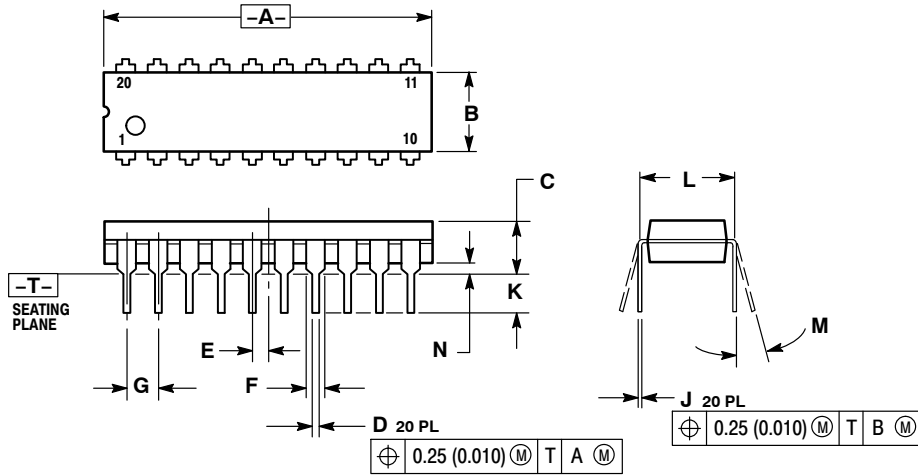
## EXPANDED LOGIC DIAGRAM



# MC74HCT374A

## PACKAGE DIMENSIONS

PDIP-20  
N SUFFIX  
CASE 738-03  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-20  
DW SUFFIX  
CASE 751D-05  
ISSUE G



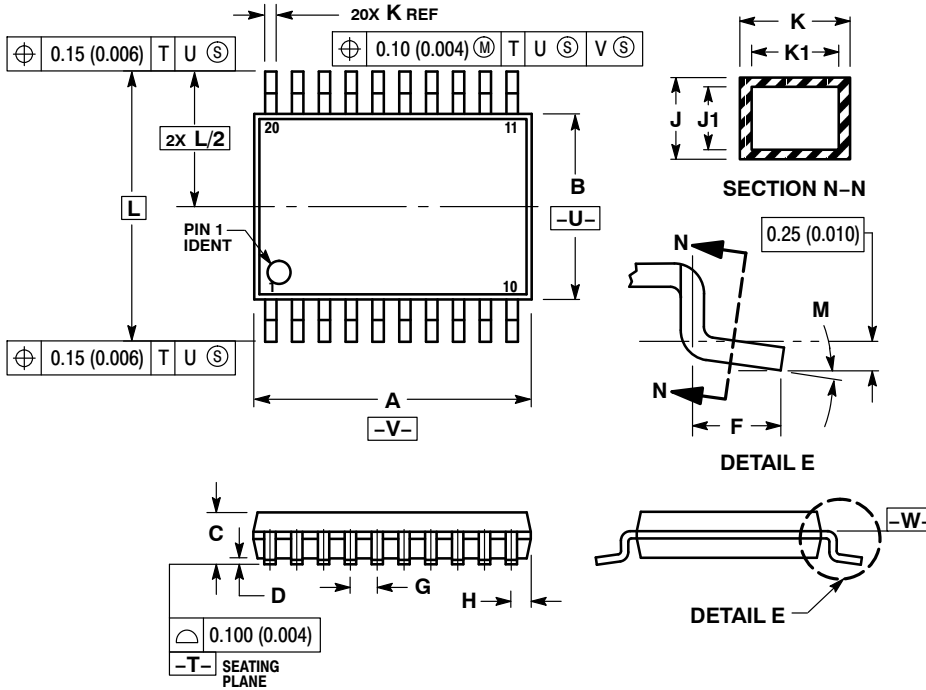
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM   | MILLIMETERS |       |
|-------|-------------|-------|
|       | MIN         | MAX   |
| A     | 2.35        | 2.65  |
| A1    | 0.10        | 0.25  |
| B     | 0.35        | 0.49  |
| C     | 0.23        | 0.32  |
| D     | 12.65       | 12.95 |
| E     | 7.40        | 7.60  |
| e     | 1.27 BSC    |       |
| H     | 10.05       | 10.55 |
| h     | 0.25        | 0.75  |
| L     | 0.50        | 0.90  |
| theta | 0°          | 7°    |

# MC74HCT374A

## PACKAGE DIMENSIONS

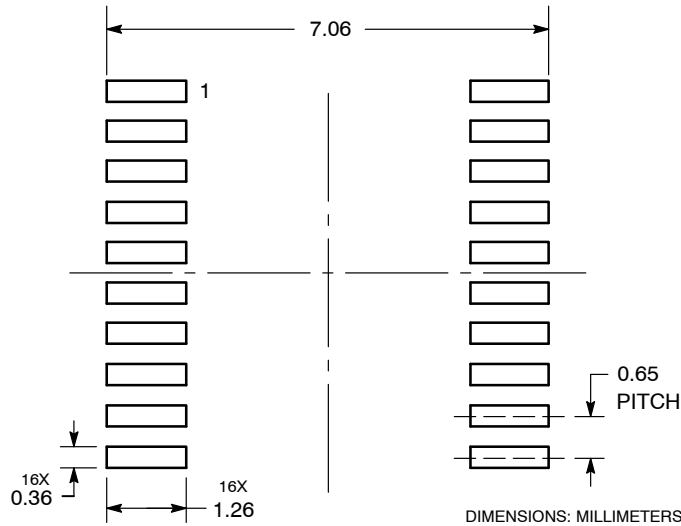
TSSOP-20  
DT SUFFIX  
CASE 948E-02  
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

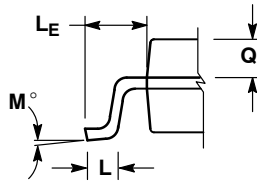
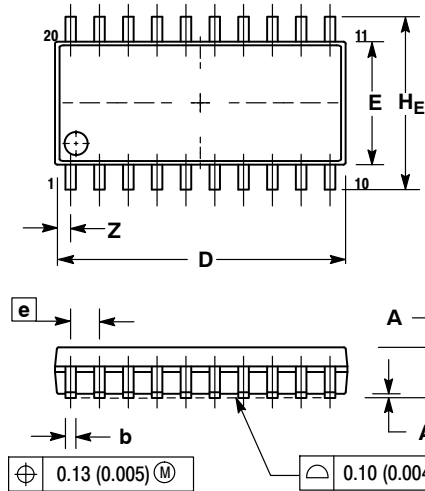
## SOLDERING FOOTPRINT



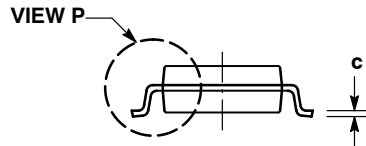
# MC74HCT374A

## PACKAGE DIMENSIONS

SOEIAJ-20  
F SUFFIX  
CASE 967-01  
ISSUE A



DETAIL P



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.15        | 0.25  | 0.006     | 0.010 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

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