2.7 V to 5.5 V, Serial-Input, Voltage-Output, 14-Bit DACs

AD5551/AD5552

FEATURES

Full 14-bit performance
3 V and 5 V single supply operation
Low 0.625 mW power dissipation
1 µs settling time
Unbuffered voltage output capable of driving 60 kΩ loads directly
SPI/QSPI/MICROWIRE-compatible interface standards
Power-on reset clears DAC output to 0 V (unipolar mode)
5 kV HBM ESD classification

APPLICATIONS

Digital gain and offset adjustment
Automatic test equipment
Data acquisition systems
Industrial process control

GENERAL DESCRIPTION

The AD5551/AD5552 are single, 14-bit, serial-input, voltage-output DACs that operate from a single 2.7 V to 5.5 V supply. The DAC output range extends from 0 V to V_{REF}.

These DACs provide 14-bit performance without any adjustments. The DAC output is unbuffered, which reduces power consumption and offset errors contributed by an output buffer.

With an external op amp, the AD5552 can be operated in bipolar mode generating a $\pm V_{REF}$ output swing. The AD5552 also includes Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity. For higher precision applications, refer to 16-bit DACs AD5541, AD5542, and AD5544.

The AD5551/AD5552 utilize a versatile 3-wire interface that is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards. The AD5551 and AD5552 are available in 8-lead and 14-lead SOIC packages.

FUNCTIONAL BLOCK DIAGRAMS

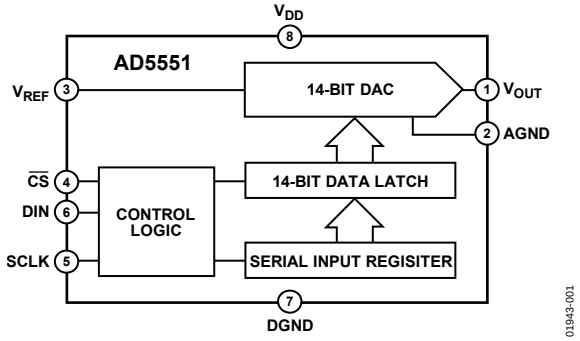

Figure 1.

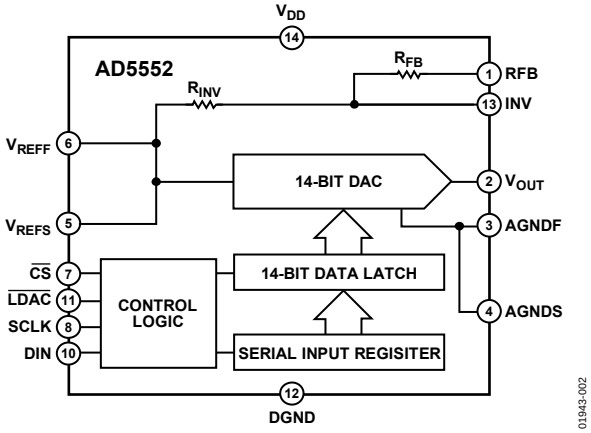

Figure 2.

PRODUCT HIGHLIGHTS

1. Single Supply Operation.
   The AD5551 and AD5552 are fully specified and guaranteed for a single 2.7 V to 5.5 V supply.
2. Low Power Consumption.
   Typically 0.625 mW with a 5 V supply.
3. 3-Wire Serial Interface.
4. Unbuffered output capable of driving 60 kΩ loads, which reduces power consumption as there is no internal buffer to drive.
5. Power-On Reset Circuitry.

Rev. A
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REVISION HISTORY

5/10—Rev. 0 to Rev. A

Updated Format ... Universal
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Changes to Pin V_{DD} Description in Table 4 and Table 5 ... 6
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7/00—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V. All specifications T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
Resolution	14			Bits	
Relative Accuracy, INL		±0.15	±1.0	LSB	B grade
Differential Nonlinearity		±0.15	±0.8	LSB	Guaranteed monotonic
Gain Error	−1.5	−0.3	+0.5	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Zero-Code Error		0.1	±1	LSB	
Zero-Code Temperature Coefficient		±0.05		ppm/°C	
AD5552					
Bipolar Resistor Matching		1.000		Ω/Ω	RFB/RINV, typically RFB = RINV = 28 kΩ
		±0.0015	±0.0152	%	Ratio error
Bipolar Zero Offset Error		±0.25	±1	LSB	
Bipolar Zero Temperature Coefficient		±0.2		ppm/°C	
Bipolar Zero-Code Error		−0.3	±1.2	LSB	
Bipolar Gain Error		−0.3	±1.2	LSB	
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	0		V_{REF} − 1 LSB	V	Unipolar operation
	$-V_{REF}$		V_{REF} − 1 LSB	V	AD5552 bipolar operation
Output Voltage Settling Time		1		µs	To ½ LSB of FS, C_L = 10 pF
Slew Rate		17		V/µs	C_L = 10 pF, measured from 0% to 63%
Digital-to-Analog Glitch Impulse		1.1		nV-sec	1 LSB change around the major carry
Digital Feedthrough		0.2		nV-sec	All 1s loaded to DAC, V_{REF} = 2.5 V
DAC Output Impedance		6.25		kΩ	Tolerance typically 20%
Power Supply Rejection Ratio			±1.0	LSB	ΔV_{DD} ± 10%
DAC REFERENCE INPUT					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[3]	9			kΩ	Unipolar operation
	7.5			kΩ	AD5552, bipolar operation
LOGIC INPUTS					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.4			V	
Input Capacitance[2]			10	pF	
Hysteresis Voltage[2]		0.15		V	
REFERENCE[2]					
Reference −3 dB Bandwidth		2.2		MHz	All 1s loaded
Reference Feedthrough		1		mV p-p	All 0s loaded, V_{REF} = 1 V p-p at 100 kHz
Signal-to-Noise Ratio		92		dB	
Reference Input Capacitance		26		pF	Code 0000_H
		26		pF	Code $3FFF_H$
POWER REQUIREMENTS					Digital inputs at rails
V_{DD}	2.7		5.5	V	
I_{DD}		125	150	µA	
Power Dissipation		0.625	0.825	mW	

[1] Temperature range is as follows: B version: −40°C to +85°C;
[2] Guaranteed by design, not subject to production test.
[3] Reference input resistance is code-dependent, minimum at 2555_H.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ 5.5 V, AGND = DGND = 0 V. All specifications −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} All Versions	Unit	Description
f_{SCLK}	25	MHz max	SCLK cycle frequency
t_1	40	ns min	SCLK cycle time
t_2	20	ns min	SCLK high time
t_3	20	ns min	SCLK low time
t_4	15	ns min	$\overline{CS}$ low to SCLK high setup
t_5	15	ns min	$\overline{CS}$ high to SCLK high setup
t_6	35	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	20	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	15	ns min	Data setup time
t_9	0	ns min	Data hold time
t_{10}	30	ns min	$\overline{LDAC}$ pulse width
t_{11}	30	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	30	ns min	$\overline{CS}$ high time between active periods

[1] Guaranteed by design, not production tested.
[2] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of +3 V and timed from a voltage level of +1.6 V).

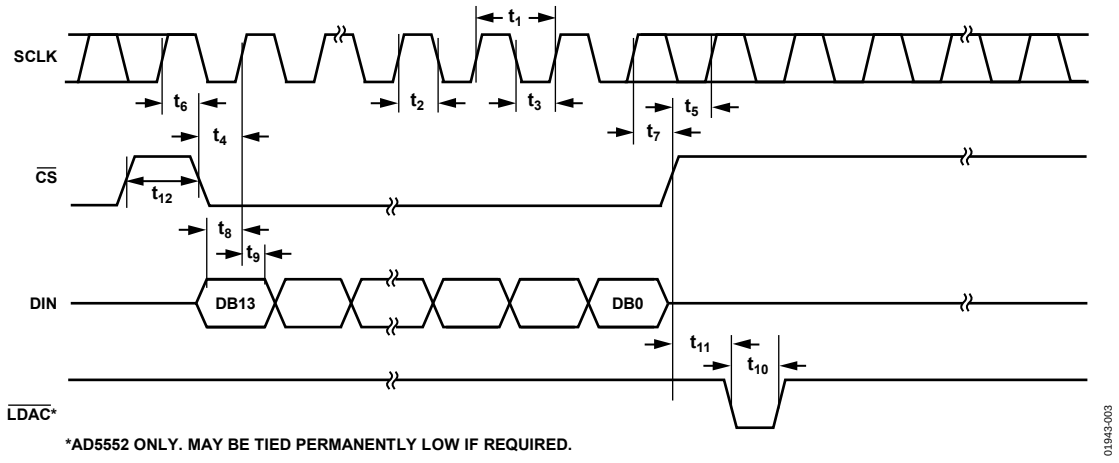


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND, AGNDF, AGNDS to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature, (T_J max)	150°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Impedance	θ_{JA}
SOIC (R-8)	149.5°C/W
SOIC (R-14)	104.5°C/W
Lead Temperature, Soldering	
Peak Temperature[1]	260°C
ESD[2]	5 kV

[1] As per JEDEC Standard 20.
[2] HBM classification.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

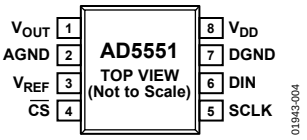


Figure 4. AD5551 Pin Configuration

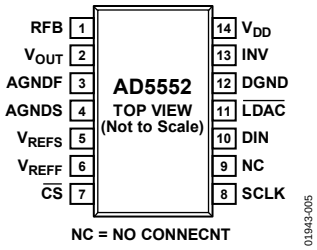


Figure 5. AD5552 Pin Configuration

Table 4. AD5551 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Analog Output Voltage from the DAC.
2	AGND	Ground Reference Point for Analog Circuitry.
3	V_{REF}	This is the voltage reference input for the DAC. Connect to external reference ranges from 2 V to V_{DD}.
4	$\overline{CS}$	This is an active low-logic input signal. The chip select signal is used to frame the serial data input.
5	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
6	DIN	Serial Data Input. This device accepts 14-bit words. Data is clocked into the input register on the rising edge of SCLK.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{DD}	Analog Supply Voltage, 2.7 V to 5.5 V ± 10%.

Table 5. AD5552 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFB	Feedback Resistor. In bipolar mode, connect this pin to external op amp output.
2	V_{OUT}	Analog Output Voltage from the DAC.
3	AGNDF	Ground Reference Point for Analog Circuitry (Force).
4	AGNDS	Ground Reference Point for Analog Circuitry (Sense).
5	V_{REFS}	This is the voltage reference input (sense) for the DAC. Connect to external reference ranges from 2 V to V_{DD}.
6	V_{REFF}	This is the voltage reference input (force) for the DAC. Connect to external reference ranges from 2 V to V_{DD}.
7	$\overline{CS}$	This is an active low-logic input signal. The chip select signal is used to frame the serial data input.
8	SCLK	Clock input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
9	NC	No Connect.
10	DIN	Serial Data Input. This device accepts 14-bit words. Data is clocked into the input register on the rising edge of SCLK.
11	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	INV	Connected to the internal scaling resistors of the DAC. Connect the INV pin to external op amps inverting input in bipolar mode.
14	V_{DD}	Analog Supply Voltage, 2.7 V to 5.5 V ± 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

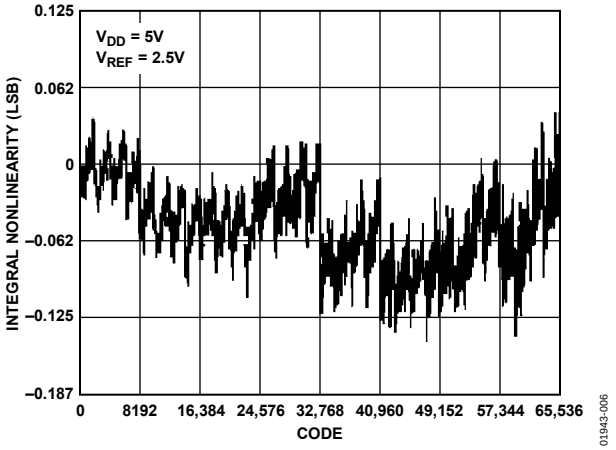


Figure 6. Integral Nonlinearity vs. Code

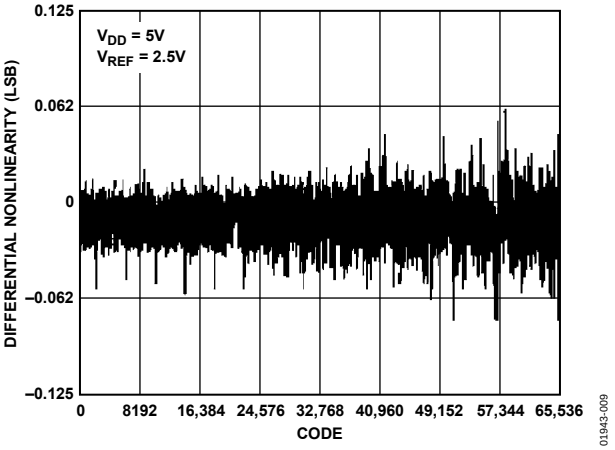


Figure 9. Differential Nonlinearity vs. Code

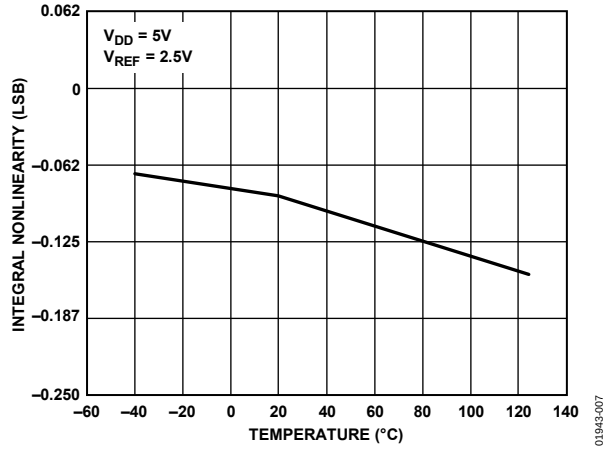


Figure 7. Integral Nonlinearity vs. Temperature

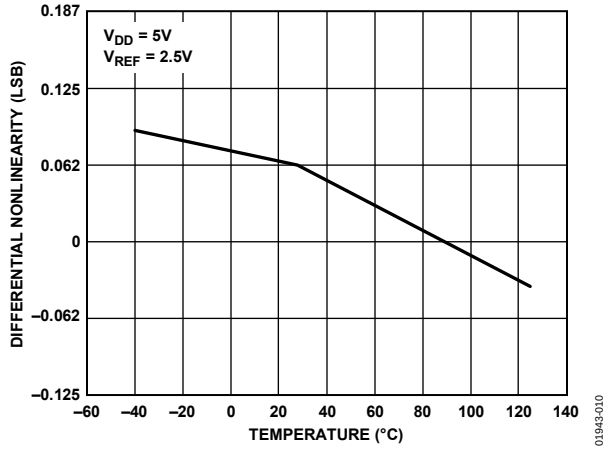


Figure 10. Differential Nonlinearity vs. Temperature

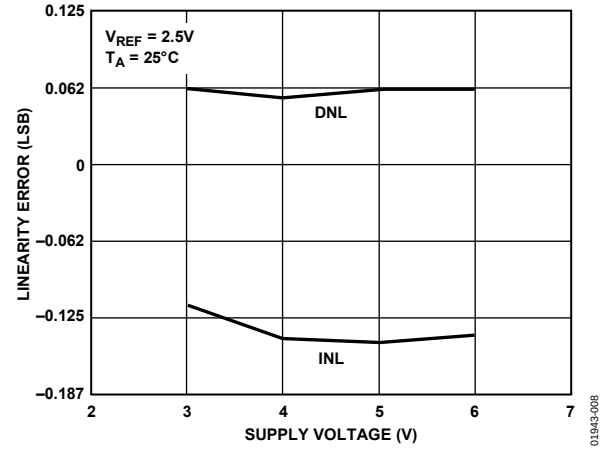


Figure 8. Linearity Error vs. Supply Voltage

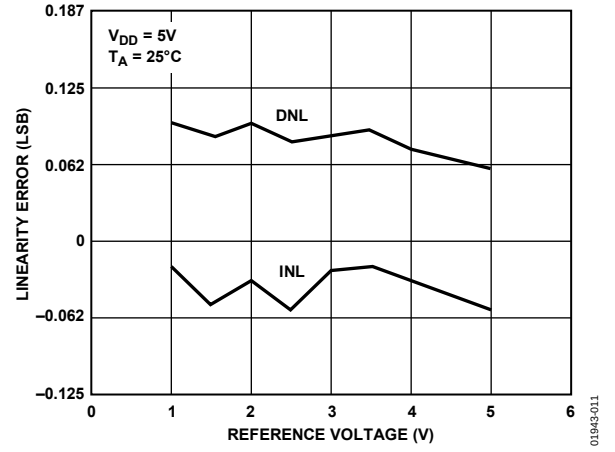


Figure 11. Linearity Error vs. Reference Voltage

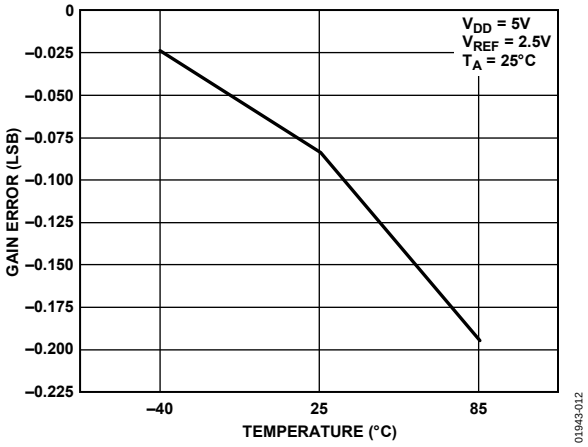


Figure 12. Gain Error vs. Temperature

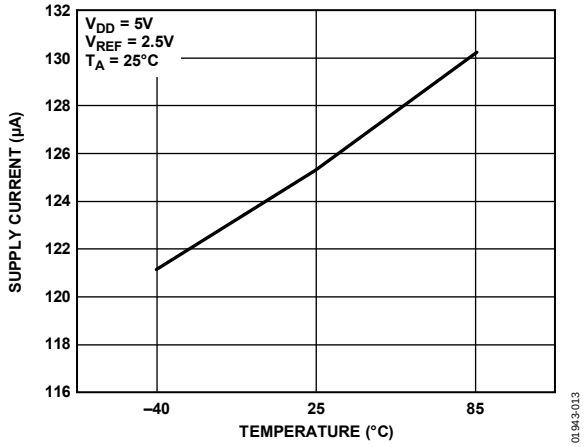


Figure 13. Supply Current vs. Temperature

Figure 14. Supply Current vs. Digital Input Voltage

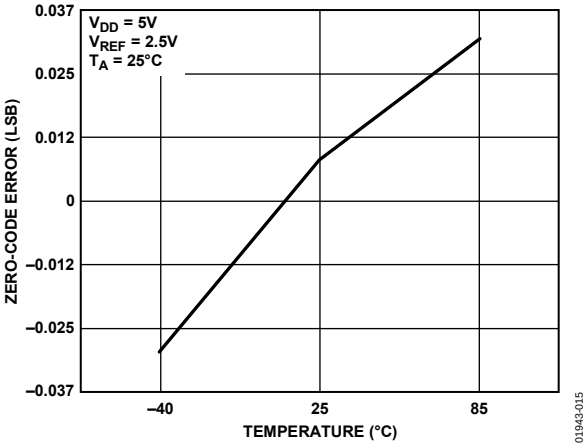


Figure 15. Zero-Code Offset Error vs. Temperature

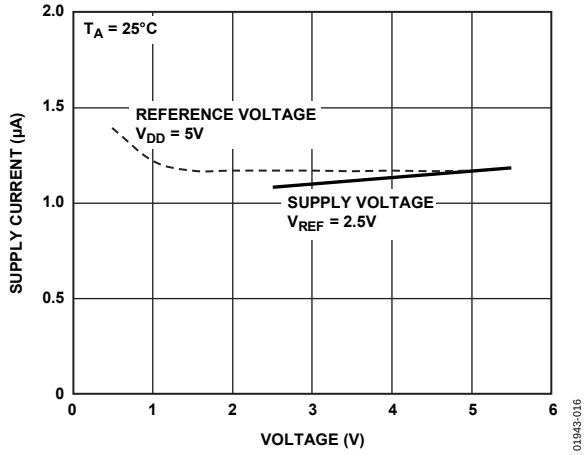


Figure 16. Supply Current vs. Reference Voltage or Supply Voltage

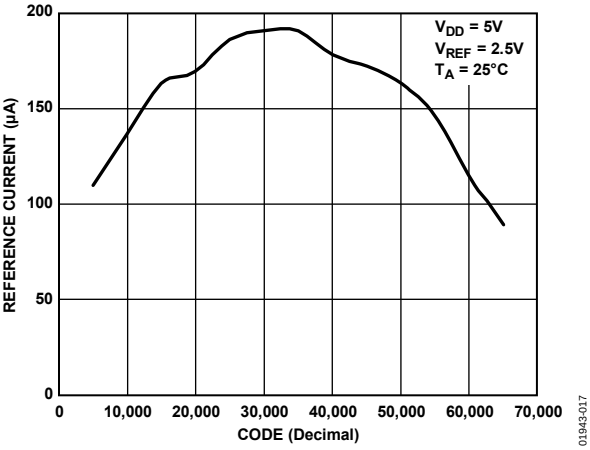


Figure 17. Reference Current vs. Code

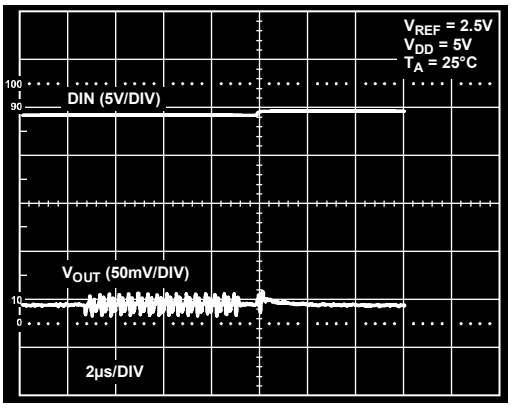


Figure 18. Digital Feedthrough

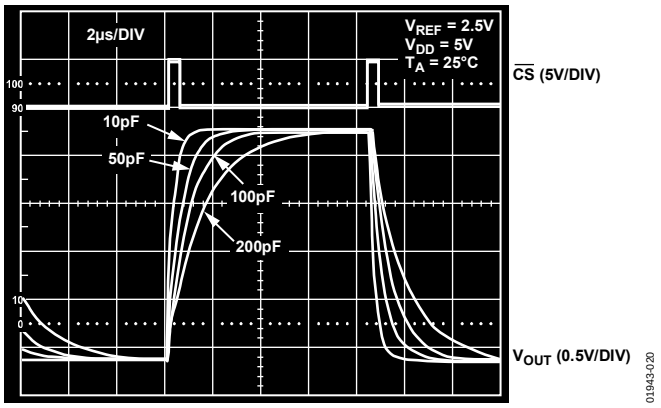


Figure 20. Large Signal Settling Time

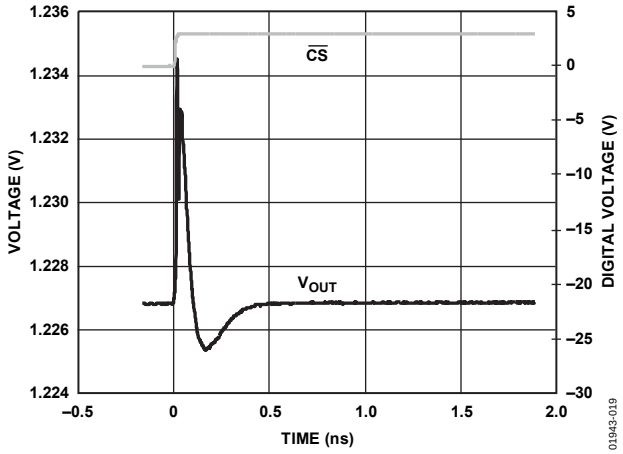


Figure 19. Digital-to-Analog Glitch Impulse

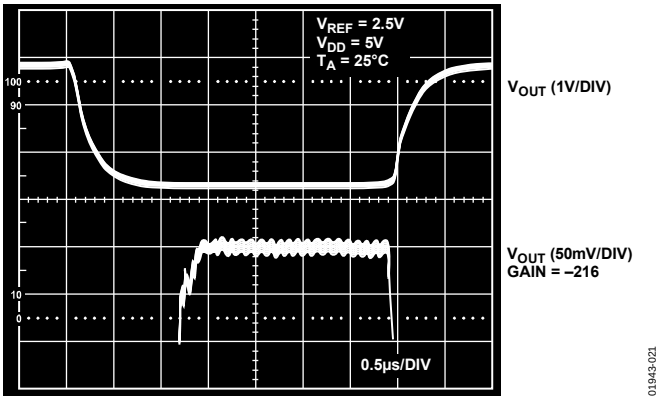


Figure 21. Small Signal Settling Time

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 6.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. A typical DNL vs. code plot can be seen in Figure 9.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
This is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero-Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero-Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A plot of the glitch impulse is shown in Figure 19.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{CS}$ is held high, while the CLK and DIN signals are toggled. It is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in Figure 18.

Power Supply Rejection Ratio
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

THEORY OF OPERATION

The AD5551/AD5552 are single, 14-bit, serial input, voltage output DACs. They operate from a single supply ranging from 2.7 V to 5.5 V and consume typically 125 μA with a supply of 5 V. Data is written to these devices in a 14-bit word format, via a 3-or 4-wire serial interface. To ensure a known power-up state, these parts were designed with a power-on reset function. In unipolar mode, the output is reset to 0 V, while in bipolar mode, the AD5552 output is set to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the AD5552.

DIGITAL-TO-ANALOG SECTION

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 22. The DAC architecture of the AD5551/AD5552 is segmented. The four MSBs of the 14-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 10 bits of the data word drive switches S0 to S9 of a 10-bit voltage mode R-2R ladder network.

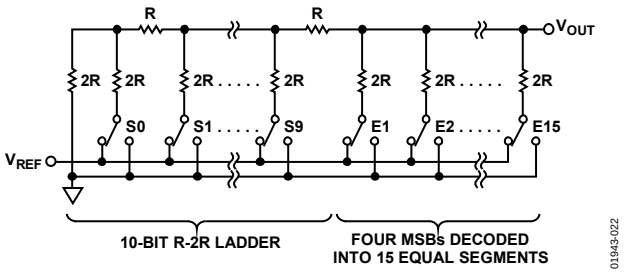


Figure 22. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data word loaded to the DAC register.
N is the resolution of the DAC.

For a reference of 2.5 V, the equation simplifies to the following,

$$V_{OUT} = \frac{2.5 \times D}{16{,}384}$$

This gives a V_{OUT} of 1.25 V with midscale loaded, and a V_{OUT} of 2.5 V with full-scale loaded to the DAC. The LSB size is $V_{REF}/16{,}384$.

SERIAL INTERFACE

The AD5551/AD5552 are controlled by a versatile 3-wire serial interface, which operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram can be seen in Figure 3. Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 14-bit words. After 14 data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can only be loaded to the part while $\overline{CS}$ is low.

The AD5552 has an $\overline{LDAC}$ function that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ may be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ loads the data to the DAC.

UNIPOLAR OUTPUT OPERATION

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low-supply current, typically 300 μA, and a low-offset error. The AD5551 provides a unipolar output swing ranging from 0 V to V_{REF}. The AD5552 can be configured to output both unipolar and bipolar voltages. Figure 23 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 6.

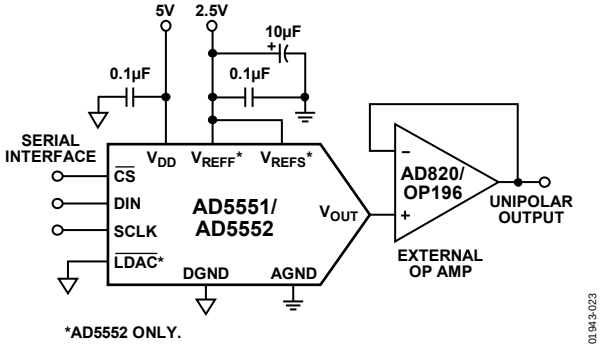


Figure 23. Unipolar Output

Table 6. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
11 1111 1111 1111	$V_{REF} \times (16{,}383/16{,}384)$
10 0000 0000 0000	$V_{REF} \times (8192/16{,}384) = ½\ V_{REF}$
00 0000 0000 0001	$V_{REF} \times (1/16{,}384)$
00 0000 0000 0000	0 V

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

$$V_{OUT-UNI} = \frac{D}{2^{14}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

where:
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
D is the decimal code loaded to the DAC.
V_{REF} is the reference voltage applied to part.
V_{GE} is the gain error in volts.
V_{ZSE} is the zero-scale error in volts.
INL is the integral nonlinearity in volts.

BIPOLAR OUTPUT OPERATION

With the aid of an external op amp, the AD5552 may be configured to provide a bipolar voltage output. A typical circuit of such operation is shown in Figure 24. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external op amp to achieve this bipolar output swing where $R_{FB} = R_{INV} = 28\ k\Omega$. Table 7 shows the transfer function for this output operating mode. Also provided on the AD5552 are a set of Kelvin connections to the analog ground inputs.

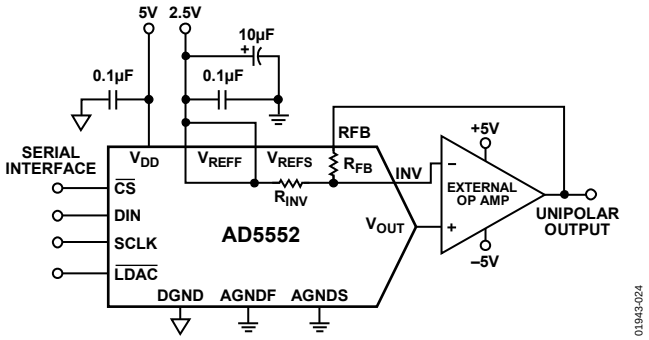


Figure 24. Bipolar Output (AD5552 Only)

Table 7. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
11 1111 1111 1111	$+V_{REF} \times (8191/8192)$
10 0000 0000 0000	$+V_{REF} \times (1/8192)$
00 0000 0000 0001	0 V
00 0000 0000 0000	$-V_{REF} \times (1/8192)$
00 0000 0000 0000	$-V_{REF} \times (8191/8192) = -V_{REF}$

Assuming a perfect reference, the worst-case bipolar output voltage may be calculated from the following equation.

$$V_{OUT-BIP} = \frac{[(V_{OUT-UNI} + V_{OS})(2 + RD) - V_{REF}(1 + RD)}{1 + (2 + RD)/A}$$

where:
V_{OS} is the external op amp input offset voltage.
RD is the R_{FB} and R_{IN} resistor matching error, unitless.
A is the op amp open-loop gain.

OUTPUT AMPLIFIER SELECTION

For bipolar mode, use a precision amplifier, supplied from a dual power supply. This provides the $\pm V_{REF}$ output. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp needs to have a very low-offset voltage, (the DAC LSB is 152 µV with a 2.5 V reference), to eliminate the need for output offset trims. Input bias current should also be very low as the bias current multiplied by the DAC output impedance (approximately 6K) adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, therefore increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a faster effective settling time of the combined DAC and amplifier.

FORCE SENSE BUFFER AMPLIFIER SELECTION

These amplifiers can be single-supply or dual supplies, low noise amplifiers. A low-output impedance at high frequencies is preferred as they need to be able to handle dynamic currents of up to ±20 mA.

REFERENCE AND GROUND

As the input impedance is code-dependent, the reference pin should be driven from a low-impedance source. The AD5551/AD5552 operate with a voltage reference ranging from 2 V to V_{DD}. Although DAC's full-scale output voltage is determined by the reference, references below 2 V results in reduced accuracy. Table 6 and Table 7 outline the analog output voltage for particular digital codes. For optimum performance, Kelvin sense connections are provided on the AD5552.

If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die. ADR291 and ADR293 are suitable references for this product.

POWER-ON RESET

These parts have a power-on reset function to ensure the output is at a known state upon power-up. After power-up, the DAC register contains all zeros, until data is loaded from the serial register. However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the DAC, 14 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 14 bits are loaded, only the last 14 are kept, and if fewer than 14 are loaded, bits remain from the previous word. If the AD5551/AD5552 needs to be interfaced with data shorter than 14 bits, the data should be padded with zeros at the LSBs.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5551/AD5552 is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD5551/AD5552 require a 14-bit data word with data valid on the rising edge of SCLK. The DAC update may be done automatically when all the data is clocked in or it may be done under control of LDAC (AD5552 only).

ADSP-21xx TO AD5551/AD5552 INTERFACE

Figure 25 shows a serial interface between the AD5551/AD5552 and the ADSP-21xx. The ADSP-21xx should be set to operate in the SPORT (serial port) transmit alternate framing mode. The ADSP-21xx is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. The first 2 bits are don't care as AD5551/AD5552 keeps the last 14 bits. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. Because of the edges-triggered difference, an inverter is required at the SCLKs between the DSP and the DAC.

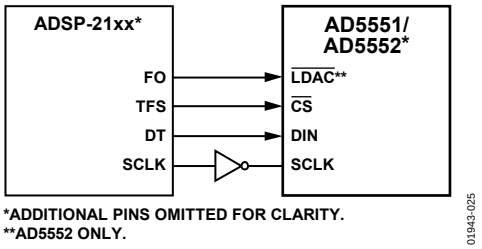


Figure 25. ADSP-21xx to AD5551/AD5552 Interface

68HC11 TO AD5551/AD5552 INTERFACE

Figure 26 shows a serial interface between the AD5551/AD5552 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC, while the MOSI output drives the serial data line DIN. $\overline{CS}$ signal is driven from one of the port lines. The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

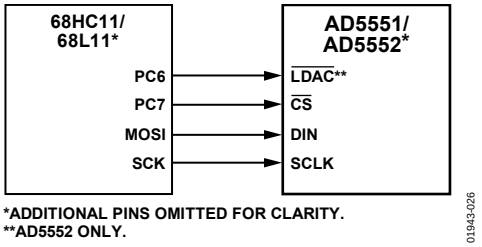


Figure 26. 68HC11/68L11 to AD5551/AD5552 Interface

MICROWIRE TO AD5551/AD5552 INTERFACE

Figure 27 shows an interface between the AD5551/AD5552 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD5551/AD5552 on the rising edge of the serial clock. No glue logic is required as the DAC clocks data into the input shift register on the rising edge.

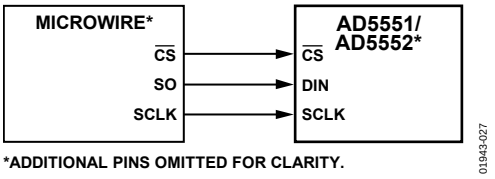


Figure 27. MICROWIRE to AD5551/AD5552 Interface

80C51/80L51 TO AD5551/AD5552 INTERFACE

A serial interface between the AD5551/AD5552 and the 80C51/80L51 microcontroller is shown in Figure 28. TxD of the microcontroller drives the SCLK of the AD5551/AD5552, while RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port which is used to drive $\overline{CS}$.

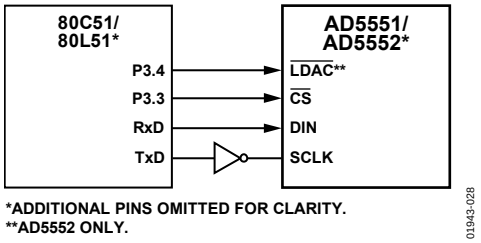


Figure 28. 80C51/80L51 to AD5551/AD5552 Interface

The 80C51/80L51 provides the LSB first, while the AD5551/AD5552 expect the MSB of the 14-bit word first. Take care to ensure that the transmit routine takes this into account. Usually it can be done through software by shifting out and accumulating the bits in the correct order before inputting to the DAC. Also, 80C51 outputs 2 byte words/16 bits data, thus the first two bits, after rearrangement, should be don't care as they are dropped from the 14-bit word of the DAC.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires a 14-bit word, P3.3 (or any one of the other programmable bits) is the $\overline{CS}$ input signal to the DAC, so P3.3 should be brought low at the beginning of the 16-bit write cycle 2 × 8 bit words and held low until the 16-bit 2 × 8 cycle is completed. After that, P3.3 is brought high again and the new data loads to the DAC. Again, the first two bits, after rearranging, should be don't care. $\overline{LDAC}$ on the AD5552 may also be controlled by the 80C51/80L51 serial port output by using another bit programmable pin, P3.4.

APPLICATIONS INFORMATION

OPTOCOUPLER INTERFACE

The digital inputs of the AD5551/AD5552 are Schmitt-triggered, so they can accept slow transitions on the digital input lines. This makes these parts ideal for industrial applications where it may be necessary that the DAC is isolated from the controller via optocouplers. Figure 29 illustrates such an interface.

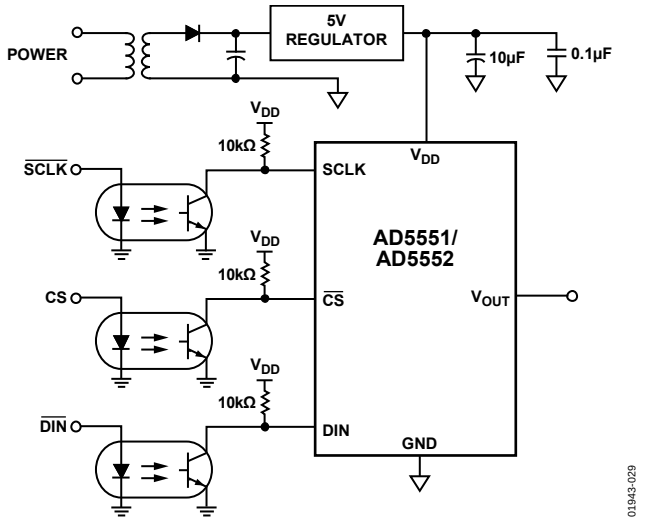


Figure 29. AD5551/AD5552 in an Optocoupler Interface

DECODING MULTIPLE AD5551/AD5552S

The $\overline{CS}$ pin of the AD5551/AD5552 can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time. The DAC addressed is determined by the decoder. There is some digital feedthrough from the digital input lines. Using a burst clock minimizes the effects of digital feedthrough on the analog signal channels. Figure 30 shows a typical circuit.

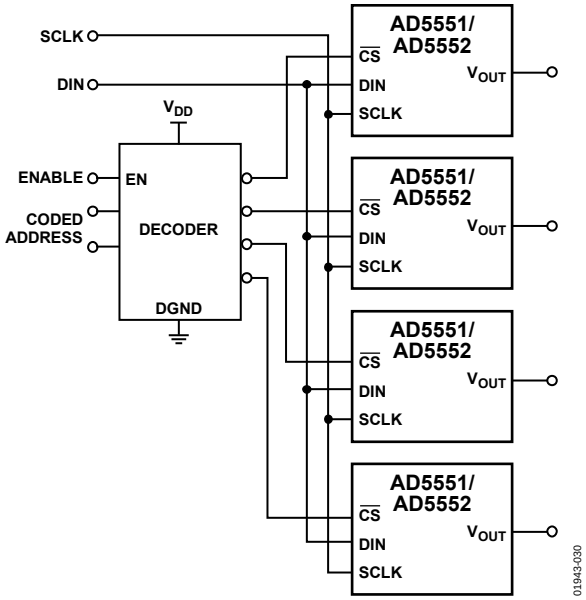
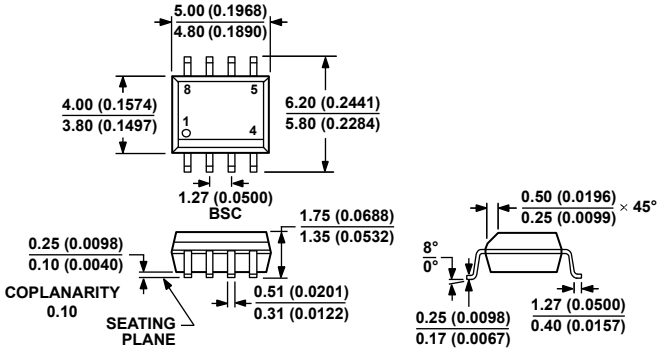


Figure 30. Addressing Multiple AD5551/AD5552s

OUTLINE DIMENSIONS



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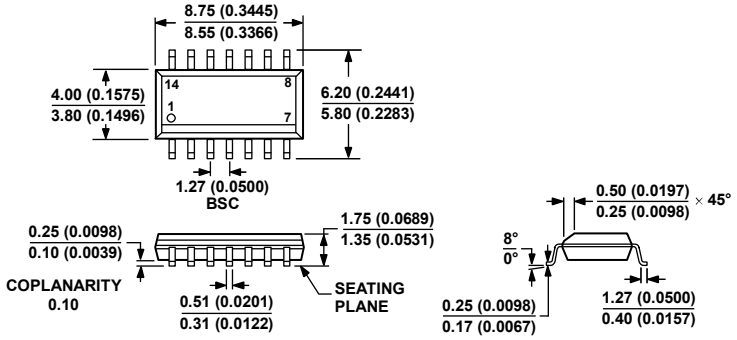
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 31. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 32. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	INL	DNL	Temperature Range	Package Description	Package Option
AD5551BRZ	±1 LSB	±0.8 LSB	−40°C to +85°C	8-Lead SOIC_N	R-8
AD5551BRZ-REEL7	±1 LSB	±0.8 LSB	−40°C to +85°C	8-Lead SOIC_N	R-8
AD5551BR	±1 LSB	±0.8 LSB	−40°C to +85°C	8-Lead SOIC_N	R-8
AD5551BR-REEL7	±1 LSB	±0.8 LSB	−40°C to +85°C	8-Lead SOIC_N	R-8
AD5552BRZ	±1 LSB	±0.8 LSB	−40°C to +85°C	14-Lead SOIC_N	R-14

[1] Z = RoHS Compliant Part.

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