1.2 A Programmable Device Power Supply with Integrated 16-Bit Level Setting DACs

Data Sheet **AD5560**

FEATURES

- Programmable device power supply (DPS)
  - FV, MI, MV, FNMV functions
- 5 internal current ranges (on-chip R_{SENSE})
  - ±5 µA, ±25 µA, ±250 µA, ±2.5 mA, ±25 mA
- 2 external high current ranges (external R_{SENSE})
  - EXTFORCE1: ±1.2 A maximum
  - EXTFORCE2: ±500 mA maximum
- Integrated programmable levels
  - All 16-bit DACs: force DAC, comparator DACs, clamp DACs, offset DAC, OSD DAC, DGS DAC
- Programmable Kelvin clamp and alarm
- Offset and gain correction registers on-chip
- Ramp mode on force DAC for power supply slewing
- Programmable slew rate feature, 1 V/µs to 0.3 V/µs
- DUTGND Kelvin sense and alarm
- 25 V FV span with asymmetrical operation within −22 V/+25 V
- On-chip comparators
- Gangable for higher current
- Guard amplifier
- System PMU connections
- Current clamps
- Die temperature sensor and shutdown feature
- On-chip diode thermal array
- Diagnostic register allows access to internal nodes
- Open-drain alarm flags (temperature, current clamp, Kelvin alarm)
- SPI-/MICROWIRE-/DSP-compatible interface
- 64-lead (10 mm × 10 mm) TQFP with exposed pad (on top)
- 72-ball (8 mm × 8 mm) flip-chip BGA

APPLICATIONS

- Automatic test equipment (ATE)
  - Device power supply

GENERAL DESCRIPTION

The AD5560 is a high performance, highly integrated device power supply consisting of programmable force voltages and measure ranges. This part includes the required DAC levels to set the programmable inputs for the drive amplifier, as well as clamping and comparator circuitry. Offset and gain correction is included on-chip for DAC functions. A number of programmable measure current ranges are available: five internal fixed ranges and two external customer-selectable ranges (EXTFORCE1 and EXTFORCE2) that can supply currents up to ±1.2 A and ±500 mA, respectively. The voltage range possible at this high current level is limited by headroom and the maximum power dissipation. Current ranges in excess of ±1.2 A or at high current and high voltage combinations can be achieved by paralleling or ganging multiple DPS devices. Open-drain alarm outputs are provided in the event of overcurrent, overtemperature, or Kelvin alarm on either the SENSE or DUTGND line.

The DPS functions are controlled via a simple 3-wire serial interface compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards running at clock speeds of up to 50 MHz.

Rev. E
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

5/2016—Rev. D to Rev. E

Changes to Figure 1 4
Changes to High Current Ranges Section 31
Added Calibration Section, Reducing Zero-Scale Error Section, Reducing Gain Error Section, Calibration Example Section, Additional Calibration Section, and System Level Calibration Section 41
Added Figure 58; Renumbered Sequentially 42
Changes to Table 25 57

8/2012—Rev. C to Rev. D

Added 72-Ball Flip-Chip BGA (Throughout) 1
Added Figure 7 and Table 5 (Renumbered Sequentially) 18
Added Applications Information Section 62
Updated Outline Dimensions 64
Changes to Ordering Guide 65

10/2010—Rev. B to Rev. C

Changes to Force Output Voltage Parameter and Load Transient Response Parameter, Table 1 5
Changes to Figure 52 29
Changes to Table 9 32

9/2009—Rev. A to Rev. B

Changes to Table 1, Measure Current and Measure Voltage Parameters 6
Changes to Die Temperature Sensor and Thermal Shutdown Section 31
Changes to Table 10 and Table 11 32
Changes to Table 18, Bit 15 45
Changes to Table 23, Bits[15:12] 50
Changes to Table 25 54

12/2008—Rev. 0 to Rev. A

Changes to Figure 1 4
Changes to Table 1 4
Changes to Table 2 13
Changes to Table 3 15
Changes to Open-Sense Detect (OSD) Alarm and Clamp 27
Changes to Figure 53 30
Change to g_m Maximum Rating, Table 13 34
Changes to Table 19 46
Changes to Bit 7, Bit 8 Functions, Table 21 48
Changes to Power Supply Decoupling Section 59

11/2008—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

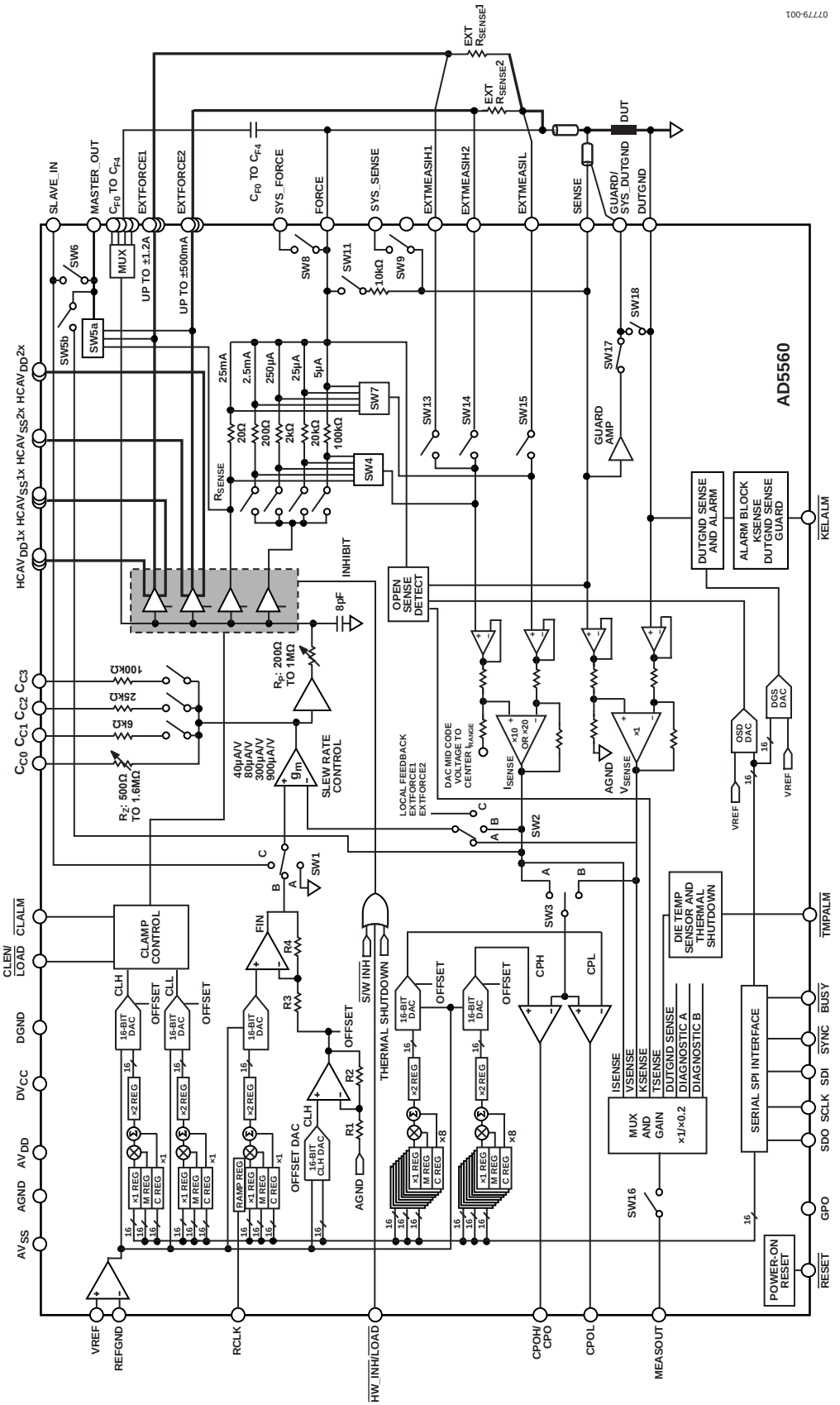


Figure 1.

SPECIFICATIONS

$HCAV_{DD}x \le (AV_{SS} + 33\ V)$, $HCAV_{DD}x \le AV_{DD}$, $HCAV_{SS}x \ge AV_{SS}$, $AV_{DD} \ge 8\ V$, $AV_{SS} \le -5\ V$, $|AV_{DD} - AV_{SS}| \ge 16\ V$ and $\le 33\ V$, DV_{CC} = 2.3 V to 5.5 V, V_{REF} = 5 V, gain (m), offset (c), and DAC offset registers are at default values; AGND = DGND = 0 V; T_J = 25°C to 90°C, maximum specifications, unless otherwise noted. FSV is full-scale voltage, FSVR is full-scale voltage range, FSC is full-scale current, FSCR is full-scale current range.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FORCE VOLTAGE					
Force Output Voltage[1]					
EXTFORCE1	AV_{SS} + 2.25		AV_{DD} − 2.25	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}1x$ + 1.75		$HCAV_{SS}1x$ − 1.75	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}1x$ + 1.25		$HCAV_{DD}1x$ − 1.25	V	Allow ±500 mV for external R_{SENSE} voltage drop; reduced headroom/footroom, clamps must be enabled[2]
EXTFORCE2	AV_{SS} + 2.25		AV_{DD} − 2.25	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}2x$ + 1.75		$HCAV_{DD}2x$ − 1.75	V	Allow ±500 mV for external R_{SENSE} voltage drop
	$HCAV_{SS}2x$ + 1.25		$HCAV_{DD}2x$ − 1.25	V	Allow ±500 mV for external R_{SENSE} voltage drop; reduced headroom/footroom, clamps must be enabled[2]
FORCE	AV_{SS} + 2.75		AV_{DD} − 2.75	V	Internal current ranges, includes ±500 mV for internal R_{SENSE} voltage drop
Headroom/Footroom[1]	−2.75		+2.75	V	Internal current ranges to AV_{DD}/AV_{SS}, includes ±500 mV for internal R_{SENSE} voltage drop.
Headroom/Footroom[1]	−2.25		+2.25	V	External current ranges, EXTFORCE1/ EXTFORCE2 to $HCAV_{DD}x$ and $HCAV_{SS}x$ supplies; includes ±500 mV for external R_{SENSE} voltage drop.\
Force Output Voltage Span	−22		+25	V	May be a skewed range but within headroom requirements and maximum power dissipation for current range
Forced Voltage Linearity Error	−2		+2	mV	
Forced Voltage Offset Error	−50		+50	mV	Uncalibrated, use c register to calibrate, measured at midscale
Forced Voltage Offset Error Tempco[1]		27		µV/°C	Standard deviation = 23 µV/°C
Forced Voltage Gain Error	−25		+25	mV	Uncalibrated, use m register to calibrate
Forced Voltage Gain Error Tempco[1]		4		ppm/°C	Standard deviation = 3 ppm/°C
Short-Circuit Current Limit[3]					Clamps off
EXTFORCE1	−3.5	±2.7	+3.5	A	Positive and negative dc short-circuit current
EXTFORCE2	−1.25	±0.9	+1.25	A	Positive and negative dc short-circuit current
FORCE	−75	±50	+75	mA	±25 mA range, positive and negative dc short-circuit current
	−20	±10	+20	mA	All other ranges, positive and negative dc short-circuit current
Active C_{Fx} Buffer	−64		+64	mA	
DC Load Regulation[1]	−1		+1	mV	EXTFORCE1 range, ±1 A load current change
	−0.4		+0.4	mV	EXTFORCE2 range, ±0.5 A load current change
Load Transient Response[1]		70		mV	1.2 A load step into 100 µF DUT capacitance (10 mΩ ESR), autocompensation mode
		140		mV	1.2 A load step into 30 µF DUT capacitance (10 mΩ ESR), autocompensation mode
NSD[1]		350		nV/√Hz	Measured at 1 kHz, at output of FORCE
MEASURE CURRENT RANGES					Sense resistors are trimmed to within 1%, nominal ±500 mV V_{RSENSE}
Internal Sense Resistors[1]		100		kΩ	±5 µA current range
		20		kΩ	±25 µA current range
		2		kΩ	±250 µA current range
		200		Ω	±2.5 mA current range
		20		Ω	±25 mA current range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Measure Current Ranges					Specified current ranges with V_{REF} = 5 V and MI gain = 20, or with V_{REF} = 2.5 V and MI gain = 5
		±5		µA	Set using internal sense resistor
		±25		µA	Set using internal sense resistor
		±250		µA	Set using internal sense resistor
		±2.5		mA	Set using internal sense resistor
		±25		mA	Set using internal sense resistor
		±500		mA	EXTFORCE2, set by user with external sense resistor, limited by headroom requirements and maximum power dissipation
		±1200		mA	EXTFORCE1, set by user with external sense resistor, limited by headroom requirements and maximum power dissipation
MEASURE CURRENT					All offset DAC/supply combinations settings, all gain settings are measure current = (I_{DUT} × R_{SENSE} × MI gain), unless otherwise noted
Differential Input Voltage Range[1]	−0.64		+0.64	V	Maximum voltage across R_{SENSE}, MI gain = 20
	−0.7		+0.7	V	Maximum voltage across R_{SENSE}, MI gain = 10
Output Voltage Span[1]		25		V	Measure current block alone (internal node)
Offset Error	−1		+1	% FSC	At 0 A, MI gain = 20, MEASOUT gain = 1
Offset Error Tempco[1]		−1		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−1.5		+1.5	% FSC	At 0 A, MI gain = 10, MEASOUT gain = 1
Offset Error Tempco[1]		−1		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−1.5		+1.5	% FSC	At 0 A, MI gain = 20, MEASOUT gain = 0.2
Offset Error Tempco[1]		3		ppm of FSC/°C	Standard deviation = 13 ppm/°C
Offset Error	−3		+3	% FSC	At 0 A, MI gain = 10, MEASOUT gain = 0.2
Offset Error Tempco[1]		8		ppm of FSC/°C	Standard deviation = 15 ppm/°C
Gain Error	−2		+2	% FSC	Internal current ranges, all gain settings
Gain Error[1]	−1		+1	% FSC	External current ranges, excluding R_{SENSE}
Gain Error Tempco[1]		20		ppm/°C	Standard deviation = 5 ppm/°C
MEASOUT Gain = 1					All supply conditions
Linearity Error	−0.01		+0.01	% FSCR	MI gain = 20 and 10
MEASOUT Gain = 0.2					Nominal supply (±16.5 V, 0x8000 offset DAC)
Linearity Error	−0.06		+0.06	% FSCR	MI gain = 20
Linearity Error	−0.05		+0.05	% FSCR	MI gain = 10
MEASOUT Gain = 0.2					Low supply (−25 V/+8 V, 0xD4EB offset DAC)
Linearity Error	−0.125		+0.125	% FSCR	MI gain = 20
Linearity Error	−0.175		+0.175	% FSCR	MI gain = 10
MEASOUT Gain = 0.2					High supply (−5 V/+28 V, 0xD1D offset DAC)
Linearity Error	−0.0875		+0.0875	% FSCR	MI gain = 20
Linearity Error	−0.1		+0.1	% FSCR	MI gain = 10
Common-Mode Error	−0.005		+0.005	%FSVR/V	% of FS change at measure output per volts change in DUT voltage
NSD[1]		900		nV/√Hz	MI gain = 20, MEASOUT gain = 1, measured at MEASOUT at 1 kHz, inputs grounded
		550		nV/√Hz	MI gain = 10, MEASOUT gain = 1, measured at MEASOUT at 1 kHz, inputs grounded
		170		nV/√Hz	MI gain = 20, MEASOUT gain = 0.2, measured at MEASOUT at 1 kHz, inputs grounded
		110		nV/√Hz	MI gain = 10, MEASOUT gain = 0.2, measured at MEASOUT at 1 kHz, inputs grounded
MEASURE VOLTAGE					MEASOUT Gain 1 and MEASOUT Gain 0.2
Measure Voltage Range[1]	AV_{SS} + 2.75		AV_{DD} − 2.75	V	All voltage ranges
Gain Error	−0.1		+0.1	% FS	
Gain Error Tempco[1]		3		ppm/°C	Standard deviation = 2 ppm/°C
MEASOUT Gain = 1					
Linearity Error	−2		+2	mV	
Offset Error	−12		+12	mV	
Offset Error Tempco[1]		2		µV/°C	Standard deviation = 12 µV/°C
NSD[1]		100		nV/√Hz	At 1 kHz, at MEASOUT, inputs grounded

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MEASOUT Gain = 0.2					
Linearity Error	−5.5		+5.5	mV	Referred to MV input, nominal supply (±16.5 V, 0x8000 offset DAC)
	−9		+24	mV	Referred to MV input, low supply (−25 V/+8 V, 0xD4EB offset DAC)
	−4		+13	mV	Referred to MV input, high supply (−5 V/+28 V, 0xD1D offset DAC)
Offset Error	−30		+20	mV	Referred to MV output
Offset Error Tempco[1]		10		µV/°C	Standard deviation = 12 µV/°C, referred to MV output
NSD[1]		50		nV/√Hz	At 1 kHz, at MEASOUT, inputs grounded
COMBINED LEAKAGE					Includes SYS_SENSE, SYS_FORCE, EXTFORCE1, EXTFORCE2, EXTMEASIH1, EXTMEASIH2, EXTMEASIL, FORCE, and SENSE; measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power up and tristate)
Leakage Current	−37.5		+37.5	nA	
	−30		+30	nA	T_J = 25°C to 70°C
Leakage Current Tempco[1]		±0.1	±0.4	nA/°C	
SENSE INPUT					
Leakage Current	−2.5		+2.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.01		nA/°C	
Pin Capacitance[1]		10		pF	
EXTMEASIH1, EXTMEASIH2, EXTMEASIL					
Leakage Current	−2.5		+2.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.01		nA/°C	
Pin Capacitance[1]		5		pF	
FORCE OUTPUT, FORCE					
Maximum Current Drive[1]	−30		+30	mA	
Leakage Current	−10		+10	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.03		nA/°C	
Pin Capacitance[1]		120		pF	
EXTFORCE1 OUTPUTS					
Maximum Current Drive[1]	−1200		+1200	mA	Set with external sense resistor, limited by headroom and power dissipation
Leakage Current	−7.5		+7.5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.03	±0.06	nA/°C	
Pin Capacitance[1]		275		pF	
EXTFORCE2 OUTPUTS					
Maximum Current Drive[1]	−500		+500	mA	Set with external sense resistor, limited by headroom and power dissipation
Leakage Current	−5		+5	nA	Measured with $\overline{PD}$ = 1, $\overline{SW\text{-}INH}$ = 0 (power-up and tristate)
Leakage Current Tempco[1]		±0.02	±0.05	nA/°C	
Pin Capacitance[1]		100		pF	
SYS_SENSE					
Voltage Range	AV_{SS}		AV_{DD}	V	
Leakage Current	−2.5		+2.5	nA	SYS_SENSE high-Z, force amplifier inhibited
Leakage Current Tempco[1]		±0.005	±0.025	nA/°C	
Path On Resistance			280	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
Pin Capacitance[1]		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYS_FORCE					
Voltage Range	AV_{SS}		AV_{DD}	V	
Current Carrying Capability[1]	−25		+25	mA	
Leakage Current	−2.5		+2.5	nA	SYS_FORCE high-Z, force amplifier inhibited
Leakage Current Tempco[1]		±0.005	±0.025	nA/°C	
Path On Resistance			35	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
Pin Capacitance[1]		5		pF	
SYS_DUTGND					
Voltage Range	AV_{SS}		AV_{DD}	V	
Path On Resistance		300	400	Ω	AV_{DD} = 16.5 V, AV_{SS} = −16.5 V
CURRENT CLAMP					
Clamp Accuracy	Programmed clamp value		Programmed clamp value + 10	% of FS	MI gain = 20, with clamp separation of 2 V, and 1 V separation from AGND/0 A
	Programmed clamp value		Programmed clamp value + 20	% of FS	MI gain = 10, with clamp separation of 2 V, and 1 V separation from AGND/0 A
VCLL to VCLH[1]	2			V	10% of FSCR (MI gain = 20), 20% of FSCR (MI gain = 10), restriction to prevent both clamps activating together
VCLL to 0 A[1]	1			V	5% of FSCR (MI gain = 20), 10% of FSCR (MI gain = 10), restriction to avoid impinging on FV before programmed level
VCLH to 0 A[1]	1			V	5% of FSCR (MI gain 20), 10% of FSCR (MI gain = 10), restriction to avoid impinging on FV before programmed level
Clamp Activation Response Time[1]		20	100	µs	Measured from $\overline{BUSY}$ going low to visible clamping
Clamp Recovery[1]		2	5	µs	Measured from $\overline{BUSY}$ going low to visible recovery
Alarm Delay [1]		50		µs	Time for $\overline{CLALM}$ to flag
FORCE AMPLIFER					
Slew Rate[1]		1		V/µs	Fastest slew rate, controlled via serial interface
		0.312		V/µs	Slowest slew rate, controlled via serial interface
Maximum Stable Load Capacitance[1]			160	µF	
Voltage Overshoot/Undershoot[1]			5	%	Of programmed value (≥1 V)
SETTLING TIME (FORCE AMPLIFER)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
FV (1200 mA EXTFORCE1 Range)[1]		16	25	µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
FV (900 mA EXTFORCE1 Range)[1]		18	30	µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
FV (500 mA EXTFORCE2 Range)[1]		34	53	µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
FV (300 mA EXTFORCE2 Range)[1]		25	50	µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
FV (25 mA Range)[1, 3]		125	180	µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
FV (2.5 mA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (250 µA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 40 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (25 µA Range)[1, 3]		400	600	µs	10 V step, R_{DUT} = 400 kΩ, C_{DUT} = 0.22 µF, full dc load
FV (5 µA Range)[1, 3]		20	40	µs	1 V step, R_{DUT} = 200 kΩ, C_{DUT} = 0.22 µF, full dc load
	Compensation Register 1 = 0x8880 (1.7 µF to 2.9 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		16	25	µs	3 V step, C_{DUT} = 2.2 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		60	80	µs	8 V step, C_{DUT} = 2.2 µF, full dc load
	Compensation Register 1 = 0xB880 (7.9µF to 13 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		55	70	µs	3 V step, C_{DUT} = 10 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		210	260	µs	8 V step, C_{DUT} = 10 µF, full dc load
	Compensation Register 1 = 0xC880 (13 µF to 22 µF, ESR 74 to 140 mΩ)				
FV (180 mA EXTFORCE1 Range)[1]		65	80	µs	3 V step, C_{DUT} = 20 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		310	370	µs	8 V step, C_{DUT} = 20 µF, full dc load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SETTLING TIME (FV, MEASURE CURRENT)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
MI (1200 mA EXTFORCE1 Range)[1]		30	40	µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
MI (900 mA EXTFORCE1 Range)[1]		32	42	µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
MI (500 mA EXTFORCE2 Range)[1]		69	95	µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
MI (300 mA EXTFORCE2 Range)[1]		70	100	µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
MI (25 mA Range)[1, 3]		650		µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
MI (2.5 mA Range)[1, 3]		6400		µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
MI Buffer Alone[1]		10	15	µs	0.5 V step using MEASOUT high-Z to within 10 mV of final value
SETTLING TIME (FV, MEASURE VOLTAGE)	Compensation Register 1 = 0x4880 (229 nF to 380 nF, ESR 74 to 140 mΩ)				To within 10 mV of programmed value
MV (1200 mA Range)[1]		16		µs	3.7 V step, R_{DUT} = 2.4 Ω, C_{DUT} = 0.22 µF, full dc load
MV (900 mA Range)[1]		20		µs	8 V step, R_{DUT} = 8.8 Ω, C_{DUT} = 0.22 µF, full dc load
MV (500 mA Range)[1]		34		µs	15 V step, R_{DUT} = 30 Ω, C_{DUT} = 0.22 µF, full dc load
MV (300 mA Range)[1]		25		µs	10 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0.22 µF, full dc load
MV (25 mA Range)[1, 3]		125	180	µs	20 V step, R_{DUT} = 800 Ω, C_{DUT} = 0.22 µF, full dc load
MV (2.5 mA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 4 kΩ, C_{DUT} = 0.22 µF, full dc load
MV (250 µA Range)[1, 3]		300	500	µs	10 V step, R_{DUT} = 40 kΩ, C_{DUT} = 0.22 µF, full dc load
MV Buffer Alone[1]		2	5	µs	10 V step using MEASOUT high-Z to within 10 mV of final value
SETTLING TIME (FV) SAFE MODE					To within 100 mV of programmed value
FV (1200 mA EXTFORCE1 Range[1]		25		µs	3.7 V step, R_{DUT} = 3.1 Ω, C_{DUT} = 0.22 µF, full dc load
FV (180 mA EXTFORCE1 Range)[1]		303		µs	3 V step, R_{DUT} = 16 Ω, C_{DUT} = 0. 22 µF to 20 µF, full dc load
FV (100 mA EXTFORCE2 Range)[1]		660		µs	8 V step, R_{DUT} = 33.3 Ω, C_{DUT} = 0. 22 µF to 20 µF, full dc load
FV (25 mA Range)[1, 3]		760	1000	µs	20 V step, R_{DUT} = 400 Ω, C_{DUT} = 0.22 µF, full dc load
SWITCHING TRANSIENTS					
Range Change Transient[1]			0.5	% of FV	C_{DUT} = 10 µF, changing from higher to adjacent lower ranges (except EXTFORCE1 to EXTFORCE2)
	20			mV	C_{DUT} = 10 µF, changing from lower (5 µA) to higher range (EXTFORCE1)
			0.5	% of FV	C_{DUT} = 100 µF, changing between all ranges
DAC SPECIFICATIONS					
Force/Comparator/Offset DACs					
Resolution		16		Bits	
Voltage Output Span	−22		+25	V	V_{REF} = 5 V, minimum and maximum values set by offset DAC
Differential Nonlinearity[1]	−1		+1	LSB	Guaranteed monotonic
Offset DAC					
Gain Error	−20		+20	mV	
Clamp DAC					CLL < CLH
Resolution		16		Bits	
Voltage Output Span	−22		+25	V	V_{REF} = 5 V, minimum and maximum values set by offset DAC
Differential Nonlinearity[1]	−1		+1	LSB	Guaranteed monotonic
OSD DAC					
Resolution		16		Bits	
Voltage Output Span	0.62		5	V	V_{REF} = 5 V
Differential Nonlinearity[1]	−2		+2	LSB	
DGS DAC					
Resolution		16		Bits	
Voltage Output Span	0		5	V	V_{REF} = 5 V
Differential Nonlinearity[1]	−2		+2	LSB	
Comparator DAC Dynamic					
Output Voltage Settling Time[1]		3.5	6	µs	1 V change to 1 LSB
Slew Rate[1]		1		V/µs	
Digital-to-Analog Glitch Energy[1]		10		nV-s	
Glitch Impulse Peak Amplitude[1]		40		mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT					
VREF DC Input Impedance	1			MΩ	Typically 100 MΩ
VREF Input Current	−10		+10	μA	Per input; typically ±30 nA
VREF Range[1]	2		5	V	
COMPARATOR					Measured directly at comparator; does not include measure block errors
Error	−7		+7	mV	Uncalibrated
VOLTAGE COMPARATOR					With respect to the measured voltage
Propagation Delay[1]		0.25		μs	
Error[1]	−12		+12	mV	Uncalibrated
CURRENT COMPARATOR					
Propagation Delay[1]		0.25	1	μs	
Error[1]	−1.5		+1.5	%	Of programmed current range, uncalibrated
MEASURE OUTPUT, MEASOUT					
Measure Output Voltage Span[1]	−12.81		+12.81	V	MEASOUT gain = 1, V_{REF} = 5 V, offset DAC = 0x8000
Measure Output Voltage Span[1]	−6.405		+6.405	V	MEASOUT gain = 1, V_{REF} = 2.5 V
Measure Output Voltage Span[1]	0		5.125	V	MEASOUT gain = 0.2, V_{REF} = 5 V, offset DAC = 0x8000
Measure Output Voltage Span[1]	0		2.56	V	MEASOUT gain = 0.2, V_{REF} = 2.5 V
Measure Pin Output Impedance			115	Ω	
Output Leakage Current	−100		+100	nA	When $\overline{HW\_INH}$ is low
Output Capacitance[1]		5		pF	
Short-Circuit Current[1]	−10		+10	mA	
OPEN-SENSE DETECT/CLAMP/ALARM					
Measurement Accuracy	−200		+200	mV	
Clamp Accuracy		600	900	mV	
Alarm Delay[1]		50		μs	
DUTGND					
Voltage Range[1]	−1		+1	V	
Pull-Up Current		+50	+70	μA	Pull-up for purpose of detecting open circuit on DUTGND, can be disabled
Leakage Current	−1		+1	μA	When pull-up disabled, DGS DAC = 0x3333 (1 V with V_{REF} = 5 V); if DUTGND voltage is far away from one of comparator thresholds, more leakage may be present
Trip Point Accuracy	−30		+10	mV	
Alarm Delay[1]		50		μs	
GUARD AMPLIFIER					
Voltage Range[1]	AV_{SS} + 2.25		AV_{DD} − 2.25	V	
Voltage Span[1]			25	V	
Output Offset	−10		+10	mV	
Short-Circuit Current[1]	−20		+20	mA	
Load Capacitance[1]			100	nF	
Output Impedance		100		Ω	
Alarm Delay[1]		200		μs	If it moves 100 mV away from input level
DIE TEMPERATURE SENSOR					
Accuracy[1]	−10		+10	%	Relative to a temperature change
Output Voltage at 25°C		1.54		V	
Output Scale Factor[1]		4.7		mV/°C	
Output Voltage Range[1]	1		2	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPI INTERFACE LOGIC					
Logic Inputs					
Input High Voltage, V_{IH}	1.7/2.0			V	(2.3 V to 2.7 V)/(2.7 V to 5.5 V) JEDEC-compliant input levels
Input Low Voltage, V_{IL}			0.7/0.8	V	(2.3 V to 2.7 V)/(2.7 V to 5.5 V) JEDEC-compliant input levels
Input Current, I_{INH}, I_{INL}	−1		+1	µA	
Input Capacitance, C_{IN}[1]			10	pF	
CMOS Logic Outputs					SDO, CPOL, CPOH, GPO, CPO
Output High Voltage, V_{OH}	DV_{CC} − 0.4			V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Tristate Leakage Current	−1		+1	µA	SDO, CPOL, CPOH, CPO
Output Capacitance[1]	10	10	10	pF	SDO, CPOL, CPOH, CPO
Open-Drain Logic Outputs					$\overline{BUSY}$, $\overline{TMPALM}$, $\overline{CLALM}$, $\overline{KELALM}$
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA, C_L = 50 pF, R_{PULLUP} = 1 kΩ
Output Capacitance[1]			10	pF	
POWER SUPPLIES					
$HCAV_{DD}1x$	4		28	V	$\lvert HCAV_{DD}x - HCAV_{SS}x \rvert$ < 33 V, $HCAV_{SS}x \geq AV_{SS}$, $HCAV_{DD}x \leq AV_{DD}$
$HCAV_{SS}1x$	−25		−5	V	
$HCAV_{DD}2x$	4		28	V	$\lvert HCAV_{DD}x - HCAV_{SS}x \rvert$ < 33 V, $HCAV_{SS}x \geq AV_{SS}$, $HCAV_{DD}x \leq AV_{DD}$
$HCAV_{SS}2x$	−25		−5	V	
AV_{DD}	8		28	V	$\lvert AV_{DD} - AV_{SS} \rvert$ < 33 V
AV_{SS}	−25		−5	V	
DV_{CC}	2.3		5.5	V	
AI_{DD}[4]			30	mA	All ranges
AI_{SS}[4]	−30			mA	All ranges
DI_{CC}			3	mA	
AI_{DD}[4]			27	mA	Channel inhibited/tristate, $\overline{HW\_INH}$ or $\overline{SW\text{-}INH}$ low
AI_{SS}[4]	−27			mA	Channel inhibited/tristate, $\overline{HW\_INH}$ or $\overline{SW\text{-}INH}$ low
					$HCAV_{DD}x$ and $HCAV_{SS}x$ supply currents shown are excluding load currents; however, for power budget calculations, the supply currents here are consumed by the load
$HCAI_{DD}1$			20	mA	When enabled, excluding load conditions
$HCAI_{DD}1$			0.5	mA	When disabled
$HCAI_{SS}1$	−20			mA	When enabled, excluding load condition
$HCAI_{SS}1$	−0.5			mA	When disabled
$HCAI_{DD}2$			15	mA	When enabled, excluding load conditions
$HCAI_{DD}2$			0.25	mA	When disabled
$HCAI_{SS}2$	−15			mA	When enabled, excluding load conditions
$HCAI_{SS}2$	−0.25			mA	When disabled
POWER-DOWN CURRENTS					Supply currents on power-up or during a power-down condition
$HCAI_{DD}$			250	µA	
$HCAI_{SS}$	−250			µA	
$HCAI_{DD}$			250	µA	
$HCAI_{SS}$	−250			µA	
AI_{DD}			5	mA	
AI_{SS}	−5			mA	
DI_{CC}			3	mA	
Maximum Power Dissipation					
EXTFORCE1			10	W	
EXTFORCE2			5	W	
Power-Up Overshoot[1]			5	%	Of programmed value

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Supply Sensitivity[1]					DC to 1 kHz
ΔForced Voltage/ΔAV_{DD}		−65		dB	−30 dB at 100 kHz
ΔForced Voltage/ΔAV_{SS}		−65		dB	−25 dB at 100 kHz
ΔForced Voltage/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔForced Voltage/$\Delta HCAV_{SS}x$		−90		dB	−62 dB at 100 kHz
ΔMeasured Current/ΔAV_{DD}		−50		dB	−25 dB at 100 kHz
ΔMeasured Current/ΔAV_{SS}		−43		dB	−20 dB at 100 kHz
ΔMeasured Current/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Current/$\Delta HCAV_{SS}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Voltage/ΔAV_{DD}		−65		dB	−30 dB at 100 kHz
ΔMeasured Voltage/ΔAV_{SS}		−65		dB	−25 dB at 100 kHz
ΔMeasured Voltage/$\Delta HCAV_{DD}x$		−90		dB	−60 dB at 100 kHz
ΔMeasured Voltage/$\Delta HCAV_{SS}x$		−90		dB	−65 dB at 100 kHz
ΔForced Voltage/ΔDV_{CC}		−80		dB	−46 dB at 100 kHz
ΔMeasured Current/ΔDV_{CC}		−80		dB	−36 dB at 100 kHz
ΔMeasured Voltage/ΔDV_{CC}		−80		dB	−46 dB at 100 kHz

[1] Guaranteed by design and characterization, not subject to production test.
[2] Programmable clamps must be enabled if taking advantage of reduced headroom/footroom.
[3] Clamps disabled.
[4] Not including internal pull-up current between AVDD/AVSS and HCAVDDx/HCAVSSx pins.

TIMING CHARACTERISTICS

$HCAV_{DD}x \le AV_{SS} + 33$ V, $HCAV_{SS}x \ge AV_{SS}$, $AV_{DD} \ge 8$ V, $AV_{SS} \le -5$ V, $|AV_{DD} - AV_{SS}| \ge 16$ V and ≤ 33 V, $V_{REF} = 5$ V (T_J = 25°C to 90°C, maximum specifications, unless otherwise noted).

Table 2. SPI Interface

Parameter[1, 2, 3]	DV_{CC} = 2.3 V to 2.7 V	DV_{CC} = 2.7 V to 3.3 V	DV_{CC} = 4.5 V to 5.5 V	Unit	Description
t_{UPDATE}	600	600	600	ns max	Channel update cycle time
t_1	25	20	20	ns min	SCLK cycle time; 60/40 duty cycle
t_2	10	8	8	ns min	SCLK high time
t_3	10	8	8	ns min	SCLK low time
t_4	10	10	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	15	15	15	ns min	Minimum $\overline{SYNC}$ high time
t_6	5	5	5	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	5	5	ns min	Data setup time
t_8	4.5	4.5	4.5	ns min	Data hold time
t_9[4]	40	35	30	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}	1.5	1.5	1.5	µs max	$\overline{BUSY}$ pulse width low for DAC x1 write
	280	280	280	ns max	$\overline{BUSY}$ pulse width low for other register write
t_{11}	25	20	10	ns min	$\overline{RESET}$ pulse width low
t_{12}	400	400	400	µs max	$\overline{RESET}$ time indicated by $\overline{BUSY}$ low
t_{13}	250	250	250	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_{14}[5, 6]	45	35	25	ns max	SCLK rising edge to SDO valid
t_{15}	30	30	30	ns max	$\overline{SYNC}$ rising edge to SDO high-Z
$\overline{LOAD}$ TIMING					
t_{16}	20	20	20	ns min	$\overline{LOAD}$ pulse width low
t_{17}	150	150	150	ns min	$\overline{BUSY}$ rising edge to force output response time
t_{18}	0	0	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LOAD}$ falling edge
t_{19}	150	150	150	ns min	$\overline{LOAD}$ rising edge to FORCE output response time
	150	150	150	ns min	$\overline{LOAD}$ rising edge to current range response

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 4 and Figure 5.
[4] This is measured with the load circuit shown in Figure 2.
[5] This is measured with the load circuit shown in Figure 3.
[6] Longer SCLK cycle time is required for correct operation of readback mode; consult timing diagrams and timing specifications.

TIMING DIAGRAMS

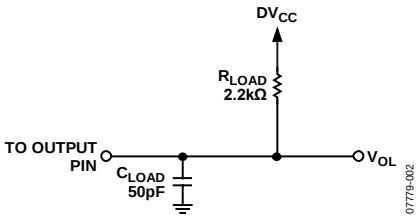


Figure 2. Load Circuit for Open Drain

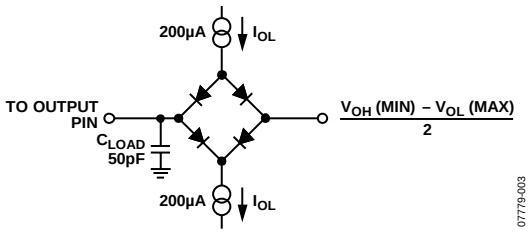


Figure 3. Load Circuit for CMOS

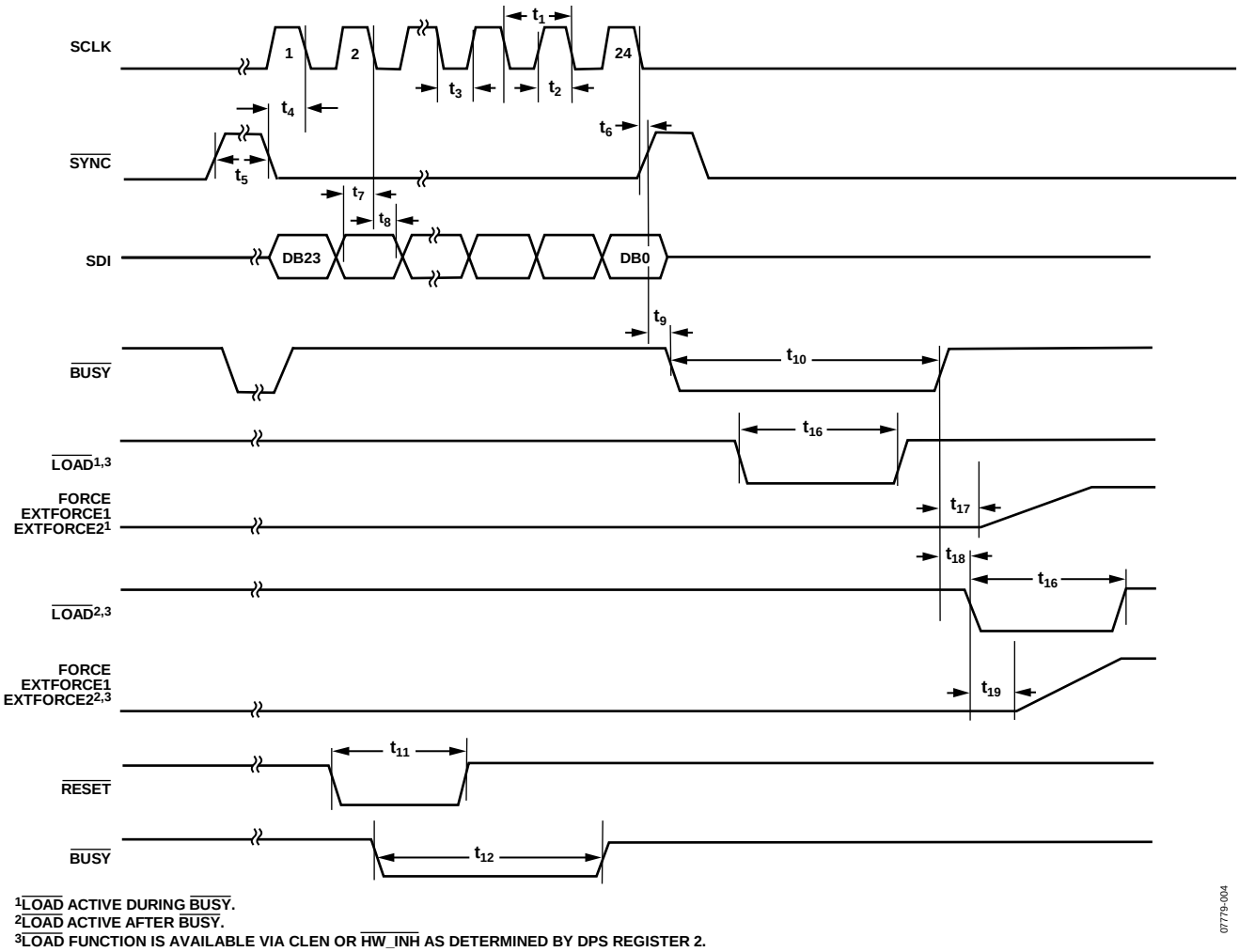


Figure 4. SPI Write Timing

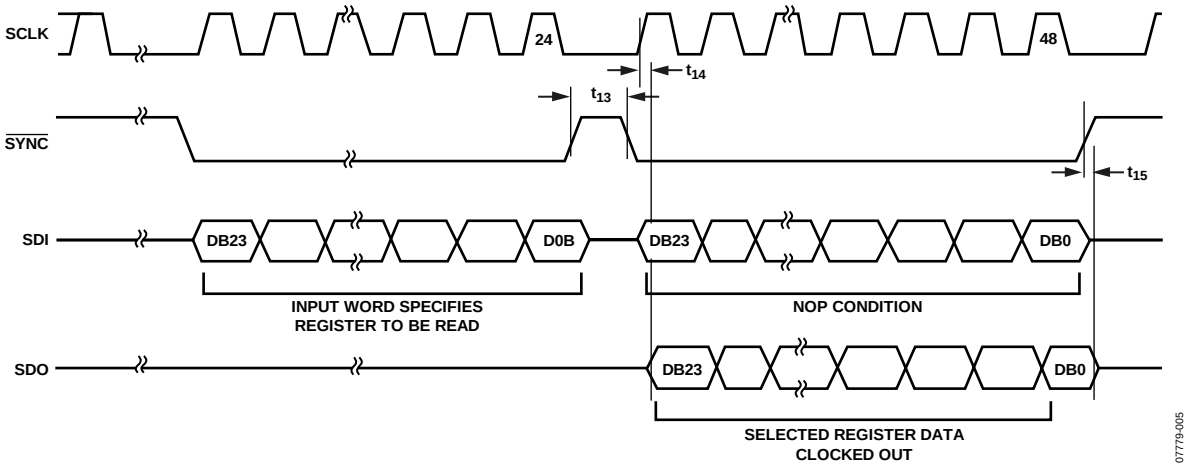


Figure 5. SPI Read Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AV_{DD} to AV_{SS}	34 V
AV_{DD} to AGND	−0.3 V to +34 V
AV_{SS} to AGND	−34 V to +0.3 V
$HCAV_{DD}x$ to $HCAV_{SS}x$	34 V
$HCAV_{DD}x$ to AGND	−0.3 V to +34 V
$HCAV_{SS}x$ to AGND	−34 V to +0.3 V
$HCAV_{DD}x$ to AV_{SS}	−0.3 V to AV_{SS} + 34 V
$HCAV_{DD}x$ to AV_{DD}	−0.3 V to AV_{DD} + 0.3 V
$HCAV_{SS}x$ to AV_{SS}	+0.3 V to AV_{SS} − 0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
REFGND to AGND	−0.3 V to +0.3 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
Analog Inputs to AGND	AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
EXTFORCE1 and EXTFORCE2 to AGND[1]	AV_{DD} − 28 V
Storage Temperature	−65°C to +125°C
Operating Junction Temperature	25°C to 90°C
Reflow Profile	J-STD 20 (JEDEC)
Junction Temperature	150°C max
Power Dissipation	10 W max (EXTFORCE1 stage)
	5 W max (EXTFORCE2 stage)
ESD	
HBM	1500 V
FICDM	500 V

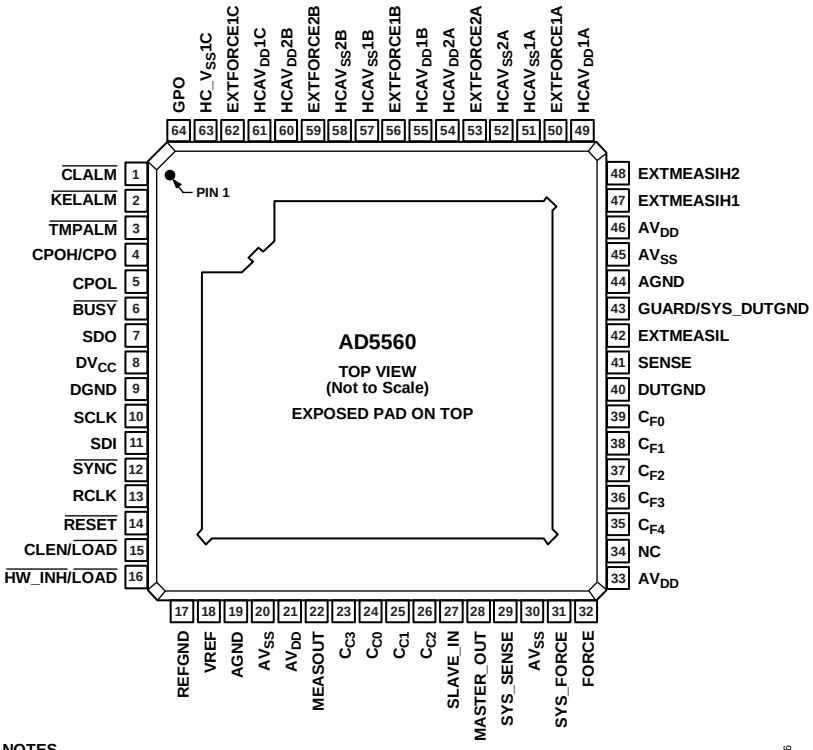
[1] When an EXTFORCE1 or EXTFORCE2 stage is enabled and the supply differential $|AV_{DD} - AV_{SS}| > 28$ V, take care to ensure that these pins are not directly shorted to AV_{SS} voltage at any time because this can cause damage to the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. EXPOSED PAD ON TOP OF PACKAGE. EXPOSED PAD IS INTERNALLY CONNECTED TO MOST NEGATIVE POINT, AV_{SS}.

Figure 6. TQFP_EP Pin Configuration

Table 4. TQFP_EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CLALM}}$	Clamp Alarm Output. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
2	$\overline{\text{KELALM}}$	Kelvin Alarm Pin for SENSE and DUTGND, Open-Drain Active Low. This pin can be programmed to be either latched or unlatched.
3	$\overline{\text{TMPALM}}$	Temperature Alarm Flag. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
4	CPOH/CPO	Comparator High Output (CPOH) or Window Comparator Output (CPO).
5	CPOL	Comparator Low Output.
6	$\overline{\text{BUSY}}$	Open-Drain Active Low Output. This pin indicates the status of the calibration engine for the DAC channels.
7	SDO	Serial Data Output. This pin is used for reading back DAC and DPS register information for diagnostic purposes.
8	DV_{CC}	Digital Supply Voltage.
9	DGND	Digital Ground Reference Point.
10	SCLK	Clock Input, Active Falling Edge.
11	SDI	Serial Data Input.
12	$\overline{\text{SYNC}}$	Frame Sync, Active Low.
13	RCLK	Ramp Clock Logic Input. If the ramp function is used, a clock signal of 833 kHz maximum should be applied to this input to drive the ramp circuitry. Tie RCLK low if it is unused.
14	$\overline{\text{RESET}}$	Logic Input. This pin is used to reset all internal nodes on the device to their power-on reset value.
15	CLEN/$\overline{\text{LOAD}}$	Clamp Enable. This input allows the user to enable or disable the clamp circuitry. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
16	$\overline{\text{HW\_INH}}$/$\overline{\text{LOAD}}$	Hardware Inhibit Input to Disable Force Amplifier. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
17	REFGND	Accurate Ground Reference for Applied Voltage Reference.

Pin No.	Mnemonic	Description
18	VREF	Reference Input for DAC Channels, Input Range 2 V to 5 V.
19, 44	AGND	Analog Ground.
20, 30, 45	AV_{SS}	Negative Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
21, 33, 46	AV_{DD}	Positive Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
22	MEASOUT	Multiplexed DUT voltage sense, DUT current sense, Kelvin sense, or temperature output; refer to AGND.
23	C_{C3}	Compensation Capacitor Input 3.
24	C_{C0}	Compensation Capacitor Input 0.
25	C_{C1}	Compensation Capacitor Input 1.
26	C_{C2}	Compensation Capacitor Input 2.
27	SLAVE_IN	Slave Input When Ganging Multiple DPS Devices.
28	MASTER_OUT	Master Output When Ganging Multiple DPS Devices.
29	SYS_SENSE	External Sense Signal Output.
31	SYS_FORCE	External Force Signal Input.
32	FORCE	Output Force Pin for Internal Current Ranges.
34	NC	No Connect.
35	C_{F4}	Feedforward Capacitor 4.
36	C_{F3}	Feedforward Capacitor 3.
37	C_{F2}	Feedforward Capacitor 2.
38	C_{F1}	Feedforward Capacitor 1.
39	C_{F0}	Feedforward Capacitor 0.
40	DUTGND	Device Under Test Ground.
41	SENSE	Input Sense Line.
42	EXTMEASIL	Low Side Measure Current Line for External High Current Ranges.
43	GUARD/SYS_DUTGND	Guard Amplifier Output Pin or System Device Under Test Ground Pin. See the DPS Register 2 in Table 19 for addressing details.
47	EXTMEASIH1	Input High Measure Line for External High Current Range 1.
48	EXTMEASIH2	Input High Measure Line for External High Current Range 2.
49, 55, 61	$HCAV_{DD}1A$, $HCAV_{DD}1B$, $HCAV_{DD}1C$	High Current Positive Analog Supply Voltage, for EXTFORCE1 Range.
50, 56, 62	EXTFORCE1A, EXTFORCE1B, EXTFORCE1C	Output Force. This pin is used for high Current Range 1, up to a maximum of ±1.2 A.
51, 57, 63	$HCAV_{SS}1A$, $HCAV_{SS}1B$, $HCAV_{SS}1C$	High Current Negative Analog Supply Voltage, for EXTFORCE1 Range.
52, 58	$HCAV_{SS}2A$, $HCAV_{SS}2B$	High Current Negative Analog Supply Voltage, for EXTFORCE2 Range.
53, 59	EXTFORCE2A, EXTFORCE2B	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
54, 60	$HCAV_{DD}2A$, $HCAV_{DD}2B$	High Current Positive Analog Supply Voltage, for EXTFORCE2 Range.
64	GPO	Extra Logic Output Bit. Ideal for external functions such as switching out a decoupling capacitor at DUT.
65	EP	The exposed pad is internally connected to AV_{SS}.

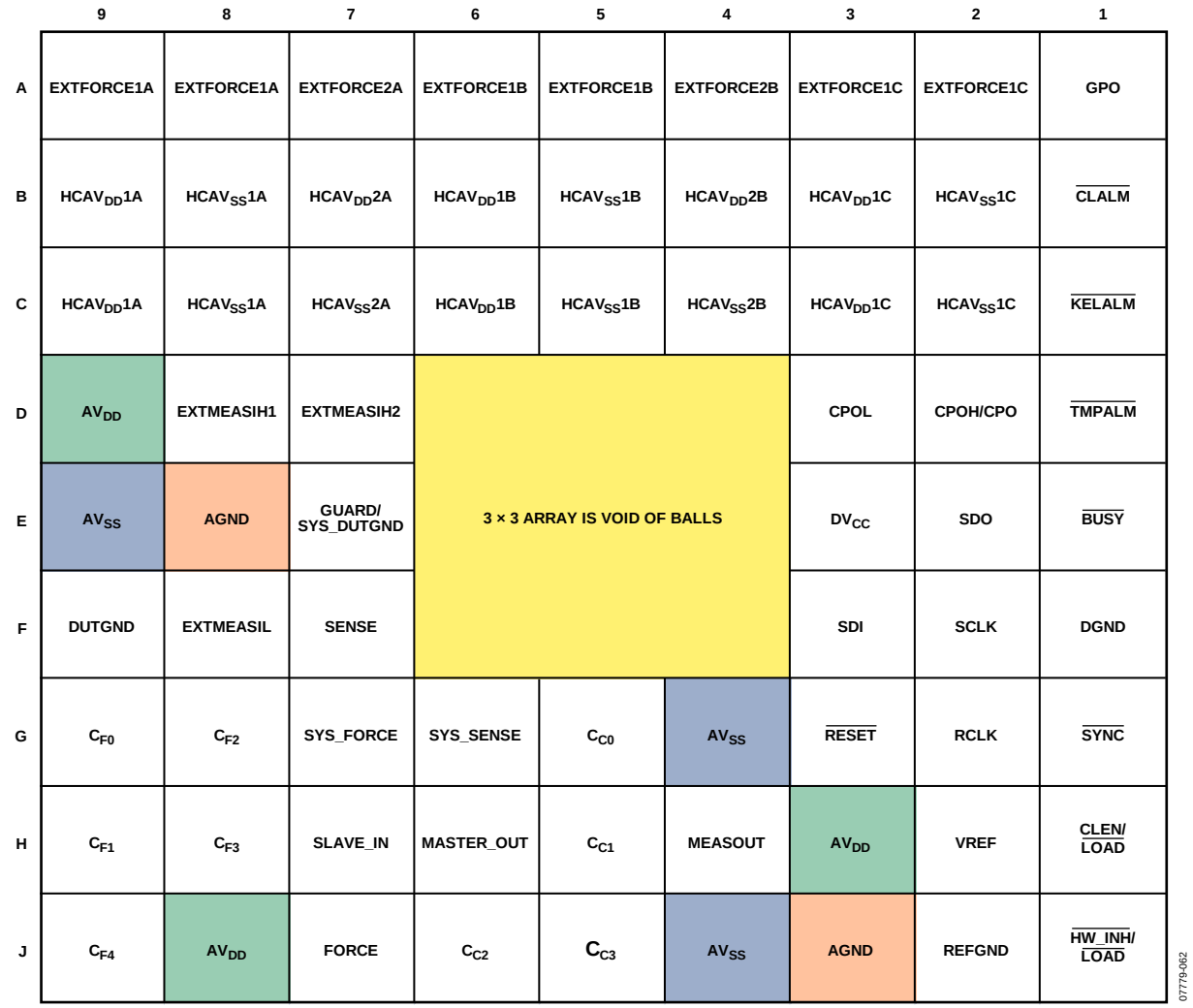


Figure 7. Flip-Chip BGA Pin Configuration, Bottom Side (BGA Balls Are Visible)

Table 5. Flip-Chip BGA Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GPO	Extra Logic Output Bit. Ideal for external functions such as switching out a decoupling capacitor at DUT.
A2, A3	EXTFORCE1C	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
A4	EXTFORCE2B	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
A5, A6	EXTFORCE1B	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
A7	EXTFORCE2A	Output Force. This pin is used for high Current Range 2, up to a maximum of ±500 mA.
A8, A9	EXTFORCE1A	Output Force. These pins are used for high Current Range 1, up to a maximum of ±1.2 A.
B1	$\overline{\text{CLALM}}$	Clamp Alarm Output. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
B2, C2	$HCAV_{SS}1C$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B3, C3	$HCAV_{DD}1C$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
B4	$HCAV_{DD}2B$	High Current Positive Analog Supply Voltage for EXTFORCE2 Range.
B5, C5	$HCAV_{SS}1B$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B6, C6	$HCAV_{DD}1B$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
B7	$HCAV_{DD}2A$	High Current Positive Analog Supply Voltage for EXTFORCE2 Range.
B8, C8	$HCAV_{SS}1A$	High Current Negative Analog Supply Voltage for EXTFORCE1 Range.
B9, C9	$HCAV_{DD}1A$	High Current Positive Analog Supply Voltage for EXTFORCE1 Range.
C1	$\overline{\text{KELALM}}$	Kelvin Alarm Pin for SENSE and DUTGND, Open-Drain Active Low. This pin can be programmed to be either latched or unlatched.
C4	$HCAV_{SS}2B$	High Current Negative Analog Supply Voltage for EXTFORCE2 Range.
C7	$HCAV_{SS}2A$	High Current Negative Analog Supply Voltage for EXTFORCE2 Range.

Pin No.	Mnemonic	Description
D1	$\overline{\text{TMPALM}}$	Temperature Alarm Flag. Open-drain output, active low; this pin can be programmed to be either latched or unlatched.
D2	CPOH/CPO	Comparator High Output (CPOH) or Window Comparator Output (CPO).
D3	CPOL	Comparator Low Output.
D7	EXTMEASIH2	Input High Measure Line for External High Current Range 2.
D8	EXTMEASIH1	Input High Measure Line for External High Current Range 1.
D9,H3, J8	AV_{DD}	Positive Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
E1	$\overline{\text{BUSY}}$	Open-Drain Active Low Output. This pin indicates the status of the calibration engine for the DAC channels.
E2	SDO	Serial Data Output. This pin is used for reading back DAC and DPS register information for diagnostic purposes.
E3	DV_{CC}	Digital Supply Voltage.
E7	GUARD/SYS_DUTGND	Guard Amplifier Output Pin or System Device Under Test Ground Pin. See the DPS Register 2 in Table 19 for addressing details.
E8	AGND	Analog Ground.
E9, G4, J4	AV_{SS}	Negative Analog Supply Voltage. These pins supply DACs and other high voltage circuitry, such as measure blocks.
F1	DGND	Digital Ground Reference Point.
F2	SCLK	Clock Input, Active Falling Edge.
F3	SDI	Serial Data Input.
F7	SENSE	Input Sense Line.
F8	EXTMEASIL	Low Side Measure Current Line for External High Current Ranges.
F9	DUTGND	Device Under Test Ground.
G1	$\overline{\text{SYNC}}$	Frame Sync, Active Low.
G2	RCLK	Ramp Clock Logic Input. If the ramp function is used, a clock signal of 833 kHz maximum should be applied to this input to drive the ramp circuitry. Tie RCLK low if it is unused.
G3	$\overline{\text{RESET}}$	Logic Input. This pin is used to reset all internal nodes on the device to their power-on reset value.
G5	C_{C0}	Compensation Capacitor Input 0.
G6	SYS_SENSE	External Sense Signal Output.
G7	SYS_FORCE	External Force Signal Input.
G8	C_{F2}	Feedforward Capacitor 2.
G9	C_{F0}	Feedforward Capacitor 0.
H1	CLEN/$\overline{\text{LOAD}}$	Clamp Enable. This input allows the user to enable or disable the clamp circuitry. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
H2	VREF	Reference Input for DAC Channels, Input Range is 2 V to 5 V.
H4	MEASOUT	Multiplexed DUT voltage sense, DUT current sense, Kelvin sense, or temperature output; refer to AGND.
H5	C_{C1}	Compensation Capacitor Input 1.
H6	MASTER_OUT	Master Output When Ganging Multiple DPS Devices.
H7	SLAVE_IN	Slave Input When Ganging Multiple DPS Devices.
H8	C_{F3}	Feedforward Capacitor 3.
H9	C_{F1}	Feedforward Capacitor 1.
J1	$\overline{\text{HW\_INH}}$/$\overline{\text{LOAD}}$	Hardware Inhibit Input to Disable Force Amplifier. This pin can be configured as a $\overline{\text{LOAD}}$ function to allow synchronization of multiple devices. Either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ input (see the system control register, Address 0x1).
J2	REFGND	Accurate Ground Reference for Applied Voltage Reference.
J3	AGND	Analog Ground.
J5	C_{C3}	Compensation Capacitor Input 3.
J6	C_{C2}	Compensation Capacitor Input 2.
J7	FORCE	Output Force Pin for Internal Current Ranges.
J9	C_{F4}	Feedforward Capacitor 4.

TYPICAL PERFORMANCE CHARACTERISTICS

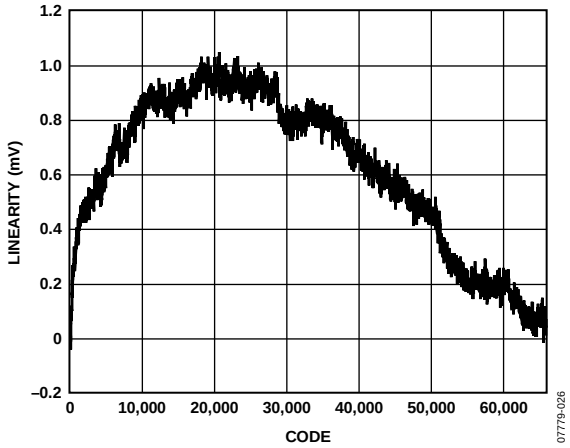


Figure 8. Force Voltage Linearity vs. Code, V_{REF} = 5 V, No Load

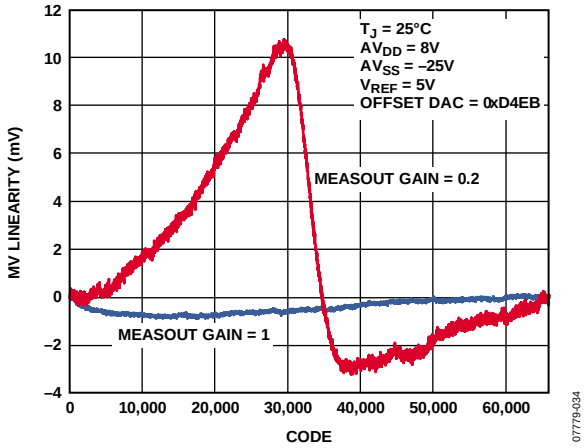


Figure 11. Measure Voltage Linearity vs. Code (MEASOUT Gain 1, MEASOUT Gain = 0.2, Negative Skew Supply)

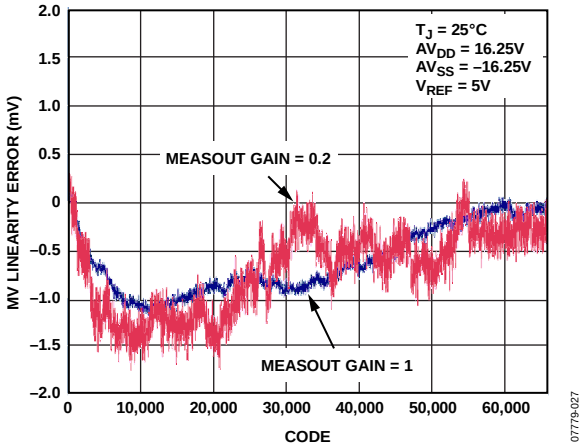


Figure 9. Measure Voltage Linearity vs. Code (MEASOUT Gain = 1, MEASOUT Gain = 0.2, Nominal Supplies)

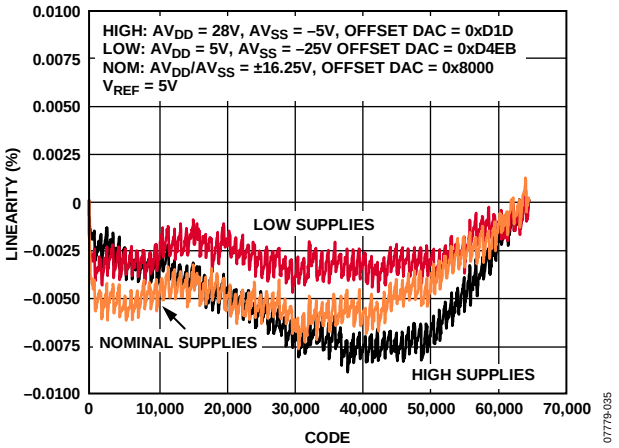


Figure 12. Measure Current Linearity vs. Code (MEASOUT Gain = 1, MI Gain = 20), T_J = 25°C

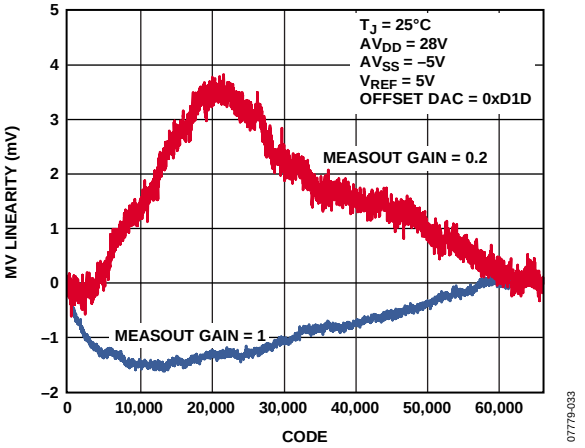


Figure 10. Measure Voltage Linearity vs. Code (MEASOUT Gain = 1, MEASOUT Gain = 0.2, Positive Skew Supply)

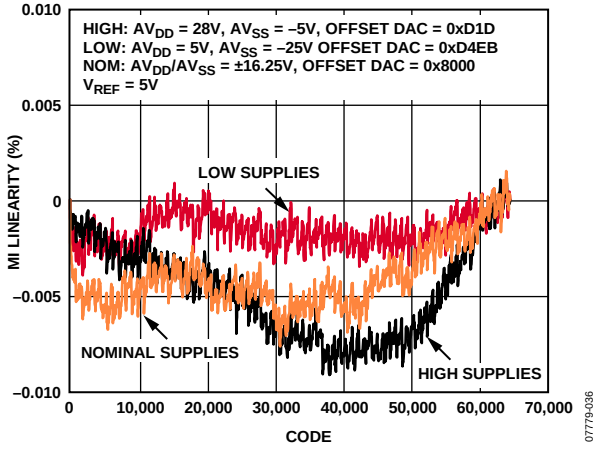


Figure 13. Measure Current Linearity vs. Code (MEASOUT Gain = 1, MI Gain = 10)

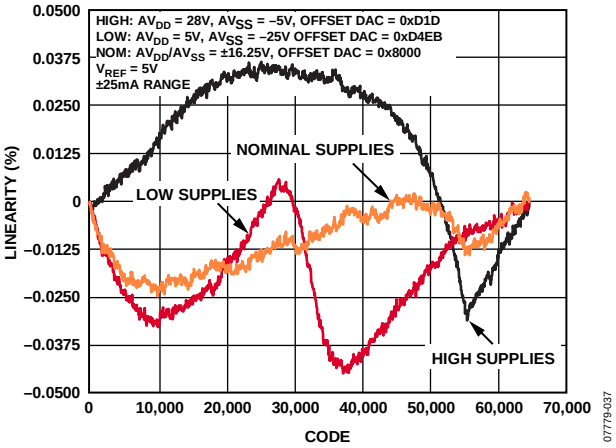


Figure 14. Measure Current Linearity vs. Code (MEASOUT Gain = 0.2, MI Gain = 20)

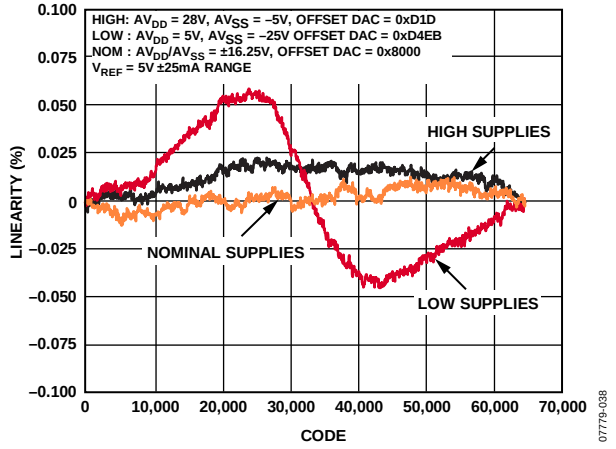


Figure 15. Measure Current Linearity vs. Code (MEASOUT Gain = 0.2, MI Gain = 10)

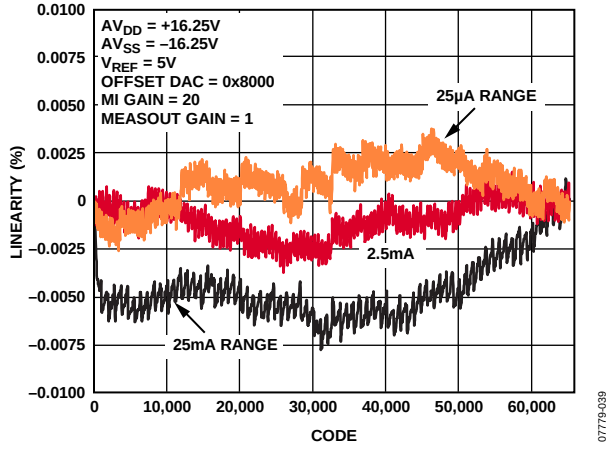


Figure 16. Measure Current Linearity vs. I_{RANGE} (MEASOUT Gain = 1, MI Gain = 20)

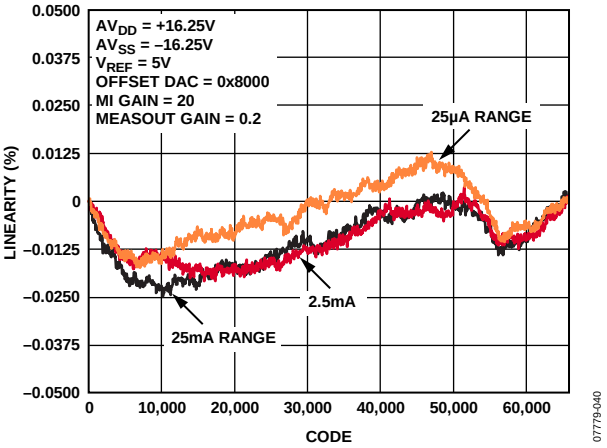


Figure 17. Measure Current Linearity vs. I_{RANGE} (MEASOUT Gain = 0.2, MI Gain = 20)

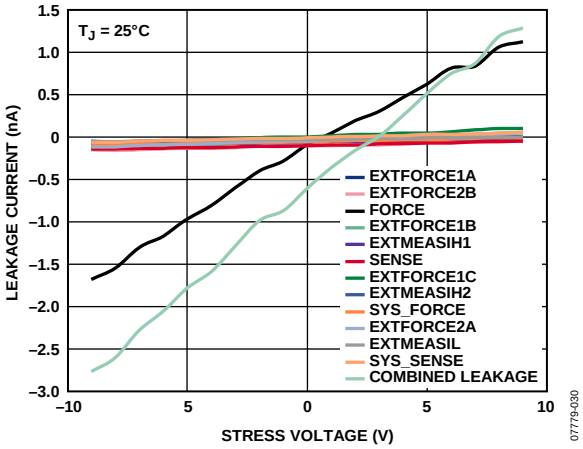


Figure 18. Leakage Current vs. Stress Voltage (Force and Combined Leakage)

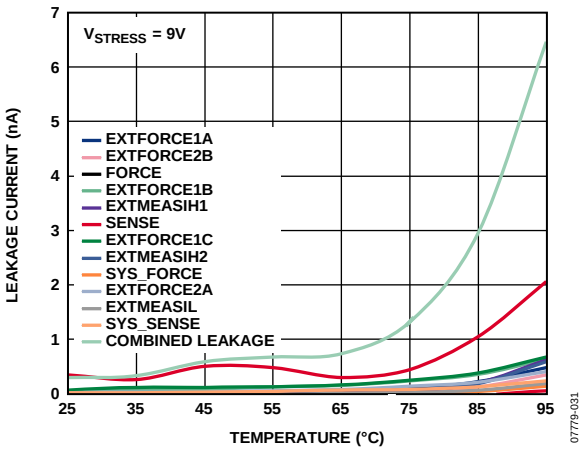


Figure 19. Leakage Current vs. Temperature (Force and Combined Leakage), V_{STRESS} = 9 V

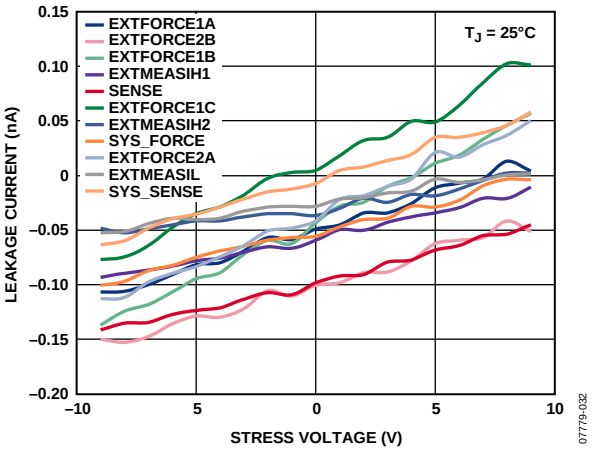


Figure 20. Leakage Current vs. Stress Voltage

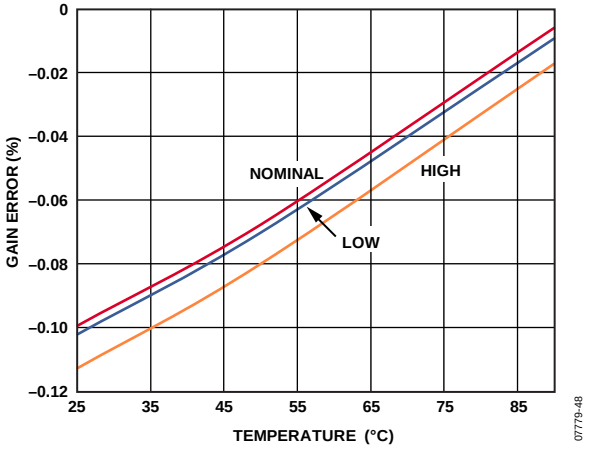


Figure 23. MI Positive Gain Error vs. Temperature, MI Gain = 20, MEASOUT Gain = 1

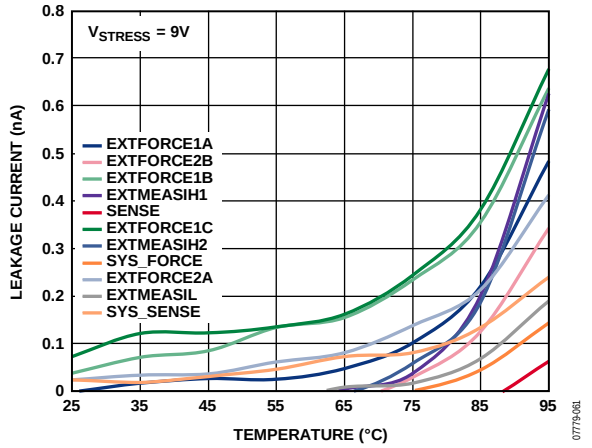


Figure 21. Leakage Current vs. Temperature, V_{STRESS} = 9 V

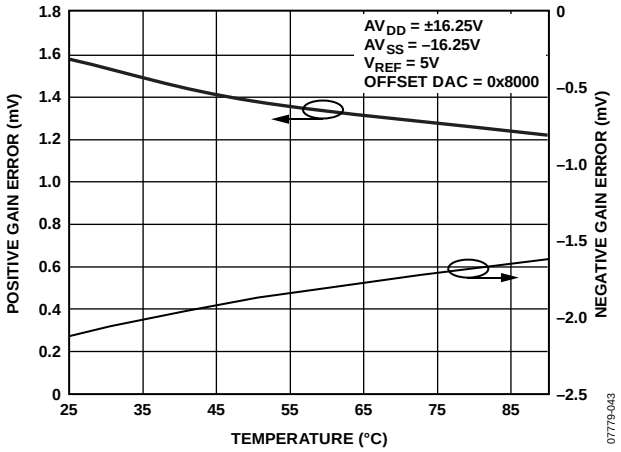


Figure 24. FV Gain Error vs. Temperature

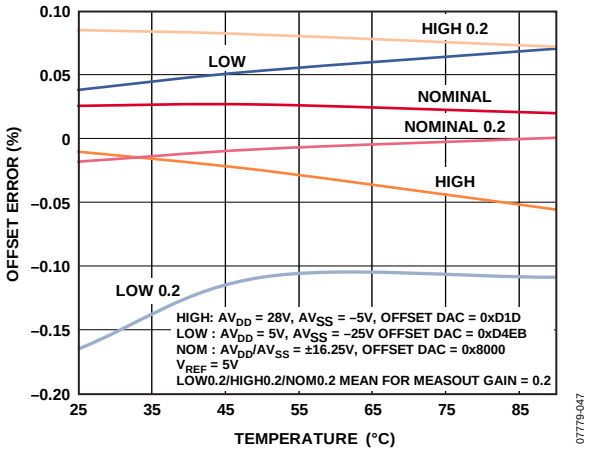


Figure 22. MI Offset Error vs. Temperature, MI Gain = 20, MEASOUT Gain = 1 and 0.2

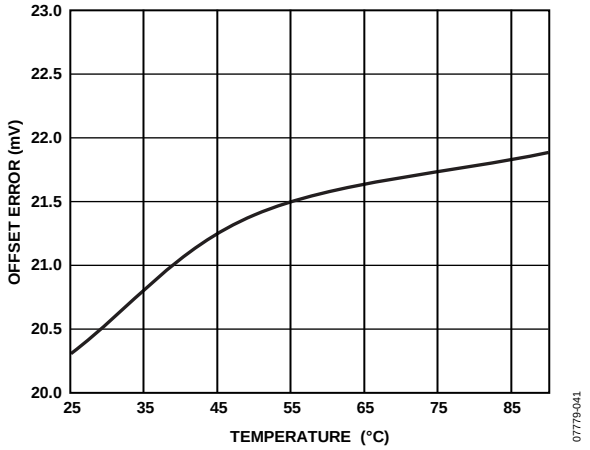


Figure 25. FV Offset Error vs. Temperature

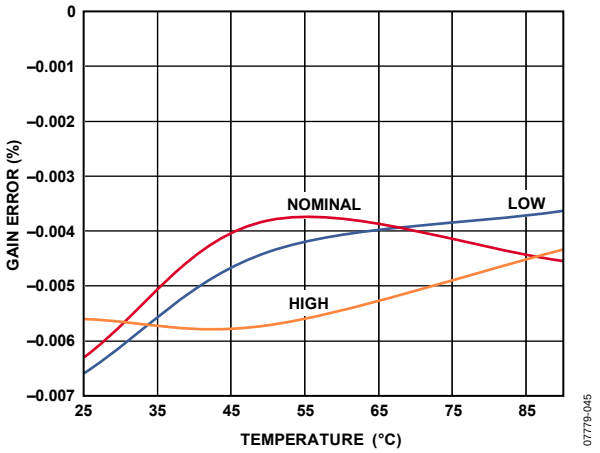


Figure 26. MV Gain Error vs. Temperature, MEASOUT Gain = 1

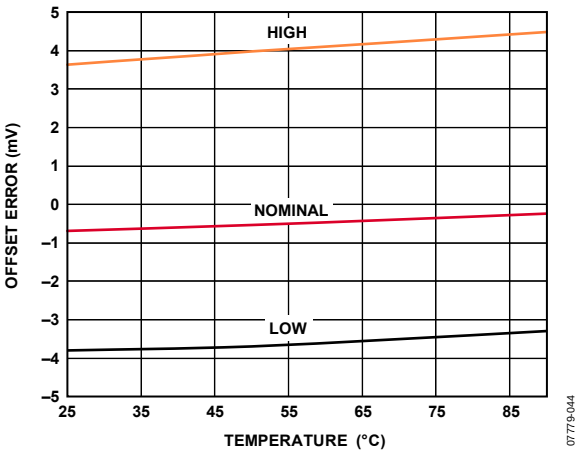


Figure 29. MV Offset Error vs. Temperature, MEASOUT Gain = 0.2

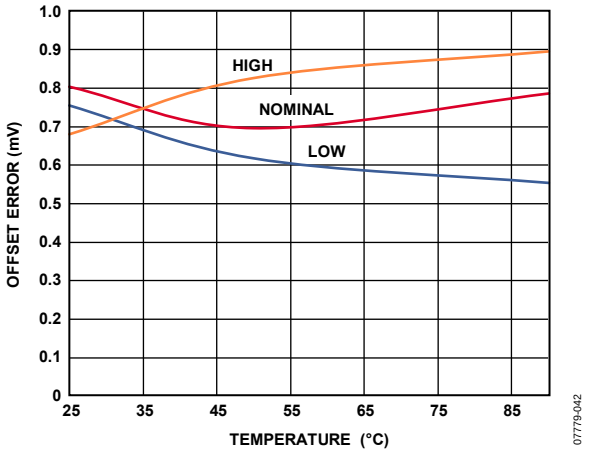


Figure 27. MV Offset Error vs. Temperature, MEASOUT Gain = 1

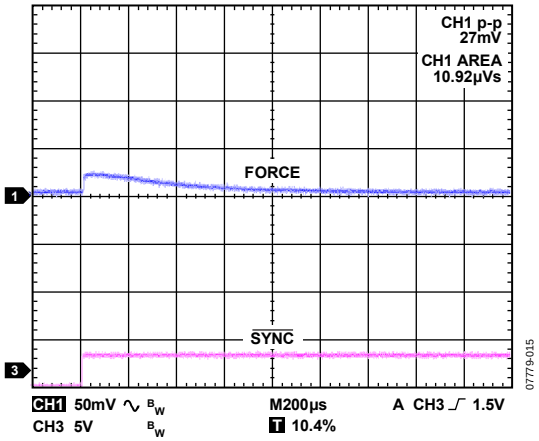


Figure 30. Range Change 2.5 mA to 25 mA, Safe Mode, 2.5 mA I_{LOAD}, 10 µF Load

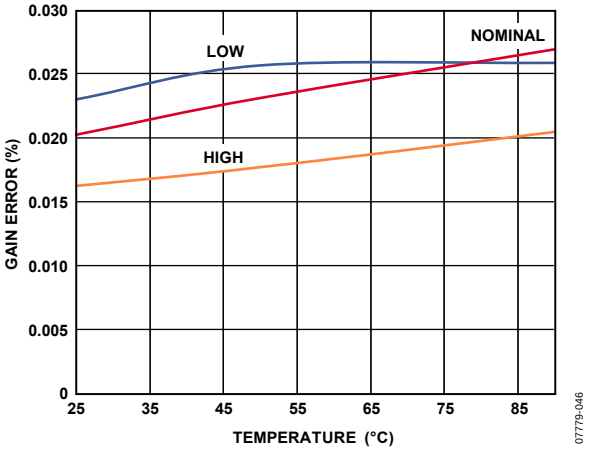


Figure 28. MV Gain Error vs. Temperature, MEASOUT Gain = 0.2

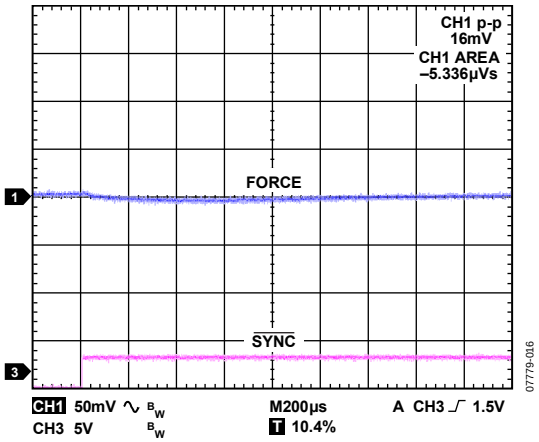


Figure 31. Range Change 25 mA to 2.5 mA, Safe Mode, 2.5 mA I_{LOAD}, 10 µF Load

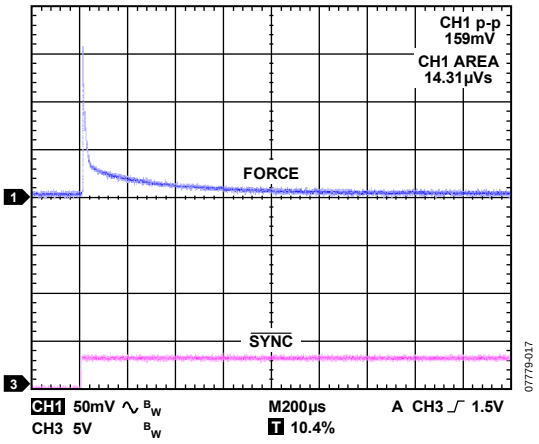


Figure 32. Range Change 25 mA to EXTFORCE2, Safe Mode, 25 mA I_{LOAD}, 10 µF Load

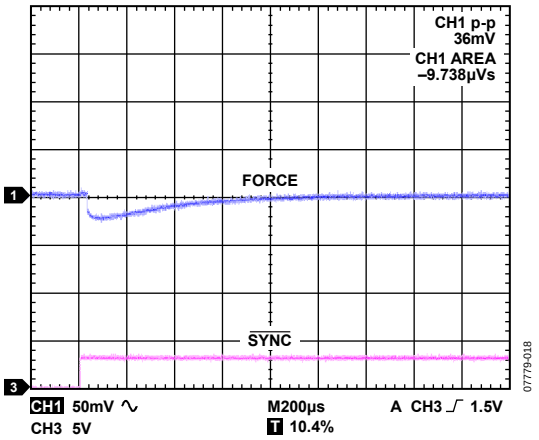


Figure 33. Range Change EXTFORCE2 to 25 mA, Safe Mode, 25 mA I_{LOAD}, 10 µF Load

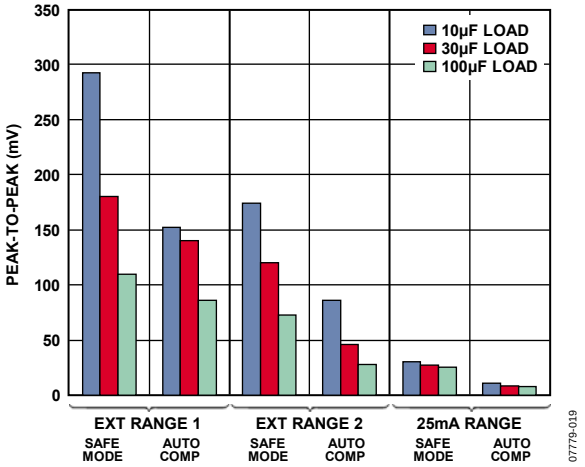


Figure 34. Kick/Droop Response vs. I_{RANGE}, Compensation, and C_{LOAD}, 10% to 90% to 10% I_{LOAD} Change

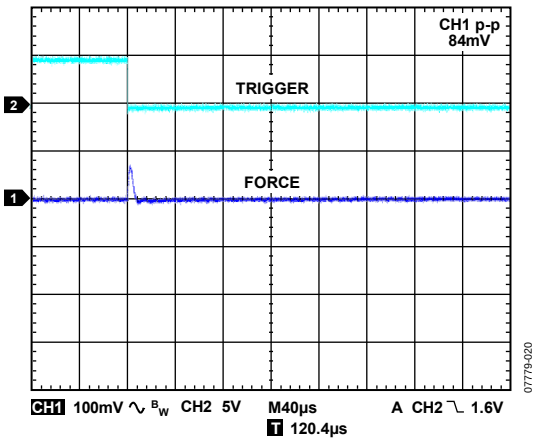


Figure 35. Autocompensation Mode 90% to 10% I_{LOAD} Change, EXTFORCE2 Range, 10 µF Load

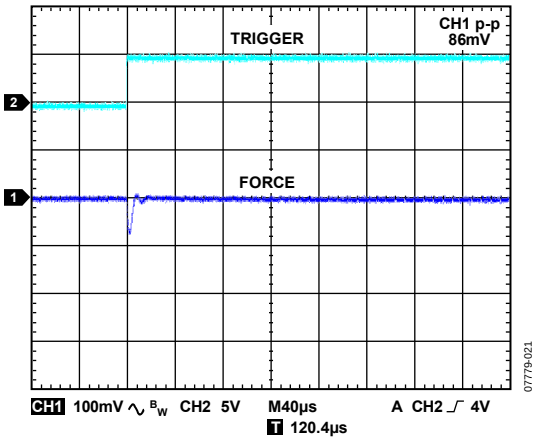


Figure 36. Autocompensation Mode 10% to 90% I_{LOAD} Change, EXTFORCE2 Range, 10 µF Load

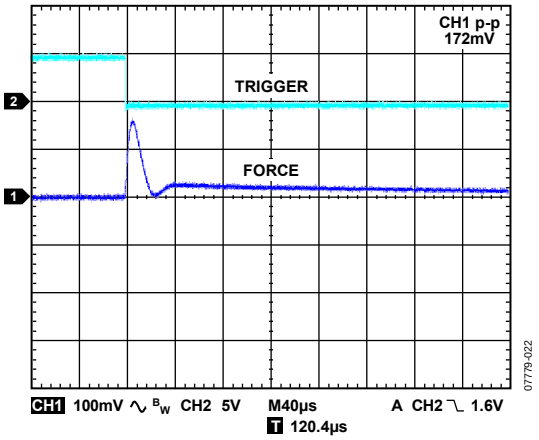


Figure 37. Safe Mode 80% to 10%, EXTFORCE2 Range, 10 µF Load

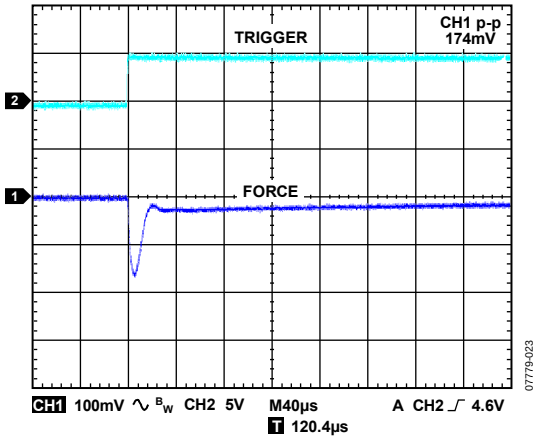


Figure 38. Safe Mode 10% to 90%, EXTFORCE2 Range, 10 µF Load

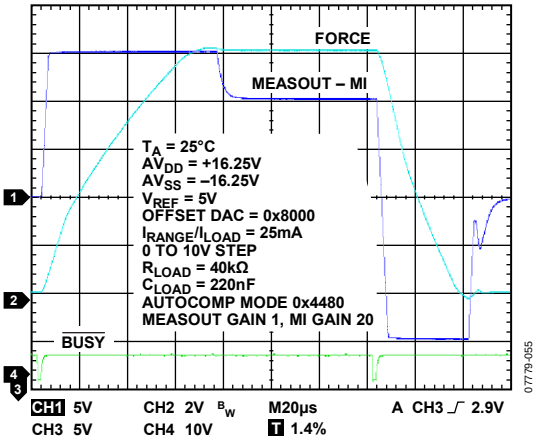


Figure 41. Transient Response FVMI Mode, 25 mA Range, Autocompensation Mode

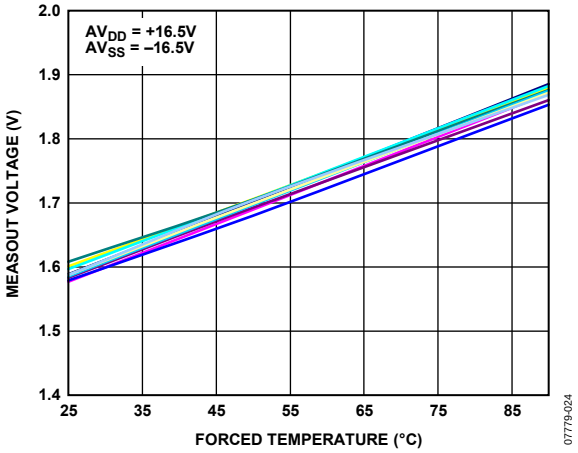


Figure 39. MEASOUT TSENSE Temperature Sensor vs. Temperature (Multiple Devices)

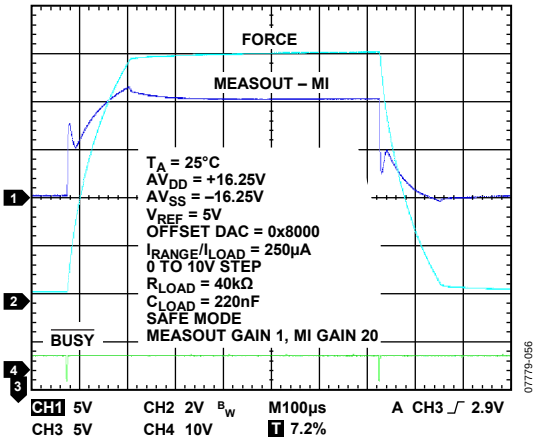


Figure 42. Transient Response FVMI Mode, 25mA Range, Safe Mode

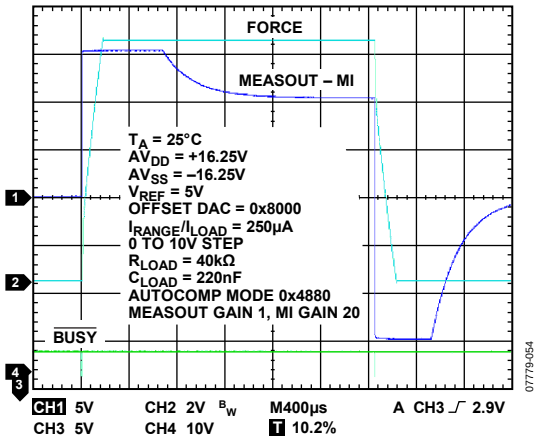


Figure 40. Transient Response FVMI Mode, ±250 µA Range, Autocompensation Mode

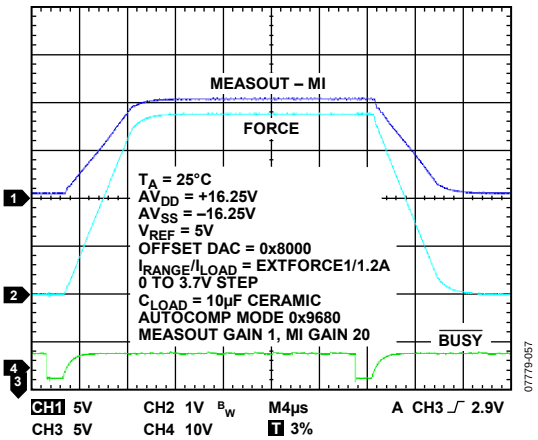


Figure 43. Transient Response FVMI Mode, EXTFORCE1 Range, Autocompensation Mode

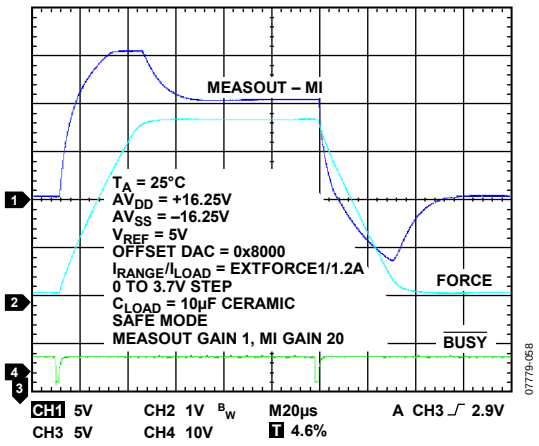


Figure 44. Transient Response FVMI Mode, EXTFORCE1 Range, Safe Mode

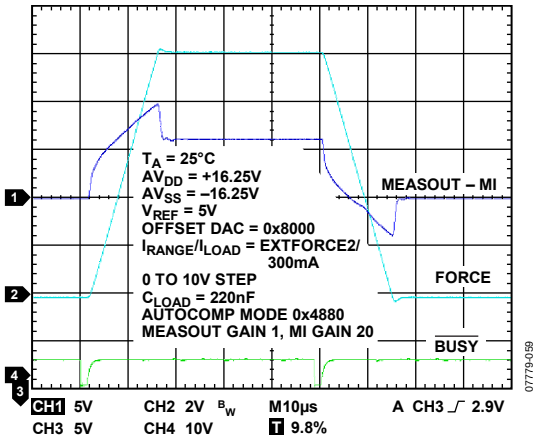


Figure 45. Transient Response FVMI Mode, EXTFORCE2 Range, Autocompensation Mode

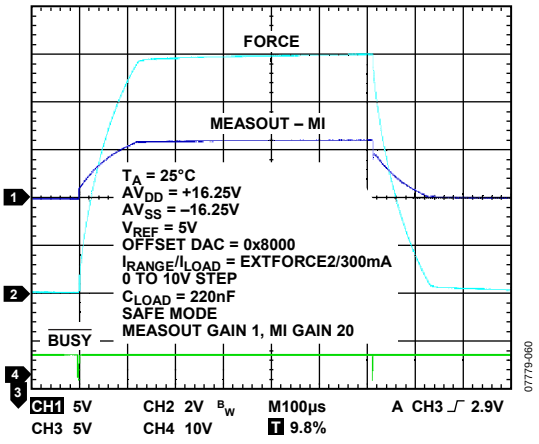


Figure 46. Transient Response FVMI Mode, EXTFORCE2 Range, Safe Mode

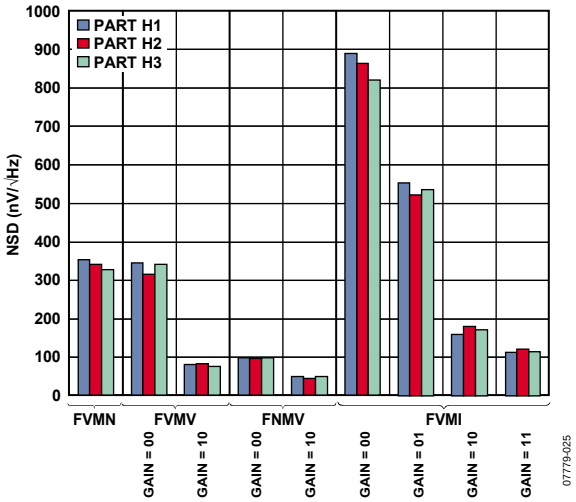


Figure 47. NSD vs. Amplifier Stage and Gain Setting at 1 kHz

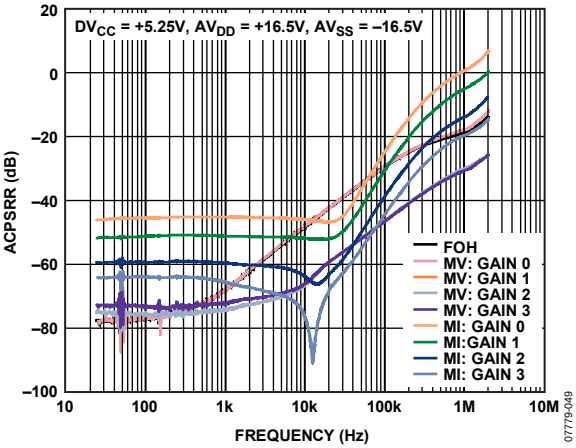


Figure 48. ACPSRR of AV_{DD} vs. Frequency

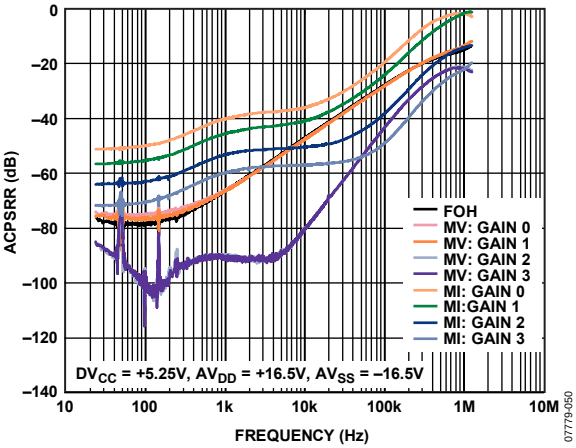


Figure 49. ACPSRR of AV_{SS} vs. Frequency

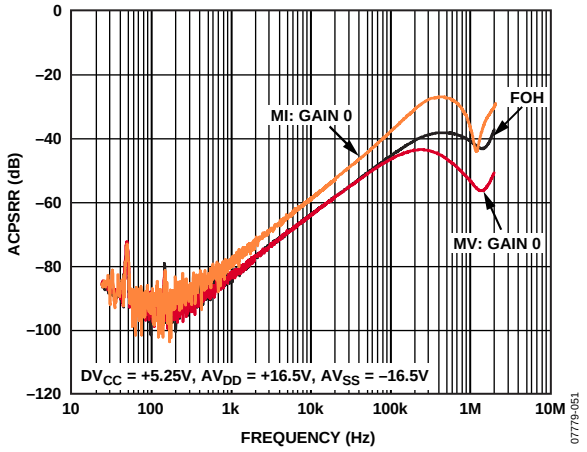


Figure 50. ACPSRR of DV_{CC} vs. Frequency

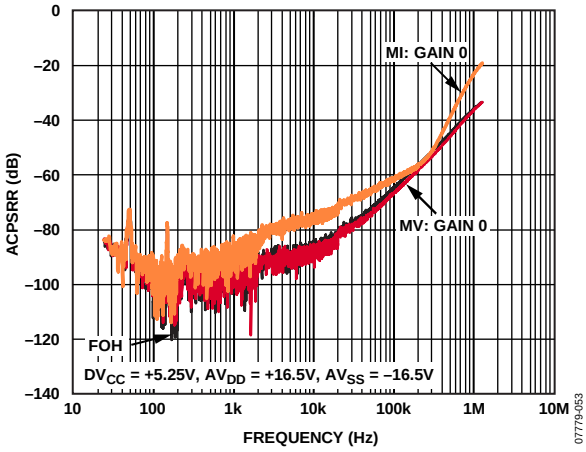


Figure 52. ACPSRR of $HCAV_{SS}x$ vs. Frequency

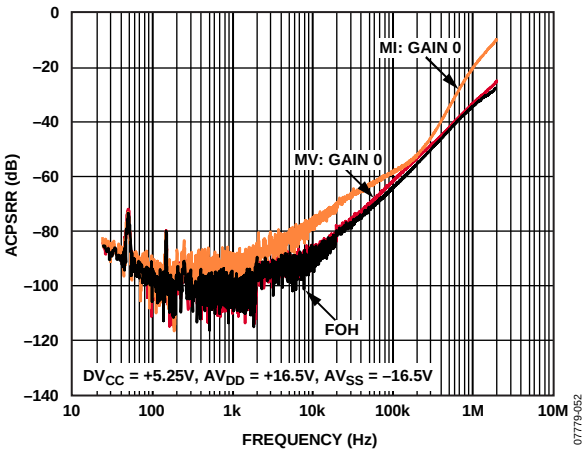


Figure 51. ACPSRR of $HCAV_{DD}x$ vs. Frequency

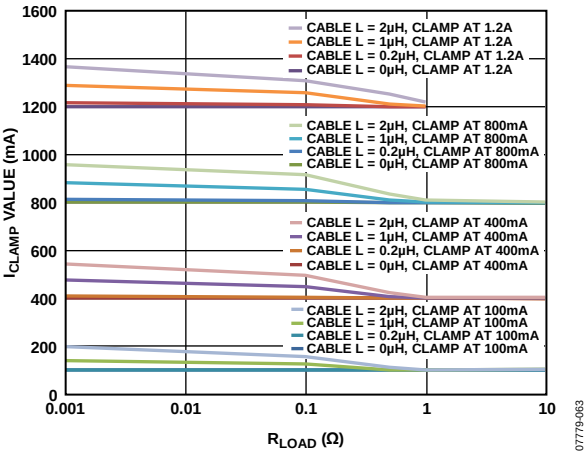


Figure 53. I_{CLAMP} Value vs. R_{LOAD} – Cal at 1Ohm

TERMINOLOGY

Offset Error
Offset error is a measure of the difference between the actual voltage and the ideal voltage at midscale or at zero current expressed in millivolts (mV) or percentage of full-scale range (%FSR).

Gain Error
Gain error is the difference between full-scale error and zero-scale error. It is expressed in percentage of full-scale range (%FSR).

Gain Error = Full-Scale Error – Zero-Scale Error

where:
Full-Scale Error is the difference between the actual voltage and the ideal voltage at full scale.
Zero-Scale Error is the difference between the actual voltage and the ideal voltage at zero scale.

Linearity Error
Linearity error, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the full-scale range. It is measured after adjusting for offset error and gain error and is expressed in millivolts (mV).

Common-Mode (CM) Error
CM error is the error at the output of the amplifier due to the common-mode input voltage. It is expressed in percentage of full-scale voltage range per volt (%FSVR/V).

Clamp Limit
Clamp limit is a measure of where the clamps begin to function fully and limit the clamped voltage or current.

Leakage Current
Leakage current is the current measured at an output pin when the circuit connected to that pin is in high impedance state.

Slew Rate
The slew rate is the rate of change of the output voltage expressed in volts per microsecond (V/µs).

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the amount of energy that is injected into the analog output at the major code transition. It is specified as the area of the glitch in nanovolts per second (nV-sec). It is measured by toggling the DAC register data between 0x7FFF and 0x8000.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is a measure of the part's ability to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.2 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR. It is expressed in decibels (dB).

V_{STRESS}
V_{STRESS} is the stress voltage applied to each pin during leakage testing.

THEORY OF OPERATION

The AD5560 is a single-channel, device power supply for use in semiconductor automatic test equipment. All the DAC levels required to operate the device are available on chip.

This device contains programmable modes to force a pin voltage and measure the corresponding current (FVMI) covering a wide current measure range of up to ±1.2 A. A voltage sense amplifier allows measurement of the DUT voltage. Measured current or voltage is available on the MEASOUT pin.

FORCE AMPLIFIER

The force amplifier is a unity gain amplifier forcing voltage directly to the device under test (DUT). This high bandwidth amplifier allows suppression of load transient induced glitching on the amplifier output. Headroom and footroom requirements for the amplifier are 2.25 V and an additional ±500 mV dropped across the selected sense resistor with full-scale current flowing.

The amplifier is designed to drive high currents up to ±1.2 A with the capability of ganging together outputs of multiple AD5560 devices for currents in excess of ±1.2 A.

The force amplifier can be compensated to ensure stability when driving DUT capacitances of up to 160 µF.

The device is capable of supplying transient currents in excess of ±1.2 A when powering a DUT with a large decoupling capacitor. A clamp enable pin (CLEN) allows disabling of the clamp circuitry to allow the amplifier to quickly charge this large capacitance.

An extra control bit (GPO) is available to switch out DUT decoupling when making low current measurements.

$\overline{\text{HW\_INH}}$ Function

A hardware inhibit pin ($\overline{\text{HW\_INH}}$/$\overline{\text{LOAD}}$) allows disabling of the force amplifier, making the output high impedance. This function is also available through the serial interface (see the $\overline{\text{SW-INH}}$ bit in the DPS Register 1, Address 0x2).

This pin can also be configured as a $\overline{\text{LOAD}}$ function to allow multiple devices to be synchronized. Note that either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ function.

DAC REFERENCE VOLTAGE (VREF)

One analog reference input, VREF, supplies all DAC levels with the necessary reference voltage to generate the required dc levels.

OPEN-SENSE DETECT (OSD) ALARM AND CLAMP

The open-sense detect (OSD) circuitry protects the DUT from overvoltage when the force and sense lines of the force amplifier becoming disconnected from each other.

This block performs three functions related to the force and sense lines.

- It clamps the sense line to within a programmable threshold level (plus a V_{BE}) of the force line, where the programmable threshold is set by the OSD DAC voltage level. This limits the maximum or minimum voltage that can appear on the FORCE pin; it can be driven no higher than [V(F_{IN} DAC) + threshold + V_{BE}] and no lower than [V(F_{IN} DAC) − threshold − V_{BE}].
- It triggers an alarm on $\overline{\text{KELALM}}$ if the force line goes more than the threshold voltage away (OSD DAC level) from the sense line.
- It translates the V(force − sense) voltage to a level relative to AGND so that it can be measured through the MEASOUT pin.

The open-sense detect level is programmable over the range 0.62 V to 5 V (16-bit OSD DAC plus one diode drop). The 5 V OSD DAC can be accessed through the serial interface (see the DAC register addressing portion of Table 24). There is a 10 kΩ resistor that can be connected between the FORCE and SENSE pins by use of SW11. This 10 kΩ resistor is intended to maintain a force/sense connection when a DUT is not in place. It is not intended to be connected when measurements are being made because this defeats the purpose of the OSD circuit in identifying an open circuit between FORCE and SENSE. In addition, the sense path has a 2.5 kΩ resistor in series; therefore, if the 10 kΩ switch is closed, errors may become apparent when in high current ranges.

DEVICE UNDER TEST GROUND (DUTGND)

DUTGND is the ground level of the DUT.

DUTGND Kelvin Sense

$\overline{\text{KELALM}}$ flags when the voltage at the DUTGND pin moves too far away from the AGND line (>1 V default setting of the DGS DAC). This alarm trigger is programmable via the serial interface. The threshold for the alarm function is programmable using the DUTGND SENSE DAC (DGS DAC) (see Table 24).

The DUTGND pin has a 50 µA pull-up resistor that allows the alarm function to detect whether DUTGND is open. Setting the disable $\overline{\text{DUTALM}}$ bit high (Register 0x6, Bit 10) disables the 50 µA pull-up resistor and also disables the alarm feature. The alarm feature can also be set to latched or unlatched (Register 0x6, Bit 11).

Kelvin Alarm ($\overline{\text{KELALM}}$)

The open-drain active low Kelvin alarm pin flags the user when an open occurs in either the sense or DUTGND line; it can be programmed to be either latched or unlatched (Register 0x6, Bit 13, Bit 11, Bit 7). The delay in the alarm flag is 50 µs.

GPO

The GPO pin can be used as an extra control bit for external switching functions, such as for switching out DUT decoupling when making low current measurements.

The GPO pin is also internally connected to an array of thermal diodes scattered across the AD5560. The diagnostic register

(Address 0x7) details the addressing and location of the diodes. These can be used for diagnostic purposes to determine the thermal gradients across the die and across a board containing many AD5560 devices. When selected, the anode of these diodes is connected to GPO and the cathode to AGND. The AD5560 evaluation board uses the ON Semiconductor® ADT7461 temperature sensor for the purpose of analyzing the temperature at different points across the die.

COMPARATORS

The DUT measured value is monitored by two comparators (CPOL, CPOH). These comparators give the advantage of speed for go-no-go testing.

Table 6. Comparator Output Function

Test Condition	CPOL	CPOH
(V_{DUT} or I_{DUT}) > CPH		0
(V_{DUT} or I_{DUT}) < CPH		1
(V_{DUT} or I_{DUT}) > CPL	1	
(V_{DUT} or I_{DUT}) < CPL	0	
CPH > (V_{DUT} or I_{DUT}) > CPL	1	1

To minimize the number of comparator output lines routed back to the controller, it is possible to change the comparator function to a window comparator that outputs on one single pin, CPO. This pin is shared with CPOH and, when configured through the serial interface, it provides information on whether the measured DUT current or voltage is inside or outside the window set by the CPL and CPH DAC levels (see Table 24).

Table 7. Comparator Output Function in CPO Mode

Test Condition	CPO Output
(V_{DUT} or I_{DUT}) > CPL and < CPH	1
(V_{DUT} or I_{DUT}) < CPL or > CPH	0

CURRENT CLAMPS

High and low current clamps are included on chip. These protect the DUT in the event of a short circuit. The CLH and CLL levels are set by the 16-bit DAC levels. The clamp works to limit the current supplied by the force amplifier to within the set levels. The clamp circuitry compares the voltage across the sense resistor (multiplied by an in-amp gain of 10 or 20) to compare to the programmed clamp limit and activates the clamp circuit if either the high level or low level is exceeded, thus ensuring that the DUT current can never exceed the programmed clamp limit + 10% of full-scale current.

If a clamp level is exceeded, this is flagged via the latched open-drain $\overline{\text{CLALM}}$ pin, and the resulting alarm information can be read back via the SPI interface.

The clamp levels should not be set to the same level; instead, they should be set a minimum of 2 V apart (irrespective of the MI gain setting). This equates to 10% of FSCR (MI gain = 20) (20% of FSCR, MI gain of 10) apart. They should also be 1 V away from the 0 A level.

The clamp register limits the CLL clamp to the range 0x0000 to 0x7FFF; any code in excess of this is seen as 0x7FFF. Similarly, the CLH clamp registers are limited to the range 0x8000 to 0xFFFF (see Table 24).

Clamp Alarm Function ($\overline{\text{CLALM}}$)

The $\overline{\text{CLALM}}$ open-drain output flags the user when a clamp limit has been hit; it can be programmed to be either latched or unlatched.

Clamp Enable Function (CLEN/$\overline{\text{LOAD}}$)

Pin 15 (CLEN) allows the user to disable the clamping function when powering a device with large DUT capacitance, thus allowing increased current drive to the device and, therefore, speeding up the charging time of the load capacitance. CLEN is active high.

This pin can also be configured as $\overline{\text{LOAD}}$ to allow multiple devices to be synchronized. Note that either CLEN or $\overline{\text{HW\_INH}}$ can be chosen as a $\overline{\text{LOAD}}$ function.

SHORT-CIRCUIT PROTECTION

The AD5560 force amplifier stage has built-in short-circuit protection per stage as noted in the Specifications section. When the current clamps are disabled, the user must minimize the duration of time that the device is left in a short-circuit condition (for all current ranges).

GUARD AMPLIFIER

A guard amplifier allows the user to force the shield of the coaxial cable to be driven to the same forced voltage at the DUT, ensuring minimal voltage drops across the cable to minimize errors from cable insulation leakage.

The guard amplifier also has an alarm function that flags the open-drain $\overline{\text{KELALM}}$ pin when the guard output is shorted. The delay in the alarm flag is 200 µs.

The guard amplifier output (GUARD/SYS_DUTGND, Pin 43) can also be configured to function as a SYS_DUTGND pin; to do this, the guard amplifier must be tristated via software (see DPS Register 2, Table 19).

COMPENSATION CAPACITORS

The force amplifier is capable of driving DUT capacitances up to 160 µF. Four external compensation capacitor (C_{Cx}) inputs are provided to ensure stability into the maximum load capacitance while ensuring that settling time is optimized. In addition, five C_{Fx} capacitor inputs are provided to switch across the sense resistors to further optimize stability and settling time performance. The AD5560 has three compensation modes: safe mode, autocompensation mode, and manual compensation mode, all of which are described in more detail in the Force Amplifier Stability section.

The range of suggested compensation capacitors allows optimum performance for any capacitive load from 0 pF to 160 µF using one of the modes previously listed.

Although there are four compensation input pins and five feed-forward capacitor inputs pins, all capacitor inputs may be used only if the user intends to drive large variations of DUT load capacitances. If the DUT load capacitance is known and does not change for all combinations of voltage ranges and test conditions, then it is possible only one set of C_{Cx} and C_{Fx} capacitors may be required.

Table 8. Suggested Compensation Capacitor Selection

Capacitor	Value
C_{C0}	100 pF
C_{C1}	100 pF
C_{C2}	330 pF
C_{C3}	3.3 nF
C_{F0}	4.7 nF
C_{F1}	22 nF
C_{F2}	100 nF
C_{F3}	470 nF
C_{F4}	2.2 µF

The voltage range for the C_{Cx} and C_{Fx} pins is the same as the voltage range expected on FORCE; therefore, choice of capacitors should take this into account. C_{Fx} capacitors can have 10% tolerance; this extra variation directly affects settling times, especially when measuring current in the low current ranges. Selection of C_{Cx} should be at ≤5% tolerance.

CURRENT RANGE SELECTION

Integrated thin film resistors minimize external components and allow easy selection of current ranges from ±5 µA to ±25 mA. Using external current sense resistors, two higher current ranges are possible: EXTFORCE1 can drive currents up to ±1.2 A, while EXTFORCE2 is designed to drive currents up to ±500 mA. The voltage drop across the selected sense resistor is ±500 mV when full-scale current is flowing through it.

The measure current amplifier has two gain settings, 10 and 20. The two gain settings allow users to achieve the quoted/specified current ranges with large or small voltage swings. The gain of 20 setting is intended for use with a 5 V reference, and the gain of 10 setting is for use with a 2.5 V reference. Both combinations ensure the specified current ranges. Other VREF/gain setting combinations should only be used to achieve smaller current ranges. Attempting to achieve greater current ranges than the specified ranges is outside the intended operation of the AD5560. The maximum guaranteed voltage across R_{SENSE} is ±0.64 V (gain of 20) or ±0.7 V (gain of 10).

HIGH CURRENT RANGES

For currents in excess of 1200 mA, a gang mode is available whereby multiple devices are ganged together to achieve higher currents. In gang mode, the loop is controlled by the master AD5560. This loop drives a maximum capacitance of 160 µF for this mode. There are two methods of ganging channels together; these are described in the Master and Slaves in Force Voltage (FV) Mode section and the Master in FV Mode, Slaves in Force Current (FI) Mode section.

Master and Slaves in Force Voltage (FV) Mode

All devices are placed in force voltage (FV) mode. One device acts as the master device and the other devices act as slaves. By connecting in this manner, any device can be configured as the master. Here, the MASTER_OUT pin of the master device is connected to the output of the force amplifier, and it feeds the inputs of each slave force amplifier (via the SLAVE_IN pin). All devices are connected externally to the DUT. For current to be shared equally, there must be good matching between each of the paths to the DUT. Settings for DPS Register 2 are master = 0x0000, slave = 0x0400. Clamps should be disabled in the slave devices.

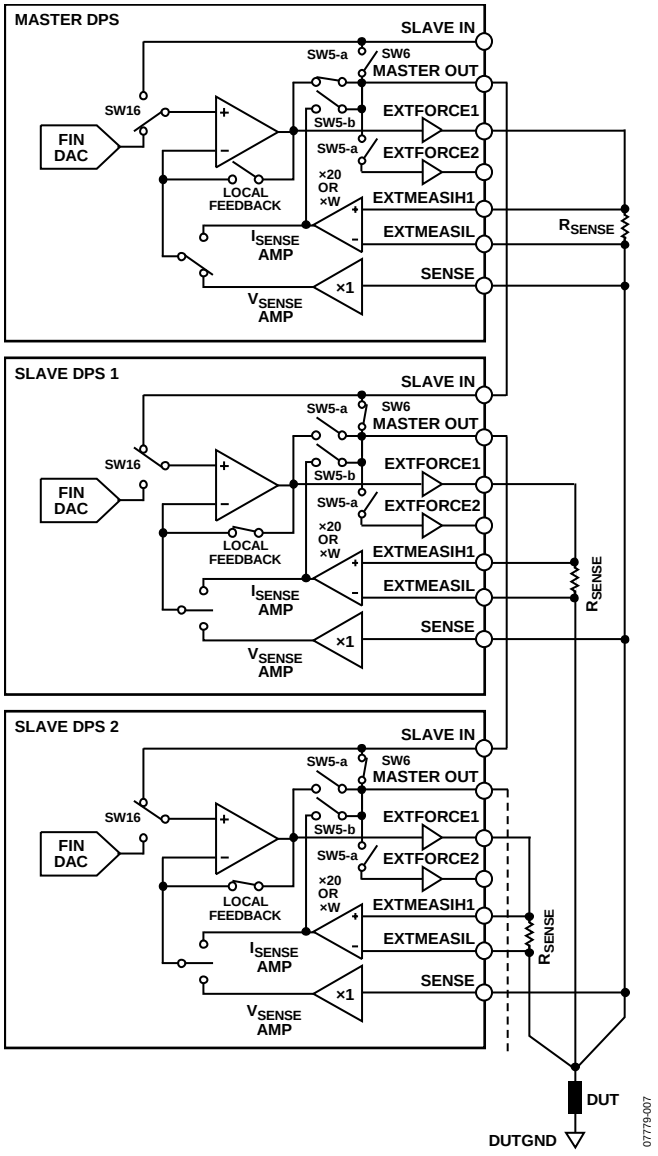


Figure 54. Simplified Block Diagram of High Current Ganging Mode

Master in FV Mode, Slaves in Force Current (FI) Mode

The master device is placed into FV mode, and all slave devices into force current (FI) mode. The measured current of the master device (MASTER_OUT) is applied to the input of all slave devices (SLAVE_IN), and the slaves act as followers. All channels work to share the current equally among all devices in the gang. Because the slaves force current, matching the DUT paths is not so critical. Settings for DPS Register 2 are master = 0x0200, slave = 0x0600. Clamps should be disabled in the slave devices.

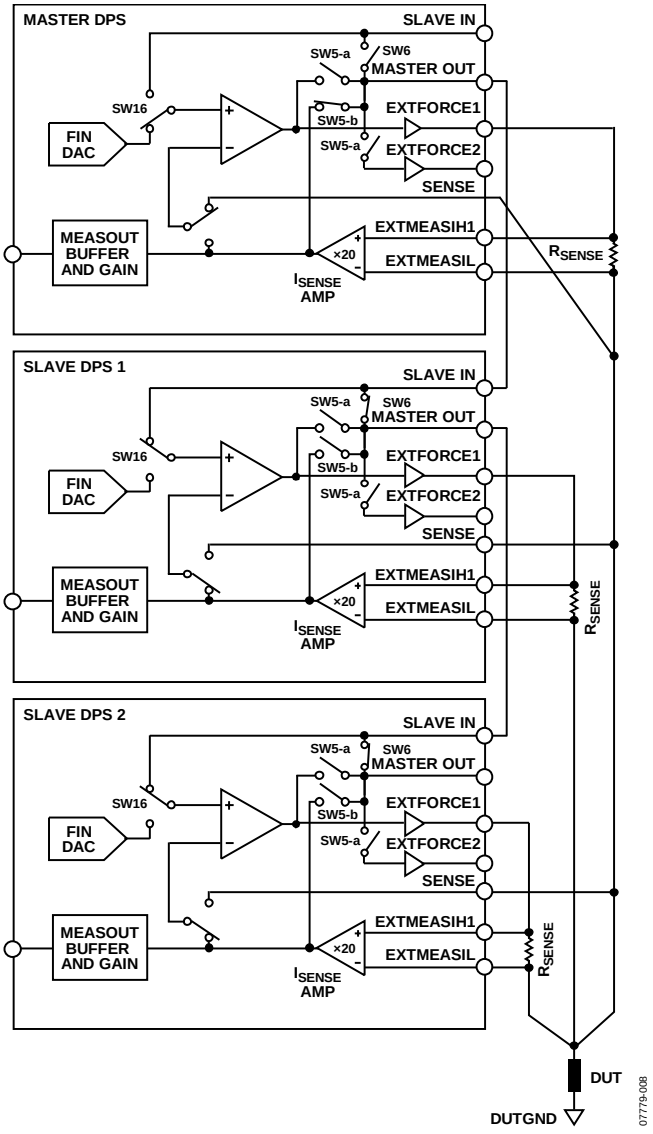


Figure 55. Simplified Block Diagram of Gang Mode, Using an FV/FI Combination

The EXTFORCE1, EXTFORCE2, or ±25 mA ranges can be used for the gang mode. Therefore, it is possible to gang devices to get a high voltage/high current combination, or a low voltage/high current combination.

For example, ganging five 25 V/25 mA devices using the 25 mA range achieves a 25 V/625 mA range, whereas five 15 V/200 mA devices using the EXTFORCE2 path can achieve a 15 V/1 A range. Similarly, ganging four 3.5 V/1.2 A devices using the EXTFORCE1 path results in a 3.5 V/4.8 A DPS.

IDEAL SEQUENCE FOR GANG MODE

Use the following steps to bring devices into and out of gang mode:

1. Choose the master device and force 0 V output, corresponding to zero current.
2. Select slave DPS 1 and place it in slave mode (keep slaves in high-Z mode via $\overline{\text{SW-INH}}$ or $\overline{\text{HW\_INH}}$ until ready to gang).
3. Select to gang in either current or voltage mode.
4. Repeat Step 2 and Step 3 one at a time through the chain of slaves.
5. Load the required voltage to the master device. The other devices copy either voltage or current as programmed.

To remove devices from the gang, the master device should be programmed to force 0 V out again. The procedure for removing devices should be the reverse of Step 1 through Step 5.

Note that this may not always be possible in practice; therefore, it is also possible to gang and ungang while driving a load. Just ensure that the slave devices are in high-Z mode while configuring them into the required range and gang setting.

Gang mode extends only to the ±25 mA range and the two high current ranges, EXTFORCE1 and EXTFORCE2. Therefore, where an accurate measurement is required at a low current, the user should remove slaves from the gang to move to the appropriate lower current range to make the measurement. Similarly, slaves can be brought back into the gang if needed.

COMPENSATION FOR GANG MODE

When ganging, the slave devices should be set to the fastest response.

When slaves are in FI mode, the AD5560 force amplifier overrides other compensation settings to enforce $C_{Fx} = 0$, $R_Z = 0$, and $g_{mx} \leq 1$. This is done internally to the force amplifier; therefore, readback does not show that the signals inside the force amplifier actually change.

SYSTEM FORCE/SENSE SWITCHES

System force/sense switches allow easy connection of a central or system parametric measurement unit (PMU) for calibration or additional measurement purposes.

The system device under test ground (SYS_DUTGND) switch is shared with the GUARD/SYS_DUTGND pin (Pin 43). See the DPS Register 2 in Table 19 for addressing details.

DIE TEMPERATURE SENSOR AND THERMAL SHUTDOWN

There are three types of temperature sensors in the AD5560.

- The first is a temperature sensor available on the MEASOUT pin and expressed in voltage terms. Nominally at 25°C, this sensor reads 1.54 V. It has a temperature coefficient of 4.7 mV/°C. This sensor is active during power-down mode.

  $Die\ Temp = (VMEASOUT_{(TSENSE)} - 1.54)/0.0047 + 25°C$

  Based on typical temperature sensor output voltage at 25°C and output scaling factor.

- The second type of temperature sensor is related to the thermal shutdown feature in the device. Here, there are sensors located in the middle of the enabled power stage, which are used to trip the thermal shutdown. The thermal shutdown feature senses only the power stages, and the power stage that it senses is determined by the active stage.

  If ranges of <25 mA are selected, the EXTFORCE1 sensor is monitored. The EXTFORCE1 power stage itself is made up of three identical stages, but the thermal shutdown is activated by only one stage (EXTFORCE1B). Similarly, the EXTFORCE2 stage is made up of two identical output stages, but the thermal shutdown can be activated by only one stage (EXTFORCE2A).

  The thermal shutdown circuit monitors these sensors and, in the event of the die temperature exceeding the programmable threshold temperature (100°C, 110°C, 120°C, 130°C (default)), the device protects itself by inhibiting the force amplifier stage, clearing $\overline{\text{SW-INH}}$ in DPS Register 1 and flagging the overtemperature event via the open-drain $\overline{\text{TMPALM}}$ pin, which can be programmed to be either latched or unlatched. These temperature sensors can be read via the MEASOUT pin by selecting them in the diagnostic register (Table 23, VPTAT low and VPTAT high). They are expressed in voltage and to scale to temperature. They must be referred to the VTSD reference voltage levels (see Table 23) also available on MEASOUT. This set of sensors is not active in power-down mode.

  $Die\ Temp\_y = \{(VPTAT\_x - VTSD\_low)/[(VTSD\_high - VTSD\_low)/(Temp\_high - Temp\_low)]\} + Temp\_low$

  where:
  x, *y* are (high, NPN) and (low, PNP).
  Temp_low = −273°C.
  Temp_high = +130°C.

- The third set of temperature sensors is an array of thermal diodes scattered across the die. These diodes allow the user to evaluate the temperature of different parts of the die and are of great use to determine the temperature gradients across the die and the temperature of the accurate portions of the die when the device is dissipating high power. For further details on the thermal array and locations, see the diagnostic register section in Table 23.

  These diodes can be muxed out onto the GPO pin. The diagnostic register (Address 0x7) details the addressing and location of the diodes. These can be used for diagnostic purposes to determine the thermal gradients across the die and across a board containing many AD5560 devices. When selected, the anode of each diode is connected to GPO and the cathode to AGND. The AD5560 evaluation board uses the ON Semiconductor ADT7461 temperature sensor for the purpose of analyzing the temperature at different points across the die.

Note that, when a thermal shutdown occurs, as the force amplifier is inhibited or tristated, user intervention is required to reactivate the device. It is necessary to clear the temperature alarm flag by issuing a read command of Register Address 0x44 (alarm status and clear alarm status register, Table 25), and then issuing a new write to the DPS Register 1 ($\overline{\text{SW-INH}}$ = 1) to reenable the force amplifier.

See also the Thermal Considerations section.

MEASURE OUTPUT (MEASOUT)

The measured DUT voltage, current (voltage representation of DUT current), K_{SENSE}, or die temperature is available on MEASOUT with respect to AGND. The default MEASOUT range is the forced voltage range for voltage measure and current measure (nominally ±12.81 V, depending on reference voltage and offset DAC) and includes overrange to allow for system error correction.

The serial interface allows the user to select another MEASOUT range of (1.025 × VREF) to AGND; this range is suitable for use with an ADC with a smaller input range.

To allow for system error correction, there is additional gain for the force function. If this overrange is used as intended, the output range on MEASOUT scales accordingly.

The MEASOUT line can be tristated via the serial interface.

When using low supply voltages, ensure that there is sufficient headroom and footroom for the required force voltage range.

V_{MID} VOLTAGE

The midcode voltage (V_{MID}) is used in the measure current amplifier block to center the current ranges at about 0 A. This is required to ensure that the quoted current ranges can be achieved when using offset DAC settings other than the default. V_{MID} corresponds to 0x8000 or the DAC midcode value, that is, the middle of the voltage range set by the offset DAC setting (see Table 15 and Figure 56).

$$V_{MID} = 5.125 \times VREF \times (32{,}768/2^{16}) - (5.125 \times VREF \times (OFFSET\_DAC\_CODE/2^{16}))$$

or

$$V_{MID} = 5.125 \times VREF \times ((32{,}768 - Offset\ DAC)/2^{16})$$

V_{MIN} is another important voltage level that is used in other parts of the circuit. When using a MEASOUT gain of 0.2, the V_{MIN} level is used to scale the voltage range; therefore, when choosing supply rails, it is very important to ensure that there is sufficient footroom so that the V_{MIN} level is not impinged on (the high voltage DAC amplifiers used here require approximately 2 V footroom to AV_{SS}). See the Choosing AVDD/AVSS Power Supply Rails section for more information.

$$V_{MIN} = -5.125 \times VREF \times (OFFSET\_DAC\_CODE/2^{16})$$

Table 9. MEASOUT Output Ranges

MEASOUT Function GAIN1 = 0, MEASOUT Gain = 1			Transfer Function	Output Voltage Range[1]		
				Offset DAC = 0x0	Offset DAC = 0x8000	Offset DAC = 0xE000
Measure Voltage (MV)			$\pm V_{DUT}$	0 V to 25.62 V	±12.81 V	−22.42 V to +3.2 V
Measure Current (MI)	GAIN0 = 0	MI gain = 20	$(I_{DUT} \times R_{SENSE} \times 20) + V_{MID}$	0 V to 25.62 V	±12.81 V	−22.42 V to +3.2 V
	GAIN0 = 1	MI gain = 10	$(I_{DUT} \times R_{SENSE} \times 10) + V_{MID}$	0 V to 12.81 V (V_{REF} = 2.5 V)	±6.4 V (V_{REF} = 2.5 V)	−11.2 V to +1.6 V (V_{REF} = 2.5 V)

[1] VREF = 5 V, unless otherwise noted.

Table 10.

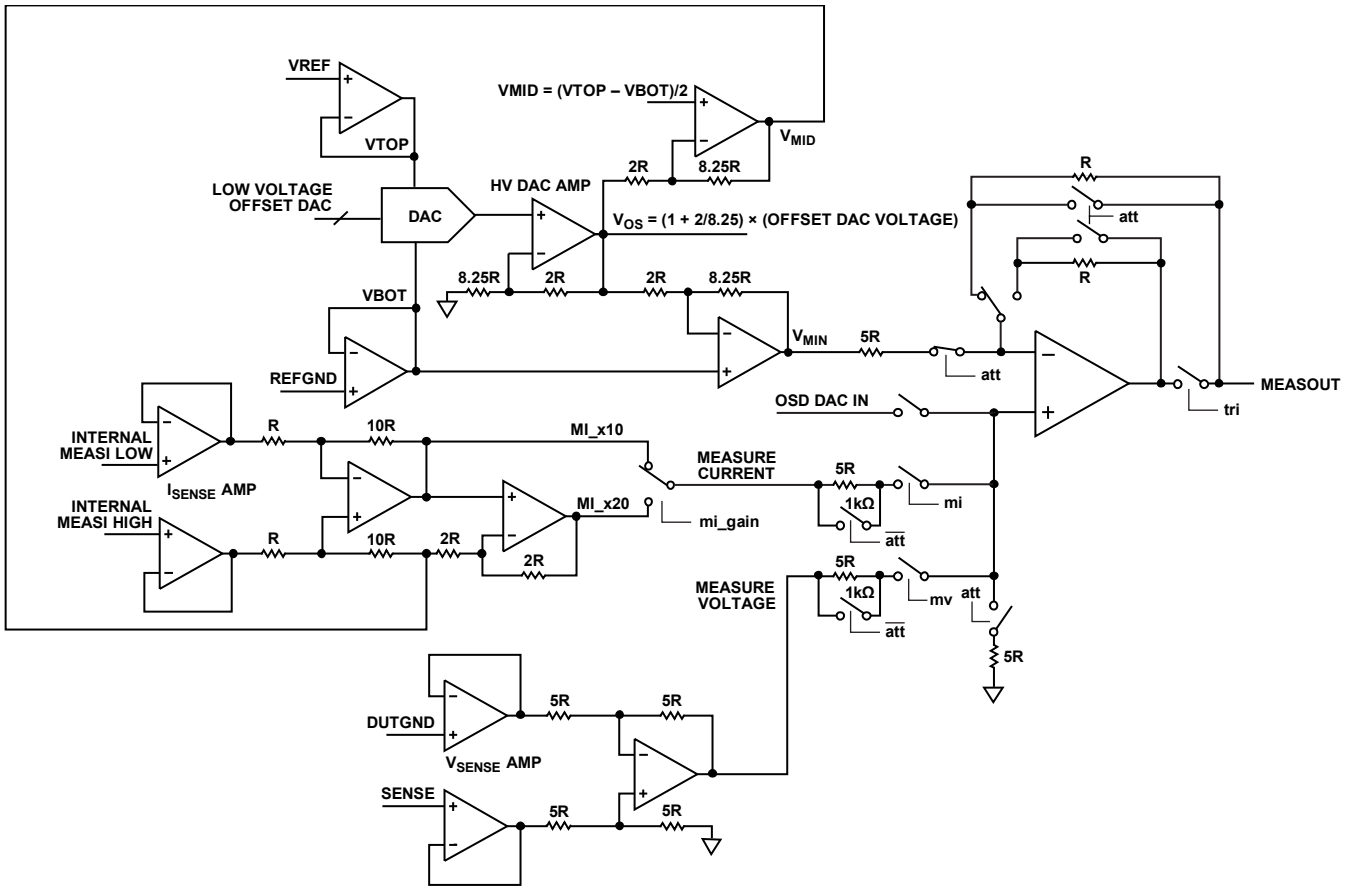
MEASOUT Function GAIN1 = 1, MEASOUT Gain = 0.2			Transfer Function	Output Voltage Range[1, 2]
Measure Voltage (MV)			$MV = 0.2 \times (V_{DUT} - V_{MIN})$	0 V to 5.12 V (±2.56 V centered around 2.56 V) (includes overrange)
Measure Current (MI)	GAIN0 = 0	MI gain = 20	$(I_{DUT} \times R_{SENSE} \times 20 \times 0.2) + 0.5125 \times VREF$	0 V to 5.12 V (±2.56 V centered around 2.56 V) (includes overrange)
	GAIN0 = 1	MI gain = 10	$(I_{DUT} \times R_{SENSE} \times 10 \times 0.2) + 0.5125 \times VREF$	1.28 V to 3.84 V (±1.28 V, centered around 2.56 V)
				0 V to 2.56 V (±1.28 V, centered around 1.28 V) (V_{REF} = 2.5 V)

[1] VREF = 5 V, unless otherwise noted.
[2] The offset DAC setting has no effect on the output voltage range.

Table 11. Possible ADCs and ADC Drivers for Use with AD5560[1]

Part No.	Resolution	Sample Rate	Channels	AIN Range[2]	Interface	ADC Driver	Multiplexer[3]	Package
AD7685	16	250 kSPS	1	0 V to VREF	Serial, SPI	ADA4841-1, ADA4841-2,	ADG704, ADG708	MSOP, LFCSP
AD7686	16	500 kSPS	1	0 V to VREF	Serial, SPI	ADA4841-1, ADA4841-2,	ADG704, ADG708	MSOP, LFCSP
AD7693	16	500 kSPS	1	−VREF to +VREF	Serial, SPI	ADA4841-1, ADA4841-2, ADA4941-1	ADG1404, ADG1408, ADG1204	MSOP, LFCSP
AD7610	16	250 kSPS	1	Bipolar 10 V, bipolar 5 V, unipolar 10 V, unipolar 5 V	Serial, parallel	AD8021	ADG1404, ADG1408, ADG1204	LFCSP, LQFP
AD7655	16	1 MSPS	4	0 V to 5 V	Serial, SPI	ADA4841-1, ADA4841-2, AD8021		LQFP, LFCSP

[1] Subset of the possible ADCs, ADC drivers, and multiplexers suitable for use with the AD5560. Visit http://www.analog.com for more options.
[2] Do not allow the MEASOUT output range to exceed the AIN range of the ADC.
[3] For the purposes of sharing ADCs among multiple DPS channels, note that the multiplexer is not absolutely necessary because the AD5560 MEASOUT path has a tristate mode.



NOTES

1. att: ATTENUATION FOR EXTERNAL MEASOUT × 0.20 FOR OUTPUT VOLTAGE RANGE 0V TO 5.125V (WITH OVERRANGE) (VREF = 5V).
   tri: TRISTATE MODE
   mv: MEASURE VOLTAGE
   mi: MEASURE CURRENT
   mi_gain: MEASURE I GAIN SELECTION

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Figure 56. MI, MV, and MEASOUT Block Showing Gain Settings and Offset DAC Influence

FORCE AMPLIFIER STABILITY

There are three modes for configuring the force amplifier: safe mode, autocompensation mode, and manual compensation mode. Manual compensation mode has highest priority, followed by safe mode, then autocompensation mode.

Safe Mode

Selected through Compensation Register 1 (see Table 20), this mode guarantees stability of the force amplifier under all conditions. Where the load is unknown, this mode is useful but results in a slow response. This is the power-on default of the AD5560.

Autocompensation Mode

Using this mode, the user inputs the C_R and ESR values, and the AD5560 decides the most appropriate compensation scheme for these load conditions. The compensation chosen is for an optimum tradeoff between ac response and stability.

Manual Compensation Mode

This mode allows access to all of the internal programmable parameters to configure poles/zeros, which affect the dynamic performance of the loop. These variables are outlined in Table 12 and Table 13.

Figure 57 shows more details of the force amplifier block.

Table 12. External Variables

Name	Description	Min	Max
C_R	DUT capacitance with contributing ESR	10 nF	160 µF
R_C	ESR in series with C_R	1 mΩ	10 Ω
C_D	DUT capacitance with negligible ESR	100 pF	10 nF
R_D	Loading resistance at the DUT	~2 Ω	Infinity
I_R	Current range	±5 µA	±1.2 A

Table 13. Internal Variables

Name	Description	Min	Max
R_Z	Resistor in series with C_{C0}, which contributes a zero.	500 Ω	1.6 MΩ
R_P	Resistor to 8 pF to contribute an additional pole	200 Ω	1 MΩ
C_{C0}:C_{C3}	Capacitors to ensure unconditional stability	100 pF	100 nF
C_{F0}:C_{F4}	Capacitors to optimize ac performance into different C_R, C_D	4.7 nF	10 µF
g_{mx}	Transconductance of force amplifier input stage	40 µA/V	900 µA/V

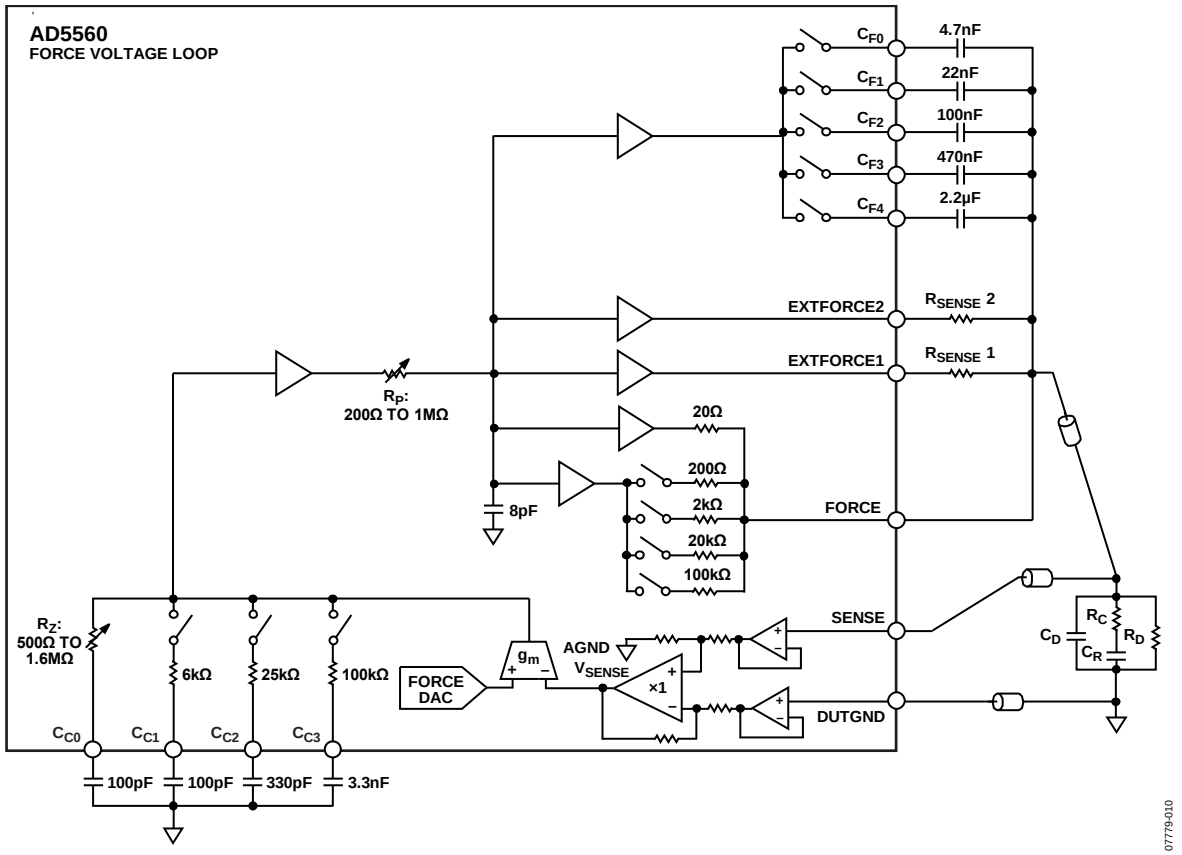

Figure 57. Block Diagram of a Force Amplifier Loop

POLES AND ZEROS IN A TYPICAL SYSTEM

Typical closed loop systems have one dominant pole in the feedback path, providing −20 dB/decade gain roll off and 90° of phase shift so that the gain decreases to 0 dB where there is a conservative 90° of phase margin.

The AD5560 has compensation options to help cope with the various load conditions that a DPS is presented with.

MINIMIZING THE NUMBER OF EXTERNAL COMPENSATION COMPONENTS

Note that, depending on the range of load conditions, not all external capacitors are required.

C_{Fx} Pins

There are five external C_{Fx} pins. All five pins are used in the autocompensation mode to choose a suitable capacitor, depending on the load being driven. To reduce component count, it is possible to connect just one capacitor, for instance, C_{F2} to the C_{F2}, C_{F1}, and C_{F0} pins. Therefore, when any of the smallest three external capacitors are selected, the same physical capacitor is used because it is connected to all three pins. A disadvantage here is that the larger C_{F2} capacitor should be bigger than optimal and may increase settling time of the whole circuit (particularly the measure current).

C_{Cx} Pins

To make the AD5560 stable with any unknown capacitor from 0 pF to 160 µF, all four C_{Cx} capacitors are required. However, if the range of load is from 0 pF to 20 µF, then C_{C3} can be omitted. Similarly, if the load range is from 0 pF to 2.2 µF, then C_{C2} and C_{C3} can be omitted. Only C_{C0} is required in autocompensation mode.

Note that safe mode, which makes the device stable in any load from 0 pF to 160 µF, simply switches in all of the four C_{Cx} capacitors. Stability into 160 µF is assured only if all four capacitors are present; otherwise, the maximum capacitor for stability is reduced to 20 µF, 2.2 µF, or 220 nF, depending on how many capacitors are missing.

EXTRA POLES AND ZEROS IN THE AD5560

The Effect of C_{Cx}

C_{C0} is switched on at all times. C_{C3}, C_{C2}, and C_{C1} can be connected in addition to C_{C0} to slow down the force amplifier loop. In the ±500 mA range looking into a small load capacitor, with only C_{C0} connected, the ac gain vs. phase response results in ~90° of phase margin and a unity gain bandwidth (UGB) of ~400 kHz.

The Effect of C_{Fx}

The output of the AD5560 passes through a sense resistor to the DUT. Coupled with the load capacitor, this sense resistor can act as a low-pass filter that adds phase shift and decreases phase margin (particularly in the low current ranges where the sense resistors are large).

Placing a capacitor in parallel with this sense resistor provides an ac feedforward path to the DUT. Therefore, at high frequencies, the DUT is driven through the C_{Fx} capacitor rather than through the sense resistor.

Note that each C_{Fx} output has an output impedance of about 3 Ω. This is very small compared to the sense resistors of the low current ranges but not so for the highest current ranges. Therefore, the C_{Fx} capacitors are most effective in the low current ranges but are of lesser benefit in higher current ranges.

As shown in the force amplifier diagram (see Figure 57), there is a pole at $1/(R_{SENSE} \times [C_{Fx} + C_R])$ and a zero at $1/[R_{SENSE} \times C_{Fx}]$. Therefore, the output impedance of each C_{Fx} output, at around 1 Ω, limits the improvement available by using the C_{Fx} capacitors. For a large load capacitance, there is still a pole at $-1/[1\ \Omega \times CR]$ above which the phase improvement is lost. If there is also a cable resistance to the DUT, or if C_{Fx} has significant ESR, this should be added to the 1 Ω to calculate the pole frequency.

If C_{Fx} is chosen to be bigger than the load capacitance, it can dominate the settling time and slow down the settling of the whole circuit. Also, it directly affects the time taken to measure a current ($R_{SENSE} \times C_{Fx}$).

The Effect of R_Z

When the load capacitance is known, R_Z can be used to optimize the response of the AD5560. Because the C_{Fx} buffers have some output impedance of about 1 Ω, there is likely to be some additional resistance to the DUT. There can still be an output pole associated with this resistance and the load capacitance, C_R, $1/[R_0 \times C_R]$ (where R_0 = the series/parallel combination of the sense resistor, the C_{Fx} output impedance, the C_{Fx} capacitor ESR, and the cable to DUT). This is particularly significant for larger load capacitances in any current range. By programming a zero into the loop response by setting R_Z (in series with C_{C0}), it is possible to cancel this pole. Above the frequency $1/[C_{C0} \times R_Z]$, the series resistance and capacitance begin to look resistive rather than capacitive, and the 90° phase shift and 20 dB/decade contributed by C_{C0} no longer apply. Note that, to cancel the load pole with the R_Z zero, the load pole must be known to exist. Adding a zero to cancel a pole that does not exist causes an oscillation (perhaps the expected load capacitor is not present). Also, it is recommended to avoid creating a zero frequency lower than the pole frequency; instead, allow the zero frequency to be 2× or 3× higher than the calculated pole frequency.

The Effect of R_P

R_P can be used to ensure circuit stability when a poor load capacitor with significant ESR is present. Above the frequency, $1/[C_R \times R_C]$, the DUT begins to look resistive. The ESR of the DUT capacitor, R_C, contributes a zero at this frequency. The load capacitor, C_R, is counted on to stabilize the system when the user has cancelled the load pole with the R_Z zero. Just as the absence of C_R under these circumstances can cause oscillations, the presence of ESR R_C while nonzero R_Z is used can cause

stability problems. This is most likely to be the case when there are both a large C_R and large R_C.

The R_P resistor is intended to solve this problem. Again, it is prudent not to cancel exact pole/zero cancellation with R_Z and instead allow the zero to be 2× to 3× the frequency of the pole. It is best to be very conservative when using R_Z to cancel the load pole. Choose a high zero frequency to avoid flat spots in the gain curve that extend bandwidth, and be conservative when choosing R_P to create a pole. Aim to place the R_Z zero at 5× the exact cancellation frequency and the R_P pole at around 2× the exact cancellation frequency. The best solution here is to avoid this complexity by using a high quality capacitor with low ESR.

COMPENSATION STRATEGIES

Ensuring Stability into an Unknown Capacitor Up to a Maximum Value

If the AD5560 has to be stable in a range of load capacitance from no load capacitance to an upper limit, then select manual compensation mode and, in Compensation Register 2, set the parameters according to the maximum load capacitance listed in Table 14.

Table 14. Suggested Compensation Settings for Load Capacitance Range of Unknown Value to Some Maximum Value

Capacitor						
Min	Max	$g_{m[1:0]}$	$R_{P[2:0]}$	$R_{Z[2:0]}$	$C_{C[3:1]}$	$C_{F[2:0]}$
0	0.22 µF	2	0	0	000	2
0	2.2 µF	2	0	0	001	3
0	10 µF	2	0	0	010	4
0	20 µF	2	0	0	011	4
0	160 µF	2	0	0	111	4

Table 14 assumes that the C_{Cx} and C_{Fx} capacitor values are those suggested in Table 8.

Making a circuit stable over a range of load capacitances for no load capacitance or greater means that the circuit is overcompensated for small load capacitances, undercompensated for high load capacitances, or both. The previous choice settings, along with the suggested capacitor values, is a compromise between both. By compromising phase margin into the largest load capacitors, the system bandwidth can be increased, which means better performance under load current transient conditions. The disadvantage is that there is more overshoot during a large DAC step. To reduce this at the expense of settling time, it may be desirable to temporarily switch a capacitor range 5× or 10× larger before making a large DAC step.

OPTIMIZING PERFORMANCE FOR A KNOWN CAPACITOR USING AUTOCOMPENSATION MODE

The autocompensation mode decides what values of g_{mx}, C_{Cx} C_{Fx}, R_Z, and R_P should be chosen for good performance in a particular capacitor. Both the capacitance and its ESR need to be known. To avoid creating an oscillator, the capacitance should not be overestimated and the ESR should not be underestimated. Use the following steps to determine compensation settings when using the manual compensation register (this algorithm is what the autocompensation method is based upon):

1. Use C_R (the load capacitance with a series ESR) and R_C (the ESR of that load capacitance) as inputs.
2. Assume that C_R has not been overestimated and that R_C has not been underestimated. (Although, when the ESR R_C is shown to have a frequency dependence, the lowest R_C that occurs near the resonant frequency is probably a better guide. However, do not underestimate this ESR).
   a. C_{C0} is the suggested 100 pF.
   b. C_{Fx} capacitor values are as suggested, and they extend up to 2.2 µF (C_{F4}). For faster settling into small capacitive loads, include smaller C_{Fx} values such as C_{F3} and C_{F2}. If a capacitor is not included, then short the corresponding C_{Fx} pin to one that is.
   c. There is approximately 1 Ω of parasitic resistance, R_C, from the AD5560 to the DUT (for example, the cable); R_C = 1 Ω.
3. Select $g_{m[1:0]}$ = 2, $C_{C[3:1]}$ = 000. This makes the input stage of the force amplifier; have g_{mx} = 300 µA/V; deselect the compensation capacitors, C_{C1}, C_{C2}, $C_{C3,}$ so that only C_{C0} is active.
4. Choose a $C_{F[2:0]}$ value from 0 to 4 to select the largest C_{Fx} capacitor that is smaller than C_R.
5. If C_R < 100 nF, then set $R_{Z[2:0]}$ = 0, $R_{P[2:0]}$ = 0. This ends the algorithm.
6. Calculate R_0, the resistive impedance to the DUT, using the following steps:
   a. Calculate R_S, the sense resistor, from the selected current range using $R_S = 0.5\ V/I_{RANGE}$.
   b. Calculate R_F, the output impedance, through the C_{Fx} capacitor, by using

      $$R_F = 1.2\ \Omega + (ESR\ of\ C_{Fx}\ capacitor)$$

   c. Calculate R_{FM}, a modified version of R_F, which takes account of frequency dependent peaking, through the C_{Fx} buffers into a large capacitive load, by using

      $$R_{FM} = R_F/(1 + [2 \times (C_{Fx}/2.2\ \mu F)])$$

      That is, R_{FM} is up to 3× smaller than R_F, when the selected C_{Fx} capacitor is large compared to 2.2 µF. Then calculate

      $$R_0 = R_C + (R_S \,||R_{FM})$$

      where R_C takes its value from the assumptions in Step 2.
7. If $R_C > (R_0/5)$, then the ESR is large enough to make the DUT look resistive. Choose $R_{Z[2:0]}$ = 0, $R_{P[2:0]}$ = 0. This ends the algorithm
8. Calculate the unity gain frequency (Fug), the ideal unity gain frequency of the force amplifier, from Fug = $g_{mx}/2\pi C_{C0}$. Using the previously suggested values ($g_{m[1:0]}$ = 2 gives g_{mx} = 300 µA/V and C_{C0} = 100 pF), Fug calculates to 480 kHz.
9. Calculate F_P, the load pole frequency, using $F_P = 1/(2\pi R_0 C_{C0})$.

10. Calculate F_Z, the ESR zero frequency, using $F_Z = 1/(2\pi RcCr)$.
11. If $F_P > Fug$, the load pole is above the bandwidth of the AD5560. Ignore it with $R_{Z[2:0]} = 0$, $R_{P[2:0]} = 0$. This ends the algorithm
12. If $R_C < (R_0/25)$, then the ESR is negligible. Attempt to cancel the load pole with R_Z zero. Choose an ideal zero frequency of $2 \times F_P$ for some safety margin and then choose the $R_{Z[2:0]}$ value that gives the closest frequency on a logarithmic scale. This ends the algorithm
13. Otherwise, this is a troublesome window in which a load pole and a load zero cannot be ignored. Use the following steps:
    - To cancel the load pole at F_P, choose an ideal zero frequency of $6 \times F_P$ (this is more conservative than the $2 \times F_P$ suggested earlier, but there is more that can go wrong with miscalculation). Then choose the $R_{Z[2:0]}$ value that gives the closest zero to this ideal frequency of $6 \times F_P$ on a logarithmic scale.
    - To cancel the ESR zero at F_Z, choose an ideal pole frequency of $2 \times F_Z$.
    - Then choose the $R_{P[2:0]}$ value that gives the closest pole to this ideal frequency of $2 \times F_Z$ on a logarithmic scale. This ends the algorithm

ADJUSTING THE AUTOCOMPENSATION MODE

The autocompensation algorithm assumes that there is 1 Ω of resistance (R_C) from the AD5560 to the DUT. If a particular application has resistance that differs greatly from this, then it is likely that the autocompensation algorithm is nonoptimal.

If using the autocompensation algorithm as a starting point, consider that overstating the C_R capacitance and understating the ESR R_C is likely to give a faster response but could cause oscillations. Understating C_R and overstating R_C is more likely to slow things down and reduce phase margin but not create an oscillator.

It is often advisable to err on the side of simplicity. Rather than insert a pole and zero at similar frequencies, it may be better to add none at all. Set $R_{P[2:0]} = R_{Z[2:0]} = 0$ to push them beyond the AD5560 bandwidth.

DEALING WITH PARALLEL LOAD CAPACITORS

In the event that the load capacitance consists of two parallel capacitors with different ESRs, it is highly likely that the overall complex impedance at the unity gain bandwidth is dominated by the larger capacitor and its ESR. Assuming that the smaller capacitor does not exist normally is a safer simplifying assumption.

A more complex alternative is to calculate the overall impedance at the expected unity gain bandwidth and use this to calculate an equivalent series C_R and R_C that have the same complex impedance at that particular frequency.

DAC LEVELS

This device contains all the dedicated DAC levels necessary for operation: a 16-bit DAC for the force amplifier, two 16-bit DACs for the clamp high and low levels, two 16-bit DACs for the comparator high and low levels, a 16-bit DAC to set a programmable open sense voltage, and a 16-bit offset DAC to bias or offset a number of DACs on chip (FORCE, CLL, CLH, CPL, CPH).

FORCE AND COMPARATOR DACS

The architecture of the main force amplifier DAC consists of a 16-bit R-2R DAC, whereas the comparator DACs are resistor-string DACs followed by an output buffer amplifier. This resistor-string architecture guarantees DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier.

The comparator DAC is similarly arranged. The force and comparator DACs have a 25.62 V span, including overrange to enable offset and gain errors to be calibrated out.

The transfer function for these 16-bit DACs is

$$V_{OUT} = 5.125 \times VREF \times \left(\frac{DAC\ CODE}{2^{16}}\right) - 5.125 \times VREF \times \left(\frac{OFFSET\_DAC\_CODE}{2^{16}}\right) + DUTGND$$

where *DAC CODE* is X2 (see the Offset and Gain Registers section).

CLAMP DACS

The architecture of the clamp DAC consists of a 16-bit resistor-string DAC followed by an output buffer amplifier. This resistor-string architecture guarantees DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier.

The clamp DACs have a 25.62 V span, including overrange, to enable offset and gain errors to be calibrated out.

The transfer function for these 16-bit DACs is

$$VCLH, VCLL = 5.125 \times V_{REF} \times \left(\frac{DAC\,CODE}{2^{16}} \right) - 5.125 \times V_{REF} \times \left(\frac{OFFSET\_DAC\_CODE}{2^{16}} \right) + DUTGND$$

The transfer function for the clamp current value is

$$ICLL, ICLH = \frac{5.125 \times V_{REF} \times \left(\frac{DAC\,CODE - 32768}{2^{16}} \right)}{R_{SENSE} \times MI\_AMP\_GAIN}$$

where:
R_{SENSE} is the sense resistor.
MI_AMP_GAIN is the gain of the MI amp (either 10 or 20).

OSD DAC

The OSD DAC is a 16-bit DAC function, again a resistor string DAC guaranteeing monotonicity. The 16-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. The OSD function is used to program the voltage difference needed between the force and sense lines before the alarm circuit flags an error. The OSD DAC has a range of 0.62 V to 5 V. The transfer function is as follows:

$$V_{OUT} = VREF \times \left(\frac{DAC\,CODE}{2^{16}} \right) \quad (1)$$

The offset DAC does not affect the OSD DAC output range.

DUTGND DAC

Similarly, the DUTGND DAC (DGS) is a 16-bit DAC and uses a resistor string DAC to guarantee monotonicity. The 16-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. This function is used to program the voltage difference needed between the DUTGND and AGND lines before the alarm circuit flags an error.

The DUTGND DAC has a range of 0 V to 5 V. The transfer function for this 16-bit DAC is shown in Equation 1.

The offset DAC does not affect the OSD DAC output range.

OFFSET DAC

In addition to the offset and gain trim, there is also a 16-bit offset DAC that offsets the output of each DAC on chip. Therefore, depending on headroom available, the input to the force amplifier can be arranged either symmetrically or asymmetrically about DUTGND but always within a voltage span of 25 V. Some extra gain is included to allow for system error correction using the m (gain) and c (offset) registers.

The usable voltage range is −22 V to +25 V. Full scale loaded to the offset DAC does not give a useful output voltage range because the output amplifiers are limited by available footroom. Table 15 shows the effect of the offset DAC on other DACs in the device (clamp, comparator, and force DACs).

Table 15. Offset DAC Relationship with Other DACs, V_{REF} = 5 V

Offset DAC Code	DAC Code[1]	DAC Output Voltage Range
0	0	0.00
0	32,768	12.81
0	65,535	25.62
…	…	…
32,768	0	−12.81
32,768	32,768	0.00
32,768	65,535	12.81
…	…	…
57,344	0	−22.42
57,344	32,768	−9.61
57,344	65,535	3.20
…	…	…
65,355	…	Footroom limitations

[1] DAC code shown for 16-bit force DAC.

OFFSET AND GAIN REGISTERS

Each DAC level contains independent offset and gain control registers that allow the user to digitally trim offset and gain. These registers give the user the ability to calibrate out errors in the complete signal chain (including the DAC) using the internal m and c registers, which hold the correction factors.

The digital input transfer function for the DACs can be represented as

$$x2 = [x1 \times (m + 1)/2^n] + (c - 2^{n-1})$$

where:
x2 is the data-word loaded to the resistor string DAC.
x1 is the 16-bit data-word written to the DAC input register.
m is the code in the gain register (default code = $2^{16} - 1$).
n is the DAC resolution (*n* = 16).
c is the code in the offset register (default code = 2^{15}).

Offset and Gain Registers for the Force Amplifier DAC

The force amplifier input (F_{IN}) DAC level contains independent offset and gain control registers that allow the user to digitally trim offset and gain. There is one set of registers for the force voltage range: x1, m, and c.

Offset and Gain Registers for the Comparator DACs

The comparator DAC levels contain independent offset and gain control registers that allow the user to digitally trim offset and gain. There are seven sets of registers consisting of a combination of x1, m, and c, one set each for the five internal force current ranges and one set each for the two external high current ranges.

Offset and Gain Registers for the Clamp DACs

The clamp DAC levels contain independent offset and gain control registers that allow the user to digitally trim offset and gain. One set of registers covers the V_{SENSE} range, the five internal force current ranges, and the two external high current ranges. Both clamp DAC x1 registers and their associated offset and gain registers are 16 bit.

REFERENCE SELECTION

The voltage applied to the VREF pin determines the output voltage range and span applied to the force amplifier, clamp, and comparator inputs and the current ranges.

This device can be used with a reference input ranging from 2 V to 5 V. However, for most applications, a reference input of 5 V is able to meet all voltage range requirements. The DAC amplifier gain is 5.125, which gives a DAC output span of 25.625 V. The DACs have gain and offset registers that can be used to calibrate out system errors. In addition, the gain register can be used to reduce the DAC output range to the desired force voltage range.

Using a 5 V reference and setting the m (gain) register to one-fourth scale or 0x4000 gives an output voltage span of 6.25 V. Because the force DAC has 18 bits of resolution even with only one-fourth of the output voltage span, it is still possible to achieve 16-bit resolution in this 6.25 V range.

The measure current amplifier has two gain settings, 10 and 20. The two gain settings allow users to achieve the quoted/specified current ranges with large or small voltage swings. The 20 gain setting is intended for use with a 5 V reference, and the 10 gain setting is for use with a 2.5 V reference. Both combinations ensure the specified current ranges. Other VREF/gain setting combinations should be used only to achieve smaller current ranges. See Table 27 for suggested references for use with the AD5560.

CALIBRATION

Calibration involves determining the gain and offset of each channel in each mode and overwriting the default values in the m and c registers of the individual DACs.

Reducing Zero-Scale Error

Zero-scale error can be reduced as follows:

1. Set the output to the lowest possible value.
2. Measure the actual output voltage and compare it to the required value. This is the zero-scale error.
3. Calculate the number of LSBs equivalent to the zero-scale error, and add or subtract this number to the default value of the c register.

Reducing Gain Error

Gain error can be reduced as follows:

1. Measure the zero-scale error.
2. Set the output to the highest possible value.
3. Measure the actual output voltage and compare it to the required value. This is the gain error.
4. Calculate the number of LSBs equivalent to the gain error and subtract this number from the default value of the m register. Note that only positive gain error can be reduced.

Calibration Example

Nominal offset coefficient = 32,768 (0x8000)

Nominal gain coefficient = 65,535 (0xFFFF)

For example, the gain error = 0.5%, and the offset error = 100 mV.

Gain error (0.5%) calibration is as follows:

$$65{,}535 \times 0.995 = 65{,}207$$

Therefore, load Code 1111 1110 1011 0111 (0xFEB7) to the m register.

Offset error (100 mV) calibration is as follows:

$$\text{LSB size} = 10.25/65{,}535 = 156\ \mu\text{V}$$

Offset coefficient for 100 mV offset = 100/0.156 = 641 LSBs

Therefore, load Code 0111 1101 0111 1111 (0x7D7F) to the c register.

ADDITIONAL CALIBRATION

The techniques described in the Calibration section are usually sufficient to reduce the zero-scale and gain errors. However, there are limitations whereby the errors may not be sufficiently reduced. For example, the offset (c) register can only be used to reduce the offset caused by negative zero-scale error. A positive offset cannot be reduced. Likewise, if the maximum voltage is below the ideal value, that is, a negative gain error, the gain (m) register cannot be used to increase the gain to compensate for the error. These limitations can be overcome by increasing the reference value.

SYSTEM LEVEL CALIBRATION

There are many ways to calibrate the device on power-on. Following is an example of how to calibrate the FIN DAC registers (Register 0x8 to Register 0xA) of the device without a DUT or DUT board connected. The calibration procedure for the force and measure circuitry is as follows:

1. Calibrate the force voltage (two-point calibration).
   a. Write zero scale to the FIN DAC registers (Register 0x8 to Register 0xA).
   b. Connect SYS_FORCE to FORCE (via SW8) and SYS_SENSE to SENSE (via SW9), and close the internal force/sense switch (SW11).
   c. Using the system PMU, measure the error between the voltage at FORCE/SENSE and the desired value.
   d. Similarly, load full scale to the FIN DAC registers (Register 0x8 to Register 0xA) and measure the error between the voltage at FORCE/SENSE and the desired value.
   e. Calculate the m and c values.
   f. Load these values to the appropriate FIN DAC m and FIN DAC c registers (Register 0x9 and Register 0xA).
2. Calibrate the measure voltage (two-point calibration).
   a. Connect SYS_FORCE to FORCE (via SW8) and SYS_SENSE to SENSE (via SW9), and close the internal force/sense switch (via SW11).

   b. Force the voltage on FORCE via SYS_FORCE and measure the voltage at MEASOUT. The difference is the error between the actual forced voltage and the voltage at MEASOUT.
3. Calibrate the measure current (two-point calibration).
   a. In FV mode, write zero scale to the FIN DAC registers (Register 0x8 to Register 0xA).
   b. Disconnect the FORCE pin and the SENSE pin. Connect SYS_FORCE to FORCE (via SW8) and SYS_SENSE to SENSE (via SW9).
   c. Connect the SYS_FORCE pin to an external ammeter and its other terminal to the SYS_SENSE pin.
   d. Connect the SYS_SENSE pin to a precision resistor (R_{DUT}), where $R_{DUT} = R_{SENSE} \times 20$ of the current range, and connect its other terminal to ground (see Figure 58).
   e. Measure the error between the ammeter reading and the MEASOUT reading by forcing ±10 V to the FIN DAC registers (Register 0x8 to Register 0xA).
   f. Repeat Step 3a through Step3e across all current ranges.
4. Similarly, calibrate the comparator and clamp DACs, and load the appropriate gain and offset registers. Calibrating these DACs requires some successive approximation to determine where the comparator trips or the clamps engage.

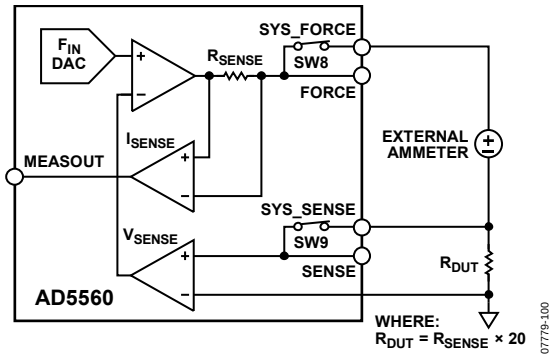

Figure 58. Measure Current Calibration

CHOOSING AV_{DD}/AV_{SS} POWER SUPPLY RAILS

As noted in the Specifications section, the minimum supply variation across the part is $|AV_{DD} - AV_{SS}| \geq 16$ V and ≤ 33 V, $AV_{DD} \geq 8$ V, and $AV_{SS} \leq -5$ V. For the AD5560 circuits to operate correctly, the supply rails must take into account not only the force voltage range but also the internal DAC minimum voltage level, as well as headroom/footroom.

The DAC amplifier gains VREF by 5.125, and the offset DAC centers that range about some chosen point. Because the DAC minimum voltage (V_{MIN}) is used in other parts of the circuit (MEASOUT gain of 0.2), it is important that AV_{SS} be chosen based on the following:

$$AV_{SS} \leq -5.125 \times (VREF \times (OFFSET\_DAC\_CODE/2^{16})) - AV_{SS}\_Headroom - V_{DUTGND} - (R_{CABLE} \times I_{LOAD})$$

where:
$AV_{SS}\_Headroom$ is the 2.75 V headroom (includes the R_{SENSE} voltage drop).
V_{DUTGND} is the voltage range anticipated at DUTGND.
R_{CABLE} is the cable/path resistance.
I_{LOAD} is the maximum load current.

When choosing AV_{DD}, remember to take into account the specified current ranges. The measure current block has either a gain of 20 or 10 and must have sufficient headroom/footroom to operate correctly.

As the nominal, V_{RSENSE} is ±0.5 V for the full-scale specified current flowing for all ranges. If this is gained by 20, the measure current amplifier output (internal node) voltage range is ±10 V with full-scale current and the default offset DAC setting. The measure current block needs ±2.25 V footroom/headroom for correct operation in addition to the ±0.5 V V_{RSENSE}.

For simplicity, when $V_{REF} = 5$ V, minimum $|AV_{DD} - AV_{SS}| =$ 31.125 V (VREF × 5.125 + headroom + footroom); otherwise, there can be unanticipated effects resulting from headroom/footroom issues. This does not take into account cable loss or DUTGND contributions.

Similarly, when $V_{REF} = 2.5$ V, minimum $|AV_{DD} - AV_{SS}| = 18.3$ V and, when $V_{REF} = 2$ V, minimum $|AV_{DD} - AV_{SS}| = 16$ V.

The AD5560 is designed to settle fast into large capacitive loads; therefore, when slewing, the device draws 2× to 3× the current range from the AV_{DD}/AV_{SS} supplies. When supply rails are chosen, they should be capable of supplying each DPS channel with sufficient current to slew.

CHOOSING $HCAV_{SS}x$ AND $HCAV_{DD}x$ SUPPLY RAILS

Selection of $HCAV_{SS}x$ and $HCAV_{DD}x$ supplies is determined by the EXTFORCE1 and EXTFORCE2 output ranges. The supply rails chosen must take into account headroom and footroom, DUTGND voltage range, cable loss, supply tolerance, and V_{RSENSE}. If diodes are used in series with the $HCAV_{SS}x$ and $HCAV_{DD}x$ supplies pins (shown in Figure 60), the diode voltage drop should also be factored into the supply rail calculation.

The AD5560 is designed to settle fast into large capacitive loads in high current ranges; therefore, when slewing, the device draws 2× to 3× the current range from the $HCAV_{SS}x$ and $HCAV_{DD}x$ supplies. When choosing supply rails, ensure that they are capable of supplying each DPS channel with sufficient current to slew.

All output stages of the AD5560 are symmetrical; they can source and sink the rated current. Supply design/bypassing should account for this.

POWER DISSIPATION

The maximum power dissipation allowed in the EXTFORCE1 stage is 10 W, whereas in the EXTFORCE2 stage, it is 5 W. Take care to ensure that the device is adequately cooled to remove the heat. The quiescent current is ~0.8 W with an

internal current range enabled and ~1 W with external current ranges, EXTFORCE1 or EXTFORCE2, enabled. This device is specified for performance up to 90°C junction temperature (T_J).

PACKAGE COMPOSITION AND MAXIMUM VERTICAL FORCE

The exposed pad and leads of the TQFP package have a 100% tin finish. The exposed paddle is connected internally to AV_{SS}. The simulated maximum allowable force for a single lead is 0.18 lbs; total allowable force for the package is 11.5 lbs. The quoted maximum force may cause permanent lead bending. Other package failure (die, mold, board) may occur first at lower forces.

SLEW RATE CONTROL

There are two methods of achieving different slew rates using the AD5560. One method is using the programmable slew rate feature that gives eight programmable rates. The second method is using the ramp feature and an external clock.

Programmable Slew Rate

Eight programmable modes of slew rates are available to choose from through the serial interface, enabling the user to choose different rates to power up the DUT. The different slew rates are achieved by variation in the internal compensation of the force DAC output amplifier. The slew rates available are 1.000 V/µs, 0.875 V/µs, 0.750 V/µs, 0.625 V/µs, 0.5 V/µs, 0.4375 V/µs, 0.35V µs, and 0.313 V/µs.

Ramp Function

Included in the AD5560 is a ramp function that enables the user to apply a rising or falling voltage ramp to the DUT. The user supplies a clock, RCLK, to control the timing.

This function is controlled via the serial interface and requires programming of a number of registers to determine the end value, the ramp size, and the clock divider register to determine the update rate.

The contents of the FIN DAC x1 register are the ramp start value. The user must load the end code register and the step size register. The sign is now generated from the difference between the FIN DAC x1 register and the end code; then the step size value is added to or subtracted from FIN DAC x1, calibrated and stored. The user must supply a clock to the RCLK pin to load the new code to the DAC. The output settles in 1.2 µs for a step of 10 mV with C_{DUT} in the lowest range of <0.2 µF.

While the output is settling, the next step is calculated to be ready for the next ramp clock. The calibration engine is used here; therefore, there is a calibration delay of 1.2 µs.

The ramp timing is controlled in two ways: by a user-supplied clock (RCLK) and by a clock divider register. This gives the user much flexibility over the frequency of the ramp steps. The ramp typically starts after (2 × clock divider + 2) clocks, although there can be a ±1 clock delay due to the asynchronous nature of RCLK. The external clock can be a maximum of 833 kHz when using clock divider = 1. Faster RCLK speeds can be used, but the fastest ramp rate is linked into the DAC calibration engine.

For slower ramp rates, an even slower RCLK can be used.

The step sizes are in multiples of 16 LSBs. If the code previous to the end code is not a multiple of this step size, the last step is smaller. If the ramp function must be interrupted at any stage during the ramp, write the interrupt ramp command. The FIN DAC x1 stops ramping at the current value and returns to normal operation.

The fastest ramp rate is 0.775 V/µs (for a 5 V reference and an 833 kHz clock using a 2032 LSB step size and divider = 1).

The slowest ramp rate is 24 µV/µs (for a 5 V reference and an 833 kHz clock using a 16 LSB step size and divider = 255). Even slower ramps can be achieved with slower SCLK. The ramp continues until any of the following occurs:

- It reaches the end code.
- An interrupt ramp is received from the user.
- If any enabled alarm triggers, the ramp stops to allow the user to service the activated alarm.

While the device is in ramp mode, the only command that the interface accepts is an interrupt ramp. No other commands should be written to the device while ramping because they are ignored.

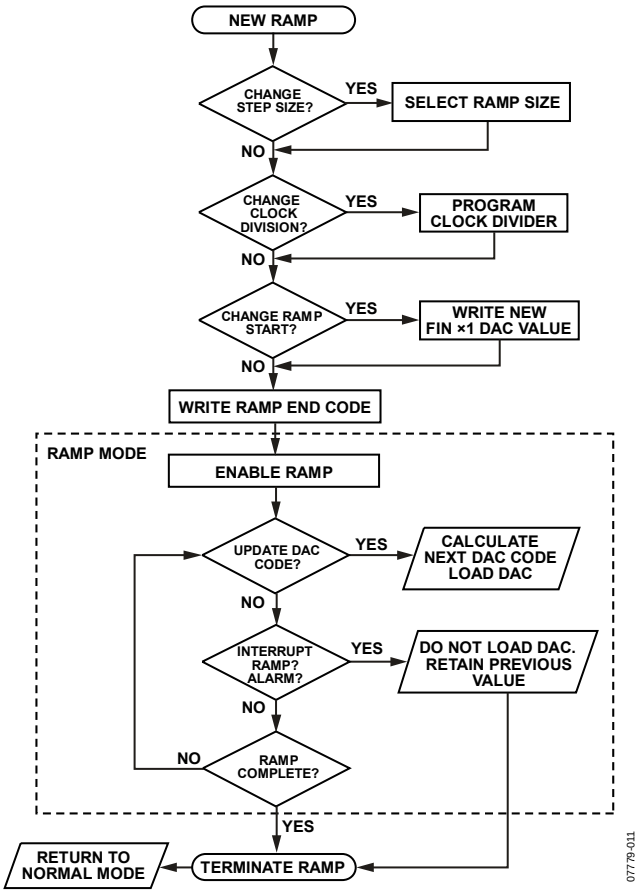

Figure 59. Flow Chart for Ramp Function

SERIAL INTERFACE

The AD5560 contains an SPI-compatible interface operating at clock frequencies of up to 50 MHz. To minimize both the power consumption of the device and on-chip digital noise, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$.

SPI INTERFACE

The serial interface is 2.5 V LVTTL-compatible when operating from a 2.3 V to 3.6 V DV_{CC} supply. It is controlled by the following four pins:

- $\overline{\text{SYNC}}$ (frame synchronization input)
- SDI (serial data input pin)
- SCLK (clocks data in and out of the device)
- SDO (serial data output pin for data readback)

SPI WRITE MODE

The AD5560 allows writing of data via the serial interface to every register directly accessible to the serial interface, which is all registers except the DAC registers.

The serial word is 24 bits long. The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5560 by clock pulses applied to SCLK. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. At least 24 falling clock edges must be applied to SCLK to clock in 24 bits of data before $\overline{\text{SYNC}}$ is taken high again.

The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be taken low again.

SDO OUTPUT

The SDO output in the AD5560 is a weak/slow output driver. If using readback or the daisy-chain function, the frequency of SCLK must be reduced so that SDO can operate properly. The SCLK frequency is dependent on the DV_{CC} supply voltage used; see Table 2 for details and the following example:

Maximum SCLK = 12 MHz, then DV_{CC} = 2.3 V to 2.7 V

Maximum SCLK = 15 MHz, then DV_{CC} = 2.7 V to 3.3 V

Maximum SCLK = 20 MHz, then DV_{CC} = 4.5 V to 5.5 V

$\overline{\text{RESET}}$ FUNCTION

$\overline{\text{RESET}}$ is a level-sensitive input. Bringing the $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low for the duration, returning high when the $\overline{\text{RESET}}$ process is complete. This sequence takes 300 µs maximum. Do not write to the serial interface while $\overline{\text{BUSY}}$ is low handling a $\overline{\text{RESET}}$ command. When $\overline{\text{BUSY}}$ returns high, normal operation resumes, and the status of the $\overline{\text{RESET}}$ pin is ignored until it goes low again.

$\overline{\text{BUSY}}$ FUNCTION

$\overline{\text{BUSY}}$ is a digital open-drain output that indicates the status of the AD5560. All writes drive the $\overline{\text{BUSY}}$ output low for some period of time; however, events that use the calibration engine, such as all DAC x1 writes, drive it lower for a longer period of time while the calculations are completed.

For the DACs, the value of the internal data (x2) loaded to the DAC data register is calculated each time the user writes new data to the corresponding x1 register. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low and x2 writes are pipelined; therefore, x2 writes can still be presented to the device while $\overline{\text{BUSY}}$ is still low (see the Register Update Rates section). The DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high.

Writes to other registers must be handled differently and should either watch the $\overline{\text{BUSY}}$ pin or be timed. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to any control register, m register, or c register but should not complete the writing process ($\overline{\text{SYNC}}$ returning high) until the $\overline{\text{BUSY}}$ signal has returned high.

$\overline{\text{BUSY}}$ also goes low during power-on reset, as well as when a low level is detected on the $\overline{\text{RESET}}$ pin.

$\overline{\text{BUSY}}$ writes to the system control register, compensation register, alarm register, and diagnostic register; m or c registers do not involve the calibration engine, thus speeding up writing to the device.

$\overline{\text{LOAD}}$ FUNCTION

The AD5560 device contains a function with which updates to multiple devices can be synchronized using the $\overline{\text{LOAD}}$ function. There is not a dedicated pin available for this function; however, either the CLEN or $\overline{\text{HW\_INH}}$ pin can be used as a $\overline{\text{LOAD}}$ input (selection is made in the system control register, Address 0x1, Bits[8:7]).

When selected as the $\overline{\text{LOAD}}$ function, the pin no longer operates in its previous function (power-on default for each of these pins is a CLEN or $\overline{\text{HW\_INH}}$ function).

The $\overline{\text{LOAD}}$ function controls the following registers:

- 0x8 FIN DAC x2 register
- 0xD CLL DAC x2 register
- 0x10 CLH DAC x2 register
- 0x4 Compensation Register 1
- 0x5 Compensation Register2
- 0x2 DPS Register1 (only current ranges, Bits[13:11])

There is, however, an alternate method for updating and using the CLEN and $\overline{\text{HW\_INH}}$ pins in their normal function.

If Bits[8:7] of the system control register (Address 0x1) are high, then the CLEN and HW_INH operate as normal, and the update waits until BUSY goes high (this way multiple channels can still be synchronized by simply tying BUSY pins together).

REGISTER UPDATE RATES

As mentioned previously, the value of the x2 register is calculated each time the user writes new data to the corresponding x1 register. The calculation is performed by a three stage process. The first two stages take 600 ns each, and the third stage takes 300 ns. When the write to one of the x1 registers is complete, the calculation process begins. The user is free to write to another register provided that the write operation does not finish until the first stage calculation is complete, that is, 600 ns after the completion of the first write operation.

CONTROL REGISTERS

DPS AND DAC ADDRESSING

The serial word assignment consists of 24 bits, as shown in Table 16. All write-to registers can be read back. There are some read-only registers (Address 0x43 and Address 0x44). DAC x2 registers are not available for readback.

A no operation (NOP) command performs no function within the device. This code may be useful when performing a readback function where a change of DAC or DPS register is not required.

Table 16. Serial Word Assignment

B23	[B22:B16]	[B15:B0]
R/$\overline{W}$	Address bits	Data bits

Table 17. Read or Write Register Addressing

Address	Register	Default	Data Bits, MSB First				
0x0	NOP	0x0000	NOP command; performs no operation.				
0x1	System control register	0x0000	**Bit**	**Name**	**Function**		
			15 14	TMP[1:0]	Thermal shutdown bits. TMP1, TMP0 allow the user to program the thermal shutdown temperature of operation.		
					TMP	**Action**	
					0	Shutdown at a T_J of 130°C (power-on default)	
					1	Shutdown at a T_J of 120°C	
					2	Shutdown at a T_J of 110°C	
					3	Shutdown at a T_J of 100°C	
			13 12	Gain[1:0]	MEASOUT output range. The MEASOUT range defaults to the voltage force span for voltage and current measurements (this is ±12.81 V), which includes some overrange to allow for error correction. The MEASOUT range can be reduced by using the gain bits. This allows for use of asymmetrical supplies or for use of a smaller input range ADC. MEASOUT gain settings do not translate the low voltage temperature sensor signal (TSENSE).		
					Gain	**MEASOUT Gain**	**MI Gain**
					0	1	20
					1	1	10
					2	0.2	20
					3	0.2	10
					To allow for system error correction, there is an additional gain of 0.125 for the force function if this error correction is used as intended; then the output range on MEASOUT scales accordingly (see Table 9).		
			11	FINGND	Writing a 1 to FINGND switches the positive input of the force amplifier to GND; when 0, the input of the force amplifier is connected to the output of the force DAC.		
			10	CPO	Write a 1 to the CPO bit to enable a simple window comparator function. In this mode, only one comparator output is available (CPOH/CPO). This provides two bits of information. The compared value is either inside or outside the window and enables the user to bring only one line back to the controller per DPS device.		
			9	$\overline{PD}$	This bit powers down the force amplifier block. Note that the amplifier must be powered up but inhibited ($\overline{SW\text{-}INH}$ or $\overline{HW\_INH}$), to meet leakage specifications. A 0 powers this block down (default).		
			8 7	$\overline{LOAD}$	Updates to registers listed in the following $\overline{LOAD}$ function column do not occur until the active $\overline{LOAD}$ pin is brought low (or in the case of $\overline{LOAD}$ 3, until $\overline{BUSY}$ goes high).		
					$\overline{LOAD}$	**$\overline{LOAD}$ Function**	
					0	Default operation, CLEN and $\overline{HW\_INH}$ function normally.	
					1	The CLEN pin is a $\overline{LOAD}$ input.	
					2	The $\overline{HW\_INH}$ pin is a $\overline{LOAD}$ input.	
					3	The device senses the $\overline{BUSY}$ open-drain pin and doesn't update until that goes high. No $\overline{LOAD}$ hardware pin. CLEN and $\overline{HW\_INH}$ function normally.	
			6:0	Unused	Set to 0.		

Table 18. DPS Register 1

Address	Default	Data Bits, MSB First		
0x2	0x0000	**Bit**	**Name**	**Function**
		15	$\overline{\text{SW-INH}}$	This bit enables the force amplifier when high and disables the amplifier when low. This bit is AND'd with the $\overline{\text{HW\_INH}}$ hardware inhibit pin.
		14	Reserved	Reserved, set to 0.
		13 12 11	I[2:0]	Current range addressing. These bits allow selection of the required current range.
			I	**Action**
			0	±5 µA current range.
			1	±25 µA current range.
			2	±250 µA current range.
			3	±2.5 mA current range.
			4	±25 mA current range.
			5	External Range 2.
			6	External Range 1.
			7	Reserved.
		10 9	CMP[1:0]	Comparator function. CMP1 acts as a comparator output enable, whereas CMP0 selects between a comparing DUT current or voltage; by default, the comparators are high-Z on power-on.
			CMP	**Action**
			0	Comparator outputs high-Z.
			1	Comparator outputs high-Z.
			2	Compare DUT current.
			3	Compare DUT voltage.
		8 7 6 5	ME[3:0]	Bits ME[3:0] allow selection of the required measure mode, allowing the MEASOUT line to be disabled; connect to the temperature sensor or enable it for measurement. ME[3] is MEASOUT enable/disable; when high, MEASOUT is enabled, and ME[2:0] can be used to preselect the measuring parameter. Where a number of MEASOUT lines are connected together and passed to a common ADC, this function can allow for much faster measurement time between channels because the slew time of the measurement buffer is reduced. For details on diagnostic functions, see Address 0x7, the diagnostic register.
			ME[2:0]	**Action**
			0	MEASOUT high-Z.
			1	Connect MEASOUT to $I_{SENSE.}$
			2	Connect MEASOUT to $V_{SENSE.}$
			3	Connect MEASOUT to $K_{SENSE.}$
			4	Connect MEASOUT to TSENSE.
			5	Connect MEASOUT to DUTGND SENSE.
			6	Connect MEASOUT to diagnostic functions: DIAG A (see Address 0x7).
			7	Connect MEASOUT to diagnostic functions: DIAG B (see Address 0x7).
		4	CLEN	Clamp enable; set high to enable the clamp; set low to disable the clamp. This bit is OR'd with the hardware CLEN pin.
		3:0	Unused	Set to 0.

Table 19. DPS Register 2

Address	Default	Data Bits, MSB First						
0x3	0x0000	**Bit**	**Name**	**Function**				
		15	SF0	System force and sense line addressing, SF0. Bit SF0 addresses each of the different combinations of switching the system force and sense lines to the force and sense pins at the DUT.				
				Guard High-Z (Bit 7)	**SFO**	**SYS_SENSE Pin**	**SYS_FORCE Pin**	**GUARD/SYS_DUTGND Pin**
				0	0	Open	Open	Guard
				0	1	Sense	Force	Guard
				1	0	Open	Open	Open
				1	1	Sense	Force	DUTGND
		14 13 12	SR[2:0]	Slew rate control, SR2, SR1, SR0. Selects the slew rate for the main DAC output amp.				
				SR	**Action**			
				0	1 V/µs			
				1	0.875 V/µs			
				2	0.75 V/µs			
				3	0.62 V/µs			
				4	0.5 V/µs			
				5	0.43 V/µs			
				6	0.35 V/µs			
				7	0.3125 V/µs			
		11	GPO	General purpose output bit. The GPO bit can be used for any function, such as disconnecting the decoupling capacitor to help speed up low current testing.				
		10 9	SLAVE, GANGIMODE	Ganging multiple devices increases the current drive available. Use these bits to enable selection of the ganging mode and place the device in slave or master mode. In default operation, each device is a master (gang of one). Figure *54* shows how the device is configured in this mode.				
				SLAVE	**Action**			
				0	Master: MASTER_OUT = internally connects to active EXTFORCE1/ EXTFORCE2 output			
				1	Master: MASTER_OUT = master MI			
				2	SLAVE FV to EXTFORCE1/EXTFORCE2 connected internally to close the FVAMP loop			
				3	SLAVE FI			
		8	INT10K	Setting this bit high allows the user to connect an internal sense short resistor of 10 kΩ between the force and the sense lines (closes SW11). This resistor is actually made up of series 4 kΩ resistors followed by a 2 kΩ switch and another 4 kΩ resistor. There is a 10 kΩ resistor that can be connected between the FORCE and SENSE pins by use of SW11. This 10 kΩ resistor is intended to maintain a force/sense connection when a DUT is not in place. It is not intended to be connected when measurements are being made because this defeats the purpose of the OSD circuit in identifying an open circuit between FORCE and SENSE. In addition, the sense path has a 2.5 kΩ resistor in series; therefore, if the 10 kΩ switch is closed, errors may become apparent when in high current ranges.				
		7	Guard high-Z	Set this bit high to high-Z the guard amplifier. This is required if using the GUARD/ SYS_DUTGND pin in the SYS_DUTGND function.				
		6:0	Unused	Set to 0.				

The AD5560 has three compensation modes. The power-on default mode is $\overline{\text{SAFEMODE}}$ enabled. This ensures that the device is stable into any load. Use Compensation Register 1 to configure the device for autocompensation, where the user inputs the CDUT and ESR bits, and the AD5560 chooses the most appropriate compensation scheme for these load conditions.

Table 20. Compensation Register 1

Address	Default	Data Bits, MSB First				
0x4	0x0000	**Bit**	**Name**	**Function**		
		15 14 13 12	CDUT[3:0]	Use these control bits to tell the device how much capacitive load there is so that the device can optimize the compensation used. Do not overestimate CDUT because this can cause oscillations. Underestimating CDUT gives suboptimal but stable performance.		
				CDUT	**CDUT Min**	**CDUT Max**
				0	0 nF	50 nF
				1	50 nF	83 nF
				2	83 nF	138 nF
				3	138 nF	229 nF
				4	229 nF	380 nF
				5	380 nF	630 nF
				6	630 nF	1.1 µF
				7	1.1 µF	1.7 µF
				8	1.7 µF	2.9 µF
				9	2.9 µF	4.8 µF
				10	4.8 µF	7.9 µF
				11	7.9 µF	13 µF
				12	13 µF	22 µF
				13	22 µF	36 µF
				14	36 µF	60 µF
				15	60 µF	160 µF
		11 10 9 8	ESR[3:0]	Use these control bits to tell the device how much ESR there is in series with CDUT so that the device can optimize the compensation used. Do not underestimate ESR because this can cause oscillations. Overestimating ESR gives suboptimal but stable performance.		
				ESR	**ESR Min**	**ESR Max**
				0	0 mΩ	1 mΩ
				1	1 mΩ	1.8 mΩ
				2	1.8 mΩ	3.4 mΩ
				3	3.4 mΩ	6.3 mΩ
				4	6.3 mΩ	12 mΩ
				5	12 mΩ	21 mΩ
				6	21 mΩ	40 mΩ
				7	40 mΩ	74 mΩ
				8	74 mΩ	140 mΩ
				9	140 mΩ	250 mΩ
				10	250 mΩ	460 mΩ
				11	460 mΩ	860 mΩ
				12	860 mΩ	1500 mΩ
				13	1500 mΩ	2900 mΩ
				14	2900 mΩ	5400 mΩ
				15	6400 mΩ	10,000 mΩ
		7	$\overline{\text{SAFEMODE}}$	$\overline{\text{SAFEMODE}}$ = 0 overrides values in Compensation Register 1 to make the force amplifier stable under most load conditions. This mode is useful if it is unknown what the DPS is driving, but it does result in an extremely slow response. The default operation on power-on or reset is $\overline{\text{SAFEMODE}}$. $\overline{\text{SAFEMODE}}$ settings are always $g_{m[1:0]} = 2$, $R_{P[2:0]} = 0$, $R_{Z[2:0]} = 0$, $C_{C[3:1]} = 111$, $C_{F[2:0]} = 5$, and $C_{C0} = 1$. Set this bit high to enable autocompensation.		
		6:0	Reserved	Set to 0.		

Table 21. Compensation Register 2

Address	Default	Data Bits, MSB First		
0x5	0x0110	**Bit**	**Name**	**Function**
		15	Manual compensation	The AD5560 can be manually configured to compensate the force amplifier into a wide range of load conditions. When this bit is high, manual compensation mode is active, and it overrides the settings of Compensation Register 1. Readback when in manual compensation mode returns the compensation settings loaded to the force amplifier and loaded to this register. Similarly, when in autocompensation mode, readback of this register address returns the compensation settings of the force amplifier. However, readback of this register address when in safe mode does not reflect $\overline{\text{SAFEMODE}}$ settings. $\overline{\text{SAFEMODE}}$ settings are $g_{m[1:0]} = 2$, $R_P[2:0] = 0$, $R_{Z[2:0]} = 0$, $C_{C[3:1]} = 111$, $C_{F[2:0]} = 5$, and $C_{C0} = 1$.
		14 13 12	$R_{Z[2:0]}$	Set the value of R_Z to add a zero at the following frequencies. This calculation assumes that $C_{C0} = 100$ pF. **R_Z** / **R_{Zx}(Ω)** / **F_Z (Hz)** 0[1] / 500 / 3.2 M 1 / 1.6 k / 1 M 2 / 5 k / 320 k 3 / 16 k / 100 k 4 / 50 k / 32 k 5 / 160 k / 10 k 6 / 500 k / 3.2 k 7 / 1.6 M / 1 k
		11 10 9	$R_{P[2:0]}$	Set the value of R_P to add an additional pole. There is an internal 8 pF capacitor to provide an RC filter, creating a pole at one of the following frequencies. **$R_{P[2:0]}$** / **R_P (Ω)** / **F_P (Hz)** 0[1] / 200 / 100 M 1 / 675 / 29 M 2 / 2280 / 8.7 M 3 / 7700 / 2.6 M 4 / 26 k / 760 k 5 / 88 k / 220 k 6 / 296 k / 67 k 7 / 1 M / 20 k
		8 7	$g_{m[1:0]}$	Set the transconductance of the force amplifiers input stage. The gain bandwidth (GBW) of the force voltage loop is equal to g_{mx}/C_{C0}. The following values assume $C_{C0} = 100$ pF. g_{mx} / g_{mx} (µA/V) / GBW (Hz) 0 / 40 / 64 k 1 / 80 / 130 k 2[1] / 300 / 480 k (default) 3 / 900 / 1.3 M
		6 5 4	$C_{F[2:0]}$	These bits determine which feedforward capacitor C_{Fx} is switched in. C_{Fx} / Action 0 / None 1 / C_{F0} 2 / C_{F1} 3 / C_{F2} 4 / C_{F3} 5[1] / C_{F4} 6 / None 7 / None
		3	C_{C3}	Connect C_{C3} in series with 100 kΩ[1]
		2	C_{C2}	Connect C_{C2} in series with 25 kΩ[1]
		1	C_{C1}	Connect C_{C1} in series with 6 kΩ[1]
		0	Reserved	0

[1] This item corresponds to a $\overline{\text{SAFEMODE}}$ setting ($\overline{\text{SAFEMODE}}$ is the power-on default setting).

Register 0x6 allows the user to enable or disable any of the alarm flags that are not required. If disabled, that particular alarm no longer flags on the appropriate open-drain pin; however, the alarm status is still available in both of the alarm status registers (Address 0x43 and Address 0x44).

Table 22. Alarm Setup Register

Address	Default	Data Bits, MSB First		
0x6	0x0000	**Bit**	**Name**	**Function**
		15	Latched $\overline{\text{TMPALM}}$	Set this latched bit high to program the open-drain $\overline{\text{TMPALM}}$ alarm pin as a latched output; leave low for an unlatched alarm pin (default).
		14	Disable $\overline{\text{TMPALM}}$	Set this bit high to disable the open-drain $\overline{\text{TMPALM}}$ alarm pin; leave low to leave enabled (default).
		13	Latched $\overline{\text{OSALM}}$	Set this latched bit high to program the $\overline{\text{OSALM}}$ as a latched alarm on the open-drain $\overline{\text{KELALM}}$ pin; leave low for an unlatched alarm pin (default).
		12	Disable $\overline{\text{OSALM}}$	Set this bit high to disable the $\overline{\text{OSALM}}$ alarm function flagging the open-drain $\overline{\text{KELALM}}$ pin; leave low to remain enabled (default). The disable $\overline{\text{GRDALM}}$, $\overline{\text{DUTALM}}$, and $\overline{\text{OSALM}}$ alarm functions share one open-drain $\overline{\text{KELALM}}$ alarm pin. These bits allow users to choose if they wish to have all or selected information flagged to the alarm pin.
		11	Latched $\overline{\text{DUTALM}}$	Set this latched bit high to program the $\overline{\text{DUTALM}}$ as a latched alarm on the open-drain $\overline{\text{KELALM}}$ pin; leave low for an unlatched alarm pin (default).
		10	Disable $\overline{\text{DUTALM}}$	Set this bit high to disable the $\overline{\text{DUTALM}}$ alarm function flagging the open-drain $\overline{\text{KELALM}}$ pin. Leave low to leave enabled (default). The disable $\overline{\text{GRDALM}}$, $\overline{\text{DUTALM}}$, and $\overline{\text{OSALM}}$ alarm functions share one open drain $\overline{\text{KELALM}}$ alarm pin. These bits allow users to choose if they wish to have all or any information flagged to the alarm pin. The DUTGND pin has a 50 µA pull-up to allow for detection of an error in the DUTGND path. Setting this bit high also disables the 50 µA pull-up.
		9	Latched $\overline{\text{CLALM}}$	Set this latched bit high to program the open-drain $\overline{\text{CLALM}}$ clamp alarm pin as a latched output; leave low for an unlatched alarm pin (default).
		8	Disable $\overline{\text{CLALM}}$	Set this bit high to disable the open drain $\overline{\text{CLALM}}$ alarm pin; leave low to leave enabled (default).
		7	Latched $\overline{\text{GRDALM}}$	Set this latched bit high to program the $\overline{\text{GRDALM}}$ as a latched alarm on the open-drain $\overline{\text{KELALM}}$ pin; leave low for an unlatched alarm pin (default).
		6	Disable $\overline{\text{GRDALM}}$	Set this bit high to disable the $\overline{\text{GRDALM}}$ alarm function flagging the open-drain $\overline{\text{KELALM}}$ pin; leave low to leave enabled (default). The disable $\overline{\text{GRDALM}}$, $\overline{\text{DUTALM}}$ and $\overline{\text{OSALM}}$ alarm functions share one open-drain $\overline{\text{KELALM}}$ alarm pin. These bits allow users to choose if they wish to have all or any information flagged to the $\overline{\text{KELALM}}$ alarm pin.
		5:0	Unused	Set to 0.

Table 23. Diagnostic Register

Address	Default	Data Bits, MSB First					
0x7	0x0000	**Bit**	**Name**	**Function**			
		15 14 13 12	DIAG select[3:0]	DIAG select selects the set of diagnostic signals that can be made available on MEASOUT. First, use MEASOUT addressing (DPS Register 1) to select either the DIAG A or the DIAG B node to be made available on MEASOUT.			
				DIAG Select	**Selected Measure Block**	**DIAG A**	**DIAG B**
				0:3	Disabled	Disabled	Disabled
				4	Force amplifier	Disabled	Disabled
				5		EXTFORCE1A	EXTFORCE2A
				6		FINP	FINM
				7		Output 2.5 mA	Output 25 mA
				8	Measure block	VPTAT low	VPTAT high
				9		VTSD low (ref V for −273°C)	VTSD high (ref V for +130°C)
				10		MI	VMID Code
				11		MV	VMIN Code
				12	DAC block	FORCE DAC	VOS DAC
				13		CLL DAC	CLH DAC
				14		CPL DAC	CPH DAC
				15		OSD DAC	DGS DAC
				VPTAT low/VPTAT high are temperature sensor devices in the middle of the enabled power stage, which gives a voltage level that can be mapped back to the VTSD low and VTSD high reference points to get a temperature value. These sensors are used in the thermal shutdown feature. See the Die Temperature Sensor and Thermal Shutdown section. VMID code is the midscale voltage of the DACs; the offset DAC has a direct effect on this voltage level. VMIN code is the zero-scale voltage of the DACs; again the offset DAC has a direct effect.			
		11 10 9 8 7	TSENSE select[3:0]	The following codes allow selection of one of three sets of eight thermal diodes. The D+ of the selected thermal diode is available on the GPO pin; the D− is on the AGND. These thermal diodes are located across the die, in the cool parts and in the power stages. Diodes [16:23] are located in the force amplifier NPNs (power output devices for supplying current). Similarly, Diodes [24:31] are located in the force amplifier PNP devices (output devices for sinking current).			
				TSENSE Select	**Selected Thermal Block**	**Connected Sensor**	
				0:7	N/A—normal GPO operation	No sensor connected	
				8	Cool block	Cool end of high current drivers, hot side of digital block	
				9		25 mA output stage	
				10		Hottest part of sensitive measurement circuitry and cool part of force amplifier	
				11		Coolest end of force amplifier block	
				12		Coolest end of DACs	
				13		Beside TSENSE available on MEASOUT	
				14		Hottest part of DACs	
				15		Cool side of digital block	
				16	Force amplifier PNPs	1A-1	
				17		1A-2	
				18		2A (similar location to VPTAT low for EXTFORCE2 range)	
				19		1B-1 (similar location to VPTAT low for EXTFORCE1 range)	
				20		1B-2	
				21		2B	
				22		1C-1	
				23		1C-2	

Address	Default	Data Bits, MSB First				
0x7	0x0000	**Bit**	**Name**	**Function**		
				24	Force amplifier NPNs	1A-1
				25		1A-2
				26		2A (similar location to VPTAT high for EXTFORCE2 range)
				27		1B-1 (similar location to VPTAT high for EXTFORCE1 range)
				28		1B-2
				29		2B
				30		1C-1
				31		1C-2
		6 5	Test Force AMP[1:0]	These register bits allow disabling of stages of the force amplifier. They can be used to ensure connectivity in each parallel stage. The enabled stage depends also on which current range is selected.		
				Current Range	**Test Force Amplifier**	**Enabled Stage**
				EXTFORCE1	0	All stages
				EXTFORCE1	1	EXTFORCE1C
				EXTFORCE1	2	EXTFORCE1B
				EXTFORCE1	3	EXTFORCE1A
				EXTFORCE2	0	All stages
				EXTFORCE2	1	Reserved
				EXTFORCE2	2	EXTFORCE2B
				EXTFORCE2	3	EXTFORCE2A
		4:0	Reserved	Set to 0.		

Table 24. Other Registers

Address	Register	Default	Data Bits, MSB First
0x8	FIN DAC x1	0x8000	x1 DAC register; D15 to D0, MSB first.
0x9	FIN DAC m	0xFFFF	m register; D15 to D0, MSB first.
0xA	FIN DAC c	0x8000	c register; D15 to D0, MSB first.
0xB	Offset DAC x	0x8000	D15 to D0.
0xC	OSD DAC x	0x1FFF	D15 to D0.
0xD	CLL DAC x1	0x0000	D15 to D0; the low clamp level can only be negative; the MSB is always 0 to ensure this.
0xE	CLL DAC m	0xFFFF	D15 to D0.
0xF	CLL DAC c	0x8000	D15 to D0.
0x10	CLH DAC x1	0xFFFF	D15 to D0; the high clamp level can only be positive; the MSB is always 1 to ensure this.
0x11	CLH DAC m	0xFFFF	D15 to D0.
0x12	CLH DAC c	0x8000	D15 to D0.
0x13	CPL DAC x1 5 µA range	0x0000	D15 to D0.
0x14	CPL DAC m 5 µA range	0xFFFF	D15 to D0.
0x15	CPL DAC c 5 µA range	0x8000	D15 to D0.
0x16	CPL DAC x1 25 µA range	0x0000	D15 to D0.
0x17	CPL DAC m 25 µA range	0xFFFF	D15 to D0.
0x18	CPL DAC c 25 µA range	0x8000	D15 to D0.
0x19	CPL DAC x1 250 µA range	0x0000	D15 to D0.
0x1A	CPL DAC m 250 µA range	0xFFFF	D15 to D0.
0x1B	CPL DAC c 250 µA range	0x8000	D15 to D0.
0x1C	CPL DAC x1 2.5 mA range	0x0000	D15 to D0.
0x1D	CPL DAC m 2.5 mA range	0xFFFF	D15 to D0.
0x1E	CPL DAC c 2.5 mA range	0x8000	D15 to D0.
0x1F	CPL DAC x1 25 mA range	0x0000	D15 to D0.
0x20	CPL DAC m 25 mA range	0xFFFF	D15 to D0.
0x21	CPL DAC c 25 mA range	0x8000	D15 to D0.
0x22	CPL DAC x1 EXT Range 2	0x0000	D15 to D0.
0x23	CPL DAC m EXT Range 2	0xFFFF	D15 to D0.
0x24	CPL DAC c EXT Range 2	0x8000	D15 to D0.
0x25	CPL DAC x1 EXT Range 1	0x0000	D15 to D0.
0x26	CPL DAC m EXT Range 1	0xFFFF	D15 to D0.
0x27	CPL DAC c EXT Range 1	0x8000	D15 to D0.
0x28	CPH DAC x 1 5 µA range	0xFFFF	D15 to D0.
0x29	CPH DAC m 5 µA range	0xFFFF	D15 to D0.
0x2A	CPH DAC c 5 µA range	0x8000	D15 to D0.
0x2B	CPH DAC x1 25 µA range	0xFFFF	D15 to D0.
0x2C	CPH DAC m 25 mA range	0xFFFF	D15 to D0.
0x2D	CPH DAC c 25 µA range	0x8000	D15 to D0.
0x2E	CPH DAC x1 250 µA range	0xFFFF	D15 to D0.
0x2F	CPH DAC m 250 µA range	0xFFFF	D15 to D0.
0x30	CPH DAC c 250 µA range	0x8000	D15 to D0.
0x31	CPH DAC x1 2.5 mA range	0x0000	D15 to D0.
0x32	CPH DAC m 2.5 mA range	0xFFFF	D15 to D0.
0x33	CPH DAC c 2.5 mA range	0x8000	D15 to D0.
0x34	CPH DAC x1 25 mA range	0xFFFF	D15 to D0.
0x35	CPH DAC m 25 mA range	0xFFFF	D15 to D0.
0x36	CPH DAC c 25 mA range	0x8000	D15 to D0.
0x37	CPH DAC x1 EXT Range 2	0xFFFF	D15 to D0.
0x38	CPH DAC m EXT Range 2	0xFFFF	D15 to D0.
0x39	CPH DAC c EXT Range 2	0x8000	D15 to D0.
0x3A	CPH DAC x1 EXT Range 1	0xFFFF	D15 to D0.
0x3B	CPH DAC m EXT Range 1	0xFFFF	D15 to D0.

Address	Register	Default	Data Bits, MSB First
0x3C	CPH DAC c EXT Range 1	0x8000	D15 to D0.
0x3D	DGS DAC	0x3333	D15 to D0 DUTGND SENSE DAC, 0 V to 5 V range.
0x3E	Ramp end code	0x0000	D15 to D0; this is the ramp end code. The ramp start code is the code that is in the FIN DAC register.
0x3F	Ramp step size	0x0001	0000 0000 D6 to D0. D6:D0 set the ramp step size in increments of 16 LSB per code, with a 5 V reference, 16 LSB = 6.1 mV. For example, 000 0000 = 16 LSBs (6.1 mV) step 000 0001 = 16 LSBs (6.1 mV) step … 111 1111 = 2032 LSBs (775 mV) step.
0x40	RCLK divider	0x0001	0000 0000 D7 to D0. D7:D0 set the RCLK divider. 0000 0000 = ÷ 1 0000 0001 = ÷ 1 0000 0010 = ÷ 2 0000 0011 = ÷ 3 … 1111 1111 = ÷ 255
0x41	Enable ramp	0x0000	0xFFFF to enable.
0x42	Interrupt ramp	0x0000	0x0000 to interrupt.

Table 25. Alarm Status and Clear Alarm Status Register

Address	Register	Default	Data Bits, MSB first		
0x43	Alarm status	0x0000	This register is a read-only register providing information on the status of the alarm functions and the comparator outputs.		
			Bit	**Name**	**Function**
			15	$\overline{\text{LTMPALM}}$	Latched temperature alarm bit; if low, this bit indicates that an alarm event has occurred.
			14	$\overline{\text{TMPALM}}$	Unlatched alarm bit; if low, these bit indicates that an alarm event is still present.
			13	$\overline{\text{LOSALM}}$	Latched open-sense alarm bit; if low, indicates that an alarm event has occurred.
			12	$\overline{\text{OSALM}}$	Unlatched open-sense alarm bit; if low, indicates that an alarm event is still present.
			11	$\overline{\text{LDUTALM}}$	Latched DUTGND Kelvin sense alarm; if low, indicates that an alarm event has occurred.
			10	$\overline{\text{DUTALM}}$	Unlatched DUTGND Kelvin sense alarm; if low, indicates that an alarm event is still present.
			9	$\overline{\text{LCLALM}}$	Latched clamp alarm; if low, indicates that an alarm event has occurred.
			8	$\overline{\text{CLALM}}$	Unlatched clamp alarm; if low, indicates that an alarm event is still present.
			7	$\overline{\text{LGRDALM}}$	Latched guard alarm; if low, indicates that an alarm event has occurred.
			6	$\overline{\text{GRDALM}}$	Unlatched guard alarm; if low, indicates that an alarm event is still present.
			5	CPOL	Comparator output low condition as per the comparator output pin.
			4	CPOH	Comparator output high condition as per the comparator output pin.
			3:0	Unused	Must be zeros.
0x44	Alarm status and clear alarm	0x0000	This register is a read-only register providing information on the status of the alarm functions and the comparator outputs. Reading this register also automatically clears any latched alarm pins or bits.		
			Bit	**Name**	**Function**
			15	$\overline{\text{LTMPALM}}$	Latched temperature alarm bit; if low, this bit indicates that an alarm event has occurred.
			14	$\overline{\text{TMPALM}}$	Unlatched alarm bit; if low, these bit indicates that an alarm event is still present.
			13	$\overline{\text{LOSALM}}$	Latched open-sense alarm bit; if low, indicates that an alarm event has occurred.
			12	$\overline{\text{OSALM}}$	Unlatched open-sense alarm bit; if low, indicates that an alarm event is still present.
			11	$\overline{\text{LDUTALM}}$	Latched DUTGND Kelvin sense alarm; if low, indicates that an alarm event has occurred.
			10	$\overline{\text{DUTALM}}$	Unlatched DUTGND Kelvin sense alarm; if low, indicates that an alarm event is still present.
			9	$\overline{\text{LCLALM}}$	Latched clamp alarm; if low, indicates that an alarm event has occurred.
			8	$\overline{\text{CLALM}}$	Unlatched clamp alarm; if low, indicates that an alarm event is still present.
			7	$\overline{\text{LGRDALM}}$	Latched guard alarm; if low, indicates that an alarm event has occurred.
			6	$\overline{\text{GRDALM}}$	Unlatched guard alarm; if low, indicates that an alarm event is still present.
			5	CPOL	Comparator output low condition as per the comparator output pin.
			4	CPOH	Comparator output high condition as per the comparator output pin.
			3:0	Unused	Must be zeros.
0x45	CPL DAC x1	0x0000	D15 to D0. V_{SENSE} comparator low threshold.		
0x46	CPL DAC m	0xFFFF	D15 to D0. V_{SENSE} comparator low gain.		
0x47	CPL DAC c	0x8000	D15 to D0. V_{SENSE} comparator low offset.		
0x48	CPH DAC x1	0xFFFF	D15 to D0. V_{SENSE} comparator high threshold.		
0x49	CPH DAC m	0xFFFF	D15 to D0. V_{SENSE} comparator high gain.		
0x4A	CPH DAC c	0x8000	D15 to D0. V_{SENSE} comparator high offset.		
0x4B to 0x7F	Reserved		Reserved.		

READBACK MODE

The AD5560 allows data readback via the serial interface from every register directly accessible to the serial interface, which is all registers except the DAC register (x2 calibrated register). To read back contents of a register, it is necessary to write a 1 to the R/$\overline{W}$ bit, address the appropriate register, and fill the data bits with all zeros.

After the write command has been written, data from the selected register is loaded to the internal shift register and is available on the SDO pin during the next SPI operation.

Address 0x43 and Address 0x44 are the only registers that are read only. The read function gives the user details of the alarm status and the comparator output result.

Alarm flags on latched alarm pins (Pin 1, Pin 2, Pin 3) and bits are cleared after a read command of Register 0x44 (alarm status and clear alarm register (see Table 25)).

SCLK frequency for readback does not operate at the full speed of the SPI interface. See the Timing Characteristics section for further details.

DAC READBACK

The DAC x1, DAC m, and DAC c registers are available to read back via the serial interface. Access to the calibrated x2 register is not available.

POWER-ON DEFAULT

During power-on, the power-on state machine resets all internal registers to their default values, and $\overline{BUSY}$ goes low. A rising edge on $\overline{BUSY}$ indicates that the power-on event is complete and that the interface is enabled. The $\overline{RESET}$ pin has no function in the power-on event.

During power-on, all DAC x1 registers corresponding to 0 V are cleared; the calibration register default corresponds to m at full scale and to c at zero scale.

The default conditions of the DPS and the system control registers are as shown in the relevant tables (see Table 17 through Table 26).

During a $\overline{RESET}$ function, all registers are reset to the power-on default.

Table 26. AD5560 Truth Table of Switches[1]

Reg	Bit Name	Bit	SW1	SW2	SW3	SW4	SW7	SW13	SW14	SW15	SW5	SW6	SW8	SW9	SW11	SW16
System Control Register	Gain0, Gain1		X	X	X	X	X	X	X	X	X	X	X	X	X	X
	FINGND	0	B	X	X	X	X	X	X	X	X	X	X	X	X	X
		1	A	X	X	X	X	X	X	X	X	X	X	X	X	X
	CPO		X	X	X	X	X	X	X	X	X	X	X	X	X	X
	$\overline{PD}$[2, 3]		X	X	X	X	X	X	X	X	X	X	X	X	X	On
DPS Register 1	$\overline{SW\text{-}INH}$[2]	0[4]	X	c	X	X	X	X	X	X	X	X	X	X	X	X
		1[5]	X	a	X	X	X	X	X	X	X	X	X	X	X	X
	I2, I1, I0	000	X	X	X	On	On	Off	Off	Off	X	X	X	X	X	X
		001	X	X	X	On	On	Off	Off	Off	X	X	X	X	X	X
		010	X	X	X	On	On	Off	Off	Off	X	X	X	X	X	X
		011	X	X	X	On	On	Off	Off	Off	X	X	X	X	X	X
		100	X	X	X	On	On	Off	Off	Off	X	X	X	X	X	X
		101	X	X	X	Off	Off	Off	On	On	X	X	X	X	X	X
		110	X	X	X	Off	Off	On	Off	On	X	X	X	X	X	X
	CMP1, CMP0	00	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		01	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		10	X	X	a	X	X	X	X	X	X	X	X	X	X	X
		11	X	X	b	X	X	X	X	X	X	X	X	X	X	X
	ME3, ME2, ME1, ME0	000	X	X	X	X	X	X	X	X	X	X	X	X	X	Off
		001	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		010	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		011	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		100	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		101	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		110	X	X	X	X	X	X	X	X	X	X	X	X	X	On
		111	X	X	X	X	X	X	X	X	X	X	X	X	X	On
DPS Register 2	SF0	0	X	X	X	X	X	X	X	X	X	X	Off	Off	X	X
		1	X	X	X	X	X	X	X	X	X	X	On	On	X	X
	Slave, GANGIMODE	00[6]	b	a	X	X	X	X	X	X	a	Off	X	X	X	X
		01[7]	b	a	X	X	X	X	X	X	b	Off	X	X	X	X
		10[8]	c	c	X	X	X	X	X	X	Off	On	X	X	X	X
		11[9]	c	b	X	X	X	X	X	X	Off	On	X	X	X	X
	INT10K	0	X	X	X	X	X	X	X	X	X	X	X	X	Off	X
		1	X	X	X	X	X	X	X	X	X	X	X	X	On	X
Hardware Pins	$\overline{HW\_INH}$[2]		X	c	X	X	X	X	X	X	X	X	X	X	X	X
	CLEN		X	X	X	X	X	X	X	X	X	X	X	X	X	X

[1] X = don't care; the switch is unaffected by the particular bit condition.
[2] Active low.
[3] Power-down mode; used for low power consumption.
[4] Force amplifier outputs tristate, low leakage mode; feedback made around amplifier.
[5] FV mode.
[6] Master: MASTER_OUT = internally connects to active EXTFORCE1/EXTFORCE2/25 mA output.
[7] Master: MASTER_OUT = master MI.
[8] Slave FV: EXTFORCE1/EXTFORCE2/25 mA connected internally to close the FVAMP loop.
[9] Slave FI.

USING THE HCAV$_{DD}$x AND HCAV$_{SS}$x SUPPLIES

The first set of power supplies, AV$_{DD}$ and AV$_{SS}$, provide power to the DAC levels and associated circuitry. They also supply the force amplifier stage for the low current ranges (ranges using internal sense resistors up to 25 mA maximum).

The second set of power supplies, HCAV$_{SS}$1 and HCAV$_{DD}$1, are intended to be used to minimize power consumption in the AD5560 device for the EXTFORCE1 range (up to ±1.2 A). Similarly, the HCAV$_{SS}$2 and HCAV$_{DD}$2 supplies are used for the EXTFORCE2 range (up to ±500 mA). These supplies must be less than or equal to the AV$_{DD}$ and AV$_{SS}$ supplies. When driving high currents at low voltages, power can be greatly minimized by ensuring that the supplies are at the lowest voltages.

Therefore, HCAV$_{SS}$x and HCAV$_{DD}$x can be switched externally to different power rails as required by the set voltage range. However, the design of the high current output stage means that these supplies always have to be at a higher voltage than the forced voltage, irrespective of the current range being used. Therefore, depending on the level of supply switching, external diodes may be required in series with each of the HCAV$_{DD}$x and HCAV$_{SS}$x supplies, as shown in Figure 60. There are internal pull-up resistors between the supplies (see Figure 60). Using diodes here allows a more flexible use of supplies and can minimize the amount of supply switching required. In the example, the AV$_{DD}$ and AV$_{SS}$ supplies can support the high voltage needs, whereas the HCAV$_{DD}$x and HCAV$_{SS}$x supplies support the low voltage, higher current ranges. Diode selection should take into account the current carrying requirements. Supply selection for HCAV$_{DD}$x and HCAV$_{SS}$x supplies must allow for this extra voltage drop.

POWER SUPPLY SEQUENCING

When the supplies are connected to the AD5560, it is important that the AGND and DGND pins be connected to the relevant ground plane before the positive or negative supplies are applied. In most applications, this is not an issue because the ground pins for the power supplies are connected to the ground pins of the AD5560 via ground planes. The AV$_{DD}$ and AV$_{SS}$ supplies must be applied to the device either before or at the same time as the HCAV$_{DD}$x and HCAV$_{SS}$x supplies, as indicated in Table 3. There are no known supply sequences surrounding the DV$_{CC}$ supply, although it is recommended that it be applied as indicated by the absolute maximum ratings (see Table 3).

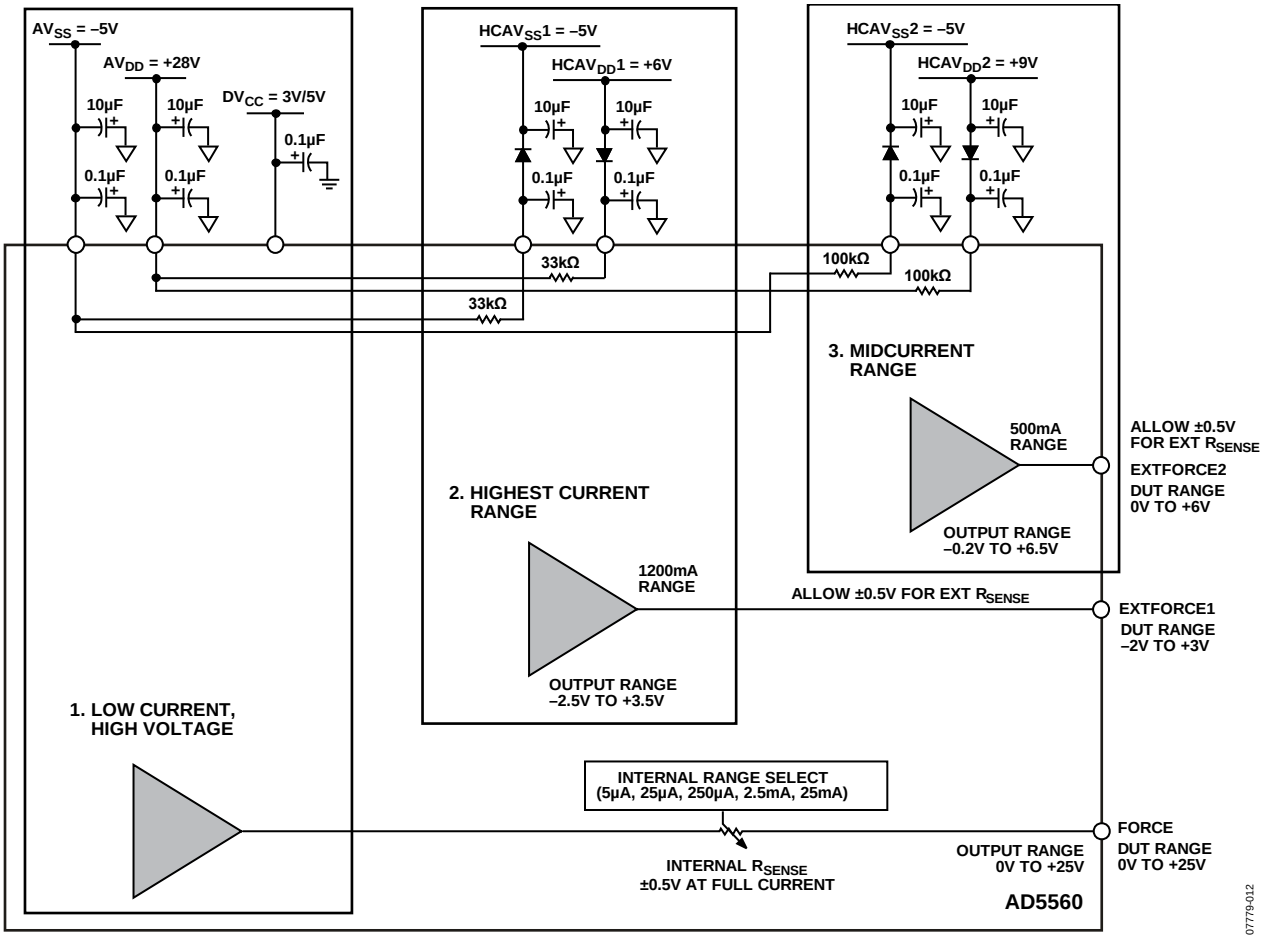

Figure 60. Example of Using the Extra Supply Rails Within the AD5560 to Achieve Multiple Voltage/Current Ranges

REQUIRED EXTERNAL COMPONENTS

The minimum required external components are shown in the block diagram in Figure 61. Decoupling is very dependent on the type of supplies used, the board layout, and the noise in the system. It is possible that less decoupling may be required as a result. Although there are four compensation input pins and five feedforward capacitor input pins, all capacitor inputs may be used only if the user intends to drive large variations of DUT load capacitances. If the DUT load capacitance is known and does not change for all combinations of voltage ranges and test conditions, then it is possible only one set of C_{Cx} and C_{Fx} is required.

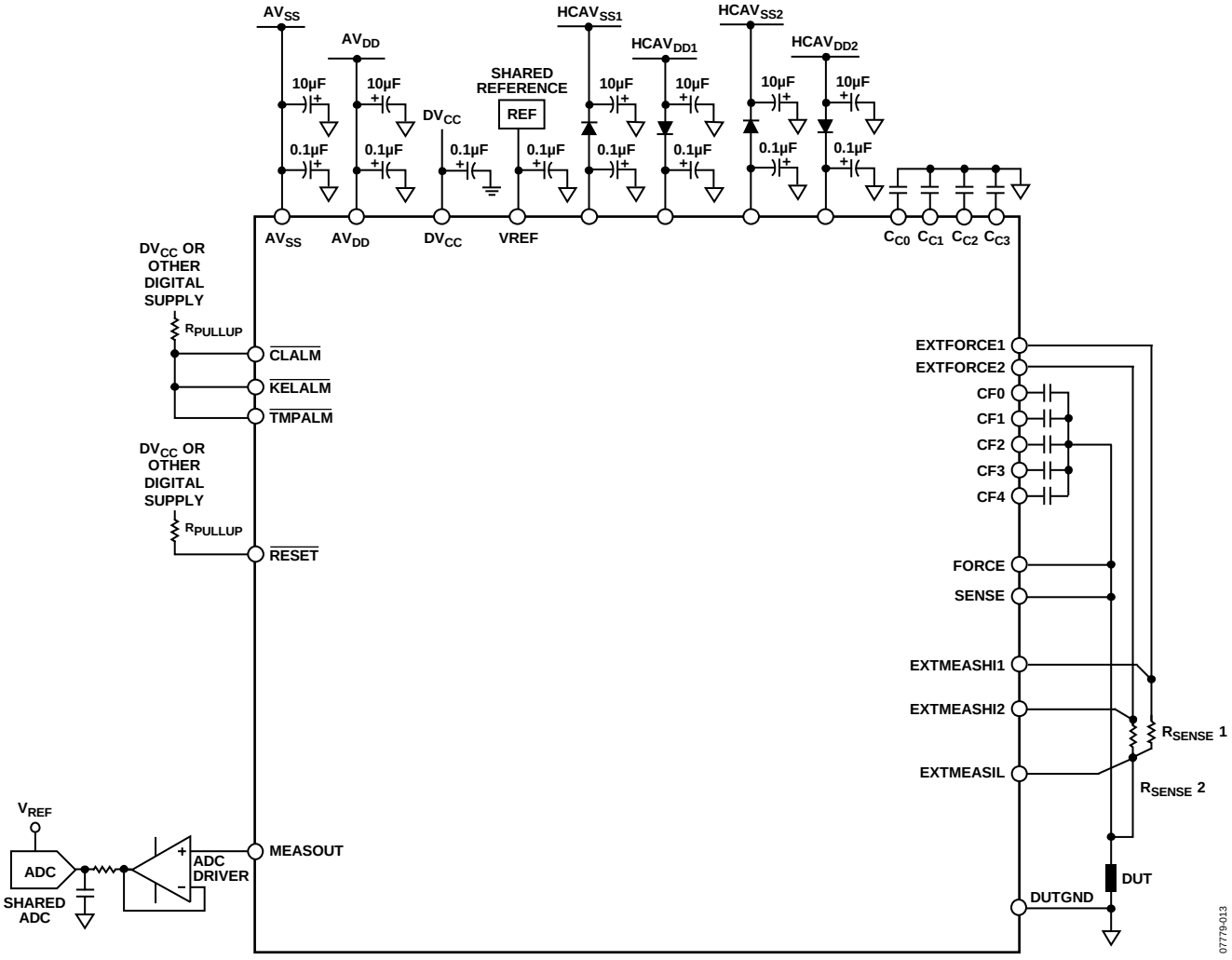

Figure 61. External Components Required for Use with the DPS

Table 27. References Suggested for Use with the AD5560[1]

Part No.	Voltage (V)	Initial Accuracy %	Ref Out Tempco (ppm/°C max) A/B Grade	Ref Output Current (mA)	Supply Voltage Range (V)	Package
ADR431	2.5	±0.04	10/3	30	4.5 to 18	MSOP, SOIC
ADR435	5	±0.04	10/3	30	7 to 18	MSOP, SOIC
ADR441	2.5	±0.04	10/3	10	3 to 18	MSOP, SOIC
ADR445	5	±0.04	10/3	10	5.5 to 18	MSOP, SOIC

[1] Subset of the possible references suitable for use with the AD5560. See http://www.analog.com/references for more options.

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5560 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5560 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. The DGND connection in the AD5560 should be treated as AGND and returned to the AGND plane. For more detail on decoupling for mixed signal applications, refer to Analog Devices Tutorial MT 031.

For supplies with multiple pins (AV_{SS}, AV_{DD}, DV_{CC}), it is recommended to tie these pins together and to decouple each supply once.

The AD5560 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the part as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESL), such as the common ceramic capacitors that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided because these couple noise onto the device. The analog ground plane should be allowed to run under the AD5560 to avoid noise coupling. The power supply lines of the AD5560 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. It is essential to minimize noise on all VREF lines. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough throughout the board. As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

Also note that the exposed paddle of the AD5560 is internally connected to the negative supply AV_{SS}.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

Table 28. Thermal Resistance for TQFP_EP[1]

Cooling	Airflow (LFPM)	θ_{JA}[2]	$\theta_{JC\ (Uniform)}$[3]	$\theta_{JC\ (Local)}$[4] Ideal TIM[6]	$\theta_{JC\ (Local)}$ w/TIM[6]	θ_{JCP} w/TIM[5]	Unit
No Heat Sink	0	39				N/A	°C/W
	200	37.2					°C/W
	500	35.7					°C/W
Heat Sink[7]	0	12.2				N/A	°C/W
	200	11.1	1.0	2.8	4.91		°C/W
	500	9.5					°C/W
Cold Plate[8]	N/A	N/A	1.0	2.8	4.91	7.5	°C/W

[1] All numbers are simulated and assume a JEDEC 4-layer test board.
[2] θ_{JA} is the thermal resistance from hottest junction to ambient air.
[3] $\theta_{JC\ (Uniform)}$ is the thermal resistance from junction to the package top, assuming total power is uniformly distributed.
[4] $\theta_{JC\ (Local)}$ is the thermal resistance from junction to the center of package top, assuming total power = 8.5 W (1 W uniformly distributed, 7.5 W in power stages—local heating).
[5] θ_{JCP} is the thermal resistance from hottest junction to infinite cold plate with consideration of thermal interface material (TIM).
[6] Ideal TIM is assuming top of package in perfect contact with an infinite cold plate. w/TIM is assuming TIM is 0.5 mm thick, with thermal conductivity of 2.56 W/m/k.
[7] Heat sink with a rated performance of θ_{CA} ~5.3°C/W under forced convection, gives ~T_J = 111°C at 500 LFM. Thermal performance of the package depends on the heat sink and environmental conditions.
[8] Attached infinite cold plate should be ≤26°C to maintain T_J < 90°C, given total power = 8.5 W. Thermal performance of the package depends on the heat sink and environmental conditions.
[9] To estimate junction temperature, the following equations can be used:

$$T_J = T_{amb} + \theta_{JA} \times Power$$
$$T_J = T_{cold\ plate} + \theta_{JCP} \times Power$$
$$T_J = T_{top} + \theta_{JC} \times Power$$

Table 29. Thermal Resistance for Flip Chip BGA[1]

Cooling	Airflow (LFPM)	θ_{JA}[2]	$\theta_{JC\ (Uniform)}$[3]	$\theta_{JC\ (Local)}$[4] Ideal TIM[6]	$\theta_{JC\ (Local)}$ w/TIM[6]	θ_{JCP}[5] w/TIM	Unit
No Heat Sink	0	40.8				N/A	°C/W
	200	38.1					°C/W
	500	36					°C/W
Heat Sink[8]	0	18				N/A	°C/W
	200	11.8	0.05	1.6	4.6		°C/W
	500	9					°C/W
Cold Plate[9]	N/A	N/A	0.05	1.6	4.6	6.5	°C/W

[1] All numbers are simulated and assume a JEDEC 4-layer test board.
[2] θ_{JA} is the thermal resistance from hottest junction to ambient air.
[3] $\theta_{JC\ (Uniform)}$ is the thermal resistance from junction to the package top, assuming total power is uniformly distributed.
[4] $\theta_{JC\ (Local)}$ is the thermal resistance from junction to the center of package top, assuming total power = 8.5 W (1 W uniformly distributed, 7.5 W in power stages—local heating).
[5] θ_{JCP} is the thermal resistance from hottest junction to infinite cold plate with consideration of thermal interface material (TIM).
[6] Ideal TIM is assuming top of package in perfect contact with an infinite cold plate. w/TIM is assuming TIM is 0.4 mm thick, with thermal conductivity of 3.57 W/m/k.
[7] Heat sink with a rated performance of θ_{CA} ~4.9°C/W under forced convection, gives ~T_J = 112°C at 500 LFM. Thermal performance of the package depends on the heat sink and environmental conditions.
[8] Attached infinite cold plate should be ≤30°C to maintain T_J < 90°C, given total power = 8.5 W. Thermal performance of the package depends on the heat sink and environmental conditions.
[9] To estimate junction temperature, the following equations can be used:

$$T_J = T_{amb} + \theta_{JA} \times Power$$
$$T_J = T_{cold\ plate} + \theta_{JCP} \times Power$$
$$T_J = T_{top} + \theta_{JC} \times Power$$

TEMPERATURE CONTOUR MAP ON THE TOP OF THE PACKAGE

TQFP_EP Package

Due to localized heating, temperature at the top surface of the package has steep gradient. Thus, the θ_{JC} value is highly dependent on where the case temperature is measured. Figure 62 shows the top of the die temperature contour map for the TQFP_EP.

BGA Package

Due to localized heating, temperature at the top surface of the package has steep gradient. Thus, the θ_{JC} value is highly dependent on where the case temperature is measured. Figure 63 shows the top of the die temperature contour map for the flip chip BGA.

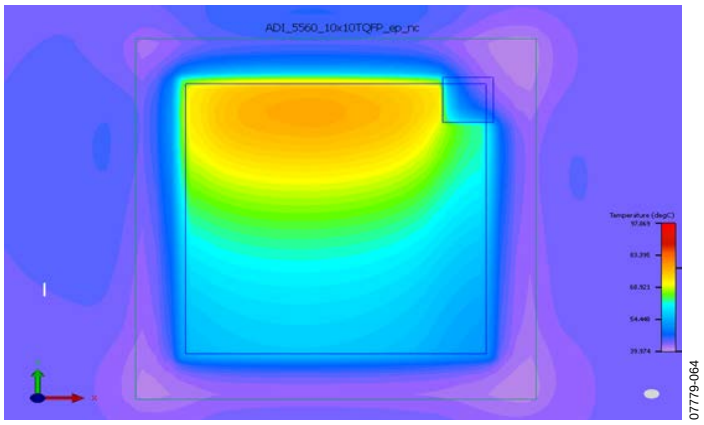

Figure 62. Temperature Contour Map for 64-Lead TQFP_EP

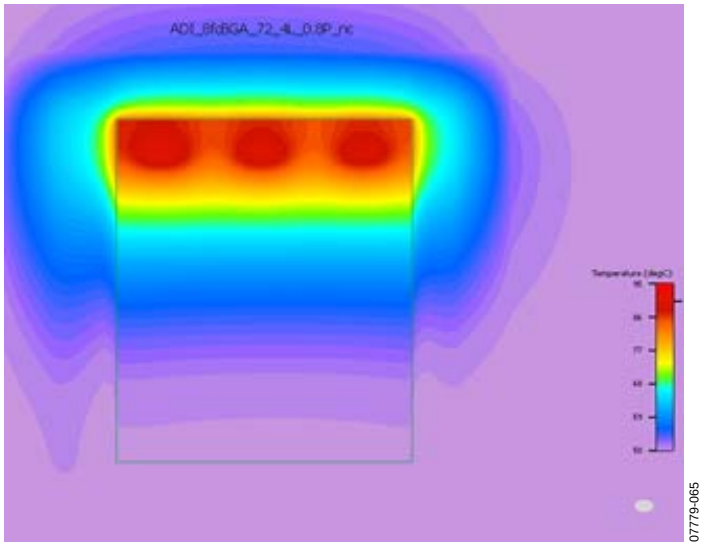

Figure 63. Temperature Contour Map for the Flip Chip BGA

OUTLINE DIMENSIONS

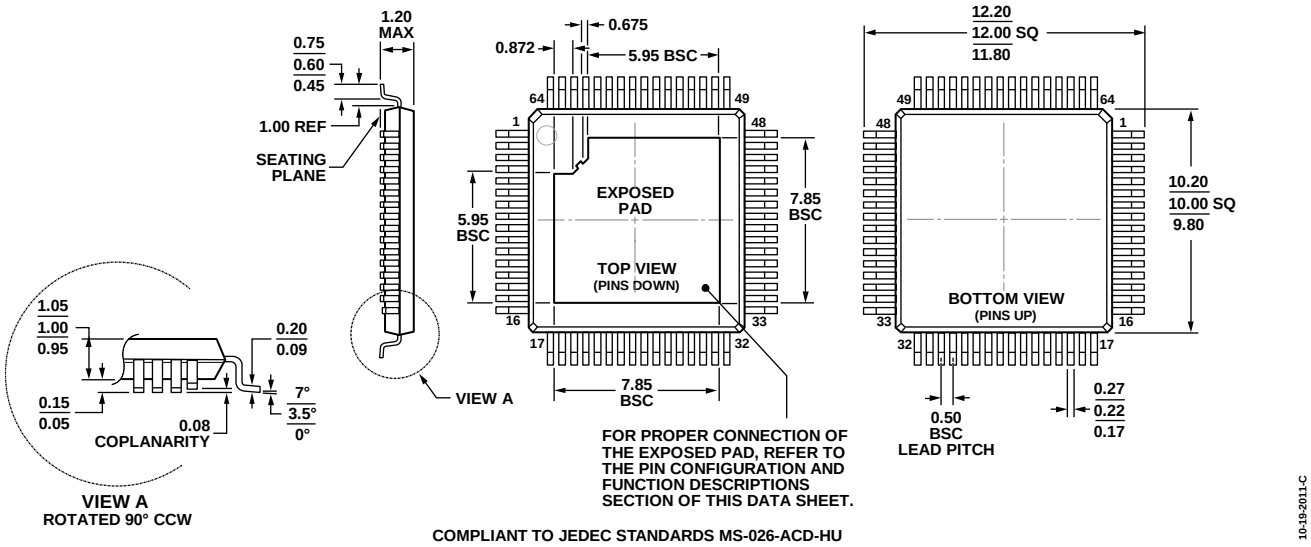

Figure 64. 64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-64-3)
Dimensions shown in millimeters

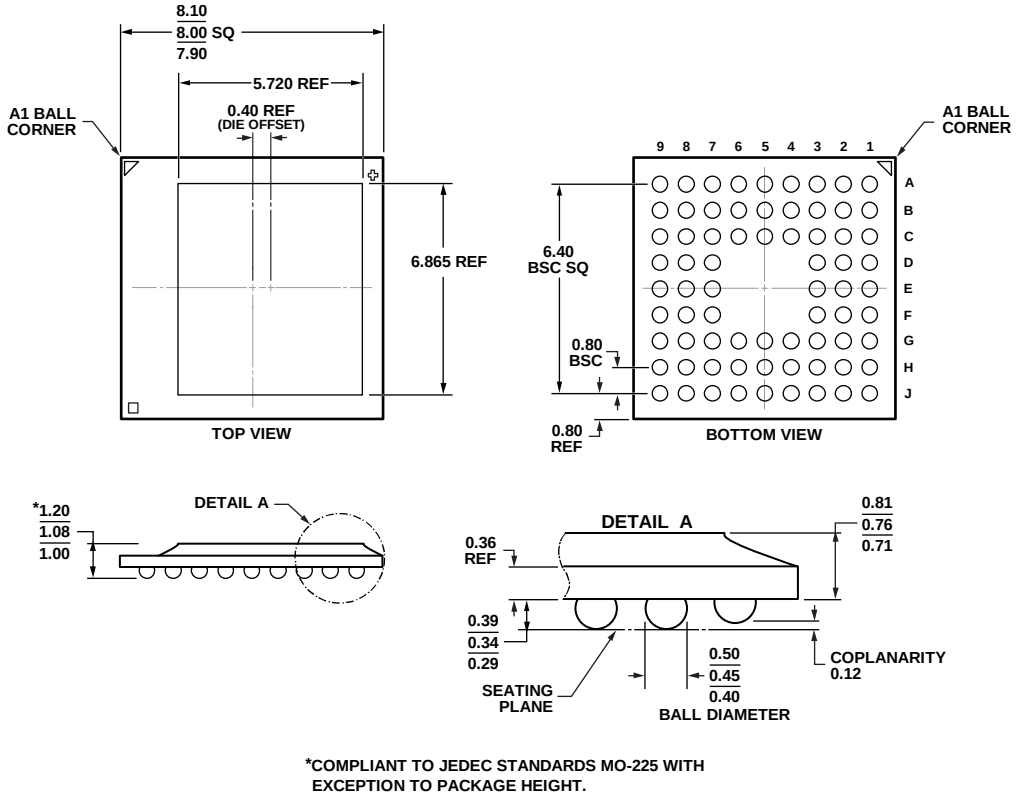

Figure 65. 72-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-72-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
AD5560JSVUZ	T_J = 25°C to +90°C	64-Lead Thin Quad Flat Pack with Exposed Pad (TQFP_EP)	SV-64-3
AD5560JSVUZ-REEL	T_J = 25°C to +90°C	64-Lead Thin Quad Flat Pack with Exposed Pad (TQFP_EP)	SV-64-3
AD5560JBCZ	T_J = 25°C to +90°C	72-Ball Chip Scale Package Ball Grid Array (CSP-BGA)	BC-72-2
AD5560JBCZ-REEL	T_J = 25°C to +90°C	72-Ball Chip Scale Package Ball Grid Array (CSP-BGA)	BC-72-2
EVAL-AD5560EBUZ		Evaluation Kit	

[1] Z = RoHS Compliant Part.
[2] T_J = junction temperature.

D07779-0-5/16(E)

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