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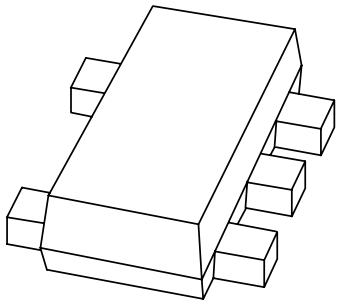
DATA SHEET



BZA900A-series
Quadruple ESD transient voltage suppressor

Product data sheet

2001 Sep 03

Quadruple ESD transient voltage suppressor

BZA900A-series

FEATURES

- ESD rating >8 kV, according to IEC61000-4-2
- SOT665 surface mount package
- Common anode configuration.

APPLICATIONS

- Computers and peripherals
- Audio and video equipment
- Communication systems

DESCRIPTION

Monolithic transient voltage suppressor diode in a five lead SOT665 package for 4-bit wide ESD transient suppression.

MARKING

TYPE NUMBER	MARKING CODE
BZA956A	Z1
BZA962A	Z2
BZA968A	Z3

PINNING

PIN	DESCRIPTION
1	cathode 1
2	common anode
3	cathode 2
4	cathode 3
5	cathode 4

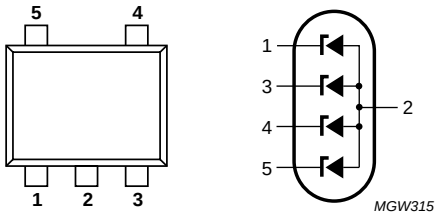


Fig.1 Simplified outline (SOT665) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
I_Z	working current	T_{amb} = 25 °C	–	note 1	mA
I_F	continuous forward current	T_{amb} = 25 °C	–	200	mA
I_{FSM}	non-repetitive peak forward current	t_p = 1 ms; square pulse	–	4	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 2; see Fig.5	–	335	mW
P_{ZSM}	non repetitive peak reverse power dissipation:	square pulse; t_p = 1 ms; see Fig.3			
	BZA956A		–	16	W
	BZA962A		–	15	W
	BZA968A		–	14	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Notes

1. DC working current limited by $P_{tot(max)}$.
2. Device mounted on standard printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	all diodes loaded	370	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to solder point; note 1	one diode loaded	135	K/W
		all diodes loaded	125	K/W

Note

1. Solder point of common anode (pin 2).

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	I_F = 200 mA	1.3	V
I_R	reverse current			
	BZA956A	V_R = 3 V	1000	nA
	BZA962A	V_R = 4 V	500	nA
	BZA968A	V_R = 4.3 V	100	nA

Table 1 Per type; BZ956A to BZA968A

T_j = 25 °C unless otherwise specified.

TYPE	WORKING VOLTAGE V_Z (V) at I_Z = 1 mA			DIFFERENTIAL RESISTANCE r_{dif} (Ω) at I_Z = 1 mA	TEMP. COEFF. S_Z (mV/K) at I_Z = 1 mA	DIODE CAP. C_d (pF) at f = 1 MHz; V_R = 0	NON-REPETITIVE PEAK REVERSE CURRENT I_{ZSM} (A) at t_p = 1 ms; T_{amb} = 25 ×°C
	MIN.	TYP.	MAX.	MAX.	TYP.	MAX.	MAX.
BZA956A	5.32	5.6	5.88	400	0.3	125	2.2
BZA962A	5.89	6.2	6.51	300	1.6	105	2.1
BZA968A	6.46	6.8	7.14	200	2.2	90	2.0

GRAPHICAL DATA

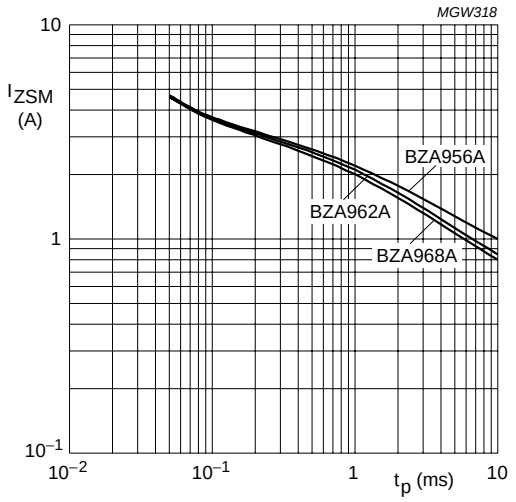
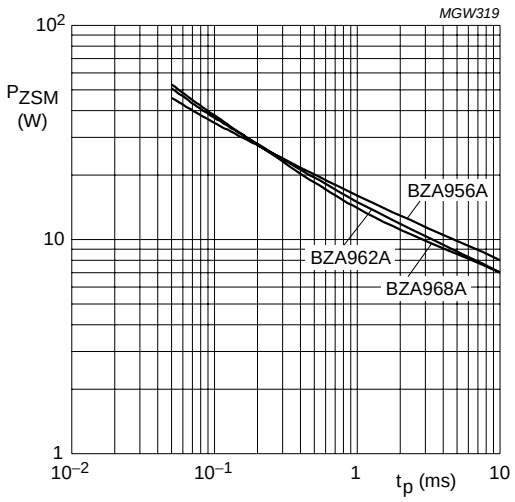
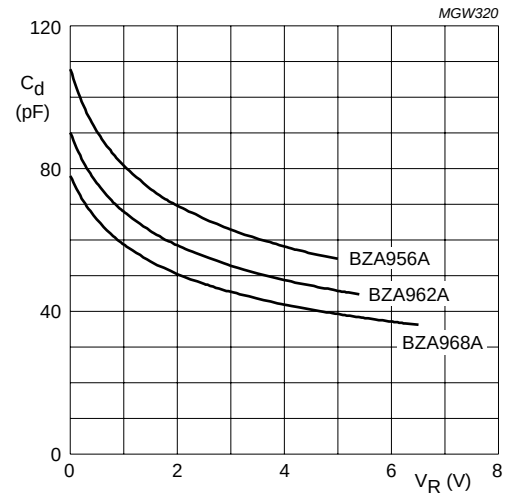


Fig.2 Maximum non-repetitive peak reverse current as a function of pulse time.



$P_{ZSM} = V_{ZSM} \times I_{ZSM}$.
V_{ZSM} is the non-repetitive peak reverse voltage at I_{ZSM}.

Fig.3 Maximum non-repetitive peak reverse power dissipation as a function of pulse duration (square pulse).



T_j = 25 °C; f = 1 MHz.

Fig.4 Diode capacitance as a function of reverse voltage; typical values.

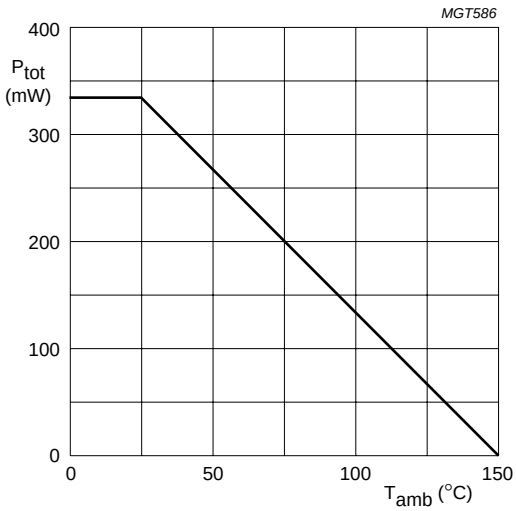
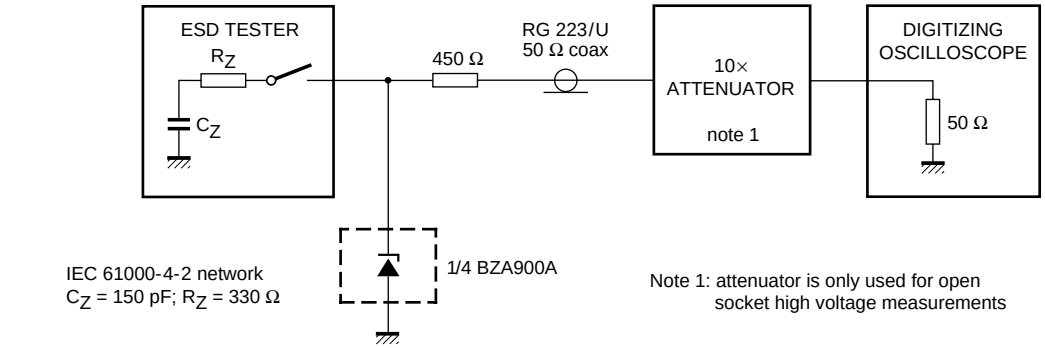
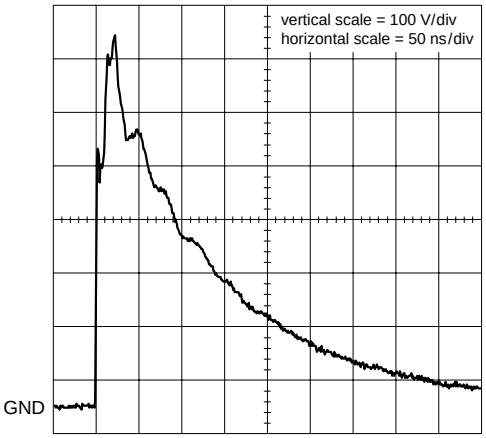
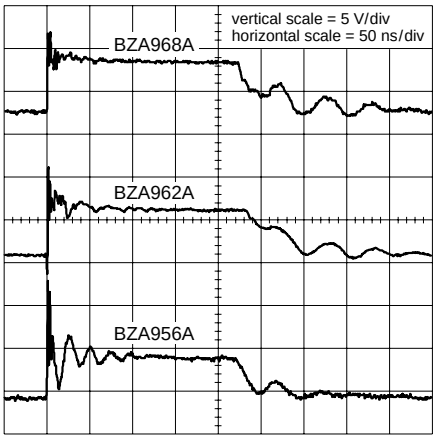


Fig.5 Power derating curve.

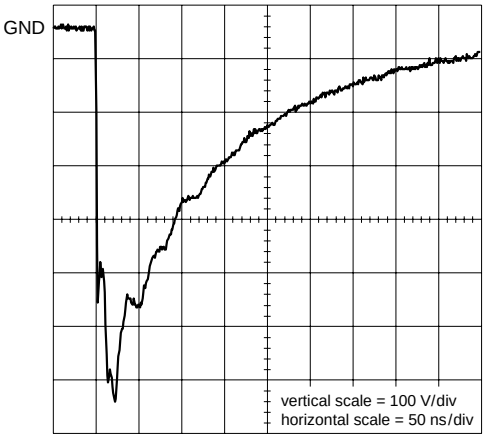




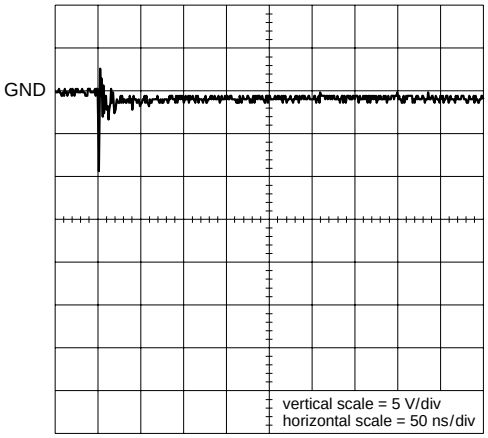
unclamped +1 kV ESD voltage waveform (IEC 61000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC 61000-4-2 network)



unclamped −1 kV ESD voltage waveform (IEC 61000-4-2 network)



clamped −1 kV ESD voltage waveform (IEC 61000-4-2 network)

MGW321

Fig.6 ESD clamping test set-up and waveforms.

APPLICATION INFORMATION

Typical common anode application

A quadruple transient suppressor in a SOT665 package makes it possible to protect four separate lines using only one package. A simplified example is shown in Fig.7.

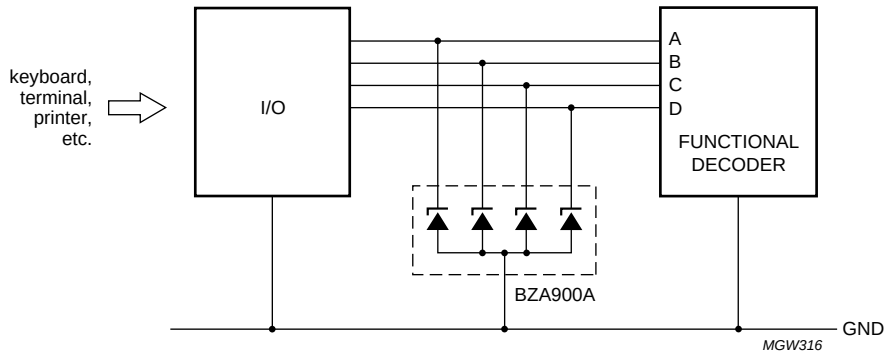


Fig.7 Computer interface protection.

Device placement and printed-circuit board layout

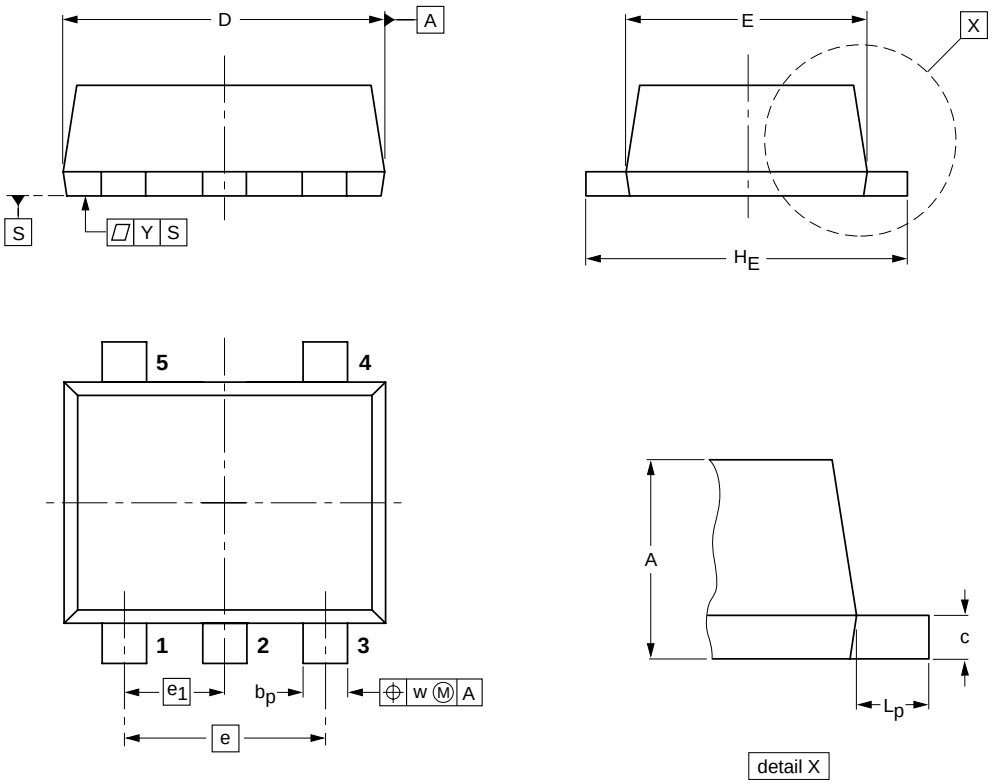
Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA900A is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage (V = L di/dt) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors
2. Keep parallel signal paths to a minimum
3. Avoid running protection conductors in parallel with unprotected conductors
4. Minimize all printed-circuit board loop areas including power and ground loops
5. Minimize the length of the transient return path to ground
6. Avoid using shared transient return paths to a common ground point.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT665**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT665						~~01-01-04~~ 01-08-27

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

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