CS43L21

Low-Power, Stereo Digital-to-Analog Converter

FEATURES

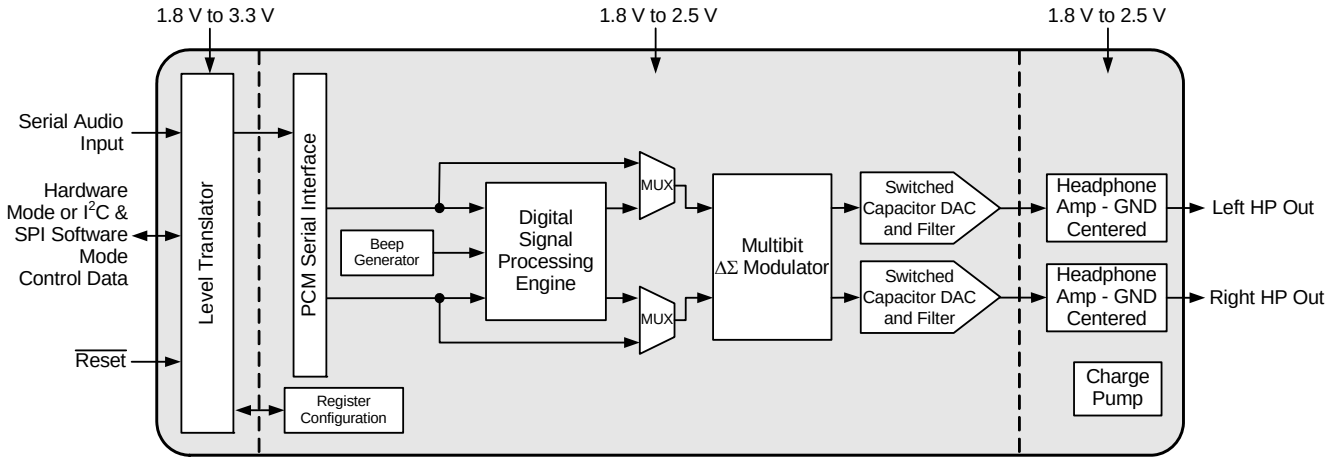
- 98 dB dynamic range (A-weighted)
- -86 dB THD+N
- Headphone amplifier–GND centered
  - On-chip charge pump provides -VA_HP
  - No DC-blocking capacitor required
  - 46 mW power into stereo 16 Ω @ 1.8 V
  - 88 mW power into stereo 16 Ω @ 2.5 V
  - -75 dB THD+N
- Digital signal processing engine
  - Bass and treble tone control, de-emphasis
  - PCM mix with independent volume control
  - Master digital volume control and limiter
  - Soft-ramp and zero-cross transitions
- Beep generator
  - Tone selections across two octaves
  - Separate volume control
  - Programmable On and Off time intervals
  - Continuous, periodic, or one-shot beep selections
- Programmable peak-detect and limiter
- Pop and click suppression

SYSTEM FEATURES

- 24-bit Conversion
- 4- to 96-kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo playback: 12.93 mW @ 1.8 V
- Variable power supplies
  - 1.8- to 2.5-V digital and analog
  - 1.8- to 3.3-V interface logic
- Power-down management
- Software Mode (I²C™ and SPI™ control)
- Hardware mode (standalone control)
- Digital routing/mixes:
  - Mono mixes
- Flexible clocking options
  - Master or slave operation
  - High-impedance digital output option (for easy MUXing between DAC and other data sources)
  - Quarter-speed mode (allows 8-kHz Fs while maintaining a flat noise floor up to 16 kHz)

APPLICATIONS

- Portable audio players
- MD players
- PDAs
- Personal media players
- Portable game consoles
- Smart phones
- Wireless headsets



GENERAL DESCRIPTION

The CS43L21 is a highly integrated, 24-bit, 96 kHz, low power stereo DAC. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. The DAC offers many features suitable for low power, portable system applications.

The DAC output path includes a digital signal processing engine. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Mixer allows independent volume control for PCM mix, as well as a master digital volume control for the analog output. All volume level changes may be configured to occur on soft ramp and zero cross transitions. The DAC also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The stereo headphone amplifier is powered from a separate positive supply and the integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

In addition to its many features, the CS43L21 operates from a low-voltage analog and digital core, making this DAC ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS43L21 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CS43L21 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see “Ordering Information” on page 64 for complete details.

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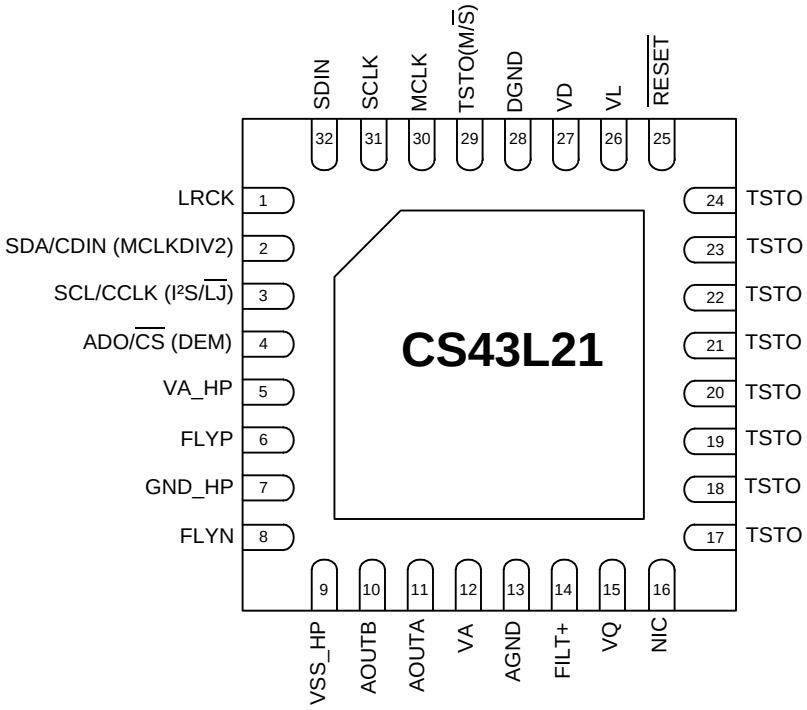
1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.
		MCLK Divide by 2 (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I²S/LJ)	3	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
		Interface Format Selection (*Input*) - Hardware Mode: Selects between I²S & Left-Justified interface formats for the DAC.
AD0/CS (DEM)	4	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
		De-Emphasis *(Input)* - Hardware Mode: Enables/disables the de-emphasis filter.
VA_HP	5	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
FLYP	6	**Charge Pump Cap Positive Node** *(Input)* **-** Positive node for the external charge pump capacitor.
GND_HP	7	**Analog Ground** (*Input*) - Ground reference for the internal headphone/charge pump section.
FLYN	8	**Charge Pump Cap Negative Node** *(Input)* **-** Negative node for the external charge pump capacitor.
VSS_HP	9	**Negative Voltage From Charge Pump** *(Output)* **-** Negative voltage rail for the internal analog headphone section.

AOUTB AOUTA	10 11	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
VA	12	**Analog Power** (*Input*) - Positive power for the internal analog section.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	14	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	15	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
NIC	16	**Not Internally Connected -** This pin is not connected internal to the device and may be connected to ground or left “floating”. No other external connection should be made to this pin.
TSTO	17	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
TSTO	18	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
TSTO	19	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
TSTO	20	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
TSTO	21 22	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
TSTO	23 24	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
$\overline{\text{RESET}}$	25	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	26	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	28	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
TSTO (M/$\overline{\text{S}}$)	29	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin). **Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	31	**Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface.
SDIN	32	**Serial Audio Data Input** (*Input*) - Input for two’s complement serial audio data.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See “QFN Thermal Pad” on page 60.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
$\overline{\text{RESET}}$	Input	-	1.8 V - 3.3 V
SCL/CCLK ($I^2S/\overline{LJ}$)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/$\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
TSTO ($M/\overline{S}$)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDIN	Input	-	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

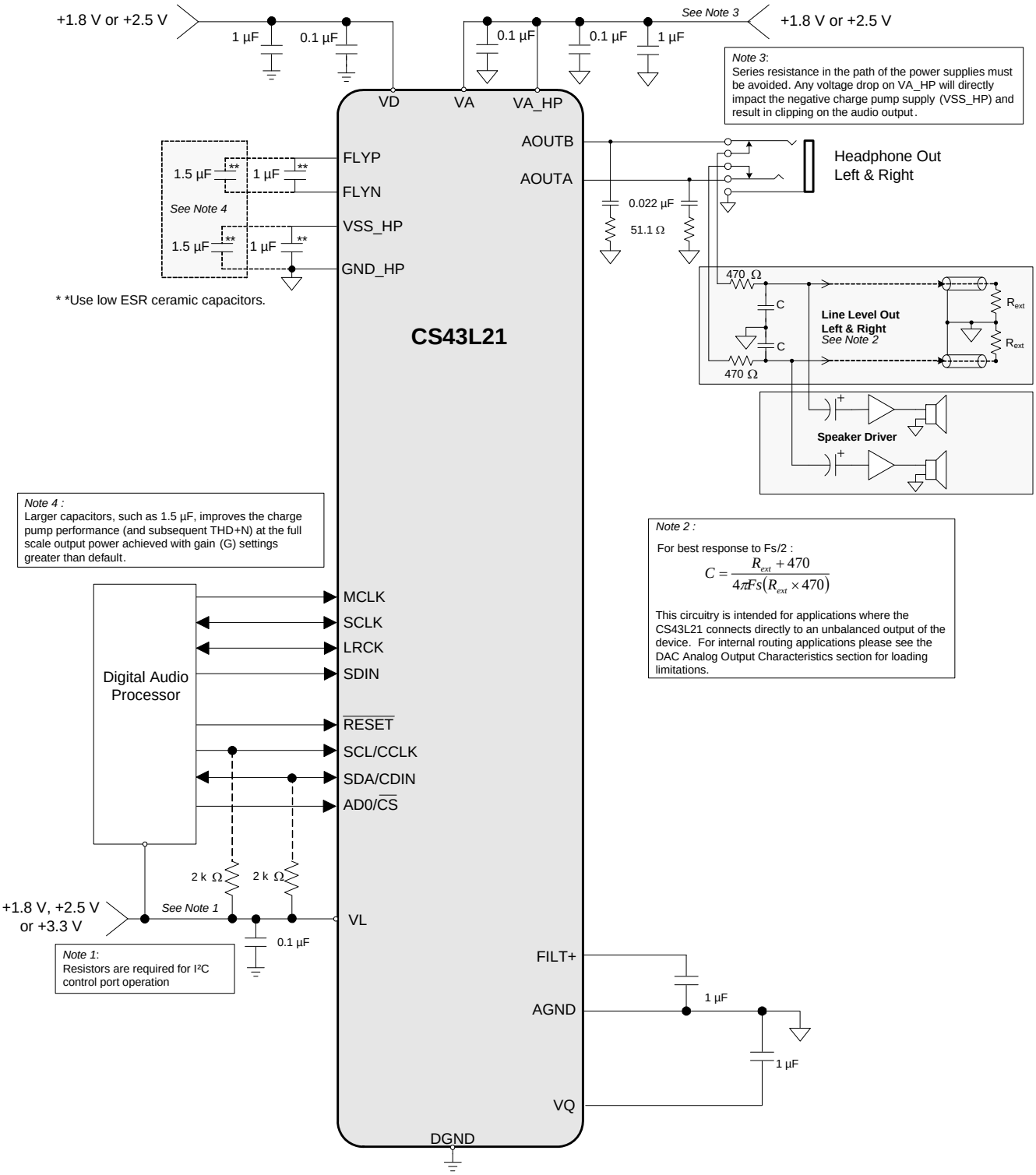


Figure 1. Typical Connection Diagram (Software Mode)

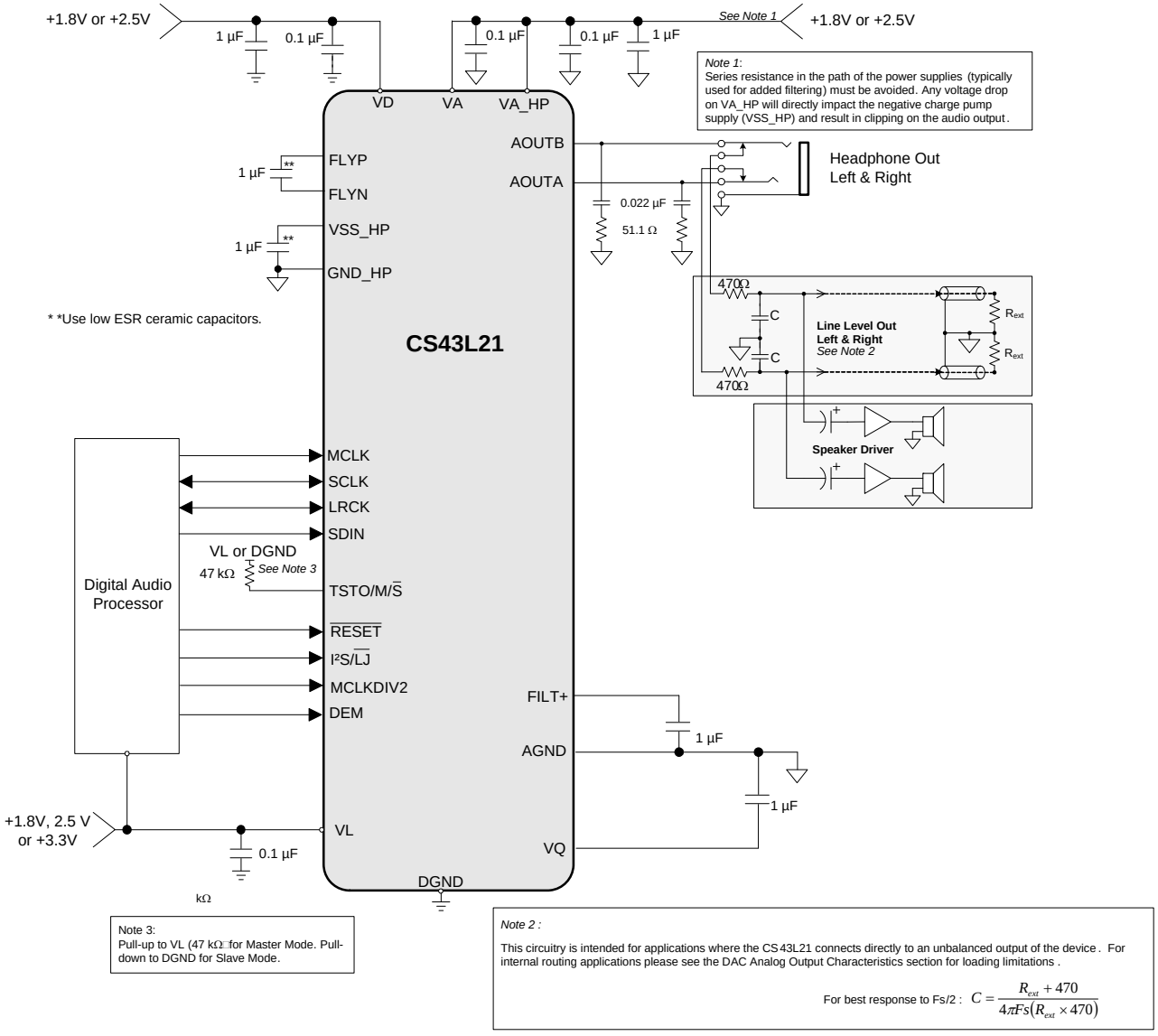


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply (Note 1)				
Analog Core	VA	1.65	2.63	V
Headphone Amplifier	VA_HP	1.65	2.63	V
Digital Core	VD	1.65	2.63	V
Serial/Control Port Interface	VL	1.65	3.47	V
Ambient Temperature Commercial - CNZ Automotive - DNZ	T_A	-10 -40	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog Digital Serial/Control Port Interface	VA, VA_HP VD VL	-0.3 -0.3 -0.3	3.0 3.0 4.0	V V V
Input Current (Note 2)	I_{in}	-	±10	mA
External Voltage Applied to Analog Output	V_{IN}	-VA_HP - 0.3	+VA_HP + 0.3	V
External Voltage Applied to Digital Input (Note 3)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)	T_A	-50	+115	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. The device will operate properly over the full range of the analog, headphone amplifier, digital core and serial/control port interface supplies.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 4)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-78	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 5)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 5)		Refer to Table "Line Output Voltage Characteristics" on page 14						Vpp
Full-scale Output Power (Note 5)		Refer to Table "Headphone Output Power Characteristics" on page 15						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 6)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 6)	-	-	150	-	-	150	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz and 96 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 4)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-73	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 5)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 5)		*Refer to Table* "Line Output Voltage Characteristics" on page 14						Vpp
Full-scale Output Power (Note 5)		*Refer to Table* "Headphone Output Power Characteristics" on page 15						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 6)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 6)	-	-	150	-	-	150	pF

LINE OUTPUT VOLTAGE CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See (Note 7)				2.79		V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 16 Ω, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V		(Note 7)		-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V		(Note 7)		-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V					(Note 5)		mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V							mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

(Note 5, 7)

4. One LSB of triangular PDF dither is added to data.
5. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain (HP_GAIN[2:0])" on page 42. High gain settings at certain VA and VA_HP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in Figures 21 - 24 on page 56.
6. See Figure 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.
7. VA_HP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

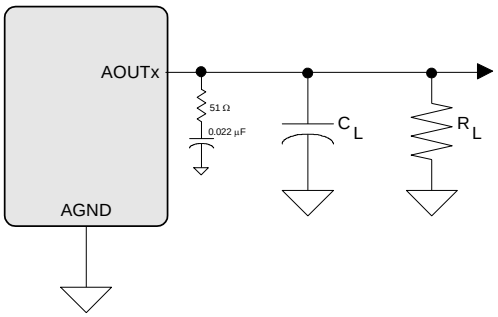


Figure 3. Headphone Output Test Load

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 8)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner to -3 dB corner	0 0	- -	0.4780 0.4996	Fs Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 9)		50	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz	- - -	- - -	+1.5/+0 +0.05/-0.25 -0.2/-0.4	dB dB dB

Notes:

8. Response is clock dependent and will scale with Fs. Note that the response plots (Figure 27 to Figure 30 on page 61) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs.
9. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL.)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 10)			1	-	ms
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle (Note 11)			45	55	%
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode Half-Speed Mode Single-Speed Mode Double-Speed Mode	F_s F_s F_s F_s	4 8 4 50	12.5 25 50 100	kHz kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

Parameters		Symbol	Min	Max	Units
Master Mode (Note 12)					
Output Sample Rate (LRCK)	All Speed Modes (Note 13)	F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDIN MSB Rising Edge		$t_{d(MSB)}$		52	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

10. After powering up the CS43L21, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
11. See "Example System Clock Frequencies" on page 58 for typical MCLK frequencies.
12. See"Master" on page 29.
13. "MCLK" refers to the external master clock applied.

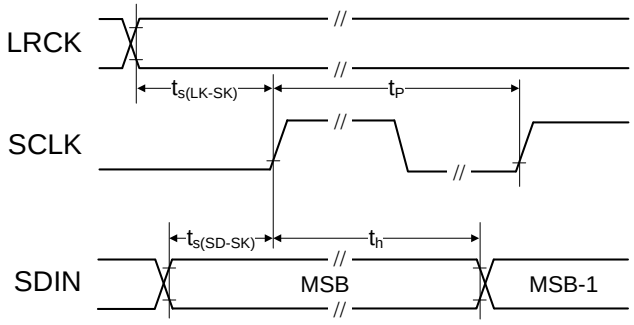


Figure 4. Serial Audio Interface Slave Mode Timing

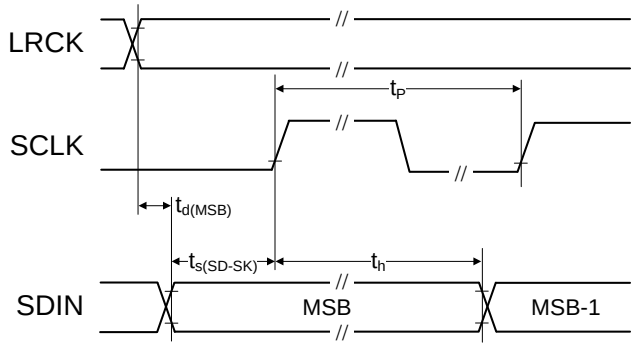


Figure 5. Serial Audio Interface Master Mode Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 14)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

14. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

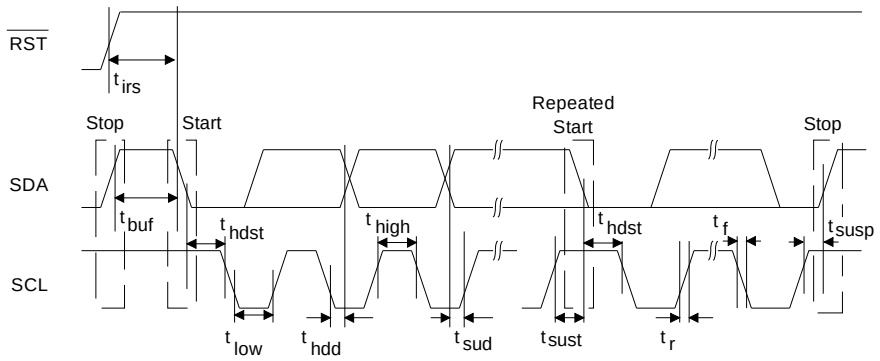


Figure 6. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	20	-	ns
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 15)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 16)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 16)	t_{f2}	-	100	ns

15. Data must be held for sufficient time to bridge the transition time of CCLK.
16. For f_{sck} <1 MHz.

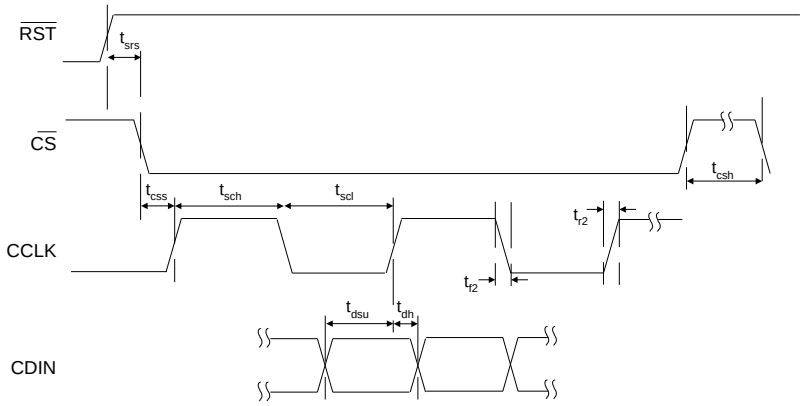


Figure 7. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 17)		-	-	10	µA
FILT+		-	VA	-	V
VSS_HP Characteristics					
Nominal Voltage		-	-0.8•(VA_HP)	-	V
DC Current Source		-		10	µA
Power Supply Rejection Ratio (PSRR) (Note 18)	1 kHz	-	60	-	dB

17. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
18. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 19)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

19. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

POWER CONSUMPTION

See (Note 20)

	Operation	Power Control Registers											Typical Current (mA)				
		02h							03h								
		PDN_DACB	PDN_DACA	BIT 4	BIT 3	BIT 2	BIT 1	PDN	BIT 3	BIT 2	BIT 1	V	i_{VA_HP}	i_{VA}	i_{VD}	i_{VL} (Note 23)	**Total Power (mW_{rms})**
1	Off (Note 21)	x	x	x	x	x	x	x	x	x	x	1.8	0	0	0	0	0
												2.5	0	0	0	0	0
2	Standby (Note 22)	x	x	x	x	x	x	1	x	x	x	1.8	0	0.01	0.02	0	0.05
												2.5	0	0.01	0.03	0	0.10
5	Mono Playback	1	0	1	1	1	1	0	1	1	1	1.8	1.66	1.40	2.35	0.01	9.74
												2.5	2.03	1.71	3.48	0.02	18.08
6	Stereo Playback	0	0	1	1	1	1	0	1	1	1	1.8	2.77	2.05	2.35	0.01	12.93
												2.5	3.21	2.50	3.49	0.02	23.02

20. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
21. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
22. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.
23. VL current will slightly increase in master mode.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS43L21 is a highly integrated, low power, 24-bit audio D/A comprised of stereo digital-to-analog converters (DAC) designed using multi-bit delta-sigma techniques. The DAC operates at an oversampling ratio of 128 Fs. The D/A operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line & Headphone Outputs

The analog output portion of the D/A includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. Eight gain settings for the headphone amplifier are available.

4.1.3 Signal Processing Engine

A signal processing engine is available to process serial input D/A data before output to the DAC. The D/A data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps. A Tone Control provides bass and treble at four selectable corner frequencies. An automatic level control provides limiting capabilities at programmable attack and release rates, maximum thresholds and soft ramping. A 15/50 μs de-emphasis filter is also available at a 44.1 kHz sample rate.

4.1.4 Beep Generator

A beep may be generated internally at select frequencies across approximately two octave major scales and configured to occur continuously, periodically or at single time intervals controlled by the user. Volume may be controlled independently.

4.1.5 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.6 Power Management

Two Software Mode control registers provide independent power-down control of the DAC, allowing operation in select applications with minimal power consumption.

4.2 Hardware Mode

A limited feature-set is available when the D/A powers up in Hardware Mode (see "Recommended Power-Up Sequence" section on page 31) and may be controlled via stand-alone control pins. Table 2 shows a list of functions/features, the default configuration and the associated stand-alone control available.

Hardware Mode Feature/Function Summary				
Feature/Function		**Default Configuration**	**Stand-Alone Control**	**Note**
Power Control	Device DACx	Powered Up Powered Up	-	-
Auto-Detect		Enabled	-	-
Speed Mode	Serial Port Slave Serial Port Master	Auto-Detect Speed Mode Single-Speed Mode	-	-
MCLK Divide		(Selectable)	"MCLKDIV2" pin 2	see Section 4.4 on page 28
Serial Port Master / Slave Selection		(Selectable)	"M/$\overline{S}$" pin 29	see Section 4.4 on page 28
Interface Control	DAC	(Selectable)	"I²S/$\overline{LJ}$" pin 3	see Section 4.5 on page 30
DAC Volume & Gain	HP Gain AOUTx Volume Invert Soft Ramp Zero Cross	G = 0.6047 0 dB Disabled Enabled Disabled	-	-
DAC De-Emphasis		(Selectable)	"DEM" pin 4	see Section on page 24
Signal Processing Engine (SPE)	Mix Beep Tone Control Peak Detect and Limiter	Disabled Disabled Disabled Disabled	-	-
Data Selection		Data Input (PCM) to DAC	-	-
Channel Mix	DAC	PCMA = L; PCMB = R	-	-
Charge Pump Frequency		(64xFs)/7	-	-

Table 2. Hardware Mode Feature Summary

4.3 Analog Outputs

AOUTA and AOUTB are the ground-centered line or headphone outputs. Various signal processing options are available, including an internal Beep Generator. The desired path to the DAC must be selected using the DATA_SEL[1:0] bits.

Software Controls:	"DAC Control (Address 09h)" on page 43.

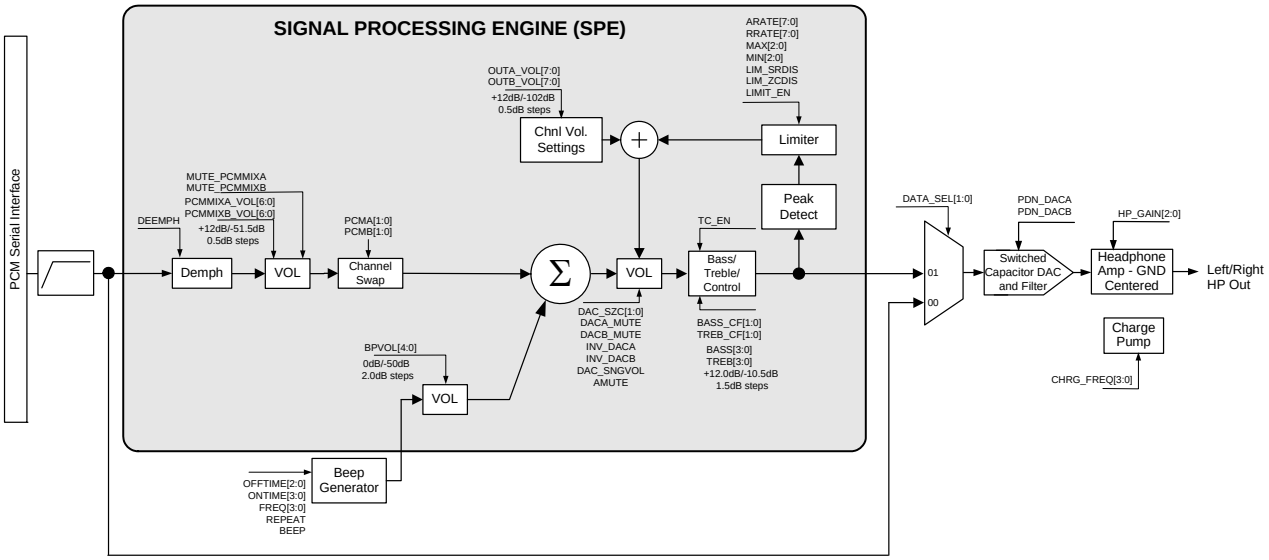


Figure 8. Output Architecture

4.3.1 De-Emphasis Filter

The device includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 9. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction. De-emphasis is only available in Single-Speed Mode.

Software Controls:	"DAC Control (Address 09h)" on page 43.		
Hardware Control:	Pin	Setting	Selection
	"DEM" pin 4.	LO	No De-Emphasis
		HI	De-Emphasis Applied

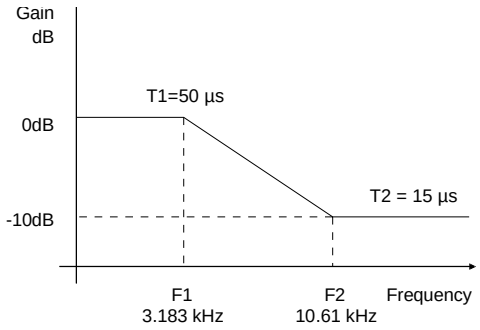


Figure 9. De-Emphasis Curve

4.3.2 Volume Controls

Two digital volume control functions offer independent control of the SDIN signal path into the mixer as well as a combined control of the mixed signals. The volume controls are programmable to ramp in increments of 0.125 dB at a rate controlled by the soft ramp/zero cross settings.

The signal paths may also be muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the DAC_SZC[1:0] bits.

Software Controls:	“PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)” on page 45“AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)” on page 49“DAC Output Control (Address 08h)” on page 42

4.3.3 Mono Channel Mixer

A channel mixer may be used to create a mix of the left and right channels for the SDIN data. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

Software Controls:	“PCM Channel Mixer (Address 18h)” on page 50.

4.3.4 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the Beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, AOUTx_VOL[7:0], will affect the Beep volume, DAC volume may alternatively be controlled using the PCMMIXx_VOL[6:0] bits.

Software Controls:	“Beep Frequency & Timing Configuration (Address 12h)” on page 46, “Beep Off Time & Volume (Address 13h)” on page 46, “Beep Configuration & Tone Configuration (Address 14h)” on page 48

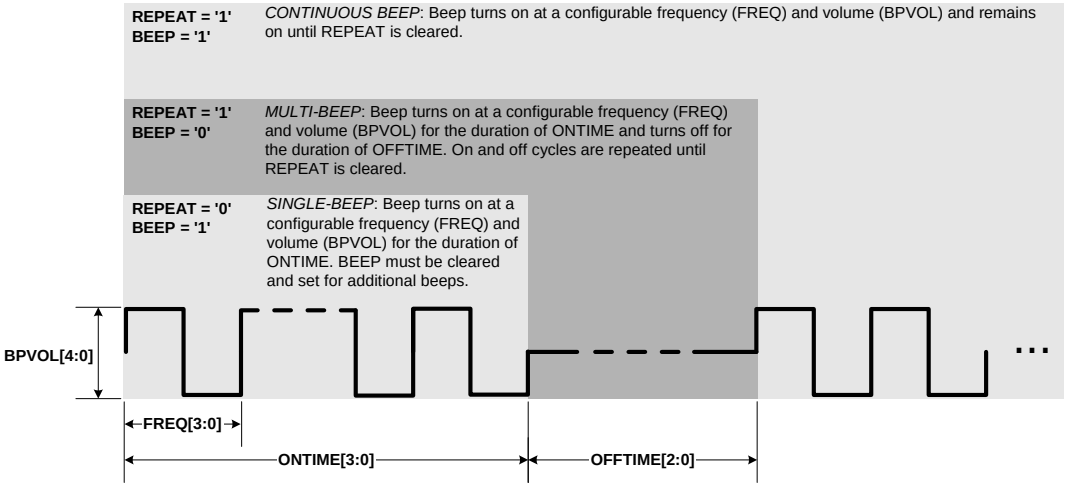


Figure 10. Beep Configuration Options

4.3.5 Tone Control

Shelving filters are used to implement bass and treble (boost and cut) with four selectable corner frequencies. Boosting will affect peak detect and limiting when levels exceed the maximum threshold settings.

Software Controls:	"Tone Control (Address 15h)" on page 49.

4.3.6 Limiter

When enabled, the limiter monitors the digital input signal before the DAC modulator, detects when levels exceed the maximum threshold settings and lowers the AOUT volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp/zero cross settings and sample rate, Fs. Limiter soft ramp and zero cross dependency may be independently enabled/disabled.

Recommended settings: Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The "cushion" bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.

Note:

1. When the Limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.
2. The Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	"Limiter Release Rate Register (Address 1Ah)" on page 52, "Limiter Attack Rate Register (Address 1Bh)" on page 53, "DAC Control (Address 09h)" on page 43

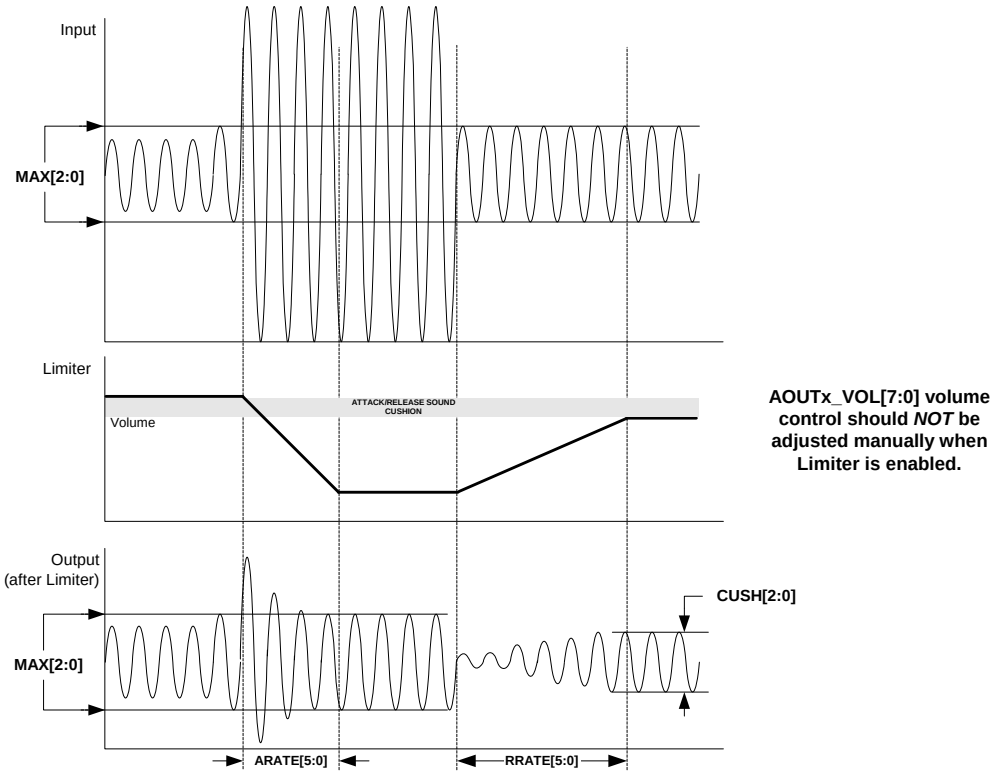


Figure 11. Peak Detect & Limiter

4.3.7 *Line-Level Outputs and Filtering*

The device contains on-chip buffer amplifiers capable of producing line level single-ended outputs on AOUTA and AOUTB. These amplifiers are ground centered and do not have any DC offset. A load stabilizer circuit, shown in the "Typical Connection Diagram (Software Mode)" on page 9 and the "Typical Connection Diagram (Hardware Mode)" on page 10, is required on the analog outputs. This allows the DAC amplifiers to drive line or headphone outputs.

Also shown in the Typical Connection diagrams is the recommended passive output filter to support higher impedances such as those found on the inputs to operational amplifiers. "Rext", shown in the typical connection diagrams, is the input impedance of the receiving device.

The invert and digital gain controls may be used to provide phase and/or amplitude compensation for an external filter.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter.

Software Controls:	"DAC Output Control (Address 08h)" on page 42, "AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)" on page 49.

4.3.8 On-Chip Charge Pump

An on-chip charge pump derives a negative supply voltage from the VA_HP supply. This provides dual rail supplies allowing a full-scale output swing centered around ground and eliminates the need for large, DC-blocking capacitors. Added benefits include greater pop suppression and improved low frequency (bass) response. **Note:** Series resistance in the path of the power supplies must be avoided. Any voltage drop on the VA_HP supply will directly impact the derived negative voltage on the charge pump supply, VSS_HP, and may result in clipping.

The FLYN and FLYP pins connect to internal switches that charges and discharges the external capacitor attached, at a default switching frequency. This frequency may be adjusted in the control port registers. Increasing the charge-pumping capacitor will slightly decease the pumping frequency. The capacitor connected to VSS_HP acts as a charge reservoir for the negative supply as well as a filter for the ripple induced by the charge pump. Increasing this capacitor will decrease the ripple on VSS_HP. Refer to the typical connection diagrams in Figure 1 on page 9 or Figure 2 on page 10 for the recommended capacitor values for the charge pump circuitry.

Software Controls:	"Charge Pump Frequency (Address 21h)" on page 54.

4.4 Serial Port Clocking

The D/A serial audio interface port operates either as a slave or master. It accepts externally generated clocks in slave mode and will generate synchronous clocks derived from an input master clock (MCLK) in master mode.

The frequency of the MCLK must be an integer multiple of, and synchronous with, the system sample rate, Fs. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device.

The SPEED and MCLKDIV2 software control bits or the M/$\overline{S}$ and MCLKDIV2 stand-alone control pins, configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. The value on the M/$\overline{S}$ pin is latched immediately after powering up in Hardware Mode.

Software Control:	, "DAC Control (Address 09h)" on page 43.		
Hardware Control:	**Pin**	**Setting**	**Selection**
	"M/$\overline{S}$" pin 29	47 kΩ Pull-down	Slave
		47 kΩ Pull-up	Master
	"MCLKDIV2" pin 2	LO	No Divide
		HI	MCLK is divided by 2 prior to all internal circuitry.

4.4.1 Slave

LRCK and SCLK are inputs in Slave Mode. The speed of the D/A is automatically determined based on the input MCLK/LRCK ratio when the Auto-Detect function is enabled. Certain input clock ratios will then require an internal divide-by-two of MCLK* using either the MCLKDIV2 bit or the MCLKDIV2 stand-alone control pin.

Additional clock ratios are allowed when the Auto-Detect function is disabled; but the appropriate speed mode must be selected using the SPEED[1:0] bits.

Auto-Detect	QSM	HSM	SSM	DSM
Disabled (Software Mode only)	512, 768, 1024, 1536, 2048, 3072	256, 384, 512, 768, 1024, 1536	128, 192, 256, 384, 512, 768	128, 192, 256, 384
Enabled	1024, 1536, 2048*, 3072*	512, 768, 1024*, 1536*	256, 384, 512*, 768*	128, 192, 256*, 384*

*MCLKDIV2 must be enabled.

Table 3. MCLK/LRCK Ratios

4.4.2 Master

LRCK and SCLK are internally derived from the internal MCLK (after the divide, if MCLKDIV2 is enabled). In Hardware Mode the D/A operates in single-speed only. In Software Mode, the D/A operates in either quarter-, half-, single- or double-speed depending on the setting of the SPEED[1:0] bits.

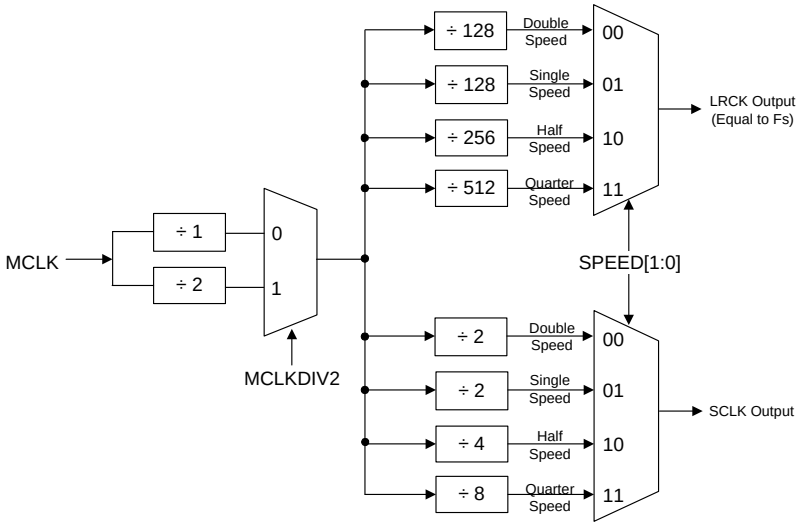


Figure 12. Master Mode Timing

4.4.3 High-Impedance Digital Output

The serial port may be placed on a clock/data bus that allows multiple masters for the SCLK/LRCK I/O without the need for external buffers. The 3ST_SP bit places the internal buffers for these I/O in a high-impedance state, allowing another device to transmit clocks without bus contention.

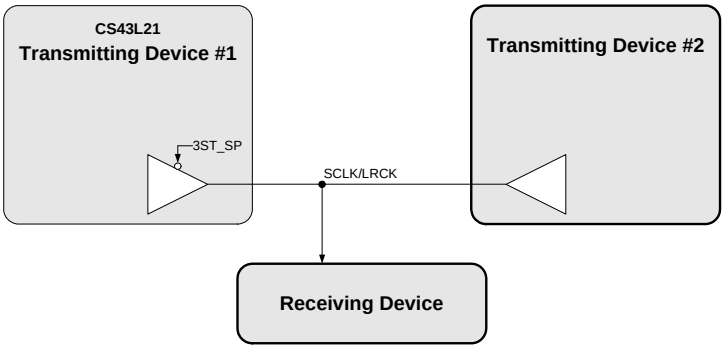


Figure 13. Tri-State SCLK/LRCK

4.4.4 Quarter- and Half-Speed Mode

Quarter-Speed Mode (QSM) and Half-Speed Mode (HSM) allow lower sample rates while maintaining a relatively flat noise floor in the typical audio band of 20 Hz - 20 kHz. Single-Speed Mode (SSM) will allow lower frequency sample rates; however, the DAC's noise floor, that normally rises out-of-band, will scale with the lower sample rate and begin to rise within the audio band. QSM and HSM corrects for most of this scaling, effectively increasing the dynamic range of the device at lower sample rates, relative to SSM.

4.5 Digital Interface Formats

The serial port operates in standard I²S, Left-Justified or Right-Justified digital interface formats with varying bit depths from 16 to 24. Data is clocked into the DAC on the rising edge of SCLK. Figures 14-16 illustrate the general structure of each format. Refer to "Switching Specifications - Serial Port" on page 16 for exact timing relationship between clocks and data.

Software Control:	"Interface Control (Address 04h)" on page 42.		
Hardware Control:	**Pin**	**Setting**	**Selection**
	"I²S/$\overline{LJ}$" pin 3	LO	Left-Justified Interface
		HI	I²S Interface

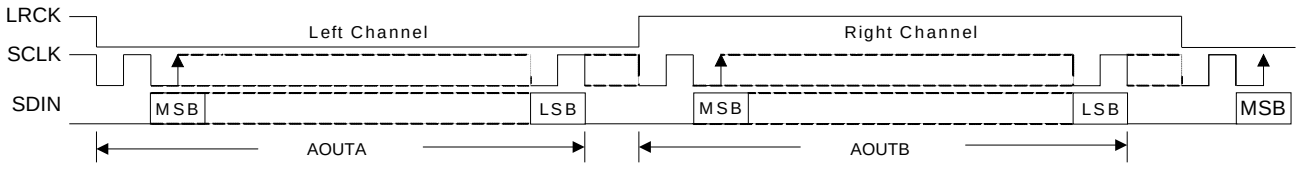


Figure 14. I²S Format

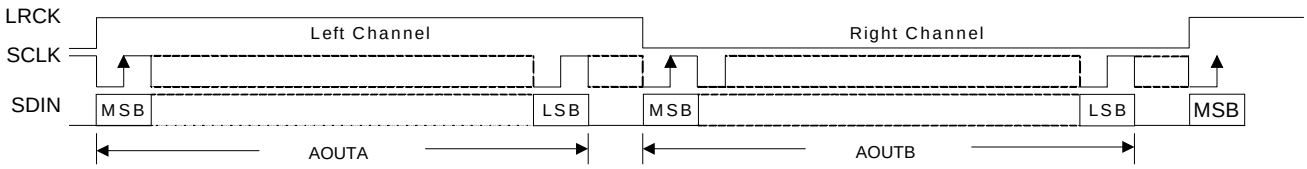


Figure 15. Left-Justified Format

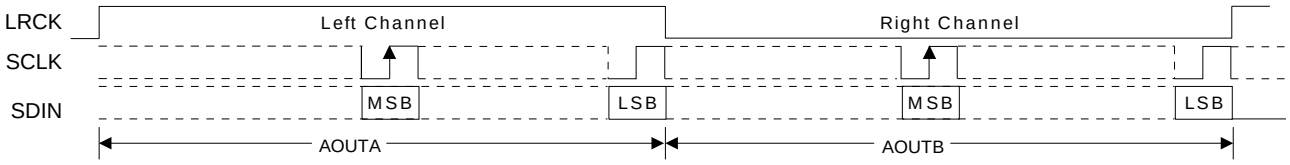


Figure 16. Right-Justified Format (DAC only)

4.6 Initialization

The initialization and Power-Down sequence flowchart is shown in Figure 16 on page 31. The device enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit DAC and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in "Software Mode" on page 34. If a valid write sequence to the control port is not made within approximately 10 ms, the device will enter Hardware Mode.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+ will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

4.7 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable; no specific power supply sequencing is required.
2. Bring $\overline{\text{RESET}}$ high. After approximately 10 ms, the device will enter Hardware Mode.
3. For Software Mode operation, set the PDN bit to '1'b in under 10 ms. This will place the device in "standby".
4. Load the desired register settings while keeping the PDN bit set to '1'b.
5. Start MCLK to the appropriate frequency, as discussed in Section 4.4. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the PDN bit to '0'b.
7. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.8 Recommended Power-Down Sequence

To minimize audible pops when turning off or placing the device in standby,

1. Mute the DACs.
2. Disable soft ramp and zero cross volume transitions.
3. Set the PDN bit to 1.
4. Wait at least 100 µs.
   The DAC will be fully powered down after this 100 µs delay. Prior to the removal of the master clock (MCLK), this delay of at least 100 µs must be implemented after step 3 to avoid premature disruption of the device's power down sequence.

   A disruption in the DAC's power down sequence (i.e. removing the MCLK signal before this 100 µs delay) has consequences on the headphone amplifier: The charge pump may stop abruptly, causing the headphone amplifiers to drive the outputs up to the +VA_HP supply.

   The disruption of the DAC's power down sequence may also cause clicks and pops on the output of the DAC's as the modulator holds the last output level before the MCLK signal was removed.
5. Optionally, MCLK may be removed at this time.
6. To achieve the lowest operating quiescent current, bring $\overline{\text{RESET}}$ low. All control port registers will be reset to their default state.
7. Power Supply Removal (Option 1): Switch power supplies to a high impedance state.
8. Power Supply Removal (Option 2): To minimize pops when the power supplies are pulled to ground, a discharge resistor must be added in parallel with the capacitor on the FILT+ pin. With a 1 MΩ resistor and a 2.2 µF capacitor on FILT+, FILT+ will ramp to ground in approximately 5 seconds. A 1 MΩ resistor on FILT+ reduces the full scale input/output voltage by approximately 0.25 dB.

   After step 5, wait the required time for FILT+ to ramp to ground before pulling VA to ground.

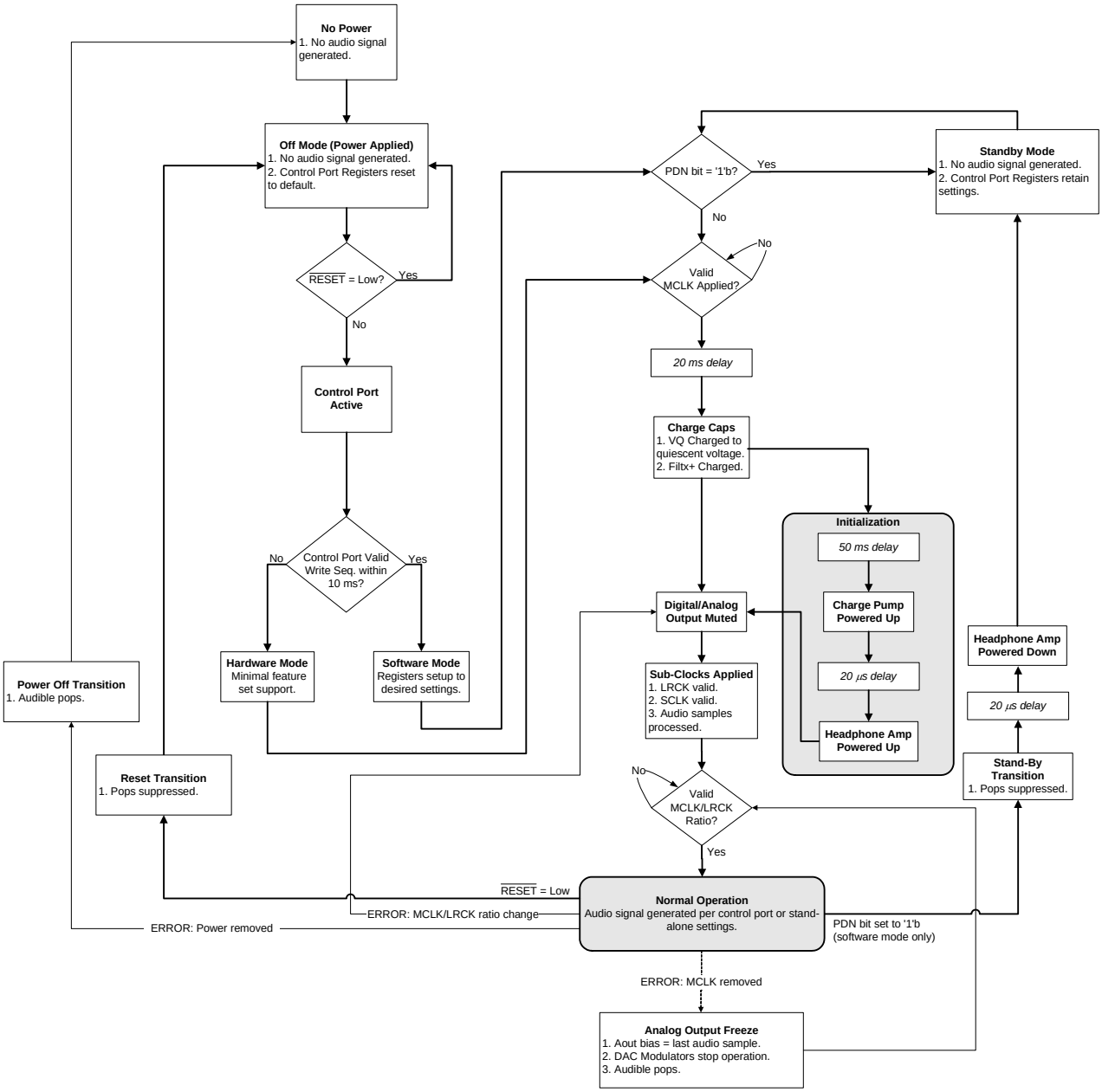


Figure 17. Initialization Flow Chart

4.9 Software Mode

The control port is used to access the registers allowing the D/A to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The device enters software mode only after a successful write command using one of two software protocols: SPI or I²C, with the device acting as a slave. The SPI protocol is permanently selected whenever there is a high-to-low transition on the AD0/CS pin after reset. If using the I²C protocol, pin AD0/CS should be permanently connected to either VL or GND; this option allows the user to slightly alter the chip address as desired.

4.9.1 SPI Control

In Software Mode, $\overline{CS}$ is the CS43L21 chip-select signal, CCLK is the control port bit clock (input into the from the microcontroller), CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The D/A will only support write operations. Read request will be ignored.

Figure 18 shows the operation of the control port in Software Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001010. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

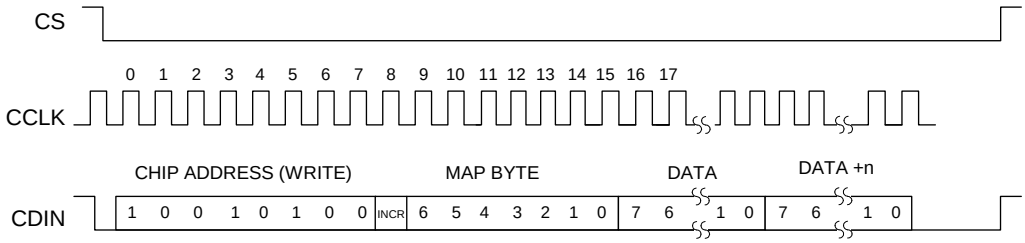


Figure 18. Control Port Timing in SPI Mode

4.9.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or DGND as desired. The state of the pin is sensed while the CS43L21 is being reset.

The signal timings for a read and write cycle are shown in Figure 19 and Figure 20. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS43L21 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100101. To communicate with a CS43L21, the chip address field, which is the first byte sent to the CS43L21, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the

operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS43L21 after each input byte is read and is input to the CS43L21 from the microcontroller after each transmitted byte.

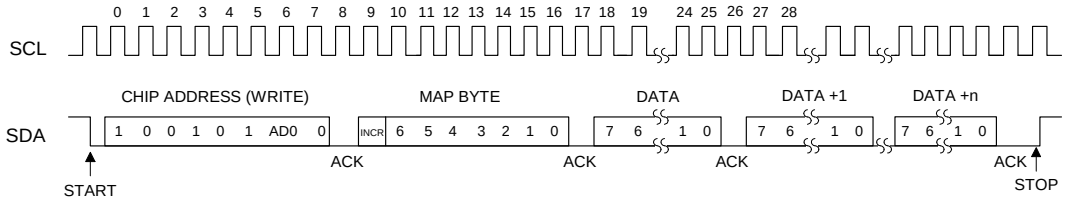


Figure 19. Control Port Timing, I²C Write

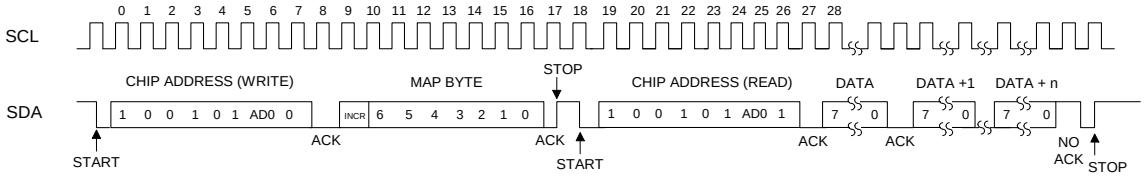


Figure 20. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 20, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100101x0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto-increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100101x1 (chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.9.3 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.9.3.1 Map Increment (INCR)

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

5. REGISTER QUICK REFERENCE

Software mode register defaults are as shown. “Reserved” registers must maintain their default state.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	Chip_ID4	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID2	Rev_ID1	Rev_ID0
	p 40 default	1	1	0	1	1	0	0	1
02h	Power Ctl. 1	Reserved	PDN_DACB	PDN_DACA	Reserve	Reserved	Reserved	Reserved	PDN
	p 40 default	0	0	0	1(See Note 2 on page 40)	1(See Note 2 on page 40)	1(See Note 2 on page 40)	1(See Note 2 on page 40)	0
03h	Speed Ctl. & Power Ctl. 2	AUTO	SPEED1	SPEED0	3-ST_SP	Reserved	Reserved	Reserved	MCLKDIV2
	p 41 default	1	0	1	0	1	1	1	0
04h	Interface Ctl.	Reserved	M/$\overline{S}$	DAC_DIF2	DAC_DIF1	DAC_DIF0	Reserved	Reserved	Reserved
	p 42 default	0	0	0	0	0	0	0	0
05h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
06h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	1	0	1	0	0	0	0	0
07h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
08h	DAC Output Control	HP_GAIN2	HP_GAIN1	HP_GAIN0	DAC_SNG VOL	INV_PCMB	INV_PCMA	DACB_ MUTE	DACA_ MUTE
	p 42 default	0	1	1	0	0	0	0	0
09h	DAC Control	DATA_SEL1	DATA_SEL0	FREEZE	Reserved	DEEMPH	AMUTE	DAC_SZC1	DAC_SZC0
	p 43 default	0	0	0	0	0	1	1	0
0Ah	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
0Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
0Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
0Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
0Eh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	0
0Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
10h	Vol. Control PCMMIXA	MUTE_PCM MIXA	PCMMIXA VOL6	PCMMIXA VOL5	PCMMIXA VOL4	PCMMIXA VOL3	PCMMIXA VOL2	PCMMIXA VOL1	PCMMIXA VOL0
	p 45 default	1	0	0	0	0	0	0	0
11h	Vol. Control PCMMIXB	MUTE_PCM MIXB	PCMMIXB VOL6	PCMMIXB VOL5	PCMMIXB VOL4	PCMMIXB VOL3	PCMMIXB VOL2	PCMMIXB VOL1	PCMMIXB VOL0
	p 45 default	1	0	0	0	0	0	0	0
12h	BEEP Freq. & OnTime	FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0
	p 46 default	0	0	0	0	0	0	0	0
13h	BEEP Off Time & Vol	OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0
	p 46 default	0	0	0	0	0	0	0	0
14h	BEEP Con-trol & Tone Config	REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN
	p 48 default	0	0	0	0	0	0	0	0
15h	Tone Control	TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0
	p 49 default	1	0	0	0	1	0	0	0
16h	Vol. Control AOUTA	AOUTA_ VOL7	AOUTA_ VOL6	AOUTA_ VOL5	OUTA_ VOL4	AOUTA_ VOL3	AOUTA_ VOL2	AOUTA_ VOL1	AOUTA_ VOL0
	p 49 default	0	0	0	0	0	0	0	0
17h	Vol. Control AOUTB	AOUTB_ VOL7	AOUTB_ VOL6	AOUTB_ VOL5	AOUTB_ VOL4	AOUTB_ VOL3	AOUTB_ VOL2	AOUTB_ VOL1	AOUTB_ VOL0
	p 49 default	0	0	0	0	0	0	0	0
18h	PCM Channel Mixer	PCMA1	PCMA0	PCMB1	PCMB0	Reserved	Reserved	Reserved	Reserved
	p 50 default	0	0	0	0	0	0	0	0
19h	Limiter Threshold & SZC Disable	MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS
	p 51 default	0	0	0	0	0	0	0	0
1Ah	Limiter Con-fig & Release Rate	LIMIT_EN	LIMIT_ALL	LIM_R-RATE5	LIM_R-RATE4	LIM_R-RATE3	LIM_R-RATE2	LIM_R-RATE1	LIM_R-RATE0
	p 52 default	0	1	1	1	1	1	1	1
1Bh	Limiter Attack Rate	Reserved	Reserved	LIM_ARATE5	LIM_ARATE4	LIM_ARATE3	LIM_ARATE2	LIM_ARATE1	LIM_ARATE0
	p 53 default	0	0	0	0	0	0	0	0
1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
1Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	1	1	1	1	1	1
1Eh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
20h	Status	Reserved	SP_CLK ERR	SPEB_OVFL	SPEA_OVFL	PCMA_OVFL	PCMB_OVFL	Reserved	Reserved
	p 53 default	0	0	0	0	0	0	0	0
21h		CHRG_ FREQ3	CHRG_ FREQ2	CHRG_ FREQ1	CHRG_ FREQ0	Reserved	Reserved	Reserved	Reserved
	p 54 default	0	1	0	1	0	0	0	0

6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.
All “Reserved” registers must maintain their default state.

6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID4	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID2	Rev_ID1	Rev_ID0

Chip I.D. (Chip_ID[4:0])

Default: 11011

Function:

I.D. code for the CS43L21. Permanently set to 11011.

Chip Revision (Rev_ID[2:0])

Default: 001

Function:

CS43L21 revision level. Revision B is coded as 001. Revision A is coded as 000.

6.2 Power Control 1 (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_DACB	PDN_DACA	Reserved	Reserved	Reserved	Reserved	PDN

Notes:

1. To activate the power-down sequence for individual channels (A or B,) *both* channels must first be powered down either by enabling the PDN bit or by enabling the power-down bits for both channels. Enabling the power-down bit on an individual channel basis after the D/A has fully powered up will mute the selected channel without achieving any power savings.
2. Reserved bits 1 - 4 should always be set “high” by the user to minimize power consumption during normal operation.

Recommended channel power-down sequence: 1.) Enable the PDN bit, 2.) enable power-down for the select channels, 3.) disable the PDN bit.

Power Down DAC X (PDN_DACX)

Default: 0

0 - Disable
1 - Enable

Function:

DAC channel x will either enter a power-down or muted state when this bit is enabled. See above.

Power Down (PDN)

Default: 0

0 - Disable
1 - Enable

Function:

The entire D/A will enter a low-power state when this function is enabled. The contents of the control port registers are retained in this mode.

6.3 Speed Control (Address 03h)

7	6	5	4	3	2	1	0
AUTO	SPEED1	SPEED0	3-ST_SP	Reserved	Reserved	Reserved	MCLKDIV2

Auto-Detect Speed Mode (AUTO)

Default: 1

0 - Disable
1 - Enable

Function:

Enables the auto-detect circuitry for detecting the speed mode of the D/A when operating as a slave. When AUTO is enabled, the MCLK/LRCK ratio must be implemented according to Table 3 on page 29. The SPEED[1:0] bits are ignored when this bit is enabled. Speed is determined by the MCLK/LRCK ratio.

Speed Mode (SPEED[1:0])

Default: 01

11 - Quarter-Speed Mode (QSM) - 4 to 12.5 kHz sample rates
10 - Half-Speed Mode (HSM) - 12.5 to 25 kHz sample rates
01 - Single-Speed Mode (SSM) - 4 to 50 kHz sample rates
00 - Double-Speed Mode (DSM) - 50 to 100 kHz sample rates

Function:

Sets the appropriate speed mode for the D/A in Master or Slave Mode. QSM is optimized for 8 kHz sample rate and HSM is optimized for 16 kHz sample rate. These bits are ignored when the AUTO bit is enabled (see Auto-Detect Speed Mode (AUTO) above).

Tri-State Serial Port Interface (3ST_SP)

Default: 0

0 - Disable
1 - Enable

Function:

When enabled and the device is configured as a master, the SCLK/LRCK signals are placed in a high-impedance output state. If the serial port is configured as a slave, SCLK/LRCK are configured as inputs.

MCLK Divide By 2 (MCLKDIV2)

Default: 0

0 - Disabled
1 - Divide by 2

Function:

Divides the input MCLK by 2 prior to all internal circuitry. This bit is ignored when the AUTO bit is disabled in Slave Mode.

6.4 Interface Control (Address 04h)

7	6	5	4	3	2	1	0
Reserved	M/S	DAC_DIF2	DAC_DIF1	DAC_DIF0	Reserved	Reserved	Reserved

Master/Slave Mode (M/S)

Default: 0

0 - Slave
1 - Master

Function:

Selects either master or slave operation for the serial port.

DAC Digital Interface Format (DAC_DIF[2:0])

Default = 000

DAC_DIF[2:0]	Description	Figure
000	Left-Justified, up to 24-bit data	15 on page 31
001	I²S, up to 24-bit data	14 on page 30
010	Right-Justified, 24-bit data	16 on page 3116 on page 31
011	Right-Justified, 20-bit data	16 on page 3116 on page 31
100	Right-Justified, 18-bit data	16 on page 3116 on page 31
101	Right-Justified, 16-bit data	16 on page 3116 on page 31
110	Reserved	-
100	Reserved	-

Function:

Selects the digital interface format used for the data in on SDIN. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the section "Digital Interface Formats" on page 30.

6.5 DAC Output Control (Address 08h)

7	6	5	4	3	2	1	0
HP_GAIN2	HP_GAIN1	HP_GAIN0	DAC_ SNGVOL	INV_PCMB	INV_PCMA	DACB_MUTE	DACA_MUTE

Headphone Analog Gain (HP_GAIN[2:0])

Default: 011

HP_GAIN[2:0]	Gain Setting
000	0.3959
001	0.4571
010	0.5111
011	0.6047
100	0.7099
101	0.8399
110	1.0000
111	1.1430

Function:

These bits select the gain multiplier for the headphone/line outputs. See "Line Output Voltage Characteristics" on page 14 and "Headphone Output Power Characteristics" on page 15.

DAC Single Volume Control (DAC_SNGVOL)

Default: 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUTA Volume Control register and the AOUTB Volume Control register is ignored.

PCMX Invert Signal Polarity (INV_PCMX)

Default: 0

0 - Disabled
1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the PCM x channel.

DACX Channel Mute (DACX_MUTE)

Default: 0

0 - Disabled
1 - Enabled

Function:

The output of channel x DAC will mute when enabled. The muting function is affected by the DACx Soft and Zero Cross bits (DACx_SZC[1:0]).

6.6 DAC Control (Address 09h)

7	6	5	4	3	2	1	0
DATA_SEL1	DATA_SEL0	FREEZE	Reserved	DEEMPH	AMUTE	DAC_SZC1	DAC_SZC0

DAC Data Selection (DATA_SEL[1:0])

Default: 00

00 - PCM Serial Port to DAC
01 - Signal Processing Engine to DAC
10 - Reserved
11 - Reserved

Function:

Selects the digital signal source for the DAC.

Note: Certain functions are only available when the "Signal Processing Engine to DAC" option is selected using these bits.

Freeze Controls (FREEZE)

Default: 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to all control port registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

Notes:

1. This bit should only be used to synchronize run-time controls, such as volume and mute, during normal operation. Using this bit before the relevant circuitry begins normal operation could cause the change to take effect immediately, ignoring the FREEZE bit.

DAC De-Emphasis Control (DEEMPH)

Default: 0

0 - No De-Emphasis
1 - De-Emphasis Enabled

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control.

Enables the digital filter to apply the standard 15μs/50μs digital de-emphasis filter response for a sample rate of 44.1 kHz.

Analog Output Auto MUTE (AMUTE)

Default: 0

0 - Auto Mute Disabled
1 - Auto Mute Enabled

Function:

Enables (or disables) Automatic Mute of the analog outputs after 8192 "0" samples on each digital input channel.

DAC Soft Ramp and Zero Cross Control (DAC_SZC[1:0])

Default = 10

00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control

Immediate Change

When Immediate Change is selected all volume-level changes will take effect immediately in one step.

Zero Cross

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 0.5 dB per 4 left/right clock periods.

Soft Ramp on Zero Crossing

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

6.7 PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)

7	6	5	4	3	2	1	0
MUTE_ PCMMIXx	PCMMIXx_ VOL6	PCMMIXx_ VOL5	PCMMIXx_ VOL4	PCMMIXx_ VOL3	PCMMIXx_ VOL2	PCMMIXx_ VOL1	PCMMIXx_ VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

PCMX Mixer Channel Mute (MUTE_PCMMIXX)

Default = 1

0 - Disabled
1 - Enabled

Function:

The PCM channel X input to the output mixer will mute when enabled. The muting function is affected by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]).

PCMX Mixer Volume Control (PCMMIXX_VOL[6:0])

Default: 000 0000

Binary Code	Volume Setting
001 1000	+12.0 dB
…	…
000 0000	0 dB
111 1111	-0.5 dB
111 1110	-1.0 dB
…	…
001 1001	-51.5 dB

Function:

The level of the PCMX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as described in the table above.

6.8 Beep Frequency & Timing Configuration (Address 12h)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Beep Frequency (FREQ[3:0])

Default: 0000

FREQ[3:0]	Frequency Fs = 12, 24, 48 or 96 kHz	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7

Function:

The frequency of the beep signal can be adjusted from 260.87 Hz to 2181.82 Hz. Beep frequency will scale directly with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 10 on page 26 for single, multiple and continuous beep configurations using the REPEAT and BEEP bits.

Beep On Time Duration (ONTIME[3:0])

Default: 0000

TIME[3:0]	On Time Fs = 12, 24, 48 or 96 kHz
0000	86 ms
…	…
1111	5.2 s

Function:

The on-duration of the beep signal can be adjusted from approximately 86 ms to 5.2 s. The on-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 10 on page 26 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

6.9 Beep Off Time & Volume (Address 13h)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Beep Off Time (OFFTIME[2:0])

Default: 000

OFFTIME[2:0]	Off Time Fs = 12, 24, 48 or 96 kHz
000	1.23 s
001	2.58 s
010	3.90 s
011	5.20 s
100	6.60 s
101	8.05 s
110	9.35 s
111	10.80 s

Function:

The off-duration of the beep signal can be adjusted from approximately 75 ms to 680 ms. The off-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 10 on page 26 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

Beep Volume (BPVOL[4:0])

Default: 00000

Binary Code	Volume Setting
00110	+12.0 dB
…	…
00000	0 dB
11111	-2 dB
11110	-4 dB
…	…
00111	-50 dB

Function:

The level of the beep into the output mixer can be adjusted in 2.0 dB increments from +12 dB to -50 dB. Refer to Figure 10 on page 26 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits. Levels are decoded as described in the table above.

6.10 Beep Configuration & Tone Configuration (Address 14h)

7	6	5	4	3	2	1	0
REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Repeat Beep (REPEAT)

Default: 0

0 - Disabled
1 - Enabled

Function:

This bit is used in conjunction with the BEEP bit to mix a continuous or periodic beep with the analog output. Refer to Figure 10 on page 26 for a description of each configuration option.

Beep (BEEP)

Default: 0

0 - Disabled
1 - Enabled

Function:

This bit is used in conjunction with the REPEAT bit to mix a continuous or periodic beep with the analog output. **Note:** Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration. Refer to Figure 10 on page 26 for a description of each configuration option.

Treble Corner Frequency (TREB_CF[1:0])

Default: 00

00 - 5 kHz
01 - 7 kHz
10 - 10 kHz
11 - 15 kHz

Function:

The treble corner frequency is user selectable as shown above.

Bass Corner Frequency (BASS_CF[1:0])

Default: 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - 250 Hz

Function:

The bass corner frequency is user-selectable as shown above.

Tone Control Enable (TC_EN)

Default = 0

0 - Disabled
1 - Enabled

Function:

The Bass and Treble tone control features are active when this bit is enabled.

6.11 Tone Control (Address 15h)

7	6	5	4	3	2	1	0
TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Treble Gain Level (TREB[3:0])

Default: 1000 dB (No Treble Gain)

Binary Code	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB

Function:

The level of the shelving treble gain filter is set by Treble Gain Level. The level can be adjusted in 1.5 dB increments from +12.0 to -10.5 dB.

Bass Gain Level (BASS[3:0])

Default: 1000 dB (No Bass Gain)

Binary Code	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB

Function:

The level of the shelving bass gain filter is set by Bass Gain Level. The level can be adjusted in 1.5 dB increments from +10.5 to -10.5 dB.

6.12 AOUTx Volume Control:

AOUTA (Address 16h) & AOUTB (Address 17h)

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

AOUTX Volume Control (AOUTX_VOL[7:0])

Default = 00h

Binary Code	Volume Setting
0001 1000	+12.0 dB
…	…
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
…	…
0011 0100	-102 dB
…	…
0001 1001	-102 dB

Function:

The analog output levels can be adjusted in 0.5 dB increments from +12 to -102 dB as dictated by the DAC Soft and Zero Cross bits (DACX_SZC[1:0]). Levels are decoded in unsigned binary as described in the table above.

Note: When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be achieved using the PCMMIXx_VOL[6:0] bits.

6.13 PCM Channel Mixer (Address 18h)

7	6	5	4	3	2	1	0
PCMA1	PCMA0	PCMB1	PCMB0	Reserved	Reserved	Reserved	Reserved

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Channel Mixer (PCMx[1:0])

Default: 00

PCMA[1:0]	AOUTA	PCMB[1:0]	AOUTB
00	L	00	R
01	$\frac{L+R}{2}$	01	$\frac{L+R}{2}$
10		10	
11	R	11	L

Function:

Implements mono mixes of the left and right channels as well as a left/right channel swap.

6.14 Limiter Threshold SZC Disable (Address 19h)

7	6	5	4	3	2	1	0
MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Maximum Threshold (MAX[2:0])

Default: 000

MAX[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate. Bass, Treble and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

Cushion Threshold (CUSH[2:0])

Default: 000

CUSH[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets a cushion level below full scale. This setting is usually set slightly below the maximum (MAX[2:0]) threshold. The Limiter uses this cushion as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the cushion setting. This provides a more natural sound as the limiter attacks and releases.

Limiter Soft Ramp Disable (LIM_SRDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the soft ramp setting. **Note:** This bit is ignored when the zero-cross function is enabled (i.e. when DAC_SZC[1:0] = '01'b or '11'b.)

Limiter Zero Cross Disable (LIM_ZCDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the zero-cross setting.

6.15 Limiter Release Rate Register (Address 1Ah)

7	6	5	4	3	2	1	0
LIMIT_EN	LIMIT_ALL	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Peak Detect and Limiter Enable (LIMIT_EN)

Default: 0

0 - Disabled
1 - Enabled

Function:

Limits the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by digital attenuation. **Note:** When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.

Peak Signal Limit All Channels (LIMIT_ALL)

Default: 1

0 - Individual Channel
1 - Both channels A & B

Function:

When set to 0, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on the specific channel indicating clipping. The other channels will not be affected.

When set to 1, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on both channels in response to any single channel indicating clipping.

Limiter RELEASE Rate (RRATE[5:0])

Default: 111111

Binary Code	Release Time
000000	Fastest Release
…	…
111111	Slowest Release

Function:

Sets the rate at which the limiter releases the digital attenuation from levels below the minimum setting in the limiter threshold register, and returns the analog output level to the AOUTx_VOL[7:0] setting.

The limiter release rate is user selectable but is also a function of the sampling frequency, Fs, and the DAC_SZC setting unless the disable bit is enabled.

6.16 Limiter Attack Rate Register (Address 1Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Limiter Attack Rate (ARATE[5:0])

Default: 000000

Binary Code	Attack Time
000000	Fastest Attack
…	…
111111	Slowest Attack

Function:

Sets the rate at which the limiter attenuates the analog output from levels above the maximum setting in the limiter threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, Fs, and the DAC_SZC setting unless the disable bit is enabled.

6.17 Status (Address 20h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	SP_CLKERR	SPEA_OVFL	SPEB_OVFL	PCMA_OVFL	PCMB_OVFL	Reserved	Reserved

For all bits in this register, a “1” means the associated error condition has occurred at least once since the register was last read. A ”0” means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

Serial Port Clock Error (SP_CLK Error)

Default: 0

Function:

Indicates an invalid MCLK to LRCK ratio. See “Serial Port Clocking” section on page 28“Serial Port Clocking” on page 28 for valid clock ratios.

Note: On initial power up and application of clocks, this bit will be high as the serial port re-synchronizes.

Signal Processing Engine Overflow (SPEX_OVFL)

Default: 0

Function:
Indicates a digital overflow condition within the data path after the signal processing engine.

PCMX Overflow (PCMX_OVFL)

Default: 0

Function:

Indicates a digital overflow condition within the data path of the PCM mix.

6.18 Charge Pump Frequency (Address 21h)

7	6	5	4	3	2	1	0
CHRG_-FREQ3	CHRG_-FREQ2	CHRG_-FREQ1	CHRG_-FREQ0	Reserved	Reserved	Reserved	Reserved

Charge Pump Frequency (CHRG_FREQ[3:0])

Default: 0101

N	CHRG_FREQ[3:0]	Frequency
0	0000	$\frac{64xFs}{N+2}$
...	...	
15	1111	

Function:

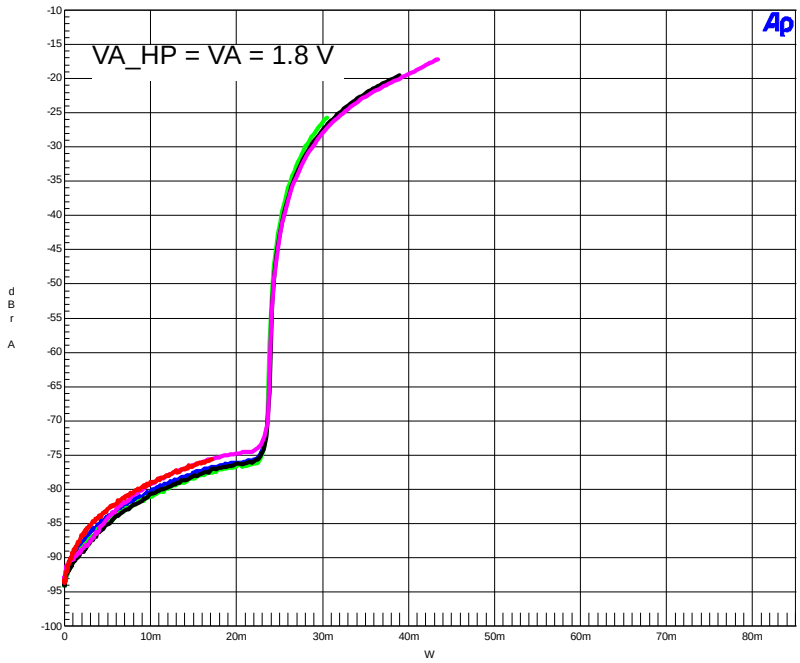
Alters the clocking frequency of the charge pump in 1/(N+2) fractions of the DAC oversampling rate, 128 Fs, should the switching frequency interfere with other system frequencies such as those in the AM radio band.

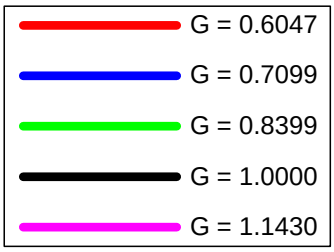
Note: Distortion performance may be affected.

7. ANALOG PERFORMANCE PLOTS

7.1 Headphone THD+N versus Output Power Plots

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48 kHz. Plots were taken from the CDB43L21 using an Audio Precision analyzer.

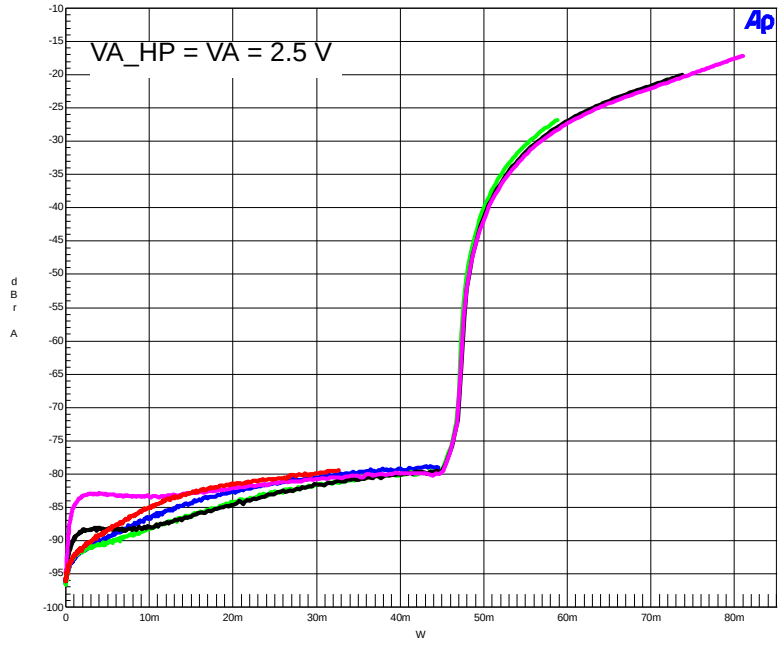


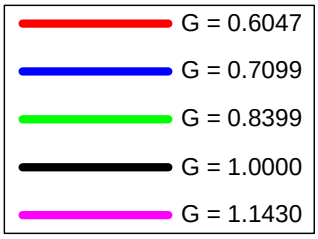


Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 23 mW into single 16 Ω and 46 mW into stereo 16 Ω with THD+N = -75 dB).

Figure 21. THD+N vs. Output Power per Channel at 1.8 V (16 Ω load)

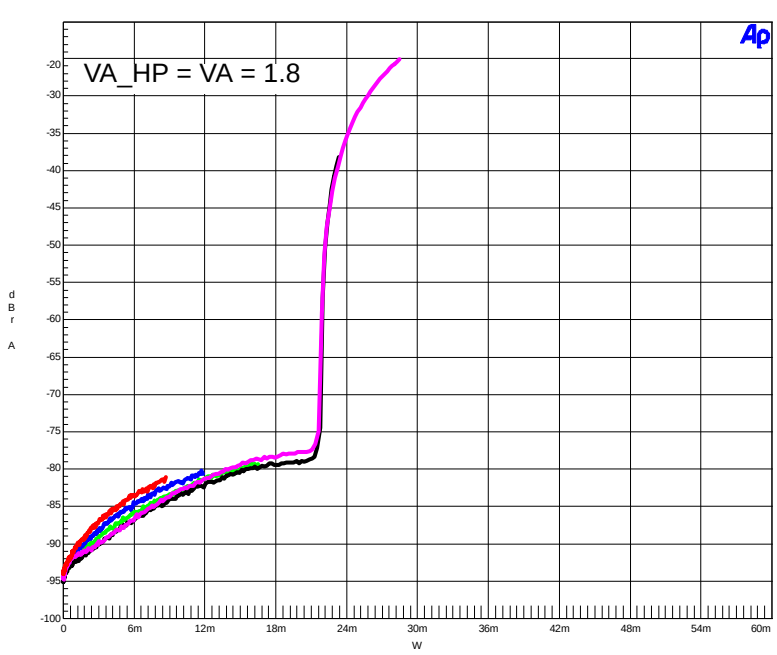


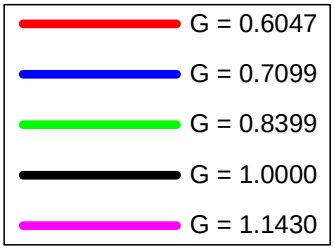


Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 44 mW into single 16 Ω and 88 mW into stereo 16 Ω with THD+N = -75 dB).

Figure 22. THD+N vs. Output Power per Channel at 2.5 V (16 Ω load)

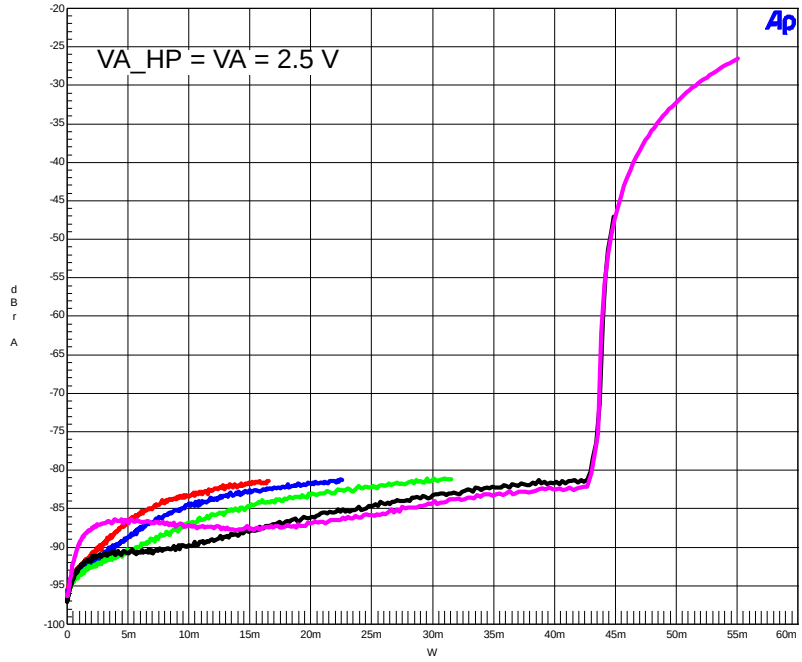


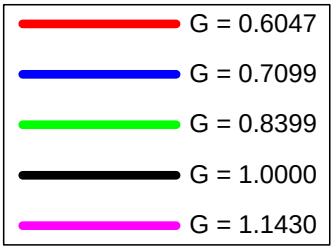


Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 22 mW into single 32 Ω and 44 mW into stereo 32 Ω with THD+N = -75 dB).

Figure 23. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)





Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 42 mW into single 32 Ω and 84 mW into stereo 32 Ω with THD+N = -75 dB).

Figure 24. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)

7.2 Headphone Amplifier Efficiency

The architecture of the headphone amplifier is that of typical class AB amplifiers. Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; Power Consumption Mode 6 - Stereo Playback with 16-Ω load. HP_GAIN = 1.1430. Best efficiency is realized when the amplifier outputs maximum power.

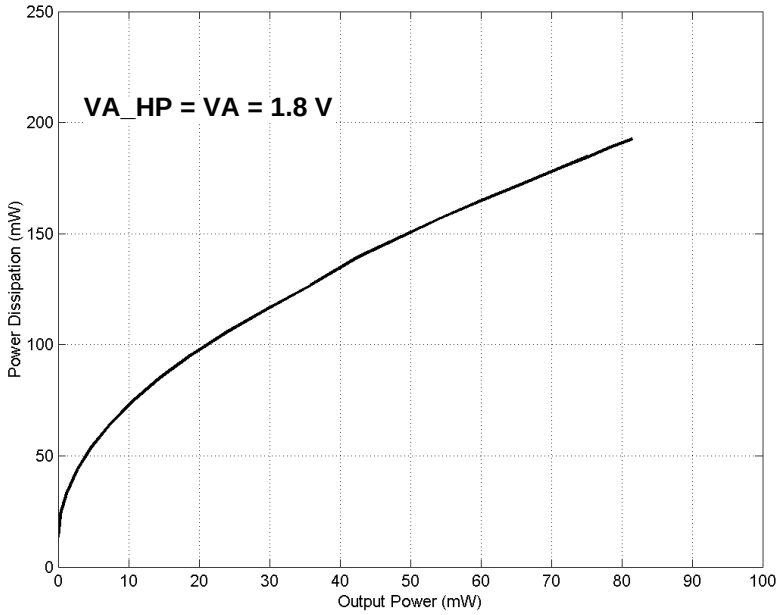


Figure 25. Power Dissipation vs. Output Power into Stereo 16 Ω

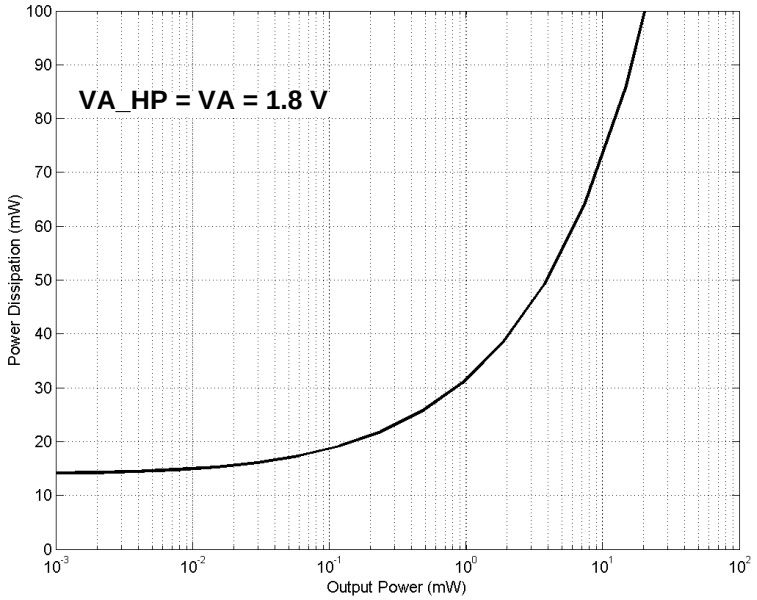


Figure 26. Power Dissipation vs. Output Power into Stereo 16 Ω (Log Detail)

8. EXAMPLE SYSTEM CLOCK FREQUENCIES

8.1 Auto Detect Enabled

Sample Rate LRCK (kHz)	MCLK (MHz)			
	1024x	1536x	2048x*	3072x*
8	8.1920	12.2880	16.3840	24.5760
11.025	11.2896	16.9344	22.5792	33.8688
12	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	512x	768x	1024x*	1536x*
16	8.1920	12.2880	16.3840	24.5760
22.05	11.2896	16.9344	22.5792	33.8688
24	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x*	768x*
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

*The”MCLKDIV2” pin 4 must be set HI.

8.2 Auto Detect Disabled

Sample Rate LRCK (kHz)	MCLK (MHz)					
	512x	768x	1024x	1536x	2048x	3072x
8	-	6.1440	8.1920	12.2880	16.3840	24.5760
11.025	-	8.4672	11.2896	16.9344	22.5792	33.8688
12	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1536x
16	-	6.1440	8.1920	12.2880	16.3840	24.5760
22.05	-	8.4672	11.2896	16.9344	22.5792	33.8688
24	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

9. PCB LAYOUT CONSIDERATIONS

9.1 Power Supply, Grounding

As with any high-resolution converter, the CS43L21 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 9 shows the recommended power arrangements, with VA and VA_HP connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS43L21 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS43L21 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CS43L21 evaluation board demonstrates the optimum layout and power supply arrangements.

9.2 QFN Thermal Pad

The CS43L21 is available in a compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS43L21 evaluation board demonstrates the optimum thermal pad and via configuration.

10.DIGITAL FILTERS

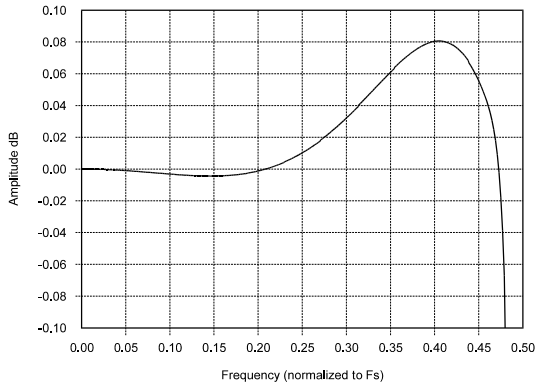


Figure 27. Passband Ripple

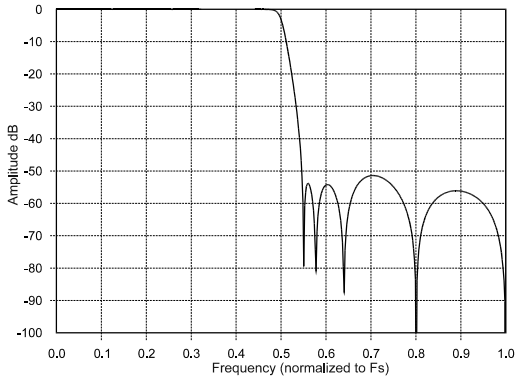


Figure 28. Stopband

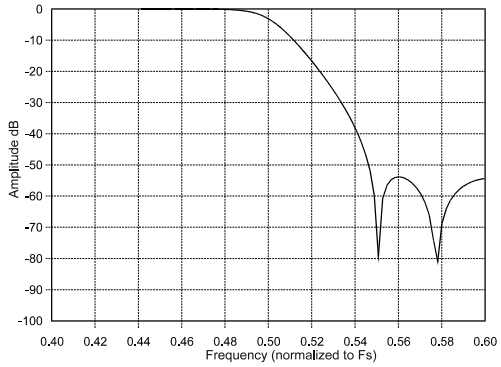


Figure 29. Transition Band

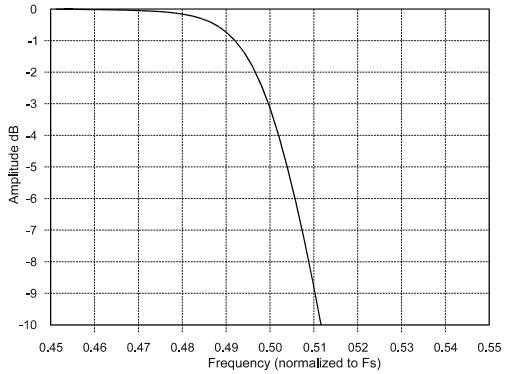


Figure 30. Transition Band (Detail)

11.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

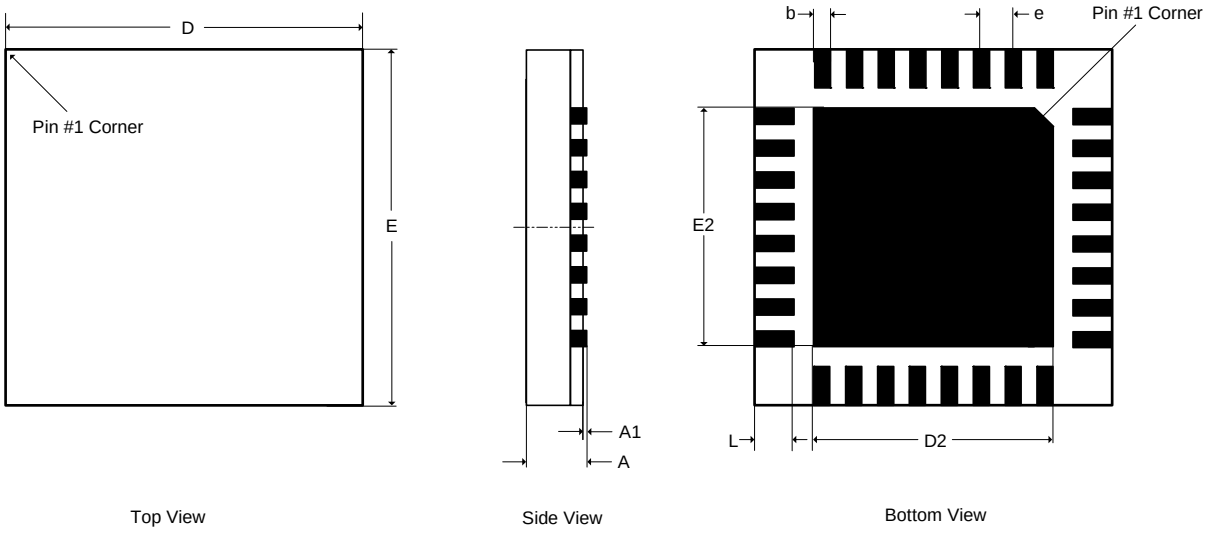
The deviation of the midscale transition (111...111 to 000...000) from the ideal. Units in mV.

12.REFERENCES

1. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000.
http://www.semiconductors.philips.com

13.PACKAGE DIMENSIONS

32L QFN (5 X 5 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D		0.1969 BSC			5.00 BSC		1
D2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
E		0.1969 BSC			5.00 BSC		1
E2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
e		0.0197 BSC			0.50 BSC		1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	52 38	- -	°C/Watt

14.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS43L21	Low-Power Stereo D/A with HP Amp for Portable Apps	32L-QFN	Yes	Commercial	-10 to +70° C	Rail	CS43L21-CNZ
						Tape & Reel	CS43L21-CNZR
				Automotive	-40 to +85° C	Rail	CS43L21-DNZ
						Tape & Reel	CS43L21-DNZR
CDB43L21	CS43L21 Evaluation Board	-	No	-	-	-	CDB43L21

15.REVISION HISTORY

Revision	Changes
F1	Updated voltage range in "Specified Operating Conditions" on page 11. Added and updated absolute maximum parameters in "Absolute Maximum Ratings" on page 11. Updated Figure 8. Output Architecture on page 24. Updated Section 4.7 "Recommended Power-Up Sequence" on page 31. Updated Section 4.8 "Recommended Power-Down Sequence" on page 32. Updated Section 4.9 "Software Mode" on page 34. Added note 1in the FREEZE control register in "DAC Control (Address 09h)" on page 43.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А