

0.95V to $V_{CC}-1V$, 0.5A/1.0A 1ch Ultra Low Dropout Linear Regulators

BD3540NUV BD3541NUV

General Description

The BD3540NUV, BD3541NUV are ultra low-dropout linear chipset regulator that operate from a very low input supply. They offer ideal performance in low input voltage to low output voltage applications. The input-to-output voltage difference is minimized by using a built-in N-Channel power MOSFET with a maximum ON-Resistance of $R_{ON}=400m\Omega(Typ)$, $200m\Omega(Typ)$. By lowering the dropout voltage, the regulator realizes high output current ($I_{OUTMAX}=0.5A$ to $1.0A$) thereby, reducing conversion loss, making it comparable to a switching regulator and its power transistor, choke coil, and rectifier diode constituents. The BD3540NUV, BD3541NUV are available in significantly downsized package profiles and allow low-cost design. An external resistor allows the entire range of output voltage configurations between 0.65V and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to a required power supply sequence.

Features

- High-Precision Voltage Regulator ($0.65V\pm 1\%$)
- Built-in VCC Undervoltage Lockout Circuit
- NRCS (soft start) Function Reduces the Magnitude of In-rush Current
- Internal N-Channel MOSFET Driver Offers Low ON-Resistance
- Built-in Current Limit Circuit
- Built-in Thermal Shutdown (TSD) Circuit
- Variable Output
- Tracking Function

Key Specifications

- IN Input Voltage Range: 0.95V to $V_{CC}-1V$
- VCC Input Voltage Range: 3.0V to 5.5V
- Output Voltage Range: 0.65V to $V_{IN}-0.9V$
- Output Current:
 - BD3540NUV 0.5A (Max)
 - BD3541NUV 1.0A (Max)
- ON-Resistance:
 - BD3540NUV 400m $\Omega(Typ)$
 - BD3541NUV 200m $\Omega(Typ)$
- Standby Current: 0 $\mu A(Typ)$
- Operating Temperature Range: -10°C to +100°C

Package

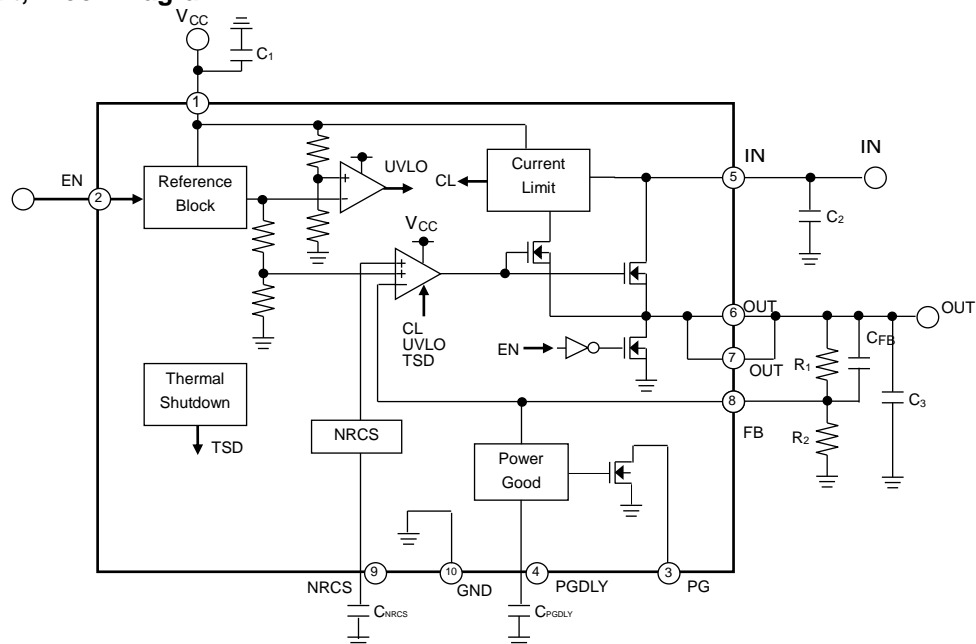
W(Typ) x D(Typ) x H(Max)



Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

Typical Application Circuit, Block Diagram



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Descriptions

| Pin No. | Pin Name | PIN Function |
|---------|----------|--|
| 1 | VCC | Power supply pin |
| 2 | EN | Enable input pin |
| 3 | PG | Power Good pin |
| 4 | PGDLY | Power Good Delay capacitor connection pin |
| 5 | IN | Input voltage pin |
| 6 | OUT | Output voltage pin |
| 7 | OUT | Output voltage pin |
| 8 | FB | Reference voltage feedback pin |
| 9 | NRCS | In-rush current protection (NRCS) capacitor connection pin |
| 10 | GND | Ground pin |

Description of Blocks

- AMP**
 This is an error amp that compares the reference voltage (0.65V) with FB voltage to drive the output N-Channel FET. Frequency optimization aids in attaining rapid transient response, and to support the use of ceramic capacitors on the output. The AMP output voltage ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output of the N-Channel FET switches OFF.
- EN**
 The EN block controls the ON and OFF state of the regulator via the EN logic input pin. During OFF state, circuit voltage stabilizes at 0μA which minimizes the current consumption during standby mode. The FET is switched ON to enable discharge of the NRCS and OUT, thereby draining the excess charge and preventing the load side of an IC from malfunctioning. Since there is no electrical connection required (e.g. between the VCC pin and the ESD prevention diode), module operation is independent of the input sequence.
- UVLO**
 To prevent malfunctions that can occur during a sudden decrease in VCC, the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and OUT. Once the UVLO threshold voltage (TYP2.5V) is reached, the power-ON reset is triggered and output is restored.
- CURRENT LIMIT**
 During ON state, the current limit function monitors the output current of the IC against the current limit value (1.0A or more: BD3540NUV). When output current exceeds this value, this block lowers the output current to protect the load of the IC. When it overcomes the overcurrent state, output voltage is restored to the normal value.
- NRCS (Non Rush Current on Start-up)**
 The soft start function is enabled by connecting an external capacitor between the NRCS pin and GND. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Output start time is calculated by formula (1) below.

$$t = C \frac{0.65V}{20\mu A} \dots (1)$$

Tracking sequence is possible by connecting the NRCS output to an external power supply instead of external capacitor. And then, ratio-metric sequence is also available by changing the resistor-divider ratio of external power supply voltage. (See page 13)

- TSD (Thermal Shut down)**
 The shutdown (TSD) circuit automatically latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus protecting the IC against "thermal runaway" and heat damage. Since the TSD circuit is designed only to shut down the IC in the occurrence of extreme heat, it is important that the T_j (max) parameter should not be exceeded in the thermal design, in order to avoid potential problems with the TSD.
- IN**
 The IN line acts as the major current supply line, and is connected to the output N-Channel FET drain. Since there is no electrical connection (such as between the CC pin and the ESD protection diode) required, IN operates independent of the input sequence. However, since an output N-Channel FET body diode exists between IN and OUT, a $V_{IN-V_{OUT}}$ electric (diode) connection is present. Therefore, that when output is switched ON or OFF, reverse current may flow from OUT to IN.

Description of Blocks – continued

8. PGOOD
It determines the status of the output voltage. This is an open-drain pin, which is connected to VCC pin through the pull-up resistance (100kΩ or so). PGOOD will be judged HIGH between the FB voltage 0.585V (TYP) to 0.715V(TYP), and will be judged LOW if the voltage is out of this range.
9. PGDLY
PGOOD output delay can be set by connecting PGDLY pin to a 100pF capacitor.
PGOOD delay time is determined by the following formula.

$$t_{\text{PGDLY}} = \frac{C(\text{pF}) \times 0.75}{I_{\text{PGDLY}}(\mu\text{A})} \quad (\mu\text{sec})$$

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Limit | | Unit |
|-----------------------------|--------------------|---------------|-----------|------|
| | | BD3540NUV | BD3541NUV | |
| Input Voltage 1 | V _{CC} | +6.0 (Note 1) | | V |
| Input Voltage 2 | V _{IN} | +6.0 (Note 1) | | V |
| Enable Input Voltage | V _{EN} | -0.3 to +6.0 | | V |
| PGOOD Input Voltage | V _{PGOOD} | +6.0 (Note 1) | | V |
| Power Dissipation 1 | Pd1 | 0.70 (Note 2) | | W |
| Power Dissipation 2 | Pd2 | 1.27 (Note 3) | | W |
| Power Dissipation 3 | Pd3 | 3.03 (Note 4) | | W |
| Operating Temperature Range | Topr | -10 to +100 | | °C |
| Storage Temperature Range | Tstg | -55 to +150 | | °C |
| Junction Temperature | Tjmax | +150 | | °C |

(Note 1) Should not exceed Pd.

(Note 2) Derate by 5.6mW/°C for Ta above 25°C (when mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, 1-layer) copper foil area 0mm²

(Note 3) Derate 10.1mW/°C for Ta above 25°C (when mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, 4-layer) copper foil area 6.28mm²

(Note 4) Derate by 24.2mW/°C for Ta above 25°C (when mounted on a 74.2mm x 74.2mm x 1.6mm glass-epoxy board, 4-layer) copper foil area 5505mm²

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|--------------------|-----------------|-----------------------------|------|
| Input Voltage 1 | V _{CC} | 3.0 | 5.5 | V |
| Input Voltage 2 | V _{IN} | 0.95 | V _{CC} -1 (Note 5) | V |
| Output Current | I _{OUT} | - | BD3540NUV | A |
| | | | 0.5 | |
| PGOOD Input Voltage | V _{PGOOD} | -0.3 | 5.5 | V |
| Output Voltage Setting Range | V _{OUT} | V _{FB} | V _{IN} -0.9 | V |
| Enable Input Voltage | V _{EN} | -0.3 | 5.5 | V |

(Note 5) V_{CC} and IN do not have to be implemented in the order listed.

Electrical Characteristics

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$, $V_{EN}=3\text{V}$, $V_{IN}=1.7\text{V}$, $R_1=3.9\text{k}\Omega$, $R_2=3.3\text{k}\Omega$)

| Parameter | Symbol | Limit | | | Unit | Conditions | |
|---|--------------|-----------------------|----------------------|-----------------------|-----------------------|--|---|
| | | Min | Typ | Max | | | |
| Circuit Current | I_{CC} | - | 0.7 | 1.0 | mA | | |
| VCC Shutdown Mode Current | I_{ST} | - | 0 | 10 | μA | $V_{EN}=0\text{V}$ | |
| Output Voltage Temperature Coefficient | T_{CVO} | - | 0.01 | - | $\%/^{\circ}\text{C}$ | | |
| Feedback Voltage 1 | V_{FB1} | 0.643 | 0.650 | 0.657 | V | | |
| Feedback Voltage 2 | V_{FB2} | 0.637 | 0.650 | 0.663 | V | $T_j=-10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ | |
| Load Regulation | Reg.L | - | 0.5 | 10 | mV | (BD3540NUV $I_{OUT}=0\text{A}$ to 0.5A) (BD3541NUV $I_{OUT}=0\text{A}$ to 1.0A) | |
| Line Regulation 1 | Reg.I1 | - | 0.1 | 0.5 | $\%/V$ | $V_{CC}=3.0\text{V}$ to 5.5V | |
| Line Regulation 2 | Reg.I2 | - | 0.1 | 0.5 | $\%/V$ | $V_{IN}=1.5\text{V}$ to 3.3V | |
| Standby Discharge Current | I_{DEN} | 1 | - | - | mA | $V_{EN}=0\text{V}$, $V_{OUT}=1\text{V}$ | |
| [ENABLE] | | | | | | | |
| Enable Pin Input Voltage High | V_{ENHI} | 2 | - | - | V | | |
| Enable Pin Input Voltage Low | V_{ENLOW} | 0 | - | $V_{CC} \times 0.15$ | V | | |
| Enable Input Bias Current | I_{EN} | - | 7 | 10 | μA | $V_{EN}=3\text{V}$ | |
| [NRCS] | | | | | | | |
| NRCS Charge Current | I_{NRCS} | 14 | 20 | 26 | μA | $V_{NRCS}=0.5\text{V}$ | |
| NRCS Standby Voltage | V_{STB} | - | 0 | 50 | mV | $V_{EN}=0\text{V}$ | |
| [UVLO] | | | | | | | |
| VCC Undervoltage Lockout Threshold Voltage | V_{CCUVLO} | 2.3 | 2.5 | 2.7 | V | VCC: Sweep-up | |
| VCC Undervoltage Lockout Hysteresis Voltage | V_{CCHYS} | 50 | 100 | 150 | mV | VCC: Sweep-down | |
| [PGOOD] | | | | | | | |
| Low-side Threshold Voltage | V_{THPGL} | $V_{OUT} \times 0.87$ | $V_{OUT} \times 0.9$ | $V_{OUT} \times 0.93$ | V | | |
| High-side Threshold Voltage | V_{THPGH} | $V_{OUT} \times 1.07$ | $V_{OUT} \times 1.1$ | $V_{OUT} \times 1.13$ | V | | |
| PGDLY Charge Current | I_{PGDLY} | 1.4 | 2.0 | 2.6 | μA | | |
| Ron | R_{PG} | 30 | 75 | 150 | Ω | | |
| [AMP] | | | | | | | |
| Minimum Dropout Voltage | BD3540NUV | dV_{OUT} | - | 200 | 300 | mV | $I_{OUT}=0.5\text{A}$, $V_{IN}=1.2\text{V}$, $T_a=-10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ |
| | BD3541NUV | dV_{OUT} | - | 200 | 300 | mV | $I_{OUT}=1.0\text{A}$, $V_{IN}=1.2\text{V}$, $T_a=-10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ |

Typical Waveforms

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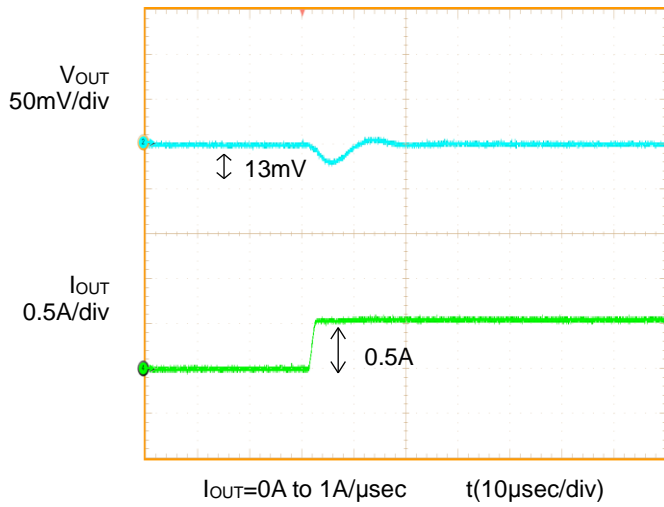


Figure 1. Transient Response
(0A to 0.5A)
 $C_{OUT}=100\mu F, C_{FB}=1000pF$

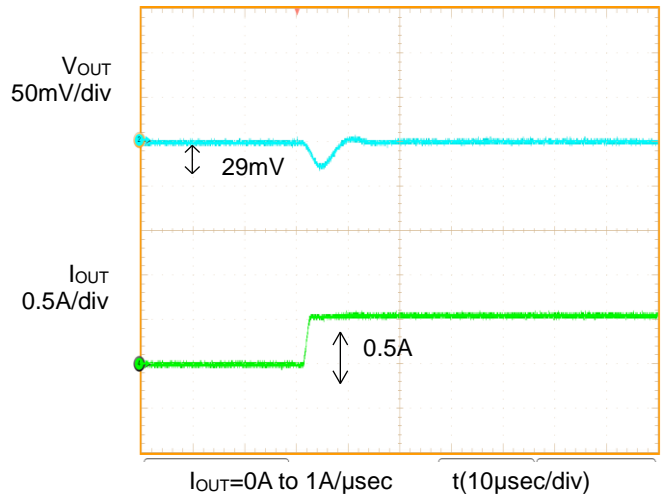


Figure 2. Transient Response
(0A to 0.5A)
 $C_{OUT}=47\mu F, C_{FB}=1000pF$

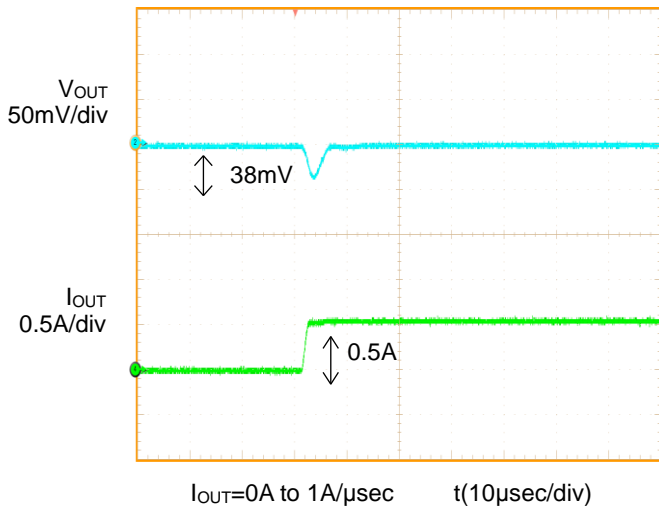


Figure 3. Transient Response
(0A to 0.5A)
 $C_{OUT}=22\mu F, C_{FB}=1000pF$

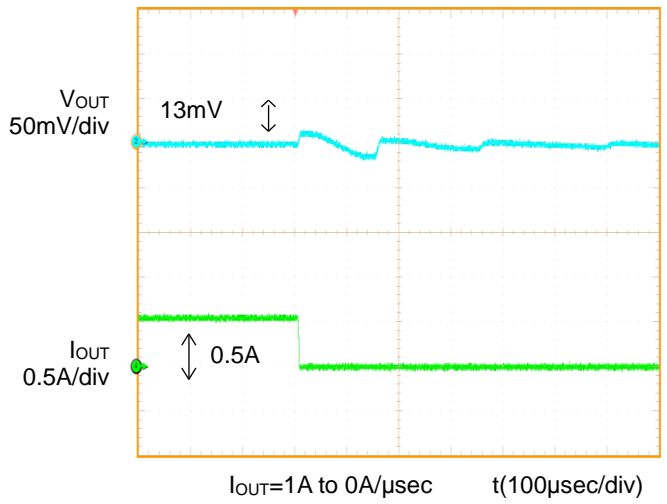


Figure 4. Transient Response
(0.5A to 0A)
 $C_{OUT}=100\mu F, C_{FB}=1000pF$

Typical Waveforms – continued

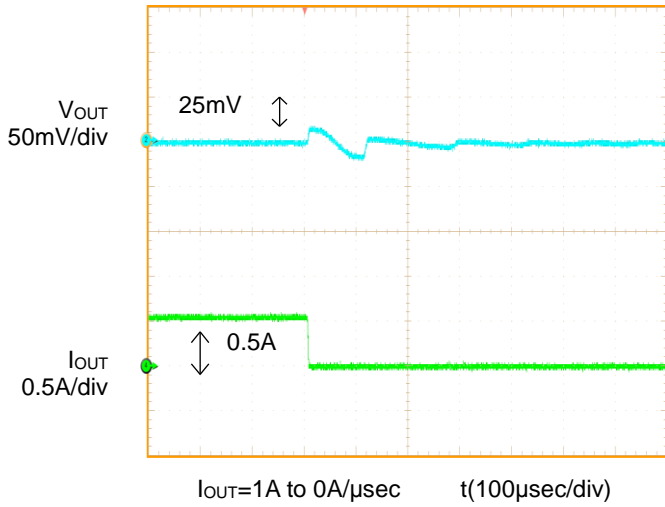


Figure 5. Transient Response
(0.5 to 0A)
 $C_{OUT}=47\mu F, C_{FB}=1000pF$

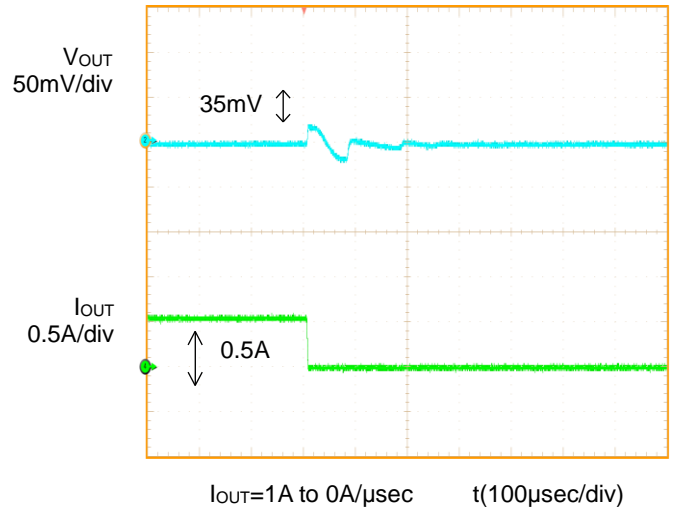


Figure 6. Transient Response
(0.5A to 0A)
 $C_{OUT}=22\mu F, C_{FB}=1000pF$

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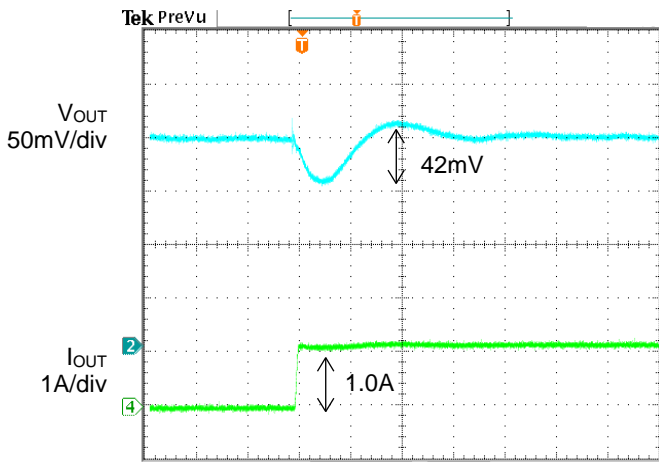


Figure 7. Transient Response
(0A to 1.0A)
 $C_{OUT}=100\mu F, C_{FB}=1000pF$

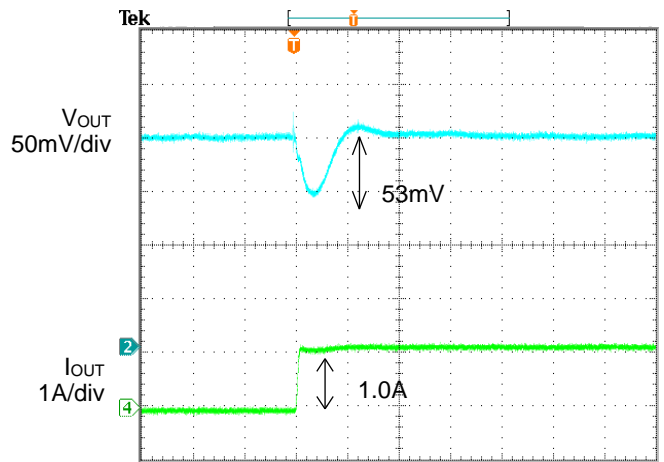


Figure 8. Transient Response
(0A to 1.0A)
 $C_{OUT}=47\mu F, C_{FB}=1000pF$

Typical Waveforms – continued

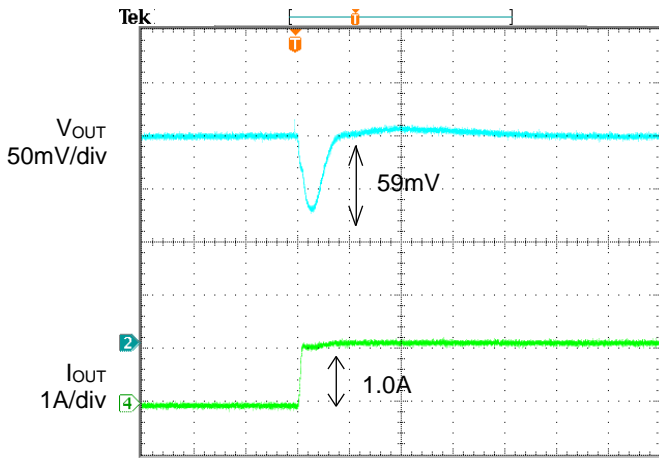


Figure 9. Transient Response
(0A to 1.0A)
 $C_{OUT}=22\mu\text{F}$, $C_{FB}=1000\text{pF}$

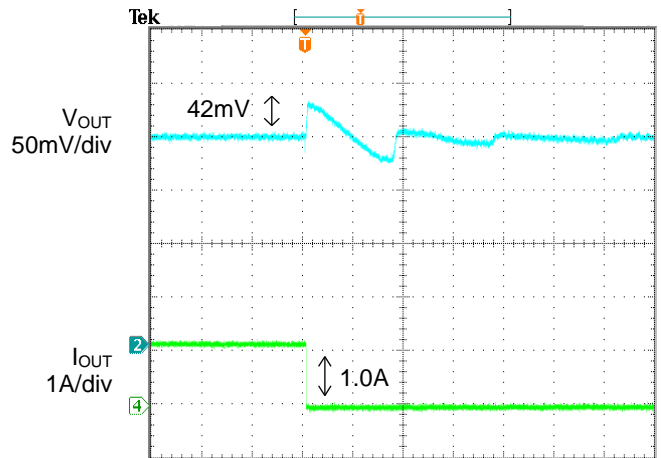


Figure 10. Transient Response
(1.0A to 0A)
 $C_{OUT}=100\mu\text{F}$, $C_{FB}=1000\text{pF}$

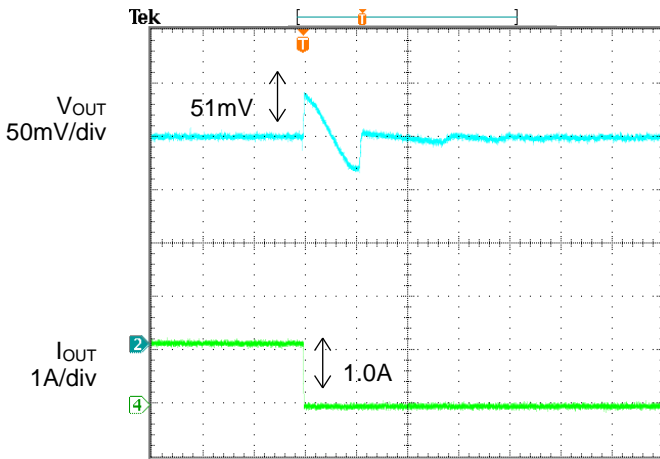


Figure 11. Transient Response
(1.0A to 0A)
 $C_{OUT}=47\mu\text{F}$, $C_{FB}=1000\text{pF}$

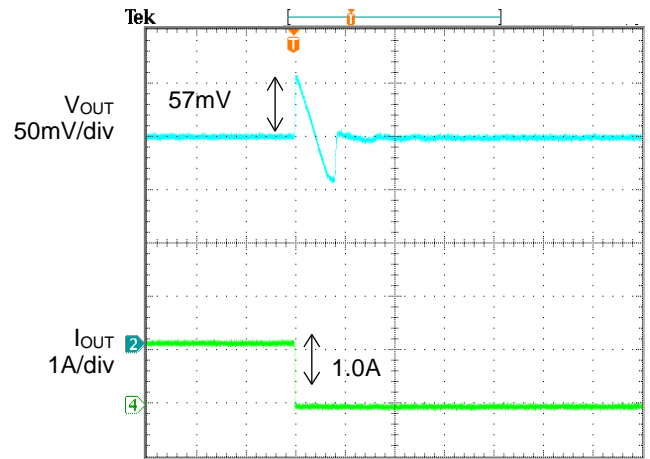


Figure 12. Transient Response
(1.0A to 0A)
 $C_{OUT}=22\mu\text{F}$, $C_{FB}=1000\text{pF}$

Typical Waveforms – continued

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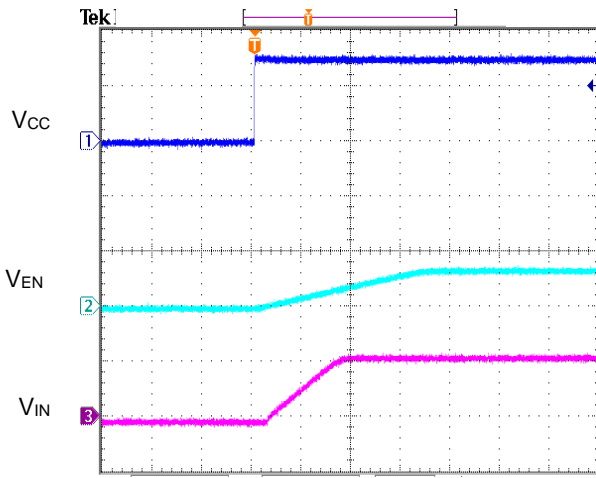


Figure 13. Waveform at Output Start

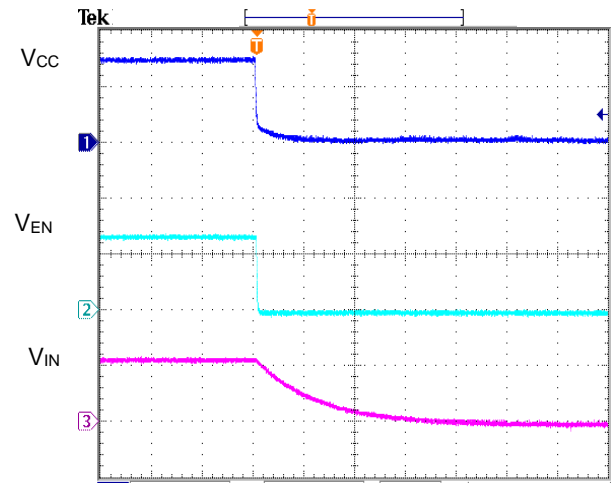


Figure 14. Waveform at Output OFF

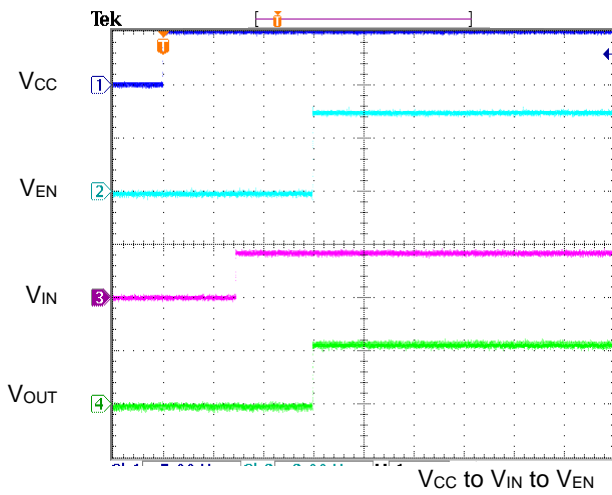


Figure 15. Input Sequence

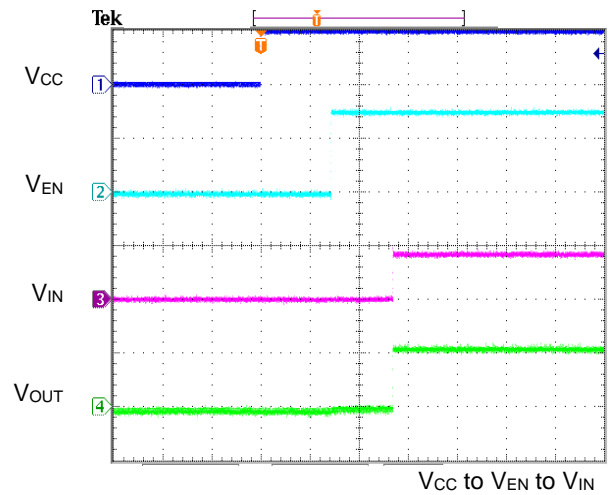


Figure 16. Input Sequence

Typical Waveforms – continued

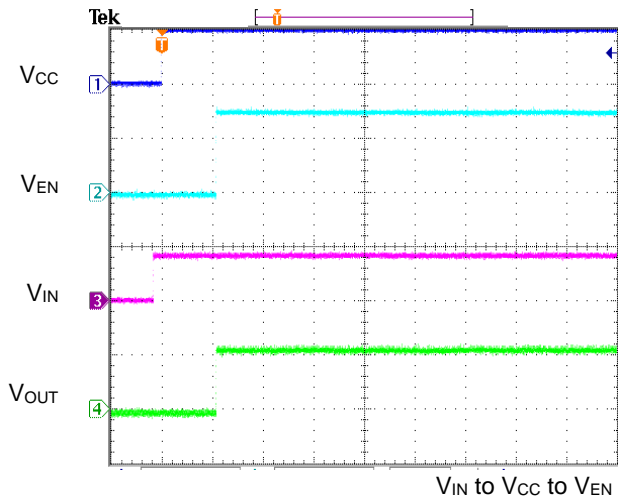


Figure 17. Input Sequence

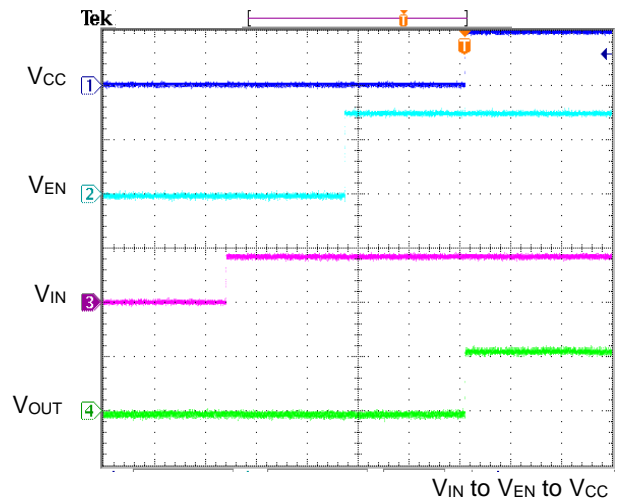


Figure 18. Input Sequence

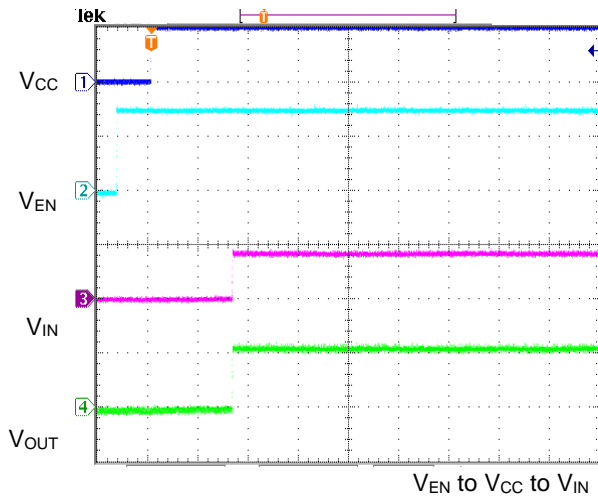


Figure 19. Input Sequence

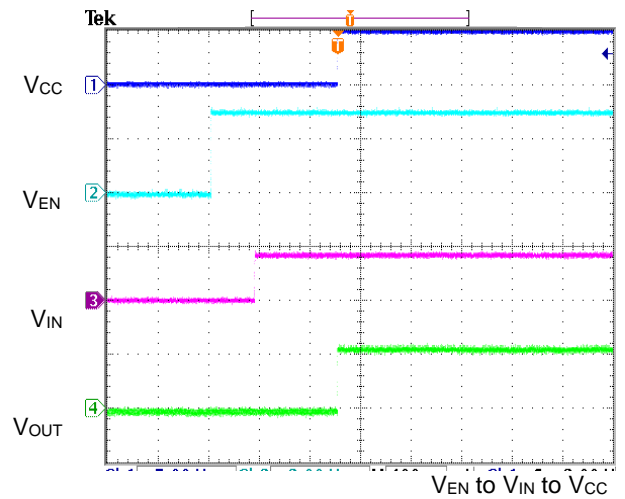


Figure 20. Input sequence

Typical Performance Curves

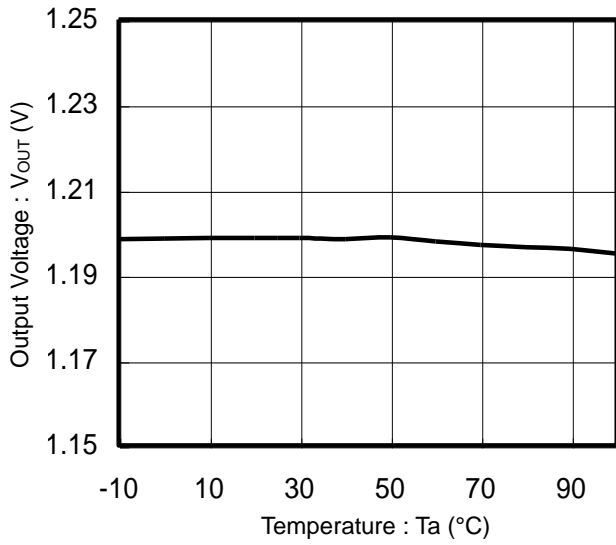


Figure 21. Output Voltage vs Temperature (I_{OUT}=0mA)

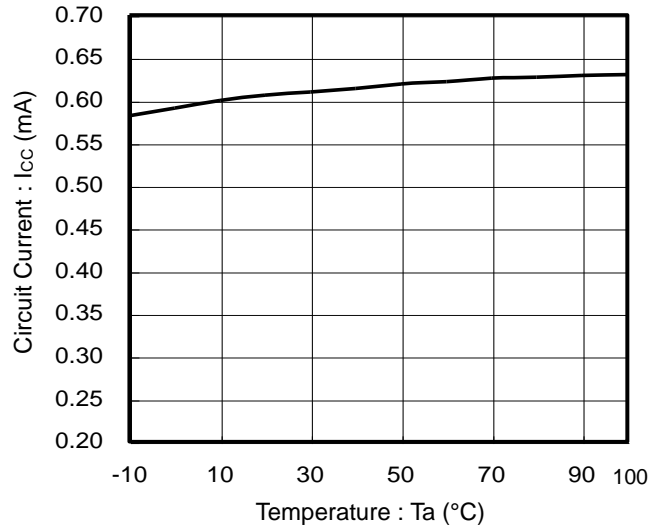


Figure 22. Circuit Current vs Temperature

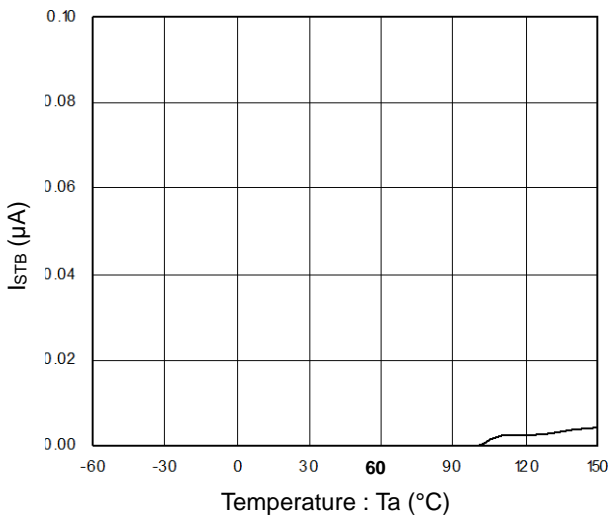


Figure 23. I_{STB} vs Temperature

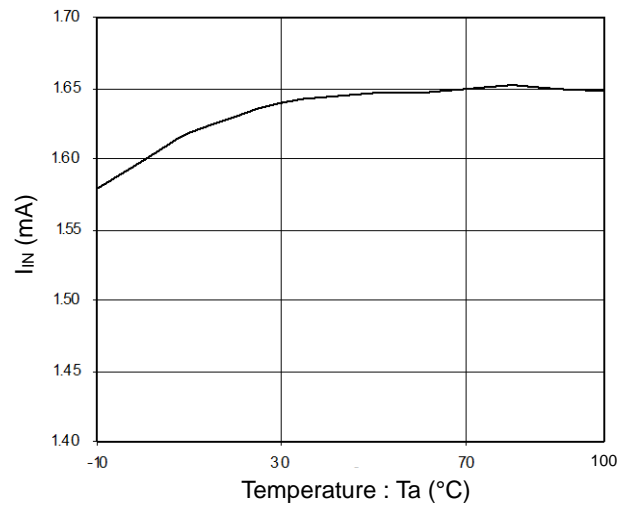


Figure 24. I_{IN} vs Temperature

Typical Performance Curves – continued

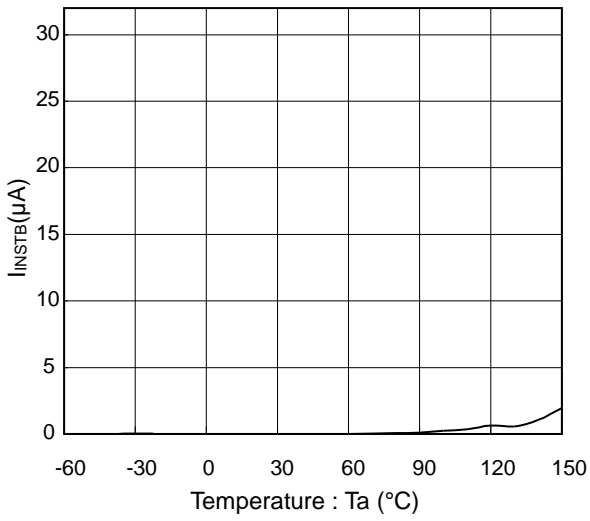


Figure 25. I_{INSTB} vs Temperature

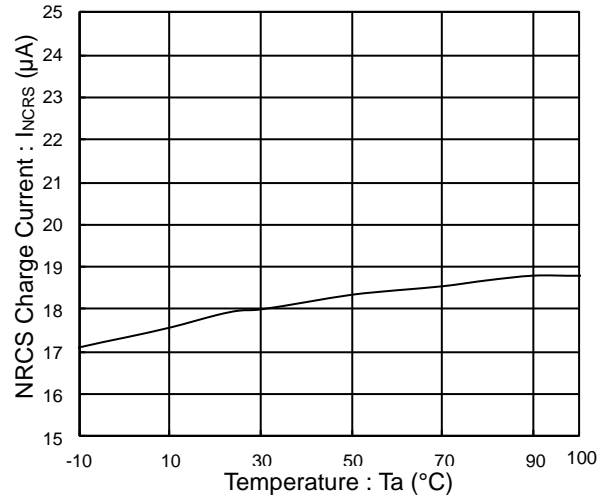


Figure 26. NCRS Charge Current vs Temperature

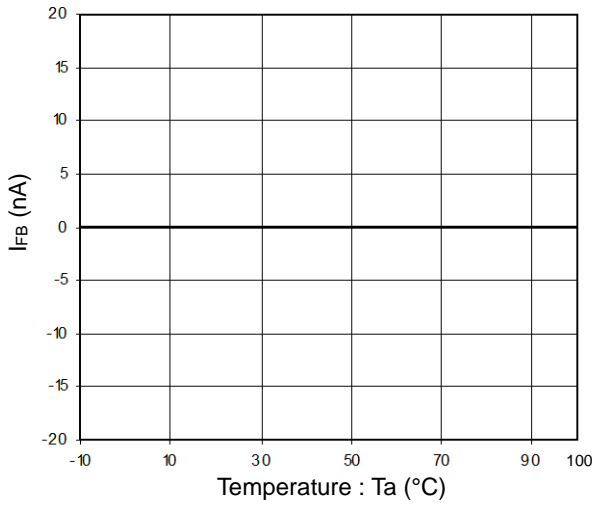


Figure 27. I_{FB} vs Temperature

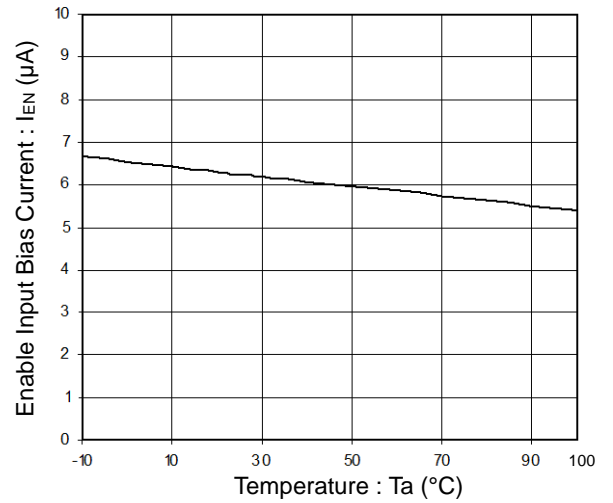


Figure 28. Enable Input Bias Current vs Temperature

Typical Performance Curves – continued

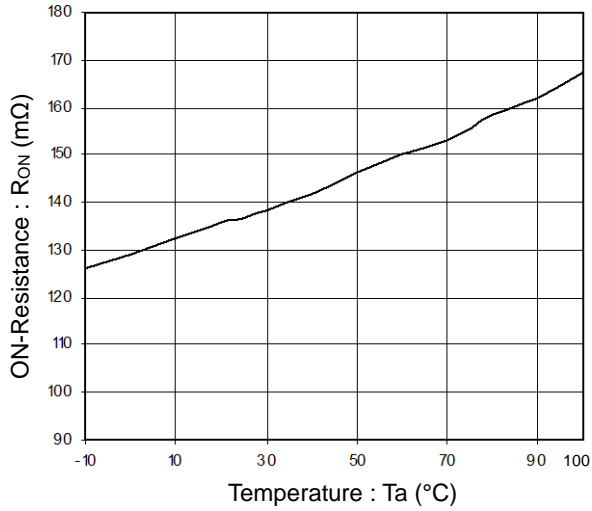


Figure 29. ON-Resistance vs Temperature
(V_{CC}=5V/V_{OUT}=1.2V)

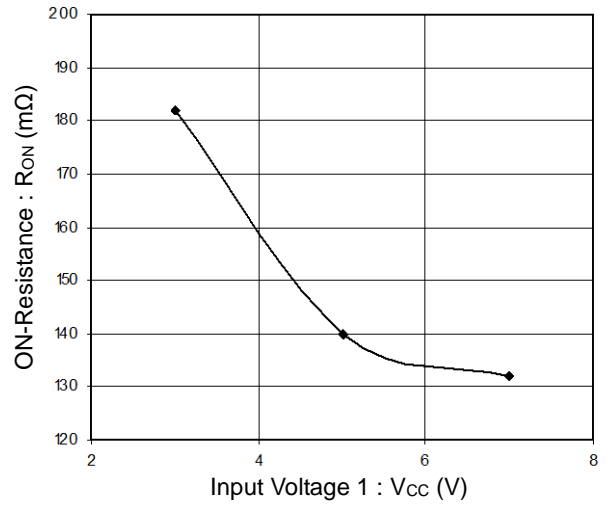
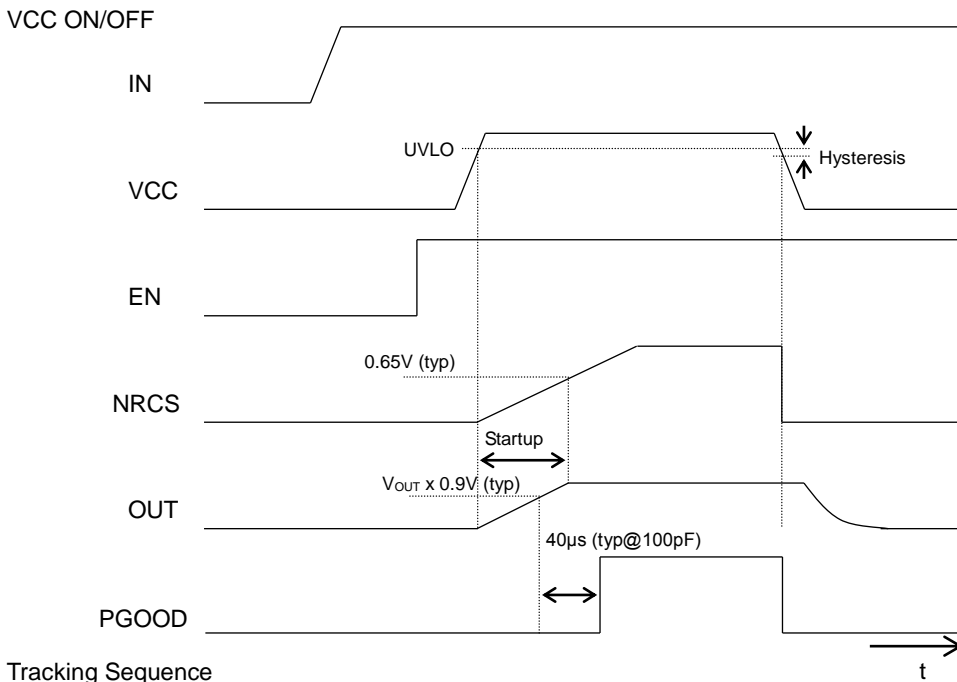
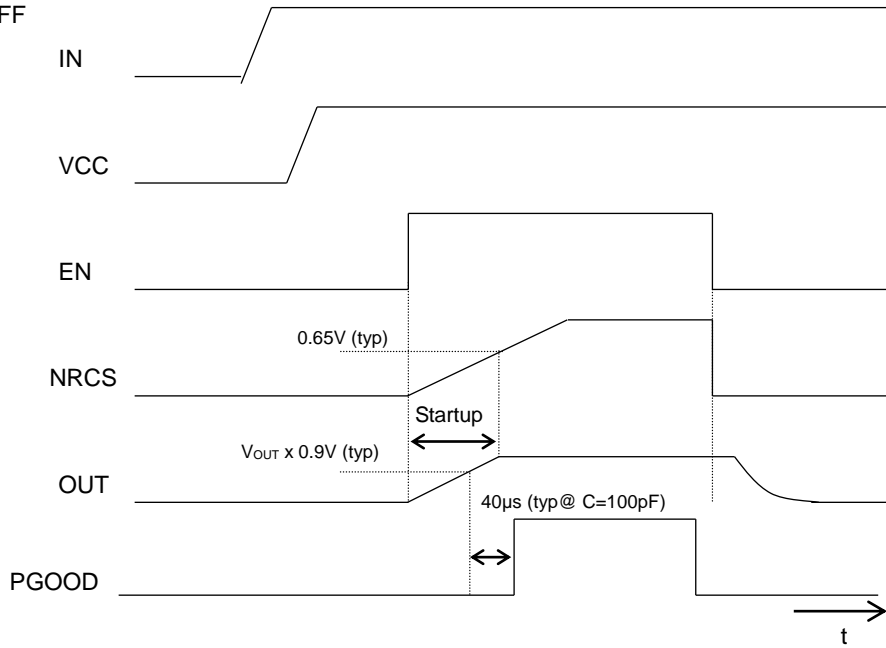
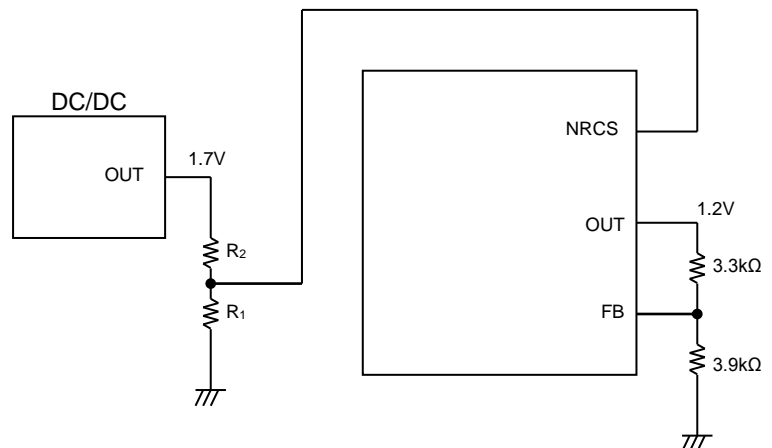
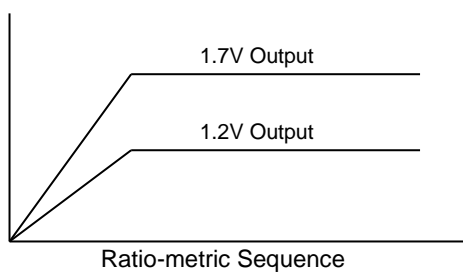
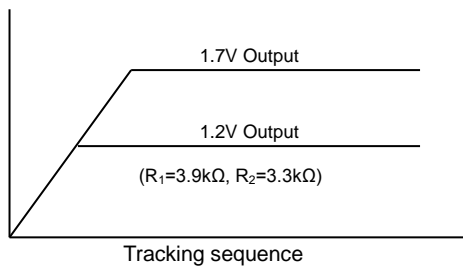


Figure 30. ON-Resistance vs Input Voltage 1

Timing Chart
EN ON/OFF



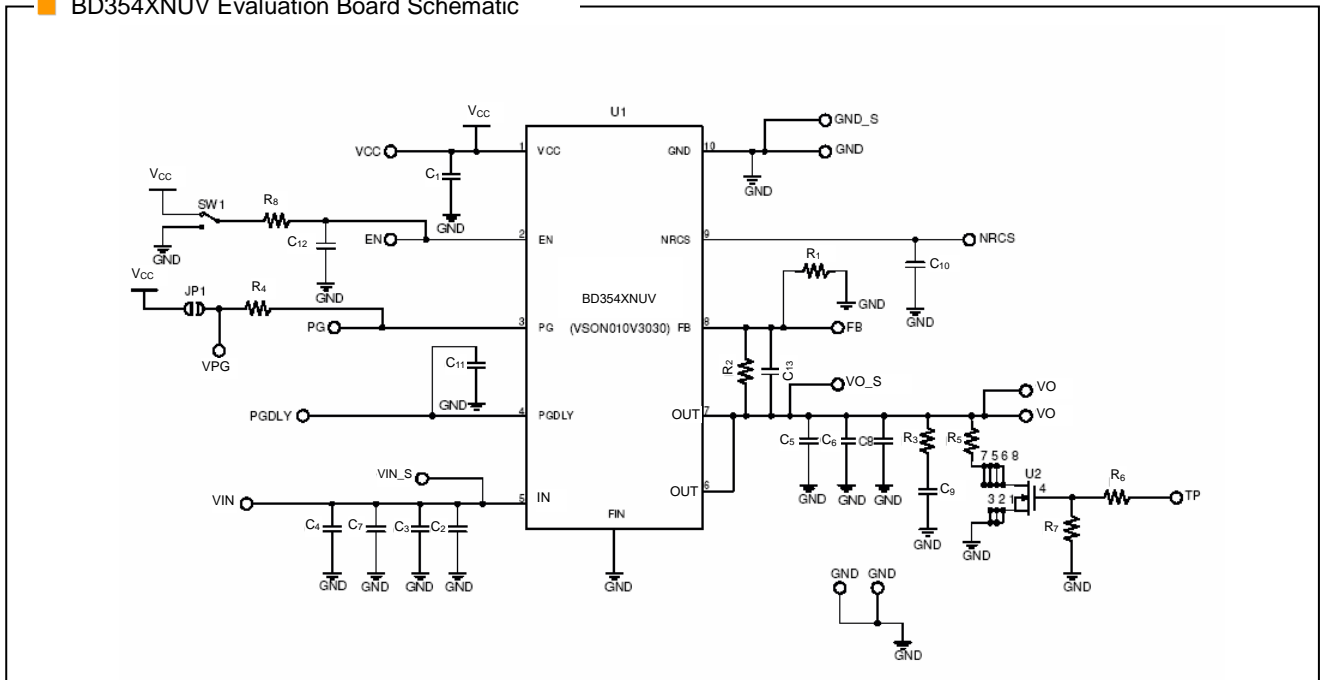
Tracking Sequence



Application Information

1. Evaluation Board

BD354XNUV Evaluation Board Schematic

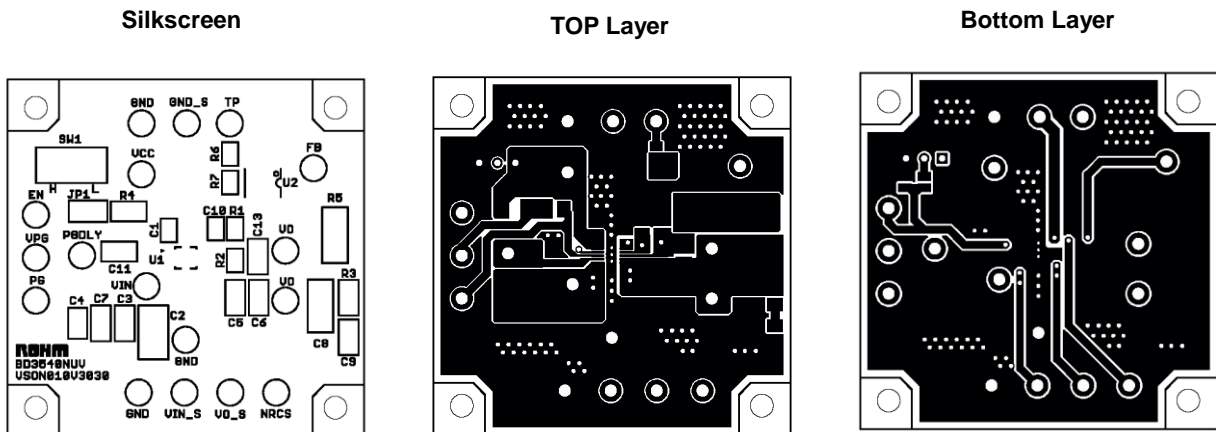


BD354XNUV Evaluation Board Standard Component List

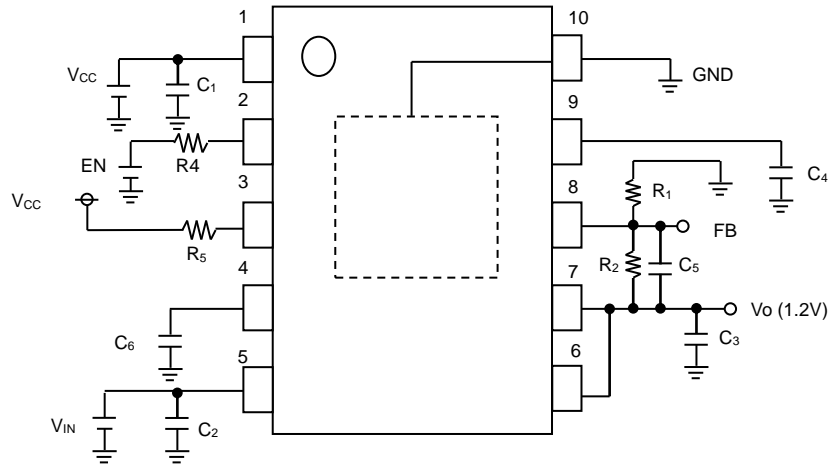
| Component | Rating | Manufacturer | Product Name |
|-----------|--------------|--------------|-----------------|
| U1 | - | ROHM | BD354XNUV |
| C1 | 1 μ F | MURATA | GRM188B11A105KD |
| C10 | 0.01 μ F | MURATA | GRM188B11H103KD |
| C11 | 100pF | MURATA | GRM188B11H101KD |
| R8 | 0 Ω | - | Jumper |
| C5 | 22 μ F | KYOCERA | CM32X5R226M10A |

| Component | Rating | Manufacturer | Product Name |
|-----------|---------------|--------------|-----------------|
| C2 | 22 μ F | KYOCERA | CM32X5R226M10A |
| C13 | 1000pF | MURATA | GRM188B11H102KD |
| R1 | 3.9k Ω | ROHM | MCR03EZPF3301 |
| R2 | 3.3k Ω | ROHM | MCR03EZPF3901 |
| R4 | 100k Ω | ROHM | MCR03EZPF |

BD354XNUV Evaluation Board Layout
(2nd layer and 3rd layer are GND Line.)

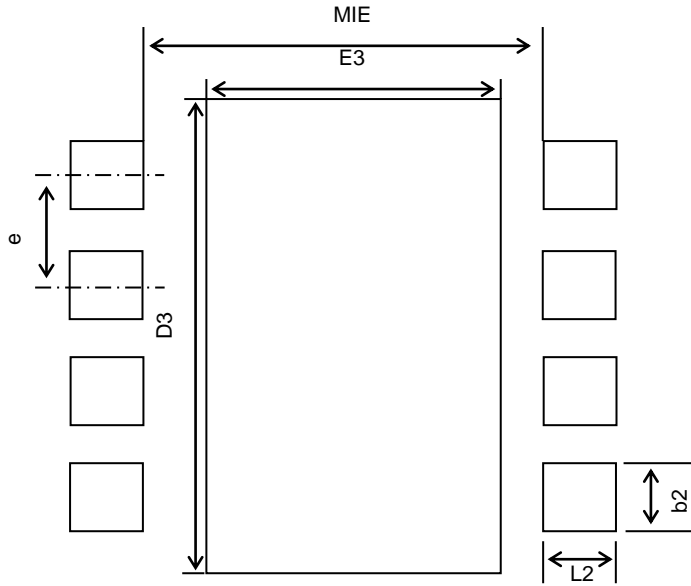


2. Recommended Circuit Example



| Component | Recommended Value | Programming Notes and Precautions |
|--------------------------------|----------------------------|---|
| R ₁ /R ₂ | 3.9k/3.3k | IC output voltage can be set with a configuration formula using the values for the internal reference output voltage (V _{FB}) and the output voltage resistors (R ₁ , R ₂). Select resistance values that will avoid the impact of the VREF current (±100nA). The recommended total resistance value is 10KΩ. |
| C ₃ | 22μF | To assure output voltage stability, make sure the OUT pins and the GND pin are connected. Output capacitors play a role in loop gain phase compensation and in minimizing output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22μF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions. |
| C ₁ /C ₂ | 1μF/22μF | Input capacitors reduce the output impedance of the voltage supply source connected to the (VCC, IN) input pins. If the impedance of this power supply were to increase, input voltage (VCC, VIN) could become unstable, leading to oscillation or decreased ripple rejection ability. While a low-ESR 1μF/22μF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions. |
| C ₄ | 0.01μF | The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (IN to OUT) and affecting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportional to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportional to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to ensure a stable soft-start time. |
| C ₅ | 1000pF | This component is employed when the C ₃ capacitor causes, or may cause, oscillation. It provides more precise internal phase correction. |
| C ₆ | 100pF | This capacitor is to set PGOOD delay time. 100pF is recommended. |
| R ₅ | 100k | This is pull-up resistor of Open Drain pin. 100kΩ is recommended. |
| R ₄ | Several kΩ to several 10kΩ | It is recommended that a resistance (several kΩ to several 10kΩ) be put in R ₄ , in case negative voltage is applied in EN pin. |

3. Reference Landing Pattern



(Unit : mm)

| | | | |
|--------------------|-------------------|----------------|---------------|
| Lead pitch | Lead pitch | landing length | landing pitch |
| e | MIE | ≥ 2 | b2 |
| 0.65 | 2.50 | 0.40 | 0.35 |
| central pad length | central pad pitch | | |
| D3 | E3 | | |
| 3.00 | 1.90 | | |

(Note) It is recommended to design suitable for the actual application.

4. Power Dissipation

In thermal design consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

- (1) Ambient temperature T_a can be no higher than 100°C.
- (2) Chip junction temperature (T_j) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

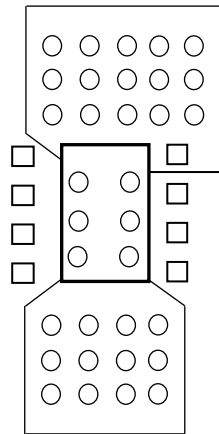
- ① Calculation based on ambient temperature (T_a)

$$T_j = T_a + \theta_j - a \times W$$

<Reference values>

| | | |
|----------------------------|--|--|
| θ_j -a:VSON010V3030 | 178.6°C/W | 1-layer substrate (copper foil density 0.2%) |
| | 98.4°C/W | 1-layer substrate (copper foil density 7%) |
| | 41.3°C/W | 2-layer substrate (copper foil density 65%) |
| | Substrate size: 70mm x 70 mm x 1.6mm ³ (substrate with thermal via) | |

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multilayer substrate). This package is so small (size: 3.0mm x 3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA as shown in the figure below), enable to achieve superior heat radiation characteristic. (This figure is an image only. It is recommended that the VIA size and the number is designed suitable for the actual situation.)



Most of the heat loss in BD354XNUV occurs at the output N-Channel FET. Power loss is determined by the total IN-OUT voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of IN and OUT in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD354XNUV) make sure to factor conditions such as substrate size into the thermal design.

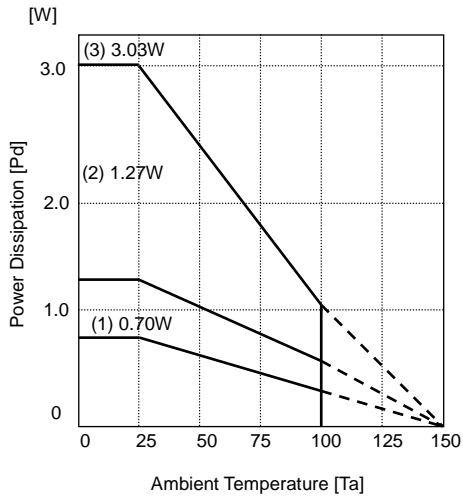
$$\text{Power consumption (W)} = \{ \text{Input voltage (V}_{IN}) - \text{Output voltage (V}_{OUT}) \} \times I_{OUT(Ave)}$$

Example)

Where $V_{IN}=1.7V$, $V_{OUT}=1.2V$, $I_{OUT(Ave)} = 1A$,

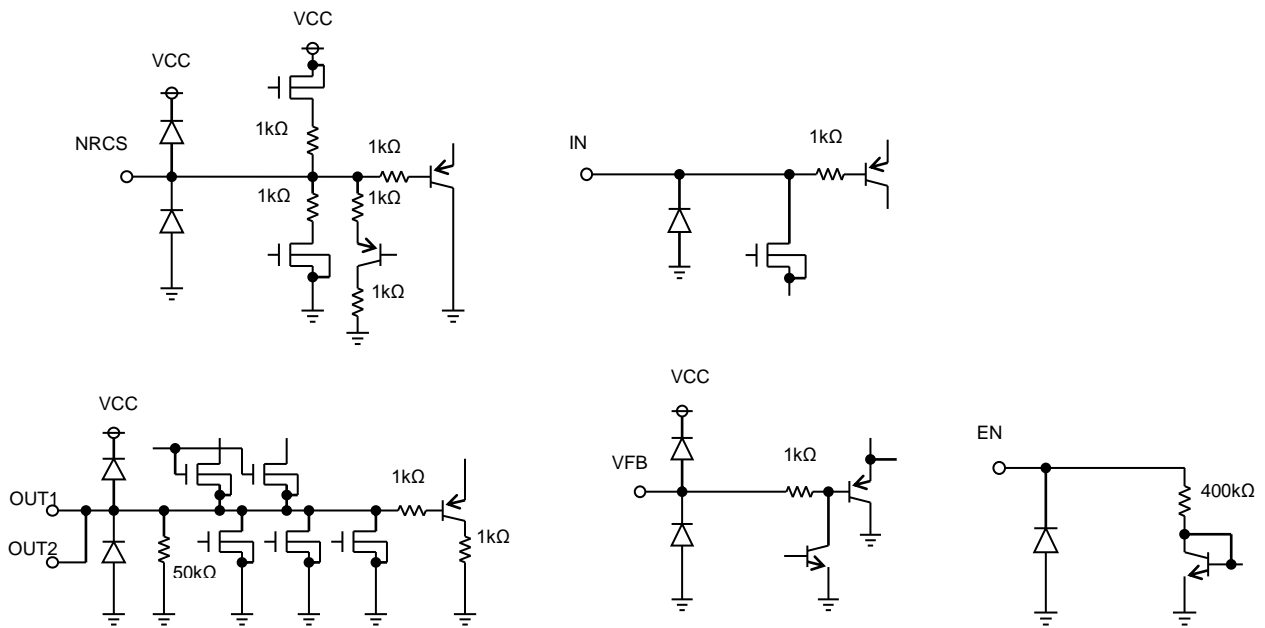
$$\begin{aligned} \text{Power consumption (W)} &= \{1.7(V) - 1.2(V)\} \times 1.0(A) \\ &= 0.5(W) \end{aligned}$$

VSON010V3030



- (1) Substrate (copper foil area: 0mm²...1-layer)
θ_{j-a}=178.6°C/W
- (2) Substrate (copper foil area: 6.28mm²...4-layer)
θ_{j-a}=98.4°C/W
- (3) Substrate (copper foil area: 5505mm²...4-layer)
θ_{j-a}=41.3°C/W

I/O Equivalent Circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

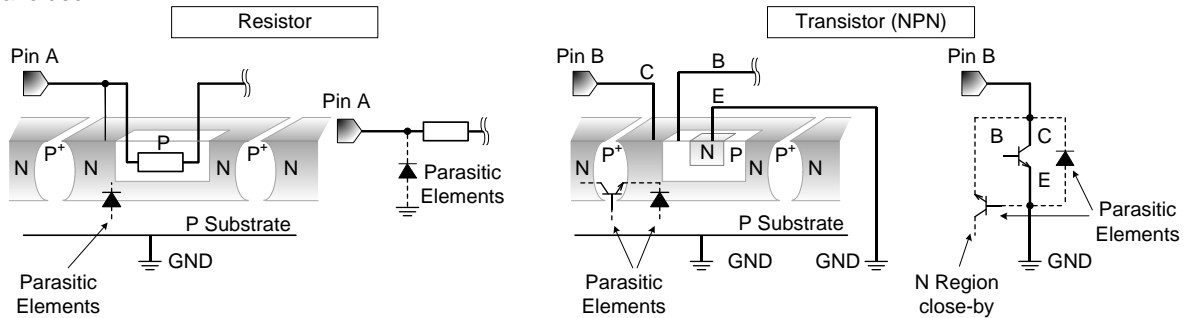


Figure 31. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

| TSD ON Temperature [°C] (typ) | Hysteresis Temperature [°C] (typ) |
|-----------------------------------|---------------------------------------|
| 175 | 15 |

15. Output Voltage Resistance Setting (R1, R2)

Output voltage resistance is adjusted with resistor R1 and R2. This IC is calculated as $V_{FB} \times (R_1 + R_2) / R_1$. Total 10kΩ is recommended so that the output voltage is not affected by the V_{FB} bias current.

16. Output Capacitors (C3)

To ensure output voltage stability, make sure that the OUT pin and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in preventing output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 47μF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.

17. Input Capacitors Setting (C1, C2)

Input capacitors reduce the impedance of the voltage supply source connected to the (VCC, IN) input pins. If the impedance of this power supply were to increase, input voltage (VCC, IN) could become unstable, leading to oscillation or decreased ripple rejection ability. Stability highly depends on the input power supply characteristic and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

Operational Notes – continued

18. NRCS Pin Capacitors Setting (C_{NRCS})

The Non Rush Current on Startup (NRCS) function is built in the IC to prevent rush current from going through the load (IN to OUT) and affecting output capacitors at power supply start-up. The constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportional to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportional to this reference voltage. To obtain a stable NRCS delay time, capacitors with low susceptibility to temperature are recommended.

19. Input Pins (VCC, IN, EN)

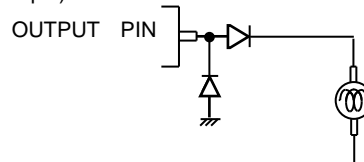
This IC's EN pin, IN pin, and VCC pin are isolated, and the UVLO function is built in the VCC pin to prevent under voltage lockout. It does not depend on the Input pin order. Output voltage starts up when VCC and EN reach the threshold voltage. However, note that when putting in IN pin lastly, OUT may result in overshooting.

20. Heat Sink (FIN)

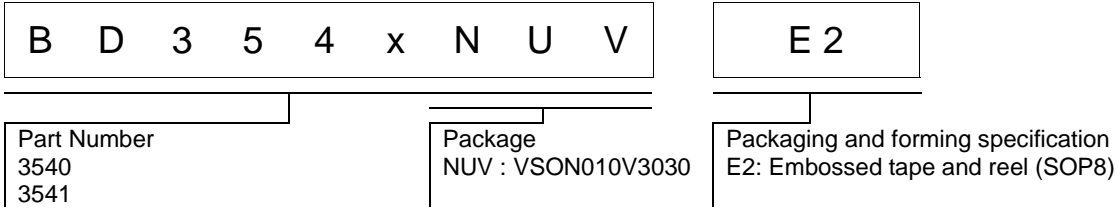
Since the heat sink (FIN) is connected to with the Sub, short it to the GND. It is possible to minimize the thermal resistance by properly soldering it to substrate.

- 21.** Add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at start-up or in output OFF condition.

(Example)

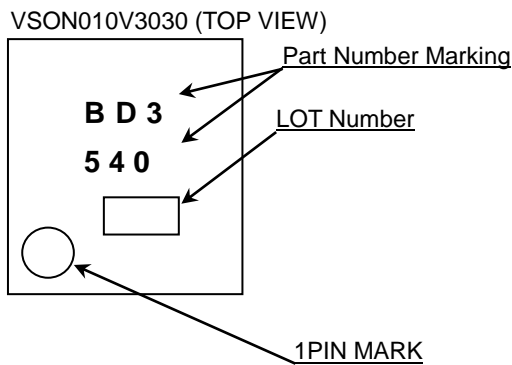


Ordering Information

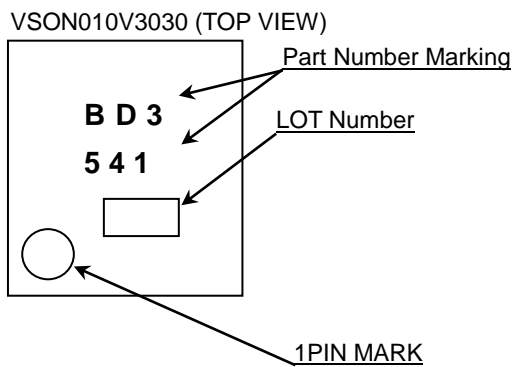


Marking Diagram

● BD3540NUV

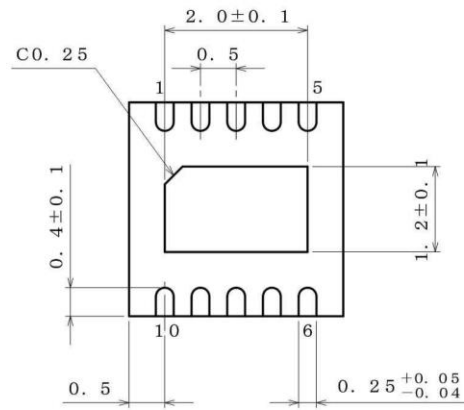
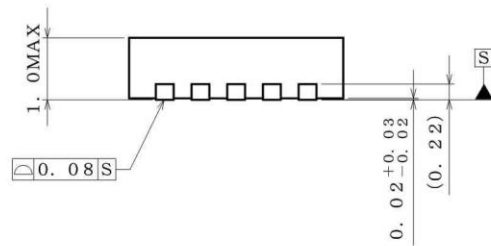
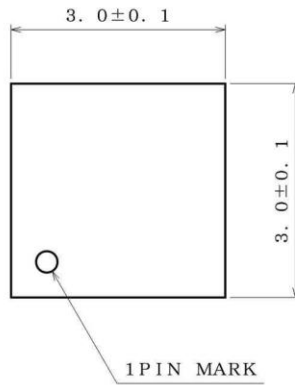


● BD3541NUV



Physical Dimension, Tape and Reel Information

| | |
|--------------|--------------|
| Package Name | VSON010V3030 |
|--------------|--------------|



(UNIT : mm)
 PKG : VSON010V3030
 Drawing No. EX184-5001-1

<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

Reel

1pin

Direction of feed

* Order quantity needs to be multiple of the minimum quantity.

Revision History

| Date | Revision | Changes |
|-------------|----------|-------------|
| 05.Oct.2015 | 001 | New Release |

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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Use of the Products in places subject to dew condensation
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- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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