ISO-CMOS 8x8 Analog Switch Array

Data Sheet

September 2011

Features

- Internal control latches and address decoder
- Short setup and hold times
- Wide operating voltage: 4.5 V to 13.2 V
- 12 Vpp analog signal capability
- R_{ON} 65 Ω max. @ V_{DD} = 12 V, 25°C
- $\Delta R_{ON} \leq 10\ \Omega$ @ V_{DD} = 12 V, 25C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology
- Internal pull-up resistor for $\overline{\text{RESET}}$ pin

Ordering Information

MT8809AP1	28 Pin PLCC*	Tubes
MT8809APR1	28 Pin PLCC*	Tape & Reel
MT8809AE1	28 Pin PDIP*	Tubes

* Pb Free Matte Tin

-40°C to +85°C

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Zarlink MT8809 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select ($\overline{\text{CS}}$) allows the crosspoint array to be cascaded for matrix expansion.

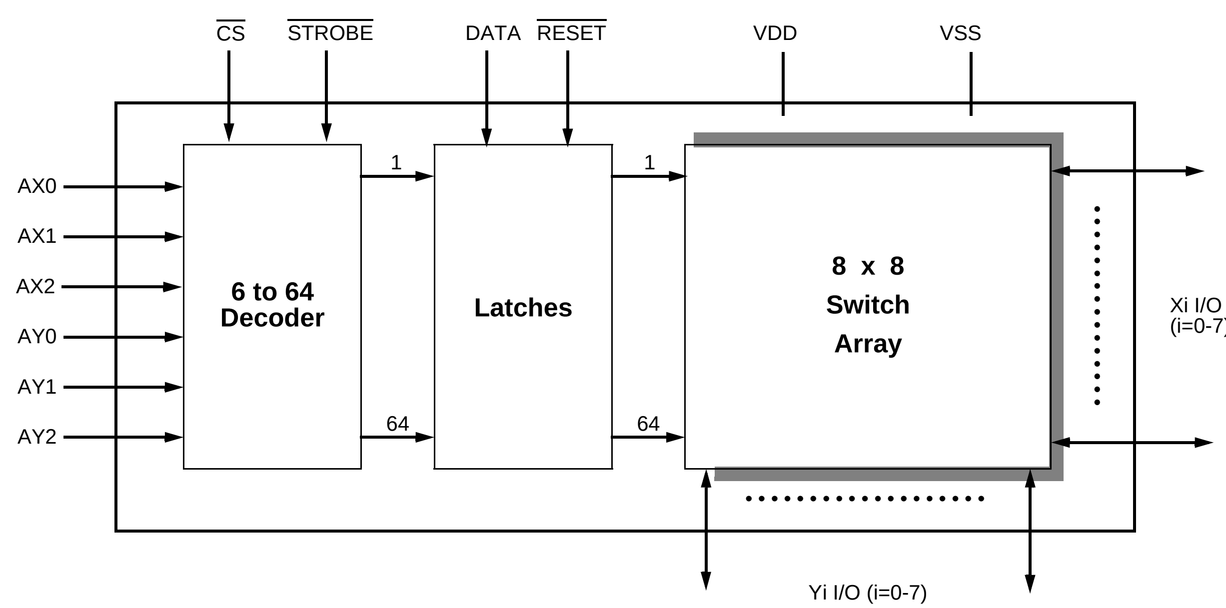

Figure 1 - Functional Block Diagram

Change Summary

Changes from the September 2005 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

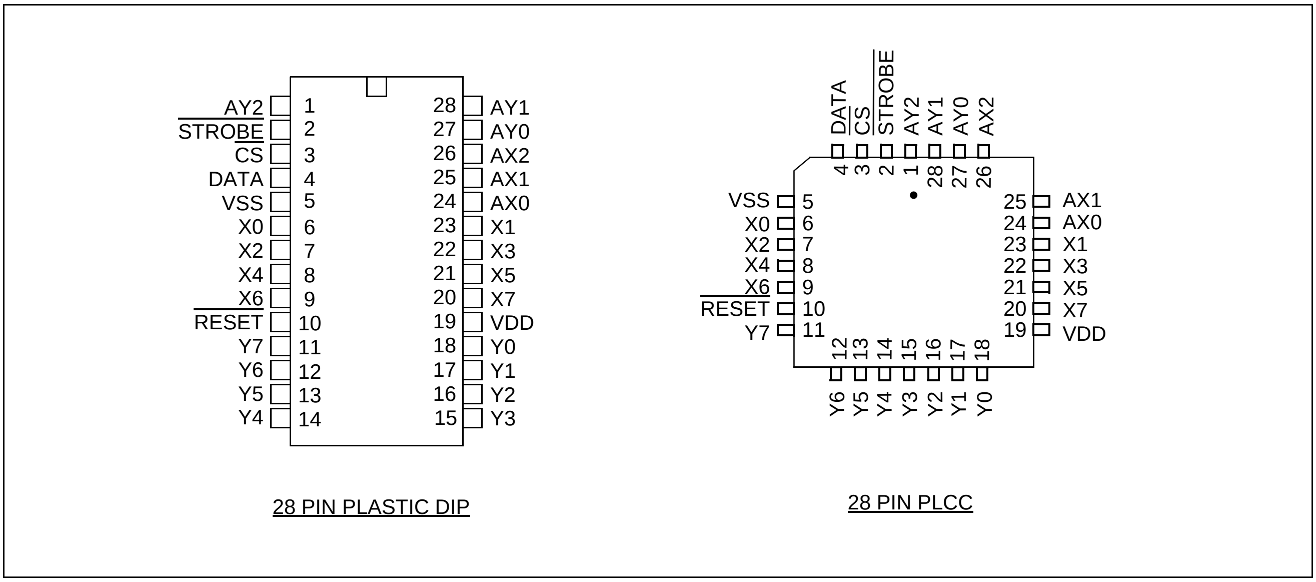

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input)**.
2	$\overline{\text{STROBE}}$	**$\overline{\text{STROBE}}$ (Input):** enables function selected by address and data. Address must be stable before $\overline{\text{STROBE}}$ goes low and DATA must be stable on the rising edge of $\overline{\text{STROBE}}$. Active Low.
3	$\overline{\text{CS}}$	**Chip Select (Input):** this is used to select the device. Active Low.
4	DATA	**DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	V_{SS}	**Ground Reference.**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	$\overline{\text{RESET}}$	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of $\overline{\text{CS}}$. A 100 kΩ internal pull-up resistor is also provided. This can be used in conjunction with a 0.1 μF capacitor (connected to the $\overline{\text{RESET}}$ pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	**Y7 - Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array.

Pin Description

Pin #	Name	Description
19	V_{DD}	**Positive Power Supply.**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	**AX0 - AX2 Address Lines (Inputs)**.
27, 28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs)**.

Functional Description

The MT8809 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the $\overline{\text{CS}}$ (Chip Select) and $\overline{\text{STROBE}}$ inputs are low and are latched on the rising edge of $\overline{\text{STROBE}}$. A logical “1” written into a memory cell turns the corresponding crosspoint switch on and a logical “0” turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical “0” on the $\overline{\text{RESET}}$ input will asynchronously return all memory locations to logical “0” turning off all crosspoint switches regardless of whether $\overline{\text{CS}}$ is high or low.

Address Decode

The six address inputs along with the $\overline{\text{STROBE}}$ and $\overline{\text{CS}}$ (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, $\overline{\text{RESET}}$ must be high and $\overline{\text{CS}}$ must go low while the address and data are set up. Then the $\overline{\text{STROBE}}$ input is set low and then high causing the data to be latched. The data can be changed while $\overline{\text{STROBE}}$ is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of $\overline{\text{STROBE}}$ in order for correct data to be written to the latch.

Absolute Maximum Ratings*- Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter		Symbol	Min.	Max.	Units
1	Supply Voltage		V_{DD} V_{SS}	-0.3 -0.3	15.0 V_{DD}+0.3	V V
2	Analog Input Voltage		V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D		0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†- Voltages are with respect to V_{SS} = 0 V, V_{DD} = 12 V unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at V_{IN} = V_{SS} V_{DD} except $\overline{RESET}$ = $V_{DD.}$
				120	400	μA	All digital inputs at V_{IN} = V_{SS} or V_{DD} except $\overline{RESET}$ = $V_{SS.}$
				0.5	1.6	mA	All digital inputs at V_{IN} = 2.4 V, V_{DD} = 5.0 V
				5	15	mA	All digital inputs at V_{IN} = 3.4 V
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$|V_{Xi} - V_{Yj}|$ = V_{DD} - V_{SS} See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	3.0			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at V_{IN} = V_{SS} or $V_{DD;}$ $\overline{RESET}$ = V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym.	25°C		70°C		85°C		Units	Test Conditions
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
1	On-state Resistance V_{DD} =12 V V_{DD}=10V V_{DD}= 5V (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	V_{SS} = 0 V, V_{DC} = V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	V_{DD} = 12 V, V_{SS} = 0, V_{DC} = V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance- V_{DC} is the external DC offset at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi})=-3 dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2 Vpp sinewave; R_L = 1 kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2 Vpp sinewave f = 1 kHz; R_L= 1 kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA}= 2Vpp sinewave f = 1 kHz; R_L = 1 kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA} = 2Vpp sinewave f = 10 MHz; R_L = 75 Ω.
				-90		dB	V_{INA} = 2Vpp sinewave f = 10kHz; R_L = 600 Ω.
				-85		dB	V_{INA}=2Vpp sinewave f = 10 kHz; R_L = 1 kΩ.
				-80		dB	V_{INA} = 2Vpp sinewave f = 1 kHz; R_L = 10 kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L = 1 kΩ; C_L = 50 pF

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

AC Electrical Characteristics† - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for $\overline{\text{CS}}$, DATA, $\overline{\text{STROBE}}$, Address)	CX_{talk}		30		mVpp	V_{IN}=3V+V_{DC} squarewave; R_{IN}=1 kΩ, R_L=1 kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1 MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to $\overline{\text{STROBE}}$	t_{DS}	10			ns	R_L= 1 kΩ, C_L= 50 pF ¿Å
5	Hold Time DATA to $\overline{\text{STROBE}}$	t_{DH}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
6	Setup Time Address to $\overline{\text{STROBE}}$	t_{AS}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
7	Hold Time Address to $\overline{\text{STROBE}}$	t_{AH}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
8	Setup Time $\overline{\text{CS}}$ to $\overline{\text{STROBE}}$	t_{CSS}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
9	Hold Time $\overline{\text{CS}}$ to $\overline{\text{STROBE}}$	t_{CSH}	10			ns	R_L= 1 kΩ, C_L= 50 pF ¿Å
10	$\overline{\text{STROBE}}$ Pulse Width	t_{SPW}	20			ns	R_L= 1 kΩ, C_L= 50 pF ¿Å
11	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	40			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
12	$\overline{\text{STROBE}}$ to Switch Status Delay	t_S		40	100	ns	R_L= 1 kΩ, C_L=50 pF Å¿
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L= 1 kΩ, C_L= 50 pF Å¿
14	$\overline{\text{RESET}}$ to Switch Status Delay	t_R		35	100	ns	R_L= 1 kΩ, C_L= 50 pF ¿Å

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5 ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Å¿Refer to Appendix, Fig. A.7 for test circuit.

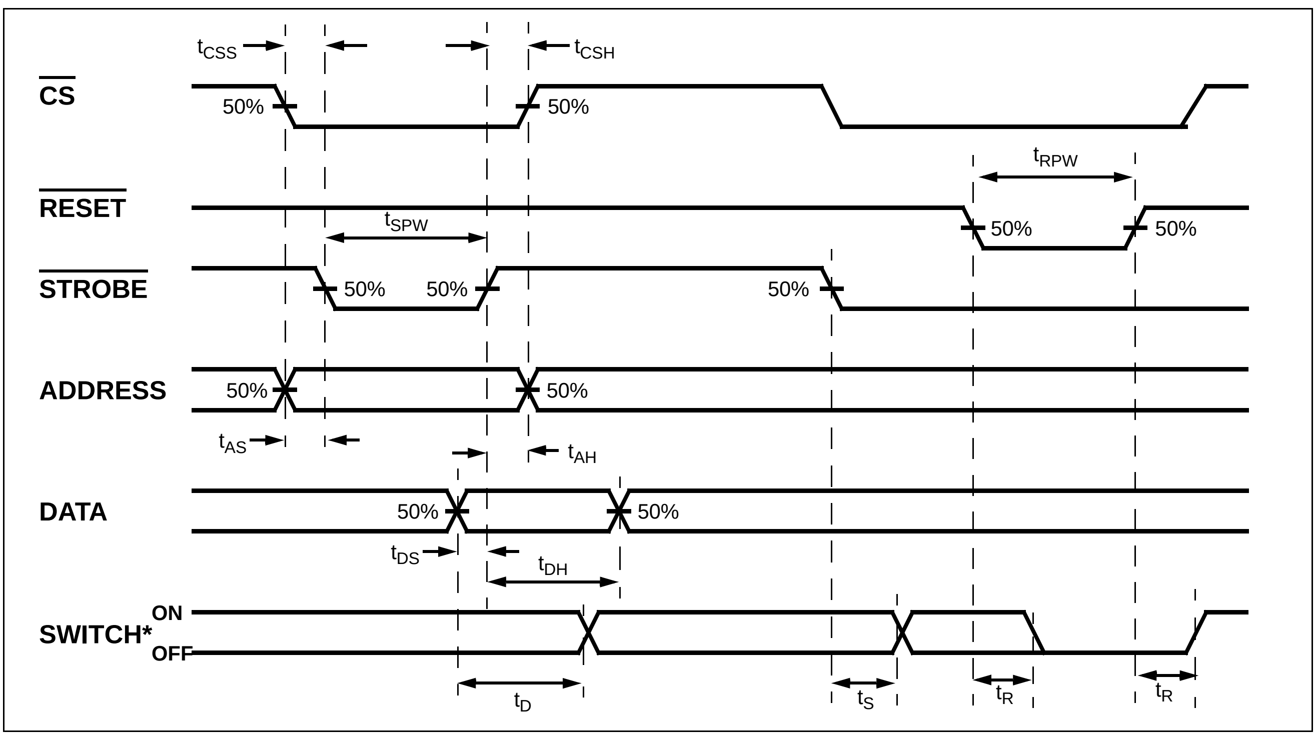

Figure 3 - Control Memory Timing Diagram

* See Appendix, Fig. A.7 for switching waveform

AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0	0	0	0	0	0	X0 Y0	1	0	0	0	0	0	X0 Y4
0	0	0	0	0	1	X1 Y0	1	0	0	0	0	1	X1 Y4
0	0	0	0	1	0	X2 Y0	1	0	0	0	1	0	X2 Y4
0	0	0	0	1	1	X3 Y0	1	0	0	0	1	1	X3 Y4
0	0	0	1	0	0	X4 Y0	1	0	0	1	0	0	X4 Y4
0	0	0	1	0	1	X5 Y0	1	0	0	1	0	1	X5 Y4
0	0	0	1	1	0	X6 Y0	1	0	0	1	1	0	X6 Y4
0	0	0	1	1	1	X7 Y0	1	0	0	1	1	1	X7 Y4
0	0	1	0	0	0	X0 Y1	1	0	1	0	0	0	X0 Y5
0	0	1	0	0	1	X1 Y1	1	0	1	0	0	1	X1 Y5
0	0	1	0	1	0	X2 Y1	1	0	1	0	1	0	X2 Y5
0	0	1	0	1	1	X3 Y1	1	0	1	0	1	1	X3 Y5
0	0	1	1	0	0	X4 Y1	1	0	1	1	0	0	X4 Y5
0	0	1	1	0	1	X5 Y1	1	0	1	1	0	1	X5 Y5
0	0	1	1	1	0	X6 Y1	1	0	1	1	1	0	X6 Y5
0	0	1	1	1	1	X7 Y1	1	0	1	1	1	1	X7 Y5
0	1	0	0	0	0	X0 Y2	1	1	0	0	0	0	X0 Y6
0	1	0	0	0	1	X1 Y2	1	1	0	0	0	1	X1 Y6
0	1	0	0	1	0	X2 Y2	1	1	0	0	1	0	X2 Y6
0	1	0	0	1	1	X3 Y2	1	1	0	0	1	1	X3 Y6
0	1	0	1	0	0	X4 Y2	1	1	0	1	0	0	X4 Y6
0	1	0	1	0	1	X5 Y2	1	1	0	1	0	1	X5 Y6
0	1	0	1	1	0	X6 Y2	1	1	0	1	1	0	X6 Y6
0	1	0	1	1	1	X7 Y2	1	1	0	1	1	1	X7 Y6
0	1	1	0	0	0	X0 Y3	1	1	1	0	0	0	X0 Y7
0	1	1	0	0	1	X1 Y3	1	1	1	0	0	1	X1 Y7
0	1	1	0	1	0	X2 Y3	1	1	1	0	1	0	X2 Y7
0	1	1	0	1	1	X3 Y3	1	1	1	0	1	1	X3 Y7
0	1	1	1	0	0	X4 Y3	1	1	1	1	0	0	X4 Y7
0	1	1	1	0	1	X5 Y3	1	1	1	1	0	1	X5 Y7
0	1	1	1	1	0	X6 Y3	1	1	1	1	1	0	X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table

MT8809

ISO-CMOS 8x8 Analog Switch Array

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- Short setup and hold times
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- 12 Vpp analog signal capability
- R_{ON} 65 Ω max. @ V_{DD} = 12 V, 25°C
- $\Delta R_{ON} \leq 10\ \Omega$ @ V_{DD} = 12 V, 25C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology
- Internal pull-up resistor for $\overline{\text{RESET}}$ pin

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

MT8809AE	28 Pin PDIP	Tubes
MT8809AP	28 Pin PLCC	Tubes
MT8809APR	28 Pin PLCC	Tape & Reel
MT8809AP1	28 Pin PLCC*	Tubes
MT8809APR1	28 Pin PLCC*	Tape & Reel
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* Pb Free Matte Tin

-40°C to +85°C

Description

The Zarlink MT8809 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select ($\overline{\text{CS}}$) allows the crosspoint array to be cascaded for matrix expansion.

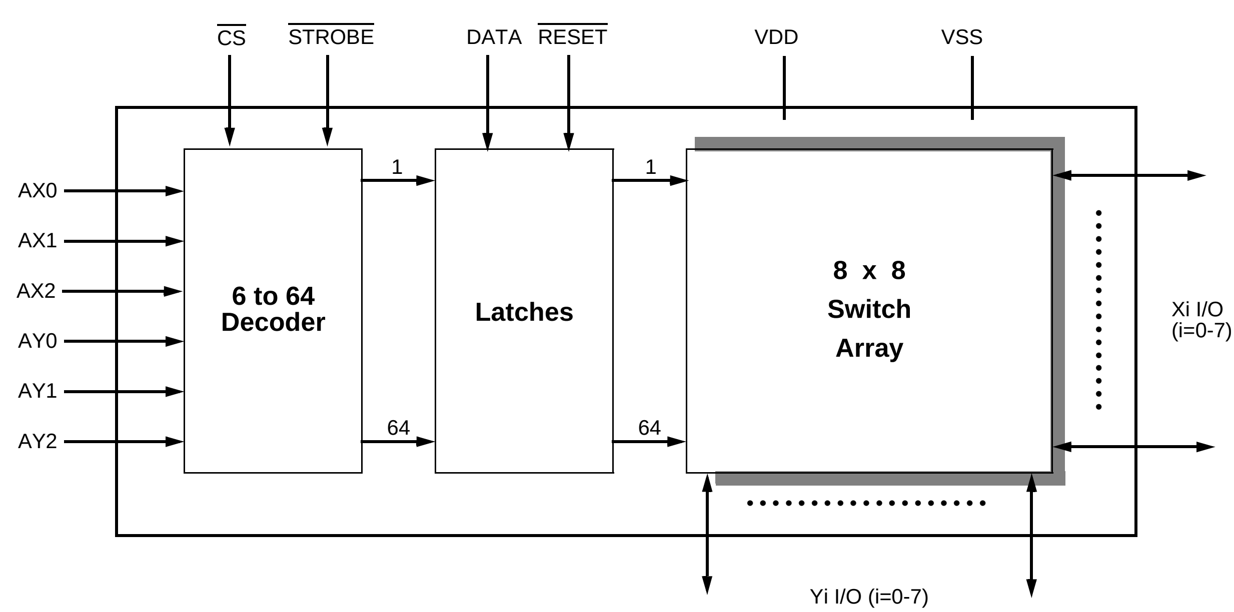

Figure 1 - Functional Block Diagram

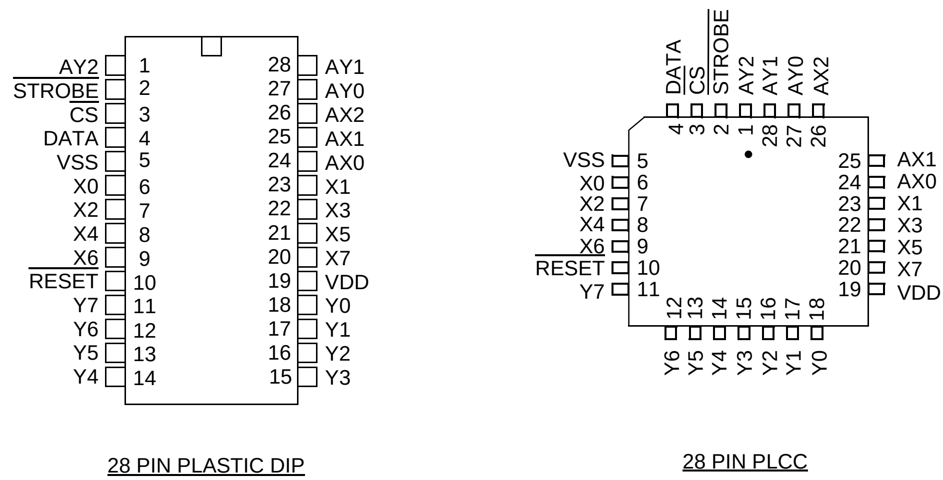

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input)**.
2	$\overline{\text{STROBE}}$	**STROBE (Input):** enables function selected by address and data. Address must be stable before $\overline{\text{STROBE}}$ goes low and DATA must be stable on the rising edge of $\overline{\text{STROBE}}$. Active Low.
3	$\overline{\text{CS}}$	**Chip Select (Input):** this is used to select the device. Active Low.
4	DATA	**DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	V_{SS}	**Ground Reference.**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	$\overline{\text{RESET}}$	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of $\overline{\text{CS}}$. A 100 kΩ internal pull-up resistor is also provided. This can be used in conjunction with a 0.1 µF capacitor (connected to the $\overline{\text{RESET}}$ pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	**Y7 - Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array.
19	V_{DD}	**Positive Power Supply.**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	**AX0 - AX2 Address Lines (Inputs)**.
27, 28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs)**.

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The MT8809 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the $\overline{CS}$ (Chip Select) and $\overline{STROBE}$ inputs are low and are latched on the rising edge of $\overline{STROBE}$. A logical “1” written into a memory cell turns the corresponding crosspoint switch on and a logical “0” turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical “0” on the $\overline{RESET}$ input will asynchronously return all memory locations to logical “0” turning off all crosspoint switches regardless of whether $\overline{CS}$ is high or low.

Address Decode

The six address inputs along with the $\overline{STROBE}$ and $\overline{CS}$ (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, $\overline{RESET}$ must be high and $\overline{CS}$ must go low while the address and data are set up. Then the $\overline{STROBE}$ input is set low and then high causing the data to be latched. The data can be changed while $\overline{STROBE}$ is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of $\overline{STROBE}$ in order for correct data to be written to the latch.

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter		Symbol	Min.	Max.	Units
1	Supply Voltage		V_{DD} V_{SS}	-0.3 -0.3	15.0 V_{DD}+0.3	V V
2	Analog Input Voltage		V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D		0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to V_{SS} = 0 V, V_{DD} = 12 V unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at V_{IN} = V_{SS} V_{DD} except $\overline{\text{RESET}}$ = V_{DD}.
				120	400	μA	All digital inputs at V_{IN} = V_{SS} or V_{DD} except $\overline{\text{RESET}}$ = V_{SS}.
				0.5	1.6	mA	All digital inputs at V_{IN} = 2.4 V, V_{DD} = 5.0 V
				5	15	mA	All digital inputs at V_{IN} = 3.4 V
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi} - V_{Yj}\rvert = V_{DD} - V_{SS}$ See Appendix, Fig. A.1
3	Input Logic “0” level	V_{IL}			0.8	V	
4	Input Logic “1” level	V_{IH}	3.0			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at V_{IN} = V_{SS} or V_{DD}; $\overline{\text{RESET}}$ = V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym.	25°C		70°C		85°C		Units	Test Conditions
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
1	On-state V_{DD} =12 V Resistance V_{DD}=10V V_{DD}= 5V (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	V_{SS} = 0 V,V_{DC} = V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	V_{DD} = 12 V, V_{SS} = 0, V_{DC} = V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance- V_{DC} is the external DC offset at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi})=-3 dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2 Vpp sinewave; R_L = 1 kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2 Vpp sinewave f = 1 kHz; R_L= 1 kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA}= 2Vpp sinewave f = 1 kHz; R_L = 1 kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA} = 2Vpp sinewave f = 10 MHz; R_L = 75 Ω.
				-90		dB	V_{INA} = 2Vpp sinewave f = 10kHz; R_L = 600 Ω.
				-85		dB	V_{INA}=2Vpp sinewave f = 10 kHz; R_L = 1 kΩ.
				-80		dB	V_{INA} = 2Vpp sinewave f = 1 kHz; R_L = 10 kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L = 1 kΩ; C_L = 50 pF

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

AC Electrical Characteristics† - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins.
Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for $\overline{\text{CS}}$, DATA, $\overline{\text{STROBE}}$, Address)	CX_{talk}		30		mVpp	V_{IN}=3V+V_{DC} squarewave; R_{IN}=1 kΩ, R_L=1 kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1 MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to $\overline{\text{STROBE}}$	t_{DS}	10			ns	R_L= 1 kΩ, C_L= 50 pF ¿ Å
5	Hold Time DATA to $\overline{\text{STROBE}}$	t_{DH}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
6	Setup Time Address to $\overline{\text{STROBE}}$	t_{AS}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
7	Hold Time Address to $\overline{\text{STROBE}}$	t_{AH}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
8	Setup Time $\overline{\text{CS}}$ to $\overline{\text{STROBE}}$	t_{CSS}	10			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
9	Hold Time $\overline{\text{CS}}$ to $\overline{\text{STROBE}}$	t_{CSH}	10			ns	R_L= 1 kΩ, C_L= 50 pF ¿Å
10	$\overline{\text{STROBE}}$ Pulse Width	t_{SPW}	20			ns	R_L= 1 kΩ, C_L= 50 pF ¿Å
11	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	40			ns	R_L= 1 kΩ, C_L= 50 pF Å¿
12	$\overline{\text{STROBE}}$ to Switch Status Delay	t_S		40	100	ns	R_L= 1 kΩ, C_L=50 pF Å¿
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L= 1 kΩ, C_L= 50 pF Å¿
14	$\overline{\text{RESET}}$ to Switch Status Delay	t_R		35	100	ns	R_L= 1 kΩ, C_L= 50 pF ¿Å

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5 ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Å¿Refer to Appendix, Fig. A.7 for test circuit.

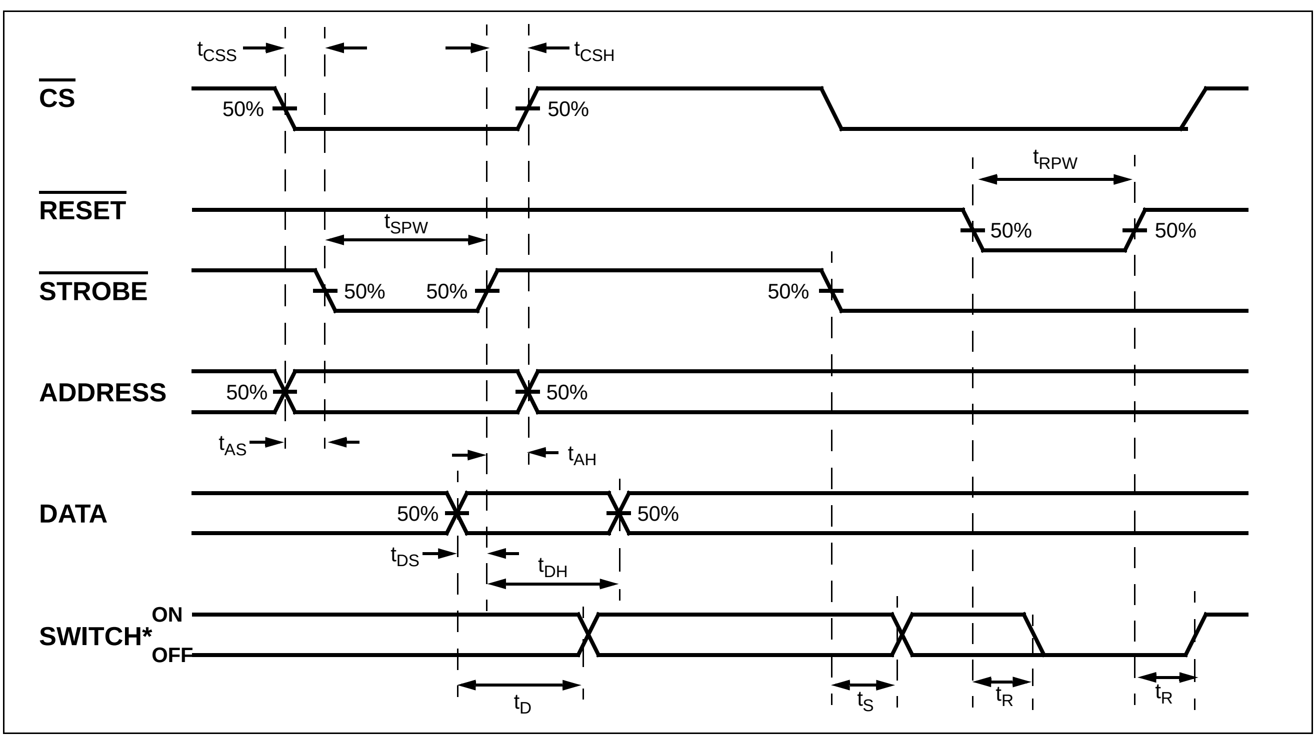
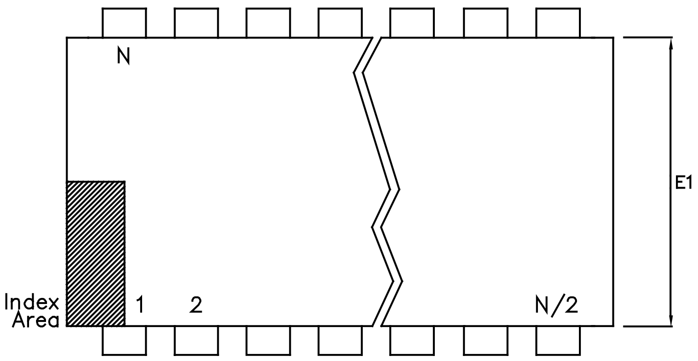


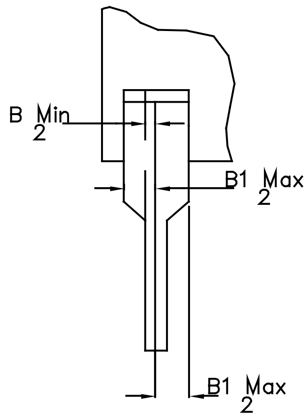
Figure 3 - Control Memory Timing Diagram

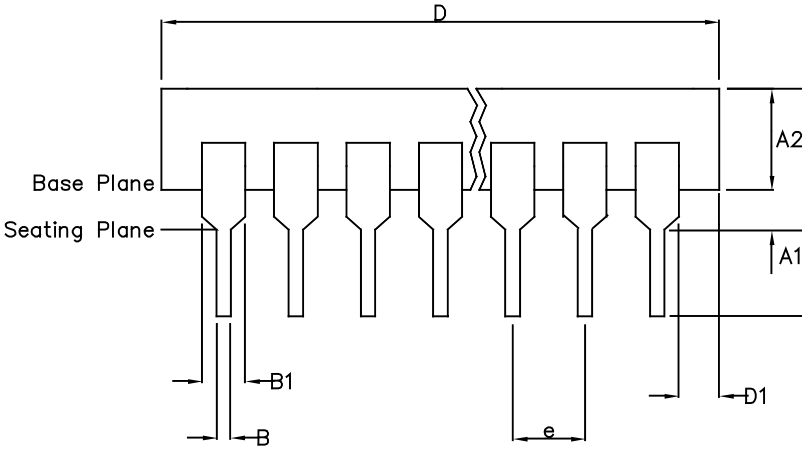
* See Appendix, Fig. A.7 for switching waveform

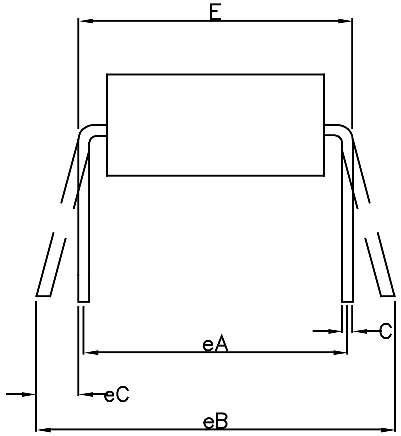
AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0	0	0	0	0	0	X0 Y0	1	0	0	0	0	0	X0 Y4
0	0	0	0	0	1	X1 Y0	1	0	0	0	0	1	X1 Y4
0	0	0	0	1	0	X2 Y0	1	0	0	0	1	0	X2 Y4
0	0	0	0	1	1	X3 Y0	1	0	0	0	1	1	X3 Y4
0	0	0	1	0	0	X4 Y0	1	0	0	1	0	0	X4 Y4
0	0	0	1	0	1	X5 Y0	1	0	0	1	0	1	X5 Y4
0	0	0	1	1	0	X6 Y0	1	0	0	1	1	0	X6 Y4
0	0	0	1	1	1	X7 Y0	1	0	0	1	1	1	X7 Y4
0	0	1	0	0	0	X0 Y1	1	0	1	0	0	0	X0 Y5
0	0	1	0	0	1	X1 Y1	1	0	1	0	0	1	X1 Y5
0	0	1	0	1	0	X2 Y1	1	0	1	0	1	0	X2 Y5
0	0	1	0	1	1	X3 Y1	1	0	1	0	1	1	X3 Y5
0	0	1	1	0	0	X4 Y1	1	0	1	1	0	0	X4 Y5
0	0	1	1	0	1	X5 Y1	1	0	1	1	0	1	X5 Y5
0	0	1	1	1	0	X6 Y1	1	0	1	1	1	0	X6 Y5
0	0	1	1	1	1	X7 Y1	1	0	1	1	1	1	X7 Y5
0	1	0	0	0	0	X0 Y2	1	1	0	0	0	0	X0 Y6
0	1	0	0	0	1	X1 Y2	1	1	0	0	0	1	X1 Y6
0	1	0	0	1	0	X2 Y2	1	1	0	0	1	0	X2 Y6
0	1	0	0	1	1	X3 Y2	1	1	0	0	1	1	X3 Y6
0	1	0	1	0	0	X4 Y2	1	1	0	1	0	0	X4 Y6
0	1	0	1	0	1	X5 Y2	1	1	0	1	0	1	X5 Y6
0	1	0	1	1	0	X6 Y2	1	1	0	1	1	0	X6 Y6
0	1	0	1	1	1	X7 Y2	1	1	0	1	1	1	X7 Y6
0	1	1	0	0	0	X0 Y3	1	1	1	0	0	0	X0 Y7
0	1	1	0	0	1	X1 Y3	1	1	1	0	0	1	X1 Y7
0	1	1	0	1	0	X2 Y3	1	1	1	0	1	0	X2 Y7
0	1	1	0	1	1	X3 Y3	1	1	1	0	1	1	X3 Y7
0	1	1	1	0	0	X4 Y3	1	1	1	1	0	0	X4 Y7
0	1	1	1	0	1	X5 Y3	1	1	1	1	0	1	X5 Y7
0	1	1	1	1	0	X6 Y3	1	1	1	1	1	0	X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	4
ACN	7010	203532	213102	CDCA
DATE	20Apr95	25Nov97	15Jul02	02Dec05
APPRD.				

ZARLINK SEMICONDUCTOR

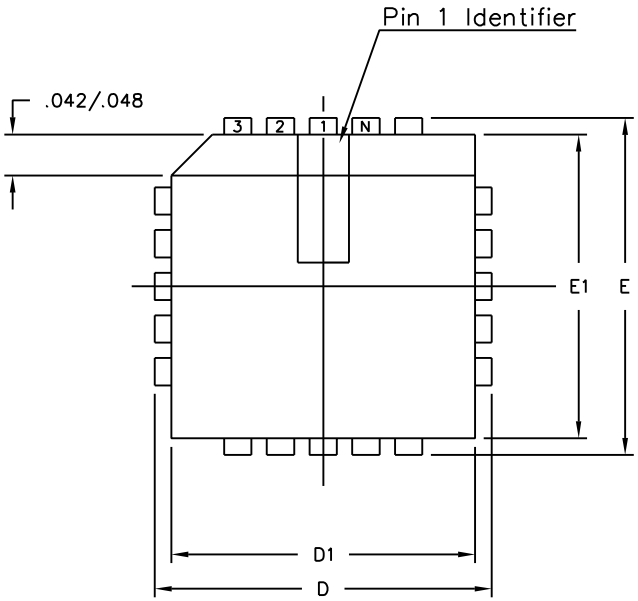
Package Code DA

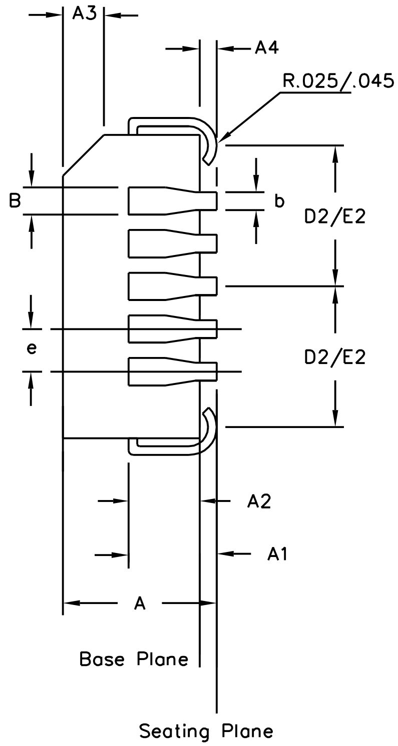
Previous package codes

DP / E

Package Outline for 28 lead 600mils PDIP

GPD00072





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code QA

Previous package codes

HP / P

Package Outline for 28 lead PLCC

GPD00002

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