88X2242

Integrated Quad-port Multi-speed Ethernet Transceiver with Electronic Dispersion Compensation Technology

Datasheet – Public

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Integrated Quad-port Multi-speed Ethernet Transceiver with Electronic Dispersion Compensation Technology

Datasheet – Public

PRODUCT OVERVIEW

The Marvell® 88X2242 transceiver is a fully integrated single chip solution providing end-to-end data transmission over fiber-optic networks as well as Twinax copper links. It is a 4-port device that performs all physical layer functions associated with 10GBASE-R, and 1000BASE-X. In addition the device supports 1 port of XAUI, and 40GBASE-R4.

The Electronic Dispersion Compensation (EDC) engine delivers high-speed bi-directional point-to-point full-duplex data transmission at 10.3 Gbps per port over a variety of media. The performance of the engine can be reduced to save power in fiber-optic applications that does not require EDC.

The line side interface supports 4 ports of 10GBASE-R, 1000BASE-X, and 1 port of 40GBASE-R4. The line side interface also supports Clause 73 AP Auto-Negotiation.

The host side interface supports 4 ports of 10GBASE-R, RXAUI, 1000BASE-X, and 2 ports of 40GBASE-R4, and XAUI. Any port from the host side can be attached to any port on the line side as long as the speeds match.

Internal registers can be accessed via an MDIO/MDC serial management interface which is compliant with the IEEE 802.3 specification (Clause 45). The MDC frequency supported is up to 25 MHz. The 88X2242 is manufactured in a 19 mm x 19 mm 324-pin FCBGA package.

Features

- 40GBASE-R4 (KR4 and CR4), 10GBASE-R, and 1000BASE-X support on the line interface
- EDC meets SFF-8431 requirements (SFP+MSA)
- MMF compensation exceeding 220m of OM1, OM2, and OM3 fibers
- SFF 8431 requirements are supported
- SMF CD/PMD compensation exceeding 80km
- 40GBASE-R4, 10GBASE-R, RXAUI, XAUI, 1000BASE-X support on the host interface
- Transmitter adjustable signal level and pre-emphasis
- IEEE 802.3 local/remote fault monitoring at SFP/SFP+ interface
- Built-in generators and checkers
- Programmable inversion on all differential signals
- Power saving modes
- Global multi-status interrupt pin
- Per-port TWSI for SFP IDPROM access (NOTE: SSCL clock stretching is not supported)
- Near and far-end loopbacks
- Supports IEEE-1149.1 and 1149.6 JTAG

Applications

- High-density line card SFP+ interfacing
- SFP+ modules, 10GSFP+Cu direct attach cables
- 1G SFP modules
- Switch to switch bridging

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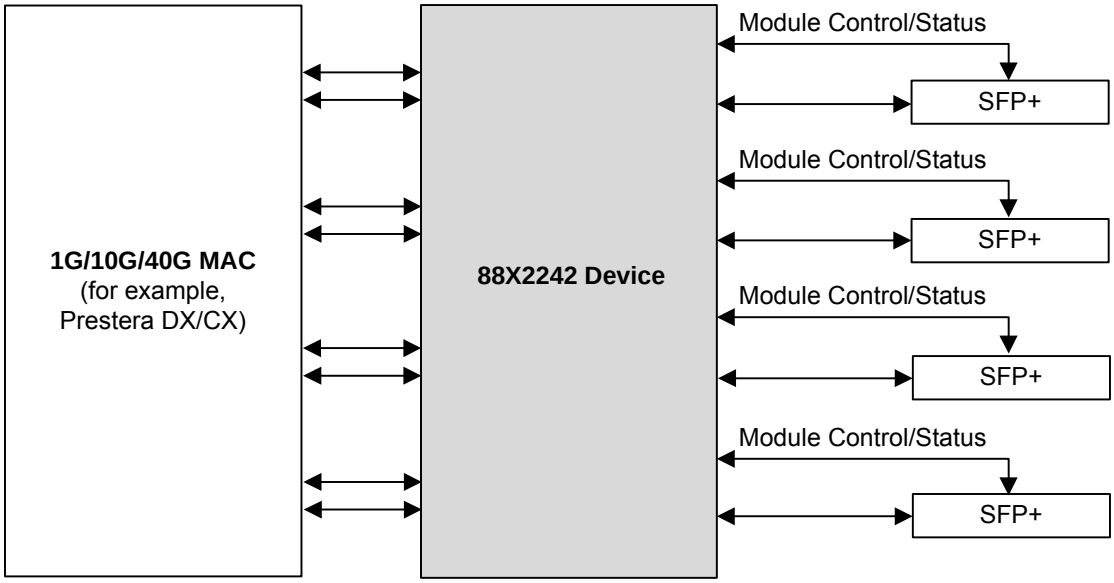
Figure 1: 88X2242 Application Diagram



MAC Interface

4 Port – 1000BASE-X
4 Port – 10GBASE-R
4 Port – RXAUI
2 Port – 40GBASE-R4
2 Port – XAUI

Media Interface

4 Port – 1000BASE-X
4 Port – 10GBASE-R
1 Port – 40GBASE-R4

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1 General Device Description

The line side and host side support various modes of operation for end-to-end data transmission over multi-mode fiber, single mode fiber, and Twinax copper cables. The DSP engine overcomes the impairments of the fiber cable, optical front end, and electrical interconnect.

Registers can be accessed by the host through standard clause 45 MDC/MDIO.

The device operates from a 1.0V digital core voltage and a 1.5V analog voltage. The digital I/O signals can operate at 1.5V, 1.8V, 2.5V, and 3.3V.

Figure 2 shows a block diagram of the 88X2242 device.

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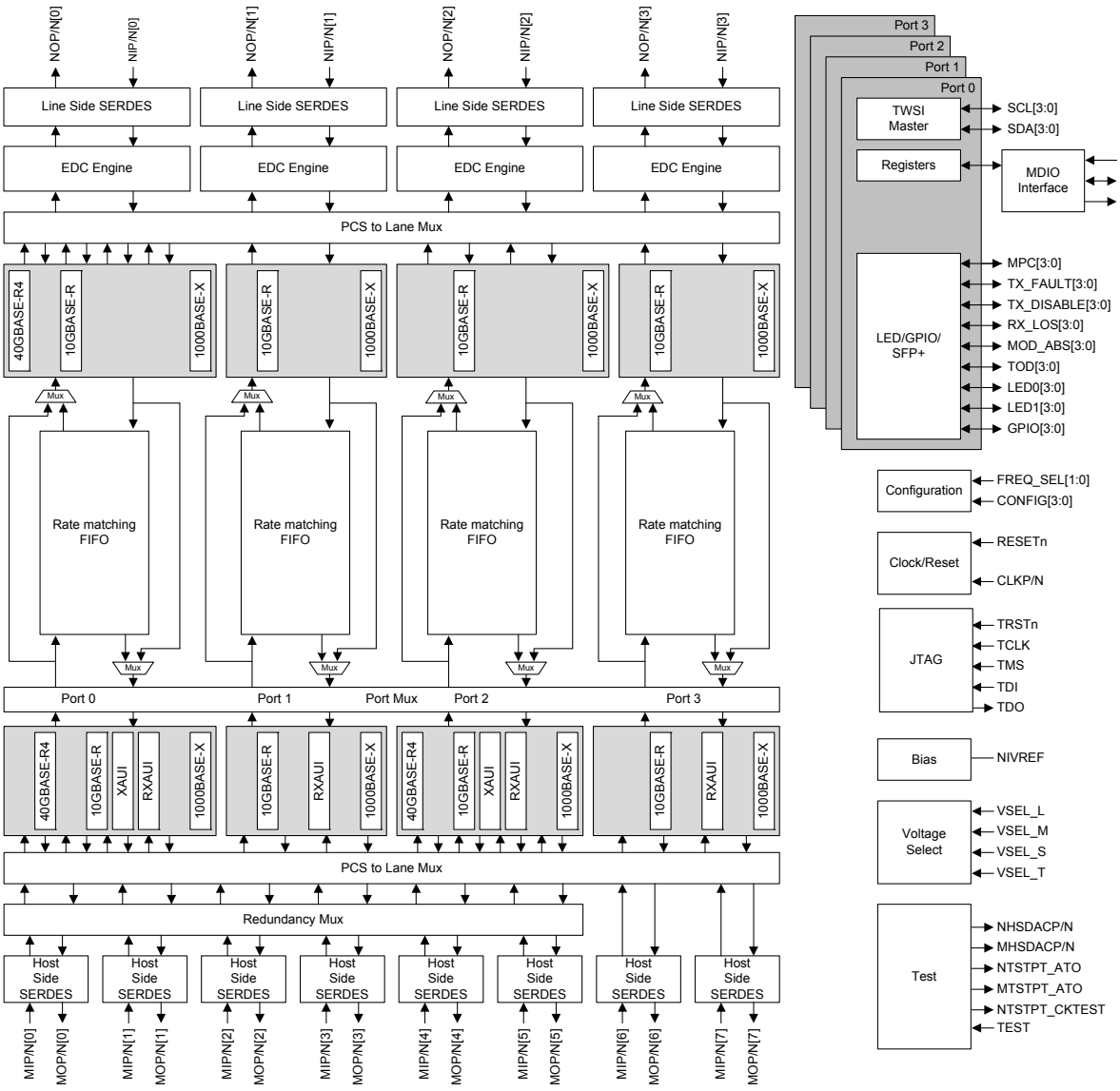
Figure 2: 88X2242 Device Functional Block Diagram



2 Signal Description

This section includes information on the following topics:

- Section 2.1, 88X2242 BGA Package
- Section 2.2, Pin Description
- Section 2.3, 88X2242 Pin Assignments
- Section 2.4, 88X2242 Device Pin Assignment List

2.1 88X2242 BGA Package

Note

Due to the large number of pins, the FCBGA package is depicted graphically over 2 facing pages. For pin 1 location, see Figure 52 on page 281.

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Figure 3: 88X2242 BGA Package, (Top Left View)

	1	2	3	4	5	6	7	8	9	
A	VSS	LED0[3]	VSS	WAN_CLKP	WAN_CLKN	NHSDACP	AVSS_N	NOP[0]	AVSS_N	A
B	LED1[3]	CONFIG[3]	TOD[3]	AVSS_N	AVSS_N	NHSDACN	AVSS_N	NON[0]	AVSS_N	B
C	LED1[2]	CONFIG[2]	TOD[2]	AVSS_N	AVSS_N	AVSS_N	NIP[0]	AVSS_N	NIP[1]	C
D	LED0[2]	VSS	GPIO[3]	VSEL_L	VDDOL	AVDD15_N	NIN[0]	AVDD15_N	NIN[1]	D
E	LED1[1]	CONFIG[1]	GPIO[2]	TOD[1]	VSSOL	NTSTPT_ ATO	AVSS_N	AVDD15_N	AVSS_N	E
F	LED0[1]	CONFIG[0]	GPIO[1]	TOD[0]	VDDOL	VSS	NIVREF	NTSTPT_ CKTEST	AVDD11_N	F
G	LED1[0]	VSS	GPIO[0]	VSSOL	VSSOL	DVDD	VSS	DVDD	VSS	G
H	LED0[0]	TDO	TRSTn	VDDOL	VDDOL	VSS	DVDD	VSS	DVDD	H
J	TDI	TCK	TMS	VSSOL	VSSOL	DVDD	VSS	DVDD	VSS	J
K	RCLK0	RCLK1	TEST	VSEL_T	VDDOT	VSS	DVDD	VSS	DVDD	K
L	VSS	RESETn	FREQ_ SEL[0]	FREQ_ SEL[1]	VSSOT	VSSOT	VSS	DVDD	VSS	L
M	CLKP	DNC	DNC	DNC	DVDD	VSS	DVDD	VSS	DVDD	M
N	CLKN	AVDD10_M	AVDD10_M	AVDD10_M	AVSS_M	AVDD10_M	AVDD10_M	AVDD10_M	MTSTPT_ ATO	N
P	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	P
R	MIP[0]	AVDD15_M	MIP[1]	AVDD15_M	MIP[2]	AVDD15_M	MIP[3]	AVDD15_M	AVSS_M	R
T	MIN[0]	AVSS_M	MIN[1]	AVSS_M	MIN[2]	AVSS_M	MIN[3]	AVSS_M	AVSS_M	T
U	AVSS_M	MOP[0]	AVSS_M	MOP[1]	AVSS_M	MOP[2]	AVSS_M	MOP[3]	AVSS_M	U
V	AVSS_M	MON[0]	AVSS_M	MON[1]	AVSS_M	MON[2]	AVSS_M	MON[3]	AVSS_M	V
	1	2	3	4	5	6	7	8	9	

Figure 4: 88X2242 BGA Package, (Top Right View)

	10	11	12	13	14	15	16	17	18	
A	NOP[1]	AVSS_N	NOP[2]	AVSS_N	NOP[3]	AVSS_N	LOS[3]	MOD_ ABS[3]	VSS	A
B	NON[1]	AVSS_N	NON[2]	AVSS_N	NON[3]	AVSS_N	MPC[3]	TX_ DISABLE[3]	SCL[3]	B
C	AVSS_N	NIP[2]	AVSS_N	NIP[3]	AVSS_N	VDDOS	LOS[2]	TX_ FAULT[3]	SDA[3]	C
D	AVDD15_N	NIN[2]	AVDD15_N	NIN[3]	AVDD15_N	MPC[2]	VSSOS	MOD_ ABS[2]	SCL[2]	D
E	AVDD15_N	AVSS_N	AVDD15_N	AVSS_N	AVDD15_N	VDDOS	VSEL_S	TX_ DISABLE[2]	SDA[2]	E
F	AVDD11_N	AVDD11_N	AVDD11_N	AVDD11_N	VSS	LOS[1]	VSSOS	TX_ FAULT[2]	SCL[1]	F
G	DVDD	VSS	DVDD	VSS	DVDD	VDDOS	MPC[1]	MOD_ ABS[1]	SDA[1]	G
H	VSS	DVDD	VSS	DVDD	VSS	LOS[0]	VSSOS	TX_ DISABLE[1]	SCL[0]	H
J	DVDD	VSS	DVDD	VSS	DVDD	MOD_ ABS[0]	MPC[0]	TX_ FAULT[1]	SDA[0]	J
K	VSS	DVDD	VSS	DVDD	VSS	TX_ FAULT[0]	TX_ DISABLE[0]	INTn	MDC	K
L	DVDD	VSS	DVDD	VSS	DVDD	VSSOM	VDDOM	VSEL_M	MDIO	L
M	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VSS	VSS	M
N	MHSDACN	MHSDACP	AVDD10_M	AVDD10_M	AVDD10_M	AVSS_M	AVDD10_M	AVDD10_M	AVDD10_M	N
P	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	AVDD15_M	AVSS_M	P
R	AVSS_M	AVDD15_M	MIP[4]	AVDD15_M	MIP[5]	AVDD15_M	MIP[6]	AVDD15_M	MIP[7]	R
T	AVSS_M	AVSS_M	MIN[4]	AVSS_M	MIN[5]	AVSS_M	MIN[6]	AVSS_M	MIN[7]	T
U	AVSS_M	MOP[4]	AVSS_M	MOP[5]	AVSS_M	MOP[6]	AVSS_M	MOP[7]	AVSS_M	U
V	AVSS_M	MON[4]	AVSS_M	MON[5]	AVSS_M	MON[6]	AVSS_M	MON[7]	AVSS_M	V
	10	11	12	13	14	15	16	17	18	

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2.2 Pin Description

Table 1: Pin Type Definitions

Pin Type	Definition
A	Analog
D	Open drain output
DNC	Do Not Connect
G	Ground
I	Input only
I/O	Input and output
O	Output only
P	Power

2.3 88X2242 Pin Assignments

Table 2: Line Side Interface

Package Pin #	Pin Name	Pin Type	Description
C13 C11 C9 C7	NIP[3] NIP[2] NIP[1] NIP[0]	Analog Input	SFI Input Positive
D13 D11 D9 D7	NIN[3] NIN[2] NIN[1] NIN[0]	Analog Input	SFI Input Negative
A14 A12 A10 A8	NOP[3] NOP[2] NOP[1] NOP[0]	Analog Output	SFI Output Positive
B14 B12 B10 B8	NON[3] NON[2] NON[1] NON[0]	Analog Output	SFI Output Negative

Table 3: Host Side Interface

Package Pin #	Pin Name	Pin Type	Description
R18 R16 R14 R12 R7 R5 R3 R1	MIP[7] MIP[6] MIP[5] MIP[4] MIP[3] MIP[2] MIP[1] MIP[0]	Analog Input	XFI Input Positive
T18 T16 T14 T12 T7 T5 T3 T1	MIN[7] MIN[6] MIN[5] MIN[4] MIN[3] MIN[2] MIN[1] MIN[0]	Analog Input	XFI Input Negative
U17 U15 U13 U11 U8 U6 U4 U2	MOP[7] MOP[6] MOP[5] MOP[4] MOP[3] MOP[2] MOP[1] MOP[0]	Analog Output	XFI Output Positive
V17 V15 V13 V11 V8 V6 V4 V2	MON[7] MON[6] MON[5] MON[4] MON[3] MON[2] MON[1] MON[0]	Analog Output	XFI Output Negative

Table 4: Clocking and Reference

Package Pin #	Pin Name	Pin Type	Description
M1	CLKP	Analog Input	Reference Clock Positive and Negative. REF_CLK is 156.25 MHz. See Section 7.8, Reference Clock, on page 275 for details.
N1	CLKN	Analog Input	
A4	WAN_CLKP	Analog Input	Reserved. For test purposes only Terminate both pins using 50 Ω to ground.
A5	WAN_CLKN	Analog Input	
F7	NIVREF	Analog Output	Resistor Reference. External 3.65 kΩ ±1% resistor connection to VSS is required for this pin.
K1	RCLK0	Digital Output	Reserved. For test purposes only. Leave floating.
K2	RCLK1	Digital Output	Reserved. For test purposes only. Leave floating.

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Table 5: Configuration and Reset

Package Pin #	Pin Name	Pin Type	Description
D4	VSEL_L	Analog Input	VDDOL Voltage Select 0 - VDDOL = 2.5V/3.3V 1 - VDDOL = 1.2V/1.8V
L17	VSEL_M	Analog Input	VDDOM Voltage Select 0 - VDDOM = 2.5V/3.3V 1 - VDDOM = 1.2V/1.8V
E16	VSEL_S	Analog Input	VDDOS Voltage Select 0 - VDDOS = 2.5V/3.3V 1 - VDDOS = 1.2V/1.8V
K4	VSEL_T	Analog Input	VDDOT Voltage Select 0 - VDDOT = 2.5V/3.3V 1 - VDDOT = 1.2V/1.8V
B2 C2 E2 F2	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	Digital Input	Hardware Configuration
L4 L3	FREQ_SEL[1] FREQ_SEL[0]	Digital Input	CLKP/N Frequency 00 = 156.25 MHz 01 = Reserved 10 = Reserved 11 = Reserved
L2	RESETn	Digital Input	Hardware Reset, 0 = Reset

Table 6: Management Interface

Package Pin #	Pin Name	Pin Type	Description
K18	MDC	Digital Input	Management Interface Clock
L18	MDIO	Digital Input/Output	Management Interface Data Bi-directional management interface data transferred synchronously to the MDC. This pin requires a pull-up resistor in a range from 1.5k to 10 kΩ.
K17	INTn	Digital Output	Interrupt

Table 7: SFP+, GPIO, LED

Package Pin #	Pin Name	Pin Type	Description
B16 D15 G16 J16	MPC[3] MPC[2] MPC[1] MPC[0]	Digital Input/Output	Managed Power Control, LED2, GPIO
B3 C3 E4 F4	TOD[3] TOD[2] TOD[1] TOD[0]	Digital Input/Output	TOD, LED3, GPIO

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Table 7: SFP+, GPIO, LED (Continued)

Package Pin #	Pin Name	Pin Type	Description
B17 E17 H17 K16	TX_DISABLE[3] TX_DISABLE[2] TX_DISABLE[1] TX_DISABLE[0]	Digital Input/Output	SFP Transmit Disable, LED4, GPIO
A17 D17 G17 J15	MOD_ABS[3] MOD_ABS[2] MOD_ABS[1] MOD_ABS[0]	Digital Input/Output	SFP Module Attached, GPIO
C17 F17 J17 K15	TX_FAULT[3] TX_FAULT[2] TX_FAULT[1] TX_FAULT[0]	Digital Input/Output	SFP Transmit Fault, GPIO
A16 C16 F15 H15	LOS[3] LOS[2] LOS[1] LOS[0]	Digital Input/Output	SFP Loss Of Signal, GPIO
B18 D18 F18 H18	SCL[3] SCL[2] SCL[1] SCL[0]	Digital Input/Output	Two Wire Serial Interface Clock, GPIO
C18 E18 G18 J18	SDA[3] SDA[2] SDA[1] SDA[0]	Digital Input/Output	Two Wire Serial Interface Data, GPIO
D3 E3 F3 G3	GPIO[3] GPIO[2] GPIO[1] GPIO[0]	Digital Input/Output	GPIO
A2 D1 F1 H1	LED0[3] LED0[2] LED0[1] LED0[0]	Digital Input/Output	LED0, GPIO
B1 C1 E1 G1	LED1[3] LED1[2] LED1[1] LED1[0]	Digital Input/Output	LED1, GPIO

Table 8: JTAG

Package Pin #	Pin Name	Pin Type	Description
J1	TDI	Digital Input	JTAG Test In
H2	TDO	Digital Output	JTAG Test Out
J3	TMS	Digital Input	JTAG Test Control

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Table 8: JTAG (Continued)

Package Pin #	Pin Name	Pin Type	Description
J2	TCK	Digital Input	JTAG Test Clock
H3	TRSTn	Digital Input	JTAG Test Reset For normal operation, TRSTn should be pulled low with a 4.7 kΩ pull-down resistor.

Table 9: Test

Package Pin #	Pin Name	Pin Type	Description
K3	TEST	Digital Input	Test Enable, 1 = Test For normal operation, TEST pin should be connected to ground.
A6	NHSDACP	Analog Output	Analog AC Test Positive Port N For normal operation, NHSDACP must be left unconnected.
B6	NHSDACN	Analog Output	Analog AC Test Negative Port N For normal operation, NHSDACN must be left unconnected.
N11	MHSDACP	Analog Output	Analog AC Test Positive Port M For normal operation, MHSDACP must be left unconnected.
N10	MHSDACN	Analog Output	Analog AC Test Negative Port M For normal operation, MHSDACN must be left unconnected.
E6	NTSTPT_ATO	Analog Output	Analog DC Test Point Port N For normal operation, NTSTPT_ATO must be left unconnected.
N9	MTSTPT_ATO	Analog Output	Analog DC Test Point Port M For normal operation, MTSTPT_ATO must be left unconnected.
F8	NTSTPT_CKTEST	Analog Output	Analog Clock Test Point Port N For normal operation, NTSTPT_CKTEST must be left unconnected.

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Table 10: Power and Ground

Package Pin #	Pin Name	Pin Type	Description
G6 G8 G10 G12 G14 H7 H9 H11 H13 J6 J8 J10 J12 J14 K7 K9 K11 K13 L8 L10 L12 L14 M5 M7 M9 M11 M13 M15	DVDD	Digital Power	1.0V Digital Core Power
P2 P4 P6 P8 P11 P13 P15 P17 R2 R4 R6 R8 R11 R13 R15 R17	AVDD15_M	Analog Power	1.5V Analog Core Power

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Table 10: Power and Ground (Continued)

Package Pin #	Pin Name	Pin Type	Description
D6 D8 D10 D12 D14 E8 E10 E12 E14	AVDD15_N	Analog Power	1.5V Analog Core Power
N2 N3 N4 N6 N7 N8 N12 N13 N14 N16 N17 N18	AVDD10_M	Analog Power	1.0V Analog Core Power
F9 F10 F11 F12 F13	AVDD11_N	Analog Power	1.1V Analog Core Power
D5 F5 H4 H5	VDDOL	I/O Power	I/O Power: CONFIG[4:0], TOD[3:0],GPIO[3:0], LED0[3:0], LED1[3:0]
I16	VDDOM	I/O Power	I/O Power: MDC, MDIO
C15 E15 G15	VDDOS	I/O Power	I/O Power: LOS[3:0], MOD_ABS[3:0], MPC[3:0], SCL[3:0], SDA[3:0], TX_DISABLE[3:0], TX_FAULT[3:0], INTn,
K5	VDDOT	I/O Power	I/O Power: RESETn, TEST, TDI, TDO, TMS, TCK, TRSTn, FREQ_SEL[1:0]

Table 10: Power and Ground (Continued)

Package Pin #	Pin Name	Pin Type	Description
A7 A9 A11 A13 A15 B4 B5 B7 B9 B11 B13 B15 C4 C5 C6 C8 C10 C12 C14 E7 E9 E11 E13	AVSS_N	Ground	Ground
N5 N15 P1 P3 P5 P7 P9 P10 P12 P14 P16 P18 R9 R10 T2 T4 T6 T8 T9 T10 T11 T13 T15 T17 U1 U3 U5 U7 U9	AVSS_M	Ground	Ground

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Table 10: Power and Ground (Continued)

Package Pin #	Pin Name	Pin Type	Description
U10 U12 U14 U16 U18 V1 V3 V5 V7 V9 V10 V12 V14 V16 V18	AVSS_M (cont.)	Ground	Ground
E5 G4 G5 J4 J5	VSSOL	Ground	Ground
L15	VSSOM	Ground	Ground
D16 F16 H16	VSSOS	Ground	Ground

Table 10: Power and Ground (Continued)

Package Pin #	Pin Name	Pin Type	Description
L5 L6	VSSOT	Ground	Ground
A1 A3 A18 D2 F6 F14 G2 G7 G9 G11 G13 H6 H8 H10 H12 H14 J7 J9 J11 J13 K6 K8 K10 K12 K14 L1 L7 L9 L11 L13 M6 M8 M10 M12 M14 M16 M17 M18	VSS	Ground	Ground

Table 11: No Connect

Package Pin #	Pin Name	Pin Type	Description
M2 M3 M4	DNC	DNC	Do not connect. Keep floating.

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2.4 88X2242 Device Pin Assignment List

Table 12: 88X2242 Pin List—Alphabetical by Signal Name

Pin Number	Pin Name	Pin Number	Pin Name
N2	AVDD10_M	R15	AVDD15_M
N3	AVDD10_M	R17	AVDD15_M
N4	AVDD10_M	D6	AVDD15_N
N6	AVDD10_M	D8	AVDD15_N
N7	AVDD10_M	D10	AVDD15_N
N8	AVDD10_M	D12	AVDD15_N
N12	AVDD10_M	D14	AVDD15_N
N13	AVDD10_M	E8	AVDD15_N
N14	AVDD10_M	E10	AVDD15_N
N16	AVDD10_M	E12	AVDD15_N
N17	AVDD10_M	E14	AVDD15_N
N18	AVDD10_M	N5	AVSS_M
F9	AVDD11_N	N15	AVSS_M
F10	AVDD11_N	P1	AVSS_M
F11	AVDD11_N	P3	AVSS_M
F12	AVDD11_N	P5	AVSS_M
F13	AVDD11_N	P7	AVSS_M
P2	AVDD15_M	P9	AVSS_M
P4	AVDD15_M	P10	AVSS_M
P6	AVDD15_M	P12	AVSS_M
P8	AVDD15_M	P14	AVSS_M
P11	AVDD15_M	P16	AVSS_M
P13	AVDD15_M	P18	AVSS_M
P15	AVDD15_M	R9	AVSS_M
P17	AVDD15_M	R10	AVSS_M
R2	AVDD15_M	T2	AVSS_M
R4	AVDD15_M	T4	AVSS_M
R6	AVDD15_M	T6	AVSS_M
R8	AVDD15_M	T8	AVSS_M
R11	AVDD15_M	T9	AVSS_M
R13	AVDD15_M	T10	AVSS_M

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Table 12: 88X2242 Pin List—Alphabetical by Signal Name (Continued)

Pin Number	Pin Name	Pin Number	Pin Name
T11	AVSS_M	B11	AVSS_N
T13	AVSS_M	B13	AVSS_N
T15	AVSS_M	B15	AVSS_N
T17	AVSS_M	C4	AVSS_N
U1	AVSS_M	C5	AVSS_N
U3	AVSS_M	C6	AVSS_N
U5	AVSS_M	C8	AVSS_N
U7	AVSS_M	C10	AVSS_N
U9	AVSS_M	C12	AVSS_N
U10	AVSS_M	C14	AVSS_N
U12	AVSS_M	E7	AVSS_N
U14	AVSS_M	E9	AVSS_N
U16	AVSS_M	E11	AVSS_N
U18	AVSS_M	E13	AVSS_N
V1	AVSS_M	N1	CLKN
V3	AVSS_M	M1	CLKP
V5	AVSS_M	F2	CONFIG[0]
V7	AVSS_M	E2	CONFIG[1]
V9	AVSS_M	C2	CONFIG[2]
V10	AVSS_M	B2	CONFIG[3]
V12	AVSS_M	M2	DNC
V14	AVSS_M	M3	DNC
V16	AVSS_M	M4	DNC
V18	AVSS_M	G6	DVDD
A7	AVSS_N	G8	DVDD
A9	AVSS_N	G10	DVDD
A11	AVSS_N	G12	DVDD
A13	AVSS_N	G14	DVDD
A15	AVSS_N	H7	DVDD
B4	AVSS_N	H9	DVDD
B5	AVSS_N	H11	DVDD
B7	AVSS_N	H13	DVDD
B9	AVSS_N	J6	DVDD

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Table 12: 88X2242 Pin List—Alphabetical by Signal Name (Continued)

Pin Number	Pin Name	Pin Number	Pin Name
J8	DVDD	H15	LOS[0]
J10	DVDD	F15	LOS[1]
J12	DVDD	C16	LOS[2]
J14	DVDD	A16	LOS[3]
K7	DVDD	K18	MDC
K9	DVDD	L18	MDIO
K11	DVDD	N10	MHSDACN
K13	DVDD	N11	MHSDACP
L8	DVDD	T1	MIN[0]
L10	DVDD	T3	MIN[1]
L12	DVDD	T5	MIN[2]
L14	DVDD	T7	MIN[3]
M5	DVDD	T12	MIN[4]
M7	DVDD	T14	MIN[5]
M9	DVDD	T16	MIN[6]
M11	DVDD	T18	MIN[7]
M13	DVDD	R1	MIP[0]
M15	DVDD	R3	MIP[1]
L3	FREQ_SEL[0]	R5	MIP[2]
L4	FREQ_SEL[1]	R7	MIP[3]
G3	GPIO[0]	R12	MIP[4]
F3	GPIO[1]	R14	MIP[5]
E3	GPIO[2]	R16	MIP[6]
D3	GPIO[3]	R18	MIP[7]
K17	INTn	J15	MOD_ABS[0]
H1	LED0[0]	G17	MOD_ABS[1]
F1	LED0[1]	D17	MOD_ABS[2]
D1	LED0[2]	A17	MOD_ABS[3]
A2	LED0[3]	V2	MON[0]
G1	LED1[0]	V4	MON[1]
E1	LED1[1]	V6	MON[2]
C1	LED1[2]	V8	MON[3]
B1	LED1[3]	V11	MON[4]

Table 12: 88X2242 Pin List—Alphabetical by Signal Name (Continued)

Pin Number	Pin Name	Pin Number	Pin Name
V13	MON[5]	A12	NOP[2]
V15	MON[6]	A14	NOP[3]
V17	MON[7]	E6	NTSTPT_ATO
U2	MOP[0]	F8	NTSTPT_CKTEST
U4	MOP[1]	K1	RCLK0
U6	MOP[2]	K2	RCLK1
U8	MOP[3]	L2	RESETn
U11	MOP[4]	H18	SCL[0]
U13	MOP[5]	F18	SCL[1]
U15	MOP[6]	D18	SCL[2]
U17	MOP[7]	B18	SCL[3]
J16	MPC[0]	J18	SDA[0]
G16	MPC[1]	G18	SDA[1]
D15	MPC[2]	E18	SDA[2]
B16	MPC[3]	C18	SDA[3]
N9	MTSTPT_ATO	J2	TCK
B6	NHSDACN	J1	TDI
A6	NHSDACP	H2	TDO
D7	NIN[0]	K3	TEST
D9	NIN[1]	J3	TMS
D11	NIN[2]	F4	TOD[0]
D13	NIN[3]	E4	TOD[1]
C7	NIP[0]	C3	TOD[2]
C9	NIP[1]	B3	TOD[3]
C11	NIP[2]	H3	TRSTn
C13	NIP[3]	K16	TX_DISABLE[0]
F7	NIVREF	H17	TX_DISABLE[1]
B8	NON[0]	E17	TX_DISABLE[2]
B10	NON[1]	B17	TX_DISABLE[3]
B12	NON[2]	K15	TX_FAULT[0]
B14	NON[3]	J17	TX_FAULT[1]
A8	NOP[0]	F17	TX_FAULT[2]
A10	NOP[1]	C17	TX_FAULT[3]

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Table 12: 88X2242 Pin List—Alphabetical by Signal Name (Continued)

Pin Number	Pin Name
D5	VDDOL
F5	VDDOL
H4	VDDOL
H5	VDDOL
L16	VDDOM
C15	VDDOS
E15	VDDOS
G15	VDDOS
K5	VDDOT
D4	VSEL_L
L17	VSEL_M
E16	VSEL_S
K4	VSEL_T
A1	VSS
A3	VSS
A18	VSS
D2	VSS
F6	VSS
F14	VSS
G2	VSS
G7	VSS
G9	VSS
G11	VSS
G13	VSS
H6	VSS
H8	VSS
H10	VSS
H12	VSS
H14	VSS
J7	VSS
J9	VSS
J11	VSS
J13	VSS

Pin Number	Pin Name
K6	VSS
K8	VSS
K10	VSS
K12	VSS
K14	VSS
L1	VSS
L7	VSS
L9	VSS
L11	VSS
L13	VSS
M6	VSS
M8	VSS
M10	VSS
M12	VSS
M14	VSS
M16	VSS
M17	VSS
M18	VSS
E5	VSSOL
G4	VSSOL
G5	VSSOL
J4	VSSOL
J5	VSSOL
L15	VSSOM
D16	VSSOS
F16	VSSOS
H16	VSSOS
L5	VSSOT
L6	VSSOT
A5	WAN_CLKN
A4	WAN_CLKP

3 Chip Level Functional Description

This section includes information on the following topics:

- Section 3.1, Datapath
- Section 3.2, Resets
- Section 3.3, Hardware Configuration
- Section 3.4, MDC/MDIO Register Access
- Section 3.5, GPIO and SFP+
- Section 3.6, LED
- Section 3.7, EEPROM Bridging and Polling
- Section 3.8, Interrupt
- Section 3.9, Power Management
- Section 3.10, IEEE1149.1 and 1149.6 Controller
- Section 3.11, Reference Clock
- Section 3.12, Power Supplies

This section describes the chip level functionality. Section 4, Line Side Description, on page 87 and Section 5, Host Side Description, on page 97 describe the individual units in more detail.

3.1 Datapath

Figure 5 illustrates the datapath of both devices. This section examines the multiplexing in more detail.

3.1.1 Cross Port Multiplexing

Although the device supports multiple different PCS with the various PCS attached to 1 or more physical lanes, the device can be fundamentally viewed as 4 ports on the line side and 4 ports on the host side. Any of the 4 ports on the line side can be attached to any of the 4 ports on the host side by programming the cross port multiplexer. Note that the association between the line and host side can be independently programmed for ingress and egress paths and need not be the same for both directions. It is also possible for data received on one port of the line (host) side to be transmitted out on more than 1 port of the host (line) side.

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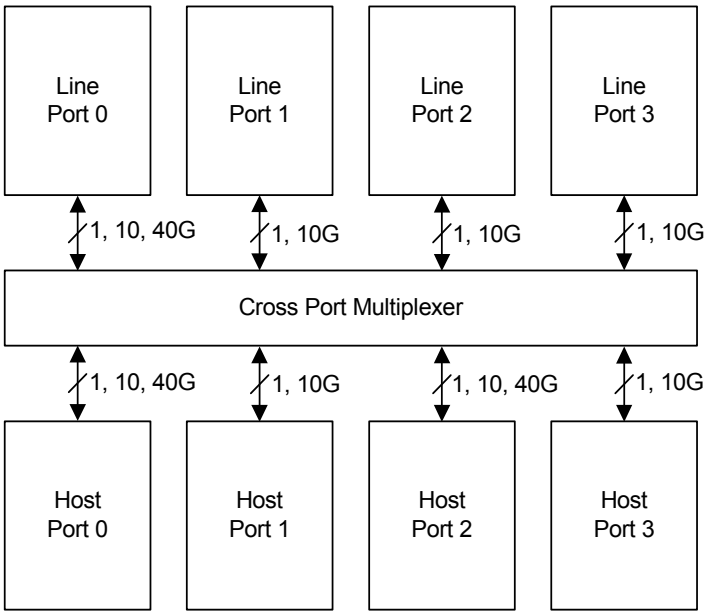
Figure 5: Cross Port Multiplexing



The attached ports must run at the same speed (though the PCS types can be different). All speeds are not supported on all ports. It is the user's responsibility to ensure that the cross port multiplexing is set correctly.

Registers 31.F400 bits 3:0, 7:4, 11:8, and 15:12 control which port on the host side attaches to ports 0, 1, 2, and 3 of the line side port transmitter, respectively.

0000 = power down the line side port transmitter

0001 = output idles on the line side port transmitter

1000 = attach to host side port 0

1001 = attach to host side port 1

1010 = attach to host side port 2

1011 = attach to host side port 3

Registers 31.F401 bits 3:0, 7:4, 11:8, and 15:12 control which port on the line side attaches to ports 0, 1, 2, and 3 of the host side port transmitter, respectively.

0000 = power down the host side port transmitter

0001 = output idles on the host side port transmitter

1000 = attach to line side port 0

1001 = attach to line side port 1

1010 = attach to line side port 2

1011 = attach to line side port 3

Registers 31.F400 and 31.F401 are global registers and can be accessed from Port 0 PHYAD.

3.1.2 PCS Operational Mode and Lane Attachment

Each port supports multiple PCS. Not all PCS are supported by all ports. Only 1 PCS can be enabled at a time for a given port, but different PCS can be selected among the different ports.

Since some PCS requires more lanes to operate than others, it is possible that conflicts can exist (for example, Port 0 in XAUI mode conflicting with the other 3 ports). In case of conflict, the lower numbered port will have the higher priority over the higher numbered port. The PCS on the port with the lower priority that has conflict will be automatically powered down.

Register 31.F002.14:8 and 31.F002.6:0 selects the PCS type for the line and host side respectively. Not all PCS type are available for each port. Table 13 lists out which PCS is available for each port.Table 14 and Table 15 list the pin mappings for PCS modes for the line and host interfaces.Table 16 and Table 17 list the valid 7 bit setting for registers 31.F002.14:8 and 31.F002.6:0.

Table 13: PCS Availability by Port

PCS Type	Line Side Port N				Host Side Port M			
	N0	N1	N2	N3	M0	M1	M2	M3
40GBASE-R4	X				X		X	
10GBASE-R	X	X	X	X	X	X	X	X
XAUI					X		X	
RXAUI					X	X	X	X
1000BASE-X	X	X	X	X	X	X	X	X

Table 14: Pin Mapping for PCS Modes - Line Interface

	Name	#	Name	#	Name	#	Name	#
	Lane 0 Pin		Lane 1 Pin		Lane 2 Pin		Lane 3 Pin	
Rx	NIP[0]	C7	NIP[1]	C9	NIP[2]	C11	NIP[3]	C13
	NIN[0]	D7	NIN[1]	D9	NIN[2]	D11	NIN[3]	D13
Tx	NOP[0]	A8	NOP[1]	A10	NOP[2]	A12	NOP[3]	A14
	NON[0]	B8	NON[1]	B10	NON[2]	B12	NON[3]	B14
PCS Modes	10GBASE-R Port 0		10GBASE-R Port 1		10GBASE-R Port 2		10GBASE-R Port 3	
	1000BASE-X Port 0		1000BASE-X Port 1		1000BASE-X Port 2		1000BASE-X Port 3	
	40GBASE-R4 Port 0							

Table 15: Pin Mapping for PCS Modes - Host Interface

	Name	#	Name	#	Name	#	Name	#
	Lane 0 Pin		Lane 1 Pin		Lane 2 Pin		Lane 3 Pin	
Rx	MIP[0]	R1	MIP[1]	R3	MIP[2]	R5	MIP[3]	R7
	MIN[0]	T1	MIN[1]	T3	MIN[2]	T5	MIN[3]	T7

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Table 15: Pin Mapping for PCS Modes - Host Interface (Continued)

	Name	#	Name	#	Name	#	Name	#
Tx	MOP[0]	U2	MOP[1]	U4	MOP[2]	U6	MOP[3]	U8
	MON[0]	V2	MON[1]	V4	MON[2]	V6	MON[3]	V8
PCS Modes	10GBASE-R lane attachment mapping is based on 31.0xF402.9							
	10GBASE-R Port 0		10GBASE-R Port 1(1)		10GBASE-R Port 1(0)		10GBASE-R Port 3(1)	
	1000BASE-X lane attachment mapping is based on 31.0xF402.8							
	—		1000BASE-X Port 1(1)		1000BASE-X Port 1(0) 1000BASE-X Port 2(1)		1000BASE-X Port 3(1)	
	RXAUI lane attachment mapping is based on 31.0xF402.11							
	RXAUI Port 0				RXAUI Port 1(0) RXAUI Port 2(1)			
	XAUI Port 0							
	40GBASE-R4 Port 0							
	Lane 4 Pin		**Lane 5 Pin**		**Lane 6 Pin**		**Lane 7 Pin**	
Rx	MIP[4]	R12	MIP[5]	R14	MIP[6]	R16	MIP[7]	R18
	MIN[4]	T12	MIN[5]	T14	MIN[6]	T16	MIN[7]	T18
Tx	MOP[4]	U11	MOP[5]	U13	MOP[6]	U15	MOP[7]	U17
	MON[4]	V11	MON[5]	V13	MON[6]	V15	MON[7]	V17
PCS Modes	10GBASE-R lane attachment mapping is based on 31.0xF402.9							
	10GBASE-R Port 2(0)				10GBASE-R Port 3(0)			
	RXAUI lane attachment mapping is based on 31.0xF402.11							
	RXAUI Port 2				RXAUI Port 3			
	XAUI Port 2							
	40GBASE-R4 Port 2							

Table 16: Valid Settings - Line Side

31.F002.14:8	PCS	Auto-Negotiation
1110000	40GBASE-R4	N/A
1110001	10GBASE-R	N/A
1111010	1000BASE-X	Off
1111011		On
1111100	SGMII (System)	Off
1111101		On
1111110	SGMII (Media)	Off
1111111		On

Table 17: Valid Settings - Host Side

31.F002.6:0	PCS	Auto-Negotiation
1110000	40GBASE-R4	N/A
1110001	10GBASE-R	N/A

Table 17: Valid Settings - Host Side (Continued)

31.F002.6:0	PCS	Auto-Negotiation
1110010	RXAUI	N/A
1110011	XAUI	N/A
1110111	Reserved	N/A
1111010	1000BASE-X	Off
1111011		On
1111100	SGMII (System)	Off
1111101		On
1111110	SGMII (Media)	Off
1111111		On

Although the various lanes can support multiple speeds, there are limitations on which speed combinations can be supported across the various lanes simultaneously.

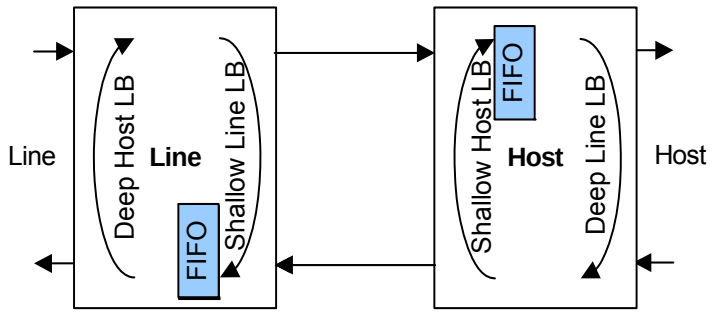
3.1.3 Loopback and Bypass

Figure 6 illustrates the possible loopback and bypass paths. Note that the cross port multiplexing is not shown in Figure 6.

For information, see the following sections:

- Line side loopbacks—Section 4.3, Loopback
- Host side loopbacks—Section 5.3, Loopback

Figure 6: 88X2242 Device Data Path



3.1.4 Frequency Compensation FIFOs

There are FIFOs in the PCS blocks to compensate the frequency offset between the host and line. The FIFO positions are illustrated in Figure 6. The FIFO depth can be set via register 3.F00C.15:14 for the Line side and register 4.F00C.15:14 for the Host side.

3.1.5 Host Side Lane Attachment

There are 8 physical lanes on the host side. All 8 physical lanes (Physical Lane 0-7) are mapped to 8 logical lanes (Logical Lane M0-7).

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The 1000BASE-X and 10GBASE-R may be attached to different logical lanes to facilitate connection to various different legacy switches. Register 31.F402 bits 11, 9, and 8 control which lanes attach to which PCS.

Table 18 shows which PCS are available and which lane attachments are possible.

Table 18: Host Side Line Muxing

Register	Function	Setting
31.F402.11	RXAUI Attachment	0 = Ports 0, 2 attached to logical lanes 0/1, 4/5 1 = Ports 0, 2 attached to logical lanes 0/1, 2/3
31.F402.9	10BASE-R Attachment	0 = Ports 0, 1, 2, 3 attached to logical lanes 0, 2, 4, 6 1 = Ports 0, 1, 2, 3 attached to logical lanes 0, 1, 2, 3
31.F402.8	1000BASE-X Attachment	0 = Ports 0, 1, 2, 3 attached to logical lanes 0, 2, 4, 6 1 = Ports 0, 1, 2, 3 attached to logical lanes 0, 1, 2, 3

Table 19: Physical Lane to PCS Mapping

Port	Lane								Comment
	0	1	2	3	4	5	6	7	
Port 0	40GBASE-R4								
	XAUI								
	RXAUI								
	10GBASE-R								
	1000BASE-X								
Port 1			RXAUI						
		10GBASE-R (1)	10GBASE-R (0)						31.F402.9 0 = Lane 2 1 = Lane 1
		1000BASE-X (1)	1000BASE-X (0)						31.F402.8 0 = Lane 2 1 = Lane 1
Port 2					40GBASE-R4				
					XAUI				
			RXAUI (1)		RXAUI (0)				Force to
			10GBASE-R (1)		10GBASE-R (0)				31.F402.9 0 = Lane 4 1 = Lane 2
			1000BASE-X (1)		1000BASE-X (0)				31.F402.8 0 = Lane 4 1 = Lane 2
Port 3							RXAUI		
				10GBASE-R (1)			10GBASE-R (0)		31.F402.9 0 = Lane 6 1 = Lane 3
				1000BASE-X (1)			1000BASE-X (0)		31.F402.8 0 = Lane 6 1 = Lane 3

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3.1.6 Polarity Inversion

The polarity of each lane can be independently inverted.

Registers 31.F406 bit 0 to 7 controls the polarity of MOP/N[0] to MOP/N[7] respectively.

Registers 31.F406 bit 8 to 15 controls the polarity of MIP/N[0] to MIP/N[7] respectively.

Registers 31.F407 bit 0 to 3 controls the polarity of NOP/N[0] to NOP/N[3] respectively.

Registers 31.F407 bit 8 to 11 controls the polarity of NIP/N[0] to NIP/N[3] respectively.

0 = Normal polarity

1 = Reverse polarity

3.2 Resets

A hardware reset (RESETn) resets the entire chip and initializes all the registers to their hardware reset default.

A software reset has a similar effect on the affected units as a hardware reset except all 'Retain' type of registers hold their value, and any previously written values in the 'Update' registers take effect.

To assert a host/line side port reset, set:

- 31.F003.15 to 1 for line side of the port
- 31.F003.7 to 1 for host side of the port

Refer to Section 4.5, Power Management, on page 92 for the line side PCS and PMA resets and Section 5.5, Power Management, on page 100 for the host side PCS and PMA resets.

To assert a global chip-level soft reset, set:

- 31.0xF404.15
- 31.0xF404.14

3.3 Hardware Configuration

After de-assertion of RESETn, the 88X2242 device will be hardware configured.

The 88X2242 device is configured through the CONFIG[3:0] pins.

Each CONFIG[3:0] pin is used to configure 2 bits. The 2-bit value is set depending on what is connected to the CONFIG pins soon after de-assertion of hardware reset. The 2-bit mapping is shown in Table 20.

Table 20: Two Bit Mapping

Pin	Bit 1,0
VSS	00
LED0[0]	01
LED1[0]	10
VDDO	11

The 2 bits for the CONFIG pin is mapped as shown in Table 21.

Table 21: Configuration Mapping

Pin	CONFIG Bit1	CONFIG Bit 0
CONFIG[0]	Must be 0	Must be 0
CONFIG[1]	PHYAD[3]	PHYAD[2]

Table 21: Configuration Mapping (Continued)

Pin	CONFIG Bit1	CONFIG Bit 0
CONFIG[2]	PDSTATE	PHYAD[4]
CONFIG[3]	Reserved Tie to 0	Reserved Tie to 0

Each bit in the configuration is defined as shown in Table 22.

Table 22: Configuration Definition

Bits	Definition	Register Affected
PHYAD[4:0]	PHY Address for port 0. Port n address is (PHYAD[4:2], 0,0) + n	None
PDSTATE	0 = Start In Power Up State 1 = Start In Power Down State	31.F400.15:0 31.F401.15:0 31.F403.7:0

The FREQ_SEL[1:0] must be set to 00. All other settings are reserved.

3.4 MDC/MDIO Register Access

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 clause 45. MDC is the management data clock input and, it can run from DC to a maximum rate of 25 MHz. At high, MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO does not require a pull-up resistor. If another open-drain device driving MDIO requires a pull-up resistor, it should drive or be pulled up to the same voltage value as the DVDDIO rail.

PHY address is configured during the hardware reset sequence. For more information on how to configure PHY addresses, see Section 3.3, Hardware Configuration, on page 49.

Typical read and write operations on the management interface are shown in Figure 7 and Figure 8. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 6, Register Description, on page 104.

Figure 7: Typical MDC/MDIO Read Operation

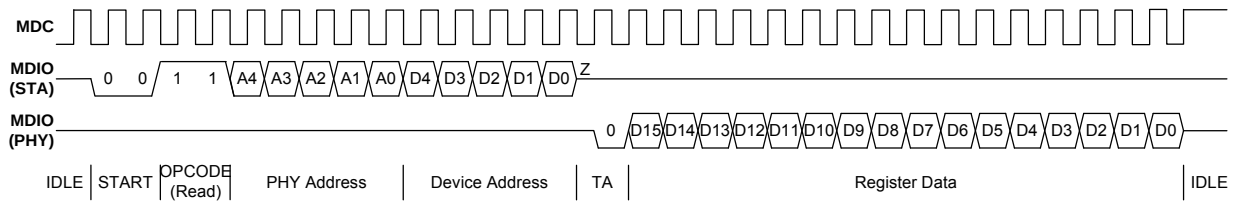

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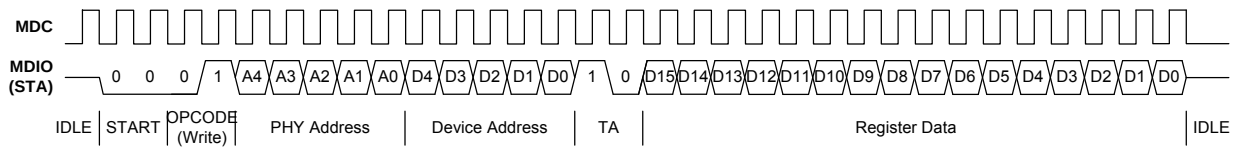
Figure 8: Typical MDC/MDIO Write Operation



3.4.1 Clause 45 MDIO Framing

The MDIO interface frame structure is compatible with Clause 22 such that the 2 management interfaces can co-exist on the same MDIO bus.

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 23.

Table 23: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

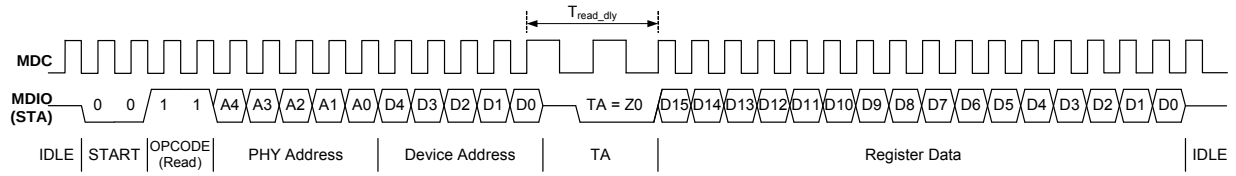
3.4.2 High-Speed MDC/MDIO Management Interface Protocol

In addition to supporting the typical MDC/MDIO protocol, the device has the capability to run MDC as fast as 40 MHz. Write operation can operate normally at this speed; however, for read operation, the MDC clock cycle must be slowed down for the TA period as shown in the Figure 9.

During read operations, the MDC clock must slow down so that the PHY has enough time to fetch the data. There are 2 scenarios. In 1 scenario, the MDIO has exclusive access to the internal register bus.

For timing details, see Table 407 on page 262.

Figure 9: 40 MHz MDC/MDIO Read Operation



3.5 GPIO and SFP+

The GPIO, LED, and TWSI functions share the same set of signal pins. Each pin can be individually programmed to operate in 1 of the 3 functions. The GPIO and TWSI functions can be combined to form the SFP+ digital interface. The pin mapping is summarized in Table 24.

Table 24: GPIO, LED, and TWSI Signal Mapping

Signal	GPIO	LED	TWSI	SFP+	Default Mode
MOD_ABS	MOD_ABS			Module Attached	GPIO Input
TX_FAULT	TX_FAULT			Transmit Fault	GPIO Input
RX_LOS	RX_LOS			Receive Loss of Signal	GPIO Input
GPIO	GPIO				GPIO Input
LED0	GPIO[4]	LED0			LED Function
LED1	GPIO[5]	LED1			LED Function
MPC	GPIO[6]	MPC		Module Power	GPIO Output Low
TOD	GPIO[7]	TOD			GPIO Input
TX_DISABLE	GPIO[8]	TX_DISABLED		Transmit Disable	GPIO Output High
SDA	GPIO[10]		TWSI Serial Data	TWSI Serial Data	TWSI
SCL	GPIO[11]		TWSI Clock	TWSI Clock	TWSI
	Bit 9 not used				

The GPIO function enables the pins listed in Table 24 to function as GPIO ports. Each pin can operate bi-directionally and can be individually configured. When operating as an output, these pins operate as open drain.

3.5.1 Enabling GPIO Functionality

The TX_DISABLED, TOD, MPC, LED1, and LED0 pins operates in the LED mode unless register 31.F016.4:3 is set to 01, and 31.F014.11, 31.F014.7, 31.F015.15, 31.F015.11, 31.F015.7, 31.F015.3 respectively are set to 1. Once set to 1, the LED pins can be controlled via the GPIO registers.

The SCL and SDA pins operate in the TWSI mode unless register 31.F016.15 and 31.F016.11 respectively are set to 1. Once set to 1, the SCL and SDA pins can be controlled via the GPIO registers.

The GPIO, RX_LOS, TX_FAULT, and MOD_ABS pins can always be controlled via the GPIO registers.

3.5.2 Controlling and Sensing

Register 31.F013 controls whether the GPIO pins are inputs or outputs. Each pin can be individually controlled.

Register 31.F012 allows the pins to be controlled and sensed.

When configured as input, a read to register 31.F012 will return the real-time sampled state of the pin at the time of the read. A write will write the output register but has no immediate effect on the pin since the pin is configured to be an input. The input is sampled once every 38.4 ns.

When configured as output, a read to register 31.F012 returns the value in the output register. A write writes the output register which in turn drives the state of the pin.

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Table 25: GPIO Data

Register	Function	Setting	Mode
31.F012.11	SCL Data	This bit has no effect unless register 31.F016.15 = 1. When 31.F013.11 = 0, a read to this register will reflect the state of the SCL pin, and a write will write the output register but will have no effect on the SCL pin. When 31.F013.11 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the SCL pin.	R/W
31.F012.10	SDA Data	This bit has no effect unless register 31.F016.11 = 1. When 31.F013.10 = 0, a read to this register will reflect the state of the SDA pin, and a write will write the output register but will have no effect on the SDA pin. When 31.F013.10 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the SDA pin.	R/W
31.F012.8	TX_DISABLED Data	This bit has no effect unless register 31.F016.3 = 1. When 31.F013.8 = 0, a read to this register will reflect the state of the TX_DISABLED pin, and a write will write the output register but will have no effect on the TX_DISABLED pin. When 31.F013.8 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the TX_DISABLED pin.	R/W
31.F012.7	TOD Data	This bit has no effect unless register 31.F015.15 = 1. When 31.F013.7 = 0, a read to this register will reflect the state of the TOD pin, and a write will write the output register but will have no effect on the TOD pin. When 31.F013.7 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the TOD pin.	R/W
31.F012.6	MPC Data	This bit has no effect unless register 31.F015.11 = 1. When 31.F013.6 = 0, a read to this register will reflect the state of the MPC pin, and a write will write the output register but will have no effect on the MPC pin. When 31.F013.6 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the MPC pin.	R/W
31.F012.5	LED1 Data	This bit has no effect unless register 31.F015.7 = 1. When 31.F013.5 = 0, a read to this register will reflect the state of the LED1 pin, and a write will write the output register but will have no effect on the LED1 pin. When 31.F013.5 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the LED1 pin.	R/W
31.F012.4	LED0 Data	This bit has no effect unless register 31.F015.3 = 1. When 31.F013.4 = 0, a read to this register will reflect the state of the LED0 pin, and a write will write the output register but will have no effect on the LED0 pin. When 31.F013.4 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the LED0 pin.	R/W

Table 25: GPIO Data (Continued)

Register	Function	Setting	Mode
31.F012.3	GPIO Data	When 31.F013.9 = 0, a read to this register will reflect the state of the GPIO pin, and a write will write the output register but will have no effect on the GPIO pin. When 31.F013.9 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the GPIO pin.	R/W
31.F012.2	RX_LOS Data	When 31.F013.2 = 0, a read to this register will reflect the state of the RX_LOS pin, and a write will write the output register but will have no effect on the RX_LOS pin. When 31.F013.2 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the RX_LOS pin.	R/W
31.F012.1	TX_FAULT Data	When 31.F013.1 = 0, a read to this register will reflect the state of the TX_FAULT pin, and a write will write the output register but will have no effect on the TX_FAULT pin. When 31.F013.1 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the TX_FAULT pin.	R/W
31.F012.0	MOD_ABS Data	When 31.F013.0 = 0, a read to this register will reflect the state of the MOD_ABS pin, and a write will write the output register but will have no effect on the MOD_ABS pin. When 31.F013.0 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and will drive the state of the MOD_ABS pin.	R/W

Table 26: GPIO Tristate Control

Register	Function	Setting	Mode
31.F013.11	SCL Output Enable	This bit has no effect unless register 31.F016.15 = 1. 0 = Input, 1 = Output	R/W
31.F013.10	SDA Output Enable	This bit has no effect unless register 31.F016.11 = 1. 0 = Input, 1 = Output	R/W
31.F013.8	TX_DISABLED Output Enable	This bit has no effect unless register 31.F016.3 = 1. 0 = Input, 1 = Output	R/W
31.F013.7	TOD Output Enable	This bit has no effect unless register 31.F015.15 = 1. 0 = Input, 1 = Output	R/W
31.F013.6	MPC Output Enable	This bit has no effect unless register 31.F015.11 = 1. 0 = Input, 1 = Output	R/W
31.F013.5	LED1 Output Enable	This bit has no effect unless register 31.F015.7 = 1. 0 = Input, 1 = Output	R/W
31.F013.4	LED0 Output Enable	This bit has no effect unless register 31.F015.3 = 1. 0 = Input, 1 = Output	R/W
31.F013.3	GPIO Output Enable	0 = Input, 1 = Output	R/W
31.F013.2	RX_LOS Output Enable	0 = Input, 1 = Output	R/W
31.F013.1	TX_FAULT Output Enable	0 = Input, 1 = Output	R/W
31.F013.0	MOD_ABS Output Enable	0 = Input, 1 = Output	R/W

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3.5.3 GPIO Interrupts

When the pins are configured as input, several types of interrupt events can be generated. Registers 31.F014, 31.F015, and 31.F016 allow each pin to be configured to generate interrupt on 1 of 5 types of events:

- Low Level
- High Level
- High to Low Transition
- Low to High Transition
- Transitions on Either Edge

The interrupt generation can also be disabled.

When an interrupt event is generated, it is latched high in register 31.F011. The register bits will remain high until read.

The INT pin can be asserted when interrupt events occur. Register 31.F010 sets the interrupt enable. Registers 31.F010 and 31.F011 are bitwise AND together. If the result is non-zero, the INT pin will assert.

If any of the following occur, no new interrupt events will be generated and reported in register 31.F011 for that particular pin:

- When a pin is set to output
- When TX_DISABLED, TOD, MPC, LED1, and LED0 are set to LED function instead of GPIO function
- When SCL and SDA are set to TWSI function instead of GPIO function

If a previous interrupt event occurred but is not read, the register will retain its value until read. In other words, if an interrupt event occurred while the pin is configured as an input, the interrupt status bit will be set. If subsequently the pin is set to an output, the interrupt status bit will remain set until it is read.

When changing a pin from output to input, an edge triggered event will not be generated on the transition. For example, if the pin is configured as an output and is driven low and there is a pull-up attached to the pin. Once the pin is configured as an input (to tri-state the pin), there will be a low to high transition. This low to high transition will not trigger an edge event. Subsequent transitions with the pin configured as input will trigger edge events.

See Table 27, Table 28, and Table 29 for information on GPIO interrupt enable, status, and type.

Table 27: GPIO Interrupt Enable

Register	Function	Setting	Mode
31.F010.11	SCL Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.10	SDA Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.8	TX_DISABLED Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.7	TOD Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.6	MPC Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.5	LED1 Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.4	LED0 Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.3	GPIO Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.2	RX_LOS Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.1	TX_FAULT Interrupt Enable	0 = Disable, 1 = Enable	R/W
31.F010.0	MOD_ABS Interrupt Enable	0 = Disable, 1 = Enable	R/W

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Table 28: GPIO Interrupt Status

Register	Function	Setting	Mode
31.F011.11	SCL Interrupt Status	This bit is not valid unless register 31.F016.15 = 1 and 31.F013.11 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.10	SDA Interrupt Status	This bit is not valid unless register 31.F016.11 = 1 and 31.F013.10 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.8	TX_DISABLED Interrupt Status	This bit is not valid unless register 31.F016.3 = 1 and 31.F013.8 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.7	TOD Interrupt Status	This bit is not valid unless register 31.F015.15 = 1 and 31.F013.7 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.6	MPC Interrupt Status	This bit is not valid unless register 31.F015.11 = 1 and 31.F013.6 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.5	LED1 Interrupt Status	This bit is not valid unless register 31.F015.7 = 1 and 31.F013.5 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.4	LED0 Interrupt Status	This bit is not valid unless register 31.F015.3 = 1 and 31.F013.4 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.3	GPIO Interrupt Status	This bit is not valid unless register 31.F013.3 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred=	RO, LH
31.F011.2	RX_LOS Interrupt Status	This bit is not valid unless register 31.F013.2 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.1	TX_FAULT Interrupt Status	This bit is not valid unless register 31.F013.1 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH
31.F011.0	MOD_ABS Interrupt Status	This bit is not valid unless register 31.F013.0 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred	RO, LH

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Table 29: GPIO Interrupt Type

Register	Function	Setting	Mode
31.F014.14:12	GPIO Select	Interrupt is effective only when 31.F013.3 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low	R/W
31.F014.11	RX_LOS Function	0 = RX_LOS is used as Signal Detect Function. 1 = RX_LOS is used for GPIO Function.	R/W
31.F014.10:8	RX_LOS Select	Interrupt is effective only when 31.F013.2 = 0. Same as 31.F014.14:12	R/W
31.F014.7	TX_FAULT Function	0 = TX_FAULT status indicated by 1.0008.11. 1 = TX_FAULT is used for GPIO Function.	R/W
31.F014.6:4	TX_FAULT Select	Interrupt is effective only when 31.F013.1 = 0. Same as 31.F014.14:12	R/W
31.F014.2:0	MOD_ABS Select	Interrupt is effective only when 31.F013.0 = 0. Same as 31.F014.14:12	R/W
31.F015.15	TOD Function	0 = TOD is used for LED Function. 1 = TOD is used for GPIO Function.	R/W
31.F015.14:12	TOD Select	Interrupt is effective only when 31.F013.7 = 0. Same as 31.F014.14:12	R/W
31.F015.11	MPC Function	0 = MPC is used for LED Function. 1 = MPC is used for GPIO Function.	R/W
31.F015.10:8	MPC Select	Interrupt is effective only when 31.F013.6 = 0. Same as 31.F014.14:12	R/W
31.F015.7	LED1 Function	0 = LED1 is used for LED Function. 1 = LED1 is used for GPIO Function.	R/W
31.F015.6:4	LED1 Select	Interrupt is effective only when 31.F013.5 = 0. Same as 31.F014.14:12	R/W
31.F015.3	LED0 Function	0 = LED0 is used for LED Function. 1 = LED0 is used for GPIO Function.	R/W
31.F015.2:0	LED0 Select	Interrupt is effective only when 31.F013.4 = 0. Same as 31.F014.14:12	R/W
31.F016.15	SCL Function	0 = SCL is used for TWSI Function. 1 = SCL is used for GPIO Function.	R/W
31.F016.14:12	SCL Select	Interrupt is effective only when 31.F013.11 = 0. Same as 31.F014.14:12	R/W
31.F016.11	SDA Function	0 = SDA is used for TWSI Function. 1 = SDA is used for GPIO Function.	R/W
31.F016.10:8	SDA Select	Interrupt is effective only when 31.F013.10 = 0. Same as 31.F014.14:12	R/W

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Table 29: GPIO Interrupt Type (Continued)

Register	Function	Setting	Mode
31.F016.4:3	TX_DISABLED Function	00 = TX_DISABLED is used for LED Function. 01 = TX_DISABLED is used for GPIO Function. 10 = TX_DISABLED controlled by 1.0009.4:0	R/W
31.F016.2:0	TX_DISABLED Select	Interrupt is effective only when 31.F013.8 = 0. Same as 31.F014.14:12	R/W

3.5.4 SFP Behavior

The behavior of TX_DISABLE, RX_LOS, and TX_FAULT pins can be set to interact with the IEEE defined registers and PCS.

3.5.4.1 TX_DISABLE

When register 31.F016.4:3 of a port is set to 10, the TX_DISABLE has the following behavior.

The TX_DISABLE pin is configured as an output and writing to registers 31.F010.8, 31.F012.8, and 31.F013.8 has no effect.

If the PCS of port N is configured to 1000BASE-X, or 10GBASE-R then

- TX_DISABLE[N] pin is set high when port N register 1.0009.0 is set to 1 or 1.0009.1 is set to 1. Otherwise TX_DISABLE[N] pin is set low.

If the PCS of port 0 is configured to XAUI, or 40GBASE-R4 then

- TX_DISABLE[0] pin is set high when port 0 register 1.0009.0 is set to 1 or 1.0009.1 is set to 1. Otherwise TX_DISABLE[0] pin is set low.
- TX_DISABLE[1] pin is set high when port 0 register 1.0009.0 is set to 1 or 1.0009.2 is set to 1. Otherwise TX_DISABLE[1] pin is set low.
- TX_DISABLE[2] pin is set high when port 0 register 1.0009.0 is set to 1 or 1.0009.3 is set to 1. Otherwise TX_DISABLE[2] pin is set low.
- TX_DISABLE[3] pin is set high when port 0 register 1.0009.0 is set to 1 or 1.0009.4 is set to 1. Otherwise TX_DISABLE[3] pin is set low.

Note that the PCS transmit path is also disabled when the transmit disable bits are set in register 1.0009.

3.5.4.2 RX_LOS

When 31.F014.11 is set to 0 the RX_LOS pin is configured as an input and writing to register 31.F013.2 has no effect. The RX_LOS is used in conjunction with the receiver status of the lane to determine signal detect. Both the RX_LOS and the receiver must detect a signal for signal detect to be up. When 31.F014.11 = 1, then RX_LOS is not used to determine signal detect and only the receiver status of the lane is used to determine signal detect status.

Port N register 31.F012.2 will report the state of RX_LOS[N], and 31.F011.2 will report the interrupt status of RX_LOS[N] regardless of the setting of register 31.F014.11.

When register 31.F014.11 of a port is set to 0, the RX_LOS has the following behavior that is dependent on the PCS.

If the PCS of port N is configured to 1000BASE-X, or 10GBASE-R then

- RX_LOS[N] pin is used for lane 0 signal detect, and port N register 1.000A.0 and 1.000A.1 reflects the signal detect status.

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If the PCS of port 0 is configured to XAUI, or 40GBASE-R4 then

- RX_LOS[0] pin is used for lane 0 signal detect, and port 0 register 1.000A.1 reflects the signal detect status.
- RX_LOS[1] pin is used for lane 1 signal detect, and port 0 register 1.000A.2 reflects the signal detect status.
- RX_LOS[2] pin is used for lane 2 signal detect, and port 0 register 1.000A.3 reflects the signal detect status.
- RX_LOS[3] pin is used for lane 3 signal detect, and port 0 register 1.000A.4 reflects the signal detect status.
- Port 0 register 1.000A.0 is set to 1 whenever all four bits of 1.000A.4:1 are set to 1.

3.5.4.3 TX_FAULT

When 31.F014.7 is set to 0, the TX_FAULT pin is configured as an input and writing to register 31.F013.1 has no effect. The TX_FAULT pin is used to determine the state of the transmit fault register 1.0008.11. When 31.F014.7 = 1, then register 1.0008.11 is always set to 0.

Port N register 31.F012.1 will report the state of TX_FAULT[N], and 31.F011.1 will report the interrupt status of TX_FAULT[N] regardless of the setting of register 31.F014.7.

When register 31.F014.7 of a port is set to 0, the TX_FAULT has the following behavior that is dependent on the PCS.

If the PCS of port N is configured to 1000BASE-X, or 10GBASE-R then

- Port N register 1.0008.11 is set to 1 when TX_FAULT[N] is high. Otherwise register 1.0008.11 is set to 0.

If the PCS of port 0 is configured to XAUI, or 40GBASE-R4 then

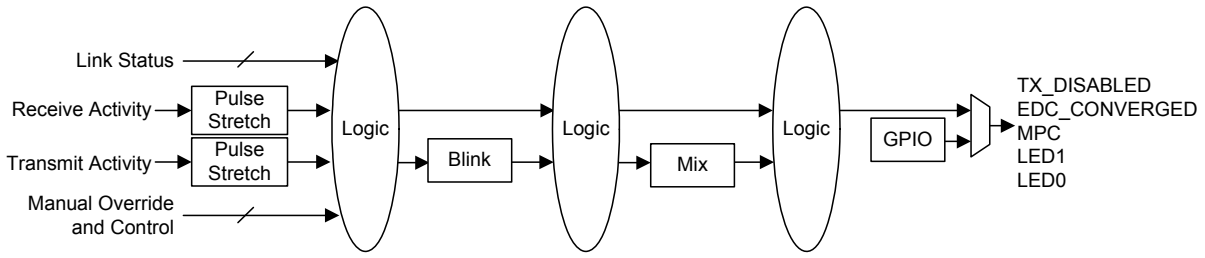
- Port 0 register 1.0008.11 is set to 1 when any of the TX_FAULT[3:0] is high. Otherwise register 1.0008.11 is set to 0.

3.6 LED

The TX_DISABLED, TOD, MPC, LED1, and LED0 pins can be used to drive LED pins. Registers 31.F020 through 31.F027 control the operation of the LED pins. TX_DISABLED, TOD, MPC, LED1, and LED0 will operate per this section unless the pin is used for GPIO purposes (see Section 3.5, GPIO and SFP+, on page 52).

Figure 10 shows the general chaining of function for the LEDs. The various functions are described in the following sections. All LED pins are open drain outputs.

Figure 10: LED Chain



3.6.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 11. In order to make things more flexible registers 31.F020.1:0, 31.F021.1:0, 31.F022.1:0, 31.F023.1:0, and 31.F024.1:0 specify the output polarity for the LED function. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z.

Figure 11: Various LED Hookup Configurations

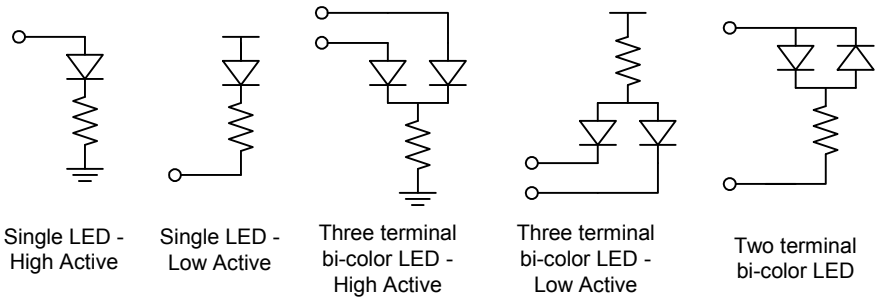


Table 30: LED Polarity

Register	LED Function	Definition
31.F020.1:0	LED0	00 = On - drive LED0 low, Off - drive LED0 high 01 = On - drive LED0 high, Off - drive LED0 low 10 = On - drive LED0 low, Off - tristate LED0 11 = On - drive LED0 high, Off - tristate LED0
31.F021.1:0	LED1	00 = On - drive LED1 low, Off - drive LED1 high 01 = On - drive LED1 high, Off - drive LED1 low 10 = On - drive LED1 low, Off - tristate LED1 11 = On - drive LED1 high, Off - tristate LED1
31.F022.1:0	MPC	00 = On - drive MPC low, Off - drive MPC high 01 = On - drive MPC high, Off - drive MPC low 10 = On - drive MPC low, Off - tristate MPC 11 = On - drive MPC high, Off - tristate MPC
31.F023.1:0	TOD	00 = On - drive TOD low, Off - drive TOD high 01 = On - drive TOD high, Off - drive TOD low 10 = On - drive TOD low, Off - tristate TOD 11 = On - drive TOD high, Off - tristate TOD
31.F024.1:0	TX_ DISABLED	00 = On - drive TX_DISABLED low, Off - drive TX_DISABLED high 01 = On - drive TX_DISABLED high, Off - drive LTX_DISABLED low 10 = On - drive TX_DISABLED low, Off - tristate TX_DISABLED 11 = On - drive TX_DISABLED high, Off - tristate TX_DISABLED

3.6.2 Pulse Stretching and Blinking

Register 31.F027.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

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Some status will require blinking instead of a solid on. Register 31.F027.10:8 and 31.F027.6:4 specifies the 2 blink rates. Note that the pulse stretching is applied first, and the blinking will reflect the duration of the stretched pulse.

Registers 31.F020.2, 31.F021.2, 31.F022.2, 31.F023.2, and 31.F024.2 select which of the 2 blink rates to use for LED0, LED1, MPC, TOD, and TX_DISABLED respectively.

0 = Select Blink Rate 1

1 = Select Blink Rate 2

The stretched/blinked output will then be mixed if needed (see Section 3.6.3, Bi-Color LED Mixing, on page 61). For information on pulse stretching and blinking, see Table 31.

Table 31: Pulse Stretching and Blinking

Register	LED Function	Definition
31.F027.14:12	Pulse stretch duration	000 = No pulse stretching 001 = 20 ms to 40 ms 010 = 40 ms to 81 ms 011 = 81 ms to 161 ms 100 = 161 ms to 322 ms 101 = 322 ms to 644 ms 110 = 644 ms to 1.3s 111 = 1.3s to 2.6s
31.F027.10:8	Blink Rate 2	000 = 40 ms 001 = 81 ms 010 = 161 ms 011 = 322 ms 100 = 644 ms 101 = 1.3s 110 = 2.6s 111 = 5.2s
31.F027.6:4	Blink Rate 1	000 = 40 ms 001 = 81 ms 010 = 161 ms 011 = 322 ms 100 = 644 ms 101 = 1.3s 110 = 2.6s 111 = 5.2s

3.6.3 Bi-Color LED Mixing

In the dual LED modes, the mixing function allows the 2 colors of the LED to be mixed to form a third color. Register 31.F026.7:4 control the amount to mix in the TOD and LED1 pins. Register 31.F026.3:0 controls the amount to mix in the MPC and LED0 pins. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are 2 types of bi-color LEDs: 3 terminal type, and 2 terminal type. For example, the third and fourth LED block from the left in Figure 11 illustrate 3 terminal types, and the one on the far right in Figure 11 illustrate the 2 terminal type. In the 3 terminal type both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 31.F026.7:4 and 31.F026.3:0 can exceed 100%. However, in the 2 terminal type, the sum should never exceed 100% since only 1 LED can be turned on at any given time.

The mixing only applies when register 31.F020.11:8 or 31.F022.11:8 are set to 101x. There is no mixing in single LED modes.

Table 32: Bi-Color LED Mixing

Register	LED Function	Definition
31.F026.7:4	TOD, LED1 mix percentage	0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
31.F026.3:0	MPC, LED0 mix percentage	0000 = 0% 0001 = 12.5%, . . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved

3.6.4 Modes of Operation

The LED pins relay various statuses of the PHY so that they can be displayed by the LEDs.

The statuses that the LEDs display is defined by registers 31.F020 to 31.F025 as shown in Table 33. For each LED, if the condition selected by bits 11:8 is true, the LED will blink. If the condition selected by bits 7:4 is true, the LED will be solid on. If both selected conditions are true, the blink will take precedence.

Table 33: LED Display

Register	LED Function	Definition
31.F020.11:8	LED0 Blink Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1000 = Reserved 1001 = Reserved 1010 = Blink Mix 1011 = Solid Mix 11xx = Reserved
31.F020.7:4	LED0 Solid Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1xxx = Reserved

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Table 33: LED Display (Continued)

Register	LED Function	Definition
31.F021.11:8	LED1 Blink Behavior	Blink Behavior has higher priority. This register ignored if 31.F020.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
31.F021.7:4	LED1 Solid Behavior	Blink Behavior has higher priority. This register ignored if 31.F020.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
31.F022.11:8	MPC Blink Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1000 = Reserved 1001 = Reserved 1010 = Blink Mix 1011 = Solid Mix 11xx = Reserved
31.F022.7:4	MPC Solid Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1xxx = Reserved

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Table 33: LED Display (Continued)

Register	LED Function	Definition
31.F023.11:8	TOD Blink Behavior	Blink Behavior has higher priority. This register ignored if 31.F022.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
31.F023.7:4	TOD Solid Behavior	Blink Behavior has higher priority. This register ignored if 31.F022.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
31.F024.11:8	TX_DISABLED Blink Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 11xx = Reserved
31.F024.7:4	TX_DISABLED Solid Behavior	Blink Behavior has higher priority. 0000 = Solid Off 0001 = Transmit or Receive Activity 0010 = Transmit Activity 0011 = Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Link 0111 = Solid On 1xxx = Reserved

3.7 EEPROM Bridging and Polling

The 88X2242 device supports the ability to cache the contents of the EEPROM into an onboard RAM for faster read access. The device has the ability to periodically read the EEPROM and refresh the RAM. The 88X2242 device can also act as a bridge so that the EEPROM or other devices can be accessed via the MDC/MDIO interface of the PHY.

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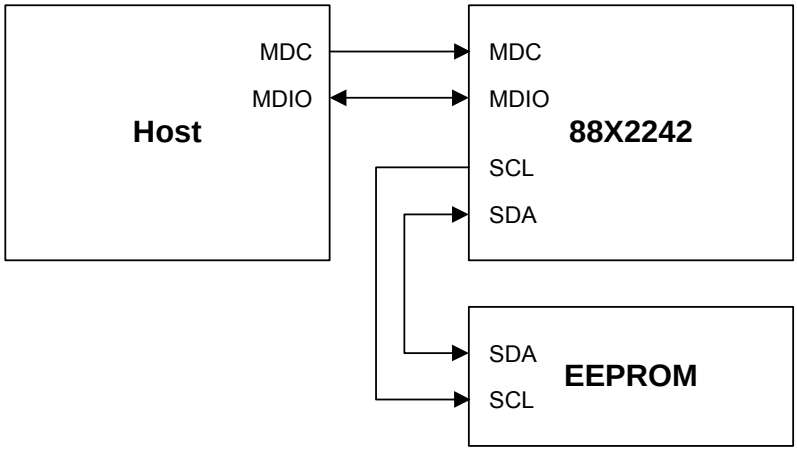
The EEPROM or external device is attached to the Two-wire Serial Interface (TWSI) via the SCL and SDA pins.

Register 1.8000.10 can be set to 1 to force the TWSI to reset.

Figure 12: MDC/MDIO Bridging



3.7.1 Bridging Function

The bridging function allows the contents of the EEPROM to be accessed directly via the MDC/MDIO. The access is through a series of reads and writes to the PHY register. Note that the access is not limited to the EEPROM but also to any device that is attached to the TWSI.

Since other devices may be connected to the TWSI where the slave address is not necessarily 1010xxx, there is a hook to access the TWSI device directly from the MDIO. Registers 1.8001, 1.8002, and 1.8003 give direct access between the MDIO and the TWSI.

Table 34: EEPROM Address Register

Register	Function	Setting	Mode
1.8001.15:9	Slave Address	Slave Address	R/W
1.8001.8	Read/Write	A write to 1.8001 will initiate a read or write command on the TWSI if the TWSI is free; otherwise, the read or write command will be ignored. Make sure register 1.8002.10:8 is not equal to 010 (command in progress) prior to writing this register A read to 1.8001 will not trigger any action. Register 1.8003.7:0 must be set to the value to be written prior to issuing a write command. 1 = Read, 0 = Write	R/W
1.8001.7:0	Byte Address	Byte Address	R/W

Table 35: EEPROM Read Data Register and EEPROM/RAM Status Register

Register	Function	Setting	Mode
1.8002.12	Cache ECC Single Bit Corrected Interrupt Status	0 = No single bit correction in ECC cache detected 1 = Single bit correction in ECC cache detected	RO, LH
1.8002.11	Cache ECC Uncorrectable Bit Interrupt Status	0 = No uncorrectable bit in ECC cache detected 1 = Uncorrectable bit in ECC cache detected	RO, LH
1.8002.10:8	TWSI Status	Register 1.8002.10:8 is the status in response to setting to writing register 1.8001. Register 1.8002.10:8 will remain at 010 until the command is completed. Once the command is completed, the status 001, 011, 100, 101, or 111 will remain until register 1.8002 is read. The register will clear on read. If a new command is issued by writing register 1.8001 without reading register 1.8002 for a previous command, the status of the previous command will be lost. If a command initiated by writing register 1.8001 is still in progress and a second command is issued, the status 1.8002.10:8 will reflect the first command. The second command is ignored but register 1.8002.10:8 will not be set to 111. Command Done - No Error is set when the TWSI slave properly responds with ACK. In the case of a write command with automatic read back, a Command Done - No Error status will be returned even if the read back data does not match the written data or if the TWSI slave does not respond with ACK during the read back. Register 1.8002.7:0 is valid only when register 1.8002.10:8 is set to 001. 000 = Ready 001 = Command Done - No Error 010 = Command in Progress 011 = Write done but read back failed 100 = Reserved 101 = Command Failed 110 = Reserved 111 = two-wire interface Busy, Command Ignored	RO, LH
1.8002.7:0	Read Data	Read Data Register 1.8002.7:0 is valid only when register 1.8002.10:8 is set to 001.	RO

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Table 36: EEPROM Write Data Register and EEPROM/RAM Control Register

Register	Function	Setting	Mode
1.8003.15:12	Write Time	0000 = EEPROM takes 0 ms to write 0001 = 1.05 ms …. 1110 = 14.68 ms 1111 = 15.73 ms	R/W
1.8003.9	Automatic read back after write	If read back is enabled, then data will always be read back after a write. The read data is stored in register 1.8002.7:0 1 = Read back, 0 = no read back	R/W
1.8003.7:0	Write Data	Write Data	R/W

3.7.1.1 Read from TWSI Slave Device to the MDIO

When a read operation to the TWSI is required, the slave address and byte address is written to register 1.8001.15:9 and 1.8001.7:0 respectively with register 1.8001.8 set to 1 indicating read. Once register 1.8001 is written, a read operation on the TWSI commences only if the TWSI is free; otherwise, a read operation on the TWSI is never issued. The byte that is read is stored in register 1.8002.7:0. The status of the read operation is stored in register 1.8002.10:8.

While the read operation is pending register 1.8002.10:8 is set to 010. Once the read operation is completed and the TWSI slave sends all acknowledges register 1.8002.10:8 is set to 001 indicating the read operation completed without error. A 101 is returned if the read command is aborted when the TWSI slave does not acknowledge properly. A 111 is returned if the TWSI is busy when register 1.8001 was written.

Note that other than the 010 setting (command in progress) a read to 1.8002 will cause bits 10:8 to clear to 000.

3.7.1.2 Write from MDIO into the TWSI Slave Device

Write commands into the EEPROM are always available through the MDIO. If write access should be disabled, the EEPROM itself should be configured to ignore write commands from the 88X2242 device.

When a write operation to the TWSI is required, the byte data should first be written into 1.8003.7:0. The slave address and byte address is written to register 1.8001.15:9 and 1.8001.7:0 respectively with register 1.8001.8 set to 0 indicating write. Once register 1.8001 is written a write operation to the TWSI commences. If the read back bit is set in register 1.8003.9 then a read operation to the same address is performed after the write. The byte that is read is stored in register 1.8002.7:0. The status of the write operation is stored in register 1.8002.10:8.

While the write operation is pending register 1.8002.10:8 is set to 010. Once the write operation is completed and, optionally, the read back command and the TWSI slave sends all acknowledges, register 1.8002.10:8 is set to 001 indicating the write operation completed without error. A 011 is returned if the write operation is successfully completed but the read back command is aborted. A 101 is returned if the write command is aborted when the TWSI slave does not acknowledge properly. A 111 is returned if the TWSI is busy when register 1.8001 was written. Note that other than the 010 setting (command in progress) a read to 1.8002 will cause bits 10:8 to clear to 000.

Since it may take some time for the write to take effect in the external device, the 88X2242 device should wait for some amount of time as programmed in register 1.8003.15:12 after the write operation before issuing a read back command.

3.7.2 EEPROM Caching into RAM

The contents of the EEPROM or other device on the TWSI can be cached into on-chip memory. There are 2 segments of 128 bytes that can be cached. The first 128 byte segment is referred to as the A0 page, and the second 128 byte segment is referred to as the secondary page.

Table 37, Table 38, and Table 39 list all the caching and polling registers. The A0 page always has a slave address of 1010000 and always reads the lower 128 bytes of the device. The A0 page control registers are located in 1.8000.1:0, the status registers located in 1.8000.3:2 and 1.8000.9, and the 128 bytes are stored in 1.8007 to 1.8086 bits 7:0.

The secondary page has similar registers located in 1.8000.12:11, 1.8000.14:13, 1.8000.15, and 1.8087 to 1.8106 bits 7:0 respectively. The only exception for the secondary page is that the slave address is not fixed and can be specified in 1.8004.7:1, and 18004.0 specifies whether the upper or lower 128 bytes of the device is read.

The caching sequence is not triggered at the de-assertion of hardware reset. Instead, the EEPROM is read, and RAM is loaded every time the MOD_ABS pin makes a high to low transition. The caching sequence takes place after a delay specified by register 1.8004.15:13. The A0 page is cached on MOD_ABS high to low transition only if 1.8000.1:0 is set to 01 or 10. The secondary page is similarly cached only if 1.8000.12:11 is set to 01 or 10. If caching is enabled for both pages, then page A0 is always loaded first.

Note that if the TWSI is active for any reason when the MOD_ABS pin is triggered, the caching sequence will be deferred until the TWSI is inactive. If the TWSI is in the middle of a caching sequence initiated by the user (see below) the current caching sequence will be aborted after the completion of the active TWSI transaction and a new caching sequence is then started.

Either or both RAM caches are periodically updated if register 1.8000.1:0 and/or 1.8000.12:11 are set to 10. The update period is specified by register 1.8004.10:9. If both caches are to be updated the A0 page gets updated first. The polling will continue until it is disabled via registers 1.8000.1:0 or 1.8000.12:11. Alternatively, if the MOD_ABS pin goes high, the polling will stop immediately after the TWSI transaction completes.

The contents of the EEPROM can be reloaded into RAM by writing register 1.8000.1:0 and/or 1.8000.12:11 to 11. These bits are self-clearing. If both 1.8000.1:0 and 1.8000.12:11 are set to 11 concurrently, the A0 page will be serviced first and, upon completion, 1.80001:0 will be cleared and then the secondary page will be serviced. Manual loading can be initiated regardless of the state of the MOD_ABS pin. The result of the reload can be read via register 1.8000.3:2, 1.8000.9 or 1.8000.14:13, 1.8000.15.

All single byte read/write commands are deferred when initiated in the middle of an RAM update cycle.

Once the caching sequence is completed, the status register in 1.8000.3:2 or 1.8000.14:13 will be updated. Registers 1.8000.3:2 and 18000.14:13 are clear on read registers. After reading, the bits clear to 00. The status registers are updated according to the following priority.

If the entire 128 bytes have been updated successfully at least once since the last read to register 1.8000, then the status bits will be set to 01.

If all attempts to read the entire 128 bytes have failed since the last read to register 1.8000, then the status bits will be set to 11. A fail is defined to have occurred if any of the 128 byte reads return error.

If the circuit is in the middle of the first attempt to update the 128 bytes since the last read to register 1.8000, then the status will return 10.

If the circuit never made an attempt to update the 128 byte registers since the last read to register 1.8000, then the status will return 00.

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Whenever MOD_ABS pin transitions from 0 to 1 or whenever software or hardware reset is asserted, then 1.8000.9 and 1.8000.15 are set to 0s. If 1 successful caching sequence completes, then 1.8000.9 or 1.8000.15 will be set to a 1 and remains set until MOD_ABS transitions from 0 to 1 or until a software or hardware reset is issued. Once the status bit is set to 1, it will remain set even if subsequent updates are not successful.

The maximum size EEPROM for each segment that can be handled is 128 bytes. The expected device type and device page selection in the slave address of the EEPROM is 1010000 for the A0 page. Any other value will result in the EEPROM not being read. Note that other pages can be read by setting registers 1.8004.7:1 and 1.8004.0.

The RAM can be access via reading registers 1.8007 to 1.8086 bits 7:0 for the A0 page and 1.8087 to 1.8106 bits 7:0 for the secondary page.

The RAM is protected by an Error Correction Circuit (ECC) that generates 2 status signals, 1 to indicate a single bit error has been corrected and another to indicate uncorrectable bit errors. These 2 signals are used to generate interrupts. Registers 1.8004.12:11 are the interrupt enable bits and 1.8002.12:11 are the interrupt status bits. The interrupt status bits latch high when the status bits assert. The bits clear on read.

Table 37: Caching and Polling Control and Status Register

Register	Function	Setting	Mode
1.8000.15	Cache Valid Secondary Page	0 = Registers 1.8087 to 1.8106 invalid 1 = Registers 1.8087 to 1.8106 valid This bit is set to 1 if at least 1 successful cache update is completed since hardware, software reset, or MOD0 transitions from 0 to 1. Use register 1.8000.14:13 for latest status.	RO
1.8000.14:13	Command Status Secondary Page	00 = Cache not updated since last read 01 = Contents in cache updated at least once since last read 10 = Cache is currently loading since last read 11 = All caching attempts since last read failed This register clears on read. Register 1.8000.15 indicates whether the content of the cache is valid from any updates in the past.	RO, SC
1.8000.12:11	Cache Setting Secondary Page	00 = No automatic caching 01 = Cache once at module plugin 10 = Cache at module plugin and periodically poll 11 = Manual cache refresh The page cached is selected by register 1.8004.7:0	R/W
1.8000.10	TWSI Reset	0 = Normal operation 1 = Force TWSI circuit to reset	R/W, SC
1.8000.9	Cache Valid Page A0	0 = Registers 1.8007 to 1.8086 invalid 1 = Registers 1.8007 to 1.8086 valid This bit is set to 1 if at least 1 successful cache update is completed since hardware, software reset, or MOD0 transitions from 0 to 1. Use register 1.8000.14:13 for latest status.	RO

Table 37: Caching and Polling Control and Status Register (Continued)

Register	Function	Setting	Mode
1.8000.3:2	Command Status Page A0	00 = Cache not updated since last read 01 = Contents in cache updated at least once since last read 10 = Cache is currently loading since last read 11 = All caching attempts since last read failed This register clears on read. Register 1.8000.9 indicates whether the content of the cache is valid from any updates in the past.	RO, SC
1.8000.1:0	Cache Setting Page A0	00 = No automatic caching 01 = Cache once at module plugin 10 = Cache at module plugin and periodically poll 11 = Manual cache refresh Page A0 lower 128 bytes are cached.	R/W

Table 38: Caching and Polling Register

Register	Function	Setting	Mode
1.8004.15:13	Auto Caching Delay	000 = No delay 001 = 0.25 Second 010 = 0.5 Second 011 = 1 Second 100 = 2 Seconds 101 = 4 Seconds 110 = 8 Seconds 111 = Auto Caching Disabled	R/W
1.8004.12	Cache ECC Single Bit Corrected Interrupt Enable	0 = Interrupt disabled 1 = Interrupt enabled	R/W
1.8004.11	Cache ECC Uncorrectable Bit Interrupt Enable	0 = Interrupt disabled 1 = Interrupt enabled	R/W
1.8004.10:9	Page Reload Frequency	00 = 250 ms 01 = 500 ms 10 = 1 second 11 = 2 seconds	R/W
1.8004.7:1	Secondary Page	Seven bit slave address to use when loading 1.8087 to 1.8106.	R/W
1.8004.0	Secondary Page Register Address MSB	0 = Lower 128 bytes of secondary page should be loaded 1 = Upper 128 bytes of secondary page should be loaded	R/W

Table 39: Cache Registers

Register	Function	Setting	Mode
1.8007 to 8086.7:0	Page A0 EEPROM Byte	Byte (REGAD - 0x8007) Of EEPROM	RO
1.8087 to 8106.7:0	Secondary Page EEPROM Byte	Byte (REGAD - 0x8087) Of EEPROM	RO

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Note EEPROM caching is supported only for applications that do not require clock stretching.

3.8 Interrupt

Various functional units in the device can generate interrupt on the INTn pin. INTn is pulled low when an enabled interrupt is active.

The interrupt status is reported upwards via 3 levels:

- First level (information purposes only)—Reports which port is generating an active interrupt
- Second level—Reports which function in the port is generating the interrupt
- Third level—Interrupt registers report the actual interrupt status

  The third level interrupt status and the corresponding enables are described in the register sections for each function, and in the interrupt tree diagrams below. The polarity of the interrupt can be controlled by Register 31.F421.

Table 40: First Level Interrupt Status

Register	Function	Setting
31.F420.7	Port M3 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.6	Port M2 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.5	Port M1 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.4	Port M0 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.3	Port N3 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.2	Port N2 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.1	Port N1 Interrupt Status	0 = No Interrupt 1 = Active Interrupt
31.F420.0	Port N0 Interrupt Status	0 = No Interrupt 1 = Active Interrupt

Table 41: Second Level Interrupt Status

Register	Function	Setting	Section Reference
31.F040.3	GPIO Interrupt	0 = No Interrupt 1 = Active Interrupt	Section 3.5.3, GPIO Interrupts, on page 55
31.F040.2	System Side PCS Interrupt	0 = No Interrupt 1 = Active Interrupt	Section 5.6, Traffic Generation and Checking, on page 100
31.F040.0	Line Side PCS Interrupt	0 = No Interrupt 1 = Active Interrupt	Section 4.7, PRBS and Pattern Generators, on page 94

Table 42: Interrupt Polarity Control

Register	Function	Setting
31.F421.2:1	Interrupt Polarity	00 = Active - drive INT low, Inactive - drive INT high 01 = Active - drive INT high, Inactive - drive INT low 10 = Active - drive INT low, Inactive - tristate INT 11 = Active - drive INT high, Inactive - tristate INT
31.F421.0	Force Interrupt Pin Active	0 = Normal operation 1 = Force interrupt pin active

Figure 13: Chip level Interrupt Generation Diagram

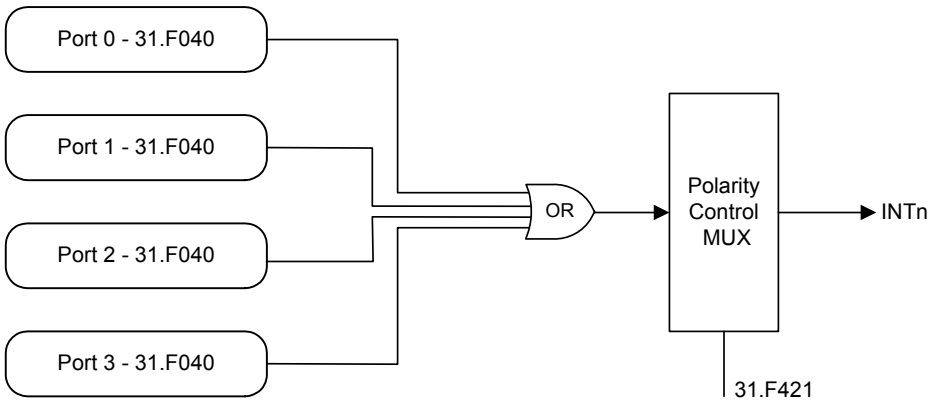

Figure 14: Chip level Interrupt Port Location (First Level)

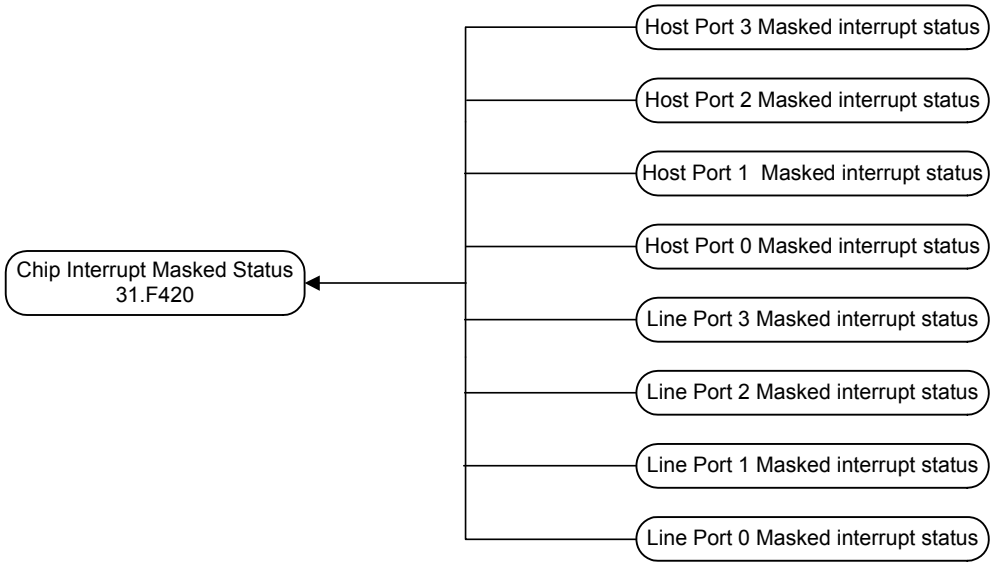

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Figure 15: Per Port Interrupt Function Source (Second Level)

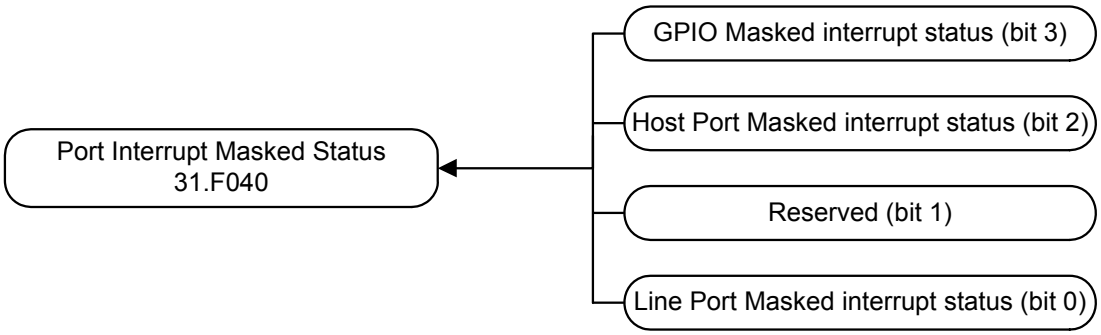


Figure 16: Interrupt Source - GPIO Interrupt Masked Status (Third Level)

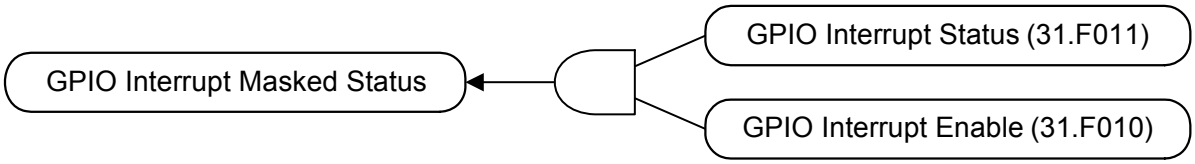


Figure 17: Interrupt Source - Host Port Interrupt Masked Status (Third Level)

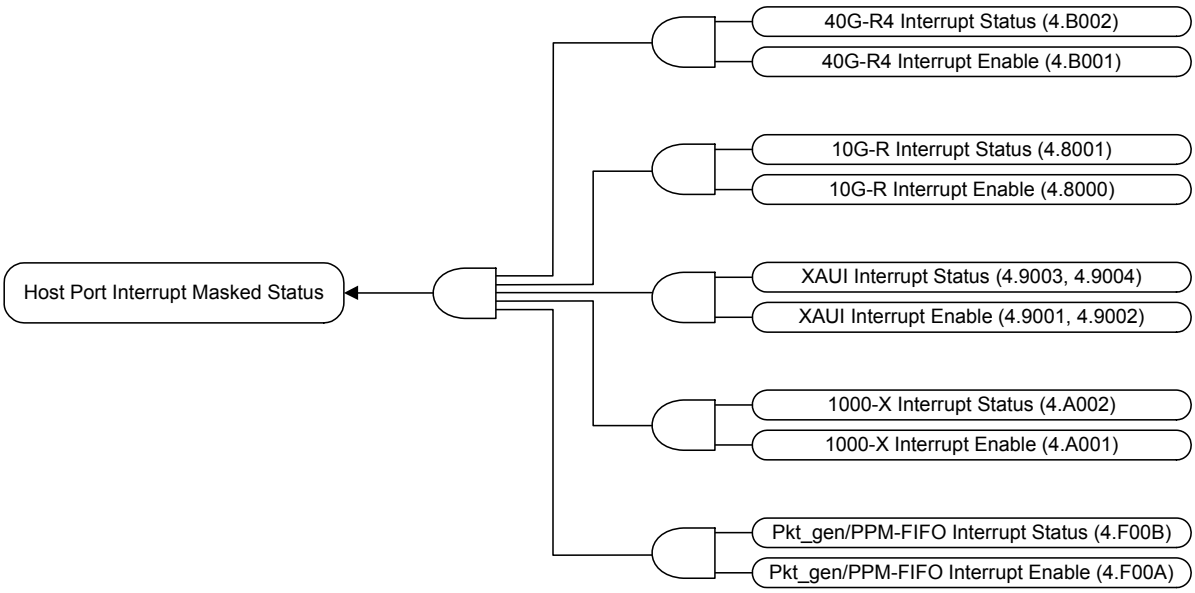


Figure 18: Interrupt Source - Line Port Interrupt Masked Status (Third Level)

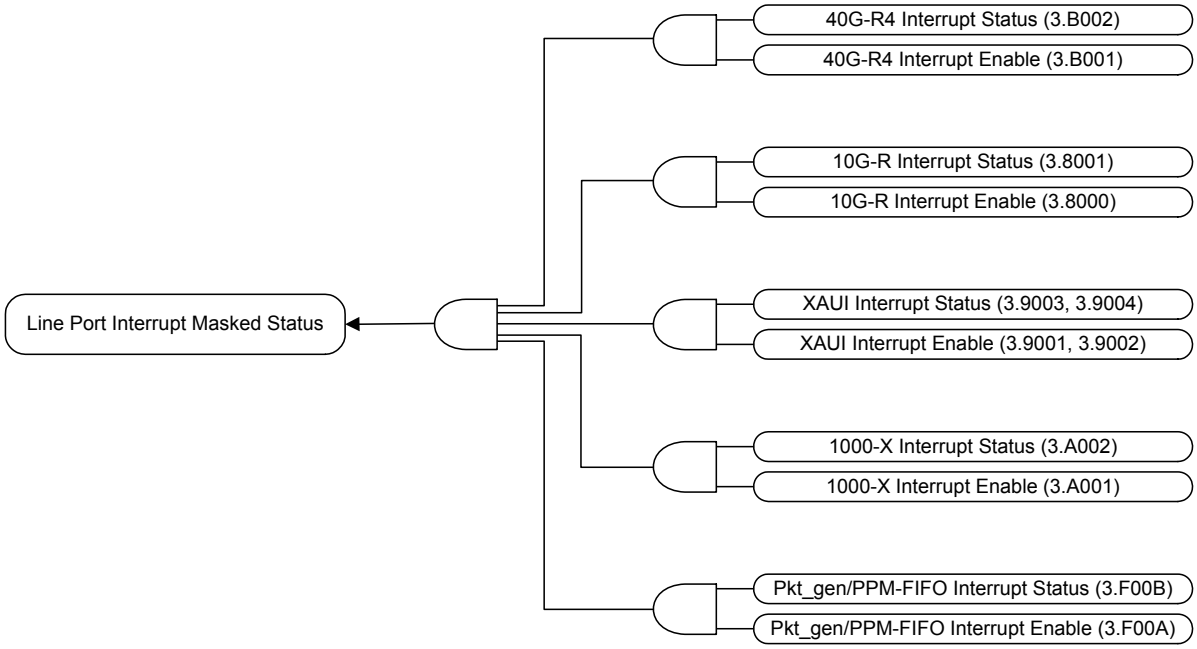
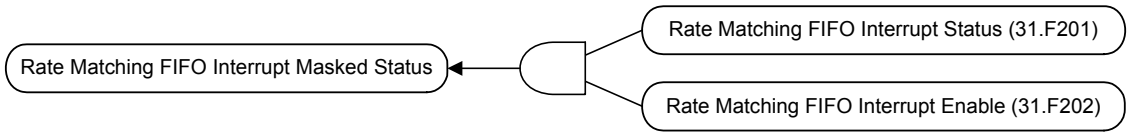


Figure 19: Interrupt Source - Rate Matching FIFO Interrupt Masked Status (Third Level)



3.9 Power Management

The chip can be globally set to be in the power down state after hardware reset. For information on how See Section 3.3, Hardware Configuration, on page 49 on how to configure the device in the power down state.

The Line and Host can be manually powered down as described in Section 4.5, Power Management, on page 92 and Section 5.5, Power Management, on page 100 respectively.

They can also be powered up and down via a single write to register 31.F403.7:0. Note that there are many registers that can be used to power down various blocks (for example, 31.F403.7:0 registers in Section 4.5, Power Management, on page 92 and Section 5.5, Power Management, on page 100). All registers associated with a block must be powered for it to be active.

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3.10 IEEE1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The 88X2242 device implements the instructions shown in Table 43. Upon reset, ID_CODE instruction is selected. The instruction opcodes are shown in Table 43.

Table 43: TAP Controller Opcodes

Instruction	OpCode
EXTEST	0000_0000
SAMPLE/PRELOAD	0000_0001
CLAMP	0000_0010
HIGH-Z	0000_0011
ID_CODE	0000_0100
EXTEST_PULSE	0000_0101
EXTEST_TRAIN	0000_0110
AC_EXTEST	0000_0111
PROG_HYST	0000_1000
BYPASS	1111_1111

The 88X2242 device reserves 5 pins called the Test Access Port (TAP) to provide test access: Test Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK while output signal (TDO) is clocked on the falling edge. For additional details, refer to the IEEE 1149.1 Boundary Scan Architecture document.

3.10.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the 88X2242 device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

3.10.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the 88X2242 device. Two functions are performed when this instruction is selected: sample and preload.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

The boundary scan register for MIN[7] is closest to TDO.

Table 44 lists the boundary scan order where:

TDI ➔ INTn ➔ … ➔ MIN7] ➔ TDO

Table 44: Boundary Scan Chain Order

Order	Ball	Type
1	MIN[7]	AC Input
2	MIP[7]	AC Input
3	MOP[7]/MON[7]	AC Output
4	MOP[7]/MON[7]	AC/DC Select
5	MIN[3]	AC Input
6	MIP[3]	AC Input
7	MOP[3]/MON[3]	AC Output
8	MOP[3]/MON[3]	AC/DC Select
9	NIN[3]	AC Input
10	NIP[3]	AC Input
11	NOP[3]/NON[3]	AC Output
12	NOP[3]/NON[3]	AC/DC Select
13	LED0[3]	Input
14	LED0[3]	Output
15	LED0[3]	Output Enable
16	LED1[3]	Input
17	LED1[3]	Output
18	LED1[3]	Output Enable
19	MPC[3]	Input
20	MPC[3]	Output
21	MPC[3]	Output Enable
22	TOD[3]	Input
23	TOD[3]	Output
24	TOD[3]	Output Enable
25	TX_DISABLE[3]	Input
26	TX_DISABLE[3]	Output
27	TX_DISABLE[3]	Output Enable
28	MOD_ABS[3]	Input
29	MOD_ABS[3]	Output
30	MOD_ABS[3]	Output Enable
31	TX_FAULT[3]	Input

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Table 44: Boundary Scan Chain Order (Continued)

Order	Ball	Type
32	TX_FAULT[3]	Output
33	TX_FAULT[3]	Output Enable
34	LOS[3]	Input
35	LOS[3]	Output
36	LOS[3]	Output Enable
37	GPIO[3]	Input
38	GPIO[3]	Output
39	GPIO[3]	Output Enable
40	SCL[3]	Input
41	SCL[3]	Output
42	SCL[3]	Output Enable
43	SDA[3]	Input
44	SDA[3]	Output
45	SDA[3]	Output Enable
46	MIN[6]	AC Input
47	MIP[6]	AC Input
48	MOP[6]/MON[6]	AC Output
49	MOP[6]/MON[6]	AC/DC Select
50	MIN[2]	AC Input
51	MIP[2]	AC Input
52	MOP[2]/MON[2]	AC Output
53	MOP[2]/MON[2]	AC/DC Select
54	NIN[2]	AC Input
55	NIP[2]	AC Input
56	NOP[2]/NON[2]	AC Output
57	NOP[2]/NON[2]	AC/DC Select
58	LED0[2]	Input
59	LED0[2]	Output
60	LED0[2]	Output Enable
61	LED1[2]	Input
62	LED1[2]	Output
63	LED1[2]	Output Enable
64	MPC[2]	Input
65	MPC[2]	Output
66	MPC[2]	Output Enable
67	TOD[2]	Input
68	TOD[2]	Output
69	TOD[2]	Output Enable
70	TX_DISABLE[2]	Input
71	TX_DISABLE[2]	Output

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Table 44: Boundary Scan Chain Order (Continued)

Order	Ball	Type
72	TX_DISABLE[2]	Output Enable
73	MOD_ABS[2]	Input
74	MOD_ABS[2]	Output
75	MOD_ABS[2]	Output Enable
76	TX_FAULT[2]	Input
77	TX_FAULT[2]	Output
78	TX_FAULT[2]	Output Enable
79	LOS[2]	Input
80	LOS[2]	Output
81	LOS[2]	Output Enable
82	GPIO[2]	Input
83	GPIO[2]	Output
84	GPIO[2]	Output Enable
85	SCL[2]	Input
86	SCL[2]	Output
87	SCL[2]	Output Enable
88	SDA[2]	Input
89	SDA[2]	Output
90	SDA[2]	Output Enable
91	MIN[5]	AC Input
92	MIP[5]	AC Input
93	MOP[5]/MON[5]	AC Output
94	MOP[5]/MON[5]	AC/DC Select
95	MIN[1]	AC Input
96	MIP[1]	AC Input
97	MOP[1]/MON[1]	AC Output
98	MOP[1]/MON[1]	AC/DC Select
99	NIN[1]	AC Input
100	NIP[1]	AC Input
101	NOP[1]/NON[1]	AC Output
102	NOP[1]/NON[1]	AC/DC Select
103	LED0[1]	Input
104	LED0[1]	Output
105	LED0[1]	Output Enable
106	LED1[1]	Input
107	LED1[1]	Output
108	LED1[1]	Output Enable
109	MPC[1]	Input
110	MPC[1]	Output
111	MPC[1]	Output Enable

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Table 44: Boundary Scan Chain Order (Continued)

Order	Ball	Type
112	TOD[1]	Input
113	TOD[1]	Output
114	TOD[1]	Output Enable
115	TX_DISABLE[1]	Input
116	TX_DISABLE[1]	Output
117	TX_DISABLE[1]	Output Enable
118	MOD_ABS[1]	Input
119	MOD_ABS[1]	Output
120	MOD_ABS[1]	Output Enable
121	TX_FAULT[1]	Input
122	TX_FAULT[1]	Output
123	TX_FAULT[1]	Output Enable
124	LOS[1]	Input
125	LOS[1]	Output
126	LOS[1]	Output Enable
127	GPIO[1]	Input
128	GPIO[1]	Output
129	GPIO[1]	Output Enable
130	SCL[1]	Input
131	SCL[1]	Output
132	SCL[1]	Output Enable
133	SDA[1]	Input
134	SDA[1]	Output
135	SDA[1]	Output Enable
136	MIN[4]	AC Input
137	MIP[4]	AC Input
138	MOP[4]/MON[4]	AC Output
139	MOP[4]/MON[4]	AC/DC Select
140	MIN[0]	AC Input
141	MIP[0]	AC Input
142	MOP[0]/MON[0]	AC Output
143	MOP[0]/MON[0]	AC/DC Select
144	NIN[0]	AC Input
145	NIP[0]	AC Input
146	NOP[0]/NON[0]	AC Output
147	NOP[0]/NON[0]	AC/DC Select
148	LED0[0]	Input
149	LED0[0]	Output
150	LED0[0]	Output Enable
151	LED1[0]	Input

Table 44: Boundary Scan Chain Order (Continued)

Order	Ball	Type
152	LED1[0]	Output
153	LED1[0]	Output Enable
154	MPC[0]	Input
155	MPC[0]	Output
156	MPC[0]	Output Enable
157	TOD[0]	Input
158	TOD[0]	Output
159	TOD[0]	Output Enable
160	TX_DISABLE[0]	Input
161	TX_DISABLE[0]	Output
162	TX_DISABLE[0]	Output Enable
163	MOD_ABS[0]	Input
164	MOD_ABS[0]	Output
165	MOD_ABS[0]	Output Enable
166	TX_FAULT[0]	Input
167	TX_FAULT[0]	Output
168	TX_FAULT[0]	Output Enable
169	LOS[0]	Input
170	LOS[0]	Output
171	LOS[0]	Output Enable
172	GPIO[0]	Input
173	GPIO[0]	Output
174	GPIO[0]	Output Enable
175	SCL[0]	Input
176	SCL[0]	Output
177	SCL[0]	Output Enable
178	SDA[0]	Input
179	SDA[0]	Output
180	SDA[0]	Output Enable
181	CONFIG[0]	Input
182	CONFIG[1]	Input
183	CONFIG[2]	Input
184	CONFIG[3]	Input
185	RCLK0	Output
186	RCLK0	Output Enable
187	RCLK1	Output
188	RCLK1	Output Enable
189	FREQ_SEL[0]	Input
190	FREQ_SEL[1]	Input
191	RESETn	Input

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Table 44: Boundary Scan Chain Order (Continued)

Order	Ball	Type
192	MDC	Input
193	MDIO	Input
194	MDIO	Output
195	MDIO	Output Enable
196	INTn	Output
197	INTn	Output Enable

3.10.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the 88X2242 device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the 88X2242 to its external connections. Note that the SERDES output pins will be driven to static levels. The positive and negative legs of the SERDES output pins are controlled via a single boundary scan cell.The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

3.10.4 CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

3.10.5 HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

Note The SERDES outputs cannot be tri-stated.

3.10.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.

Table 45: ID CODE Instruction

Version	Part Number	Manufacturer Identity	Bit
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	Bit 0
0000	0000000000110001	00111101001	1

3.10.7 EXTEST_PULSE Instruction

When the AC/DC select is set to DC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the SERDES output pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the SERDES positive output pins output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the SERDES positive output pins output the inverted level specified by the test stimulus and SERDES negative output pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the SERDES positive output pins again output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

3.10.8 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the SERDES output pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon execution of the EXTEST_PULSE instruction, the SERDES positive output pins output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state, the SERDES output pins will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the SERDES positive output pins again output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

3.10.9 AC-JTAG Fault Detection

The fault detection across AC coupled connections can be detected with a combination of (DC) EXTEST and any one of the AC JTAG commands. The AC coupled connection is shown in Figure 20. The fault signature is shown in Table 46.

- Column 1 lists the fault type.
- Columns 2 to 5 list the behavior when both the transmitter and receiver are running the EXTEST_TRAIN and EXTEST_PULSE commands.
  - Column 2 shows the expected value captured by the boundary scan cell that is connected to the test receiver, which is connected to the positive input when a negative differential pulse is transmitted.
  - Column 3 is the same as column 2 except for the negative input.
  - Columns 4 and 5 are similar to columns 2 and 3 except a positive differential pulse is transmitted.
- Columns 6 to 9 is similar to columns 2 to 5 except both the transmitter and receiver are running the (DC) EXTEST command.

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While it is not possible to identify precisely which fault is occurring based on the fault signature, the signature to the no fault condition is unique when the (DC) EXTEST command is run with at least 1 of the EXTEST_TRAIN, or EXTEST_PULSE commands. Note that running only AC JTAG commands is not sufficient since the no fault condition signature is not distinguishable from the Tx to Rx short (see shaded cells in Table 46).

Figure 20: AC Coupled Connection

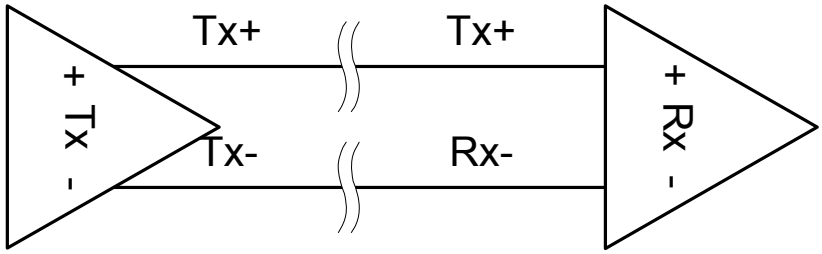


Table 46 provides details about the positive/negative legs for AC testing samples and (DC) EXTEST samples. In Table 46, the positive leg column is identified as +, and the negative leg column is identified as –.

Table 46: AC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	+	–	+	–	+	–	+	–
Tx+ Open	0	X	0	X	1	X	1	X
Tx- Open	X	0	X	0	X	1	X	1
Rx+ Open	0	X	0	X	1	X	1	X
Rx- Open	X	0	X	0	X	1	X	1
Tx+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
Tx- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
Rx+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
Rx- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
Tx+ short to ground	0	X	0	X	1	X	1	X
Tx- short to ground	X	0	X	0	X	1	X	1
Rx+ short to ground	0	X	0	X	0	X	0	X
Rx- short to ground	X	0	X	0	X	0	X	0
Tx+ short to Tx-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
Rx+ short to Rx-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
Tx+ short to Rx-	X	0	X	1	X	0	X	1
Tx- short to Rx+	1	X	0	X	1	X	0	X

NOTES:
1. Short on positive and negative leg can have several behavior on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.
2. A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.

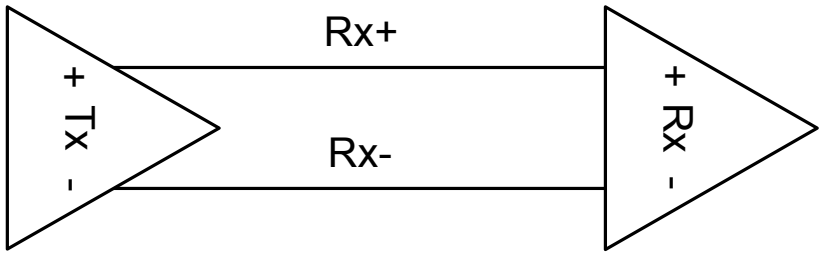
Table 46: AC Coupled Connection Fault Signature (Continued)

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	+	–	+	–	+	–	+	–
Tx+ short to Rx+	0	X	1	X	0	X	1	X
Tx- short to Rx-	X	1	X	0	X	1	X	0
No Fault	0	1	1	0	1	1	1	1

NOTES:
1. Short on positive and negative leg can have several behavior on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.
2. A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.

The fault detection across DC coupled connections can be detected with any one of the AC JTAG or (DC) EXTEST commands. The DC coupled connection is shown in Figure 21. The fault signature is shown in Table 47.

Figure 21: DC Coupled Connection



In Table 47, the positive leg column is identified as +, and the negative leg column is identified as –.

Table 47: DC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	+	–	+	–	+	–	+	–
Rx+ Open	0	X	0	X	1	X	1	X
Rx- Open	X	0	X	0	X	1	X	1
Rx+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
Rx- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
Rx+ short to ground	0	X	0	X	0	X	0	X
Rx- short to ground	X	0	X	0	X	0	X	0

NOTES:
1. Short on positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.
2. A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.

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Table 47: DC Coupled Connection Fault Signature (Continued)

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	+	–	+	–	+	–	+	–
Rx+ short to Rx-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
No Fault	0	1	1	0	0	1	1	0

NOTES:
1. Short on positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.
2. A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.

3.11 Reference Clock

An external oscillator provides a reference for the on-board transmit Phase Lock Loop (PLL) and clock generation block that provides internal clocks for both the transmit and receive data paths. The clock input pins are CLKP/CLKN.

CLKP/CLKN runs on a 156.25 MHz differential clock. The FREQ_SEL[1:0] should be set to 00.

3.12 Power Supplies

The 88X2242 device requires 3 power supplies: 1.5V (analog), 1.1V (analog), and 1.0V (digital).

If 1.2V, 1.8V, 2.5V, or 3.3V I/Os are required, then additional supplies will be required.

3.12.1 AVDD15

AVDD15_N and AVDD15_M are the 1.5V analog supplies.

3.12.2 AVDD11

AVDD11_N is the 1.1V analog supply.

3.12.3 AVDD10

AVDD10_M is the 1.0V analog supply.

3.12.4 DVDD

DVDD is the core logic 1.0V digital supply.

3.12.5 VDDO

There are 4 separate VDDO segments (VDDOT, VDDOS, VDDOL, and VDDOM). Each segment can be independently set to 1 for the following voltages: 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V. Each VDDO segment has a corresponding voltage select configuration pin (VSEL_T, VSEL_S, VSEL_L, and VSEL_M). Table 48 lists the signals under each of the VDDO segments.

If the VDDO* segment is set to 1.2V, 1.5V, or 1.8V, then its corresponding VSEL_* should tied to VDDO*.

If the VDDO* segment is set to 2.5V, or 3.3V, then its corresponding VSEL_* should tied to VSS.

The input pins are not high voltage tolerant. For example, if VDDOT is tied to 2.5V, then RESETn should not be driven to 3.3V.

Table 48: Signal Power Segment

Power Segment	VDDOT	VDDOS	VDDOL	VDDOM
Voltage Select	VSEL_T	VSEL_S	VSEL_L	VSEL_M
Signals	FREQ_SEL[1:0]	LOS[3:0]	CONFIG[3:0]	INTn
	RESETn	MOD_ABS[3:0]	TOD[3:0]	MDC
	TCK	MPC[3:0]	GPIO[3:0]	MDIO
	TDI	SCL[3:0]	LED0[3:0]	
	TDO	SDA[3:0]	LED1[3:0]	
	TEST	TX_DISABLE[3:0]		
	TMS	TX_FAULT[3:0]		
	TRST			

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4 Line Side Description

This section includes information on the following topics:

- Section 4.1, Media Electrical Interface
- Section 4.2, PCS
- Section 4.3, Loopback
- Section 4.4, Synchronization FIFO
- Section 4.5, Power Management
- Section 4.6, Traffic Generation and Checking
- Section 4.7, PRBS and Pattern Generators
- Section 4.8, Interrupt

The line side interface is comprised of 4 differential input lanes NIP[3:0] / NIN[3:0] and 4 differential output lanes NOP[3:0] / NON[3:0]. They can operate over multi-mode fiber, single mode fiber, and Twinax copper cables. The DSP engine overcomes the impairments of the fiber cable, optical front end, and electrical interconnect. In this document, each set of input / output lanes is referred to as lane N0, N1, N2, and N3.

These lanes can be arranged to form 4-ports of 1000BASE-X,10GBASE-R, and 1-port of 40GBASE-R4.

4.1 Media Electrical Interface

The input and output buffers of the SERDES interface are internally terminated by 50Ω impedance (100Ω differential). No external terminations are required.

The SERDES transmitter uses a 3 tap (1 pre-tap and 1 post-tap) FIR filter that is implemented for the purpose of channel equalization. The FIR tap values can be manually adjusted to optimize the transmit eye over a particular channel.

The SERDES receiver contains a DSP based Electronic Dispersion Compensation engine to perform clock and data recovery that significantly exceed the receiver performance specified by the 10GBASE-LRM standard. Advanced algorithms enables operation over multi-mode fiber.

The Electronic Dispersion Compensation can be disabled when not needed to trade performance vs. power and latency.

4.2 PCS

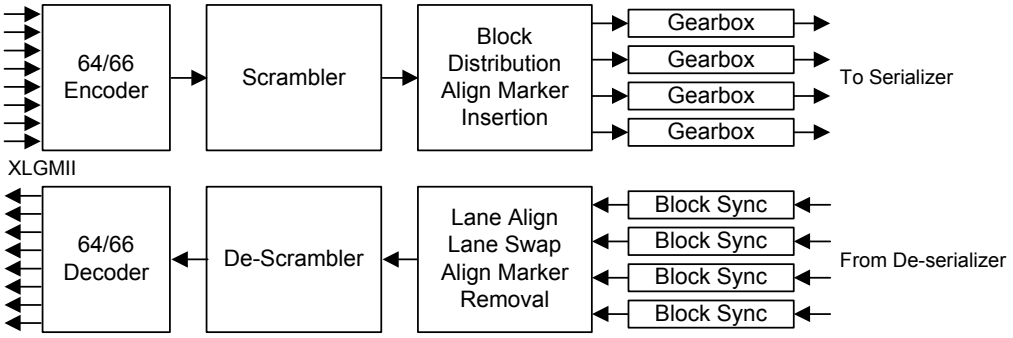
Each port supports a multiple number of different PCS. Section 3.1.2, PCS Operational Mode and Lane Attachment, on page 44 describes how to configure each port for the various PCS. This section focuses on the PCS itself.

4.2.1 40GBASE-R4

The 40GBASE-R4 PCS is available only on port 0. Lanes N0 to N3 correspond to lanes 0 to 3 of the PCS. It is enabled by setting register 31.F002.14:8 to 0x70.

The 40GBASE-R4 PCS operates according to Clause 82 and 83 of the IEEE 802.3ba specification. The PCS uses a 64B/66B coding and scrambling to improve the transmission characteristics of the serial data and ease clock recovery at the receiver. The data stream is distributed across 4 lanes. The alignment markers allows the lanes to be aligned and lanes to be swapped at the receiver. The synchronization headers for 64B/66B code enable the receiver to achieve block alignment on the receive data. For further details refer to the IEEE 802.3ba specification.

Figure 22: 40GBASE-R4 PCS

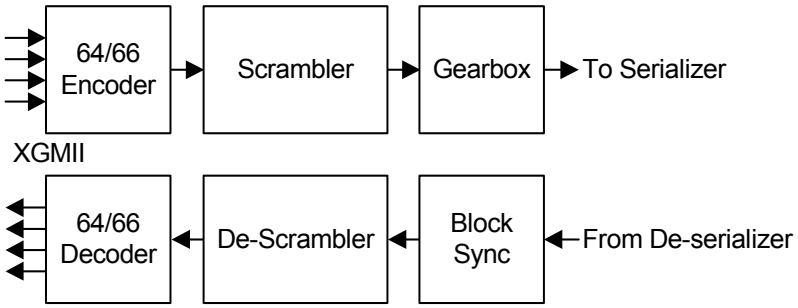


4.2.2 10GBASE-R

The 10GBASE-R PCS is available on all ports. Lanes N0 through N3 are used by port 0 through 3 respectively. It is enabled by setting register 31.F002.14:8 to 0x71.

The 10GBASE-R PCS operates according to Clause 49 of the IEEE 802.3ae specification. The PCS uses a 64B/66B coding and scrambling to improve the transmission characteristics of the serial data and ease clock recovery at the receiver. The synchronization headers for 64B/66B code enable the receiver to achieve block alignment on the receive data. For further details refer to the IEEE 802.3 specification.

Figure 23: 10GBASE-R PCS



4.2.3 1000BASE-X

The 1000BASE-X PCS is available on all ports. Lanes N0 through N3 are used by port 0 through 3 respectively. There are several modes of 1000BASE-X. It is enabled by setting register 31.F002.14:8 to 1 for the following values.

- 0x7A = 1000BASE-X, 1000BASE-X Auto-Negotiation off

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- 0x7B = 1000BASE-X, 1000BASE-X Auto-Negotiation on
- 0x7C = SGMII (system), SGMII Auto-Negotiation off
- 0x7D = SGMII (system), SGMII Auto-Negotiation on
- 0x7E = SGMII (media), SGMII Auto-Negotiation off
- 0x7F = SGMII (media), SGMII Auto-Negotiation on

4.2.3.1 PCS

The 1000BASE-X PCS operates according to Clause 36 of the IEEE 802.3 specification. The PCS uses a 8/10 bit coding for DC line balancing. For further details refer to the IEEE 802.3 specification.

The SGMII protocol is also supported over 1000BASE-X. The SGMII allows 10 Mbps, 100 Mbps, and 1000 Mbps throughput over 1000BASE-X line coding.

When SGMII Auto-Negotiation is turned off (3.2000.12 = 0) the speed setting is programmed via register 3.2000 bits 13 and 6. Link is established when the underlying 1000BASE-X establishes link.

When SGMII Auto-Negotiation is turned on (3.2000.12 = 1) and the SGMII is set to the media side the speed setting is programmed via register 3.2000 bits 13 and 6. This speed capability is advertised and Auto-Negotiations have to complete prior to link being established.

When SGMII Auto-Negotiation is turned on(3.2000.12 = 1) and the SGMII is set to the system side the speed setting is determined by the Auto-Negotiation speed advertised by the link partner. Auto-Negotiations must be complete prior to link being established.

Although register 31.F002.14:8 can set the Auto-Negotiation to be on or off, that setting can be overridden by writing register 3.2000.12.

The SGMII mode is intended to be operated in pairs. In general the port on the line side will be set to SGMII system while the attached port on the host side set to SGMII media, though it is possible to reverse this. If SGMII Auto-Negotiation is turned on, the Auto-Negotiation results on the SGMII system on the line side will be passed to the SGMII media on the host side which will in turn advertise the results.

4.2.3.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE 802.3 specification. It is used to auto-negotiate duplex and flow control over fiber cable. Registers 3.2000, 3.2004, 3.2005, 3.2006, 3.2007, 3.2008, and 3.200F are used to enable AN, advertise capabilities, determine link partner's capabilities, show AN status, and show the duplex mode of operation respectively.

The device supports Next Page option for 1000BASE-X Auto-Negotiation. Register 3.2007 of the fiber pages is used to transmit Next Pages, and register 3.2008 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set Register 3.2004.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in Register 3.2007.

If the PHY enables 1000BASE-X Auto-Negotiation and the link partner does not, the link cannot be established. The device implements an Auto-Negotiation bypass mode. For more details, see Section 4.2.3.4, Auto-Negotiation Bypass Mode, on page 90.

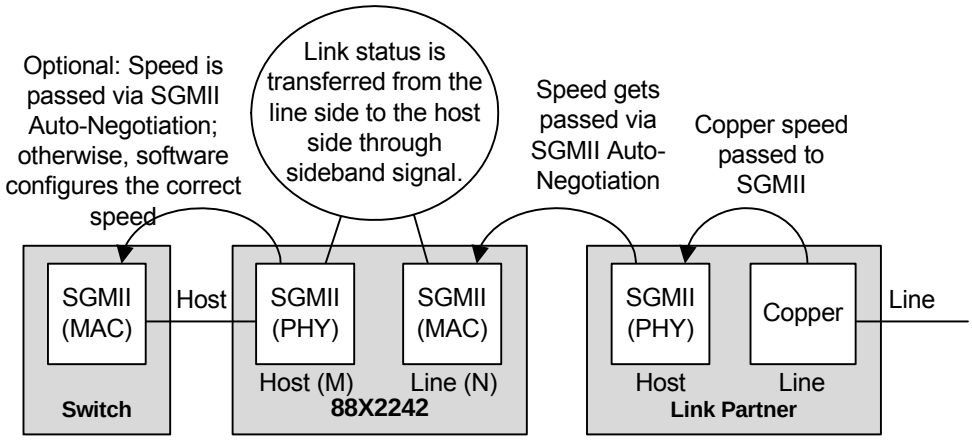
4.2.3.3 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the "Cisco SGMII Specification" and the "MAC Interfaces and Auto-Negotiation" application note for further details.

The device supports SGMII with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 3.2000.12 followed by a soft reset. If SGMII Auto-Negotiation is disabled, the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (for example, by reading PHY registers for link, speed, and duplex status).

The SGMII Auto-Negotiation information flow is shown in Figure 24.

Figure 24: SGMII Auto-Negotiation Information Flow



4.2.3.4 Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the link partner does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Auto-Negotiation Bypass Mode. When entering the state “Ability_Detect”, a bypass timer begins to count down from an initial value of approximately 200 ms. If the device receives idles during that 200 ms, the device will interpret that the other side is “alive” but cannot send configuration codes to perform Auto-Negotiation. After the 200 ms timeframe, the state machine will move to a new state called “Bypass_Link_Up” in which the device assumes a link-up status and the operational mode is set to the value listed under the Comments column of Table 49.

Table 49: SGMII Auto-Negotiation Modes

Reg. 3.2000.12	Reg. 3.A000.13	Comments
0	X	No Auto-Negotiation. User responsible for determining speed, link, and duplex status by reading PHY registers.
1	0	Normal SGMII Auto-Negotiation. Speed, link, and duplex status automatically communicated to the MAC during Auto-Negotiation.
1	1	MAC Auto-Negotiation enabled. Normal operation.
		MAC Auto-Negotiation disabled. After 200 ms the PHY will disable Auto-Negotiation and link based on idles.

4.3 Loopback

The line side SERDES support 2 loopback paths.

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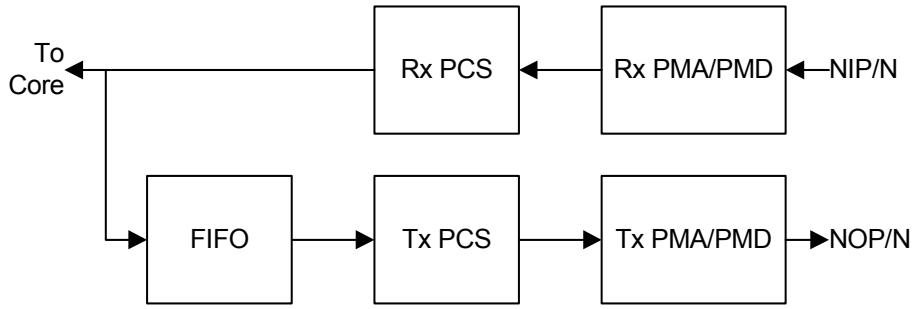
If register 3.F003.12 = 1 then data from the line will loopback to the line as shown in Figure 25.

Figure 25: Shallow Line Loopback



Registers 2.0000.14, 3.0000.14, 3.1000.14, 3.2000.14, and 3.3000.14 are physically the same bit. If any of these bits are set to 1 then data from the core will loopback to the core as shown in Figure 26 and Figure 27. If register 3.F003.6 = 0 then the egress path will not be blocked as shown in Figure 26. If register 3.F003.6 = 1 then the egress path will be blocked as shown in Figure 27.

Figure 26: Deep Host Loopback, No Egress Blocking

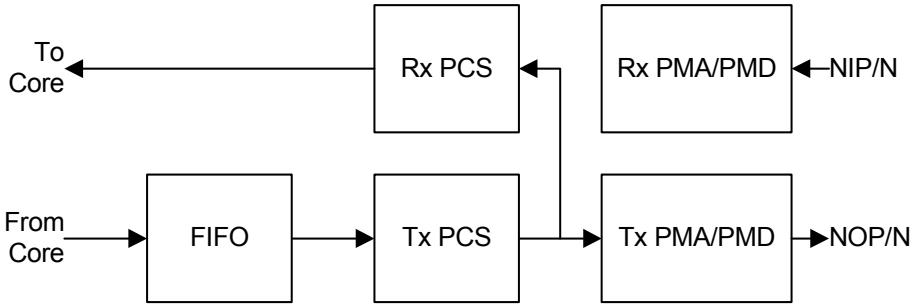
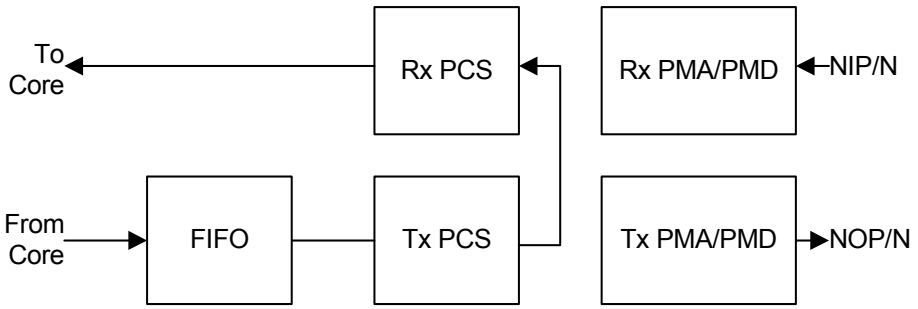


Figure 27: Deep Host Loopback, Egress Blocking



4.4 Synchronization FIFO

Each port has a transmit synchronizing FIFOs to reconcile frequency differences between the clocks of the internal bus and the clock used to transmit data onto the media interface. The depth of the FIFO can be programmed by setting Register 3.F00C.15:14.

The FIFO depths can be increased in length to support longer frames. The device has settings for maximum frame sizes of 10K, 20K, 40K, and 80K bytes with up to ± 100 ppm clock jitter in 10 Gbps operation and 10K, 15K, 20K, and 25K bytes with up to ±100 ppm clock jitter in 1 Gbps operation. The deeper the FIFO depth, the higher the latency will be.

The FIFO overflow/underflow status is reported in Register 3.F00B.1:0.

4.5 Power Management

The 88X2242 device will automatically power down unused circuits. The media side can be forced into a power down state by setting 1.0000.11, 2.0000.11, 3.0000.11, 3.1000.11, 3.2000.11, or 3.3000.11 to 1. Note that these power down registers are physically the same bit even though they reside in different locations. Port level register, 31.F003.14 can also be used to power down the media side. Since 31.0xF003.14 is physically a separate register bit, setting this bit won't be reflected into PCS power down bits mentioned above, but will override them.

To soft reset the media side set registers 1.0000.15, 2.0000.15, 3.0000.15, 3.1000.15, 3.2000.15, 3.3000.15, or 7.0000.15 to 1. Register 31.F003.15 can also be used to soft reset the media side. Note that these software reset registers are physically the same bit even though they reside in different locations.

4.6 Traffic Generation and Checking

This section describes the Generator/Checker functions. All counters are 48 bits long. If Register 3.F010.14 is set to 1, the counters clear on read. If Register 3.F010.14 is set to 0, the counters will keep counting unto 3.F010.6 is set to 1 to clear the contents.

4.6.1 Packet Generator

A packet generator enables the device to generate traffic onto the media without the need to receive data from the host.

Register 3.F010.1 enables the internal packet generator.

Register 3.F016 specifies the number of bytes in the packet that is to be generated. This count includes the frame bytes but does not include the 4 byte CRC (unless it is appended - Register 3.F011.3 = 0), the terminate symbol, nor the 8 preamble bytes. If the register is set to 0x0000 then the length will be randomly selected between 64 to 1518 bytes. If the register is set to 0x0001 then the length will be randomly selected to be between 64 to 0x0FFF bytes, 0x0002 then 64 to 0x1FFF bytes, 0x0003 then 64 to 0x3FFF bytes, 0x0004 then 64 to 0x7FFF bytes, 0x0005 then 64 to 0xFFFF bytes. If 0x0008 to 0xFFFF then the number of bytes transmitted is fixed from 8 to 0xFFFF.

Register 3.F017 specifies the number of packets to burst. 0x0000 means stop generation, 0xFFFF means continuously generate packets, 0x0001 to 0xFFFE means send a burst of 1 to 0xFFFE packets.

Register 3.F018 specifies the gap between packets. Each increment in the value increases the idle time by 4 bytes. 3.F018.14:0 specifies the upper limit of the gap. If 3.F018.15 is 0 then the lower limit for IPG is also specified by 3.F018.14:0. Otherwise a random gap between 1 x 4 bytes to 3.F018.14:0 x 4 bytes will be used. For the purposes of counting IPG all lanes must be idle for it to be counted as an IPG. In other words if the terminate symbol is in the XGMII word then it does not count towards the IPG.

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Register 3.F012 and 3.F013 specifies the initial value of the payload or the fixed value of the payload. The 4 bytes in this register corresponds to the first 4 bytes of the frame. Register 3.F011.7:4 specifies the behavior of the payload.

When 3.F011.7:4 = 000x then registers 3.F012 and 3.F013 are used as the payload repeatedly.

When 3.F011.7:4 = 0010 then registers 3.F012 and 3.F013 are used as the payload repeatedly but every other XGMII word should be inverted. That is, a payload of 034EA675 will result in a sequence of 034EA675, FCB1598A, 034EA675, FCB1598A, ….

When 3.F011.7:4 = 0011 then registers 3.F012 and 3.F013 are used as the payload repeatedly but inverted every second XGMII word. That is, a payload of 034EA675 will result in a sequence of 034EA675, 034EA675, FCB1598A, FCB1598A, 034EA675, 034EA675, FCB1598A, FCB1598A, ….

When 3.F011.7:4 = 0100 then registers 3.F012 and 3.F013 are used as the initial value and each byte subsequently bitwise left shifted. That is, a payload of 034EA675 will result in a sequence of 034EA675, 069C4DEA, 0C399AD5, 187235AB, ….

When 3.F011.7:4 = 0101 then registers 3.F012 and 3.F013 are used as the initial value and each byte subsequently bitwise right shifted.

When 3.F011.7:4 = 0110 then registers 3.F012 and 3.F013 are used as the initial value and the 32 bits subsequently bitwise left shifted. That is, a payload of C34EA675 will result in a sequence of C34EA675, 869D4CEB, 0D3A99D7, 1A7533AE, ….

When 3.F011.7:4 = 0111 then registers 3.F012 and 3.F013 are used as the initial value and the 32 bits subsequently bitwise right shifted.

When 3.F011.7:4 = 1000 then registers 3.F012 and 3.F013 are used as the initial value and subsequently bytewise incremented. That is, a payload of FFFE0055 will result in a sequence of FFFE0055, 00FF0156, 01000257, 02010358, ….

When 3.F011.7:4 = 1001 then registers 3.F012 and 3.F013 are used as the initial value and subsequently bytewise decremented.

When 3.F011.7:4 = 1010 then registers 3.F012 and 3.F013 are ignored and a pseudo random payload is generated. All 4 bytes are the same value for each cycle.

When 3.F011.7:4 = 1011 then registers 3.F012 and 3.F013 are ignored and a pseudo random payload is generated. All 4 bytes are randomly generated for each cycle.

At the start of each packet registers 3.F012 and 3.F013 should be used to reset the initial values to ensure that the pattern in the packet is the same when repeated over and over many times. The only time that the pattern in the packet will be different is when pseudo random generation is selected.

For each packet generated the 48 bit counter in 3.F01B, 3.F01C, and 3.F01D is incremented by 1.

For each byte generated the 48 bit counter in 3.F01E, 3.F01F, and 3.F020 is incremented by 1. Preamble bytes are not counted but CRC bytes are counted.

Register 3.F011.3 controls whether the CRC is generated or not.

4.6.2 Checker

The CRC checker is enabled by setting Register 3.F010.0 to 1.

If Register 3.F010.2 = 0, the checker will wait until the start of frame delimiter (SFD) is detected to detect the frame boundary.

If Register 3.F010.2 = 1, the checker will assume the first 8 bytes of the packet is the preamble and the frame starts at the ninth byte of the packet.

There are 3 sets of 48-bit counters for the checker.

- Registers 3.F021, 3.F022, 3.F023 is the receive packet counter.

- Register 3.F027, 3.F028, and 3.F029 is the receive packet error counter.
- Register 3.F024, 3.F025, and 3.F026 is the receive byte counter.

The receive packet counter counts the number of packets received regardless of whether there is a CRC error. The receive packet error counter increments once per packet with a CRC error. The byte counter counts the number of bytes in the frame including the CRC. The preamble bytes are not counted.

4.7 PRBS and Pattern Generators

The device supports various IEEE defined and proprietary PRBS generators and checkers, and transmit waveform pattern generators. Only 1 generator/checker may be enabled at a time per lane. Unpredictable results may occur if multiple generators are enabled simultaneously.

4.7.1 General PRBS Generators and Checkers

Each lane has its own general PRBS generator and checker. Port 0 registers controls lane 0, port 1 controls lane 1, port 2 controls lane 2, and port 3 controls lane 3.

Register 3.F030 controls the generator and checker. Setting register 3.F030.5 to 1 enables the generator, and setting register 3.F030.4 to 1 enables the checker. If either of these bits is set to 1, the general PRBS generator and checker overrides the PCS specific generators and checkers.

Register 3.F030.3:0 controls the pattern that is generated and checked. There is no checker for the high frequency, low frequency, mixed frequency, and square wave patterns as there are waveforms to check the transmitter performance.

0000 = IEEE 49.2.8 - PRBS 31

0001 = PRBS 7

0010 = PRBS 9 IEEE 83.7

0011 = PRBS 23

0100 = PRBS 31 Inverted

0101 = PRBS 7 Inverted

1000 = PRBS 15

1001 = PRBS 15 Inverted

0110 = PRBS 9 Inverted

0111 = PRBS 23 Inverted

1100 = High frequency pattern

1101 = Low frequency pattern

1110 = Mixed frequency pattern

1111 = Square Wave pattern

All counters are 48 bits long. If register 3.F030.13 is set to 1 then the counters will clear on read. If register 3.F030.13 is set to 0 then the counters will keep counting until register 3.F030.6 is set to 1 to clear the contents. If register 3.F030.7 is set to 0, then the PRBS counters will not start to count until the checker first locks onto the incoming PRBS data. If register 3.F030.7 is set to 1 then the PRBS checker will start counting errors without first locking to the incoming PRBS data. Register 3.F030.8 indicates whether the PRBS checker has locked.

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All 48-bit counters are formed by 3 16-bit registers. The lowest addressed register is the least significant 16 bits and the highest addressed register is the most significant 16 bits of the counter. When the least significant register is read, the 2 upper registers are updated and frozen so that the 3 register read is atomic. Note that it is not necessary to read the upper registers. However, upon subsequent reads of the least significant register, the values of the upper registers from the previous reads are lost. In order to get the correct upper register value the least significant register must be read first.

Register 3.F031, 3.F032, and 3.F033 is the transmit bit counter. Register 3.F034, 3.F035, and 3.F036 is the receive bit counter. Register 3.F037, 3.F038, and 3.F039 is the receive bit error counter.

4.7.2 40GBASE-R4 Specific Generators and Checkers

Register 3.302A.7 is used to enable generation of scramble idle code.

4.7.3 10GBASE-R Specific Generators and Checkers

Registers 3.002A.4 and 3.002A.5 when set to 1 enables the PRBS31 generator and checker respectively. Register 3.002A.3 and 3.002A.2 when set to 1 enables the transmit and receive test patterns respectively. Register 3.002A.1 selects the test pattern. The error counter is in register 3.002B.15:0 and clears on read.

4.7.4 XAUI Specific Generators and Checkers

Register 3.9010.2:0 can select any of the 5 jitter patterns specified by IEEE 802.3.

000 = Jitter 48A.1 (high freq)

001 = Jitter 48A.2 (low freq)

010 = Jitter 48A.3 (mix freq)

100 = Jitter 48A.4 (CRPAT)

101 = Jitter 48A.5 (CJPAT)

The transmit jitter pattern is enabled by setting 3.9010.4 to 1.

The 48A.1, 48A.2, and 48A.3 transmit patterns can also be enabled by setting register 3.1019.2 to 1 and selecting the pattern via register 3.1019.1:0.

There is a checker to check the CRPAT and CJPAT patterns. This is enabled by setting 3.9010.5 to 1.

Register 3.9011 and 3.9012 forms a 32 bit counter that increments once for every CRPAT or CJPAT packet transmitted. Register 3.9013 and 3.9014 forms a 32 bit counter that increments once for every CRPAT or CJPAT packet received. Register 3.9015 and 3.9016 forms a 32 bit counter that increments once for every CRPAT or CJPAT packet received with error.

The lower addressed register is the least significant 16 bits and the higher addressed register is the most significant 16 bits of the counter. When the least significant register is read, the upper register is updated and frozen so that the 2 register read is atomic. The counters can be cleared only by setting register 3.9010.7 to 1.

4.8 Interrupt

The Line PCS supports several interrupts. The interrupt enable, interrupt status, and real time status are shown in Table 50.

The INTn interrupt pin will be active if any of the events enabled in the interrupt enable register occurs. If an interrupt event corresponding to a disabled interrupt enable bit occurs, the corresponding interrupt status bit will be set even though the event does not activate the INTn pin. The interrupts are cleared after a read to the interrupt status register.

Table 50: Interrupt Registers

Type	Interrupt Enable	Interrupt Status	Real Time Status
10GBASE-R	3.8000	3.8001	3.8002
1000BASE-X	3.A001	3.A002	3.A003
40GBASE-R4	3.B001	3.B002	3.B003
Misc	3.F00A	3.F00B	

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5 Host Side Description

This section includes information on the following topics:

- Section 5.1, Host Electrical Interface
- Section 5.2, PCS
- Section 5.3, Loopback
- Section 5.4, Synchronizing FIFO
- Section 5.5, Power Management
- Section 5.6, Traffic Generation and Checking
- Section 5.7, PRBS and Pattern Generators
- Section 5.8, Interrupt

The host side interface is comprised of 8 differential input lanes MIP[7:0] / MIN[7:0] and 4 differential output lanes MOP[7:0] / MON[7:0]. They are designed to operate over short backplanes to the host device. In this document, each set of input / output lanes is referred to as lane M0, M1, M2, M3, M4, M5, M6, and M7.

These lanes can be arranged to form 4-ports of 1000BASE-X,10GBASE-R, and RXAUI, 2-ports of XAUI, and 40GBASE-R4.

The host side can also be configured to support redundant switches as described in Section 3.1.5, Host Side Lane Attachment, on page 46. In the redundant operation only 4 functional lanes are supported; hence, the lanes can be arranged to support 4-ports of 1000BASE-X and 10GBASE-R, 2-ports RXAUI, 1 port of XAUI, and 40GBASE-R4.

5.1 Host Electrical Interface

The input and output buffers of the SERDES interface are internally terminated by 50Ω impedance (100Ω differential). No external terminations are required.

The SERDES transmitter uses a 3 tap (1 pre-tap and 1 post-tap) FIR filter that is implemented for the purpose of channel equalization. The FIR tap can be manually adjusted to optimize the transmit eye over a particular channel.

The receiver performs clock and data recovery and de-serializes the data.

5.2 PCS

Each port supports a multiple number of different PCS. Section 3.1.2, PCS Operational Mode and Lane Attachment, on page 44 describes how to configure each port for the various PCS. This section focuses on the PCS itself.

5.2.1 40GBASE-R4

The 40GBASE-R4 PCS is available only on ports 0 and 2. Lanes M0 to M3 are used by port 0 and correspond to lanes 0 to 3. Lanes M4 to M7 are used by port 2 and correspond to lanes 0 to 3. These lanes are enabled by setting register 31.F002.6:0 to 0x70.

In all other respects, the 40GBASE-R4 functionality is identical to Section 4.2.1, 40GBASE-R4, on page 87 except the DEVAD is 4 instead of 3.

5.2.2 10GBASE-R

The 10GBASE-R PCS is available on all ports. It is enabled by setting register 31.F002.6:0 to 0x71.

If register 31.F402.9 is set to 1, then lanes M0 through M3 are used by port 0 through 3 respectively.

If register 31.F402.9 is set to 0, then lanes M0, M2, M4, M6 are used by port 0 through 3 respectively.

In all other respects, the 10GBASE-R functionality is identical to Section 4.2.2, 10GBASE-R, on page 88 except the DEVAD is 4 instead of 3.

5.2.3 XAUI

The XAUI PCS is available only on ports 0 and 2. It is enabled by setting register 31.F002.6:0 to 0x73.

Normally, lanes M0 to M3 are used by port 0 and correspond to lanes 0 to 3, and lanes M4 to M7 are used by port 2 and correspond to lanes 4 to 7. However, if register 4.9000.7 is set to 1, then the lane order will be reversed with lanes M3 to M0 used by port 0 and corresponding to lanes 0 to 3, and lanes M7 to M4 are by port 2 and corresponding to lanes 4 to 7. The reverse lane order configuration only applies to the PCS. Access for all PMA registers is not lane reversed.

In all other respects, XAUI functionality is identical to Section 4.2.3, 1000BASE-X, on page 88 except the DEVAD is 4 instead of 3.

5.2.4 1000BASE-X

The 1000BASE-X PCS is available on all ports. There are several modes of 1000BASE-X.

It is enabled by setting register 31.F002.6:0 to 1 of the following values.

- 0x7A = 1000BASE-X, 1000BASE-X Auto-Negotiation off
- 0x7B = 1000BASE-X, 1000BASE-X Auto-Negotiation on
- 0x7C = SGMII (system), SGMII Auto-Negotiation off
- 0x7D = SGMII (system), SGMII Auto-Negotiation on
- 0x7E = SGMII (media), SGMII Auto-Negotiation off
- 0x7F = SGMII (media), SGMII Auto-Negotiation on

If register 31.F402.8 is set to 1, then lanes M0 through M3 are used by port 0 through 3 respectively.

If register 31.F402.8 is set to 0, then lanes M0, M2, M4, M6 are used by port 0 through 3 respectively.

In all other respects, the 1000BASE-X functionality is identical to Section 4.2.3, 1000BASE-X, on page 88 except the DEVAD is 4 instead of 3.

5.3 Loopback

The host side SERDES supports 2 loopback paths.

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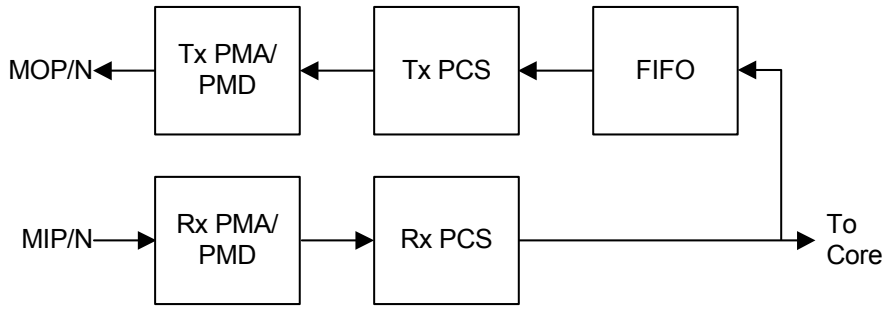
If register 4.F003.12 = 1, then data from the host will loopback to the host as shown in Figure 28.

Figure 28: Shallow Host Loopback



Registers 4.0000.14, 4.1000.14, 4.2000.14, and 4.3000.14 are physically the same bit. If any of these bits are set to 1, then data from the core will loopback to the core as shown in Figure 29 and Figure 30. If register 4.F003.6 = 0, then the ingress path will not be blocked as shown in Figure 29. If register 4.F003.6 = 1, then the ingress path will be blocked as shown in Figure 30.

Figure 29: Deep Line Loopback, No Ingress Blocking

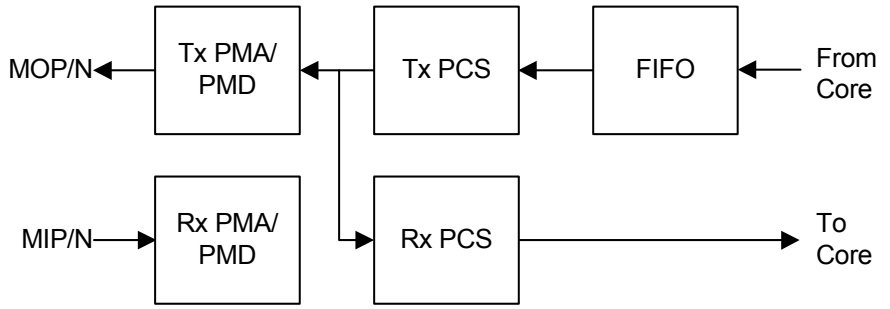
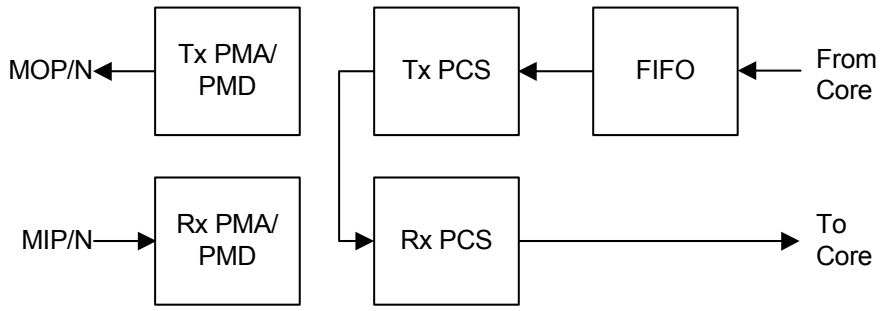


Figure 30: Deep Line Loopback, Ingress Blocking



5.4 Synchronizing FIFO

Each port has a transmit synchronizing FIFOs to reconcile frequency differences between the internal bus clocks and the clock used to transmit data onto the host interface. The depth of the FIFO can be programmed by setting register 4.F00C.15:14.

The FIFO depths can be increased in length to support longer frames. The device has settings for maximum frame sizes of:

- 10 KBs, 20 KBs, 40 KBs, and 80 KBs with up to ± 100 ppm clock jitter in 10 Gbps operation and
- 10 KBs, 15 KBs, 20 KBs, and 25 KBs with up to ±100 ppm clock jitter in 1 Gbps operation

The deeper the FIFO depth, the higher the latency will be.

The FIFO overflow/underflow status is reported in register 4.F00B.1:0.

5.5 Power Management

The 88X2242 device will automatically power down unused circuits. The host side can be forced into a power down state by setting 4.0000.11, 4.1000.11, 4.2000.11, or 4.3000.11 to 1. Register 31.0xF003.6 can also be used to power down the host side port. Note that these power down registers are physically the same bit even though they reside in different locations. Since 31.0xF003.6 is physically a separate register bit, setting this bit won't be reflected into PCS power down bits mentioned above but will override them.

To soft reset only the host side, set registers 4.0000.15, 4.1000.15, 4.2000.15, or 4.3000.15. Register 31.F003.7 can also be used to soft reset the host side. Note that these software reset registers are physically the same bit even though they reside in different locations.

5.6 Traffic Generation and Checking

This section describes the generator and checker functions. All counters are 48 bits long. If register 4.F010.14 is set to 1, the counters clear on read. If register 4.F010.14 is set to 0, the counters will keep counting unto 4.F010.6 is set to 1 to clear the contents.

5.6.1 Packet Generator

A packet generator enables the device to generate traffic onto the host without the need to receive data from the media.

Register 4.F010.1 enables the internal packet generator.

Register 4.F016 specifies the number of bytes in the packet that is to be generated. This count includes the frame bytes but does not include the 4 byte CRC (unless it is appended - register 4.F011.3 = 0), the terminate symbol, nor the 8 preamble bytes. The length depends upon the register setting:

- If the register is set to 0x0000, then the length will be randomly selected between 64 to 1518 bytes.
- If the register is set to 0x0001, then the length will be randomly selected to be between 64 to 0x0FFF bytes.
- If the register is set to 0x0002, then the length will be 64 to 0x1FFF bytes,
- If the register is set to 0x0003, then the length will be 64 to 0x3FFF bytes,
- If the register is set to 0x0004, then the length will be 64 to 0x7FFF bytes,
- If the register is set to 0x0005, then the length will be 64 to 0xFFFF bytes.
- If the register is set to 0x0008 to 0xFFFF, then the number of bytes transmitted is fixed from 8 to 0xFFFF.

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Register 4.F017 specifies the number of packets to burst. 0x0000 means stop generation, 0xFFFF means continuously generate packets, 0x0001 to 0xFFFE means send a burst of 1 to 0xFFFE packets.

Register 4.F018 specifies the gap between packets. Each increment in the value increases the idle time by 4 bytes. 4.F018.14:0 specifies the upper limit of the gap. If 4.F018.15 is 0, then the lower limit for IPG is also specified by 4.F018.14:0; otherwise, a random gap between 1 x 4 bytes to 4.F018.14:0 x 4 bytes will be used. For the purposes of counting IPG, all lanes must be idle for it to be counted as an IPG. In other words, if the terminate symbol is in the XGMII word, then it does not count towards the IPG.

Register 4.F012 and 4.F013 specifies the initial value of the payload or the fixed value of the payload. The 4 bytes in this register corresponds to the first 4 bytes of the frame. Register 4.F011.7:4 specifies the behavior of the payload.

When 4.F011.7:4 = 000x, then registers 4.F012 and 4.F013 are used as the payload repeatedly.

When 4.F011.7:4 = 0010, then registers 4.F012 and 4.F013 are used as the payload repeatedly, but every other XGMII word should be inverted. That is, a payload of 034EA675 will result in a sequence of 034EA675, FCB1598A, 034EA675, FCB1598A, ….

When 4.F011.7:4 = 0011, then registers 4.F012 and 4.F013 are used as the payload repeatedly but inverted every second XGMII word. That is, a payload of 034EA675 will result in a sequence of 034EA675, 034EA675, FCB1598A, FCB1598A, 034EA675, 034EA675, FCB1598A, FCB1598A, ….

When 4.F011.7:4 = 0100, then registers 4.F012 and 4.F013 are used as the initial value, and each subsequent byte is shifted left bitwise. That is, a payload of 034EA675 will result in a sequence of 034EA675, 069C4DEA, 0C399AD5, 187235AB, ….

When 4.F011.7:4 = 0101, then registers 4.F012 and 4.F013 are used as the initial value, and each subsequent byte is shifted right bitwise.

When 4.F011.7:4 = 0110, then registers 4.F012 and 4.F013 are used as the initial value, and the subsequent 32 bits are shifted left bitwise. That is, a payload of C34EA675 will result in a sequence of C34EA675, 869D4CEB, 0D3A99D7, 1A7533AE, ….

When 4.F011.7:4 = 0111, then registers 4.F012 and 4.F013 are used as the initial value, and the subsequent 32 bits are shifted right bitwise.

When 4.F011.7:4 = 1000, then registers 4.F012 and 4.F013 are used as the initial value and are subsequently bytewise incremented. That is, a payload of FFFE0055 will result in a sequence of FFFE0055, 00FF0156, 01000257, 02010358, ….

When 4.F011.7:4 = 1001, registers 4.F012 and 4.F013 are used as the initial value and are subsequently bytewise decremented.

When 4.F011.7:4 = 1000, registers 4.F012 and 4.F013 are ignored, and a pseudo random payload is generated. All 4 bytes are the same value for each cycle.

When 4.F011.7:4 = 1001, registers 4.F012 and 4.F013 are ignored, and a pseudo random payload is generated. All 4 bytes are randomly generated for each cycle.

At the start of each packet, registers 4.F012 and 4.F013 should be used to reset the initial values to ensure that the pattern in the packet is the same when repeated many times. The only time that the pattern in the packet will be different is when pseudo random generation is selected.

The following 48-bit counters are incremented by 1:

- For each packet generated, 4.F01B, 4.F01C, and 4.F01D
- For each byte generated, 4.F01E, 4.F01F, and 4.F020

  Preamble bytes are not counted but CRC bytes are counted.

Register 4.F011.3 controls whether the CRC is generated or not.

5.6.2 Checker

The CRC checker is enabled by setting register 4.F010.0 to 1.

If register 4.F010.2 = 0, the checker will wait until the SFD is detected to detect the frame boundary.

If register 4.F010.2 = 1, the checker will assume the first 8 bytes of the packet is the preamble, and the frame starts at the ninth byte of the packet.

There are 3 sets of 48-bit counters for the checker:

- Receive packet counter
  - Registers 4.F021, 4.F022, 4.F023
  - Counts the number of packets received regardless of whether there is a CRC error
- Receive packet error counter
  - Registers 4.F027, 4.F028, and 4.F029
  - Increments once per packet with a CRC error
- Receive byte counter
  - Registers 4.F024, 4.F025, and 4.F026
  - Counts the number of bytes in the frame including the CRC (note that preamble bytes are not counted)

5.7 PRBS and Pattern Generators

The device supports various IEEE-defined and proprietary PRBS generators and checkers, and transmit waveform pattern generators. Only 1 generator/checker per lane may be enabled simultaneously.

Caution If multiple generators are enabled simultaneously, unpredictable results may occur.

5.7.1 General PRBS Generators and Checkers

Each lane has its own general PRBS generator and checker:

- Port 0 registers control lanes 0 and 4
- Port 1 registers control lanes 1 and 5
- Port 2 registers control lanes 2 and 6
- Port 3 registers control lanes 3 and 7

For lanes 0 to 3, the functionality is identical to Section 4.7.1, General PRBS Generators and Checkers, on page 94 except the DEVAD is 4 instead of 3.

For lanes 4 to 7, the function of registers 4.F040 to 4.F049 is identical to registers 4.F030 to 4.F039 except the registers control a different lane.

5.7.2 40GBASE-R4-Specific Generators and Checkers

The functionality is identical to Section 4.7.2, 40GBASE-R4 Specific Generators and Checkers, on page 95 except the DEVAD is 4 instead of 3.

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5.7.3 10GBASE-R-Specific Generators and Checkers

The functionality is identical to Section 4.7.3, 10GBASE-R Specific Generators and Checkers, on page 95 except the DEVAD is 4 instead of 3.

5.7.4 XAUI-Specific Generators and Checkers

The functionality is identical to Section 4.7.4, XAUI Specific Generators and Checkers, on page 95 except the DEVAD is 4 instead of 3.

5.8 Interrupt

The Host PCS supports several interrupts. Table 51 shows the interrupt enable, interrupt status, and real time status.

The INTn interrupt pin will be active if any of the events enabled in the interrupt enable register occurs. If an interrupt event corresponding to a disabled interrupt enable bit occurs, the corresponding interrupt status bit will be set even though the event does not activate the INTn pin. The interrupts are cleared after a read to the interrupt status register.

Table 51: Interrupt Registers

Type	Interrupt		Real-Time Status
	Enable	Status	
10GBASE-R	4.8000	4.8001	4.8002
XAUI RXAUI	4.9001, 3.9002	4.9003, 4.9004	4.9006
1000BASE-X	4.A001	4.A002	4.A003
40GBASE-R4	4.B001	4.B002	4.B003
Misc	4.F00A	4.F00B	

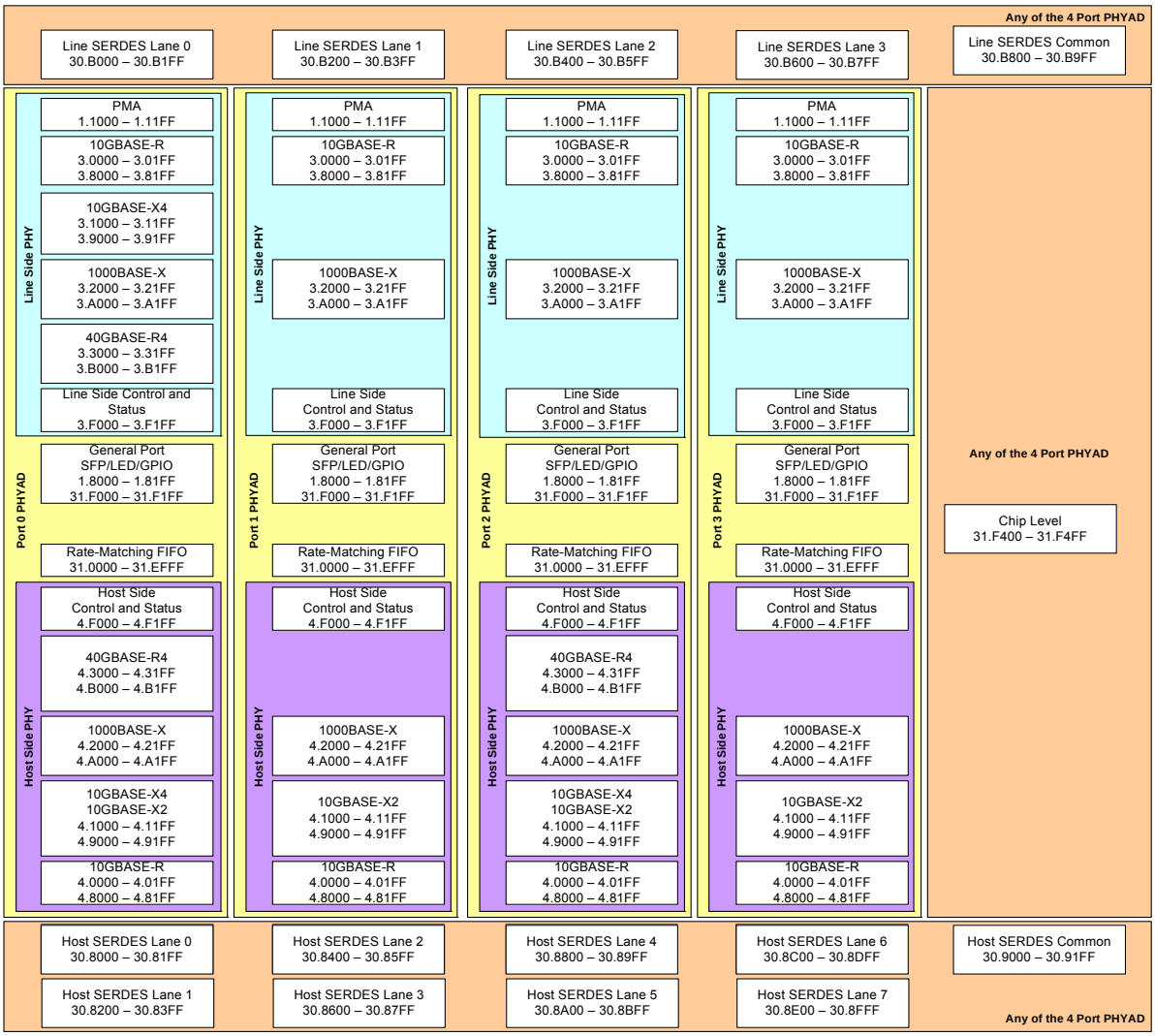
6 Register Description

This section includes information on the following topics:

- Section 6.1, Chip Level Registers
- Section 6.2, Port Level Registers
- Section 6.3, SFI Registers
- Section 6.4, XFI Registers

The registers are partitioned as shown in Figure 31.

Figure 31: 88X2242 Register Map Summary



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6.1 Chip Level Registers

The registers in this section are accessible through any of the 4 PHY addresses.

Table 52: Chip Level Registers - Register Map

Register Name	Register Address	Table and Page
Transmitter Source N	Device 31, Register 0xF400	Table 53, p. 105
Transmitter Source M	Device 31, Register 0xF401	Table 54, p. 106
Host Side Lane Muxing	Device 31, Register 0xF402	Table 55, p. 107
Chip Global Reset And Misc	Device 31, Register 0xF404	Table 56, p. 107
Host SERDES Lane Polarity Inversion	Device 31, Register 0xF406	Table 57, p. 107
Line SERDES Lane Polarity Inversion	Device 31, Register 0xF407	Table 58, p. 108
Recovered Clock and PCS_HW Reset Control	Device 31, Register 0xF408	Table 59, p. 109
Global Interrupt Status	Device 31, Register 0xF420	Table 60, p. 109
Global Interrupt Control	Device 31, Register 0xF421	Table 61, p. 110

Table 53: Transmitter Source N
Device 31, Register 0xF400

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	N3 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = M0 1001 = M1 1010 = M2 1011 = M3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1011.
11:8	N2 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = M0 1001 = M1 1010 = M2 1011 = M3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1010.
7:4	N1 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = M0 1001 = M1 1010 = M2 1011 = M3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1001.

Table 53: Transmitter Source N (Continued)
Device 31, Register 0xF400

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	N0 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = M0 1001 = M1 1010 = M2 1011 = M3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1000.

Table 54: Transmitter Source M
Device 31, Register 0xF401

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	M3 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = N0 1001 = N1 1010 = N2 1011 = N3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1011.
11:8	M2 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = N0 1001 = N1 1010 = N2 1011 = N3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1010.
7:4	M1 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = N0 1001 = N1 1010 = N2 1011 = N3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1001.
3:0	M0 Source	R/W	See Desc.	Retain	0000 = Output Powered Down 0001 = Output Idles 1000 = N0 1001 = N1 1010 = N2 1011 = N3 Else = Reserved On hardware reset will default to 0000 if PDOWN = 1 else 1000.

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Table 55: Host Side Lane Muxing
Device 31, Register 0xF402

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Update	Set to 0
11	RXAUI Attachment	R/W	0x0	Update	0 = Ports 0, 2 attached to logical lanes 0/1, 4/5 1 = Ports 0, 2 attached to logical lanes 0/1, 2/3
10	Reserved	R/W	0x0	Update	Set to 0
9	10BASE-R Attachment	R/W	0x0	Update	0 = Ports 0, 1, 2, 3 attached to logical lanes 0, 2, 4, 6 1 = Ports 0, 1, 2, 3 attached to logical lanes 0, 1, 2, 3
8	1000BASE-X Attachment	R/W	0x0	Update	0 = Ports 0, 1, 2, 3 attached to logical lanes 0, 2, 4, 6 1 = Ports 0, 1, 2, 3 attached to logical lanes 0, 1, 2, 3
7:0	Reserved	R/W	0x00	Update	Set to 0

Table 56: Chip Global Reset And Misc
Device 31, Register 0xF404

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Global Software Reset	W, SC	0x0	0x0	1 = Soft reset asserted for the whole chip
14	Global Hardware Reset	W,SC	0x0	0x0	1 = Hard reset asserted for the whole chip
13:9	Reserved	RO	0x00	0x00	0
8	Disable Fragment Packet Control	R/W	0x0	0x0	1 = Disable fragment packet control
7:0	Reserved	RO	0x00	0x00	Writing to this field is forbidden

Table 57: Host SERDES Lane Polarity Inversion
Device 31, Register 0xF406

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Invert Lane 7 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
14	Invert Lane 6 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
13	Invert Lane 5 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
12	Invert Lane 4 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
11	Invert Lane 3 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
10	Invert Lane 2 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
9	Invert Lane 1 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert

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Table 57: Host SERDES Lane Polarity Inversion (Continued)
Device 31, Register 0xF406

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Invert Lane 0 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
7	Invert Lane 7 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
6	Invert Lane 6 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
5	Invert Lane 5 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
4	Invert Lane 4 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
3	Invert Lane 3 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
2	Invert Lane 2 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
1	Invert Lane 1 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
0	Invert Lane 0 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert

Table 58: Line SERDES Lane Polarity Inversion
Device 31, Register 0xF407

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Set to 0s.
11	Invert Lane 3 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
10	Invert Lane 2 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
9	Invert Lane 1 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
8	Invert Lane 0 Input Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
7:4	Reserved	R/W	0x0	Retain	Set to 0s.
3	Invert Lane 3 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
2	Invert Lane 2 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert
1	Invert Lane 1 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert

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Table 58: Line SERDES Lane Polarity Inversion (Continued)
Device 31, Register 0xF407

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Invert Lane 0 Output Polarity	R/W	0x0	Retain	0 = Normal, 1 = Invert

Table 59: Recovered Clock and PCS_HW Reset Control
Device 31, Register 0xF408

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x0	0x0	Set to 0.
6:4	RCLK1 Control	R/W	0x0	Retain	000 = Low 100 = Output lane 0 recovered clock divided by 64 101 = Output lane 1 recovered clock divided by 64 110 = Output lane 2 recovered clock divided by 64 111 = Output lane 3 recovered clock divided by 64 Else = Reserved
3	Reserved	R/W	0x0	Retain	Set to 0.
2:0	RCLK0 Control	R/W	0x0	Retain	000 = Low 100 = Output lane 0 recovered clock divided by 64 101 = Output lane 1 recovered clock divided by 64 110 = Output lane 2 recovered clock divided by 64 111 = Output lane 3 recovered clock divided by 64 Else = Reserved

Table 60: Global Interrupt Status
Device 31, Register 0xF420

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	0
7	M3 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
6	M2 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
5	M1 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
4	M0 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
3	N3 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
2	N2 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
1	N1 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
0	N0 Interrupt Status	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt

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Table 61: Global Interrupt Control
Device 31, Register 0xF421

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SPEED_UP_TI_ TIMERS	R/W	0x0	Retain	When set, accelerates cunit timer
14:3	Reserved	RO	0x000	Retain	Set to 0s.
2:1	Interrupt Polarity	R/W	0x2	Retain	00 = Active - drive INT low, Inactive - drive INT high 01 = Active - drive INT high, Inactive - drive INT low 10 = Active - drive INT low, Inactive - tristate INT 11 = Active - drive INT high, Inactive - tristate INT
0	Force Interrupt Pin Active	R/W	0x0	Retain	0 = Normal operation 1 = Force interrupt pin active

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6.2 Port Level Registers

The registers in this section apply to all ports.

Table 62: Port Level Registers - Register Map

Register Name	Register Address	Table and Page
Two Wire Interface Caching Control/Status Register	Device 1, Register 0x8000	Table 63, p. 112
Two Wire Interface Memory Address Register	Device 1, Register 0x8001	Table 64, p. 113
Two Wire Interface Memory Read Data and Status Register	Device 1, Register 0x8002	Table 65, p. 113
Two Wire Interface Memory Write Data and Control Register	Device 1, Register 0x8003	Table 66, p. 114
Two Wire Interface Caching Delay	Device 1, Register 0x8004	Table 67, p. 115
EEPROM Cache Page A0	Device 1, Register 0x8007 to 8086	Table 68, p. 115
EEPROM Cache Page A2	Device 1, Register 0x8087 to 8106	Table 69, p. 115
Per Lane Clocking Configuration	Device 31, Register 0xF001	Table 70, p. 116
Port PCS Configuration	Device 31, Register 0xF002	Table 71, p. 116
Port Reset and Power Down	Device 31, Register 0xF003	Table 72, p. 117
GPIO Interrupt Enable	Device 31, Register 0xF010	Table 73, p. 117
GPIO Interrupt Status	Device 31, Register 0xF011	Table 74, p. 118
GPIO Data	Device 31, Register 0xF012	Table 75, p. 119
GPIO Tristate Control	Device 31, Register 0xF013	Table 76, p. 121
GPIO Interrupt Type 1	Device 31, Register 0xF014	Table 77, p. 122
GPIO Interrupt Type 2	Device 31, Register 0xF015	Table 78, p. 123
GPIO Interrupt Type 3	Device 31, Register 0xF016	Table 79, p. 124
Heartbeat Counter	Device 31, Register 0xF01F	Table 80, p. 125
LED0 Control	Device 31, Register 0xF020	Table 81, p. 125
LED1 Control	Device 31, Register 0xF021	Table 82, p. 126
MPC Control	Device 31, Register 0xF022	Table 83, p. 127
DSP_LOCK Control	Device 31, Register 0xF023	Table 84, p. 128
TX_DISABLED Control	Device 31, Register 0xF024	Table 85, p. 128
LED Mixing Control	Device 31, Register 0xF026	Table 86, p. 129
LED Timer Control	Device 31, Register 0xF027	Table 87, p. 130
Port Interrupt Status	Device 31, Register 0xF040	Table 88, p. 130

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Table 63: Two Wire Interface Caching Control/Status Register
Device 1, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Cache Valid Secondary Page	RO	0x0	0x0	0 = Registers 1.8087 to 1.8106 invalid 1 = Registers 1.8087 to 1.8106 valid This bit is set to 1 if at least one successful cache update is completed since hardware, software reset, or MOD0 transitions from 0 to 1. Use register 1.8000.14:13 for latest status.
14:13	Command Status Secondary Page	RO, SC	0x0	0x0	00 = Cache not updated since last read 01 = Contents in cache updated at least once since last read 10 = Cache is currently loading since last read 11 = All caching attempts since last read failed This register clears on read. Register 1.8000.15 indicates whether the content of the cache is valid from any updates in the past.
12:11	Cache Setting Secondary Page	R/W, SC	0x0	Retain	00 = No automatic caching 01 = Cache once at module plugin 10 = Cache at module plugin and periodically poll 11 = Manual cache refresh The page cached is selected by register 1.8004.7:0 This register will self clear when set to 11.
10	TWSI Reset	R/W, SC	0x0	0x0	0 = Normal operation 1 = Force TWSI circuit to reset
9	Cache Valid Page A0	RO	0x0	0x0	0 = Registers 1.8007 to 1.8086 invalid 1 = Registers 1.8007 to 1.8086 valid This bit is set to 1 if at least one successful cache update is completed since hardware, software reset, or MOD0 transitions from 0 to 1. Use register 1.8000.14:13 for latest status.
8:6	Reserved	RO	0x0	0x0	000
5	EEPROM Read/Write	RO	0x0	0x0	0 = Read. Writing from internal memory to EEPROM is not supported. Use registers 1.8001 and 1.8002 to write registers one by one if needed.
4	Reserved	RO	0x0	0x0	0
3:2	Command Status Page A0	RO, SC	0x0	0x0	00 = Cache not updated since last read 01 = Contents in cache updated at least once since last read 10 = Cache is currently loading since last read 11 = All caching attempts since last read failed This register clears on read. Register 1.8000.9 indicates whether the content of the cache is valid from any updates in the past.

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Table 63: Two Wire Interface Caching Control/Status Register (Continued)
Device 1, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
1:0	Cache Setting Page A0	R/W, SC	0x1	Retain	00 = No automatic caching 01 = Cache once at module plugin 10 = Cache at module plugin and periodically poll 11 = Manual cache refresh Page A0 lower 128 bytes are cached. This register will self clear when set to 11.

Table 64: Two Wire Interface Memory Address Register
Device 1, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Slave Address	R/W	0x50	Retain	Slave Address
8	Read/Write	R/W	0x1	Retain	A write to 1.8001 will initiate a read or write command on the two-wire interface if the two-wire interface is free, otherwise the read or write command will be ignored. Make sure register 1.8002.10:8 is not equal to 010 (command in progress) prior to writing register 1.8001. A read to 1.8001 will not trigger any action. Register 1.8003.7:0 must be set to the value to be written prior to issuing a write command. 1 = Read 0 = Write
7:0	Byte Address	R/W	0x00	Retain	Byte Address

Table 65: Two Wire Interface Memory Read Data and Status Register
Device 1, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0000
12	Cache ECC Single Bit Corrected Interrupt Status	RO, LH	0x0	0x0	0 = No single bit correction in ECC cache detected 1 = Single bit correction in ECC cache detected
11	Cache ECC Uncorrectable Bit Interrupt Status	RO, LH	0x0	0x0	0 = No uncorrectable bit in ECC cache detected 1 = Uncorrectable bit in ECC cache detected

Table 65: Two Wire Interface Memory Read Data and Status Register (Continued)
Device 1, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
10:8	TWSI Status	RO, LH	0x0	0x0	Register 1.8002.10:8 is the status in response to setting to writing register 1.8001. Register 1.8002.10:8 will remain at 010 until the command is completed. Once the command is completed the status 001, 011, 100, 101, or 111 will remain until register 1.8002 is read. The register will clear on read. If a new command is issued by writing register 1.8001 without reading register 1.8002 for a previous command, the status of the previous command will be lost. If a command initiated by writing register 1.8001 is still in progress and a second command is issued, the status register 1.8002.10:8 will reflect the first command. The second command is ignored but register 1.8002.10:8 will not be set to 111. Command Done - No Error is set when the TWSI slave properly responds with ACK. In the case of a write command with automatic read back a Command Done - No Error status will be returned even if the read back data does not match the written data or if the TWSI slave does not respond with ACK during the read back. Register 1.8002.7:0 is valid only when register 1.8002.10:8 is set to 001. 000 = Ready 001 = Command Done - No Error 010 = Command in Progress 011 = Write done but readback failed 100 = Reserved 101 = Command Failed 110 = Reserved 111 = Two-wire interface Busy, Command Ignored
7:0	Read Data	RO	0x00	0x00	Read Data Register 1.8002.7:0 is valid only when register 1.8002.10:8 is set to 001.

Table 66: Two Wire Interface Memory Write Data and Control Register
Device 1, Register 0x8003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Write Time	R/W	0xA	Retain	0000 = EEPROM takes 0ms to write 0001 = 1.05 ms .... 1110 = 14.68 ms 1111 = 15.73 ms
11:10	Reserved	R/W	0x0	0x0	Set to 0.
9	Automatic Read Back After Write	R/W	0x0	Retain	If read back is enabled then data will always be read back after a write. The read data is stored in register 1.8002.7:0 1 = Read back, 0 = No read back
8	Reserved	R/W	0x0	0x0	Set to 0.

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Table 66: Two Wire Interface Memory Write Data and Control Register (Continued)
Device 1, Register 0x8003

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Write Data	R/W	0x00	Retain	Write Data.

Table 67: Two Wire Interface Caching Delay
Device 1, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Auto Caching Delay	R/W	0x3	Retain	000 = No delay 001 = 0.25 Second 010 = 0.5 Second 011 = 1 Second 100 = 2 Seconds 101 = 4 Seconds 110 = 8 Seconds 111 = Auto Caching Disabled
12	Cache ECC Single Bit Corrected Interrupt Enable	R/W	0x0	Retain	0 = Interrupt disabled 1 = Interrupt enabled
11	Cache ECC Uncorrectable Bit Interrupt Enable	R/W	0x0	Retain	0 = Interrupt disabled 1 = Interrupt enabled
10:9	Page Reload Frequency	R/W	0x1	Retain	00 = 250 ms 01 = 500 ms 10 = 1 second 11 = 2 seconds
8	Reserved	R/W	0x0	Retain	Set to 0
7:1	Secondary Page	R/W	0x51	Retain	Seven bit slave address to use when loading 1.8087 to 1.8106.
0	Secondary Page Register Address MSB	R/W	0x0	Retain	0 = Lower 128 bytes of secondary page should be loaded 1 = Upper 128 bytes of secondary page should be loaded

Table 68: EEPROM Cache Page A0
Device 1, Register 0x8007 to 8086

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0
7:0	EEPROM Byte	RO	--	--	Byte (REGAD - 0x8007) Of EEPROM

Table 69: EEPROM Cache Page A2
Device 1, Register 0x8087 to 8106

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0
7:0	EEPROM Byte	RO	--	--	Byte (REGAD - 0x8087) Of EEPROM

Table 70: Per Lane Clocking Configuration
Device 31, Register 0xF001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	R/W	0x00	Update	Set to 0
9:8	Line Side Transmit Clocking	R/W	0x0	Update	00 = Local reference clock 01 = Host side recovered clock 10 = Line side recovered clock
1:0	Host Side Transmit Clocking	R/W	0x0	Update	00 = Local reference clock 01 = Host side recovered clock 10 = Line side recovered clock

Table 71: Port PCS Configuration
Device 31, Register 0xF002

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Set to 0.
14:8	Line Side PCS Select	R/W	0x71	Update	PCS Select Bits 14:12 must set 111 then bits 3:0 has the following meaning (Not all PCS available in all ports) 0000 = 40GBASE-R4 0001 = 10GBASE-R 0010 = Reserved 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = 1000BASE-X, 1000BASE_X autoneg off 1011 = 1000BASE-X, 1000BASE_X autoneg on 1100 = SGMII (MAC), SGMII autoneg off 1101 = SGMII (MAC), SGMII autoneg on 1110 = SGMII (Line), SGMII autoneg off 1111 = SGMII (Line), SGMII autoneg on Changes to this register will not take effect unless 31.F002.15 is issued.
7	Reserved	R/W	0x0	Retain	Set to 0.

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Table 71: Port PCS Configuration (Continued)
Device 31, Register 0xF002

Bits	Field	Mode	HW Rst	SW Rst	Description
6:0	Host Side PCS Select	R/W	0x71	Update	PCS Select Bits 6:4 must set 111 then bits 3:0 has the following meaning (Not all PCS available in all ports) 0000 = 40GBASE-R4 0001 = 10GBASE-R 0010 = RXAUI 0011 = XAUI 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = 1000BASE-X, 1000BASE_X autoneg off 1011 = 1000BASE-X, 1000BASE_X autoneg on 1100 = SGMII (MAC), SGMII autoneg off 1101 = SGMII (MAC), SGMII autoneg on 1110 = SGMII (Line), SGMII autoneg off 1111 = SGMII (Line), SGMII autoneg on Changes to this register will not take effect unless 31.F002.15 is issued.

Table 72: Port Reset and Power Down
Device 31, Register 0xF003

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Line Side Software Reset	R/W, SC	0x0	Update	0 = Normal Operation 1 = Reset
14	Line Side Power Down	R/W	0x0	Retain	0 = Power Up 1 = Power Down
13:8	Reserved	R/W	0x00	Retain	Set to 0s.
7	Host Side Software Reset	R/W, SC	0x0	Update	0 = Normal Operation 1 = Reset
6	Host Side Power Down	R/W	0x0	Retain	0 = Power Up 1 = Power Down
5:0	Reserved	R/W	0x00	Retain	Set to 0s.

Table 73: GPIO Interrupt Enable
Device 31, Register 0xF010

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Set to 0s.
11	SCL Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable

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Table 73: GPIO Interrupt Enable (Continued)
Device 31, Register 0xF010

Bits	Field	Mode	HW Rst	SW Rst	Description
10	SDA Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
9	Reserved	R/W	0x0	Retain	Set to 0s.
8	TX_DISABLE Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
7	DSP_LOCK Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
6	MPC Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
5	LED1 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
4	LED0 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
3	GPIO Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
2	RX_LOS Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
1	TX_FAULT Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
0	MOD_ABS Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable

Table 74: GPIO Interrupt Status
Device 31, Register 0xF011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11	SCL Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F016.15 = 1 and 31.F013.11 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
10	SDA Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F016.11 = 1 and 31.F013.10 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
9	Reserved	RO	0x0	Retain	0
8	TX_DISABLE Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F016.3 = 1 and 31.F013.8 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred

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Table 74: GPIO Interrupt Status (Continued)
Device 31, Register 0xF011

Bits	Field	Mode	HW Rst	SW Rst	Description
7	DSP_LOCK Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F015.15 = 1 and 31.F013.7 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
6	MPC Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F015.11 = 1 and 31.F013.6 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
5	LED1 Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F015.7 = 1 and 31.F013.5 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
4	LED0 Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F015.3 = 1 and 31.F013.4 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
3	GPIO Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F013.3 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
2	RX_LOS Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F013.2 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
1	TX_FAULT Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F013.1 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred
0	MOD_ABS Interrupt Status	RO, LH	0x0	Retain	This bit is not valid unless register 31.F013.0 = 0. 0 = No Interrupt Occurred 1 = Interrupt Occurred

Table 75: GPIO Data
Device 31, Register 0xF012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11	SCL Data	R/W	0x0	Retain	This bit has no effect unless register 31.F016.15 = 1. When 31.F013.11 = 0 a read to this register will reflect the state of the SCL pin, and a write will write the output register but have no effect on the SCL pin. When 31.F013.11 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the SCL pin.

Table 75: GPIO Data (Continued)
Device 31, Register 0xF012

Bits	Field	Mode	HW Rst	SW Rst	Description
10	SDA Data	R/W	0x0	Retain	This bit has no effect unless register 31.F016.11 = 1. When 31.F013.10 = 0 a read to this register will reflect the state of the SDA pin, and a write will write the output register but have no effect on the SDA pin. When 31.F013.10 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the SDA pin.
9	Reserved	RO	0x0	Retain	
8	TX_DISABLED Data	R/W	0x1	Retain	This bit has no effect unless register 31.F016.3 = 1. When 31.F013.8 = 0 a read to this register will reflect the state of the TX_DISABLED pin, and a write will write the output register but have no effect on the TX_DISABLED pin. When 31.F013.8 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the TX_DISABLED pin.
7	DSP_LOCK Data	R/W	0x0	Retain	This bit has no effect unless register 31.F015.15 = 1. When 31.F013.7 = 0 a read to this register will reflect the state of the DSP_LOCK pin, and a write will write the output register but have no effect on the DSP_LOCK pin. When 31.F013.7 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the DSP_LOCK pin.
6	MPC Data	R/W	0x0	Retain	This bit has no effect unless register 31.F015.11 = 1. When 31.F013.6 = 0 a read to this register will reflect the state of the MPC pin, and a write will write the output register but have no effect on the MPC pin. When 31.F013.6 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the MPC pin.
5	LED1 Data	R/W	0x0	Retain	This bit has no effect unless register 31.F015.7 = 1. When 31.F013.5 = 0 a read to this register will reflect the state of the LED1 pin, and a write will write the output register but have no effect on the LED1 pin. When 31.F013.5 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the LED1 pin.
4	LED0 Data	R/W	0x0	Retain	This bit has no effect unless register 31.F015.3 = 1. When 31.F013.4 = 0 a read to this register will reflect the state of the LED0 pin, and a write will write the output register but have no effect on the LED0 pin. When 31.F013.4 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the LED0 pin.

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Table 75: GPIO Data (Continued)
Device 31, Register 0xF012

Bits	Field	Mode	HW Rst	SW Rst	Description
3	GPIO Data	R/W	0x0	Retain	When 31.F013.3 = 0 a read to this register will reflect the state of the GPIO pin, and a write will write the output register but have no effect on the GPIO pin. When 31.F013.3 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the GPIO pin.
2	RX_LOS Data	R/W	0x0	Retain	When 31.F013.2 = 0 a read to this register will reflect the state of the RX_LOS pin, and a write will write the output register but have no effect on the RX_LOS pin. When 31.F013.2 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the RX_LOS pin.
1	TX_FAULT Data	R/W	0x0	Retain	When 31.F013.1 = 0 a read to this register will reflect the state of the TX_FAULT pin, and a write will write the output register but have no effect on the TX_FAULT pin. When 31.F013.1 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the TX_FAULT pin.
0	MOD_ABS Data	R/W	0x0	Retain	When 31.F013.0 = 0 a read to this register will reflect the state of the MOD_ABS pin, and a write will write the output register but have no effect on the MOD_ABS pin. When 31.F013.0 = 1 a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the MOD_ABS pin.

Table 76: GPIO Tristate Control
Device 31, Register 0xF013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11	SCL Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F016.15 = 1. 0 = Input 1 = Output
10	SDA Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F016.11 = 1. 0 = Input 1 = Output
9	Reserved	R/W	0x1	Retain	Set to 0.
8	TX_DISABLE Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F016.3 = 1. 0 = Input 1 = Output
7	DSP_LOCK Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F015.15 = 1. 0 = Input 1 = Output
6	MPC Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F015.11 = 1. 0 = Input 1 = Output

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Table 76: GPIO Tristate Control (Continued)
Device 31, Register 0xF013

Bits	Field	Mode	HW Rst	SW Rst	Description
5	LED1 Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F015.7 = 1. 0 = Input 1 = Output
4	LED0 Output Enable	R/W	0x1	Retain	This bit has no effect unless register 31.F015.3 = 1. 0 = Input 1 = Output
3	GPIO Output Enable	R/W	0x0	Retain	0 = Input 1 = Output
2	RX_LOS Output Enable	R/W	0x0	Retain	0 = Input 1 = Output
1	TX_FAULT Output Enable	R/W	0x0	Retain	0 = Input 1 = Output
0	MOD_ABS Output Enable	R/W	0x0	Retain	0 = Input 1 = Output

Table 77: GPIO Interrupt Type 1
Device 31, Register 0xF014

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Set to 0.
14:12	GPIO Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.3 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
11	RX_LOS Function	R/W	0x1	Retain	0 = RX_LOS is used as signal detect 1 = RX_LOS is used for GPIO Function.
10:8	RX_LOS Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.2 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
7	TX_FAULT Function	R/W	0x1	Retain	0 = TX_FAULT is status is indicated by 1.0008.11. 1 = TX_FAULT is used for GPIO Function.

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Table 77: GPIO Interrupt Type 1 (Continued)
Device 31, Register 0xF014

Bits	Field	Mode	HW Rst	SW Rst	Description
6:4	TX_FAULT Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.1 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
3	Reserved	RO	0x0	Retain	Set to 0.
2:0	MOD_ABS Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.0 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low

Table 78: GPIO Interrupt Type 2
Device 31, Register 0xF015

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DSP_LOCK Function	R/W	0x0	Retain	0 = DSP_LOCK is used for LED Function. 1 = DSP_LOCK is used for GPIO Function.
14:12	DSP_LOCK Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.7 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
11	MPC Function	R/W	0x1	Retain	0 = MPC is used for LED Function. 1 = MPC is used for GPIO Function.
10:8	MPC Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.6 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
7	LED1 Function	R/W	0x0	Retain	0 = LED1 is used for LED Function. 1 = LED1 is used for GPIO Function.

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Table 78: GPIO Interrupt Type 2 (Continued)
Device 31, Register 0xF015

Bits	Field	Mode	HW Rst	SW Rst	Description
6:4	LED1 Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.5 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
3	LED0 Function	R/W	0x0	Retain	0 = LED0 is used for LED Function. 1 = LED0 is used for GPIO Function.
2:0	LED0 Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.4 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low

Table 79: GPIO Interrupt Type 3
Device 31, Register 0xF016

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SCL Function	R/W	0x0	Retain	0 = SCL is used for TWSI Function. 1 = SCL is used for GPIO Function.
14:12	SCL Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.11 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
11	SDA Function	R/W	0x0	Retain	0 = SDA is used for TWSI Function. 1 = SDA is used for GPIO Function.
10:8	SDA Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.10 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low
7:5	Reserved	R/W	0x0	Retain	Set to 0

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Table 79: GPIO Interrupt Type 3 (Continued)
Device 31, Register 0xF016

Bits	Field	Mode	HW Rst	SW Rst	Description
4:3	TX_DISABLE Function	R/W	0x1	Retain	00 = TX_DISABLE is used for LED Function. 01 = TX_DISABLE is used for GPIO Function. 10 = TX_DISABLE is controlled by 1.0009.0.
2:0	TX_DISABLE Select	R/W	0x0	Retain	Interrupt is effective only when 31.F013.8 = 0. 000 = No Interrupt 001 = Reserved 010 = Interrupt on Low Level 011 = Interrupt on High Level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on Low to High or High to Low

Table 80: Heartbeat Counter
Device 31, Register 0xF01F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Heartbeat Counter Control	R/W	0x0	Retain	0 = bits 14:0 clear on read and saturates at 0x7FFF 1 = bits 14:0 does not clear on read and will rollover
14:0	Heartbeat Counter	R/W, SC	0x0000	0x0000	A write to this register will set the count value. Indicates the number of seconds that elapsed. The counter will self clear if bit 15 is set to 0.

Table 81: LED0 Control
Device 31, Register 0xF020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11:8	LED0 Blink Behavior	R/W	0x1	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1000 = Reserved 1001 = Reserved 1010 = Blink Mix 1011 = Solid Mix 11xx = Reserved

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Table 81: LED0 Control (Continued)
Device 31, Register 0xF020

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	LED0 Solid Behavior	R/W	0x6	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1xxx = Reserved
3	Reserved	R/W	0x0	Retain	Set to 0
2	LED0 Blink Rate Select	R/W	0x0	Retain	0 = Select Blink Rate 1 1 = Select Blink Rate 2
1:0	LED0 Polarity	R/W	0x0	Retain	00 = On - drive LED0 low, Off - drive LED0 high 01 = On - drive LED0 high, Off - drive LED0 low 10 = On - drive LED0 low, Off - tristate LED0 11 = On - drive LED0 high, Off - tristate LED0

Table 82: LED1 Control
Device 31, Register 0xF021

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11:8	LED1 Blink Behavior	R/W	0x1	Retain	Blink Behavior has higher priority. This register ignored if 31.F020.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
7:4	LED1 Solid Behavior	R/W	0x6	Retain	Blink Behavior has higher priority. This register ignored if 31.F020.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
3	Reserved	RO	0x0	Retain	Set to 0

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Table 82: LED1 Control (Continued)
Device 31, Register 0xF021

Bits	Field	Mode	HW Rst	SW Rst	Description
2	LED1 Blink Rate Select	R/W	0x0	Retain	This register ignored if 31.F020.11:10 = 10 (Dual Mode). 0 = Select Blink Rate 1 1 = Select Blink Rate 2
1:0	LED1 Polarity	R/W	0x0	Retain	00 = On - drive LED1 low, Off - drive LED1 high 01 = On - drive LED1 high, Off - drive LED1 low 10 = On - drive LED1 low, Off - tristate LED1 11 = On - drive LED1 high, Off - tristate LED1

Table 83: MPC Control
Device 31, Register 0xF022

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11:8	MPC Blink Behavior	R/W	0x0	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1000 = Reserved 1001 = Reserved 1010 = Blink Mix 1011 = Solid Mix 11xx = Reserved
7:4	MPC Solid Behavior	R/W	0x0	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 1xxx = Reserved
3	Reserved	RO	0x0	Retain	Set to 0
2	MPC Blink Rate Select	R/W	0x0	Retain	0 = Select Blink Rate 1 1 = Select Blink Rate 2
1:0	MPC Polarity	R/W	0x0	Retain	00 = On - drive MPC low, Off - drive MPC high 01 = On - drive MPC high, Off - drive MPC low 10 = On - drive MPC low, Off - tristate MPC 11 = On - drive MPC high, Off - tristate MPC

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Table 84: DSP_LOCK Control
Device 31, Register 0xF023

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Set to 0s.
11:8	DSP_LOCK Blink Behavior	R/W	0x0	Retain	Blink Behavior has higher priority. This register ignored if 31.F022.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
7:4	DSP_LOCK Solid Behavior	R/W	0x4	Retain	Blink Behavior has higher priority. This register ignored if 31.F022.11:10 = 10 (Dual Mode). 0000 = Solid Off 0001 = Line Side Transmit or Receive Activity 0010 = Line Side Transmit Activity 0011 = Line Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Line Side Link 0111 = Solid On 1xxx = Reserved
3	Reserved	RO	0x0	Retain	Set to 0
2	DSP_LOCK Blink Rate Select	R/W	0x0	Retain	This register ignored if 31.F022.11:10 = 10 (Dual Mode). 0 = Select Blink Rate 1 1 = Select Blink Rate 2
1:0	DSP_LOCK Polarity	R/W	0x0	Retain	00 = On - drive DSP_LOCK low, Off - drive DSP_LOCK high 01 = On - drive DSP_LOCK high, Off - drive DSP_LOCK low 10 = On - drive DSP_LOCK low, Off - tristate DSP_LOCK 11 = On - drive DSP_LOCK high, Off - tristate DSP_LOCK

Table 85: TX_DISABLED Control
Device 31, Register 0xF024

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Set to 0s.

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Table 85: TX_DISABLED Control (Continued)
Device 31, Register 0xF024

Bits	Field	Mode	HW Rst	SW Rst	Description
11:8	TX_DISABLED Blink Behavior	R/W	0x0	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = System Side Transmit or Receive Activity 0010 = System Side Transmit Activity 0011 = System Side Receive Activity 0100 = Reserved 0101 = Reserved 0110 = System Side Link 0111 = Solid On 11xx = Reserved
7:4	TX_DISABLED Solid Behavior	R/W	0x0	Retain	Blink Behavior has higher priority. 0000 = Solid Off 0001 = Transmit or Receive Activity 0010 = Transmit Activity 0011 = Receive Activity 0100 = Reserved 0101 = Reserved 0110 = Link 0111 = Solid On 1xxx = Reserved
3	Reserved	RO	0x0	Retain	Set to 0
2	TX_DISABLED Blink Rate Select	R/W	0x0	Retain	0 = Select Blink Rate 1 1 = Select Blink Rate 2
1:0	TX_DISABLED Polarity	R/W	0x0	Retain	00 = On - drive TX_DISABLED low, Off - drive TX_DISABLED high 01 = On - drive TX_DISABLED high, Off - drive TX_DISABLED low 10 = On - drive TX_DISABLED low, Off - tristate TX_DISABLED 11 = On - drive TX_DISABLED high, Off - tristate TX_DISABLED

Table 86: LED Mixing Control
Device 31, Register 0xF026

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	Set to 0s.
7:4	DSP_LOCK, LED1 Mix Percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%,.., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
3:0	MPC, LED0 Mix Percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%,..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved

Table 87: LED Timer Control
Device 31, Register 0xF027

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Set to 0.
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = no pulse stretching 001 = 20 ms to 40 ms 010 = 40 ms to 81 ms 011 = 81 ms to 161 ms 100 = 161 ms to 322 ms 101 = 322 ms to 644 ms 110 = 644 ms to 1.3 s 111 = 1.3 s to 2.6 s
11	Reserved	RO	0x0	Retain	Set to 0.
10:8	Blink Rate 2	R/W	0x5	Retain	000 = 40 ms 001 = 81 ms 010 = 161 ms 011 = 322 ms 100 = 644 ms 101 = 1.3s 110 = 2.6 s 110 = 5.2 s
7	Reserved	RO	0x0	Retain	Set to 0.
6:4	Blink Rate 1	R/W	0x1	Retain	000 = 40 ms 001 = 81 ms 010 = 161 ms 011 = 322 ms 100 = 644 ms 101 = 1.3s 110 = 2.6 s 110 = 5.2 s
3:0	Reserved	RO	0x0	Retain	Set to 0.

Table 88: Port Interrupt Status
Device 31, Register 0xF040

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	Retain	0
3	GPIO Interrupt	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
2	System Side PCS Interrupt	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt
1	Reserved	RO	0x0	Retain	0
0	Line Side PCS Interrupt	RO	0x0	Retain	0 = No Interrupt 1 = Active Interrupt

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6.3 SFI Registers

6.3.1 SFI PMA

The registers in this section apply to all ports. However, descriptions for Lanes 1, 2, and 3 may not be applicable depending on the PCS setting.

Table 89: SFI PMA Registers - Register Map

Register Name	Register Address	Table and Page
PMA/PMD Control 1	Device 1, Register 0x0000	Table 90, p. 131
PMA/PMD Status 1	Device 1, Register 0x0001	Table 91, p. 132
PMA/PMD Device Identifier 1	Device 1, Register 0x0002	Table 92, p. 132
PMA/PMD Device Identifier 2	Device 1, Register 0x0003	Table 93, p. 133
PMA/PMD Speed Ability	Device 1, Register 0x0004	Table 94, p. 133
PMA/PMD Devices In Package 1	Device 1, Register 0x0005	Table 95, p. 133
PMA/PMD Devices In Package 2	Device 1, Register 0x0006	Table 96, p. 134
10G PMA/PMD Control 2	Device 1, Register 0x0007	Table 97, p. 134
PMA/PMD Status 2	Device 1, Register 0x0008	Table 98, p. 135
PMD Transmit Disable	Device 1, Register 0x0009	Table 99, p. 135
PMD Receive Signal Detect	Device 1, Register 0x000A	Table 100, p. 136
PMA/PMD Extended Ability	Device 1, Register 0x000B	Table 101, p. 136
40G PMA/PMD Extended Ability	Device 1, Register 0x000D	Table 102, p. 137
PMA/PMD Package Identifier 1	Device 1, Register 0x000E	Table 103, p. 137
PMA/PMD Package Identifier 2	Device 1, Register 0x000F	Table 104, p. 138
BASE-R PMD Control Register	Device 1, Register 0x0096	Table 105, p. 138
BASE-R PMD Status Register	Device 1, Register 0x0097	Table 106, p. 138
Test Pattern Ability	Device 1, Register 0x05DC	Table 107, p. 139
PRBS Pattern Testing Control	Device 1, Register 0x05DD	Table 108, p. 139
Square Wave Testing Control	Device 1, Register 0x05E6	Table 109, p. 140
PRBS Rx Error Counter Lane 0	Device 1, Register 0x06A4	Table 110, p. 140
PRBS Rx Error Counter Lane 1	Device 1, Register 0x06A5	Table 111, p. 141
PRBS Rx Error Counter Lane 2	Device 1, Register 0x06A6	Table 112, p. 141
PRBS Rx Error Counter Lane 3	Device 1, Register 0x06A7	Table 113, p. 141

Table 90: PMA/PMD Control 1
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Reserved	RO	0x0	0x0	Set to 0
13	Speed Select	RO	0x1	0x1	This bit is ignored and is always set to 1

Table 90: PMA/PMD Control 1 (Continued)
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Reserved	RO	0x0	0x0	Set to 0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10:7	Reserved	RO	0x0	0x0	Set to 0s
6	Speed Select	RO	0x1	0x1	This bit is ignored and is always set to 1
5:2	Speed Select	RO	0x0	0x0	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1	PMA Remote Loopback	R/W	0x0	0x0	0 = Disable PMA remote loopback. Writing this register has no effect.
0	PMA Local Loopback	R/W	0x0	0x0	0 = Disable PMA local loopback. 1 = PMA shall loopback transmit data on the received path.

Table 91: PMA/PMD Status 1
Device 1, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	00000000
7	Fault	RO	0x0	0x0	1 = Fault condition 0 = No fault condition Bit 1.0001.7 = 1.0008.11 OR 1.0008.10
6:3	Reserved	RO	0x0	0x0	0000
2	Receive Link Status	RO, LL	0x0	0x0	1 = PMA/PMD link up 0 = PMA/PMD link down Bit 1.0001.2 is the inverse of 1.0008.10
1	Low Power Ability	RO	0x1	0x1	1 = PMA/PMD supports low power
0	Reserved	RO	0x0	0x0	0

Table 92: PMA/PMD Device Identifier 1
Device 1, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

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Table 93: PMA/PMD Device Identifier 2
Device 1, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 94: PMA/PMD Speed Ability
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	000000
9	100G Capable	RO	0x0	0x0	0 = PMA/PMD is not capable of operating at 100 Gbps
8	40G Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 40 Gbps
7	Reserved	RO	0x0	0x0	0
6	10M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Mbps
5	100M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 100 Mbps
4	1000M Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 1000 Mbps
3	Reserved	RO	0x0	0x0	0
2	10PASS-TS Capable	RO	0x0	0x0	0 = PMA/PMD is not capable of operating as 10PASS-TS
1	2BASE-TL Capable	RO	0x0	0x0	0 = PMA/PMD is not capable of operating as 2BASE-TL
0	10G Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 10 Gbps

Table 95: PMA/PMD Devices In Package 1
Device 1, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000
11	Separated PMA (4)	RO	0x0	0x0	1 = Separated PMA (4) present in package 0 = Separated PMA (4) not present in package
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package

Table 95: PMA/PMD Devices In Package 1 (Continued)
Device 1, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 96: PMA/PMD Devices In Package 2
Device 1, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 97: 10G PMA/PMD Control 2
Device 1, Register 0x0007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	Set to 0s.
5:0	PMA/PMD Type Selection	RO	0x00	0x00	This register is ignored. PMA is automatically set based on the mode selected in register 31.F002. PMD is based on the external optics used.

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Table 98: PMA/PMD Status 2
Device 1, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address
13	Transmit Fault Ability	RO	0x1	0x1	1 = PMA/PMD has ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have ability to detect a fault condition on the transmit path
12	Receive Fault Ability	RO	0x1	0x1	1 = PMA/PMD has ability to detect a fault condition on the receive path 0 = PMA/PMD does not have ability to detect a fault condition on the receive path
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault condition on transmit path 0 = No fault condition on transmit path
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault condition on receive path 0 = No fault condition on receive path
9	Extended Abilities	RO	0x1	0x1	1 = PMA/PMD has extended abilities listed in register 1.000B
8	PMD Transmit Disable Ability	RO	0x1	0x1	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path
7	10GBASE-SR Ability	RO	0x1	0x1	1 = Able 0 = Not able
6	10GBASE-LR Ability	RO	0x1	0x1	1 = Able 0 = Not able
5	10GBASE-ER Ability	RO	0x1	0x1	1 = Able 0 = Not able
4	10GBASE-LX4 Ability	RO	0x1	0x1	1 = Able 0 = Not able
3	10GBASE-SW Ability	RO	0x1	0x1	1 = Able 0 = Not able
2	10GBASE-LW Ability	RO	0x1	0x1	1 = Able 0 = Not able
1	10GBASE-EW Ability	RO	0x1	0x1	1 = Able 0 = Not able
0	PMA Local Loopback Ability	RO	0x1	0x1	1 = Able 0 = Not able

Table 99: PMD Transmit Disable
Device 1, Register 0x0009

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Set to 00000000000 Software reset is defined to be 1.0000.15 only.

Table 99: PMD Transmit Disable (Continued)
Device 1, Register 0x0009

Bits	Field	Mode	HW Rst	SW Rst	Description
4	PMD Transmit Disable Lane 3	R/W	0x0	0x0	0 = Enable transmitter 1 = Disable transmitter This register is ignored if the PCS does not require lane 3.
3	PMD Transmit Disable Lane 2	R/W	0x0	0x0	0 = Enable transmitter 1 = Disable transmitter This register is ignored if the PCS does not require lane 2.
2	PMD Transmit Disable Lane 1	R/W	0x0	0x0	0 = Enable transmitter 1 = Disable transmitter This register is ignored if the PCS does not require lane 1.
1	PMD Transmit Disable Lane 0	R/W	0x0	0x0	0 = Enable transmitter 1 = Disable transmitter
0	Global PMD Transmit Disable	R/W	0x0	0x0	0 = Enable transmitter 1 = Disable transmitter

Table 100: PMD Receive Signal Detect
Device 1, Register 0x000A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	0
4	PMD Receive Signal Detect Disable Lane 3	RO	0x0	0x0	1 = Signal detected on receive 0 = Signal not detected on receive This register should be ignored if the PCS does not require lane 3.
3	PMD Receive Signal Detect Disable Lane 2	RO	0x0	0x0	1 = Signal detected on receive 0 = Signal not detected on receive This register should be ignored if the PCS does not require lane 2.
2	PMD Receive Signal Detect Disable Lane 1	RO	0x0	0x0	1 = Signal detected on receive 0 = Signal not detected on receive This register should be ignored if the PCS does not require lane 1.
1	PMD Receive Signal Detect Disable Lane 0	RO	0x0	0x0	1 = Signal detected on receive 0 = Signal not detected on receive
0	Global PMD Receive Signal Detect	RO	0x0	0x0	1 = Signal detected on receive 0 = Signal not detected on receive

Table 101: PMA/PMD Extended Ability
Device 1, Register 0x000B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	0

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Table 101: PMA/PMD Extended Ability (Continued)
Device 1, Register 0x000B

Bits	Field	Mode	HW Rst	SW Rst	Description
10	40G/100G Extended Abilities	RO	0x1	0x1	1 = PMA/PMD has 40G/100G extended abilities listed in register 1.000C
9	Reserved	RO	0x0	0x0	0
8	10BASE-T	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10BASE-T
7	100BASE-TX	RO	0x0	0x0	0 = PMA/PMD is not able to perform 100BASE-TX
6	1000BASE-KX	RO	0x1	0x1	1 = PMA/PMD is able to perform 1000BASE-KX
5	1000BASE-T	RO	0x0	0x0	0 = PMA/PMD is not able to perform 1000BASE-T
4	10GBASE-KR	RO	0x1	0x1	1 = PMA/PMD is able to perform 10GBASE-KR
3	10GBASE-KX4	RO	0x1	0x1	1 = PMA/PMD is able to perform 10GBASE-KX4
2	10GBASE-T	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-T
1	10GBASE-LRM	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-LRM
0	10GBASE-CX4	RO	0x1	0x1	1 = PMA/PMD is able to perform 10GBASE-CX4

Table 102: 40G PMA/PMD Extended Ability
Device 1, Register 0x000D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PMA Remote loopback ability	RO	0x0	0x0	1 = PMA has the ability ti perform a remote loopback function 0 = PMA doesn't have the ability ti perform a remote loopback function
14:4	Reserved	RO	0x000	0x000	0
3	40GBASE-LR4	RO	0x1	0x1	1 = PMA/PMD is able to perform 40GBASE-LR4
2	40GBASE-SR4	RO	0x1	0x1	1 = PMA/PMD is able to perform 40GBASE-SR4
0	40GBASE-KR4	RO	0x1	0x1	1 = PMA/PMD is able to perform 40GBASE-KR4

Table 103: PMA/PMD Package Identifier 1
Device 1, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 104: PMA/PMD Package Identifier 2
Device 1, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 105: BASE-R PMD Control Register
Device 1, Register 0x0096

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	0000
1	Training Enable	R/W	0x0	Retain	1 = Enable BASE-R start-up protocol 0 = Disable BASE-R start-up protocol
0	Restart Training	R/W, SC	0x0	Retain	1 = Reset BASE-R start-up protocol 0 = Normal operation

Table 106: BASE-R PMD Status Register
Device 1, Register 0x0097

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Training Failure 3	RO	0x0	Retain	1 = Training failure has been detected for lane 3 0 = Training failure has not been detected for lane 3
14	Start-Up Protocol Status 3	RO	0x0	Retain	1 = Start-up protocol in progress for lane 3 0 = Start-up protocol complete for lane 3
13	Frame Lock 3	RO	0x0	Retain	1 = Training frame delineation detected for lane 3 0 = Training frame delineation not detected for lane 3
12	Receiver Status 3	RO	0x0	Retain	1 = Receiver trained and ready to receive data for lane 3 0 = Receiver training for lane 3
11	Training Failure 2	RO	0x0	Retain	1 = Training failure has been detected for lane 2 0 = Training failure has not been detected for lane 2
10	Start-Up Protocol Status 2	RO	0x0	Retain	1 = Start-up protocol in progress for lane 2 0 = Start-up protocol complete for lane 2
9	Frame Lock 2	RO	0x0	Retain	1 = Training frame delineation detected for lane 2 0 = Training frame delineation not detected for lane 2
8	Receiver Status 2	RO	0x0	Retain	1 = Receiver trained and ready to receive data for lane 2 0 = Receiver training for lane 2
7	Training Failure 1	RO	0x0	Retain	1 = Training failure has been detected for lane 1 0 = Training failure has not been detected for lane 1

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Table 106: BASE-R PMD Status Register (Continued)
Device 1, Register 0x0097

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Start-Up Protocol Status 1	RO	0x0	Retain	1 = Start-up protocol in progress for lane 1 0 = Start-up protocol complete for lane 1
5	Frame Lock 1	RO	0x0	Retain	1 = Training frame delineation detected for lane 1 0 = Training frame delineation not detected for lane 1
4	Receiver Status 1	RO	0x0	Retain	1 = Receiver trained and ready to receive data for lane 1 0 = Receiver training for lane 1
3	Training Failure 0	RO	0x0	Retain	1 = Training failure has been detected for lane 0 0 = Training failure has not been detected for lane 0
2	Start-Up Protocol Status 0	RO	0x0	Retain	1 = Start-up protocol in progress for lane 0 0 = Start-up protocol complete for lane 0
1	Frame Lock 0	RO	0x0	Retain	1 = Training frame delineation detected for lane 0 0 = Training frame delineation not detected for lane 0
0	Receiver Status 0	RO	0x0	Retain	1 = Receiver trained and ready to receive data for lane 0 0 = Receiver training for lane 0

Table 107: Test Pattern Ability
Device 1, Register 0x05DC

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	Square wave test ability	RO	0x1	0x1	1 = Square wave testing supported 0 = Square waver testing not supported
11:6	Reserved	RO	0x00	0x00	0
5	PRBS9 Tx generator Ability	RO	0x1	0x1	1 = PRBS9 Tx direction pattern generation supported 0 = PRBS9 Tx direction pattern generation not supported
4	PRBS9 Rx generator Ability	RO	0x0	0x0	1 = PRBS9 Rx direction pattern generation supported 0 = PRBS9 Rx direction pattern generation not supported
3	PRBS31 Tx generator Ability	RO	0x1	0x1	1 = PRBS31 Tx direction pattern generation supported 0 = PRBS31 Tx direction pattern generation not supported
2	PRBS31 Tx checker Ability	RO	0x0	0x0	1 = PRBS31 Tx direction pattern checker supported 0 = PRBS31 Tx direction pattern checker not supported
1	PRBS31 Rx generator Ability	RO	0x0	0x0	1 = PRBS31 Rx direction pattern generation supported 0 = PRBS31 Rx direction pattern generation not supported
0	PRBS31 Rx checker Ability	RO	0x1	0x1	1 = PRBS31 Rx direction pattern checker supported 0 = PRBS31 Rx direction pattern checker not supported

Table 108: PRBS Pattern Testing Control
Device 1, Register 0x05DD

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0

Table 108: PRBS Pattern Testing Control (Continued)
Device 1, Register 0x05DD

Bits	Field	Mode	HW Rst	SW Rst	Description
7	PRBS31 Pattern Enable	R/W	0x0	0x0	1 = Enable PRBS31 test-pattern 0 = Disable PRBS31 test-pattern
6	PRBS9 Pattern Enable	R/W	0x0	0x0	1 = Enable PRBS9 test-pattern 0 = Disable PRBS9 test-pattern
5:4	Reserved	RO	0x0	0x0	0
3	Tx generator Enable	R/W	0x0	0x0	1 = Enable Tx direction test-pattern generator 0 = Disable Tx direction test-pattern generator
2	Tx checker Enable	RO	0x0	0x0	1 = Enable Tx direction test-pattern checker 0 = Disable Tx direction test-pattern checker
1	Rx generator Enable	RO	0x0	0x0	1 = Enable Rx direction test-pattern generator 0 = Disable Rx direction test-pattern generator
0	Rx checker Enable	R/W	0x0	0x0	1 = Enable Rx direction test-pattern checker 0 = Disable Rx direction test-pattern checker

Table 109: Square Wave Testing Control
Device 1, Register 0x05E6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	Lane 3 SW enable	R/W	0x0	0x0	1 = Enable square wave on lane 3 0 = Disable square wave on lane 3
2	Lane 2 SW enable	R/W	0x0	0x0	1 = Enable square wave on lane 2 0 = Disable square wave on lane 2
1	Lane 1 SW enable	R/W	0x0	0x0	1 = Enable square wave on lane 1 0 = Disable square wave on lane 1
0	Lane 0 SW enable	R/W	0x0	0x0	1 = Enable square wave on lane 0 0 = Disable square wave on lane 0

Table 110: PRBS Rx Error Counter Lane 0
Device 1, Register 0x06A4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count [15:0]	RO	0x0	0x0	Increments by 1 for every bit error received per lane. This register clears on read and held at all ones in case of overflow.

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Table 111: PRBS Rx Error Counter Lane 1
Device 1, Register 0x06A5

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count [15:0]	RO	0x0	0x0	Increments by 1 for every bit error received per lane. This register clears on read and held at all ones in case of overflow.

Table 112: PRBS Rx Error Counter Lane 2
Device 1, Register 0x06A6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count [15:0]	RO	0x0	0x0	Increments by 1 for every bit error received per lane. This register clears on read and held at all ones in case of overflow.

Table 113: PRBS Rx Error Counter Lane 3
Device 1, Register 0x06A7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count [15:0]	RO	0x0	0x0	Increments by 1 for every bit error received per lane. This register clears on read and held at all ones in case of overflow.

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6.3.2 SFI 10GBASE-R PCS

The registers in this section apply to all ports.

Table 114: SFI 10GBASE-R PCS Registers - Register Map

Register Name	Register Address	Table and Page
10GBASE-R PCS Control 1	Device 3, Register 0x0000	Table 115, p. 142
10GBASE-R PCS Status 1	Device 3, Register 0x0001	Table 116, p. 143
PCS Device Identifier 1	Device 3, Register 0x0002	Table 117, p. 144
PCS Device Identifier 2	Device 3, Register 0x0003	Table 118, p. 144
PCS Speed Ability	Device 3, Register 0x0004	Table 119, p. 144
PCS Devices In Package 1	Device 3, Register 0x0005	Table 120, p. 144
PCS Devices In Package 2	Device 3, Register 0x0006	Table 121, p. 145
PCS Control 2	Device 3, Register 0x0007	Table 122, p. 145
10GBASE-R PCS Status 2	Device 3, Register 0x0008	Table 123, p. 145
PCS Package Identifier 1	Device 3, Register 0x000E	Table 124, p. 146
PCS Package Identifier 2	Device 3, Register 0x000F	Table 125, p. 146
PCS EEE Capability Register	Device 3, Register 0x0014	Table 126, p. 147
BASE-R PCS Status 1	Device 3, Register 0x0020	Table 127, p. 147
BASE-R PCS Status 2	Device 3, Register 0x0021	Table 128, p. 147
10GBASE-R PCS Test Pattern Seed A 0	Device 3, Register 0x0022	Table 129, p. 148
10GBASE-R PCS Test Pattern Seed A 1	Device 3, Register 0x0023	Table 130, p. 148
10GBASE-R PCS Test Pattern Seed A 2	Device 3, Register 0x0024	Table 131, p. 148
10GBASE-R PCS Test Pattern Seed A 3	Device 3, Register 0x0025	Table 132, p. 148
10GBASE-R PCS Test Pattern Seed B 0	Device 3, Register 0x0026	Table 133, p. 148
10GBASE-R PCS Test Pattern Seed B 1	Device 3, Register 0x0027	Table 134, p. 148
10GBASE-R PCS Test Pattern Seed B 2	Device 3, Register 0x0028	Table 135, p. 148
10GBASE-R PCS Test Pattern Seed B 3	Device 3, Register 0x0029	Table 136, p. 149
BASE-R PCS Test Pattern Control	Device 3, Register 0x002A	Table 137, p. 149
10GBASE-R PCS Test Pattern Error Counter	Device 3, Register 0x002B	Table 138, p. 149
10GBASE-R Interrupt Enable Register	Device 3, Register 0x8000	Table 139, p. 149
10GBASE-R Interrupt Status Register	Device 3, Register 0x8001	Table 140, p. 150
10GBASE-R PCS Real Time Status Register	Device 3, Register 0x8002	Table 141, p. 150

Table 115: 10GBASE-R PCS Control 1
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Loopback	R/W	0x0	0x0	1 = Loopback 0 = Normal

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Table 115: 10GBASE-R PCS Control 1 (Continued)
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
12	Reserved	RO	0x0	0x0	0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Clock Stoppable	R/W	0x0	0x0	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:7	Reserved	RO	0x0	0x0	000
6	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
5:2	Speed Select	RO	0x0	0x0	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1:0	Reserved	RO	0x0	0x0	00

Table 116: 10GBASE-R PCS Status 1
Device 3, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000000
11	TX LP Idle Received	RO/LH	0x0	0x0	1 = Tx PCS has received LP Idle 0 = LP Idle not received
10	Rx LP Idle Received	RO/LH	0x0	0x0	1 = Rx PCS has received LP Idle 0 = LP Idle not received
9	Tx LP Idle Indication	RO	0x0	0x0	1 = Tx PCS is currently receiving LP Idle 0 = Tx PCS is not currently receiving LP Idle
8	Rx LP Idle Indication	RO	0x0	0x0	1 = Rx PCS is currently receiving LP Idle 0 = Rx PCS is not currently receiving LP Idle
7	Fault	RO	0x0	0x0	1 = Fault condition 0 = No fault condition
6	Clock Stop Capable	RO	0x0	0x0	0 = Clock not stoppable
5:3	Reserved	RO	0x0	0x0	000
2	Link Status	RO, LL	0x0	0x0	1 = PCS link up 0 = PCS link down
1	Low Power Ability	RO	0x1	0x1	1 = PCS Supports Low Power
0	Reserved	RO	0x0	0x0	0

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Table 117: PCS Device Identifier 1
Device 3, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 118: PCS Device Identifier 2
Device 3, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 119: PCS Speed Ability
Device 3, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	100G Capable	RO	0x0	0x0	0 = Not capable of operating at 100 Gbps
2	40G Capable	RO	0x1	0x1	1 = Capable of operating at 40 Gbps
1	10PASS-TS/2BASE-TL Capable	RO	0x0	0x0	0 = Not capable of operating as the 10P/2B PCS
0	10G Capable	RO	0x1	0x1	1 = Capable of operating at 10Gbps

Table 120: PCS Devices In Package 1
Device 3, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	00000
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package

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Table 120: PCS Devices In Package 1 (Continued)
Device 3, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 121: PCS Devices In Package 2
Device 3, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 122: PCS Control 2
Device 3, Register 0x0007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2:0	PCS Type Selection	RO	0x0	0x0	This register is ignored. PCS is automatically set based on the mode selected in register 31.F002

Table 123: 10GBASE-R PCS Status 2
Device 3, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address

Table 123: 10GBASE-R PCS Status 2 (Continued)
Device 3, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
13:12	Reserved	RO	0x0	0x0	00
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault on transmit path, 0 = No fault
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault on receive path, 0 = No fault
9:6	Reserved	RO	0x0	0x0	0000000
5	100GBASE-R Capable	RO	0x0	0x0	1 = PCS is able to support 100GBASE-R PCS types 0 = PCS is not able to support 100GBASE-R PCS types
4	40GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 40GBASE-R PCS types 0 = PCS is not able to support 40GBASE-R PCS types
3	10GBASE-T Capable	RO	0x0	0x0	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	10GBASE-X Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types
0	10GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types

Table 124: PCS Package Identifier 1
Device 3, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 125: PCS Package Identifier 2
Device 3, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

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Table 126: PCS EEE Capability Register
Device 3, Register 0x0014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	0
6	10GBASE-KR EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KR
5	10GBASE-KX4 EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KX4
4	1000BASE-KX EEE	RO	0x0	0x0	1 = EEE is supported for 1000BASE-KX
3:0	Reserved	RO	0x0	0x0	0

Table 127: BASE-R PCS Status 1
Device 3, Register 0x0020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	10GBASE-R Receive Link Status	RO	0x0	0x0	1 = 10G BASE-R PCS receive link up 0 = 10G BASE-R PCS receive link down
11:4	Reserved	RO	0x00	0x00	0
3	PRBS9 Pattern Testing Ability	RO	0x1	0x1	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing
2	PRBS31 Pattern Testing Ability	RO	0x1	0x1	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing
1	10GBASE-R PCS High Bit Error Rate	RO	0x0	0x0	1 = 10G BASE-R PCS reporting high BER 0 = 10G BASE-R PCS not reporting high BER
0	10GBASE-R PCS Block Lock	RO	0x0	0x0	1 = 10G BASE-R PCS locked to received block 0 = 10G BASE-R PCS not locked

Table 128: BASE-R PCS Status 2
Device 3, Register 0x0021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Latched Block Lock	RO, LL	0x0	0x0	1 = PCS Has Block Lock 0 = PCS Does Not Have Block Lock
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS Has Reported High BER 0 = PCS Has Not Reported High BER
13:8	Bit Error Rate Counter	RO	0x00	0x00	Bit Error Rate Counter Counter clears on read. Counter will peg at all 1s.
7:0	Errored Blocks Counter	RO	0x00	0x00	Errored Blocks Counter Counter clears on read. Counter will peg at all 1s.

Table 129: 10GBASE-R PCS Test Pattern Seed A 0
Device 3, Register 0x0022

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed A 0	R/W	0x0000	0x0000	Test Pattern Seed A bits 0 to 15

Table 130: 10GBASE-R PCS Test Pattern Seed A 1
Device 3, Register 0x0023

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed A 1	R/W	0x0000	0x0000	Test Pattern Seed A bits 16 to 31

Table 131: 10GBASE-R PCS Test Pattern Seed A 2
Device 3, Register 0x0024

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed A 2	R/W	0x0000	0x0000	Test Pattern Seed A bits 32 to 47

Table 132: 10GBASE-R PCS Test Pattern Seed A 3
Device 3, Register 0x0025

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	000000
9:0	Test Pattern Seed A 3	R/W	0x000	0x000	Test Pattern Seed A bits 48 to 57

Table 133: 10GBASE-R PCS Test Pattern Seed B 0
Device 3, Register 0x0026

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed B 0	R/W	0x0000	0x0000	Test Pattern Seed B bits 0 to 15

Table 134: 10GBASE-R PCS Test Pattern Seed B 1
Device 3, Register 0x0027

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed B 1	R/W	0x0000	0x0000	Test Pattern Seed B bits 16 to 31

Table 135: 10GBASE-R PCS Test Pattern Seed B 2
Device 3, Register 0x0028

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Seed B 2	R/W	0x0000	0x0000	Test Pattern Seed B bits 32 to 47

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Table 136: 10GBASE-R PCS Test Pattern Seed B 3
Device 3, Register 0x0029

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	000000
9:0	Test Pattern Seed B 3	R/W	0x000	0x000	Test Pattern Seed B bits 48 to 57

Table 137: BASE-R PCS Test Pattern Control
Device 3, Register 0x002A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	0
6	PRBS9 Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Enable On Transmit Path 0 = Disable On Transmit Path
5	PRBS31 Receive Test Pattern Enable	R/W	0x0	0x0	1 = Enable On Receive Path 0 = Disable On Receive Path
4	PRBS31 Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Enable On Transmit Path 0 = Disable On Transmit Path
3	Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Enable 0 = Disable
2	Receive Test Pattern Enable	R/W	0x0	0x0	1 = Enable 0 = Disable
1	Test Pattern Select	R/W	0x0	0x0	1 = Square Wave 0 = Pseudo Random
0	Data Pattern Select	R/W	0x0	0x0	1 = Zeros Data Pattern 0 = LF Data Pattern

Table 138: 10GBASE-R PCS Test Pattern Error Counter
Device 3, Register 0x002B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Error Counter	RO	0x0000	0x0000	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s. In Pseudo-random test mode, it counts block errors. In PRBS31 test mode it counts bit errors at the PRBS31 pattern checker output.

Table 139: 10GBASE-R Interrupt Enable Register
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Set to 0
11	Local Fault Transmitted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 139: 10GBASE-R Interrupt Enable Register (Continued)
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Local Fault Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9:4	Reserved	R/W	0x00	Retain	Set to 0
3	Reserved	R/W	0x0	Retain	Set to 0
2	Link status change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	High BER Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Block Lock Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 140: 10GBASE-R Interrupt Status Register
Device 3, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO,LH	0x0	0x0	Set to 0
11	Local Fault Transmitted Interrupt	RO,LH	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitter
10	Local Fault Received Interrupt	RO,LH	0x0	0x0	1 = Local fault received 0 = No local fault received
9:4	Reserved	RO,LH	0x00	0x00	Set to 0
3	Reserved	RO,LH	0x0	0x0	Set to 0
2	Link status change Detected	RO,LH	0x0	0x0	1 = Link status changed detected 0 = Link status changed not detected
1	High BER Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
0	Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

Table 141: 10GBASE-R PCS Real Time Status Register
Device 3, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	Set to 0
11	Local Fault Transmitted Status	RO	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitted
10	Local Fault Received Status	RO	0x0	0x0	1 = Local fault received 0 = No local fault received
9:5	Reserved	RO	0x00	0x00	Set to 0

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Table 141: 10GBASE-R PCS Real Time Status Register (Continued)
Device 3, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Jit_0_lock	RO	0x0	0x0	1 = JIT 0 lock achieved
3	Jit_lf_lock	RO	0x0	0x0	1 = JIT local fault lock achieved
2	Link Status	RO	0x0	0x0	1 = 10GBASE-R link achieved 0 = No link
1	High BER Status	RO	0x0	0x0	1 = High BER 0 = No high BER
0	Lane 3 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

6.3.3 Line Side 1000BASE-X, SGMII PCS

The registers in this section apply to all ports.

Table 142: Line Side 1000BASE-X, SGMII PCS Registers - Register Map

Register Name	Register Address	Table and Page
1000BASE-X/SGMII Control Register	Device 3, Register 0x2000	Table 143, p. 152
1000BASE-X/SGMII Status Register	Device 3, Register 0x2001	Table 144, p. 153
PHY Identifier	Device 3, Register 0x2002	Table 145, p. 154
PHY Identifier	Device 3, Register 0x2003	Table 146, p. 154
1000BASE-X Auto-Negotiation Advertisement Register	Device 3, Register 0x2004	Table 147, p. 155
SGMII (Media side) Auto-Negotiation Advertisement Register	Device 3, Register 0x2004	Table 148, p. 156
SGMII (System side) Auto-Negotiation Advertisement Register	Device 3, Register 0x2004	Table 149, p. 156
1000BASE-X Link Partner Ability Register	Device 3, Register 0x2005	Table 150, p. 157
SGMII (Media side) Link Partner Ability Register	Device 3, Register 0x2005	Table 151, p. 158
SGMII (System side) Link Partner Ability Register	Device 3, Register 0x2005	Table 152, p. 158
1000BASE-X Auto-Negotiation Expansion Register	Device 3, Register 0x2006	Table 153, p. 159
1000BASE-X Next Page Transmit Register	Device 3, Register 0x2007	Table 154, p. 159
1000BASE-X Link Partner Next Page Register	Device 3, Register 0x2008	Table 155, p. 160
Extended Status Register	Device 3, Register 0x200F	Table 156, p. 160
1000BASE-X Timer Mode Select Register	Device 3, Register 0xA000	Table 157, p. 161
1000BASE-X Interrupt Enable Register	Device 3, Register 0xA001	Table 158, p. 161
1000BASE-X Interrupt Status Register	Device 3, Register 0xA002	Table 159, p. 162
1000ASE-X PHY Specific Status Register	Device 3, Register 0xA003	Table 160, p. 162

Table 143: 1000BASE-X/SGMII Control Register
Device 3, Register 0x2000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Loopback	R/W	See Desc.	Retain	1 = Loopback 0 = Normal
13	SGMII Speed (LSB)	R/W	See Desc.	Retain	This register is used to control SGMII speed only. (bit 6, bit 13) 00 = 10 Mbps, 01 = 100 Mbps, 10 = 1000 Mbps
12	1000BASE-X Auto-Negotiation Enable	R/W	See Desc.	Retain	If the value of this bit is Changed, the link will be broken and 1000BASE-X Auto-Negotiation restarted (bit 3.2000.9 is set to 1). 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

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Table 143: 1000BASE-X/SGMII Control Register (Continued)
Device 3, Register 0x2000

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Isolate	RO	0x0	0x0	The core bus is embedded hence this function is not supported
9	Restart 1000BASE-X Negotiation	R/W, SC	0x1	SC	Auto-Negotiation automatically restarts after hardware reset, software reset (3.2000.15) or Change in auto-negotiation enable (3.2000.12) regardless of whether or not the restart bit (3.2000.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 3.2000.12. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex Mode	RO	0x1	Retain	Writing this bit has no effect since only full-duplex mode is supported. 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	R/W	0x0	0x0	No effect since half-duplex not supported. 1 = Enable COL signal test 0 = Disable COL signal test
6	SGMII Speed Selection (MSB)	R/W	See Desc.	Retain	This register is used to control SGMII speed only. (bit 6, bit 13) 00 = 10 Mbps, 01 = 100 Mbps, 10 = 1000 Mbps
5:0	Reserved	RO	0x00	0x00	Always 0.

Table 144: 1000BASE-X/SGMII Status Register
Device 3, Register 0x2001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	0x0	0x0	0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex
8	Extended Status	RO	0x1	0x1	1 = Extended status information in Register 3.200F

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Table 144: 1000BASE-X/SGMII Status Register (Continued)
Device 3, Register 0x2001

Bits	Field	Mode	HW Rst	SW Rst	Description
7	Reserved	RO	0x0	0x0	Must always be 0.
6	MF Preamble Suppression	RO	0x1	0x1	1 = PHY accepts management frames with preamble suppressed
5	1000BASE-X Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled.
4	1000BASE-X Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII modes.
3	Auto-Negotiation Ability	RO	See Desc.	See Desc.	If register 3.F002.6= 1, then this bit is always 1, otherwise this bit is 0. 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation
2	1000BASE-X Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, read this register back-to-back. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Must be 0
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 145: PHY Identifier
Device 3, Register 0x2002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 146: PHY Identifier
Device 3, Register 0x2003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

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Table 147: 1000BASE-X Auto-Negotiation Advertisement Register
Device 3, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 3.2000.15) Restart Auto-Negotiation is asserted (Register 3.2000.9) Power down (Register 3.2000.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
14	Reserved	RO	Always 0	Always 0	0
13:12	Remote Fault 2/ Remote Fault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 3.2000.15) Re-start Auto-Negotiation is asserted (Register 3.2000.9) Power down (Register 3.2000.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	Always 000	Always 000	0
8:7	Pause	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 3.2000.15) Re-start Auto-Negotiation is asserted (Register 3.2000.9) Power down (Register 3.2000.11) transitions from power down to normal operation Link goes down 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	Retain	1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	RO	0x1	Retain	1 = Advertise 0 = Not advertised

Table 147: 1000BASE-X Auto-Negotiation Advertisement Register (Continued)
Device 3, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	Reserved	R/W	0x00	0x00	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 3.2000.15) Re-start Auto-Negotiation is asserted (Register 3.2000.9) Power down (Register 3.2000.11) transitions from power down to normal operation Link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

Table 148: SGMII (Media side) Auto-Negotiation Advertisement Register
Device 3, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is not up on the attached interface 1 = Link is up on the attached interface
14	Reserved	RO	0x0	0x0	0
13	Reserved	RO	0x0	0x0	0
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to half-duplex 1 = Interface Resolved to full-duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	0 = Disabled 1 = Enabled
8	Receive Pause	RO	0x0	0x0	0 = Disabled 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	0 = Copper media 1 = Fiber media
6:0	Reserved	RO	0x01	0x01	Always set to 0000001 as per the SGMII Specification

Table 149: SGMII (System side) Auto-Negotiation Advertisement Register
Device 3, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	0x0001	0x0001	Per SGMII Specification Always 0x0001

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Table 150: 1000BASE-X Link Partner Ability Register
Device 3, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:9
8:7	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved	RO	0x00	0x00	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bits 4:0 Must be 0

Table 151: SGMII (Media side) Link Partner Ability Register
Device 3, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Must be 0
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Received Code Word Bits 13:0 Must receive 00_0000_0000_0001 per SGMII spec

Table 152: SGMII (System side) Link Partner Ability Register
Device 3, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13 Must be 0
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the Link Partner is capable of full-duplex 0 = Copper Interface on the link partner is capable of half-duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = reserved
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto-Negotiation. Received Code Word Bit 9 0 = Disabled, 1 = Enabled

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Table 152: SGMII (System side) Link Partner Ability Register (Continued)
Device 3, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto-Negotiation. Received Code Word Bit 8 0 = Disabled, 1 = Enabled
7	Fiber/Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto-Negotiation. Received Code Word Bit 7 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x00	0x00	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bits 6:0 Must be 0000001

Table 153: 1000BASE-X Auto-Negotiation Expansion Register
Device 3, Register 0x2006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
3	Link Partner Next Page Able	RO	0x0	0x0	In SGMII mode this bit is always 0. In 1000BASE-X mode register 3.2006.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 3.2006.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 3.2000.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 154: 1000BASE-X Next Page Transmit Register
Device 3, Register 0x2007

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Register 7 only has effect in the 1000BASE-X mode. Transmit Code Word Bit 15

Table 154: 1000BASE-X Next Page Transmit Register (Continued)
Device 3, Register 0x2007

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 155: 1000BASE-X Link Partner Next Page Register
Device 3, Register 0x2008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register 8 only has effect in the 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 156: Extended Status Register
Device 3, Register 0x200F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	0x1	0x1	1 = 1000 BASE-X full-duplex capable 0 = Not 1000 BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	0x0	0x0	1 = 1000 BASE-X half-duplex capable 0 = Not 1000 BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = Not 1000 BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = Not 1000 BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

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Table 157: 1000BASE-X Timer Mode Select Register
Device 3, Register 0xA000

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	SGMII Autoneg Timer Select	R/W	0x0	Retain	Selects link_timer value in SGMII mode 00 = 1.6 ms 01 = 0.5 us 10 = 1 us 11 = 2 us
13	Serial Interface Auto-Negotiation Bypass Enable	R/W	0x1	Retain	Changes to this bit are disruptive to the normal operation; hence, any Changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
12:2	Reserved	RO	0x000	0x000	
1	Reserved	R/W	0x0	Retain	Reserved
0	Noise Filter	R/W	0x0	Retain	When set, noise filter is enabled.

Table 158: 1000BASE-X Interrupt Enable Register
Device 3, Register 0xA001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Set to 0
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Up to Link Down Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Link Down to Link Up Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:0	Reserved	R/W	0x00	Retain	Set to 0s

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Table 159: 1000BASE-X Interrupt Status Register
Device 3, Register 0xA002

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Up to Link Down Detected	RO,LH	0x0	0x0	1 = Link up to link down detected 0 = Link up to link down not detected
9	Link Down to Link Up Detected	RO,LH	0x0	0x0	1 = Link down to link up detected 0 = Link down to link up not detected
8	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
7	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
6:0	Reserved	RO	0x00	0x00	0000000

Table 160: 1000ASE-X PHY Specific Status Register
Device 3, Register 0xA003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	0x0	These status bits are valid only after resolved bit 3.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	0x0	This status bit is valid only after resolved bit 3.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled this bit is always 1. 1 = Resolved 0 = Not resolved
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down

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Table 160: 1000ASE-X PHY Specific Status Register (Continued)
Device 3, Register 0xA003

Bits	Field	Mode	HW Rst	SW Rst	Description
9:6	Reserved	RO	0x0	0x0	0
5	Sync Status	RO	0x0	0x0	1 = Sync 0 = No Sync
4	Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 3.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 3.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved	RO	0x0	0x0	00

6.3.4 SFI 40GBASE-R4 PCS

The registers in this section apply to port 0 for 40GBASE-R4 only.

Table 161: SFI 40GBASE-R4 Registers - Register Map

Register Name	Register Address	Table and Page
40GBASE-R4 PCS Control 1	Device 3, Register 0x3000	Table 162, p. 164
40GBASE-R4 PCS Status 1	Device 3, Register 0x3001	Table 163, p. 165
PCS Device Identifier 1	Device 3, Register 0x3002	Table 164, p. 166
PCS Device Identifier 2	Device 3, Register 0x3003	Table 165, p. 166
PCS Speed Ability	Device 3, Register 0x3004	Table 166, p. 166
PCS Devices In Package 1	Device 3, Register 0x3005	Table 167, p. 166
PCS Devices In Package 2	Device 3, Register 0x3006	Table 168, p. 167
PCS Control 2	Device 3, Register 0x3007	Table 169, p. 167
40GBASE-R4 PCS Status 2	Device 3, Register 0x3008	Table 170, p. 167
PCS Package Identifier 1	Device 3, Register 0x300E	Table 171, p. 168
PCS Package Identifier 2	Device 3, Register 0x300F	Table 172, p. 168
BASE-R Status1 Register	Device 3, Register 0x3020	Table 173, p. 169
BASE-R PCS Status 2	Device 3, Register 0x3021	Table 174, p. 169
40GBASE-R PCS Test Pattern Control	Device 3, Register 0x302A	Table 175, p. 169
40GBASE-R PCS Test Pattern Error Counter	Device 3, Register 0x302B	Table 176, p. 170
40GBASE-R PCS BER High Order Counter	Device 3, Register 0x302C	Table 177, p. 170
40GBASE-R PCS Errored Blocks High Order Counter	Device 3, Register 0x302D	Table 178, p. 170
Multi-lane BASE-R PCS Alignment Status 1	Device 3, Register 0x3032	Table 179, p. 170
Multi-lane BASE-R PCS Alignment Status 2	Device 3, Register 0x3034	Table 180, p. 171
BIP Error Counter Lanes 0 Register	Device 3, Register 0x30C8	Table 181, p. 171
BIP Error Counter Lanes 1 Register	Device 3, Register 0x30C9	Table 182, p. 171
BIP Error Counter Lanes 2 Register	Device 3, Register 0x30CA	Table 183, p. 172
BIP Error Counter Lanes 3 Register	Device 3, Register 0x30CB	Table 184, p. 172
Lanes 0 Mapping Register	Device 3, Register 0x3190	Table 185, p. 172
Lanes 1 Mapping Register	Device 3, Register 0x3191	Table 186, p. 172
Lanes 2 Mapping Register	Device 3, Register 0x3192	Table 187, p. 172
Lanes 3 Mapping Register	Device 3, Register 0x3193	Table 188, p. 172
40GBASE-R4 Interrupt enable Register	Device 3, Register 0xB001	Table 189, p. 173
40GBASE-R4 Interrupt Status Register	Device 3, Register 0xB002	Table 190, p. 174
40GBASE-R4 PCS Real Time Status Register	Device 3, Register 0xB003	Table 191, p. 175

Table 162: 40GBASE-R4 PCS Control 1
Device 3, Register 0x3000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.

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Table 162: 40GBASE-R4 PCS Control 1 (Continued)
Device 3, Register 0x3000

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Loopback	R/W	0x0	0x0	1 = Loopback 0 = Normal
13	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
12	Reserved	RO	0x0	0x0	Set to 0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Clock Stoppable	R/W	0x0	0x0	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:7	Reserved	RO	0x0	0x0	000
6	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
5:2	Speed Select	RO	0x3	0x3	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1:0	Reserved	RO	0x0	0x0	Set to 0s

Table 163: 40GBASE-R4 PCS Status 1
Device 3, Register 0x3001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000000
11	TX LP Idle Received	RO/LH	0x0	0x0	1 = Tx PCS has received LP Idle 0 = LP Idle not received
10	Rx LP Idle Received	RO/LH	0x0	0x0	1 = Rx PCS has received LP Idle 0 = LP Idle not received
9	Tx LP Idle Indication	RO	0x0	0x0	1 = Tx PCS is currently receiving LP Idle 0 = Tx PCS is not currently receiving LP Idle
8	Rx LP Idle Indication	RO	0x0	0x0	1 = Rx PCS is currently receiving LP Idle 0 = Rx PCS is not currently receiving LP Idle
7	Fault	RO	0x0	0x0	1 = Transmit or Receive fault condition 0 = No fault condition
6	Clock Stop Capable	RO	0x0	0x0	0 = Clock not stoppable
5:3	Reserved	RO	0x0	0x0	000
2	Link Status	RO, LL	0x0	0x0	1 = PCS link up 0 = PCS link down
1	Low Power Ability	RO	0x1	0x1	1 = PCS supports low power
0	Reserved	RO	0x0	0x0	0

Table 164: PCS Device Identifier 1
Device 3, Register 0x3002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 165: PCS Device Identifier 2
Device 3, Register 0x3003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 166: PCS Speed Ability
Device 3, Register 0x3004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	100G Capable	RO	0x0	0x0	0 = Not capable of operating at 100Gbps
2	40G Capable	RO	0x1	0x1	1 = Capable of operating at 40Gbps
1	10PASS-TS/2BASE-TL Capable	RO	0x0	0x0	0 = Not capable of operating as the 10P/2B PCS
0	10G Capable	RO	0x1	0x1	1 = Capable of operating at 10Gbps

Table 167: PCS Devices In Package 1
Device 3, Register 0x3005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	00000
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package

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Table 167: PCS Devices In Package 1 (Continued)
Device 3, Register 0x3005

Bits	Field	Mode	HW Rst	SW Rst	Description
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 168: PCS Devices In Package 2
Device 3, Register 0x3006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 169: PCS Control 2
Device 3, Register 0x3007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2:0	PCS Type	RO	0x4	0x4	This register is ignored. PCS is automatically set based on the mode selected in register 31.F002

Table 170: 40GBASE-R4 PCS Status 2
Device 3, Register 0x3008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address

Table 170: 40GBASE-R4 PCS Status 2 (Continued)
Device 3, Register 0x3008

Bits	Field	Mode	HW Rst	SW Rst	Description
13:12	Reserved	RO	0x0	0x0	00
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault on transmit path, 0 = No fault
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault on receive path, 0 = No fault
9:6	Reserved	RO	0x0	0x0	0000000
5	100GBASE-R Capable	RO	0x0	0x0	1 = PCS is able to support 100GBASE-R PCS types 0 = PCS is not able to support 100GBASE-R PCS types
4	40GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 40GBASE-R PCS types 0 = PCS is not able to support 40GBASE-R PCS types
3	10GBASE-T Capable	RO	0x0	0x0	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types
2	Reserved	RO	0x0	0x0	Reserved
1	10GBASE-X Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types
0	10GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types

Table 171: PCS Package Identifier 1
Device 3, Register 0x300E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 172: PCS Package Identifier 2
Device 3, Register 0x300F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

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Table 173: BASE-R Status1 Register
Device 3, Register 0x3020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	40G Rx Link Status	RO	0x0	0x0	1 = 40GBASE-R PCS receive link up 0 = 40GBASE-R PCS receive link down
11:4	Reserved	RO	0x00	0x00	0
3	10GBASE-R PRBS9 Test Ability	RO	0x1	0x1	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing
2	10GBASE-R PRBS31 Test Ability	RO	0x1	0x1	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing
1	40G PCS High BER	RO	0x0	0x0	1 = 40GBASE-R PCS reporting high BER 0 = 40GBASE-R PCS not reporting high BER
0	40G PCSR Block Lck	RO	0x0	0x0	1 = 40GBASE-R PCS locked to received block 0 = 40GBASE-R PCS not locked

Table 174: BASE-R PCS Status 2
Device 3, Register 0x3021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Latched Block Lock	RO, LL	0x0	0x0	1 = PCS Has Block Lock 0 = PCS Does Not Have Block Lock
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS Has Reported High BER 0 = PCS Has Not Reported High BER
13:8	Bit Error Rate Counter	RO	0x00	0x00	Bit Error Rate Counter Counter clears on read. Counter will peg at all 1s.
7:0	Errored Blocks	RO	0x00	0x00	Errored Blocks Counter Counter clears on read. Counter will peg at all 1s.

Table 175: 40GBASE-R PCS Test Pattern Control
Device 3, Register 0x302A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0
7	Scramble_idle Test Pattern Enable	R/W	0x0	0x0	1 = Enable On Transmit Path 0 = Disable On Transmit Path
6	PRBS9 Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
5	PRBS31 Receive Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
4	PRBS31 Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored.

Table 175: 40GBASE-R PCS Test Pattern Control (Continued)
Device 3, Register 0x302A

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored.
2	Receive Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored.
1	Test Pattern Select	RO	0x0	0x0	Write to this bit is ignored.
0	Data Pattern Select	RO	0x0	0x0	Write to this bit is ignored.

Table 176: 40GBASE-R PCS Test Pattern Error Counter
Device 3, Register 0x302B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Error Counter	RO	0x0000	0x0000	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s.

Table 177: 40GBASE-R PCS BER High Order Counter
Device 3, Register 0x302C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	BER High Order	RO	0x0000	0x0000	Bits 21:6 of 22-bit BER counter. Register 3.3021 should be read first. Counter clears on read of 3.3021. 22-bit Counter will peg at all 1s.

Table 178: 40GBASE-R PCS Errored Blocks High Order Counter
Device 3, Register 0x302D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	High Order Counter Present	RO	0x1	0x1	1 = High order counter is present
14	Reserved	RO	0x0	0x0	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s.
13:0	Errored Blocks High Order	RO	0x0000	0x0000	Bits 21:8 of 22-bits Errored Blocks Counter. Register 3.3021 should be read first. Counter clears on read of 3.3021. 22-bit Counter will peg at all 1s.

Table 179: Multi-lane BASE-R PCS Alignment Status 1
Device 3, Register 0x3032

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	
12	PCS Lane Alignment Status	RO	0x0	0x0	1 = PCS receive lanes locked and aligned 0 = PCS receive lanes not locked and aligned
11:4	Reserved	RO	0x00	0x00	

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Table 179: Multi-lane BASE-R PCS Alignment Status 1 (Continued)
Device 3, Register 0x3032

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Lane 3 Block Lock	RO	0x0	0x0	1 = Lane 3 is locked 0 = Lane 3 is not locked
2	Lane 2 Block Lock	RO	0x0	0x0	1 = Lane 2 is locked 0 = Lane 2 is not locked
1	Lane 1 Block Lock	RO	0x0	0x0	1 = Lane 1 is locked 0 = Lane 1 is not locked
0	Lane 0 Block Lock	RO	0x0	0x0	1 = Lane 0 is locked 0 = Lane 0 is not locked

Table 180: Multi-lane BASE-R PCS Alignment Status 2
Device 3, Register 0x3034

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	
3	Lane 3 Aligned	RO	0x0	0x0	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked
2	Lane 2 Aligned	RO	0x0	0x0	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked
1	Lane 1 Aligned	RO	0x0	0x0	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked
0	Lane 0 Aligned	RO	0x0	0x0	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked

Table 181: BIP Error Counter Lanes 0 Register
Device 3, Register 0x30C8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Bip Err Count	RO	0x0000	0x0000	Lane 0 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 182: BIP Error Counter Lanes 1 Register
Device 3, Register 0x30C9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 1 Bip Err Count	RO	0x0000	0x0000	Lane 1 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 183: BIP Error Counter Lanes 2 Register
Device 3, Register 0x30CA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 2 Bip Err Count	RO	0x0000	0x0000	Lane 2 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 184: BIP Error Counter Lanes 3 Register
Device 3, Register 0x30CB

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 3 Bip Err Count	RO	0x0000	0x0000	Lane 3 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 185: Lanes 0 Mapping Register
Device 3, Register 0x3190

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 0 Mapping	RO	0x00	0x00	PCS lane received in service interface lane 0. The content is valid when lane 0 aligned bit (3.3034.0) is set to one, and invalid otherwise.

Table 186: Lanes 1 Mapping Register
Device 3, Register 0x3191

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 1 Mapping	RO	0x00	0x00	PCS lane received in service interface lane 1. The content is valid when lane 1 aligned bit (3.3034.1) is set to one, and invalid otherwise.

Table 187: Lanes 2 Mapping Register
Device 3, Register 0x3192

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 2 Mapping	RO	0x00	0x00	PCS lane received in service interface lane 2. The content is valid when lane 2 aligned bit (3.3034.2) is set to one, and invalid otherwise.

Table 188: Lanes 3 Mapping Register
Device 3, Register 0x3193

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	

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Table 188: Lanes 3 Mapping Register (Continued)
Device 3, Register 0x3193

Bits	Field	Mode	HW Rst	SW Rst	Description
5:0	Lane 3 Mapping	RO	0x00	0x00	PCS lane received in service interface lane 3. The content is valid when lane 3 aligned bit (3.3034.3) is set to one, and invalid otherwise.

Table 189: 40GBASE-R4 Interrupt enable Register
Device 3, Register 0xB001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
10	Local Fault Received Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
9	Lane_alignment change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	Tx_Lane_cnt_err Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
7	JIT 0 Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
6	JIT Local-Fault Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
5	Link Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
4	High BER Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
3	Lane 3 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable

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Table 189: 40GBASE-R4 Interrupt enable Register (Continued)
Device 3, Register 0xB001

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Lane 2 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
1	Lane 1 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
0	Lane 0 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable

Table 190: 40GBASE-R4 Interrupt Status Register
Device 3, Register 0xB002

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Interrupt	RO,LH	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitter
10	Local Fault Received Interrupt	RO,LH	0x0	0x0	1 = Local fault received 0 = No local fault received
9	Lane_Alignment change Interrupt Enable	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	Tx_Lane_cnt_err Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
7	JIT 0 Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
6	JIT Local-Fault Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
5	Link Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
4	High BER Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
3	Lane 3 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

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Table 190: 40GBASE-R4 Interrupt Status Register (Continued)
Device 3, Register 0xB002

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Lane 2 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
1	Lane 1 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
0	Lane 0 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

Table 191: 40GBASE-R4 PCS Real Time Status Register
Device 3, Register 0xB003

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock Status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock Status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock Status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock Status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Status	RO	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitted
10	Local Fault Received Status	RO	0x0	0x0	1 = Local fault received 0 = No local fault received
9	Lane_Alignment Status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	TX_LANE_CNT_ERR Status	RO	0x0	0x0	1= TX Blk dist lane cnt error. If this is set, 40GBASE-R4 won't behave as desired. 0 = No error
7	JIT 0 Lock Status	RO	0x0	0x0	1 =JIT 0 lock achieved 0 = No JIT 0 lock
6	JIT Local-Fault Lock Status	RO	0x0	0x0	1 =JIT local fault lock achieved 0 = No local fault lock
5	Link Status	RO	0x0	0x0	1 = 40GBASE-R link achieved 0 = No link
4	High BER Status	RO	0x0	0x0	1 = High BER 0 = No high BER
3	Lane 3 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock
2	Lane 2 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

Table 191: 40GBASE-R4 PCS Real Time Status Register (Continued)
Device 3, Register 0xB003

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Lane 1 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock
0	Lane 0 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

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6.3.5 SFI Common Registers

The registers in this section apply to all ports.

Table 192: SFI Common Registers - Register Map

Register Name	Register Address	Table and Page
SERDES Control Register 1	Device 3, Register 0xF003	Table 193, p. 178
FIFO and CRC Interrupt Enable	Device 3, Register 0xF00A	Table 194, p. 178
FIFO and CRC Interrupt Status	Device 3, Register 0xF00B	Table 195, p. 178
PPM FIFO Control 1	Device 3, Register 0xF00C	Table 196, p. 179
Packet Generation Control 1	Device 3, Register 0xF010	Table 197, p. 179
Packet Generation Control 2	Device 3, Register 0xF011	Table 198, p. 180
Initial Payload 0-1/Packet Generation	Device 3, Register 0xF012	Table 199, p. 180
Initial Payload 2-3/Packet Generation	Device 3, Register 0xF013	Table 200, p. 180
Packet Generation Length	Device 3, Register 0xF016	Table 201, p. 180
Packet Generation Burst Sequence	Device 3, Register 0xF017	Table 202, p. 181
Packet Generation IPG	Device 3, Register 0xF018	Table 203, p. 181
Transmit Packet Counter [15:0]	Device 3, Register 0xF01B	Table 204, p. 181
Transmit Packet Counter [31:16]	Device 3, Register 0xF01C	Table 205, p. 181
Transmit Packet Counter [47:32]	Device 3, Register 0xF01D	Table 206, p. 181
Transmit Byte Counter [15:0]	Device 3, Register 0xF01E	Table 207, p. 182
Transmit Byte Counter [31:16]	Device 3, Register 0xF01F	Table 208, p. 182
Transmit Byte Counter [47:32]	Device 3, Register 0xF020	Table 209, p. 182
Receive Packet Counter [15:0]	Device 3, Register 0xF021	Table 210, p. 182
Receive Packet Counter [31:16]	Device 3, Register 0xF022	Table 211, p. 183
Receive Packet Counter [47:32]	Device 3, Register 0xF023	Table 212, p. 183
Receive Byte Count [15:0]	Device 3, Register 0xF024	Table 213, p. 183
Receive Byte Count [31:16]	Device 3, Register 0xF025	Table 214, p. 183
Receive Byte Count [47:32]	Device 3, Register 0xF026	Table 215, p. 184
Receive Packet Error Count [15:0]	Device 3, Register 0xF027	Table 216, p. 184
Receive Packet Error Count [31:16]	Device 3, Register 0xF028	Table 217, p. 184
Receive Packet Error Count [47:32]	Device 3, Register 0xF029	Table 218, p. 184
PRBS Control	Device 3, Register 0xF030	Table 219, p. 184
PRBS Symbol Tx Counter [15:0]	Device 3, Register 0xF031	Table 220, p. 185
PRBS Symbol Tx Counter [31:16]	Device 3, Register 0xF032	Table 221, p. 186
PRBS Symbol Tx Counter [47:32]	Device 3, Register 0xF033	Table 222, p. 186
PRBS Symbol Rx Counter [15:0]	Device 3, Register 0xF034	Table 223, p. 186
PRBS Symbol Rx Counter [31:16]	Device 3, Register 0xF035	Table 224, p. 186
PRBS Symbol Rx Counter [47:32]	Device 3, Register 0xF036	Table 225, p. 187
PRBS Error Count [15:0]	Device 3, Register 0xF037	Table 226, p. 187
PRBS Error Count [31:16]	Device 3, Register 0xF038	Table 227, p. 187
PRBS Error Count [47:32]	Device 3, Register 0xF039	Table 228, p. 187

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Table 192: SFI Common Registers - Register Map (Continued)

Register Name	Register Address	Table and Page
PRBS Elapse Timer	Device 3, Register 0xF03A	Table 229, p. 188
Power Management TX state control	Device 3, Register 0xF074	Table 230, p. 188

Table 193: SERDES Control Register 1
Device 3, Register 0xF003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	Set to 0s
13	Reserved	R/W	0x0	Retain	0
12	Line Loopback	R/W	0x0	0x0	1 = Enable Loopback 0 = Normal Operation
11	Reserved	RO	0x0	0x0	0
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Reserved	RO	0x0	0x0	0
8	Receiver Power Down	R/W	0x0	Retain	1 = Receiver Powered Down 0 = Receiver Can Power Up
7	Force Signal Detect	R/W	0x0	Retain	1 = Force signal detect to be good 0 = Normal Operation
6	Block Transmit On Loopback	R/W	0x0	Retain	0 = Do not block egress path 1 = Block egress path
5:0	Reserved	R/W	0x00	Retain	Set to 0s.

Table 194: FIFO and CRC Interrupt Enable
Device 3, Register 0xF00A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	Set to 0
2	CRC Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	FIFO Overflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	FIFO Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 195: FIFO and CRC Interrupt Status
Device 3, Register 0xF00B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0

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Table 195: FIFO and CRC Interrupt Status (Continued)
Device 3, Register 0xF00B

Bits	Field	Mode	HW Rst	SW Rst	Description
2	CRC Interrupt Status	RO,LH	0x0	0x0	This interrupt will be set only if the packet checker is enabled. 1 = CRC Error detected 0 = CRC error not detected
1	FIFO Overflow Status	RO,LH	0x0	0x0	1 = FIFO overflow occurred 0 = FIFO overflow did not occur
0	FIFO Underflow Status	RO,LH	0x0	0x0	1 = FIFO underflow occurred 0 = FIFO underflow did not occur

Table 196: PPM FIFO Control 1
Device 3, Register 0xF00C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	PPM FIFO Depth	R/W	0x0	0x0	PPM FIFO depth selection Default setting varies based on the PCS mode. 10GBASE-R, XAUI, RXAUI: 01 40GBASE-R4: 11 Else: 00
13:0	Reserved	RO	0x0000	0x0000	Set to 0s

Table 197: Packet Generation Control 1
Device 3, Register 0xF010

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Read Clear	R/W	0x0	Retain	1= Enable clear on read 0 = Use 3.F010.6 to clear counters
14:7	Reserved	R/W	0x00	0x00	Set to 0s.
6	Pkt-Gen/Chk Counter Reset	R/W, SC	0x0	0x0	This bit self clears after counters are cleared. 1 = Clear counters 0 = Normal Operation
5:3	Reserved	RO	0x0	0x0	0000
2	Use SFD in Checker	R/W	0x0	0x0	0 = Look for SFD before starting CRC checking 1 = Start CRC checking after the first 8 bytes in packet
1	Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Pkt generator enable 0 = Disable
0	Receive Test Pattern Enable	R/W	0x0	0x0	1 = Pkt checker enable 0 = Disable

Table 198: Packet Generation Control 2
Device 3, Register 0xF011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	Set to 0s
7:4	Internal Packet Generation Control	R/W	0x0	Retain	000x = No Mask 0010 = Invert every other word 0011 = 2 no invert, 2 invert 0100 = Left shift byte 0101 = Right shift byte 0110 = Left shift word 0111 = Right shift word 1000 = Increment byte 1001 = decrement byte 1010 = Pseudo random byte 1011 = Pseudo random word 11xx = reserved
3	CRC Generation	R/W	0x0	Retain	0 = On 1 = Off
2:0	Reserved	RO	0x0	Retain	Set to 0s

Table 199: Initial Payload 0-1/Packet Generation
Device 3, Register 0xF012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Byte 1	R/W	0x00	Retain	Initial payload value for byte 1
7:0	Byte 0	R/W	0x00	Retain	Initial payload value for byte 0

Table 200: Initial Payload 2-3/Packet Generation
Device 3, Register 0xF013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Byte 3	R/W	0x00	Retain	Initial payload value for byte 1
7:0	Byte 2	R/W	0x00	Retain	Initial payload value for byte 0

Table 201: Packet Generation Length
Device 3, Register 0xF016

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Number Of Bytes In Frame	R/W	0x0000	Retain	0000 = Random length between 64 bytes to 1518 bytes 0001 = Random length between 64 bytes to 0x0FFF bytes 0002 = Random length between 64 bytes to 0x1FFF bytes 0003 = Random length between 64 bytes to 0x3FFF bytes 0004 = Random length between 64 bytes to 0x7FFF bytes 0005 = Random length between 64 bytes to 0xFFFF bytes 0006 to 0007 = Undefined 0008 to FFFF = Length in number of bytes

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Table 202: Packet Generation Burst Sequence
Device 3, Register 0xF017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Number Of Packets To Send	R/W	0x0000	Retain	0000 = Stop generation 0001 to FFFE = Number of packets to send FFFF = Continuous

Table 203: Packet Generation IPG
Device 3, Register 0xF018

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Random IPG	R/W	0x0	Retain	0 = Fixed IPG per bits 14:0 1 = Random IPG from 5 bytes to value specified per bits 14:0
14:0	IPG Duration	R/W	0x0002	Retain	Each bit equals 4 bytes of idle

Table 204: Transmit Packet Counter [15:0]
Device 3, Register 0xF01B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [15:0]	RO	0x0000	0x0000	Counts the total number of packets transmitted. If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read.

Table 205: Transmit Packet Counter [31:16]
Device 3, Register 0xF01C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [31:16]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F01B first in order to update this register. This ensures that the 48 bit read is atomic.

Table 206: Transmit Packet Counter [47:32]
Device 3, Register 0xF01D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [47:32]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F01B first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 207: Transmit Byte Counter [15:0]
Device 3, Register 0xF01E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [15:0]	RO	0x0000	0x0000	Counts the total number of bytes in frame (including premable) transmitted. If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read.

Table 208: Transmit Byte Counter [31:16]
Device 3, Register 0xF01F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [13:16]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F01E first in order to update this register. This ensures that the 48 bit read is atomic.

Table 209: Transmit Byte Counter [47:32]
Device 3, Register 0xF020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [47:32]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F01E first in order to update this register. This ensures that the 48 bit read is atomic.

Table 210: Receive Packet Counter [15:0]
Device 3, Register 0xF021

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [15:0]	RO	0x0000	0x0000	Counts the total number of packets received. If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read.

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Table 211: Receive Packet Counter [31:16]
Device 3, Register 0xF022

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [31:16]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F021 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 212: Receive Packet Counter [47:32]
Device 3, Register 0xF023

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [47:32]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F021 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 213: Receive Byte Count [15:0]
Device 3, Register 0xF024

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [15:0]	RO	0x0000	0x0000	Counts the total number of bytes in frame (including premable) received. If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read.

Table 214: Receive Byte Count [31:16]
Device 3, Register 0xF025

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [31:16]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F024 first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 215: Receive Byte Count [47:32]
Device 3, Register 0xF026

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [47:32]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F024 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 216: Receive Packet Error Count [15:0]
Device 3, Register 0xF027

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [15:0]	RO	0x0000	0x0000	Counts the number of packets with CRC Error received. If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read.

Table 217: Receive Packet Error Count [31:16]
Device 3, Register 0xF028

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [31:16]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F027 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 218: Receive Packet Error Count [47:32]
Device 3, Register 0xF029

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [47:32]	RO	0x0000	0x0000	If 3.F010.14 = 0 then register does not clear on read. Cleared only when register 3.F010.6 transitions from 0 to 1. If 3.F010.14 = 1 then register clear on read. Must read register 3.F027 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 219: PRBS Control
Device 3, Register 0xF030

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	Set to 0s.
14	BER_mode_en	R/W	0x1	Retain	0 = Legacy mode of error count accumulation 1 = BER mode enabled for error accumulation. This is used for average Bit Error Rate (BER) calculation.

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Table 219: PRBS Control (Continued)
Device 3, Register 0xF030

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Read Clear	R/W	0x0	Retain	1= Enable clear on read 0 = Use 3.F030.6 to clear counters
12:9	Reserved	R/W	0x0	0x0	Set to 0s.
8	PRBS Lock	RO	0x0	0x0	1 = PRBS locked 0 = PRBS not locked
7	Immediate Error Count Enable	R/W	0x0	0x0	1 = Count PRBS errors before locking 0 = Wait until PRBS locks before counting
6	PRBS Counter Reset	R/W, SC	0x0	0x0	This bit self clears after counters are cleared. 1 = Clear counters 0 = Normal Operation
5	Transmit Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. 1 = Enable 0 = Disable
4	Receive Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. Note that there is no receive checking done for IEEE 48.A.1, 48.A.2, and 48.A.3. 1 = Enable, 0 = Disable
3:0		R/W	0x0	0x0	0000 = IEEE 49.2.8 - PRBS 31 0001 = PRBS 7 0010 = PRBS 9 IEEE 83.7 0011 = PRBS 23 0100 = PRBS 31 Inverted 0101 = PRBS 7 Inverted 1000 = PRBS 15 1001 = PRBS 15 Inverted 0110 = PRBS 9 Inverted 0111 = PRBS 23 Inverted 1100 = High frequency pattern 1101 = Low frequency pattern 1110 = Mixed frequency pattern 1111 = Square Wave pattern

Table 220: PRBS Symbol Tx Counter [15:0]
Device 3, Register 0xF031

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit transmitted per lane. If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read.

Table 221: PRBS Symbol Tx Counter [31:16]
Device 3, Register 0xF032

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [31:16]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 222: PRBS Symbol Tx Counter [47:32]
Device 3, Register 0xF033

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [47:32]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 223: PRBS Symbol Rx Counter [15:0]
Device 3, Register 0xF034

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit received per lane. If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read.

Table 224: PRBS Symbol Rx Counter [31:16]
Device 3, Register 0xF035

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [31:16]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 225: PRBS Symbol Rx Counter [47:32]
Device 3, Register 0xF036

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [47:32]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 226: PRBS Error Count [15:0]
Device 3, Register 0xF037

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit error received per lane. If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read.

Table 227: PRBS Error Count [31:16]
Device 3, Register 0xF038

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [31:16]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F037 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 228: PRBS Error Count [47:32]
Device 3, Register 0xF039

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [47:32]	RO	0x0000	0x0000	If 3.F030.13 = 0 then register does not clear on read. Cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F037 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 229: PRBS Elapse Timer
Device 3, Register 0xF03A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Elapse Timer Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every 2 second. Valid only if 3.F030.14 = 1 If 3.F030.13 = 0 then register does not clear on read, but cleared only when register 3.F030.6 transitions from 0 to 1. If 3.F030.13 = 1 then register clear on read. Must read register 3.F037 first in order to update this register.

Table 230: Power Management TX state control
Device 3, Register 0xF074

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	Writing to this section is forbidden
13	RG_EN_RST_DSP_S	R/W	0x1	Retain	0=Disable 1 = Enable
12:0	Reserved	RO	0x0000	0x0000	Writing to this section is forbidden

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6.3.6 SFI SERDES Registers

By default LDSP tries to automatically train the link partner for the best transmitter settings. The transmitter comes up with default settings which can be read back from registers in Table 232 to Table 239. If manual forcing of transmitter amplitude/pre/post emphasis is desired, it can be achieved by writing to the same registers. Here register address 1E.B116.15 should be read as 0x1E.0xB116 and so on.

Table 231: SFI SERDES Registers - Register Map

Register Name	Register Address	Table and Page
SFI Transmitter Lane 0 Settings	Register 0x1E.0xB116	Table 232, p. 189
SFI Transmitter Lane 0 Settings	Register 0x1E.0xB117	Table 233, p. 189
SFI Transmitter Lane 1 Settings	Register 0x1E.0xB316	Table 234, p. 190
SFI Transmitter Lane 1 Settings	Register 0x1E.0xB317	Table 235, p. 190
SFI Transmitter Lane 2 Settings	Register 0x1E.0xB516	Table 236, p. 190
SFI Transmitter Lane 2 Settings	Register 0x1E.0xB517	Table 237, p. 190
SFI Transmitter Lane 3 Settings	Register 0x1E.0xB716	Table 238, p. 191
SFI Transmitter Lane 3 Settings	Register 0x1E.0xB717	Table 239, p. 191

Table 232: SFI Transmitter Lane 0 Settings
Register 0x1E.0xB116

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 233: SFI Transmitter Lane 0 Settings
Register 0x1E.0xB117

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

Table 234: SFI Transmitter Lane 1 Settings
Register 0x1E.0xB316

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 235: SFI Transmitter Lane 1 Settings
Register 0x1E.0xB317

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

Table 236: SFI Transmitter Lane 2 Settings
Register 0x1E.0xB516

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 237: SFI Transmitter Lane 2 Settings
Register 0x1E.0xB517

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

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Table 238: SFI Transmitter Lane 3 Settings
Register 0x1E.0xB716

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 239: SFI Transmitter Lane 3 Settings
Register 0x1E.0xB717

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	N2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	NRST[5:0]

6.4 XFI Registers

6.4.1 XFI 10GBASE-R PCS

The registers in this section apply to all ports.

Table 240: XFI 10GBASE-R PCS Registers - Register Map

Register Name	Register Address	Table and Page
10GBASE-R PCS Control 1	Device 4, Register 0x0000	Table 241, p. 192
10GBASE-R PCS Status 1	Device 4, Register 0x0001	Table 242, p. 193
PCS Device Identifier 1	Device 4, Register 0x0002	Table 243, p. 193
PCS Device Identifier 2	Device 4, Register 0x0003	Table 244, p. 194
PCS Speed Ability	Device 4, Register 0x0004	Table 245, p. 194
PCS Devices In Package 1	Device 4, Register 0x0005	Table 246, p. 194
PCS Devices In Package 2	Device 4, Register 0x0006	Table 247, p. 195
PCS Control 2	Device 4, Register 0x0007	Table 248, p. 195
10GBASE-R PCS Status 2	Device 4, Register 0x0008	Table 249, p. 195
PCS Package Identifier 1	Device 4, Register 0x000E	Table 250, p. 196
PCS Package Identifier 2	Device 4, Register 0x000F	Table 251, p. 196
PCS EEE Capability Register	Device 4, Register 0x0014	Table 252, p. 196
BASE-R PCS Status 1	Device 4, Register 0x0020	Table 253, p. 197
BASE-R PCS Status 2	Device 4, Register 0x0021	Table 254, p. 197
10GBASE-R PCS Test Pattern Error Counter	Device 4, Register 0x002B	Table 255, p. 197
10GBASE-R Interrupt Enable Register	Device 4, Register 0x8000	Table 256, p. 197
10GBASE-R Interrupt Status Register	Device 4, Register 0x8001	Table 257, p. 198
10GBASE-R PCS Real Time Status Register	Device 4, Register 0x8002	Table 258, p. 198

Table 241: 10GBASE-R PCS Control 1
Device 4, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Loopback	R/W	0x0	0x0	1 = Loopback 0 = Normal
13	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
12	Reserved	RO	0x0	0x0	0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.

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Table 241: 10GBASE-R PCS Control 1 (Continued)
Device 4, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Clock Stoppable	R/W	0x0	0x0	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:7	Reserved	RO	0x0	0x0	000
6	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
5:2	Speed Select	RO	0x0	0x0	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1:0	Reserved	RO	0x0	0x0	00

Table 242: 10GBASE-R PCS Status 1
Device 4, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000000
11	TX LP Idle Received	RO/LH	0x0	0x0	1 = Tx PCS has received LP Idle 0 = LP Idle not received
10	Rx LP Idle Received	RO/LH	0x0	0x0	1 = Rx PCS has received LP Idle 0 = LP Idle not received
9	Tx LP Idle Indication	RO	0x0	0x0	1 = Tx PCS is currently receiving LP Idle 0 = Tx PCS is not currently receiving LP Idle
8	Rx LP Idle Indication	RO	0x0	0x0	1 = Rx PCS is currently receiving LP Idle 0 = Rx PCS is not currently receiving LP Idle
7	Fault	RO	0x0	0x0	1 = Fault condition 0 = No fault condition
6	Clock Stop Capable	RO	0x0	0x0	0 = Clock not stoppable
5:3	Reserved	RO	0x0	0x0	000
2	Link Status	RO, LL	0x0	0x0	1 = PCS link up 0 = PCS link down
1	Low Power Ability	RO	0x1	0x1	1 = PCS Supports Low Power
0	Reserved	RO	0x0	0x0	0

Table 243: PCS Device Identifier 1
Device 4, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 244: PCS Device Identifier 2
Device 4, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 245: PCS Speed Ability
Device 4, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	100G Capable	RO	0x0	0x0	0 = Not capable of operating at 100Gbps
2	40G Capable	RO	0x1	0x1	1 = Capable of operating at 40Gbps
1	10PASS-TS/2BASE-TL Capable	RO	0x0	0x0	0 = Not capable of operating as the 10P/2B PCS
0	10G Capable	RO	0x1	0x1	1 = Capable of operating at 10Gbps

Table 246: PCS Devices In Package 1
Device 4, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	00000
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package

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Table 246: PCS Devices In Package 1 (Continued)
Device 4, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 247: PCS Devices In Package 2
Device 4, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 248: PCS Control 2
Device 4, Register 0x0007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2:0	PCS Type Selection	RO	0x0	0x0	This register is ignored. PCS is automatically set based on the mode selected in register 31.F002

Table 249: 10GBASE-R PCS Status 2
Device 4, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address
13:12	Reserved	RO	0x0	0x0	00
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault on transmit path, 0 = No fault
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault on receive path, 0 = No fault
9:6	Reserved	RO	0x0	0x0	0000000
5	100GBASE-R Capable	RO	0x0	0x0	1 = PCS is able to support 100GBASE-R PCS types 0 = PCS is not able to support 100GBASE-R PCS types

Table 249: 10GBASE-R PCS Status 2 (Continued)
Device 4, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
4	40GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 40GBASE-R PCS types 0 = PCS is not able to support 40GBASE-R PCS types
3	10GBASE-T Capable	RO	0x0	0x0	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	10GBASE-X Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types
0	10GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types

Table 250: PCS Package Identifier 1
Device 4, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 251: PCS Package Identifier 2
Device 4, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 252: PCS EEE Capability Register
Device 4, Register 0x0014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	0
6	10GBASE-KR EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KR
5	10GBASE-KX4 EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KX4
4	1000BASE-KX EEE	RO	0x0	0x0	1 = EEE is supported for 1000BASE-KX
3:0	Reserved	RO	0x0	0x0	0

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Table 253: BASE-R PCS Status 1
Device 4, Register 0x0020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	10GBASE-R Receive Link Status	RO	0x0	0x0	1 = 10G BASE-R PCS receive link up 0 = 10G BASE-R PCS receive link down
11:4	Reserved	RO	0x00	0x00	0
3	PRBS9 Pattern Testing Ability	RO	0x1	0x1	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing
2	PRBS31 Pattern Testing Ability	RO	0x1	0x1	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing
1	10GBASE-R PCS High Bit Error Rate	RO	0x0	0x0	1 = 10G BASE-R PCS reporting high BER 0 = 10G BASE-R PCS not reporting high BER
0	10GBASE-R PCS Block Lock	RO	0x0	0x0	1 = 10G BASE-R PCS locked to received block 0 = 10G BASE-R PCS not locked

Table 254: BASE-R PCS Status 2
Device 4, Register 0x0021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Latched Block Lock	RO, LL	0x0	0x0	1 = PCS Has Block Lock 0 = PCS Does Not Have Block Lock
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS Has Reported High BER 0 = PCS Has Not Reported High BER
13:8	Bit Error Rate Counter	RO	0x00	0x00	Bit Error Rate Counter Counter clears on read. Counter will peg at all 1s.
7:0	Errored Blocks Counter	RO	0x00	0x00	Errored Blocks Counter Counter clears on read. Counter will peg at all 1s.

Table 255: 10GBASE-R PCS Test Pattern Error Counter
Device 4, Register 0x002B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Error Counter	RO	0x0000	0x0000	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s. In Pseudo-random test mode, it counts block errors. In PRBS31 test mode it counts bit errors at the PRBS31 pattern checker output.

Table 256: 10GBASE-R Interrupt Enable Register
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Set to 0

Table 256: 10GBASE-R Interrupt Enable Register (Continued)
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Local Fault Transmitted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Local Fault Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9:4	Reserved	R/W	0x00	Retain	Set to 0
3	Reserved	R/W	0x0	Retain	Set to 0
2	Link status change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	High BER Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Block Lock Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 257: 10GBASE-R Interrupt Status Register
Device 4, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO,LH	0x0	0x0	Set to 0
11	Local Fault Transmitted Interrupt	RO,LH	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitter
10	Local Fault Received Interrupt	RO,LH	0x0	0x0	1 = Local fault received 0 = No local fault received
9:4	Reserved	RO,LH	0x00	0x00	Set to 0
3	Reserved	RO,LH	0x0	0x0	Set to 0
2	Link status change Detected	RO,LH	0x0	0x0	1 = Link status changed detected 0 = Link status changed not detected
1	High BER Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
0	Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

Table 258: 10GBASE-R PCS Real Time Status Register
Device 4, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	Set to 0
11	Local Fault Transmitted Status	RO	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitted

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Table 258: 10GBASE-R PCS Real Time Status Register (Continued)
Device 4, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Local Fault Received Status	RO	0x0	0x0	1 = Local fault received 0 = No local fault received
9:5	Reserved	RO	0x00	0x00	Set to 0
4	Jit_0_lock	RO	0x0	0x0	1 = JIT 0 lock achieved
3	Jit_lf_lock	RO	0x0	0x0	1 = JIT local fault lock achieved
2	Link Status	RO	0x0	0x0	1 = 10GBASE-R link achieved 0 = No link
1	High BER Status	RO	0x0	0x0	1 = High BER 0 = No high BER
0	Lane 3 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

6.4.2 XFI XAUI, RXAUI PCS

The registers in this section applies to ports 0 and 2 for XAUI, RXAUI PCS and ports 1 and 3 for RXAUI only.

Table 259: XFI XAUI, RXAUI PCS Registers - Register Map

Register Name	Register Address	Table and Page
XAUI PCS Control 1	Device 4, Register 0x1000	Table 260, p. 200
XAUI PCS Status 1	Device 4, Register 0x1001	Table 261, p. 201
PCS Device Identifier 1	Device 4, Register 0x1002	Table 262, p. 202
PCS Device Identifier 2	Device 4, Register 0x1003	Table 263, p. 202
PCS Speed Ability	Device 4, Register 0x1004	Table 264, p. 202
PCS Devices In Package 1	Device 4, Register 0x1005	Table 265, p. 202
PCS Devices In Package 2	Device 4, Register 0x1006	Table 266, p. 203
PCS Control 2	Device 4, Register 0x1007	Table 267, p. 203
XAUI PCS Status 2	Device 4, Register 0x1008	Table 268, p. 203
PCS Package Identifier 1	Device 4, Register 0x100E	Table 269, p. 204
PCS Package Identifier 2	Device 4, Register 0x100F	Table 270, p. 204
PCS EEE Capability Register	Device 4, Register 0x1014	Table 271, p. 205
10GBASE-X Lane Status	Device 4, Register 0x1018	Table 272, p. 205
10GBASE-X Test Control Register	Device 4, Register 0x1019	Table 273, p. 205
XAUI Control	Device 4, Register 0x9000	Table 274, p. 206
XAUI Interrupt Enable 1	Device 4, Register 0x9001	Table 275, p. 206
XAUI Interrupt Enable 2	Device 4, Register 0x9002	Table 276, p. 207
XAUI Interrupt Status 1	Device 4, Register 0x9003	Table 277, p. 207
XAUI Interrupt Status 2	Device 4, Register 0x9004	Table 278, p. 208
XAUI Real Time Status Register 2	Device 4, Register 0x9006	Table 279, p. 208
XAUI Random Sequence Control	Device 4, Register 0x9010	Table 280, p. 209
XAUI Jitter Packet Transmit Counter LSB	Device 4, Register 0x9011	Table 281, p. 209
XAUI Jitter Packet Transmit Counter MSB	Device 4, Register 0x9012	Table 282, p. 209
XAUI Jitter Packet Received Counter LSB	Device 4, Register 0x9013	Table 283, p. 210
XAUI Jitter Packet Received Counter MSB	Device 4, Register 0x9014	Table 284, p. 210
XAUI Jitter Pattern Error Counter LSB	Device 4, Register 0x9015	Table 285, p. 210
XAUI Jitter Pattern Error Counter MSB	Device 4, Register 0x9016	Table 286, p. 210

Table 260: XAUI PCS Control 1
Device 4, Register 0x1000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Loopback	R/W	0x0	0x0	1 = Loopback 0 = Normal

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Table 260: XAUI PCS Control 1 (Continued)
Device 4, Register 0x1000

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
12	Reserved	RO	0x0	0x0	0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Clock Stoppable	R/W	0x0	0x0	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:7	Reserved	RO	0x0	0x0	000
6	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
5:2	Speed Select	RO	0x0	0x0	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1:0	Reserved	RO	0x0	0x0	00

Table 261: XAUI PCS Status 1
Device 4, Register 0x1001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000000
11	TX LP Idle Received	RO/LH	0x0	0x0	1 = Tx PCS has received LP Idle 0 = LP Idle not received
10	Rx LP Idle Received	RO/LH	0x0	0x0	1 = Rx PCS has received LP Idle 0 = LP Idle not received
9	Tx LP Idle Indication	RO	0x0	0x0	1 = Tx PCS is currently receiving LP Idle 0 = Tx PCS is not currently receiving LP Idle
8	Rx LP Idle Indication	RO	0x0	0x0	1 = Rx PCS is currently receiving LP Idle 0 = Rx PCS is not currently receiving LP Idle
7	Fault	RO	0x0	0x0	1 = Fault condition 0 = No fault condition
6	Clock Stop Capable	RO	0x0	0x0	0 = Clock not stoppable
5:3	Reserved	RO	0x0	0x0	000
2	Link Status	RO, LL	0x0	0x0	1 = PCS link up 0 = PCS link down
1	Low Power Ability	RO	0x1	0x1	1 = PCS supports low power
0	Reserved	RO	0x0	0x0	0

Table 262: PCS Device Identifier 1
Device 4, Register 0x1002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 263: PCS Device Identifier 2
Device 4, Register 0x1003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 264: PCS Speed Ability
Device 4, Register 0x1004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RO	0x00	0x00	0
8	100G Capable	RO	0x0	0x0	0 = Not capable of operating at 100 Gbps
7	40G Capable	RO	0x1	0x1	1 = Capable of operating at 40 Gbps
6:2	Reserved	RO	0x00	0x00	0
1	10PASS-TS/2BASE-TL Capable	RO	0x0	0x0	0 = Not capable of operating as the 10P/2B PCS
0	10G Capable	RO	0x1	0x1	1 = Capable of operating at 10G

Table 265: PCS Devices In Package 1
Device 4, Register 0x1005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	00000
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package

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Table 265: PCS Devices In Package 1 (Continued)
Device 4, Register 0x1005

Bits	Field	Mode	HW Rst	SW Rst	Description
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 266: PCS Devices In Package 2
Device 4, Register 0x1006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 267: PCS Control 2
Device 4, Register 0x1007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2:0	PCS Type Selection	RO	0x1	0x1	This register is ignored. PCS is automatically set based on the mode selected in register 31.F002

Table 268: XAUI PCS Status 2
Device 4, Register 0x1008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address

Table 268: XAUI PCS Status 2 (Continued)
Device 4, Register 0x1008

Bits	Field	Mode	HW Rst	SW Rst	Description
13:12	Reserved	RO	0x0	0x0	00
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault on transmit path, 0 = No fault
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault on receive path, 0 = No fault
9:6	Reserved	RO	0x0	0x0	0000000
5	100GBASE-R Capable	RO	0x0	0x0	1 = PCS is able to support 100GBASE-R PCS types 0 = PCS is not able to support 100GBASE-R PCS types
4	40GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 40GBASE-R PCS types 0 = PCS is not able to support 40GBASE-R PCS types
3	10GBASE-T Capable	RO	0x0	0x0	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types
2	Reserved	RO	0x0	0x0	Reserved
1	10GBASE-X Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types
0	10GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types

Table 269: PCS Package Identifier 1
Device 4, Register 0x100E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 270: PCS Package Identifier 2
Device 4, Register 0x100F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

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Table 271: PCS EEE Capability Register
Device 4, Register 0x1014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	0
6	10GBASE-KR EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KR
5	10GBASE-KX4 EEE	RO	0x0	0x0	1 = EEE is supported for 10GBASE-KX4
4	1000BASE-KX EEE	RO	0x0	0x0	1 = EEE is supported for 1000BASE-KX
3:0	Reserved	RO	0x0	0x0	0

Table 272: 10GBASE-X Lane Status
Device 4, Register 0x1018

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	000
12	Lane Alignment Status	RO	0x0	0x0	1 = Rx Lanes Aligned 0 = Rx Lanes Not Aligned
11	Pattern Testing Ability	RO	0x1	0x1	1 = Is Able To Generate Test Patterns
10	PHY XGXS Loopback Ability	RO	0x1	0x1	1 = Has Ability To Perform Loopback Function
9:4	Reserved	RO	0x00	0x00	000000
3	Lane 3 Sync	RO	0x0	0x0	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized
2	Lane 2 Sync	RO	0x0	0x0	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized
1	Lane 1 Sync	RO	0x0	0x0	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized
0	Lane 0 Sync	RO	0x0	0x0	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized

Table 273: 10GBASE-X Test Control Register
Device 4, Register 0x1019

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2	Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Transmit test pattern enable 0 = Transmit test pattern not enabled Jitter 48A.1, 48A.2, and 48A.3 can also be generated by setting register 4.9010.2:0 If both 4.1019.2 and 4.9010.4 are asserted, the setting in 4.1019.1:0 takes priority.

Table 273: 10GBASE-X Test Control Register (Continued)
Device 4, Register 0x1019

Bits	Field	Mode	HW Rst	SW Rst	Description
1:0	Test Pattern Select	R/W	0x0	0x0	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved See Desc. in 4.1019.2

Table 274: XAUI Control
Device 4, Register 0x9000

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	0
7	XAUI Lane Reverse Enable	R/W	0x0	Retain	1 = Lane reverse enable 0 = Lane reverse disable
6	Signal Detect Override Value	R/W	0x0	Retain	Signal detect override value when bit 5 is set to 1.
5	Signal Detect Override Enable	R/W	0x0	Retain	1 = Override enable 0 = Override disable
4:2	Reserved	RO	0x0	Retain	0
1	X2 Disparity Enable.	R/W	0x0	Retain	There are two methods to interleave the lanes in RXAUI mode. The Disparity Calculation Is Different. 1 = Interleave two 8-bit stream first and then apply 8/10 encoding 0 = Apply 8/10 encoding first and then interleave at the 10 bit level.
0	LPI Codeword Enable	R/W	0x0	Retain	1 = Low Power Idle codeword support enabled 0 = LPI support disabled

Table 275: XAUI Interrupt Enable 1
Device 4, Register 0x9001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	R/W	0x000	Retain	Set to 0.
3	Link Up to Link Down Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	Link Down to Link Up Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	0x0	0

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Table 276: XAUI Interrupt Enable 2
Device 4, Register 0x9002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	0
9	Fault Line To Core Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	Fault Core To Line Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Lane 3 Energy Detect Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	Lane 2 Energy Detect Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Lane 1 Energy Detect Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
4	Lane 0 Energy Detect Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	Lane 3 Sync Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	Lane 2 Sync Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Lane 1 Sync Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Lane 0 Sync Change Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 277: XAUI Interrupt Status 1
Device 4, Register 0x9003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	Link Up to Link Down Detected	RO,LH	0x0	0x0	1 = Link up to link down detected 0 = Link up to link down not detected
2	Link Down to Link Up Detected	RO,LH	0x0	0x0	1 = Link down to link up detected 0 = Link down to link up not detected
1:0	Reserved	RO	0x0	0x0	0

Table 278: XAUI Interrupt Status 2
Device 4, Register 0x9004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	0
9	Fault Line To Core Interrupt	RO, LH	0x0	0x0	1 = Fault occurred 0 = No fault
8	Fault Core To Line Interrupt	RO, LH	0x0	0x0	1 = Fault occurred 0 = No fault
7	Lane 3 Energy Detect Changed Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
6	Lane 2 Energy Detect Changed Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
5	Lane 1 Energy Detect Changed Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
4	Lane 0 Energy Detect Changed Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
3	Lane 3 Sync Change Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
2	Lane 2 Sync Change Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
1	Lane 1 Sync Change Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change
0	Lane 0 Sync Change Interrupt	RO, LH	0x0	0x0	1= Change detected 0 = No Change

Table 279: XAUI Real Time Status Register 2
Device 4, Register 0x9006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0
7	Lane 3 Energy Detect Status	RO	0x0	0x0	1 = Energy detected 0 = No Energy Detected
6	Lane 2 Energy Detect Status	RO	0x0	0x0	1 = Energy detected 0 = No Energy Detected
5	Lane 1 Energy Detect Status	RO	0x0	0x0	1 = Energy detected 0 = No Energy Detected
4	Lane 0 Energy Detect Status	RO	0x0	0x0	1 = Energy detected 0 = No Energy Detected
3	Lane 3 Sync Status	RO	0x0	0x0	1 = Sync 0 = No Sync
2	Lane 2 Sync Status	RO	0x0	0x0	1 = Sync 0 = No Sync

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Table 279: XAUI Real Time Status Register 2 (Continued)
Device 4, Register 0x9006

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Lane 1 Sync Status	RO	0x0	0x0	1 = Sync 0 = No Sync
0	Lane 0 Sync Status	RO	0x0	0x0	1 = Sync 0 = No Sync

Table 280: XAUI Random Sequence Control
Device 4, Register 0x9010

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	Set to 0
7	Counter Reset	R/W, SC	0x0	Retain	This bit self clears after counters are cleared. 1 = Clear counter 0 = Normal operation
6	Reserved	RO	0x0	Retain	Set to 0
5	Jitter Receive Checking Enable	R/W	0x0	Retain	1 = Jitter Test Receive Enable
4	Jitter Transmit Generation Enable	R/W	0x0	Retain	1 = Jitter Test Transmit Enable Jitter 48A.1, 48A.2, and 48A.3 can also be generated by setting register 4.1019.1:0 If both 4.1019.2 and 4.9010.4 are asserted the setting in 4.1019.1:0 takes priority.
3	Reserved	RO	0x0	Retain	Set to 0.
2:0	Jitter Test Select	R/W	0x0	Retain	000 = Jitter 48A.1 (high freq) 001 = Jitter 48A.2 (low freq) 010 = Jitter 48A.3 (mix freq) 100 = Jitter 48A.4 (CRPAT) 101 = Jitter 48A.5 (CJPAT) Else = reserved

Table 281: XAUI Jitter Packet Transmit Counter LSB
Device 4, Register 0x9011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count LSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1.

Table 282: XAUI Jitter Packet Transmit Counter MSB
Device 4, Register 0x9012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count MSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1. Must read register 4.9011 first in order to update register 4.9012. This insures the 32 bit read is atomic.

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Table 283: XAUI Jitter Packet Received Counter LSB
Device 4, Register 0x9013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count LSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1.

Table 284: XAUI Jitter Packet Received Counter MSB
Device 4, Register 0x9014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count MSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1. Must read register 4.9013 first in order to update register 4.9014. This insures the 32 bit read is atomic.

Table 285: XAUI Jitter Pattern Error Counter LSB
Device 4, Register 0x9015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count LSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1

Table 286: XAUI Jitter Pattern Error Counter MSB
Device 4, Register 0x9016

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Error Count MSB	RO	0x0000	Retain	Register does not clear on read. Cleared only when register 4.9010.7 is set to 1. Must read register 4.9015 first in order to update register 4.9016. This insures the 32 bit read is atomic.

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6.4.3 Host Side 1000BASE-X, SGMII PCS

The registers in this section apply to all ports.

Table 287: Host Side 1000BASE-X, SGMII PCS Registers - Register Map

Register Name	Register Address	Table and Page
1000BASE-X/SGMII Control Register	Device 4, Register 0x2000	Table 288, p. 211
1000BASE-X/SGMII Status Register	Device 4, Register 0x2001	Table 289, p. 212
PHY Identifier	Device 4, Register 0x2002	Table 290, p. 213
PHY Identifier	Device 4, Register 0x2003	Table 291, p. 213
1000BASE-X Auto-Negotiation Advertisement Register	Device 4, Register 0x2004	Table 292, p. 214
SGMII (Media side) Auto-Negotiation Advertisement Register	Device 4, Register 0x2004	Table 293, p. 215
SGMII (System side) Auto-Negotiation Advertisement Register	Device 4, Register 0x2004	Table 294, p. 215
1000BASE-X Link Partner Ability Register	Device 4, Register 0x2005	Table 295, p. 216
SGMII (Media side) Link Partner Ability Register	Device 4, Register 0x2005	Table 296, p. 217
SGMII (System side) Link Partner Ability Register	Device 4, Register 0x2005	Table 297, p. 217
1000BASE-X Auto-Negotiation Expansion Register	Device 4, Register 0x2006	Table 298, p. 218
1000BASE-X Next Page Transmit Register	Device 4, Register 0x2007	Table 299, p. 219
1000BASE-X Link Partner Next Page Register	Device 4, Register 0x2008	Table 300, p. 219
Extended Status Register	Device 4, Register 0x200F	Table 301, p. 219
1000BASE-X Timer Mode Select Register	Device 4, Register 0xA000	Table 302, p. 220
1000BASE-X Interrupt Enable Register	Device 4, Register 0xA001	Table 303, p. 220
1000BASE-X Interrupt Status Register	Device 4, Register 0xA002	Table 304, p. 221
1000ASE-X PHY Specific Status Register	Device 4, Register 0xA003	Table 305, p. 221

Table 288: 1000BASE-X/SGMII Control Register
Device 4, Register 0x2000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.
14	Loopback	R/W	See Desc.	Retain	1 = Loopback 0 = Normal
13	SGMII Speed (LSB)	R/W	See Desc.	Retain	This register is used to control SGMII speed only. (bit 6, bit 13) 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps
12	1000BASE-X Auto-Negotiation Enable	R/W	See Desc.	Retain	If the value of this bit is Changed, the link will be broken and 1000BASE-X Auto-Negotiation restarted (bit 4.2000.9 is set to 1). 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Table 288: 1000BASE-X/SGMII Control Register (Continued)
Device 4, Register 0x2000

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Isolate	RO	0x0	0x0	The core bus is embedded hence this function is not supported
9	Restart 1000BASE-X Negotiation	R/W, SC	0x1	SC	Auto-Negotiation automatically restarts after hardware reset, software reset (4.2000.15) or Change in auto-negotiation enable (4.2000.12) regardless of whether or not the restart bit (4.2000.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 4.2000.12. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex Mode	RO	0x1	Retain	Writing this bit has no effect since only full-duplex mode is supported. 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	R/W	0x0	0x0	No effect since half-duplex not supported. 1 = Enable COL signal test 0 = Disable COL signal test
6	SGMII Speed Selection (MSB)	R/W	See Desc.	Retain	This register is used to control SGMII speed only. (bit 6, bit 13) 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps
5:0	Reserved	RO	0x00	0x00	Always 0.

Table 289: 1000BASE-X/SGMII Status Register
Device 4, Register 0x2001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	0x0	0x0	0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	0x0	0x0	0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	0x0	0x0	0 = PHY not able to perform half-duplex

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Table 289: 1000BASE-X/SGMII Status Register (Continued)
Device 4, Register 0x2001

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Extended Status	RO	0x1	0x1	1 = Extended status information in Register 4.200F
7	Reserved	RO	0x0	0x0	Must always be 0.
6	MF Preamble Suppression	RO	0x1	0x1	1 = PHY accepts management frames with preamble suppressed
5	1000BASE-X Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled.
4	1000BASE-X Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII modes.
3	Auto-Negotiation Ability	RO	See Desc.	See Desc.	If register 4.F002.6= 1, then this bit is always 1, otherwise this bit is 0. 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation
2	1000BASE-X Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, read this register back-to-back. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Must be 0
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 290: PHY Identifier
Device 4, Register 0x2002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 291: PHY Identifier
Device 4, Register 0x2003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 292: 1000BASE-X Auto-Negotiation Advertisement Register
Device 4, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 4.2000.15) Restart Auto-Negotiation is asserted (Register 4.2000.9) Power down (Register 4.2000.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
14	Reserved	RO	Always 0	Always 0	0
13:12	Remote Fault 2/ RemoteFault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 4.2000.15) Re-start Auto-Negotiation is asserted (Register 4.2000.9) Power down (Register 4.2000.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	Always 000	Always 000	0
8:7	Pause	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 4.2000.15) Re-start Auto-Negotiation is asserted (Register 4.2000.9) Power down (Register 4.2000.11) transitions from power down to normal operation Link goes down 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	Retain	1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	RO	0x1	Retain	1 = Advertise 0 = Not advertised

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Table 292: 1000BASE-X Auto-Negotiation Advertisement Register (Continued)
Device 4, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	Reserved	R/W	0x00	0x00	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 4.2000.15) Re-start Auto-Negotiation is asserted (Register 4.2000.9) Power down (Register 4.2000.11) transitions from power down to normal operation Link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

Table 293: SGMII (Media side) Auto-Negotiation Advertisement Register
Device 4, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is not up on the attached interface 1 = Link is up on the attached interface
14	Reserved	RO	0x0	0x0	0
13	Reserved	RO	0x0	0x0	0
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to half-duplex 1 = Interface Resolved to full-duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	0 = Disabled, 1 = Enabled
8	Receive Pause	RO	0x0	0x0	0 = Disabled, 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x01	0x01	Always set to 0000001 as per the SGMII Specification

Table 294: SGMII (System side) Auto-Negotiation Advertisement Register
Device 4, Register 0x2004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	0x0001	0x0001	Per SGMII Specification Always 0x0001

Table 295: 1000BASE-X Link Partner Ability Register
Device 4, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:9
8:7	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved	RO	0x00	0x00	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bits 4:0 Must be 0

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Table 296: SGMII (Media side) Link Partner Ability Register
Device 4, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Must be 0
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Received Code Word Bits 13:0 Must receive 00_0000_0000_0001 per SGMII spec

Table 297: SGMII (System side) Link Partner Ability Register
Device 4, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13 Must be 0
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the Link Partner is capable of full-duplex 0 = Copper Interface on the link partner is capable of half-duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = reserved

Table 297: SGMII (System side) Link Partner Ability Register (Continued)
Device 4, Register 0x2005

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto-Negotiation. Received Code Word Bit 9 0 = Disabled 1 = Enabled
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto Negotiation. Received Code Word Bit 8 0 = Disabled, 1 = Enabled
7	Fiber/Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII Auto-Negotiation. Received Code Word Bit 7 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x00	0x00	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bits 6:0 Must be 0000001

Table 298: 1000BASE-X Auto-Negotiation Expansion Register
Device 4, Register 0x2006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
3	Link Partner Next Page Able	RO	0x0	0x0	In SGMII mode this bit is always 0. In 1000BASE-X mode register 4.2006.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 4.2006.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 4.2000.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

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Table 299: 1000BASE-X Next Page Transmit Register
Device 4, Register 0x2007

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Register 7 only has effect in the 1000BASE-X mode. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 300: 1000BASE-X Link Partner Next Page Register
Device 4, Register 0x2008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register 8 only has effect in the 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 301: Extended Status Register
Device 4, Register 0x200F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	0x1	0x1	1 = 1000 BASE-X full duplex capable 0 = Not 1000 BASE-X full duplex capable
14	1000BASE-X Half-Duplex	RO	0x0	0x0	1 = 1000 BASE-X half-duplex capable 0 = Not 1000 BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = Not 1000 BASE-T full-duplex capable

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Table 301: Extended Status Register (Continued)
Device 4, Register 0x200F

Bits	Field	Mode	HW Rst	SW Rst	Description
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = Not 1000 BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 302: 1000BASE-X Timer Mode Select Register
Device 4, Register 0xA000

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	SGMII Autoneg Timer Select	R/W	0x0	Retain	Selects link_timer value in SGMII mode 00 = 1.6 ms 01 = 0.5 us 10 = 1 us 11 = 2 us
13	Serial Interface Auto-Negotiation Bypass Enable	R/W	0x1	Retain	Changes to this bit are disruptive to the normal operation; hence, any Changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
12:2	Reserved	RO	0x000	0x000	
1	Reserved	R/W	0x0	Retain	Reserved
0	Noise Filter	R/W	0x0	Retain	When set, noise filter is enabled.

Table 303: 1000BASE-X Interrupt Enable Register
Device 4, Register 0xA001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Set to 0
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Up to Link Down Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Link Down to Link Up Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

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Table 303: 1000BASE-X Interrupt Enable Register (Continued)
Device 4, Register 0xA001

Bits	Field	Mode	HW Rst	SW Rst	Description
7	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:0	Reserved	R/W	0x00	Retain	Set to 0s

Table 304: 1000BASE-X Interrupt Status Register
Device 4, Register 0xA002

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Up to Link Down Detected	RO,LH	0x0	0x0	1 = Link up to link down detected 0 = Link up to link down not detected
9	Link Down to Link Up Detected	RO,LH	0x0	0x0	1 = Link down to link up detected 0 = Link down to link up not detected
8	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
7	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
6:0	Reserved	RO	0x00	0x00	0000000

Table 305: 1000ASE-X PHY Specific Status Register
Device 4, Register 0xA003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	0x0	These status bits are valid only after resolved bit 4.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps

Table 305: 1000ASE-X PHY Specific Status Register (Continued)
Device 4, Register 0xA003

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Duplex	RO	0x0	0x0	This status bit is valid only after resolved bit 4.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled this bit is always 1. 1 = Resolved 0 = Not resolved
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:6	Reserved	RO	0x0	0x0	0
5	sync status	RO	0x0	0x0	1 = Sync 0 = No Sync
4	Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 4.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 4.A003.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved	RO	0x0	0x0	00

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6.4.4 XFI 40GBASE-R4

The registers in this section apply to Port 0 for 40GBASE-R4 only.

Table 306: XFI 40GBASE-R4 - Register Map

Register Name	Register Address	Table and Page
40GBASE-R4 PCS Control 1	Device 4, Register 0x3000	Table 307, p. 223
40GBASE-R4 PCS Status 1	Device 4, Register 0x3001	Table 308, p. 224
PCS Device Identifier 1	Device 4, Register 0x3002	Table 309, p. 225
PCS Device Identifier 2	Device 4, Register 0x3003	Table 310, p. 225
PCS Speed Ability	Device 4, Register 0x3004	Table 311, p. 225
PCS Devices In Package 1	Device 4, Register 0x3005	Table 312, p. 225
PCS Devices In Package 2	Device 4, Register 0x3006	Table 313, p. 226
PCS Control 2	Device 4, Register 0x3007	Table 314, p. 226
40GBASE-R4 PCS Status 2	Device 4, Register 0x3008	Table 315, p. 226
PCS Package Identifier 1	Device 4, Register 0x300E	Table 316, p. 227
PCS Package Identifier 2	Device 4, Register 0x300F	Table 317, p. 227
BASE-R Status1 Register	Device 4, Register 0x3020	Table 318, p. 228
BASE-R PCS Status 2	Device 4, Register 0x3021	Table 319, p. 228
40GBASE-R PCS Test Pattern Control	Device 4, Register 0x302A	Table 320, p. 228
40GBASE-R PCS Test Pattern Error Counter	Device 4, Register 0x302B	Table 321, p. 229
40GBASE-R PCS BER High Order Counter	Device 4, Register 0x302C	Table 322, p. 229
40GBASE-R PCS Errored Blocks High Order Counter	Device 4, Register 0x302D	Table 323, p. 229
Multi-lane BASE-R PCS Alignment Status 1	Device 4, Register 0x3032	Table 324, p. 229
Multi-lane BASE-R PCS Alignment Status 2	Device 4, Register 0x3034	Table 325, p. 230
BIP Error Counter Lanes 0 Register	Device 4, Register 0x30C8	Table 326, p. 230
BIP Error Counter Lanes 1 Register	Device 4, Register 0x30C9	Table 327, p. 230
BIP Error Counter Lanes 2 Register	Device 4, Register 0x30CA	Table 328, p. 231
BIP Error Counter Lanes 3 Register	Device 4, Register 0x30CB	Table 329, p. 231
Lanes 0 Mapping Register	Device 4, Register 0x3190	Table 330, p. 231
Lanes 1 Mapping Register	Device 4, Register 0x3191	Table 331, p. 231
Lanes 2 Mapping Register	Device 4, Register 0x3192	Table 332, p. 231
Lanes 3 Mapping Register	Device 4, Register 0x3193	Table 333, p. 231
40GBASE-R4 Interrupt enable Register	Device 4, Register 0xB001	Table 334, p. 232
40GBASE-R4 Interrupt Status Register	Device 4, Register 0xB002	Table 335, p. 233
40GBASE-R4 PCS Real Time Status Register	Device 4, Register 0xB003	Table 336, p. 234

Table 307: 40GBASE-R4 PCS Control 1
Device 4, Register 0x3000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	0x0	1 = Reset 0 = Normal This register will soft reset all PCS/PMA and associated registers of this interface.

Table 307: 40GBASE-R4 PCS Control 1 (Continued)
Device 4, Register 0x3000

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Loopback	R/W	0x0	0x0	1 = Loopback 0 = Normal
13	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
12	Reserved	RO	0x0	0x0	Set to 0
11	Low Power	R/W	See Desc.	Retain	1 = Power Down 0 = Normal This register will power down all PCS/PMA of this interface. Initial power state is a function of hardware configuration.
10	Clock Stoppable	R/W	0x0	0x0	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:7	Reserved	RO	0x0	0x0	000
6	Speed Select	RO	0x1	0x1	1 = Bits 5:2 select speed.
5:2	Speed Select	RO	0x3	0x3	This register is ignored. Speed is automatically set based on the mode selected in register 31.F002
1:0	Reserved	RO	0x0	0x0	Set to 0s

Table 308: 40GBASE-R4 PCS Status 1
Device 4, Register 0x3001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	00000000
11	TX LP Idle Received	RO/LH	0x0	0x0	1 = Tx PCS has received LP Idle 0 = LP Idle not received
10	Rx LP Idle Received	RO/LH	0x0	0x0	1 = Rx PCS has received LP Idle 0 = LP Idle not received
9	Tx LP Idle Indication	RO	0x0	0x0	1 = Tx PCS is currently receiving LP Idle 0 = Tx PCS is not currently receiving LP Idle
8	Rx LP Idle Indication	RO	0x0	0x0	1 = Rx PCS is currently receiving LP Idle 0 = Rx PCS is not currently receiving LP Idle
7	Fault	RO	0x0	0x0	1 = Transmit or Receive fault condition 0 = No fault condition
6	Clock Stop Capable	RO	0x0	0x0	0 = Clock not stoppable
5:3	Reserved	RO	0x0	0x0	000
2	Link Status	RO, LL	0x0	0x0	1 = PCS link up 0 = PCS link down
1	Low Power Ability	RO	0x1	0x1	1 = PCS supports low power
0	Reserved	RO	0x0	0x0	0

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Table 309: PCS Device Identifier 1
Device 4, Register 0x3002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 310: PCS Device Identifier 2
Device 4, Register 0x3003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 311: PCS Speed Ability
Device 4, Register 0x3004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3	100G Capable	RO	0x0	0x0	0 = Not capable of operating at 100Gbps
2	40G Capable	RO	0x1	0x1	1 = Capable of operating at 40Gbps
1	10PASS-TS/2BASE-TL Capable	RO	0x0	0x0	0 = Not capable of operating as the 10P/2B PCS
0	10G Capable	RO	0x1	0x1	1 = Capable of operating at 10Gbps

Table 312: PCS Devices In Package 1
Device 4, Register 0x3005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	00000
10	Separated PMA (3)	RO	0x0	0x0	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package
9	Separated PMA (2)	RO	0x0	0x0	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package
8	Separated PMA (1)	RO	0x0	0x0	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-negotiation present in package 0 = Auto-negotiation not present in package

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Table 312: PCS Devices In Package 1 (Continued)
Device 4, Register 0x3005

Bits	Field	Mode	HW Rst	SW Rst	Description
6	TC Present	RO	0x0	0x0	1 = TC present in package 0 = TC not present in package
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x1	0x1	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	Reserved	RO	0x1	0x1	Reserved Do not write any value other than the HW Rst value.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 313: PCS Devices In Package 2
Device 4, Register 0x3006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Marvell Specific Device 2 Present	RO	0x1	0x1	1 = Marvell specific device 2 present 0 = Marvell specific device 2 not present
14	Marvell Specific Device 1 Present	RO	0x1	0x1	1 = Marvell specific device 1 present 0 = Marvell specific device 1 not present
13	Clause 22 Extension Present	RO	0x0	0x0	1 = Clause 22 extension present 0 = Clause 22 extension not present
12:0	Reserved	RO	0x0000	0x0000	0

Table 314: PCS Control 2
Device 4, Register 0x3007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2:0	PCS Type	RO	0x4	0x4	This register is ignored. PCS is automatically set based on the mode selected in register 31.F002

Table 315: 40GBASE-R4 PCS Status 2
Device 4, Register 0x3008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding to this address

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Table 315: 40GBASE-R4 PCS Status 2 (Continued)
Device 4, Register 0x3008

Bits	Field	Mode	HW Rst	SW Rst	Description
13:12	Reserved	RO	0x0	0x0	00
11	Transmit Fault	RO, LH	0x0	0x0	1 = Fault on transmit path, 0 = No fault
10	Receive Fault	RO, LH	0x0	0x0	1 = Fault on receive path, 0 = No fault
9:6	Reserved	RO	0x0	0x0	0000000
5	100GBASE-R Capable	RO	0x0	0x0	1 = PCS is able to support 100GBASE-R PCS types 0 = PCS is not able to support 100GBASE-R PCS types
4	40GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 40GBASE-R PCS types 0 = PCS is not able to support 40GBASE-R PCS types
3	10GBASE-T Capable	RO	0x0	0x0	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types
2	Reserved	RO	0x0	0x0	Reserved
1	10GBASE-X Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types
0	10GBASE-R Capable	RO	0x1	0x1	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types

Table 316: PCS Package Identifier 1
Device 4, Register 0x300E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	0000000101000001 Marvell OUI is 0x005043

Table 317: PCS Package Identifier 2
Device 4, Register 0x300F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x03	0x03	000011
9:4	Model Number	RO	0x31	0x31	110001
3:0	Revision Number	RO	See Desc.	See Desc.	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 318: BASE-R Status1 Register
Device 4, Register 0x3020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	0
12	40G Rx Link Status	RO	0x0	0x0	1 = 40GBASE-R PCS receive link up 0 = 40GBASE-R PCS receive link down
11:4	Reserved	RO	0x00	0x00	0
3	10GBASE-R PRBS9 Test Ability	RO	0x1	0x1	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing
2	10GBASE-R PRBS31 Test Ability	RO	0x1	0x1	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing
1	40G PCS High BER	RO	0x0	0x0	1 = 40GBASE-R PCS reporting high BER 0 = 40GBASE-R PCS not reporting high BER
0	40G PCSR Block Lck	RO	0x0	0x0	1 = 40GBASE-R PCS locked to received block 0 = 40GBASE-R PCS not locked

Table 319: BASE-R PCS Status 2
Device 4, Register 0x3021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Latched Block Lock	RO, LL	0x0	0x0	1 = PCS Has Block Lock 0 = PCS Does Not Have Block Lock
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS Has Reported High BER 0 = PCS Has Not Reported High BER
13:8	Bit Error Rate Counter	RO	0x00	0x00	Bit Error Rate Counter Counter clears on read. Counter will peg at all 1s.
7:0	Errored Blocks	RO	0x00	0x00	Errored Blocks Counter Counter clears on read. Counter will peg at all 1s.

Table 320: 40GBASE-R PCS Test Pattern Control
Device 4, Register 0x302A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	0
7	Scramble_idle Test Pattern Enable	R/W	0x0	0x0	1 = Enable On Transmit Path 0 = Disable On Transmit Path
6	PRBS9 Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
5	PRBS31 Receive Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
4	PRBS31 Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored

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Table 320: 40GBASE-R PCS Test Pattern Control (Continued)
Device 4, Register 0x302A

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Transmit Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
2	Receive Test Pattern Enable	RO	0x0	0x0	Write to this bit is ignored
1	Test Pattern Select	RO	0x0	0x0	Write to this bit is ignored
0	Data Pattern Select	RO	0x0	0x0	Write to this bit is ignored

Table 321: 40GBASE-R PCS Test Pattern Error Counter
Device 4, Register 0x302B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Test Pattern Error Counter	RO	0x0000	0x0000	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s.

Table 322: 40GBASE-R PCS BER High Order Counter
Device 4, Register 0x302C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	BER High Order	RO	0x0000	0x0000	Bits 21:6 of 22-bit BER counter. Register 4.3021 should be read first. Counter clears on read of 4.3021. 22-bit Counter will peg at all 1s.

Table 323: 40GBASE-R PCS Errored Blocks High Order Counter
Device 4, Register 0x302D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	High order counter present	RO	0x1	0x1	1 = High order counter is present
14	Reserved	RO	0x0	0x0	Test Pattern Error Counter Counter clears on read. Counter will peg at all 1s.
13:0	Errored blocks high order	RO	0x0000	0x0000	Bits 21:8 of 22-bits Errored Blocks Counter. Register 4.3021 should be read first. Counter clears on read of 4.3021. 22-bit Counter will peg at all 1s.

Table 324: Multi-lane BASE-R PCS Alignment Status 1
Device 4, Register 0x3032

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	0x0	0x0	
12	PCS Lane Alignment Status	RO	0x0	0x0	1 = PCS receive lanes locked and aligned 0 = PCS receive lanes not locked and aligned
11:4	Reserved	RO	0x00	0x00	

Table 324: Multi-lane BASE-R PCS Alignment Status 1 (Continued)
Device 4, Register 0x3032

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Lane 3 Block Lock	RO	0x0	0x0	1 = Lane 3 is locked 0 = Lane 3 is not locked
2	Lane 2 Block Lock	RO	0x0	0x0	1 = Lane 2 is locked 0 = Lane 2 is not locked
1	Lane 1 Block Lock	RO	0x0	0x0	1 = Lane 1 is locked 0 = Lane 1 is not locked
0	Lane 0 Block Lock	RO	0x0	0x0	1 = Lane 0 is locked 0 = Lane 0 is not locked

Table 325: Multi-lane BASE-R PCS Alignment Status 2
Device 4, Register 0x3034

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	
3	Lane 3 Aligned	RO	0x0	0x0	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked
2	Lane 2 Aligned	RO	0x0	0x0	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked
1	Lane 1 Aligned	RO	0x0	0x0	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked
0	Lane 0 Aligned	RO	0x0	0x0	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked

Table 326: BIP Error Counter Lanes 0 Register
Device 4, Register 0x30C8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Bip Err Count	RO	0x0000	0x0000	Lane 0 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 327: BIP Error Counter Lanes 1 Register
Device 4, Register 0x30C9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 1 Bip Err Count	RO	0x0000	0x0000	Lane 1 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

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Table 328: BIP Error Counter Lanes 2 Register
Device 4, Register 0x30CA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 2 Bip Err Count	RO	0x0000	0x0000	Lane 2 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 329: BIP Error Counter Lanes 3 Register
Device 4, Register 0x30CB

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 3 Bip Err Count	RO	0x0000	0x0000	Lane 3 BIP Error Counter Counter clears on read. Counter will peg at all 1s.

Table 330: Lanes 0 Mapping Register
Device 4, Register 0x3190

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 0 mapping	RO	0x00	0x00	PCS lane received in service interface lane 0. The content is valid when lane 0 aligned bit (4.3034.0) is set to one, and invalid otherwise.

Table 331: Lanes 1 Mapping Register
Device 4, Register 0x3191

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 1 mapping	RO	0x00	0x00	PCS lane received in service interface lane 1. The content is valid when lane 1 aligned bit (4.3034.1) is set to one, and invalid otherwise.

Table 332: Lanes 2 Mapping Register
Device 4, Register 0x3192

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	
5:0	Lane 2 mapping	RO	0x00	0x00	PCS lane received in service interface lane 2. The content is valid when lane 2 aligned bit (4.3034.2) is set to one, and invalid otherwise.

Table 333: Lanes 3 Mapping Register
Device 4, Register 0x3193

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	

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Table 333: Lanes 3 Mapping Register (Continued)
Device 4, Register 0x3193

Bits	Field	Mode	HW Rst	SW Rst	Description
5:0	Lane 3 mapping	RO	0x00	0x00	PCS lane received in service interface lane 3. The content is valid when lane 3 aligned bit (4.3034.3) is set to one, and invalid otherwise.

Table 334: 40GBASE-R4 Interrupt enable Register
Device 4, Register 0xB001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
10	Local Fault Received Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
9	Lane_alignment change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	Tx_Lane_cnt_err Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
7	JIT 0 Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
6	JIT Local-Fault Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
5	Link Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
4	High BER Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
3	Lane 3 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable

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Table 334: 40GBASE-R4 Interrupt enable Register (Continued)
Device 4, Register 0xB001

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Lane 2 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
1	Lane 1 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
0	Lane 0 Block Lock Change Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable

Table 335: 40GBASE-R4 Interrupt Status Register
Device 4, Register 0xB002

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock Change Interrupt	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Interrupt	RO,LH	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitter
10	Local Fault Received Interrupt	RO,LH	0x0	0x0	1 = Local fault received 0 = No local fault received
9	Lane_alignment change Interrupt Enable	RO,LH	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	Tx_Lane_cnt_err Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
7	JIT 0 Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
6	JIT Local-Fault Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
5	Link Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
4	High BER Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
3	Lane 3 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

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Table 335: 40GBASE-R4 Interrupt Status Register (Continued)
Device 4, Register 0xB002

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Lane 2 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
1	Lane 1 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change
0	Lane 0 Block Lock Change Interrupt	RO,LH	0x0	0x0	1= Change detected 0 = No Change

Table 336: 40GBASE-R4 PCS Real Time Status Register
Device 4, Register 0xB003

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Lane 3 AM_lock status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Lane 2 AM_lock status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
13	Lane 1 AM_lock status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
12	Lane 0 AM_lock status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
11	Local Fault Transmitted Status	RO	0x0	0x0	1 = Local fault transmitted 0 = No local fault transmitted
10	Local Fault Received Status	RO	0x0	0x0	1 = Local fault received 0 = No local fault received
9	Lane_alignment status	RO	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
8	Tx_Lane_cnt_err Status	RO	0x0	0x0	1= TX Blk dist lane cnt error. If this is set, 40GBASE-R4 won't behave as desired. 0 = No error
7	JIT 0 Lock Status	RO	0x0	0x0	1 =JIT 0 lock achieved 0 = No JIT 0 lock
6	JIT Local-Fault Lock Status	RO	0x0	0x0	1 =JIT local fault lock achieved 0 = No local fault lock
5	Link Status	RO	0x0	0x0	1 = 40GBASE-R link achieved 0 = No link
4	High BER Status	RO	0x0	0x0	1 = High BER 0 = No high BER
3	Lane 3 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock
2	Lane 2 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

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Table 336: 40GBASE-R4 PCS Real Time Status Register (Continued)
Device 4, Register 0xB003

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Lane 1 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock
0	Lane 0 Block Lock Status	RO	0x0	0x0	1 = Block lock achieved 0 = No block lock

6.4.5 XFI Common Registers

The registers in this section apply to all ports.

Table 337: XFI Common Registers - Register Map

Register Name	Register Address	Table and Page
SERDES Control Register 1	Device 4, Register 0xF003	Table 338, p. 237
Repeater mode Phase_FIFO Status	Device 4, Register 0xF008	Table 339, p. 238
FIFO and CRC Interrupt Enable	Device 4, Register 0xF00A	Table 340, p. 238
FIFO and CRC Interrupt Status	Device 4, Register 0xF00B	Table 341, p. 238
PPM FIFO Control 1	Device 4, Register 0xF00C	Table 342, p. 239
Packet Generation Control 1	Device 4, Register 0xF010	Table 343, p. 239
Packet Generation Control 2	Device 4, Register 0xF011	Table 344, p. 239
Initial Payload 0-1/Packet Generation	Device 4, Register 0xF012	Table 345, p. 240
Initial Payload 2-3/Packet Generation	Device 4, Register 0xF013	Table 346, p. 240
Packet Generation Length	Device 4, Register 0xF016	Table 347, p. 240
Packet Generation Burst Sequence	Device 4, Register 0xF017	Table 348, p. 240
Packet Generation IPG	Device 4, Register 0xF018	Table 349, p. 240
Transmit Packet Counter [15:0]	Device 4, Register 0xF01B	Table 350, p. 241
Transmit Packet Counter [31:16]	Device 4, Register 0xF01C	Table 351, p. 241
Transmit Packet Counter [47:32]	Device 4, Register 0xF01D	Table 352, p. 241
Transmit Byte Counter [15:0]	Device 4, Register 0xF01E	Table 353, p. 241
Transmit Byte Counter [31:16]	Device 4, Register 0xF01F	Table 354, p. 242
Transmit Byte Counter [47:32]	Device 4, Register 0xF020	Table 355, p. 242
Receive Packet Counter [15:0]	Device 4, Register 0xF021	Table 356, p. 242
Receive Packet Counter [31:16]	Device 4, Register 0xF022	Table 357, p. 242
Receive Packet Counter [47:32]	Device 4, Register 0xF023	Table 358, p. 243
Receive Byte Count [15:0]	Device 4, Register 0xF024	Table 359, p. 243
Receive Byte Count [31:16]	Device 4, Register 0xF025	Table 360, p. 243
Receive Byte Count [47:32]	Device 4, Register 0xF026	Table 361, p. 243
Receive Packet Error Count [15:0]	Device 4, Register 0xF027	Table 362, p. 244
Receive Packet Error Count [31:16]	Device 4, Register 0xF028	Table 363, p. 244
Receive Packet Error Count [47:32]	Device 4, Register 0xF029	Table 364, p. 244
PRBS 0 Control	Device 4, Register 0xF030	Table 365, p. 244
PRBS 0 Symbol Tx Counter [15:0]	Device 4, Register 0xF031	Table 366, p. 245
PRBS 0 Symbol Tx Counter [31:16]	Device 4, Register 0xF032	Table 367, p. 245
PRBS 0 Symbol Tx Counter [47:32]	Device 4, Register 0xF033	Table 368, p. 246
PRBS 0 Symbol Rx Counter [15:0]	Device 4, Register 0xF034	Table 369, p. 246
PRBS 0 Symbol Rx Counter [31:16]	Device 4, Register 0xF035	Table 370, p. 246
PRBS 0 Symbol Rx Counter [47:32]	Device 4, Register 0xF036	Table 371, p. 246
PRBS 0 Error Count [15:0]	Device 4, Register 0xF037	Table 372, p. 247
PRBS 0 Error Count [31:16]	Device 4, Register 0xF038	Table 373, p. 247
PRBS 0 Error Count [47:32]	Device 4, Register 0xF039	Table 374, p. 247

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Table 337: XFI Common Registers - Register Map (Continued)

Register Name	Register Address	Table and Page
PRBS 0 Elapse Timer	Device 4, Register 0xF03A	Table 375, p. 247
PRBS 1 Control	Device 4, Register 0xF040	Table 376, p. 247
PRBS 1 Symbol Tx Counter [15:0]	Device 4, Register 0xF041	Table 377, p. 249
PRBS 1 Symbol Tx Counter [31:16]	Device 4, Register 0xF042	Table 378, p. 249
PRBS 1 Symbol Tx Counter [47:32]	Device 4, Register 0xF043	Table 379, p. 249
PRBS 1 Symbol Rx Counter [15:0]	Device 4, Register 0xF044	Table 380, p. 249
PRBS 1 Symbol Rx Counter [31:16]	Device 4, Register 0xF045	Table 381, p. 250
PRBS 1 Symbol Rx Counter [47:32]	Device 4, Register 0xF046	Table 382, p. 250
PRBS 1 Error Count [15:0]	Device 4, Register 0xF047	Table 383, p. 250
PRBS 1 Error Count [31:16]	Device 4, Register 0xF048	Table 384, p. 250
PRBS 1 Error Count [47:32]	Device 4, Register 0xF049	Table 385, p. 251
PRBS 1 Elapse Timer	Device 4, Register 0xF04A	Table 386, p. 251
Power Management TX state control	Device 4, Register 0xF074	Table 387, p. 251

Table 338: SERDES Control Register 1
Device 4, Register 0xF003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	Set to 0s
13	Ftygr_1byte_ipg	R/W	0x0	Retain	1 = In Ftygkr mode PPM_FIFO will do ppm adjustments maintaining up to a min of one byte of IPG (Just the /T/). 0 = PPM_FIFO will do ppm adjustments maintaining up to a min of 5 bytes of IPG(/ T I I I I /)
12	Host Loopback	R/W	0x0	0x0	1 = Enable Loopback 0 = Normal Operation
11	Reserved	RO	0x0	0x0	0
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Reserved	RO	0x0	0x0	0
8	Receiver Power Down	R/W	0x0	Retain	1 = Receiver Powered Down 0 = Receiver Can Power Up
7	Force Signal Detect	R/W	0x0	Retain	1 = Force signal detect to be good 0 = Normal Operation
6	Block Transmit On Loopback	R/W	0x0	Retain	0 = Do not block ingress path 1 = Block ingress path
5:0	Reserved	R/W	0x00	Retain	Set to 0s.

Table 339: Repeater mode Phase_FIFO Status
Device 4, Register 0xF008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	Set to 0
2	Repxg-X phase_FIFO error	RO,LH	0x0	0x0	This bit is latched HIGH whenever Repxg-X phase_FIFO empty or full flag is asserted. Cleared on read.
1	Repxg-R phase_FIFO full	RO,LH	0x0	0x0	This bit is latched HIGH whenever Repxg-R phase_FIFO full flag is asserted. Cleared on read.
0	Repxg-R phase_FIFO empty	RO,LH	0x0	0x0	This bit is latched HIGH whenever Repxg-R phase_FIFO empty flag is asserted. Cleared on read.

Table 340: FIFO and CRC Interrupt Enable
Device 4, Register 0xF00A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	Set to 0
2	CRC Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	FIFO Overflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	FIFO Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 341: FIFO and CRC Interrupt Status
Device 4, Register 0xF00B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	0x0000	0
2	CRC Interrupt Status	RO,LH	0x0	0x0	This interrupt will be set only if the packet checker is enabled. 1 = CRC Error detected 0 = CRC error not detected
1	FIFO Overflow Status	RO,LH	0x0	0x0	1 = FIFO overflow occurred 0 = FIFO overflow did not occur
0	FIFO Underflow Status	RO,LH	0x0	0x0	1 = FIFO underflow occurred 0 = FIFO underflow did not occur

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Table 342: PPM FIFO Control 1
Device 4, Register 0xF00C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	PPM FIFO Depth	R/W	0x0	0x0	PPM FIFO depth selection Default setting varies based on the PCS mode. 10GBASE-R, XAUI, RXAUI: 01 40GBASE-R4: 11 Else: 00
13:0	Reserved	RO	0x0000	0x0000	Set to 0s

Table 343: Packet Generation Control 1
Device 4, Register 0xF010

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Read Clear	R/W	0x0	Retain	1= Enable clear on read 0 = Use 4.F010.6 to clear counters
14:7	Reserved	R/W	0x00	0x00	Set to 0s.
6	Pkt-Gen/Chk Counter Reset	R/W, SC	0x0	0x0	This bit self clears after counters are cleared. 1 = Clear counters, 0 = Normal Operation
5:3	Reserved	RO	0x0	0x0	0000
2	Use SFD in Checker	R/W	0x0	0x0	0 = Look for SFD before starting CRC checking 1 = Start CRC checking after the first 8 bytes in packet
1	Transmit Test Pattern Enable	R/W	0x0	0x0	1 = Pkt generator enable, 0 = Disable
0	Receive Test Pattern Enable	R/W	0x0	0x0	1 = Pkt checker enable, 0 = Disable

Table 344: Packet Generation Control 2
Device 4, Register 0xF011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	Set to 0s
7:4	Internal Packet Generation Control	R/W	0x0	Retain	000x = No Mask 0010 = Invert every other word 0011 = 2 no invert, 2 invert 0100 = Left shift byte 0101 = Right shift byte 0110 = Left shift word 0111 = Right shift word 1000 = Increment byte 1001 = decrement byte 1010 = Pseudo random byte 1011 = Pseudo random word 11xx = reserved
3	CRC Generation	R/W	0x0	Retain	0 = On, 1 = off
2:0	Reserved	RO	0x0	Retain	Set to 0s

Table 345: Initial Payload 0-1/Packet Generation
Device 4, Register 0xF012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Byte 1	R/W	0x00	Retain	Initial payload value for byte 1
7:0	Byte 0	R/W	0x00	Retain	Initial payload value for byte 0

Table 346: Initial Payload 2-3/Packet Generation
Device 4, Register 0xF013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Byte 3	R/W	0x00	Retain	Initial payload value for byte 1
7:0	Byte 2	R/W	0x00	Retain	Initial payload value for byte 0

Table 347: Packet Generation Length
Device 4, Register 0xF016

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Number Of Bytes In Frame	R/W	0x0000	Retain	0000 = Random length between 64 bytes to 1518 bytes 0001 = Random length between 64 bytes to 0x0FFF bytes 0002 = Random length between 64 bytes to 0x1FFF bytes 0003 = Random length between 64 bytes to 0x3FFF bytes 0004 = Random length between 64 bytes to 0x7FFF bytes 0005 = Random length between 64 bytes to 0xFFFF bytes 0006 to 0007 = Undefined 0008 to FFFF = Length in number of bytes

Table 348: Packet Generation Burst Sequence
Device 4, Register 0xF017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Number Of Packets To Send	R/W	0x0000	Retain	0000 = Stop generation 0001 to FFFE = Number of packets to send FFFF = Continuous

Table 349: Packet Generation IPG
Device 4, Register 0xF018

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Random IPG	R/W	0x0	Retain	0 = Fixed IPG per bits 14:0 1 = Random IPG from 5 bytes to value specified per bits 14:0
14:0	IPG Duration	R/W	0x0002	Retain	Each bit equals 4 bytes of idle

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Table 350: Transmit Packet Counter [15:0]
Device 4, Register 0xF01B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [15:0]	RO	0x0000	0x0000	Counts the total number of packets transmitted. If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read.

Table 351: Transmit Packet Counter [31:16]
Device 4, Register 0xF01C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [31:16]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F01B first in order to update this register. This ensures that the 48 bit read is atomic.

Table 352: Transmit Packet Counter [47:32]
Device 4, Register 0xF01D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [47:32]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F01B first in order to update this register. This ensures that the 48 bit read is atomic.

Table 353: Transmit Byte Counter [15:0]
Device 4, Register 0xF01E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [15:0]	RO	0x0000	0x0000	Counts the total number of bytes in frame (including premable) transmitted. If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read.

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Table 354: Transmit Byte Counter [31:16]
Device 4, Register 0xF01F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [13:16]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F01E first in order to update this register. This ensures that the 48 bit read is atomic.

Table 355: Transmit Byte Counter [47:32]
Device 4, Register 0xF020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Byte Count [47:32]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F01E first in order to update this register. This ensures that the 48 bit read is atomic.

Table 356: Receive Packet Counter [15:0]
Device 4, Register 0xF021

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [15:0]	RO	0x0000	0x0000	Counts the total number of packets received. If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read.

Table 357: Receive Packet Counter [31:16]
Device 4, Register 0xF022

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [31:16]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F021 first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 358: Receive Packet Counter [47:32]
Device 4, Register 0xF023

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [47:32]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F021 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 359: Receive Byte Count [15:0]
Device 4, Register 0xF024

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [15:0]	RO	0x0000	0x0000	Counts the total number of bytes in frame (including premable) received. If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read.

Table 360: Receive Byte Count [31:16]
Device 4, Register 0xF025

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [31:16]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F024 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 361: Receive Byte Count [47:32]
Device 4, Register 0xF026

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Byte Count [47:32]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F024 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 362: Receive Packet Error Count [15:0]
Device 4, Register 0xF027

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [15:0]	RO	0x0000	0x0000	Counts the number of packets with CRC Error received. If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read.

Table 363: Receive Packet Error Count [31:16]
Device 4, Register 0xF028

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [31:16]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F027 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 364: Receive Packet Error Count [47:32]
Device 4, Register 0xF029

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Error Count [47:32]	RO	0x0000	0x0000	If 4.F010.14 = 0 then register does not clear on read. Cleared only when register 4.F010.6 transitions from 0 to 1. If 4.F010.14 = 1 then register clear on read. Must read register 4.F027 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 365: PRBS 0 Control
Device 4, Register 0xF030

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	Set to 0s.
14	BER_mode_en	R/W	0x1	Retain	0 = Legacy mode of error count accumulation 1 = BER mode enabled for error accumulation. This is used for average Bit Error Rate (BER) calculation.
13	Read Clear	R/W	0x0	Retain	1= Enable clear on read 0 = Use 4.F030.6 to clear counters
12:9	Reserved	R/W	0x0	0x0	Set to 0s.
8	PRBS Lock	RO	0x0	0x0	1 = PRBS locked, 0 = PRBS not locked
7	Immediate Error Count Enable	R/W	0x0	0x0	1 = Count PRBS errors before locking 0 = Wait until PRBS locks before counting
6	PRBS Counter Reset	R/W, SC	0x0	0x0	This bit self clears after counters are cleared. 1 = Clear counters, 0 = Normal Operation

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Table 365: PRBS 0 Control (Continued)
Device 4, Register 0xF030

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Transmit Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. 1 = Enable 0 = Disable
4	Receive Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. Note that there is no receive checking done for IEEE 48.A.1, 48.A.2, and 48.A.3. 1 = Enable 0 = Disable
3:0		R/W	0x0	0x0	0000 = IEEE 49.2.8 - PRBS 31 0001 = PRBS 7 0010 = PRBS 9 IEEE 83.7 0011 = PRBS 23 0100 = PRBS 31 Inverted 0101 = PRBS 7 Inverted 1000 = PRBS 15 1001 = PRBS 15 Inverted 0110 = PRBS 9 Inverted 0111 = PRBS 23 Inverted 1100 = High frequency pattern 1101 = Low frequency pattern 1110 = Mixed frequency pattern 1111 = Square Wave pattern

Table 366: PRBS 0 Symbol Tx Counter [15:0]
Device 4, Register 0xF031

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit transmitted per lane. If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read.

Table 367: PRBS 0 Symbol Tx Counter [31:16]
Device 4, Register 0xF032

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [31:16]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 368: PRBS 0 Symbol Tx Counter [47:32]
Device 4, Register 0xF033

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [47:32]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 369: PRBS 0 Symbol Rx Counter [15:0]
Device 4, Register 0xF034

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit received per lane. If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read.

Table 370: PRBS 0 Symbol Rx Counter [31:16]
Device 4, Register 0xF035

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [31:16]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 371: PRBS 0 Symbol Rx Counter [47:32]
Device 4, Register 0xF036

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [47:32]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 372: PRBS 0 Error Count [15:0]
Device 4, Register 0xF037

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit error received per lane. If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read.

Table 373: PRBS 0 Error Count [31:16]
Device 4, Register 0xF038

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [31:16]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F037 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 374: PRBS 0 Error Count [47:32]
Device 4, Register 0xF039

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 0 Error Count [47:32]	RO	0x0000	0x0000	If 4.F030.13 = 0 then register does not clear on read. Cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F037 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 375: PRBS 0 Elapse Timer
Device 4, Register 0xF03A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Elapse Timer Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every 2 second. Valid only if 4.F030.14 = 1 If 4.F030.13 = 0 then register does not clear on read, but cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F030.13 = 1 then register clear on read. Must read register 4.F037 first in order to update this register.

Table 376: PRBS 1 Control
Device 4, Register 0xF040

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	Set to 0s.

Table 376: PRBS 1 Control (Continued)
Device 4, Register 0xF040

Bits	Field	Mode	HW Rst	SW Rst	Description
14	BER_mode_en	R/W	0x1	0x1	0 = Legacy mode of error count accumulation 1 = BER mode enabled for error accumulation. This is used for average Bit Error Rate (BER) calculation.
13	Read Clear	R/W	0x0	Retain	1= Enable clear on read 0 = Use 4.F040.6 to clear counters
12:9	Reserved	R/W	0x0	0x0	Set to 0s.
8	PRBS Lock	RO	0x0	0x0	1 = PRBS locked 0 = PRBS not locked
7	Immediate Error Count Enable	R/W	0x0	0x0	1 = Count PRBS errors before locking 0 = Wait until PRBS locks before counting
6	PRBS Counter Reset	R/W, SC	0x0	0x0	This bit self clears after counters are cleared. 1 = Clear counters 0 = Normal Operation
5	Transmit Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. 1 = Enable 0 = Disable
4	Receive Test Pattern Enable	R/W	0x0	0x0	Test enabled only if the appropriate mode is selected. Note that there is no receive checking done for IEEE 48.A.1, 48.A.2, and 48.A.3. 1 = Enable 0 = Disable
3:0		R/W	0x0	0x0	0000 = IEEE 49.2.8 - PRBS 31 0001 = PRBS 7 0010 = PRBS 9 IEEE 83.7 0011 = PRBS 23 0100 = PRBS 31 Inverted 0101 = PRBS 7 Inverted 1000 = PRBS 15 1001 = PRBS 15 Inverted 0110 = PRBS 9 Inverted 0111 = PRBS 23 Inverted 1100 = High frequency pattern 1101 = Low frequency pattern 1110 = Mixed frequency pattern 1111 = Square Wave pattern

Note

This selection is valid in any SERDES speed.

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Table 377: PRBS 1 Symbol Tx Counter [15:0]
Device 4, Register 0xF041

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit transmitted per lane. If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read.

Table 378: PRBS 1 Symbol Tx Counter [31:16]
Device 4, Register 0xF042

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [31:16]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 379: PRBS 1 Symbol Tx Counter [47:32]
Device 4, Register 0xF043

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Transmit Count [47:32]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F031 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 380: PRBS 1 Symbol Rx Counter [15:0]
Device 4, Register 0xF044

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit received per lane. If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read.

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Table 381: PRBS 1 Symbol Rx Counter [31:16]
Device 4, Register 0xF045

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [31:16]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 382: PRBS 1 Symbol Rx Counter [47:32]
Device 4, Register 0xF046

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count [47:32]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F034 first in order to update this register. This ensures that the 48 bit read is atomic.

Table 383: PRBS 1 Error Count [15:0]
Device 4, Register 0xF047

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 1 Error Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every bit error received per lane. If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read.

Table 384: PRBS 1 Error Count [31:16]
Device 4, Register 0xF048

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 1 Error Count [31:16]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F03A first in order to update this register. This ensures that the 48 bit read is atomic.

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Table 385: PRBS 1 Error Count [47:32]
Device 4, Register 0xF049

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Lane 1 Error Count [47:32]	RO	0x0000	0x0000	If 4.F040.13 = 0 then register does not clear on read. Cleared only when register 4.F040.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F03A first in order to update this register. This ensures that the 48 bit read is atomic.

Table 386: PRBS 1 Elapse Timer
Device 4, Register 0xF04A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Elapse Timer Count [15:0]	RO	0x0000	0x0000	Increments by 1 for every 2 second. Valid only if 4.F040.14 = 1 If 4.F040.13 = 0 then register does not clear on read, but cleared only when register 4.F030.6 transitions from 0 to 1. If 4.F040.13 = 1 then register clear on read. Must read register 4.F047 first in order to update this register.

Table 387: Power Management TX state control
Device 4, Register 0xF074

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	Writing to this section is forbidden
13	Rg_en_rst_dsp_s	R/W	0x1	Retain	0=Disable 1 = Enable
12:0	Reserved	RO	0x0000	0x0000	Writing to this section is forbidden

6.4.6 XFI SERDES Registers

The transmitter comes up with default settings which can be read back from registers in Table 389 to Table 396. If manual forcing of transmitter amplitude/pre/post emphasis is desired, it can be achieved by writing to the same registers. Here register address 1E.80E6 should be read as 0x1E.0x80E6 and so on.

Table 388: XFI SERDES Registers - Register Map

Register Name	Register Address	Table and Page
XFI Transmitter Lane 0 Settings	Register 0x1E.0x80E6	Table 389, p. 252
XFI Transmitter Lane 0 Settings	Register 0x1E.0x80E7	Table 390, p. 252
XFI Transmitter Lane 1 Settings	Register 0x1E.0x82E6	Table 391, p. 253
XFI Transmitter Lane 1 Settings	Register 0x1E.0x82E7	Table 392, p. 253
XFI Transmitter Lane 2 Settings	Register 0x1E.0x84E6	Table 393, p. 253
XFI Transmitter Lane 2 Settings	Register 0x1E.0x84E7	Table 394, p. 253
XFI Transmitter Lane 3 Settings	Register 0x1E.0x86E6	Table 395, p. 254
XFI Transmitter Lane 3 Settings	Register 0x1E.0x86E7	Table 396, p. 254

Table 389: XFI Transmitter Lane 0 Settings
Register 0x1E.0x80E6

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 390: XFI Transmitter Lane 0 Settings
Register 0x1E.0x80E7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

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Table 391: XFI Transmitter Lane 1 Settings
Register 0x1E.0x82E6

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 392: XFI Transmitter Lane 1 Settings
Register 0x1E.0x82E7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

Table 393: XFI Transmitter Lane 2 Settings
Register 0x1E.0x84E6

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 394: XFI Transmitter Lane 2 Settings
Register 0x1E.0x84E7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

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Table 395: XFI Transmitter Lane 3 Settings
Register 0x1E.0x86E6

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force Enable	R/W	0x0	Retain	Force enable for bit 14:0 and next register bit 15:0 0 = This register and next register are read back values 1 = This register and next register are forced values
14	Spare	R/W	0x0	Retain	
13:8	Pre-cursor tap	R/W	0x0	Retain	n0[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Main tap	R/W	0x0	Retain	n1[5:0]

Table 396: XFI Transmitter Lane 3 Settings
Register 0x1E.0x86E7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Spares	R/W	0x0	Retain	
13:8	Post Cursor Tap	R/W	0x0	Retain	n2[5:0]
7:6	Spares	R/W	0x0	Retain	
5:0	Remaining Tap	R/W	0x0	Retain	nrst[5:0]

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7 Electrical Specifications

This section includes information on the following topics:

- Section 7.1, Absolute Maximum Ratings
- Section 7.2, Recommended Operating Conditions
- Section 7.3, Package Thermal Information
- Section 7.4, Current Consumption
- Section 7.5, Digital I/O Electrical Specifications
- Section 7.6, XFI
- Section 7.7, SFI
- Section 7.8, Reference Clock
- Section 7.9, Latency

7.1 Absolute Maximum Ratings

Table 397: Absolute Maximum Ratings[1]

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDA15}	Power Supply Voltage on AVDD15_N and AVDD15_M with respect to VSS	-0.5		1.8	V
V_{DDA11}	Power Supply Voltage on AVDD11_N with respect to VSS	-0.5		1.5	V
V_{DDA10}	Power Supply Voltage on AVDD10_M with respect to VSS	-0.5		1.5	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.5	V
V_{DDO}	Power Supply Voltage on VDDOT, VDDOS, VDDOL, and VDDOM with respect to VSS	-0.5		3.6	V
V_{PIN}	Voltage applied to any digital input pin	-0.5		5.0 or VDDO + 0.7, whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[2]	°C

1. On power-up, no special power supply sequencing is required.
2. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

7.2 Recommended Operating Conditions

Table 398: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDA15}[1]	AVDD15_M supply	For AVDD15_M	1.425	1.5	1.575	V
V_{DDA11}[1]	AVDD11_N supply	For AVDD11_N	1.045	1.1	1.155	V
V_{DDA10}[1]	AVDD10_M supply	For AVDD10_M	0.95	1.0	1.05	V
V_{DD}	DVDD supply	For DVDD at 1.0V	0.95	1.0	1.05	V
V_{DDO}	VDDOT, VDDOS, VDDOL, and VDDOM supply	For VDDO at 1.2V	1.14	1.2	1.26	V
		For VDDO at 1.5V	1.425	1.5	1.575	V
		For VDDO at 1.8V	1.71	1.8	1.89	V
		For VDDO at 2.5V	2.375	2.5	2.625	V
		For VDDO at 3.3V	3.13	3.3	3.47	V
RSET	Internal bias reference	Resistor connected to V_{SS}		3650 ± 1% tolerance		Ω
T_A	Commercial Ambient operating temperature		0		70[2]	°C
T_J	Maximum junction temperature				125[3]	°C

1. Maximum noise allowed on supplies is 20 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g, 45 °C ~55 °C. The 70 °C max is Marvell specification limit
3. Refer to white paper on TJ Thermal Calculations for more information.

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7.3 Package Thermal Information

7.3.1 Thermal Conditions for 324-Pin FCBGA Package

Table 399: Thermal Conditions for 324-pin FCBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient for the 324-Pin, FCBGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		11.7		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		10.0		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		9.2		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		8.7		°C/W
ψ_{JT}	Thermal characteristic parameter[a] - junction to top center of the 324-Pin, FCBGA package $\psi_{JT} = (T_J-T_{top})/P$. P = Total power dissipation, T_{top}: Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.4		°C/W
θ_{JC}	Thermal resistance[a] - junction to case for the 324-Pin, FCBGA package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow		0.6		°C/W
θ_{JB}	Thermal resistance[a] - junction to board for the 324-Pin, FCBGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		3.1		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

7.4 Current Consumption

Warning Current consumption numbers are estimates at this time and are subject to change.

The current consumption is broken down by each power supply. The total current consumption for each power supply is calculated by summing the various components in the tables below. The total chip power consumption is calculated as follows:

$$I_{supply_Total} = I_{supply_Base} + \sum_{N-0}^{3} I_{supply_PCS}(\text{port N}) + \sum_{N-0}^{3} I_{supply_MS}(\text{port N})$$

I_{supply_PCS} =Current consumption for the PCS selected. 0 mA if the port is turned off.

I_{supply_DSP} =Incremental current consumption when the Electronic Dispersion Compensation DSP Engine is enabled, otherwise 0 mA.

Supply is one of AVDD15, AVDD11, AVDD10, and DVDD.

The current consumption numbers for I_{supply_PCS} and I_{supply_MS} are per port.

The current consumption numbers for I_{supply_DSP} is per active lane on the line side.

Table 400: Base Current Consumption (Per Chip)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDD15_Base}	1.5V analog supply	AVDD15_M AVDD15_N	All ports powered down		80	90	mA
I_{AVDD11_Base}	1.1V analog supply	AVDD11_N	All ports powered down		20	140	mA
I_{AVDD10_Base}	1.0V analog supply	AVDD10_M	All ports powered down		110	230	mA
I_{DVDD_Base}	1.0V digital supply	DVDD	All ports powered down		640	3380	mA

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Table 401: AVDD15 Current Consumption by Mode (Per Port)

Symbol	Parameter	Pins	Condition (host, line)	Min	Typ	Max	Units
I_{AVDD15_PCS}	1.5V analog supply	AVDD15_M AVDD15_N	1000BASE-X, 1000BASE-X		340	390	mA
			10GBASE-R, 10GBASE-R		470	520	mA
			XAUI, 10GBASE-R		1130	1240	mA
			RXAUI, 10GBASE-R		680	740	mA
			40GBASE-R4, 40GBASE-R4		1890	2140	mA
			Dual 1000BASE-X, 1000BASE-X		540	600	mA
			Dual 10GBASE-R, 10GBASE-R		700	790	mA
			1000BASE-X, Dual 1000BASE-X		480	570	mA
			10GBASE-R, Dual 10GBASE-R		710	770	mA

Table 402: AVDD11 Current Consumption by Mode (Per Port)

Symbol	Parameter	Pins	Condition (host, line)	Min	Typ	Max	Units
I_{AVDD11_PCS}	1.1V analog supply	AVDD11_N	1000BASE-X, 1000BASE-X		100	110	mA
			10GBASE-R, 10GBASE-R		140	150	mA
			XAUI, 10GBASE-R		130	160	mA
			RXAUI, 10GBASE-R		130	140	mA
			40GBASE-R4, 40GBASE-R4		520	560	mA
			Dual 1000BASE-X, 1000BASE-X		100	110	mA
			Dual 10GBASE-R, 10GBASE-R		130	140	mA
			1000BASE-X, Dual 1000BASE-X		200	220	mA
			10GBASE-R, Dual 10GBASE-R		260	270	mA

Table 403: AVDD10 Current Consumption by Mode (Per Port)

Symbol	Parameter	Pins	Condition (host, line)	Min	Typ	Max	Units
I_{AVDD10_PCS}	1.0V analog supply	AVDD10_M	1000BASE-X, 1000BASE-X		20	20	mA
			10GBASE-R, 10GBASE-R		30	40	mA
			XAUI, 10GBASE-R		80	80	mA
			RXAUI, 10GBASE-R		40	40	mA
			40GBASE-R4, 40GBASE-R4		160	160	mA
			Dual 1000BASE-X, 1000BASE-X		30	30	mA
			Dual 10GBASE-R, 10GBASE-R		80	80	mA
			1000BASE-X, Dual 1000BASE-X		20	20	mA
			10GBASE-R, Dual 10GBASE-R		40	40	mA

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Table 404: DVDD Current Consumption by Mode (Per Port)

Symbol	Parameter	Pins	Condition (host, line)	Min	Typ	Max	Units
I_{DVDD_PCS}	1.0V digital supply	DVDD	1000BASE-X, 1000BASE-X		40	50	mA
			10GBASE-R, 10GBASE-R		470	640	mA
			XAUI, 10GBASE-R		520	620	mA
			RXAUI, 10GBASE-R		500	570	mA
			40GBASE-R4, 40GBASE-R4		1950	2410	mA
			Dual 1000BASE-X, 1000BASE-X		70	80	mA
			Dual 10GBASE-R, 10GBASE-R		520	800	mA
			1000BASE-X, Dual 1000BASE-X		50	170	mA
			10GBASE-R, Dual 10GBASE-R		870	1010	mA

7.5 Digital I/O Electrical Specifications

7.5.1 DC Operating Conditions

Table 405: DC Operating Conditions

All digital I/O are on one of four supply rails – VDDOT, VDDOS, VDDOL, and VDDOM. Each supply rail can be independently programmed to operate at 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V. See section Section 3.12.4, DVDD, on page 85 for more details.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0		VDDO + 0.6V	V
			VDDO = 2.5V	1.75		VDDO + 0.6V	V
			VDDO = 1.8V	1.26		VDDO + 0.6V	V
			VDDO = 1.5V	1.05		VDDO + 0.6V	V
			VDDO = 1.2V	0.84		VDDO + 0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V	-0.3		0.8	V
			VDDO = 2.5V	-0.3		0.75	V
			VDDO = 1.8V	-0.3		0.54	V
			VDDO = 1.5V	-0.3		0.45	V
			VDDO = 1.2V	-0.3		0.36	V
VOH	High level output voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 4 mA			0.4	V
I_{ILK}	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA
CIN	Input capacitance	All pins				5	pF

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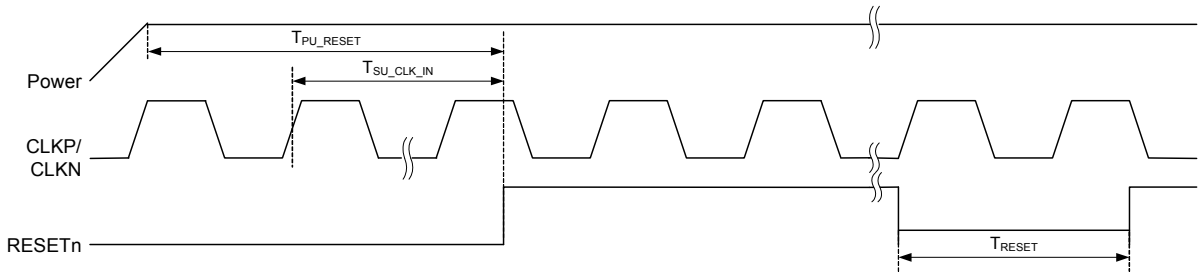
7.5.2 Reset Timing

Table 406: Reset Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESET de-assertion	10			ms
$T_{SU_CLK_IN}$	Number of valid CLKP/CLKN cycles prior to RESET de-assertion	50			clks
T_{RESET}	Minimum reset pulse width during normal operation	10			ms

Figure 32: Reset Timing



7.5.3 MDC/MDIO Management Interface Timing

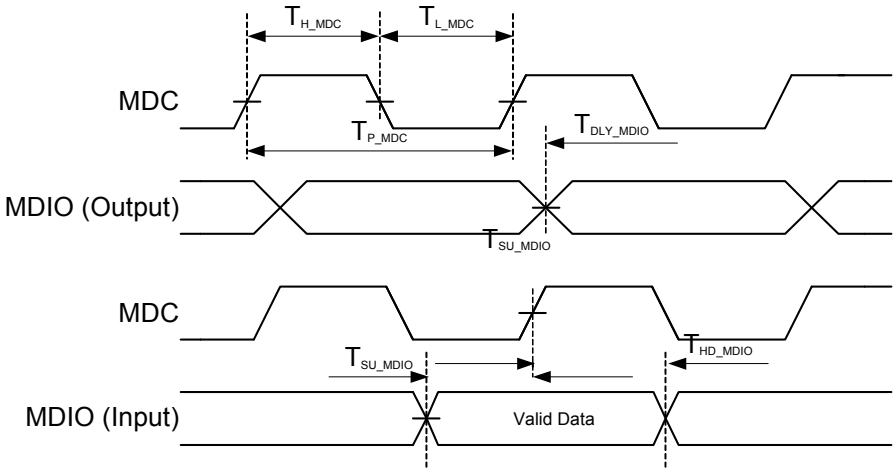
Table 407: MDC/MDIO Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	25 pf load on MDIO	3.5 ns + half cycle		19	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		6.5			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		0.5			ns
T_{P_MDC}	MDC Period	Subject to T_{READ_DLY}	25[1]			ns
T_{H_MDC}	MDC High		12			ns
T_{L_MDC}	MDC Low		12			ns
T_{READ_DLY}	Two MDC Period during Read Turnaround. For details, see Section 3.4.2, High-Speed MDC/MDIO Management Interface Protocol, on page 51.		80			ns

1. T_{P_MDC} is minimum of 25 ns for 40 MHz MDC clock support with stretched TA, but 40 ns (25 MHz) with standard TA as per IEEE specification. MDC of 40 MHz is supported only with VDDO supply of 1.8V and above. For lower VDDO, MDC frequency of up to 25 MHz is supported.

Figure 33: MDC/MDIO Management Interface



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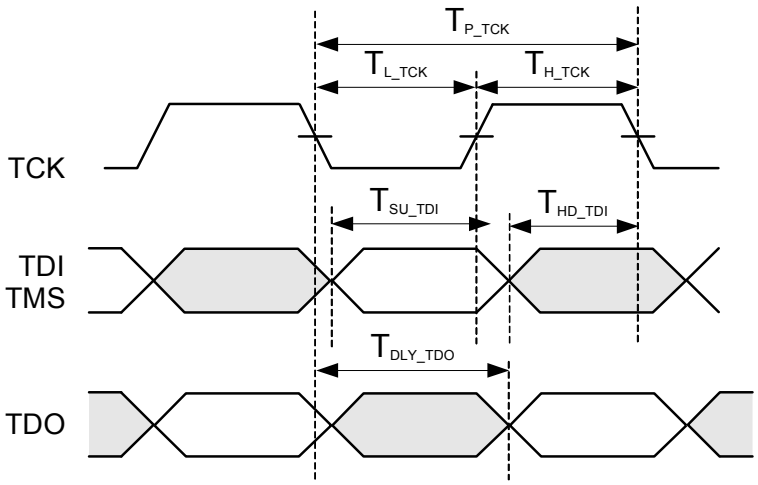
7.5.4 JTAG Timing

Table 408: JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	60			ns
T_{H_TCK}	TCK High	12			ns
T_{L_TCK}	TCK Low	12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	10			ns
T_{DLY_TDO}	TCK to TDO Delay	0		15	ns

Figure 34: JTAG Timing



7.5.5 Two-wire Serial Interface (Master) Timing

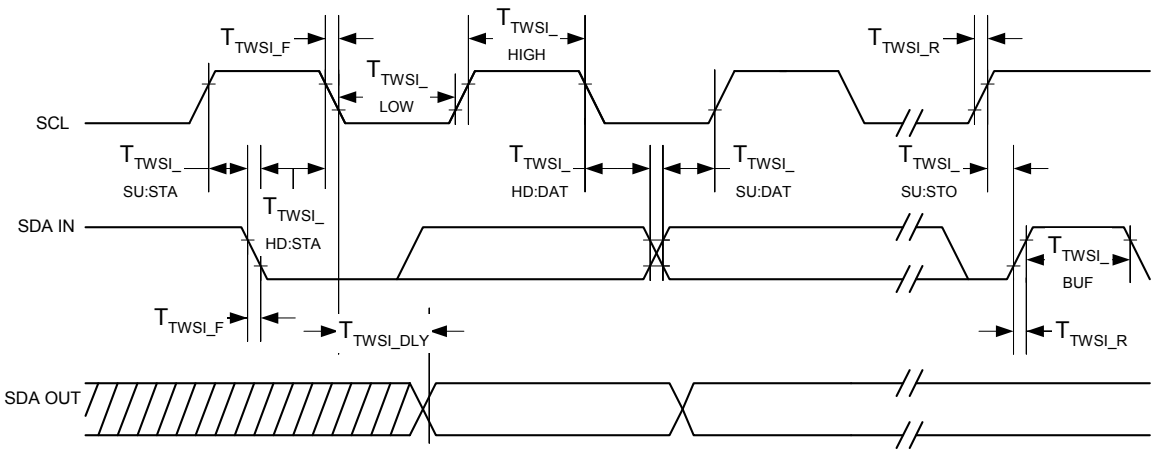
Table 409: Two-wire Serial Interface (Master) Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SSCL Clock Frequency	100 kHz	100		400	kHz
T_{TWSI_NS}	Noise Suppression Time at SSDA Inputs	100 kHz			80	ns
T_{TWSI_R}	SSCL/SSDA Rise time	100 kHz			1000	ns
T_{TWSI_F}	SSCL/SSDA Fall Time	100 kHz			300	ns
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000			ns
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700			ns
$T_{TWSI_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700			ns
$T_{TWSI_HD:STA}$	Start Condition Hold Time	100 kHz	4000			ns
$T_{TWSI_SU:STO}$	Stop Condition Setup Time	100 kHz	4000			ns
$T_{TWSI_SU:DAT}$	Data in Setup Time	100 kHz	250			ns
$T_{TWSI_HD:DAT}$	Data in Hold Time	100 kHz	300			ns
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700			ns
T_{TWSI_DLY}	SSCL Low to SSDA Data Out Valid	100 kHz	40		200	ns

Note SSCL clock stretching is not supported.

Figure 35: TWSI Master Timing



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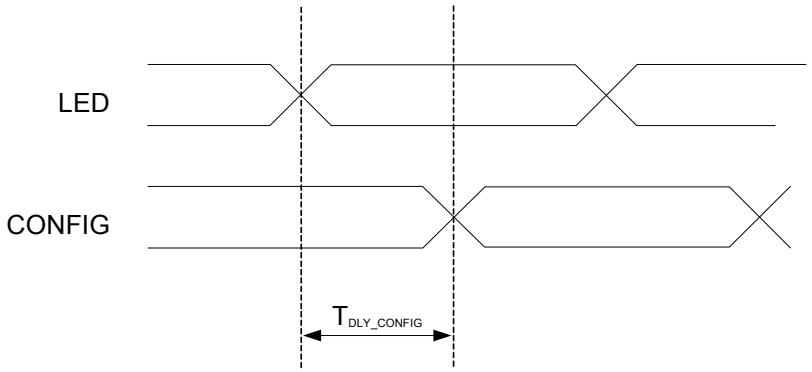
7.5.6 LED to CONFIG Timing

Table 410: LED to CONFIG Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay	0		25	ns

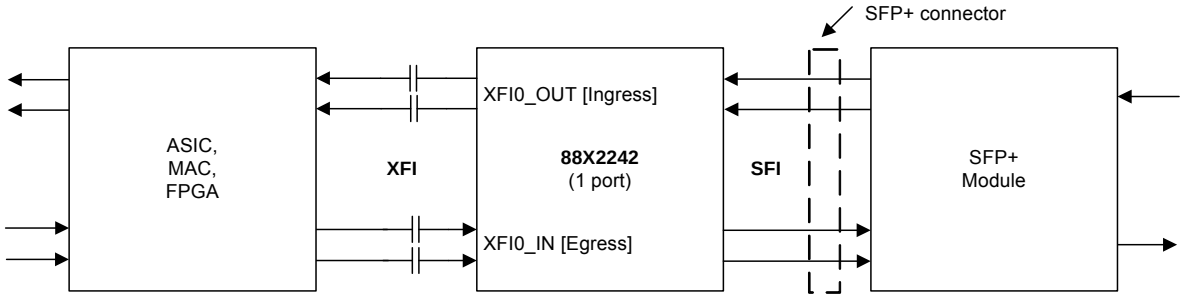
Figure 36: LED to CONFIG Timing



7.6 XFI

7.6.1 XFI Application Reference Model

Figure 37: XFI Application Reference Model



The high-speed 10G serial electrical module interface includes XFI0_OUTP/N and XFI0_INP/N pins. All high-speed SFI I/Os should be AC-coupled.

7.6.2 XFI Output (XFI[3:0]_OUT) Specifications

The specifications shown in Table 411 and Table 412 are at 10.3125G at the output of the chip measured with a minimal loss channel terminated into 2×50Ω through AC coupling.

Table 411: XFI[3:0]_OUT Electrical Specifications

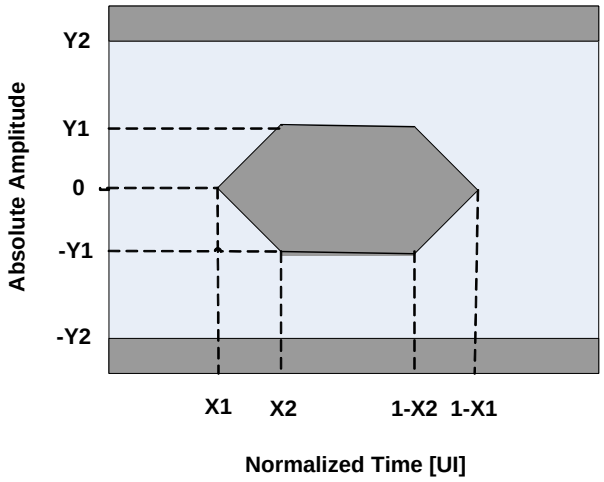
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{diff}	Differential Output Voltage		Note[1]		Note[1]	
ΔZ_M	Termination Mismatch	See INF-8077i section 3.6			5	%
	Output AC Common Mode Voltage	See INF-8077i section 3.6			15	mV (RMS)
t_{RH}, t_{FH}	Output Rise and Fall times [20% to 80%]	Note[2]	24			ps
SDD22	Differential Output Reflection Coefficient	0.05 - 0.1 GHz	20			dB
		0.1 - 7.5 GHz	10			
SCC22	Common Mode Output Reflection Coefficient	0.1 - 15 GHz	6			dB

1. Differential output voltage shall meet the Y1 and Y2 eye mask values in Table 412
2. The eye mask limits the maximum output rise and fall times.

Table 412: XFI[3:0]_OUT Jitter Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
DJ	Deterministic Jitter	See INF-8077i section 3.6			0.15	UI_{pp}
TJ	Total Jitter				0.30	UI_{pp}
X1	Eye Mask	See INF-8077i section 3.6			0.15	UI
X2					0.40	UI
Y1			180			mV
Y2					385	mV

Figure 38: XFI[3:0]_OUT Differential Output Compliance Mask



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7.6.3 XFI[3:0]_OUT 1GE Specifications

All voltage and jitter specifications at 1.25G are identical to the specifications at 10.3125G. Jitter and mask parameters scale with data rate (same UI values).

7.6.4 XFI Receiver (XFI[3:0]_IN) Input Specifications

The specifications shown in Table 413 and Table 414 are at 10.3125G at the input of the chip measured with a minimal loss channel from a test equipment of 2×50Ω impedance through AC coupling.

Note XFI receiver specifications are generally based on datacom applications for FC-PI-3, point D. Point D sinusoidal jitter tolerance specifications account for the peaking impairments of a CDR in an XFP module. However, the 88X2242 device's receiver is located at the same point in a system where FC-PI-3 defines a module to be, which is point B. Since there is no CDR in this path, the sinusoidal jitter tolerance requirements for point B are used.

Table 413: XFI[3:0]_IN Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input AC Common Mode Voltage Tolerance	See FC-PI-3 section D.5.2				15	mV_{rms}
SDD11	Differential Input Reflection Coefficient	0.05 - 0.1 GHz	20			dB
		0.1 - 7.5 GHz	10			
SCC11		0.1 - 15 GHz	6			dB
SCD11	Differential to Common Mode Conversion	0.1 - 15 GHz	12			dB

Table 414: XFI[3:0]_IN Jitter and Mask Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
TJ	Total Jitter	See INF-8077i section 3.6			0.65	UI
	Total non-EQJ Jitter				0.45	UI
SJ	Sinusoidal Jitter Tolerance				See[1]	
X1	Eye Mask				0.325	
Y1	Eye Mask		55			
Y2	Eye Mask				525	

1. Sinusoidal jitter tolerance for datacom is given in Figure 40 on page 268.

Figure 39: XFI[3:0]_OUT Differential Channel Input Compliance Mask

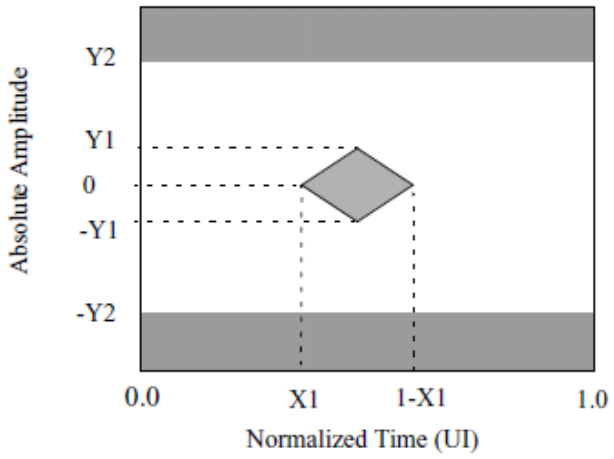
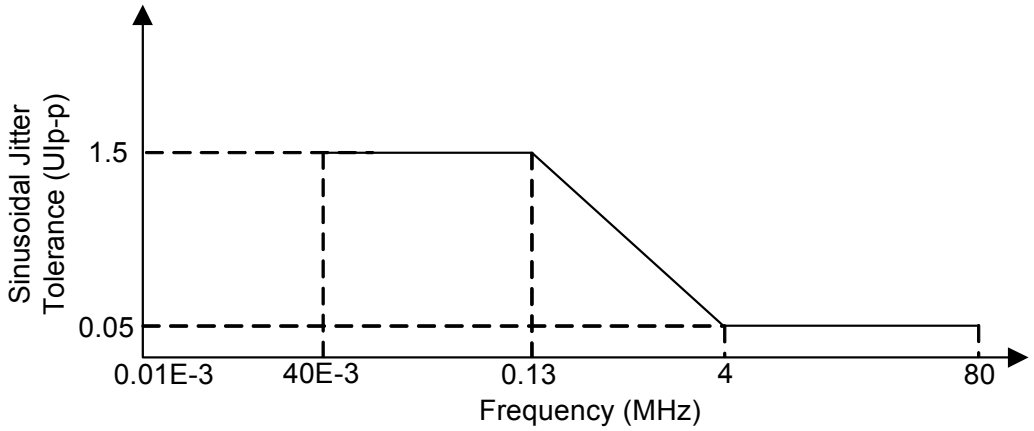


Figure 40: XFI[3:0]_IN Sinusoidal Jitter Tolerance Template at 10.3125G



7.6.5 XFI[3:0]_IN 1GE Specifications

All voltage and jitter specifications at 1.25G are identical to the specifications at 10.3125G, except that the maximum input voltage swing that can be tolerated is 850 mV pk-pk. Jitter parameters scale with data rate (same UI values). Sinusoidal jitter tolerance frequencies scale with data rate.

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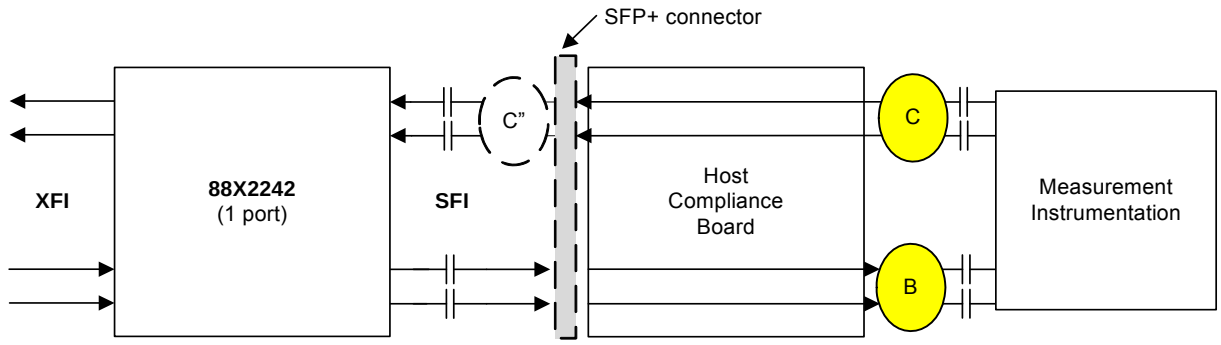
7.7 SFI

7.7.1 SFI Specification Reference Model

Figure 41: SFI Specification Reference Model



The high-speed 10G serial electrical module interface includes SFI0_OUTP/N and SFI0_INP/N pins. All high-speed SFI I/Os should be AC-coupled.

The SFI adheres to the electrical specifications for both limiting and linear interfaces defined in the SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module “SFP+”. For definitions for test points C”, B, and C, see SFF-8431.

7.7.2 SFI[3:0]_OUT

The full set of 10G parameters and test conditions for output specifications at Test Point B are described in SFF8431 section 3.5.1 and section E.2 for a host channel which applies to the recommendations in Annex A of SFF-8431.

Table 415: SFI[3:0]_OUT Output Electrical Specifications at B

Symbol	Parameter	Condition	Min	Typ	Max	Units
S_{EOVR}	Single Ended Output Voltage Range		-0.3		4.0	V
ΔZ_M	Termination Mismatch	See SFF-8431 section D.16, Figure 55			5	%
	Output AC Common Mode Voltage	See SFF-8431, D.15			15	$mV_{(RMS)}$
SDD22	Differential Output S-parameter	0.01 - 2 GHz			-12	dB
		2 - 11.1 GHz			See[1]	
SCC22	Common Mode Output S-parameter	0.01 - 2.5 GHz			See[2]	dB
		2.5 - 11.1 GHz			-3	

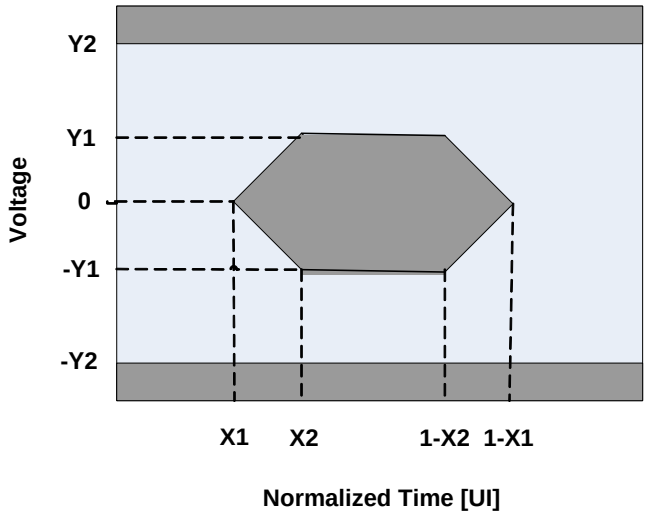
1. Reflection coefficient given by equation SDD22(dB) < -6.68 + 12.1×log10(f/5.5), with f in GHz.
2. Reflection coefficient given by equation SCC22(dB) < -7 + 1.6×f, with f in GHz.

Table 416: SFI[3:0]_OUT Output Jitter and Eye Mask Specifications at B

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_r, T_f	Crosstalk Source Rise/Fall Time (20% - 80%)	See[1] SFF-8431, D.6		34		ps
	Crosstalk Source Amplitude (p-p differential)	See[1] SFF-8431, D.7		1000		mV
T_r, T_f	Signal Rise/Fall time (20% - 80%)	See SFF-8431, D.6	34			ps
TJ	Total Jitter	See SFF-8431, D.5			0.28	UI_{pp}
DDJ	Data Dependent Jitter	See SFF-8431, D.3			0.1	UI_{pp}
DDPWS	Data Dependent Pulse Width Shrinkage				0.055	UI_{pp}
UJ	Uncorrelated Jitter	See SFF-8431, D.4			0.023	UI_{rms}
Q_{sq}	Transmitter Q_{sq}	See SFF-8431, D8	50			
Eye Mask	X1	Mask hit ratio of $5x10^{-5}$ see SFF-8431, D.2, Figure 42		0.12		UI
	X2			0.33		UI
	Y1			95		mV
	Y2			350		mV
VMA	Voltage Modulation Amplitude	See SFF-8431, D.7	300			mVpp
TWDPc	Output TWDP	See[2], [3]			10.7	dBe

1. Measured at C" with Host Compliance Board and Module Compliance Board pair, see SFF-8431 Figure 42.
2. Electrical output measured with LRM 14 taps FFE and 5 taps DFE Equalizer with PRBS9 for copper direct attached stressor, see SFF-8431 Appendix G.
3. The stressor for TWDPc is given in SFF-8431Table 34 and is included in the code in SFF-8431 Appendix G.

Figure 42: SFI[3:0]_OUT Output Mask for 10.3125 Gbps Operation



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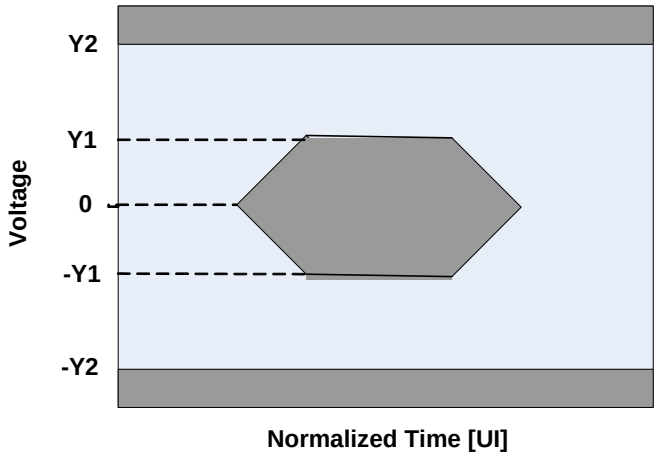
7.7.3 SFI[3:0]_OUT 1GE Specifications

Specifications for 1.25 Gbps are per SFP-8431 section F.2 for the B point and assume the same channel recommendation as in SFF-8431 Annex A. 1G jitter specs at B are per IEEE 802.3 clause 38.5, TP1.

Table 417: SFI[3:0]_OUT Requirements to Support 1.25 Gbps Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{out}	SFI Output VMA Differential		500			mV
DJ	Deterministic Jitter	Assumes the channel recommendations in SFF-8431 Annex A.			0.1	UI
TJ	Total Jitter				0.24	UI
Eye Mask	Y1	See SFF-8431, D.2 and Figure 43	150			mV
	Y2		500			mV

Figure 43: SFI[3:0]_OUT Output Mask for 1.25 Gbps Operation



7.7.4 SFI[3:0]_IN

The full set of 10G parameters and test conditions for Test Point C are described in SFF-8431 sections 3.5.2 and E.3 with channels per the SFP channel specs SFF-8431 section A. This includes both linear and limiting.

Table 418: SFI[3:0]_IN Input Electrical Specifications at C

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Single Ended Input Voltage	Referenced to V_{eeR}	-0.3		4.0	V
	Input AC Common Mode Voltage Tolerance	See[1] and SFF-8431 D.15	7.5			mV_{rms}
	Damage Threshold (p-p differential)	See[1]	2000			mV

Table 418: SFI[3:0]_IN Input Electrical Specifications at C (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
SDD11	Differential Input S-parameter	0.01 to 2 GHz			-12	dB
		2 to 11.1 GHz			See[2]	
SCD11	Reflected Differential to Common Mode Conversion	0.1 to 11.1 GHz			-10	dB

1. Measured at C" with the Module Compliance Board.
2. Reflection Coefficient given by equation SDD11(dB) < -6.68 + 12.1×$\log_{10}$(f/5.5), with f in GHz.

Table 419: SFI[3:0]_IN Supporting Limiting Module Input Compliance Test Signal Calibrated at C"

Symbol	Parameter	Condition	Min	Target	Max	Units
T_r, T_f	Crosstalk Source Rise/Fall time (20%-80%)	SFF-8431, D.6		34		ps
	Crosstalk Source Amplitude (p-p differential)	See[1]		700		mV
	AC Common Mode Voltage	See [2] and SFF-8431, D.15			7.5	mV_{rms}
J2	99% Jitter	See [3] and SFF-8431, D.5, D.11		0.42		UI_{pp}
TJ	Total Jitter	BER $1x10^{-12}$, See SFF-8431 D.5, D11		0.70		UI_{pp}
DDPWS	Pulse Width Shrinkage Jitter	See [4] and SFF-8431, D.3		0.3		UI_{pp}
X1	Eye Mask	Mask hit ratio of $1x10^{-12}$, see SFF-8431 D.2, D11 and Figure 44		0.35		UI
Y1	Eye Mask Amplitude Sensitivity[5, 8]			150		mV
Y2	Eye Mask Amplitude Overload[6, 7, 8]			425		mV

1. Measured at B" with host Compliance Board and Module Compliance Board pair, see SFF-8431 Figure 16.
2. The tester is not expected to generate this common mode voltage however its output must not exceed this value.
3. Includes sinusoidal jitter, per SFF-8431 figure 21, when measured with the reference PLL specified by the relevant IEEE standard.
4. In practice the test implementer may trade DDPWS with other pulse width shrinkage from the sinusoidal interferer.
5. Eye mask amplitude sensitivity tests the host receiver with the minimum eye opening expected at the input within the constraint set by Y2.
6. Eye mask amplitude overload test the host receiver tolerance to the largest peak signal levels expected at the input within the constraint set by Y1.
7. It is not expected that module Rx output will exhibit both maximum peak level and minimum eye opening.
8. Sensitivity and overload are tested separately, see SFF-8431 D.11.

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Figure 44: SFI[3:0]_IN Input Compliance Mask at C" Supporting Limiting Module

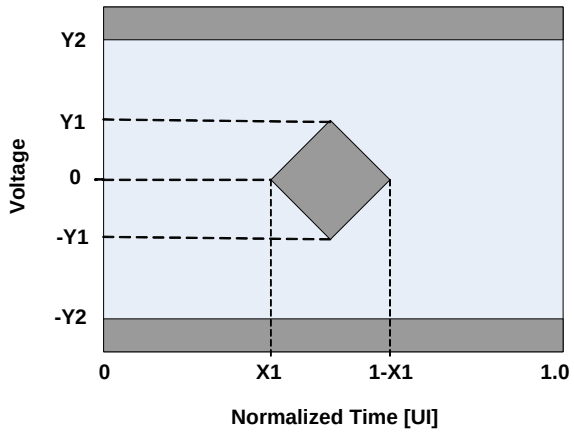

Table 420: SFI[3:0]_IN Linear Passive Copper Module Compliance Test Signal Calibrated at C"

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_r, T_f	Crosstalk Source Rise/Fall time (20%-80%)	See [1], SFF-8431, D.6		34		ps
	Crosstalk Source Amplitude (p-p differential)	See [1]		700		mV
	AC Common Mode Voltage	See[2] and SFF-8431, D.15			7.5	mV_{rms}
VMA	Differential Voltage Modulation Amplitude	For LRM see[3]	180		600	mV
	Differential Voltage Modulation Amplitude	For SR and LR see[3]	150		600	mV

1. Measured at B" with host Compliance Board and Module Compliance Board pair, see SFF-8431 Figure 16.
2. The tester is not expected to generate this common mode voltage however its output must not exceed this value.
3. Peak levels of received signals in service may exceed their VMA due to overshoot of the far end transmitter and/or the module receiver.

Table 421: SFI[3:0]_IN Linear Optical Module Compliance Test Signal Calibrated at C”

Symbol	Applications	Compliance Stress Test Conditions, see[1] and[2] SFF-8431 D.13	Target WDP (dBo)	Target RN, (rms)		WDPi (dBo)
				m	b	
WDP	LRM	High WDP & precursor stressor	Approx. 5.1, see[3]	0.014	0.0477	4.1
		High WDP & split symmetric stressor	5.4	8		3.9
		High WDP & post cursor stressor	Approx. 5.2, see[3]			4.2
		Low WDP & precursor stressor	Approx. 4.7, see[4]			4.1
		Low WDP & split symmetric stressor	Approx 4.7, see[4]			3.9
		Low WDP & post cursor stressor	Approx. 4.8, see[3]			4.2
	LR	Low WDP	Approx. 2.6, see[4]	-0.02	0.096	1.9

1. Target WDP is calibrated with a reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps.
2. Target RN rms values are given by the following equation: RN=m×(WDP-WDPi)+b, where WDP is the actual value of the tester, and WDPi values are based on wave shapes expected at TP3.
3. The filter bandwidth in the TP3 to electrical adapter in SFF-8431 figure 52 is set to produce 5.4 dBo for WDP for the split-symmetrical TP3 stressor. The same filter is to be used for high WDP pre-cursor LRM stressors – their approximate target WDP values are given only for guidance. WDP is to measured for each stressor, and target RN is determined by the relevant equation in note 2.
4. The filter bandwidth in TP3 to electrical adaptor in SFF-8431 Figure 52 is set to 7.5 GHz for all three LRM low WDP conditions and for LR condition. The approximate target WDP values are given for guidance. WDP is to measured for each stressor, and target RN is determined by relevant equation in note 2.

For LR, the SFP+ linear host shall operate with sinusoidal jitter given by Figure 12 in SFF-8431, while the stress conditions given in Table 421 are applied. For LRM, the host shall operate with sinusoidal jitter as defined in IEEE802.3 clause 68, with the other stressors and noises in SFF-8431, Figure 52 turned off, including those in the TP3 tester.

Table 422: SFI[3:0]_IN Linear Passive Copper Compliance Test Signal Calibrated at C”

Symbol	Parameter	Condition	Min	Typ Target	Max	Units
WDPc	Waveform Distortion Penalty of the ISI Generator	See[1, 2]		9.3		dBe
Q_{sq}	Transmitter Q_{sq}	See[3, 4]		63.1		
N_o	Post channel fixed noise source	See[5]		2.14		mV_{rms}
VMA	Differential Voltage Modulation Amplitude	See[3]		180		mV
	Differential Peak-Peak Voltage Overload			700		mV
	Input AC Common Mode Voltage	See[6] and SFF-8431 D.15.2			13.5	mV_{rms}

1. Copper stressor as defined in SFF-8431 table 36. WDPc is measured with reference receiver with 14 FFE tabs and with 5 DFE taps, see SFF-8431 Appendix G.
2. WDPc for the stress is smaller than the transmitter TWDPc due the VMA loss in the host stressor.
3. Square patterns with eight ONEs and eight ZEROs.

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4. Q_{sq}=1/RN if the one level and zero level noises are identical and see SFF-8431 D.8. Qsq is calibrated at the output of the MCB in a 12 GHz bandwidth with the ISI of the channel model in SFF-8431 figure 61 disabled. The source for No should be disabled during this calibration.
5. N_o is the rms voltage measured over one symbol period at the output of the MCB in a 12 GHz bandwidth. The source for Qsq should be disabled during this calibration.
6. AC common mode target value is achieved by adjusting relative delay of the P and N signals.

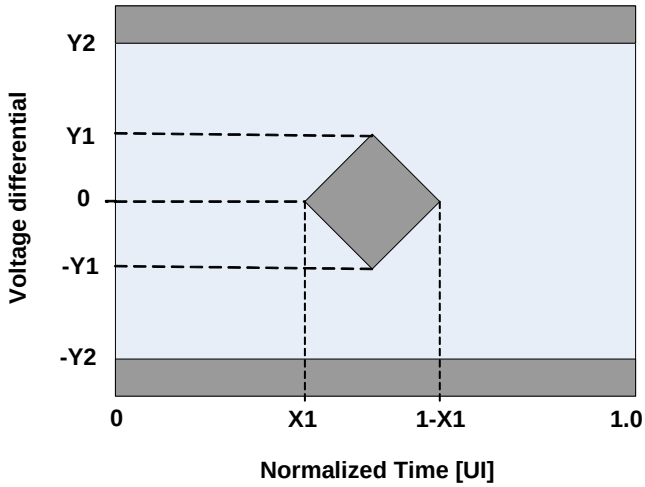
7.7.5 SFI[3:0]_IN 1GE Specifications

1G voltage and jitter specifications are given in Table 423 and Figure 45. 1G jitter specs at C are per IEEE 802.3 clause 38.5, TP4.

Table 423: SFI[3:0]_IN Input Specifications at 1.25 Gbps at Point C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	SFI Input VMA Differential		370			mV
DJ	DJ Jitter	Assumes channel recommendations in SFF-8431 Annex A.			0.46	UI
TJ	Total Jitter				0.75	UI
Eye Mask	Y1	See SFF-8431 D.2 and Figure 45	125			mV
	Y2		600			mV

Figure 45: SFI0_IN Input Mask for 1.25 Gbps Operation



7.8 Reference Clock

Table 424: Reference Clock

Symbol	Parameter	Condition	Min	Typ	Max	Units
Fclk	Frequency	REF_CLK is 156.25 MHz.	-100 ppm	156.25	+100 ppm	MHz
tr, tf	Rise, fall time	20%-80% of swing	0.3	0.5	0.8	ns
Vppd	Amplitude	Differential pk-pk	0.4	0.8	1.6	V

Table 424: Reference Clock (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input Voltage Limits	Single-ended	0.0		AVDD15	V
Tduty	Duty cycle		0.45	0.5	0.55	
Tjit	Jitter	Integrated from 1-30 MHz			0.5	ps, rms
Zin	Input Impedance	Differential	90	100	110	Ω
Vicm	Input CM	CLK can be DC coupled	0.1	0.85	AVDD15 - 0.1	V
SDD11	Input Return Loss	Differential, 100Ω			-12	db

Figure 46: Reference Clock Input Waveform

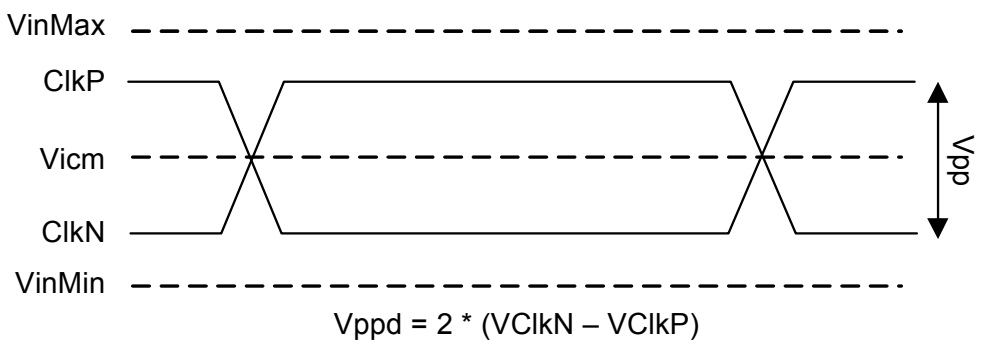
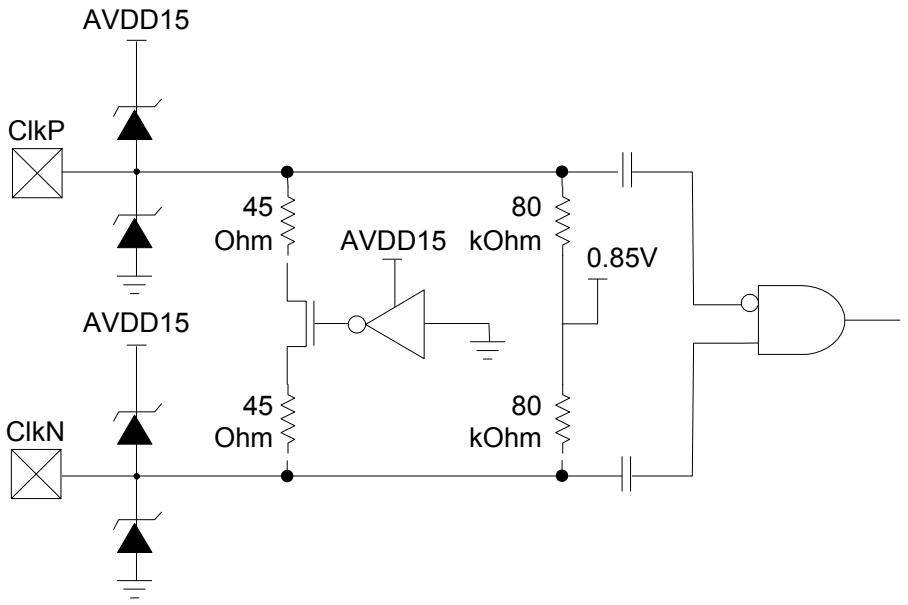


Figure 47: Simplified Reference Clock Input Schematics



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7.9 Latency

The latency is calculated from the tables below by summing the various components.

Total Egress Latency = $T_{EGRESS} + T_{FEC_TX}$.

Total Ingress Latency = $T_{INGRESS} + T_{SFI_DSP} + T_{FEC_RX}$.

Total Egress Latency = T_{EGRESS}

Total Ingress Latency = $T_{INGRESS}$

T_{EGRESS} and $T_{INGRESS}$ are based on the datapath selected.

Table 425: Egress Latency

Symbol	Parameter	Condition (host, line)	Min	Typ	Max	Units
T_{EGRESS}	Egress Path Latency	1000BASE-X, 1000BASE-X	451		473	ns
		10GBASE-R, 10GBASE-R	160		171	ns
		XAUI, 10GBASE-R	243		268	ns
		RXAUI, 10GBASE-R	206		227	ns
		40GBASE-R4, 40GBASE-R4	353		362	ns

Table 426: Ingress Latency

Symbol	Parameter	Condition (host, line)	Min	Typ	Max	Units
$T_{INGRESS}$	Ingress Path Latency	1000BASE-X, 1000BASE-X	451		473	ns
		10GBASE-R, 10GBASE-R	160		171	ns
		XAUI, 10GBASE-R	184		227	ns
		RXAUI, 10GBASE-R	161		169	ns
		40GBASE-R4, 40GBASE-R4	353		362	ns

Table 427: Electronic Dispersion Compensation DSP Latency

Symbol	Parameter	Condition (host, line)	Min	Typ	Max	Units
T_{SFI_DSP}	Incremental EDC Latency	10GBASE-R				ns

Table 428: FEC Latency

Symbol	Parameter	Condition (host, line)	Min	Typ	Max	Units
T_{FEC_TX}	Transmit FEC Latency	10GBASE-R and 40GBASE-R4			13	ns
T_{FEC_RX}	Receive FEC Latency	10GBASE-R and 40GBASE-R4			269	ns

8 Mechanical Drawings

Figure 48: 324-Pin FCBGA Package Mechanical Drawings - Top View

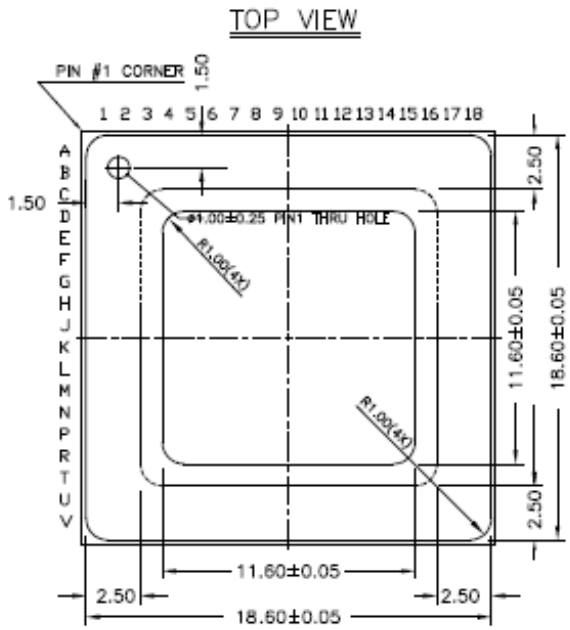

Figure 49: 324-Pin FCBGA Package Mechanical Drawings - Side View

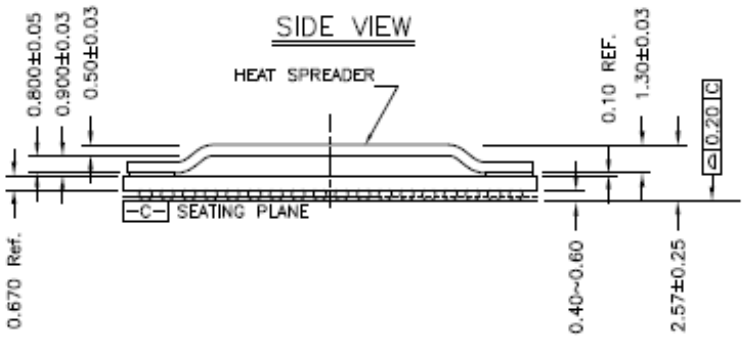

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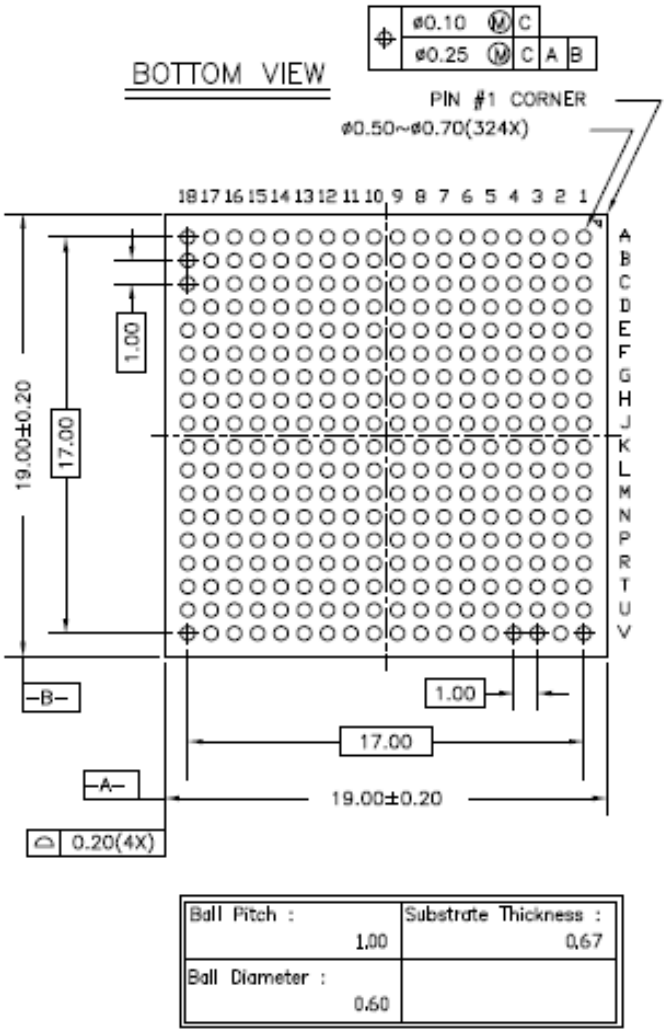
Figure 50: 324-Pin FCBGA Package Mechanical Drawings - Bottom View



9 Part Order Numbering/Package Marking

This section includes information on the following topics:

- Section 9.1, Part Order Numbering
- Section 9.2, Package Marking

9.1 Part Order Numbering

Figure 51 shows the part order numbering scheme for the 88X2242 device. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 51: Sample Part Number

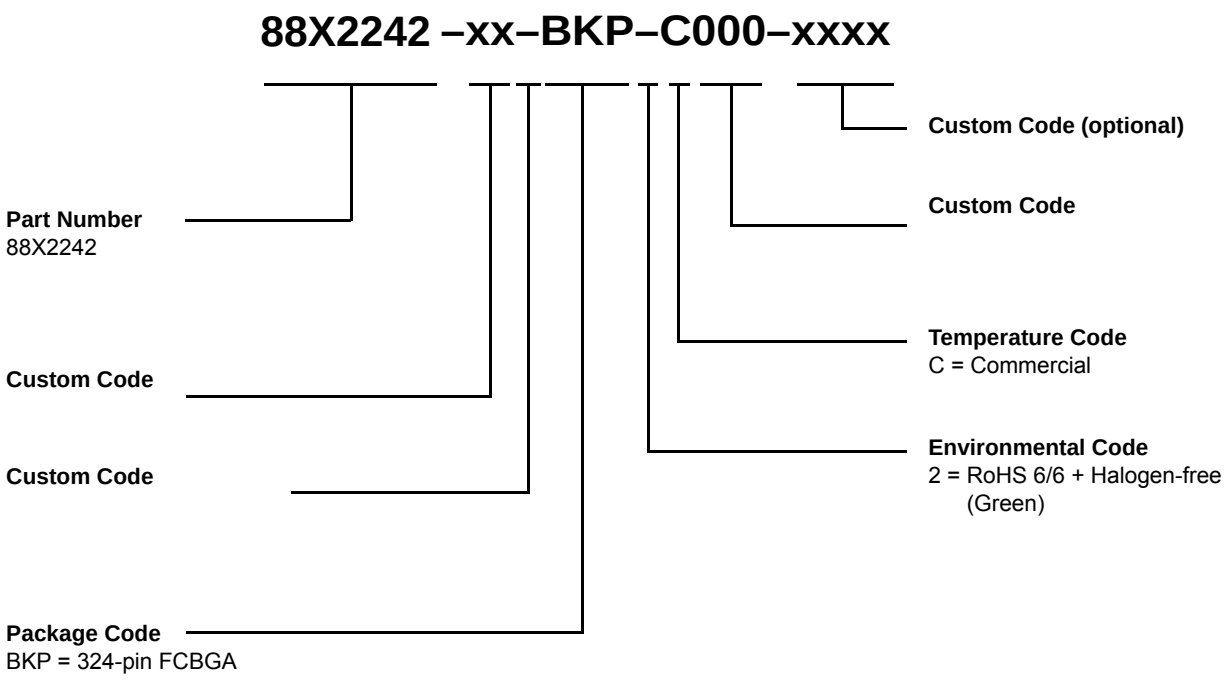


Table 429: 88X2242 Device Part Order Options

Package Type	Part Order Number
Commercial	
324-pin FCBGA	88X2242-xx-BKP2C000 (Commercial, Green, RoHS 6/6 + Halogen-free compliant package)

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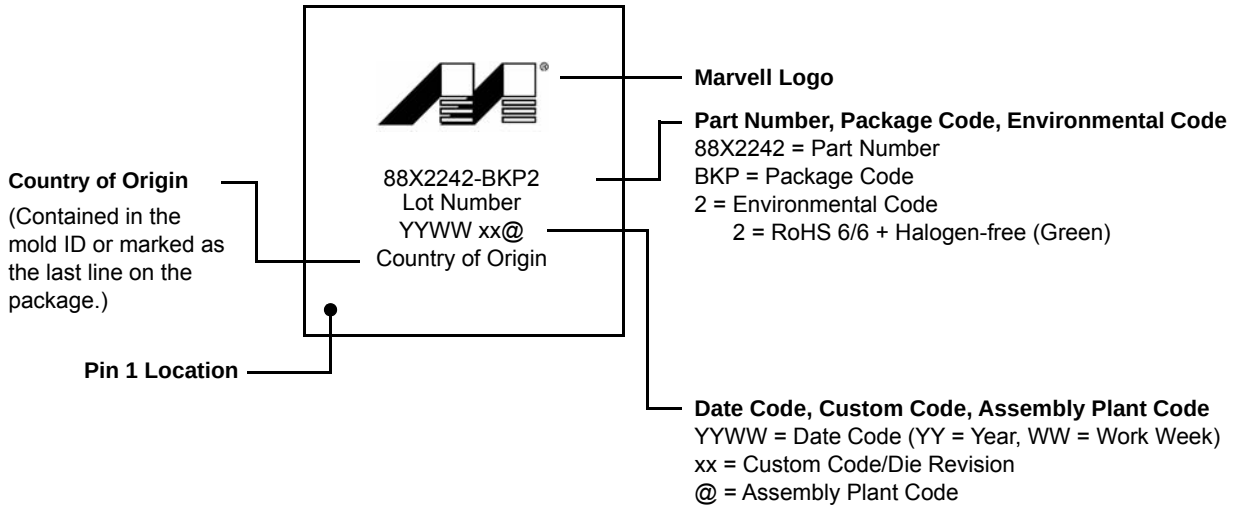
9.2 Package Marking

Figure 52 shows a sample Commercial package marking and pin 1 location for the 88X2242.

Figure 52: Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Acronyms and Abbreviations

API	Application Programming Interface
ECC	Error Correction Circuit
EDC	Electronic Dispersion Compensation
FAE	Field Application Engineer
MDIO	Management Data Input/Output
PCS	
PLL	Phase Lock Loop
SFD	Start of Frame Delimiter
TAP	Test Access Port
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TRSTn	Test Reset Input
TWSI	Two-Wire Serial Interface

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B Revision History

Table 430: Revision History

Revision	Date	Section	Detail
Rev. B	May 16, 2018	All applicable	Cosmetic enhancements
		Chip Level Functional Description	Figure 18: Interrupt Source - Line Port Interrupt Masked Status (Third Level): updated
		Register Description	Table 95: PMA/PMD Devices In Package 1: updated bit [2]
			Table 120: PCS Devices In Package 1: updated bit [2]
			Table 167: PCS Devices In Package 1: updated bit [2]
			Table 246: PCS Devices in Package 1: updated bit [2]
			Table 265: PCS Devices In Package 1: updated bit [2]
			Table 312: PCS Devices In Package 1: updated bit [2]
		Mechanical Drawings	Separated Figure 46: 324-Pin FCBGA Package Mechanical Drawings - Top View into Figure 48: 324-Pin FCBGA Package Mechanical Drawings - Top View and Figure 49: 324-Pin FCBGA Package Mechanical Drawings - Side View
		Part Order Numbering/Package Marking	Changed “HFCBGA” to “FCBGA” in Figure 51: Sample Part Number and Table 429 88X2242 Device Part Order Options
		Acronyms and Abbreviations	New appendix added
Rev. A	March 9, 2018	All applicable	Initial release

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