

**RL78/G1A**

R01DS0151EJ0210

RENESAS MCU

Rev.2.10

Nov 30, 2016

Combines Multi-channel 12-Bit A/D Converter, True Low Power Platform (as low as 66  $\mu\text{A}/\text{MHz}$ , and 0.57  $\mu\text{A}$  for RTC + LVD), 1.6 V to 3.6 V operation, 16 to 64 Kbyte Flash, 41 DMIPS at 32 MHz

**1. OUTLINE**
**1.1 Features**
**Ultra-Low Power Technology**

- 1.6 V to 3.6 V operation from a single supply
- Stop (RAM retained): 0.23  $\mu\text{A}$ , (LVD enabled): 0.31  $\mu\text{A}$
- Halt (RTC + LVD): 0.57  $\mu\text{A}$
- Snooze: 0.7 mA (UART), 0.6 mA (ADC)
- Operating: 66  $\mu\text{A}/\text{MHz}$

**16-bit RL78 CPU Core**

- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

**Code Flash Memory**

- Density: 16 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

**Data Flash Memory**

- Data Flash with background operation
- Data flash size: 4 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 3.6 V

**RAM**

- 2 KB to 4 KB size options
- Supports operands or instructions
- Back-up retention in all modes

**High-speed On-chip Oscillator**

- 32 MHz with +/- 1% accuracy over voltage (1.8 V to 3.6 V) and temperature (-20  $^{\circ}\text{C}$  to +85  $^{\circ}\text{C}$ )
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz

**Reset and Supply Management**

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 12 setting options (Interrupt and/or reset function)

**Data Memory Access (DMA) Controller**

- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

**Multiple Communication Interfaces**

- Up to 6 x I<sup>2</sup>C master
- Up to 1 x I<sup>2</sup>C multi-master
- Up to 6 x CSI/SPI (7-, 8-bit)
- Up to 3 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

**Extended-Function Timers**

- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

**Rich Analog**

- ADC: Up to 28 channels, 12-bit resolution, 3.375  $\mu\text{s}$  conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

**Safety Features (IEC or UL 60730 compliance)**

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

**General Purpose I/O**

- 3.6 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

**Operating Ambient Temperature**

- Standard: -40  $^{\circ}\text{C}$  to +85  $^{\circ}\text{C}$
- Extended: -40  $^{\circ}\text{C}$  to +105  $^{\circ}\text{C}$

**Package Type and Pin Count**

From 3 mm x 3 mm to 10 mm x 10 mm  
 QFP: 48, 64  
 QFN: 32, 48  
 LGA: 25  
 BGA: 64

## ○ ROM, RAM capacities

| Flash ROM | Data flash | RAM              | RL78/G1A |          |          |          |
|-----------|------------|------------------|----------|----------|----------|----------|
|           |            |                  | 25 pins  | 32 pins  | 48 pins  | 64 pins  |
| 64 KB     | 4 KB       | 4 KB <b>Note</b> | R5F10E8E | R5F10EBE | R5F10EGE | R5F10ELE |
| 48 KB     | 4 KB       | 3 KB             | R5F10E8D | R5F10EBD | R5F10EGD | R5F10ELD |
| 32 KB     | 4 KB       | 2 KB             | R5F10E8C | R5F10EBC | R5F10EGC | R5F10ELC |
| 16 KB     | 4 KB       | 2 KB             | R5F10E8A | R5F10EBA | R5F10EGA | –        |

**Note** This is about 3 KB when the self-programming function and data flash function are used. (For details, see **3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = –40 to +105°C)**)

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1A



**Caution** The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

&lt;R&gt;

Table 1-1. List of Ordering Part Numbers

| Pin count | Package  | Fields of Application <sup>Note</sup> | Ordering Part Number  |
|-----------|--|---------------------------------------|---|
| 25 pins   | 25-pin plastic WFLGA<br>(3 × 3 mm, 0.5 mm pitch)   | A                                     | R5F10E8AALA#U0, R5F10E8CALA#U0,<br>R5F10E8DALA#U0, R5F10E8EALA#U0,<br>R5F10E8AALA#W0, R5F10E8CALA#W0,<br>R5F10E8DALA#W0, R5F10E8EALA#W0 |
|           |  | G                                     | R5F10E8AGLA#U0, R5F10E8CGLA#U0,<br>R5F10E8DGLA#U0, R5F10E8EGLA#U0,<br>R5F10E8AGLA#W0, R5F10E8CGLA#W0,<br>R5F10E8DGLA#W0, R5F10E8EGLA#W0 |
| 32 pins   | 32-pin plastic HWQFN<br>(5 × 5 mm, 0.5 mm pitch)   | A                                     | R5F10EBAANA#U0, R5F10EBCANA#U0,<br>R5F10EBDANA#U0, R5F10EBEANA#U0,<br>R5F10EBAANA#W0, R5F10EBCANA#W0,<br>R5F10EBDANA#W0, R5F10EBEANA#W0 |
|           |  | G                                     | R5F10EBAGNA#U0, R5F10EBCGNA#U0,<br>R5F10EBDGNA#U0, R5F10EBEGNA#U0,<br>R5F10EBAGNA#W0, R5F10EBCGNA#W0,<br>R5F10EBDGNA#W0, R5F10EBEGNA#W0 |
| 48 pins   | 48-pin plastic LFQFP<br>(7 × 7 mm, 0.5 mm pitch)   | A                                     | R5F10EGAAFV#V0, R5F10EGCAFV#V0,<br>R5F10EGDAFV#V0, R5F10EGEAFV#V0,<br>R5F10EGAAFV#X0, R5F10EGCAFV#X0,<br>R5F10EGDAFV#X0, R5F10EGEAFV#X0 |
|           |  | G                                     | R5F10EBAGNA#V0, R5F10EBCGNA#V0,<br>R5F10EBDGNA#V0, R5F10EBEGNA#V0,<br>R5F10EBAGNA#X0, R5F10EBCGNA#X0,<br>R5F10EBDGNA#X0, R5F10EBEGNA#X0 |
|           | 48-pin plastic HWQFN<br>(7 × 7 mm, 0.5 mm pitch)   | A                                     | R5F10EGAANA#U0, R5F10EGCANA#U0,<br>R5F10EGDANA#U0, R5F10EGEANA#U0,<br>R5F10EGAANA#W0, R5F10EGCANA#W0,<br>R5F10EGDANA#W0, R5F10EGEANA#W0 |
|           |  | G                                     | R5F10EGAGNA#U0, R5F10EGCGNA#U0,<br>R5F10EGDGNA#U0, R5F10EGEGNA#U0,<br>R5F10EGAGNA#W0, R5F10EGCGNA#W0,<br>R5F10EGDGNA#W0, R5F10EGEGNA#W0 |
| 64 pins   | 64-pin plastic LFQFP<br>(10 × 10 mm, 0.5 mm pitch) | A                                     | R5F10ELCAFV#V0, R5F10ELDADFV#V0, R5F10ELEAFV#V0,<br>R5F10ELCAFV#X0, R5F10ELDADFV#X0, R5F10ELEAFV#X0                                     |
|           |  | G                                     | R5F10ELCGFV#V0, R5F10ELDGFV#V0,<br>R5F10ELEGFV#V0,<br>R5F10ELCGFV#X0, R5F10ELDGFV#X0, R5F10ELEGFV#X0                                    |
|           | 64-pin plastic VFPGA<br>(4 × 4 mm, 0.4 mm pitch)   | A                                     | R5F10ELCABG#U0, R5F10ELDABG#U0,<br>R5F10ELEABG#U0, R5F10ELCABG#W0,<br>R5F10ELDABG#W0, R5F10ELEABG#W0                                    |
|           |  | G                                     | R5F10ELCGBG#U0, R5F10ELDGBG#U0,<br>R5F10ELEGBG#U0, R5F10ELCGBG#W0,<br>R5F10ELDGBG#W0, R5F10ELEGBG#W0                                    |

<R> **Note** For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1A**.

**Caution** The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)



|   | A                 | B               | C   | D   | E                                 |   |
|---|-------------------|-----------------|---|---|-----------------------------------|---|
| 5 | P40/TOOL0         | RESET           | P03/ANI16/<br>RxD1/TO00/<br>(KR1)         | P23/ANI3/<br>(KR3)                            | AV <sub>SS</sub>                  | 5 |
| 4 | P122/X2/<br>EXCLK | P137/INTP0      | P02/ANI17/<br>TxD1/TI00/<br>(KR0)         | P22/ANI2/<br>(KR2)                            | AV <sub>DD</sub>                  | 4 |
| 3 | P121/X1           | V <sub>DD</sub> | P21/ANI1/<br>AV <sub>REFM</sub>           | P11/ANI20/<br>SI00/SDA00/<br>RxD0/<br>TOOLRxD | P10/ANI18/<br>SCK00/SCL00         | 3 |
| 2 | REGC              | V <sub>SS</sub> | P30/ANI27/<br>SCK11/SCL11/<br>INTP3       | P51/ANI25/<br>SO11/INTP2                      | P50/ANI26/<br>SI11/SDA11<br>INTP1 | 2 |
| 1 | P60/SCLA0         | P61/SDAA0       | P31/ANI29/TI03/<br>TO03/PCLBUZ0<br>/INTP4 | P12/ANI21/<br>SO00/TxD0/<br>TOOLTxD           | P20/ANI0/<br>AV <sub>REFP</sub>   | 1 |
|   | A                 | B               | C   | D   | E                                 |   |

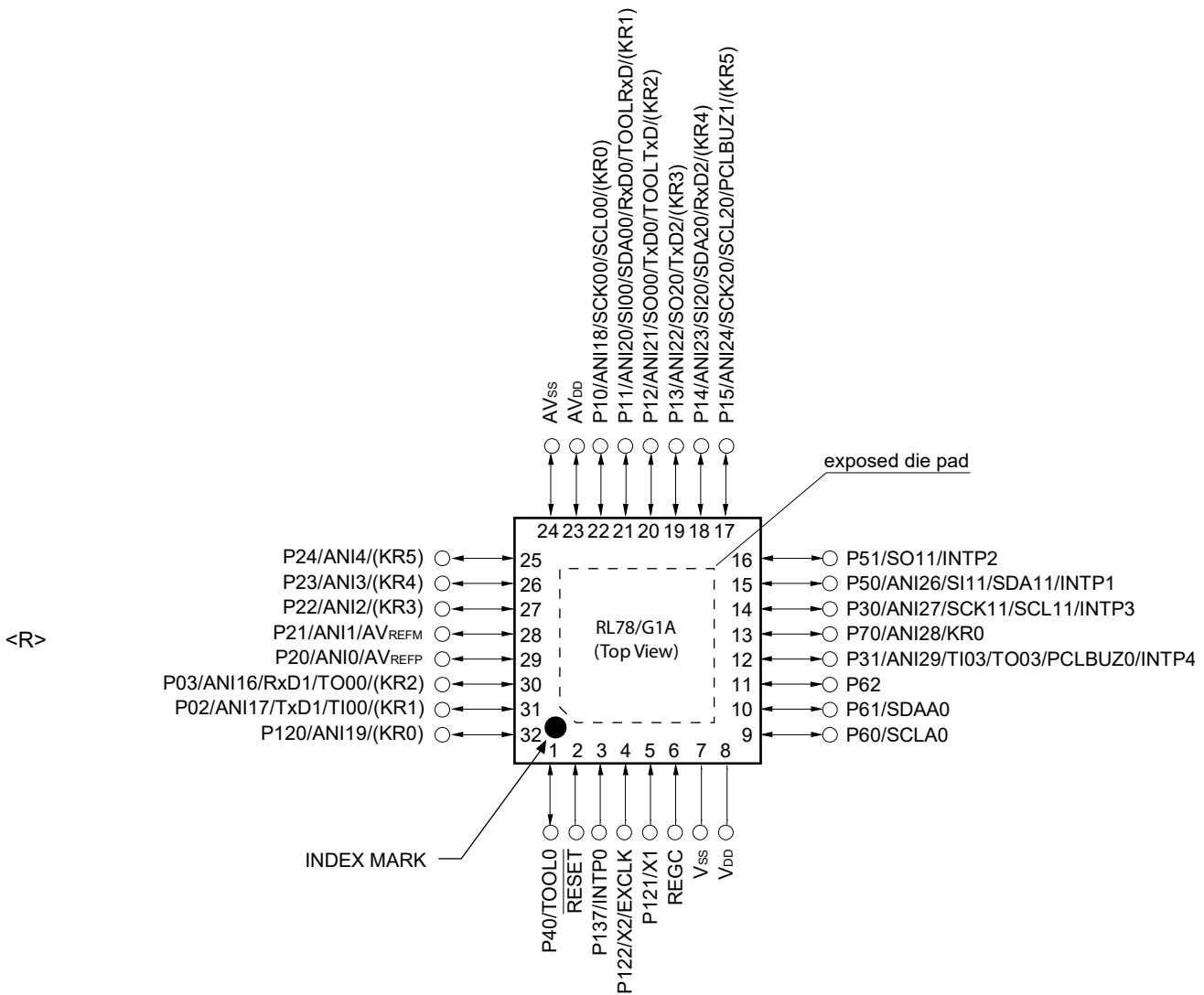
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

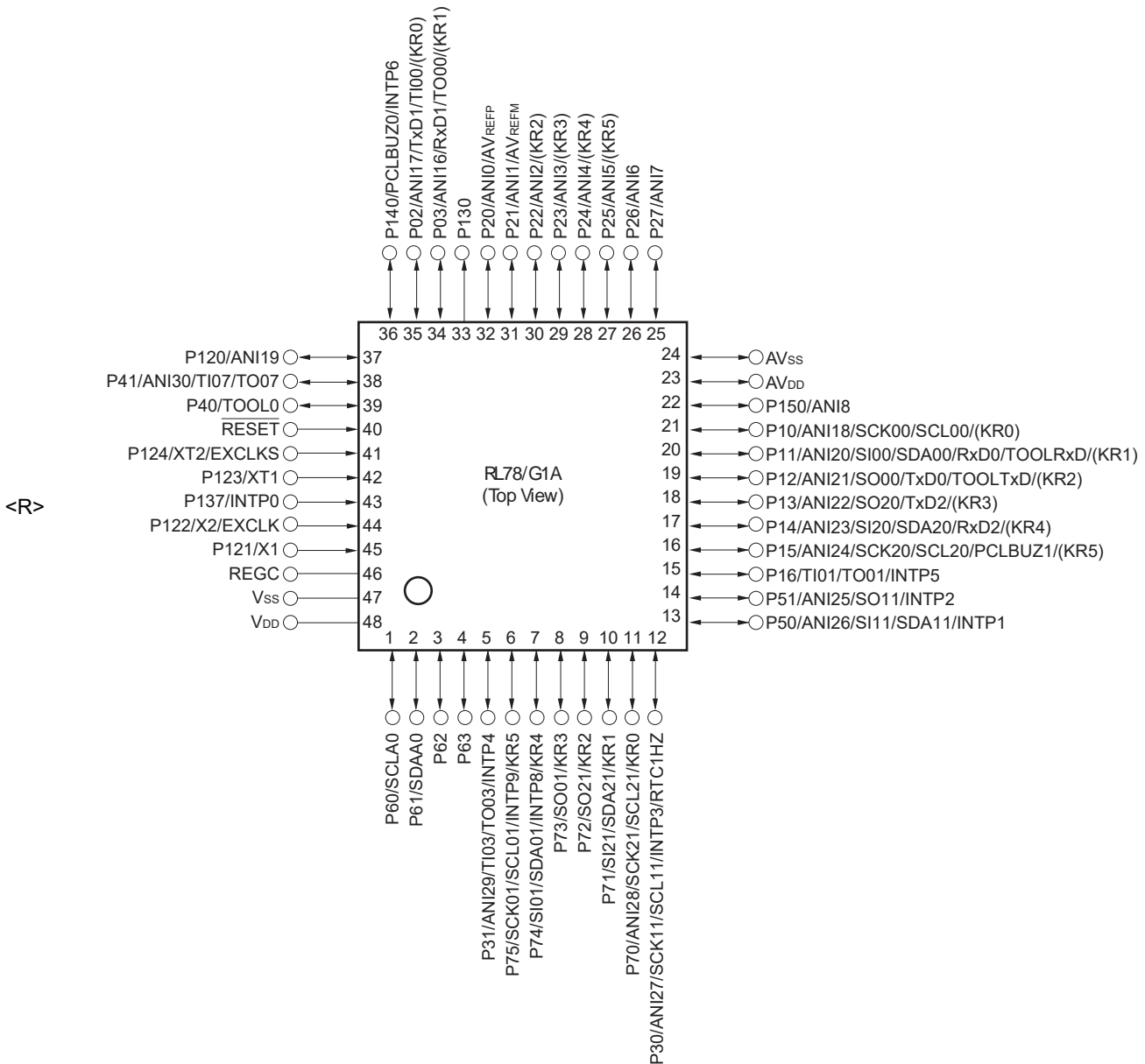
**Remarks 1.** For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

3. It is recommended to connect an exposed die pad to V<sub>SS</sub>.

1.3.3 48-pin products

- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

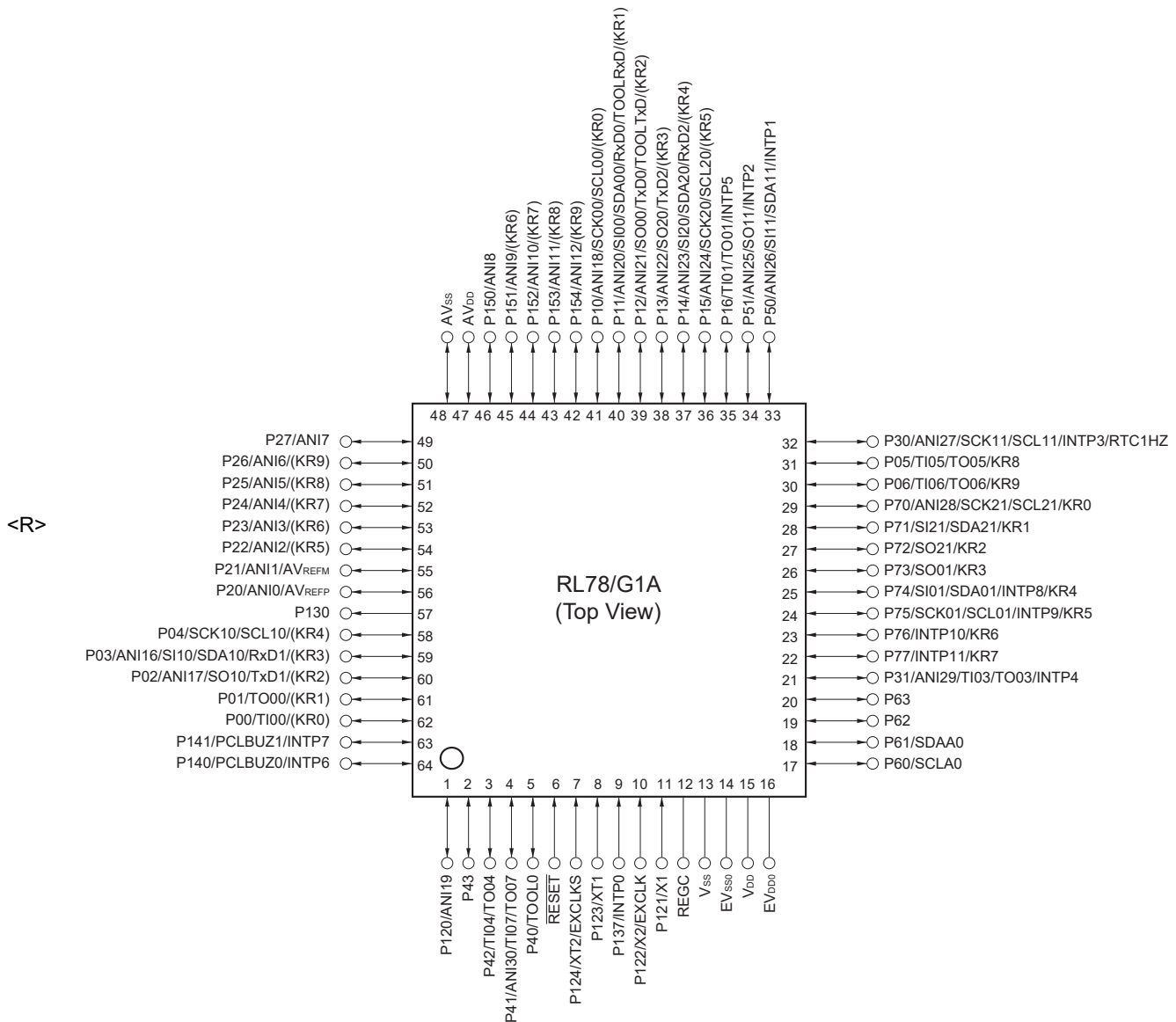
**Remarks 1.** For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).



1.3.4 64-pin products

- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



- Cautions 1.** Make EV<sub>SS0</sub> pin the same potential as V<sub>SS</sub> pin.
- Make V<sub>DD</sub> pin the potential that is higher than EV<sub>DD0</sub> pin.
  - Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD0</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS0</sub> pins to separate ground lines.
- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).



## 1.4 Pin Identification

|                  |  |                           |  |
|------------------|--|---------------------------|--|
| ANI0 to ANI12,   |  | PCLBUZ0, PCLBUZ1:         | Programmable clock output/buzzer output        |
| ANI16 to ANI30:  | Analog input                                     |                           |  |
| AVDD:            | Analog power supply                              | REGC:                     | Regulator capacitance                          |
| AVSS:            | Analog ground                                    | RESET:                    | Reset  |
| AVREFM:          | A/D converter reference potential (– side) input | RTC1HZ:                   | Real-time clock correction clock (1 Hz) output |
| AVREFP:          | A/D converter reference potential (+ side) input | RxD0 to RxD2:             | Receive data                                   |
| EVDD0:           | Power supply for port                            | SCK00, SCK01, SCK10,      |  |
| EVSS0:           | Ground for port                                  | SCK11, SCK20, SCK21:      | Serial clock input/output                      |
| EXCLK:           | External clock input (main system clock)         | SCLA0, SCL00, SCL01,      |  |
|                  |  | SCL10, SCL11, SCL20,      |  |
|                  |  | SCL21:                    | Serial clock output                            |
| EXCLKS:          | External clock input (subsystem clock)           | SDAA0, SDA00, SDA01,      |  |
|                  |  | SDA10, SDA11, SDA20,      |  |
| INTP0 to INTP11: | Interrupt Request from External                  | SDA21:                    | Serial data input/output                       |
|                  |  | SI00, SI01, SI10, SI11,   |  |
| KR0 to KR9:      | Key return                                       | SI20, SI21:               | Serial data input                              |
| P00 to P06:      | Port 0   | SO00, SO01, SO10,         |  |
| P10 to P16:      | Port 1   | SO11, SO20, SO21:         | Serial data output                             |
| P20 to P27:      | Port 2   | TI00, TI01, TI03 to TI07: | Timer input                                    |
| P30, P31:        | Port 3   | TO00, TO01,               |  |
| P40 to P43:      | Port 4   | TO03 to TO07:             | Timer output                                   |
| P50, P51:        | Port 5   | TOOL0:                    | Data input/output for tool                     |
| P60 to P63:      | Port 6   | TOOLRxD, TOOLTxD:         | Data input/output for external device          |
| P70 to P77:      | Port 7   | TxD0 to TxD2:             | Transmit data                                  |
| P120 to P124:    | Port 12  | VDD:                      | Power supply                                   |
| P130, P137:      | Port 13  | VSS:                      | Ground   |
| P140, P141:      | Port 14  | X1, X2:                   | Crystal oscillator (main system clock)         |
| P150 to P154:    | Port 15  | XT1, XT2:                 | Crystal oscillator (subsystem clock)           |

1.5 Block Diagram

1.5.1 25-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.2 32-pin products



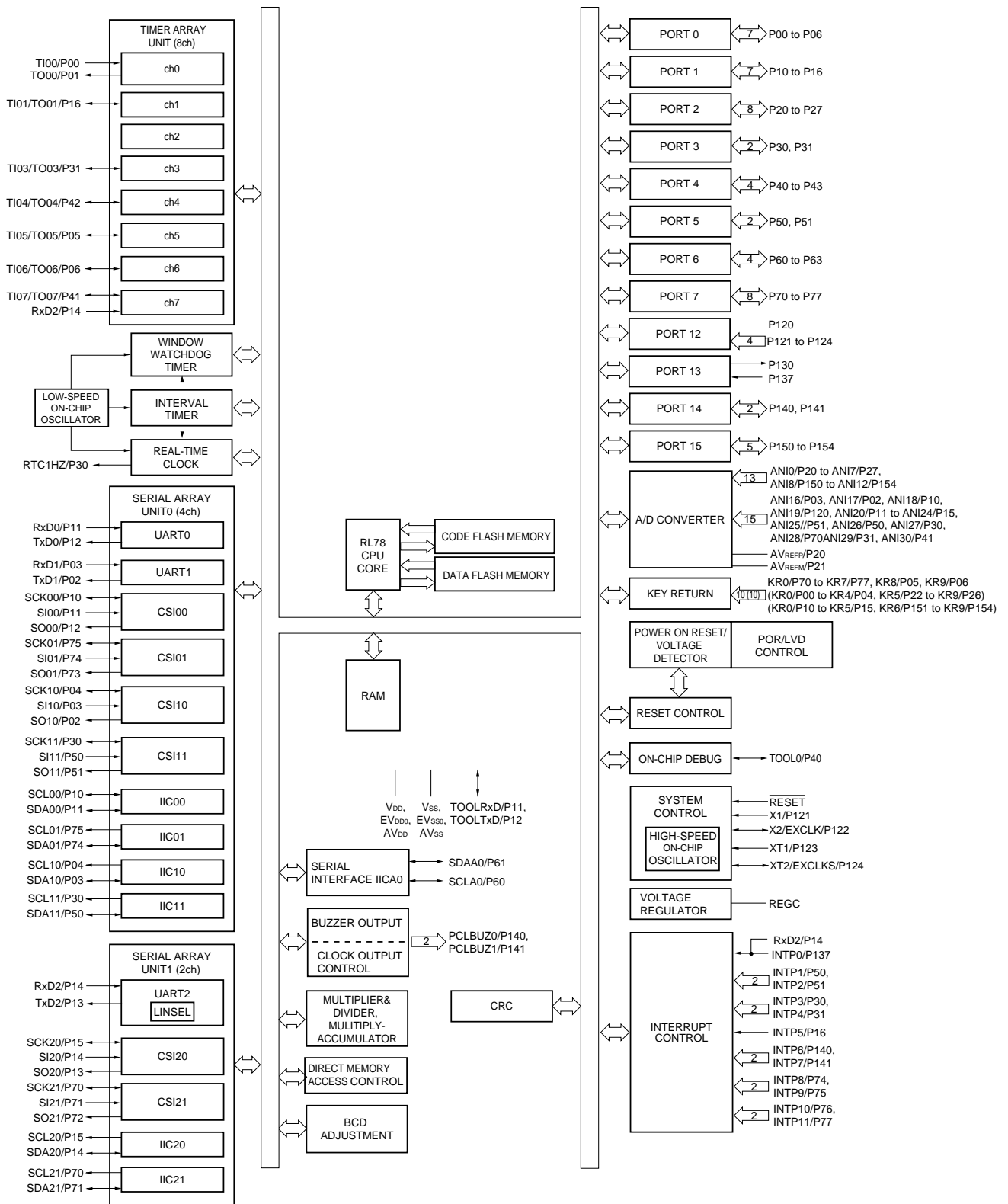
**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.3 48-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

(1/2)

| Item                               |                                     | 25-pin  | 32-pin   | 48-pin   | 64-pin   |    |
|------------------------------------|-------------------------------------|---|--|--|--|----|
|                                    |                                     | R5F10E8x  | R5F10EBx   | R5F10EGx   | R5F10ELx   |    |
| Code flash memory (KB)             |                                     | 16 to 64  | 16 to 64   | 16 to 64   | 32 to 64   |    |
| Data flash memory (KB)             |                                     | 4   | 4  | 4  | 4  |    |
| RAM (KB)                           |                                     | 2 to 4 <sup>Note 1</sup>  | 2 to 4 <sup>Note 1</sup>                                     | 2 to 4 <sup>Note 1</sup>   | 2 to 4 <sup>Note 1</sup>   |    |
| Address space                      |                                     | 1 MB  |  |  |  |    |
| <R>                                | Main system clock                   | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 3.6 V),<br>HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 3.6 V),<br>LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 3.6 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 3.6 V) |  |  |  |    |
|                                    | High-speed system clock             | HS (High-speed main) mode : 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 3.6 V),<br>HS (High-speed main) mode : 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 3.6 V),<br>LS (Low-speed main) mode : 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 3.6 V),<br>LV (Low-voltage main) mode : 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 3.6 V)   |  |  |  |    |
| Subsystem clock                    |                                     | -   |  | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.) |  |    |
| Low-speed on-chip oscillator       |                                     | 15 kHz (TYP.)   |  |  |  |    |
| General-purpose register           |                                     | (8-bit register × 8) × 4 bank   |  |  |  |    |
| Minimum instruction execution time |                                     | 0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)  |  |  |  |    |
|                                    |                                     | 0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)   |  |  |  |    |
|                                    |                                     | -   |  | 30.5 μs (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)                   |  |    |
| Instruction set                    |                                     | <ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits × 8 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li> </ul>   |  |  |  |    |
| <R>                                | I/O port                            | Total   | 19   | 26   | 42   | 56 |
|                                    | CMOS I/O                            | 14<br>(N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 6)  | 20<br>(N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 9) | 32<br>(N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 11)                        | 46<br>(N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 12)  |    |
|                                    | CMOS input                          | 3   | 3  | 5  | 5  |    |
|                                    | CMOS output                         | -   | -  | 1  | 1  |    |
|                                    | N-ch open-drain I/O (6 V tolerance) | 2   | 3  | 4  | 4  |    |
| Timer                              | 16-bit timer                        | 8 channels  |  |  |  |    |
|                                    | Watchdog timer                      | 1 channel   |  |  |  |    |
|                                    | Real-time clock (RTC)               | 1 channel <sup>Note 2</sup>   |  | 1 channel  |  |    |
|                                    | 12-bit interval timer (IT)          | 1 channel   |  |  |  |    |
|                                    | Timer output                        | 2 channels (PWM outputs: 1 <sup>Note 3</sup> )  |  | 4 channels (PWM outputs: 3 <sup>Note 3</sup> )                                       | 7 channels (PWM outputs: 6 <sup>Note 3</sup> )   |    |
|                                    | RTC output                          | -   |  | 1  | <ul style="list-style-type: none"> <li>• 1 Hz (subsystem clock: f<sub>SUB</sub> = 32.768 kHz)</li> </ul> |    |

**Notes 1.** In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T<sub>A</sub> = -40 to +105°C)**)

- <R>
2. Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f<sub>IL</sub>) is selected.
  3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (**6.9.3 Operation as multiple PWM output function**).



(2/2)

| Item  | 25-pin   | 32-pin                        | 48-pin  | 64-pin      |
|---|--|-------------------------------|---|-------------|
|   | R5F10E8x   | R5F10EBx                      | R5F10EGx  | R5F10ELx    |
| Clock output/buzzer output                  | 1  | 2                             | 2   | 2           |
|   | <ul style="list-style-type: none"> <li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br/>(Main system clock: <math>f_{MAIN} = 20</math> MHz operation)</li> </ul>   |                               | <ul style="list-style-type: none"> <li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br/>(Main system clock: <math>f_{MAIN} = 20</math> MHz operation)</li> <li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br/>(Subsystem clock: <math>f_{SUB} = 32.768</math> kHz operation)</li> </ul> |             |
| 8/12-bit resolution A/D converter           | 13 channels  | 18 channels                   | 24 channels   | 28 channels |
| Serial interface                            | <p>[25-pin products]</p> <ul style="list-style-type: none"> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li> </ul> <p>[32-pin products]</p> <ul style="list-style-type: none"> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART (UART supporting LIN-bus): 1 channel</li> </ul> <p>[48-pin products]</p> <ul style="list-style-type: none"> <li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li> <li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li> <li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li> </ul> <p>[64-pin products]</p> <ul style="list-style-type: none"> <li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li> <li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li> <li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li> </ul> |                               |   |             |
| I <sup>2</sup> C bus                        | 1 channel  | 1 channel                     | 1 channel   | 1 channel   |
| Multiplier and divider/multiply-accumulator | <ul style="list-style-type: none"> <li>16 bits × 16 bits = 32 bits (Unsigned or signed)</li> <li>32 bits ÷ 32 bits = 32 bits (Unsigned)</li> <li>16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)</li> </ul>   |                               |   |             |
| DMA controller                              | 2 channels   |                               |   |             |
| Vectored interrupt sources                  | Internal   | 24                            | 27  | 27          |
|   | External   | 6                             | 6   | 10          |
| Key interrupt                               | 0 ch (4 ch) <sup>Note 1</sup>  | 1 ch (6 ch) <sup>Note 1</sup> | 6 ch  | 10 ch       |
| Reset                                       | <ul style="list-style-type: none"> <li>Reset by RESET pin</li> <li>Internal reset by watchdog timer</li> <li>Internal reset by power-on-reset</li> <li>Internal reset by voltage detector</li> <li>Internal reset by illegal instruction execution<sup>Note 2</sup></li> <li>Internal reset by RAM parity error</li> <li>Internal reset by illegal-memory access</li> </ul>  |                               |   |             |
| Power-on-reset circuit                      | <ul style="list-style-type: none"> <li>Power-on-reset: 1.51 V (TYP.)</li> <li>Power-down-reset: 1.50 V (TYP.)</li> </ul>   |                               |   |             |
| Voltage detector                            | <ul style="list-style-type: none"> <li>Rising edge : 1.67 V to 3.14 V (12 stages)</li> <li>Falling edge : 1.63 V to 3.06 V (12 stages)</li> </ul>  |                               |   |             |
| On-chip debug function                      | Provided   |                               |   |             |
| Power supply voltage                        | $V_{DD} = 1.6$ to $3.6$ V  |                               |   |             |
| Operating ambient temperature               | $T_A = -40$ to $+85^\circ\text{C}$ (A: Consumer application), $T_A = -40$ to $+105^\circ\text{C}$ (G: Industrial application)  |                               |   |             |

**Notes** 1. Can be used by the Peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA  
 R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA  
 R5F10EGAAFb, R5F10EGCAFb, R5F10EGDAFb, R5F10EGEAFb  
 R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA  
 R5F10ELCAFb, R5F10ELDADFb, R5F10ELEAFb  
 R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

G: Industrial applications When  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA  
 R5F10EGAGFb, R5F10EGCGFb, R5F10EGDGFb, R5F10EGEGFb  
 R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA  
 R5F10ELCGFb, R5F10ELDGFb, R5F10ELEGFb

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $EV_{DD0}$  or  $EV_{SS0}$  pin, replace  $EV_{DD0}$  with  $V_{DD}$ , or replace  $EV_{SS0}$  with  $V_{SS}$ .

## 2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/2)

| Parameter              | Symbols            | Conditions   | Ratings   | Unit |
|------------------------|--------------------|--|---|------|
| Supply voltage         | V <sub>DD</sub>    |  | -0.5 to +6.5  | V    |
|                        | EV <sub>DD0</sub>  |  | -0.5 to +6.5  | V    |
|                        | AV <sub>DD</sub>   |  | -0.5 to +4.6  | V    |
|                        | AV <sub>REFP</sub> |  | -0.3 to AV <sub>DD</sub> + 0.3 <sup>Note 3</sup>  | V    |
|                        | EV <sub>SS0</sub>  |  | -0.5 to +0.3  | V    |
|                        | AV <sub>SS</sub>   |  | -0.5 to +0.3  | V    |
|                        | AV <sub>REFM</sub> |  | -0.3 to AV <sub>DD</sub> + 0.3 <sup>Note 3</sup><br>and AV <sub>REFM</sub> ≤ AV <sub>REFP</sub> | V    |
| REGC pin input voltage | V <sub>IREGC</sub> | REGC   | -0.3 to +2.8<br>and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>                             | V    |
| Input voltage          | V <sub>I1</sub>    | P00 to P06, P10 to P16, P30, P31, P40 to P43,<br>P50, P51, P70 to P77, P120, P140, P141                      | -0.3 to EV <sub>DD0</sub> + 0.3<br>and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>          | V    |
|                        | V <sub>I2</sub>    | P60 to P63 (N-ch open-drain)   | -0.3 to +6.5  | V    |
|                        | V <sub>I3</sub>    | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$   | -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>   | V    |
|                        | V <sub>I4</sub>    | P20 to P27, P150 to P154   | -0.3 to AV <sub>DD</sub> + 0.3 <sup>Note 2</sup>  | V    |
| Output voltage         | V <sub>O1</sub>    | P00 to P06, P10 to P16, P30, P31, P40 to P43,<br>P50, P51, P60 to P63, P70 to P77, P120, P130,<br>P140, P141 | -0.3 to EV <sub>DD0</sub> + 0.3 <sup>Note 2</sup>   | V    |
|                        | V <sub>O2</sub>    | P20 to P27, P150 to P154   | -0.3 to AV <sub>DD</sub> + 0.3 <sup>Note 2</sup>  | V    |
| Analog input voltage   | V <sub>AI1</sub>   | ANI16 to ANI30   | -0.3 to EV <sub>DD0</sub> + 0.3<br>and -0.3 to AV <sub>REF(+)</sub> + 0.3 <sup>Notes 2, 4</sup> | V    |
|                        | V <sub>AI2</sub>   | ANI0 to ANI12  | -0.3 to AV <sub>DD</sub> + 0.3<br>and -0.3 to AV <sub>REF(+)</sub> + 0.3 <sup>Notes 2, 4</sup>  | V    |

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Must be 4.6 V or lower.

**4.** Do not exceed AV<sub>REF(+)</sub> + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** AV<sub>REF(+)</sub>: + side reference voltage of the A/D converter.

**3.** V<sub>SS</sub>: Reference voltage

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ ) (2/2)**

| Parameter                     | Symbols                          | Conditions                   |  | Ratings  | Unit             |
|-------------------------------|----------------------------------|------------------------------|--|--|------------------|
| Output current, high          | $I_{OH1}$                        | Per pin                      | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | -40  | mA               |
|                               |                                  | Total of all pins<br>-170 mA | P00 to P04, P40 to P43, P120, P130, P140, P141   | -70  | mA               |
|                               |                                  |                              | P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,                                      | -100   | mA               |
|                               | $I_{OH2}$                        | Per pin                      | P20 to P27, P150 to P154   | -0.1   | mA               |
|                               |                                  | Total of all pins            |  | -1.3   | mA               |
|                               | Output current, low              | $I_{OL1}$                    | Per pin  | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141 | 40               |
| Total of all pins<br>170 mA   |                                  |                              | P00 to P04, P40 to P43, P120, P130, P140, P141   | 70   | mA               |
|                               |                                  |                              | P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77                           | 100  | mA               |
| $I_{OL2}$                     |                                  | Per pin                      | P20 to P27, P150 to P154   | 0.4  | mA               |
|                               |                                  | Total of all pins            |  | 6.4  | mA               |
| Operating ambient temperature |                                  | $T_A$                        | In normal operation mode   |  | -40 to +85       |
|                               | In flash memory programming mode |                              |  |  |                  |
| Storage temperature           | $T_{stg}$                        |                              |  | -65 to +150  | $^\circ\text{C}$ |

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V)

| Parameter   | Resonator                           | Conditions                      | MIN. | TYP.   | MAX. | Unit |
|---|-------------------------------------|---------------------------------|------|--------|------|------|
| X1 clock oscillation frequency (f <sub>x</sub> ) <sup>Note</sup>  | Ceramic resonator/crystal resonator | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V | 1.0  |        | 20.0 | MHz  |
|   |                                     | 2.4 V ≤ V <sub>DD</sub> < 2.7 V | 1.0  |        | 16.0 | MHz  |
|   |                                     | 1.8 V ≤ V <sub>DD</sub> < 2.4 V | 1.0  |        | 8.0  | MHz  |
|   |                                     | 1.6 V ≤ V <sub>DD</sub> < 1.8 V | 1.0  |        | 4.0  | MHz  |
| XT1 clock oscillation frequency (f <sub>x</sub> ) <sup>Note</sup> | Crystal resonator                   |                                 | 32   | 32.768 | 35   | kHz  |

**Note** Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

### 2.2.2 On-chip oscillator characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V)

| Oscillators   | Parameters     | Conditions    | MIN.                            | TYP. | MAX. | Unit |   |
|---|----------------|---------------|---------------------------------|------|------|------|---|
| High-speed on-chip oscillator clock frequency <sup>Notes 1, 2</sup> | f <sub>H</sub> |               | 1                               |      | 32   | MHz  |   |
| High-speed on-chip oscillator clock frequency accuracy              |                | -20 to +85 °C | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V | -1.0 |      | +1.0 | % |
|   |                |               | 1.6 V ≤ V <sub>DD</sub> < 1.8 V | -5.0 |      | +5.0 | % |
|   |                | -40 to -20 °C | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V | -1.5 |      | +1.5 | % |
|   |                |               | 1.6 V ≤ V <sub>DD</sub> < 1.8 V | -5.5 |      | +5.5 | % |
| Low-speed on-chip oscillator clock frequency                        | f <sub>L</sub> |               |                                 | 15   |      | kHz  |   |
| Low-speed on-chip oscillator clock frequency accuracy               |                |               | -15                             |      | +15  | %    |   |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (1/5)

| Items                                  | Symbol  | Conditions   | MIN.                              | TYP. | MAX.  | Unit                    |    |
|--|---|--|-----------------------------------|------|-------|-------------------------|----|
| Output current, high <sup>Note 1</sup> | I <sub>OH1</sub>  | Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |      |       | -10.0 <sup>Note 2</sup> | mA |
|  |   | Total of P00 to P04, P40 to P43, P120, P130, P140, P141<br>(When duty ≤ 70% <sup>Note 3</sup> )        | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |      |       | -10.0                   | mA |
|  |   |  | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V |      |       | -5.0                    | mA |
|  |   |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V |      |       | -2.5                    | mA |
|  |   | Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,<br>(When duty ≤ 70% <sup>Note 3</sup> ) | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |      |       | -19.0                   | mA |
|  |   |  | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V |      |       | -10.0                   | mA |
|  |   |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V |      |       | -5.0                    | mA |
|  | Total of all pins<br>(When duty ≤ 70% <sup>Note 3</sup> ) | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V  |                                   |      | -29.0 | mA                      |    |
|  | I <sub>OH2</sub>  | Per pin for P20 to P27, P150 to P154   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V  |      |       | -0.1 <sup>Note 2</sup>  | mA |
|  |   | Total of all pins<br>(When duty ≤ 70% <sup>Note 3</sup> )  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V  |      |       | -1.3                    | mA |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, V<sub>DD</sub> pins to an output pin.
  - However, do not exceed the total current value.
  - Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)  
 <Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA  
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≅ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/5)

| Items   | Symbol  | Conditions  | MIN.                              | TYP. | MAX.                   | Unit                  |    |
|---|---|---|-----------------------------------|------|------------------------|-----------------------|----|
| Output current,<br>I <sub>OL</sub> <sup>Note 1</sup>      | I <sub>OL1</sub>  | Per pin for P00 to P06, P10 to P16,<br>P30, P31, P40 to P43, P50, P51,<br>P70 to P77, P120, P130, P140, P141            |                                   |      | 20.0 <sup>Note 2</sup> | mA                    |    |
|   |   | Per pin for P60 to P63  |                                   |      | 15.0 <sup>Note 2</sup> | mA                    |    |
|   |   | Total of P00 to P04, P40 to P43, P120,<br>P130, P140, P141<br>(When duty ≤ 70% <sup>Note 3</sup> )                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |      |                        | 15.0                  | mA |
|   |   |   | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V |      |                        | 9.0                   | mA |
|   |   |   | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V |      |                        | 4.5                   | mA |
|   |   | Total of P05, P06, P10 to P16, P30,<br>P31, P50, P51, P60 to P63,<br>P70 to P77<br>(When duty ≤ 70% <sup>Note 3</sup> ) | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |      |                        | 35.0                  | mA |
|   |   |   | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V |      |                        | 20.0                  | mA |
|   | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                         |   |                                   |      | 10.0                   | mA                    |    |
|   | Total of all pins<br>(When duty ≤ 70% <sup>Note 3</sup> ) |   |                                   |      | 50.0                   | mA                    |    |
|   | I <sub>OL2</sub>  | Per pin for P20 to P27, P150 to P154  |                                   |      |                        | 0.4 <sup>Note 2</sup> | mA |
| Total of all pins<br>(When duty ≤ 70% <sup>Note 3</sup> ) |   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V  |                                   |      | 5.2                    | mA                    |    |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV<sub>SS0</sub> and V<sub>SS</sub> pin.
  - However, do not exceed the total current value.
  - Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OL</sub> × 0.7)/(n × 0.01)
- <Example> Where n = 80% and I<sub>OL</sub> = 10.0 mA
- $$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (3/5)

| Items               | Symbol           | Conditions   | MIN.  | TYP.                 | MAX. | Unit                 |   |
|---------------------|------------------|--|---|----------------------|------|----------------------|---|
| Input voltage, high | V <sub>IH1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | Normal input buffer                                   | 0.8EV <sub>DD0</sub> |      | EV <sub>DD0</sub>    | V |
|                     | V <sub>IH2</sub> | P01, P03, P04, P10, P11, P13 to P16, P43   | TTL input buffer<br>3.3 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 2.0                  |      | EV <sub>DD0</sub>    | V |
|                     |                  |  | TTL input buffer<br>1.6 V ≤ EV <sub>DD0</sub> < 3.3 V | 1.5                  |      | EV <sub>DD0</sub>    | V |
|                     | V <sub>IH3</sub> | P20 to P27, P150 to P154   |   | 0.7AV <sub>DD</sub>  |      | AV <sub>DD</sub>     | V |
|                     | V <sub>IH4</sub> | P60 to P63   |   | 0.7EV <sub>DD0</sub> |      | 6.0                  | V |
|                     | V <sub>IH5</sub> | P121 to P124, P137, EXCLK, EXCLKS, RESET   |   | 0.8V <sub>DD</sub>   |      | V <sub>DD</sub>      | V |
| Input voltage, low  | V <sub>IL1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | Normal input buffer                                   | 0                    |      | 0.2EV <sub>DD0</sub> | V |
|                     | V <sub>IL2</sub> | P01, P03, P04, P10, P11, P13 to P16, P43   | TTL input buffer<br>3.3 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                    |      | 0.5                  | V |
|                     |                  |  | TTL input buffer<br>1.6 V ≤ EV <sub>DD0</sub> < 3.3 V | 0                    |      | 0.32                 | V |
|                     | V <sub>IL3</sub> | P20 to P27, P150 to P154   |   | 0                    |      | 0.3AV <sub>DD</sub>  | V |
|                     | V <sub>IL4</sub> | P60 to P63   |   | 0                    |      | 0.3EV <sub>DD0</sub> | V |
|                     | V <sub>IL5</sub> | P121 to P124, P137, EXCLK, EXCLKS, RESET   |   | 0                    |      | 0.2V <sub>DD</sub>   | V |

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV<sub>DD0</sub>, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (4/5)

| Items  | Symbol           | Conditions   | MIN.  | TYP.                    | MAX. | Unit |
|--|------------------|--|---|-------------------------|------|------|
| Output voltage, high   | V <sub>OH1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OH1</sub> = -2.0 mA | EV <sub>DD0</sub> - 0.6 |      | V    |
|  |                  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OH1</sub> = -1.5 mA | EV <sub>DD0</sub> - 0.5 |      | V    |
|  |                  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OH1</sub> = -1.0 mA | EV <sub>DD0</sub> - 0.5 |      | V    |
|  | V <sub>OH2</sub> | P20 to P27, P150 to P154   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V, I <sub>OH2</sub> = -100 μA  | AV <sub>DD</sub> - 0.5  |      | V    |
| Output voltage, low  | V <sub>OL1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OL1</sub> = 3.0 mA  |                         | 0.6  | V    |
|  |                  |  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OL1</sub> = 1.5 mA  |                         | 0.4  | V    |
|  |                  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OL1</sub> = 0.6 mA  |                         | 0.4  | V    |
|  |                  |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V, I <sub>OL1</sub> = 0.3 mA  |                         | 0.4  | V    |
|  | V <sub>OL2</sub> | P20 to P27, P150 to P154   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V, I <sub>OL2</sub> = 400 μA   |                         | 0.4  | V    |
|  | V <sub>OL3</sub> | P60 to P63   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OL3</sub> = 3.0 mA  |                         | 0.4  | V    |
|  |                  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, I <sub>OL3</sub> = 2.0 mA  |                         | 0.4  | V    |
| 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V, I <sub>OL3</sub> = 1.0 mA |                  |  |   | 0.4                     | V    |      |

**Caution** P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (5/5)

| Items                       | Symbol                   | Conditions   | MIN.   | TYP.                                  | MAX. | Unit |     |    |
|-----------------------------|--------------------------|--|--|---------------------------------------|------|------|-----|----|
| Input leakage current, high | I <sub>LIH1</sub>        | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141 | V <sub>I</sub> = EV <sub>DD0</sub>                 |                                       | 1    | μA   |     |    |
|                             | I <sub>LIH2</sub>        | P137, $\overline{\text{RESET}}$  | V <sub>I</sub> = V <sub>DD</sub>                   |                                       | 1    | μA   |     |    |
|                             | I <sub>LIH3</sub>        | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   | V <sub>I</sub> = V <sub>DD</sub>                   | In input port or external clock input | 1    | μA   |     |    |
|                             |                          |  |  | In resonator connection               | 10   | μA   |     |    |
| I <sub>LIH4</sub>           | P20 to P27, P150 to P154 | V <sub>I</sub> = AV <sub>DD</sub>  |  | 1                                     | μA   |      |     |    |
| Input leakage current, low  | I <sub>LIL1</sub>        | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141 | V <sub>I</sub> = EV <sub>SS0</sub>                 |                                       | -1   | μA   |     |    |
|                             | I <sub>LIL2</sub>        | P137, $\overline{\text{RESET}}$  | V <sub>I</sub> = V <sub>SS</sub>                   |                                       | -1   | μA   |     |    |
|                             | I <sub>LIL3</sub>        | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   | V <sub>I</sub> = V <sub>SS</sub>                   | In input port or external clock input | -1   | μA   |     |    |
|                             |                          |  |  | In resonator connection               | -10  | μA   |     |    |
| I <sub>LIL4</sub>           | P20 to P27, P150 to P154 | V <sub>I</sub> = AV <sub>SS</sub>  |  | -1                                    | μA   |      |     |    |
| On-chip pull-up resistance  | R <sub>U</sub>           | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141             | V <sub>I</sub> = EV <sub>SS0</sub> , In input port |                                       | 10   | 20   | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = E<sub>VSS0</sub> = 0 V)

(1/3)

| Parameter                        | Symbol            | Conditions             |  |   | MIN.                    | TYP.                                       | MAX.                    | Unit                 |     |     |     |
|----------------------------------|-------------------|------------------------|--|---|-------------------------|--|-------------------------|----------------------|-----|-----|-----|
| Supply current <sup>Note 1</sup> | I <sub>DD1</sub>  | Operating mode         | HS (high-speed main) mode <sup>Note 5</sup>  | f <sub>IH</sub> = 32 MHz <sup>Note 3</sup>                              | Basic operation         | V <sub>DD</sub> = 3.0 V                    |                         | 2.1                  |     | mA  |     |
|                                  |                   |                        |  |   | Normal operation        | V <sub>DD</sub> = 3.0 V                    |                         | 4.6                  | 7.0 | mA  |     |
|                                  |                   |                        |  | Normal operation  | V <sub>DD</sub> = 3.0 V | f <sub>IH</sub> = 24 MHz <sup>Note 3</sup> |                         | 3.7                  | 5.5 | mA  |     |
|                                  |                   |                        |  |   |                         | f <sub>IH</sub> = 16 MHz <sup>Note 3</sup> |                         | 2.7                  | 4.0 | mA  |     |
|                                  |                   |                        | LS (low-speed main) mode <sup>Note 5</sup>   | f <sub>IH</sub> = 8 MHz <sup>Note 3</sup>                               | Normal operation        | V <sub>DD</sub> = 3.0 V                    |                         | 1.2                  | 1.8 | mA  |     |
|                                  |                   |                        |  |   |                         |  | V <sub>DD</sub> = 2.0 V |                      | 1.2 |     | 1.8 |
|                                  |                   |                        | LV (Low-voltage main) mode <sup>Note 5</sup> | f <sub>IH</sub> = 4 MHz <sup>Note 3</sup>                               | Normal operation        | V <sub>DD</sub> = 3.0 V                    |                         | 1.2                  | 1.7 | mA  |     |
|                                  |                   |                        |  |   |                         | V <sub>DD</sub> = 2.0 V                    |                         | 1.2                  | 1.7 |     |     |
|                                  |                   |                        | HS (high-speed main) mode <sup>Note 5</sup>  | f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> ,<br>V <sub>DD</sub> = 3.0 V | Normal operation        | Square wave input                          |                         | 3.0                  | 4.6 | mA  |     |
|                                  |                   |                        |  |   |                         | Resonator connection                       |                         | 3.2                  | 4.8 |     |     |
|                                  |                   |                        |  |   | Normal operation        | Square wave input                          | V <sub>DD</sub> = 3.0 V |                      | 1.9 | 2.7 | mA  |
|                                  |                   |                        |  |   |                         |  | V <sub>DD</sub> = 2.0 V |                      | 1.9 | 2.7 |     |
|                                  |                   |                        | LS (low-speed main) mode <sup>Note 5</sup>   | f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> ,<br>V <sub>DD</sub> = 3.0 V  | Normal operation        | Square wave input                          |                         | 1.1                  | 1.7 | mA  |     |
|                                  |                   |                        |  |   |                         | Resonator connection                       |                         | 1.1                  | 1.7 |     |     |
|                                  |                   |                        |  | Normal operation  | Square wave input       | V <sub>DD</sub> = 3.0 V                    |                         | 1.1                  | 1.7 | mA  |     |
|                                  |                   |                        |  |   |                         | V <sub>DD</sub> = 2.0 V                    |                         | 1.1                  | 1.7 |     |     |
|                                  |                   |                        | Subsystem clock mode                         | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>                         | Normal operation        | Square wave input                          | T <sub>A</sub> = -40°C  |                      | 4.1 | 4.9 | μA  |
|                                  |                   |                        |  |   |                         |  | Resonator connection    |                      | 4.2 | 5.0 |     |
|                                  |                   |                        |  |   | Normal operation        | Square wave input                          | T <sub>A</sub> = +25°C  |                      | 4.2 | 4.9 | μA  |
|                                  |                   |                        |  |   |                         |  |                         | Resonator connection |     | 4.3 |     |
| Normal operation                 | Square wave input | T <sub>A</sub> = +50°C |  |   |                         | 4.3  | 5.5                     | μA                   |     |     |     |
|                                  |                   |                        |  |   | Resonator connection    |  | 4.4                     |                      | 5.6 |     |     |
| Normal operation                 | Square wave input | T <sub>A</sub> = +70°C |  |   |                         | 4.5  | 6.3                     | μA                   |     |     |     |
|                                  |                   |                        |  |   | Resonator connection    |  | 4.6                     |                      | 6.4 |     |     |
| Normal operation                 | Square wave input | T <sub>A</sub> = +85°C |  |   |                         | 4.8  | 7.7                     | μA                   |     |     |     |
|                                  |                   |                        |  |   | Resonator connection    |  | 4.9                     |                      | 7.8 |     |     |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode: V<sub>DD</sub> = 2.7 V to 3.6 V@1 MHz to 32 MHz  
V<sub>DD</sub> = 2.4 V to 3.6 V@1 MHz to 16 MHz
    - LS (low-speed main) mode: V<sub>DD</sub> = 1.8 V to 3.6 V@1 MHz to 8 MHz
    - LV (Low-voltage main) mode: V<sub>DD</sub> = 1.6 V to 3.6 V@1 MHz to 4 MHz

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/3)

| Parameter                        | Symbol                             | Conditions |   |   | MIN.  | TYP.                    | MAX. | Unit |      |      |    |
|----------------------------------|------------------------------------|------------|---|---|---|-------------------------|------|------|------|------|----|
| Supply current <sup>Note 1</sup> | I <sub>DD2</sub> <sup>Note 2</sup> | HALT mode  | HS (high-speed main) mode <sup>Note 7</sup>                               | f <sub>IH</sub> = 32 MHz <sup>Note 4</sup>                                | V <sub>DD</sub> = 3.0 V   |                         | 0.54 | 1.63 | mA   |      |    |
|                                  |                                    |            |   | f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>                                | V <sub>DD</sub> = 3.0 V   |                         | 0.44 | 1.28 | mA   |      |    |
|                                  |                                    |            |   | f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>                                | V <sub>DD</sub> = 3.0 V   |                         | 0.40 | 1.00 | mA   |      |    |
|                                  |                                    |            |   | LS (low-speed main) mode <sup>Note 7</sup>                                | f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>                               | V <sub>DD</sub> = 3.0 V |      | 270  | 530  | μA   |    |
|                                  |                                    |            |   |   |   | V <sub>DD</sub> = 2.0 V |      | 270  | 530  |      |    |
|                                  |                                    |            |   | LV (Low-voltage main) mode <sup>Note 7</sup>                              | f <sub>IH</sub> = 4 MHz <sup>Note 4</sup>                               | V <sub>DD</sub> = 3.0 V |      | 435  | 640  | μA   |    |
|                                  |                                    |            |   |   |   | V <sub>DD</sub> = 2.0 V |      | 435  | 640  |      |    |
|                                  |                                    |            |   | HS (high-speed main) mode <sup>Note 7</sup>                               | f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V | Square wave input       |      | 0.28 | 1.00 | mA   |    |
|                                  |                                    |            |   |   |   | Resonator connection    |      | 0.45 | 1.17 |      |    |
|                                  |                                    |            | f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V   |   | Square wave input   |                         | 0.19 | 0.60 | mA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 0.26 | 0.67 |      |      |    |
|                                  |                                    |            | LS (low-speed main) mode <sup>Note 7</sup>                                |   | f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V  | Square wave input       |      | 95   | 330  | μA   |    |
|                                  |                                    |            |   |   |   | Resonator connection    |      | 145  | 380  |      |    |
|                                  |                                    |            |   | f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 2.0 V    | Square wave input   |                         | 95   | 330  | μA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 145  | 380  |      |      |    |
|                                  |                                    |            | Subsystem clock mode  | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = -40°C | Square wave input   |                         | 0.25 | 0.57 | μA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 0.44 | 0.76 |      |      |    |
|                                  |                                    |            |   | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +25°C | Square wave input   |                         | 0.30 | 0.57 | μA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 0.49 | 0.76 |      |      |    |
|                                  |                                    |            |   | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +50°C | Square wave input   |                         | 0.38 | 1.17 | μA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 0.57 | 1.36 |      |      |    |
|                                  |                                    |            |   | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +70°C | Square wave input   |                         | 0.52 | 1.97 | μA   |      |    |
|                                  |                                    |            |   |   | Resonator connection  |                         | 0.71 | 2.16 |      |      |    |
|                                  |                                    |            | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +85°C | Square wave input   |   | 0.97                    | 3.37 | μA   |      |      |    |
|                                  |                                    |            |   | Resonator connection  |   | 1.16                    | 3.56 |      |      |      |    |
|                                  |                                    |            | I <sub>DD3</sub> <sup>Note 6</sup>  | STOP mode <sup>Note 8</sup>   | T <sub>A</sub> = -40°C  |                         |      |      | 0.16 | 0.50 | μA |
|                                  |                                    |            |   |   | T <sub>A</sub> = +25°C  |                         |      |      | 0.23 | 0.50 |    |
|                                  |                                    |            |   |   | T <sub>A</sub> = +50°C  |                         |      |      | 0.34 | 1.10 |    |
| T <sub>A</sub> = +70°C           |                                    |            |   |   |   | 0.46                    | 1.90 |      |      |      |    |
| T <sub>A</sub> = +85°C           |                                    |            |   |   |   | 0.75                    | 3.30 |      |      |      |    |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). Including the current flowing into the RTC. However, not including the current flowing into the 12-bit interval timer, and watchdog timer.
  6. When subsystem clock is stopped. Not including the current flowing into the RTC, 12-bit interval timer, watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }16\text{ MHz}$
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} < 3.6\text{ V}@1\text{ MHz to }8\text{ MHz}$
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }4\text{ MHz}$
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

<R> (T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (3/3)

| Parameter                                      | Symbol                                    | Conditions  |  | MIN. | TYP. | MAX. | Unit |
|--|---|---|--|------|------|------|------|
| Low-speed on-chip oscillator operating current | I <sub>FIL</sub> <sup>Note 1</sup>        |   |  |      | 0.20 |      | μA   |
| RTC operating current                          | I <sub>RTC</sub> <sup>Notes 1, 2, 3</sup> |   |  |      | 0.02 |      | μA   |
| 12-bit interval timer operating current        | I <sub>IT</sub> <sup>Notes 1, 2, 4</sup>  |   |  |      | 0.02 |      | μA   |
| Watchdog timer operating current               | I <sub>WDT</sub> <sup>Notes 1, 2, 5</sup> | f <sub>IL</sub> = 15 kHz  |  |      | 0.22 |      | μA   |
| A/D converter operating current                | I <sub>ADC</sub> <sup>Notes 6, 7</sup>    | AV <sub>DD</sub> = 3.0 V, When conversion at maximum speed              |  |      | 420  | 720  | μA   |
| AV <sub>REF(+)</sub> current                   | I <sub>AVREF</sub> <sup>Note 8</sup>      | AV <sub>DD</sub> = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 <sup>Note 7</sup>    |  |      | 14.0 | 25.0 | μA   |
|  |   | AV <sub>REFP</sub> = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 <sup>Note 10</sup> |  |      | 14.0 | 25.0 | μA   |
|  |   | ADREFP1 = 1, ADREFP0 = 0 <sup>Note 1</sup>                              |  |      | 14.0 | 25.0 | μA   |
| A/D converter reference voltage current        | I <sub>ADREF</sub> <sup>Notes 1, 9</sup>  | V <sub>DD</sub> = 3.0 V   |  |      | 75.0 |      | μA   |
| Temperature sensor operating current           | I <sub>TMP</sub> <sup>Note 1</sup>        | V <sub>DD</sub> = 3.0 V   |  |      | 75.0 |      | μA   |
| LVD operating current                          | I <sub>LVD</sub> <sup>Notes 1, 11</sup>   |   |  |      | 0.08 |      | μA   |
| BGO operating current                          | I <sub>BGO</sub> <sup>Notes 1, 12</sup>   |   |  |      | 2.5  | 12.2 | mA   |
| Self-programming operating current             | I <sub>FSP</sub> <sup>Notes 1, 13</sup>   |   |  |      | 2.5  | 12.2 | mA   |
| SNOOZE operating current                       | I <sub>SNOZ</sub>                         | A/D converter operation (AV <sub>DD</sub> = 3.0 V)                      | The mode is performed <sup>Notes 1, 14</sup> |      | 0.50 | 0.60 | mA   |
|  |   |   | During A/D conversion <sup>Note 1</sup>      |      | 0.60 | 0.75 | mA   |
|  |   |   | During A/D conversion <sup>Note 7</sup>      |      | 420  | 720  | μA   |
|  |   | CSI/UART operation <sup>Note 1</sup>                                    |  | 0.70 | 0.84 | mA   |      |

(Notes and Remarks are listed on the next page.)

- <R> **Notes**
1. Current flowing to V<sub>DD</sub>.
  2. When high-speed on-chip oscillator and high-speed system clock are stopped.
  3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I<sub>DD1</sub> or I<sub>DD2</sub>, and I<sub>RTC</sub>, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I<sub>FIL</sub> should be added. I<sub>DD2</sub> subsystem clock operation includes the operational current of the real-time clock.
  4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I<sub>DD1</sub> or I<sub>DD2</sub>, and I<sub>IT</sub>, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I<sub>FIL</sub> should be added.
  5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub>, or I<sub>DD3</sub> and I<sub>WDT</sub> when the watchdog timer is in operation.
  6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub> or I<sub>DD2</sub> and I<sub>ADC</sub>, I<sub>AVREF</sub>, I<sub>ADREF</sub> when the A/D converter operates in an operation mode or the HALT mode.
  7. Current flowing to the AV<sub>DD</sub>.
  8. Current flowing from the reference voltage source of A/D converter.
  9. Operation current flowing to the internal reference voltage.
  10. Current flowing to the AV<sub>REFP</sub>.
  11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>LVD</sub> when the LVD circuit is in operation.
  12. Current flowing only during data flash rewrite.
  13. Current flowing only during self programming.

- Remarks**
1. f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
  2. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  3. f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
  4. Temperature condition of the TYP. value is T<sub>A</sub> = 25°C



## 2.4 AC Characteristics

(T<sub>A</sub> = -40 to +85°C, AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Items  | Symbol                                | Conditions                                       |   | MIN.                            | TYP.    | MAX. | Unit               |    |
|--|---------------------------------------|--|---|---------------------------------|---------|------|--------------------|----|
| Instruction cycle (minimum instruction execution time)           | T <sub>cy</sub>                       | Main system clock (f <sub>MAIN</sub> ) operation | HS (high-speed main) mode   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.03125 | 1    | μs                 |    |
|  |                                       |  |   | 2.4 V ≤ V <sub>DD</sub> < 2.7 V | 0.0625  | 1    | μs                 |    |
|  |                                       |  | LS (low-speed main) mode  | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.125   | 1    | μs                 |    |
|  |                                       |  |   | 1.6 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.25    | 1    | μs                 |    |
|  |                                       | Subsystem clock (f <sub>SUB</sub> ) operation    |   | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V | 28.5    | 30.5 | 31.3               | μs |
|  |                                       | In the self programming mode                     | HS (high-speed main) mode   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.03125 | 1    | μs                 |    |
|  |                                       |  |   | 2.4 V ≤ V <sub>DD</sub> < 2.7 V | 0.0625  | 1    | μs                 |    |
|  |                                       |  | LS (low-speed main) mode  | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.125   | 1    | μs                 |    |
| 1.6 V ≤ V <sub>DD</sub> ≤ 3.6 V                                  | 0.25                                  |  |   | 1                               | μs      |      |                    |    |
| External system clock frequency                                  | f <sub>EX</sub>                       | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V                  |   | 1.0                             |         | 20.0 | MHz                |    |
|  |                                       | 2.4 V ≤ V <sub>DD</sub> < 2.7 V                  |   | 1.0                             |         | 16.0 | MHz                |    |
|  |                                       | 1.8 V ≤ V <sub>DD</sub> < 2.4 V                  |   | 1.0                             |         | 8.0  | MHz                |    |
|  |                                       | 1.6 V ≤ V <sub>DD</sub> < 1.8 V                  |   | 1.0                             |         | 4.0  | MHz                |    |
|  | f <sub>EXS</sub>                      |  |   | 32                              |         | 35   | kHz                |    |
| External system clock input high-level width, low-level width    | t <sub>EXH</sub> , t <sub>EXL</sub>   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V                  |   | 24                              |         |      | ns                 |    |
|  |                                       | 2.4 V ≤ V <sub>DD</sub> < 2.7 V                  |   | 30                              |         |      | ns                 |    |
|  |                                       | 1.8 V ≤ V <sub>DD</sub> < 2.4 V                  |   | 60                              |         |      | ns                 |    |
|  |                                       | 1.6 V ≤ V <sub>DD</sub> < 1.8 V                  |   | 120                             |         |      | ns                 |    |
|  | t <sub>EXHS</sub> , t <sub>EXLS</sub> |  |   | 13.7                            |         |      | μs                 |    |
| Ti00, Ti01, Ti03 to Ti07 input high-level width, low-level width | t <sub>TIH</sub> , t <sub>TIL</sub>   |  |   | 1/f <sub>MCK</sub> +10          |         |      | ns <sup>Note</sup> |    |
| TO00, TO01, TO03 to TO07 output frequency                        | f <sub>TO</sub>                       | HS (high-speed main) mode                        | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 8    | MHz                |    |
|  |                                       |  | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V                                       |                                 |         | 4    | MHz                |    |
|  |                                       |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                                       |                                 |         | 2    | MHz                |    |
|  |                                       | LS (low-speed main) mode                         | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 4    | MHz                |    |
|  |                                       |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                                       |                                 |         | 2    | MHz                |    |
|  |                                       | LV (low-voltage main) mode                       | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 2    | MHz                |    |
| PCLBUZ0, PCLBUZ1 output frequency                                | f <sub>PCL</sub>                      | HS (high-speed main) mode                        | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 8    | MHz                |    |
|  |                                       |  | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V                                       |                                 |         | 4    | MHz                |    |
|  |                                       |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                                       |                                 |         | 2    | MHz                |    |
|  |                                       | LS (low-speed main) mode                         | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 4    | MHz                |    |
|  |                                       |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                                       |                                 |         | 2    | MHz                |    |
|  |                                       | LV (low-voltage main) mode                       | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 4    | MHz                |    |
|  |                                       | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V                |   |                                 | 2       | MHz  |                    |    |
| Interrupt input high-level width, low-level width                | t <sub>INTH</sub> , t <sub>INTL</sub> | INTP0  | 1.6 V ≤ V <sub>DD</sub> ≤ 3.6 V   | 1                               |         |      | μs                 |    |
|  |                                       | INTP1 to INTP11                                  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       | 1                               |         |      | μs                 |    |
| Key interrupt input high-level width, low-level width            | t <sub>KR</sub>                       | KR0 to KR9                                       | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>1.8 V ≤ AV <sub>DD0</sub> ≤ 3.6 V | 250                             |         |      | ns                 |    |
|  |                                       |  | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>1.6 V ≤ AV <sub>DD0</sub> < 1.8 V | 1                               |         |      | μs                 |    |
| RESET low-level width  | t <sub>RSL</sub>                      |  |   | 10                              |         |      | μs                 |    |

(Note and Remark are listed on the next page.)

**Note** The following conditions are required for low-voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.

1.8 V ≤ EV<sub>DD0</sub> < 2.7 V : MIN. 125 ns

1.6 V ≤ EV<sub>DD0</sub> < 1.8 V : MIN. 250 ns

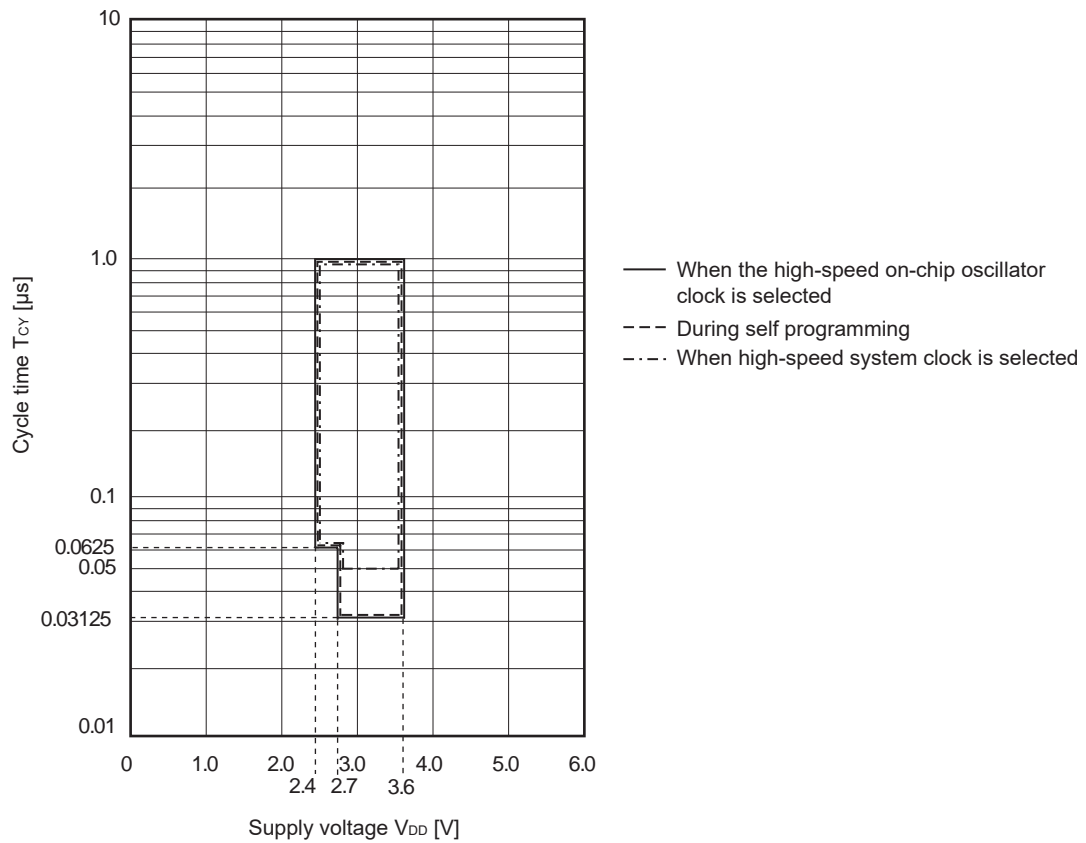
**Remark** f<sub>MCK</sub>: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer clock select register 0 (TPS0) and timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

**Minimum Instruction Execution Time during Main System Clock Operation**

<R>

T<sub>CY</sub> vs V<sub>DD</sub> (HS (high-speed main) mode)



<R>

T<sub>CY</sub> vs V<sub>DD</sub> (LS (low-speed main) mode)

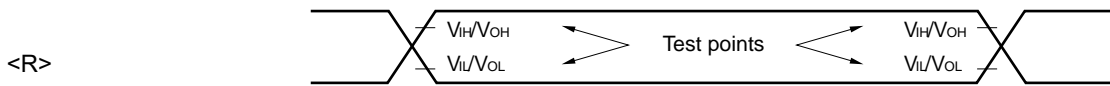


<R>

T<sub>CY</sub> vs V<sub>DD</sub> (LV (low-voltage main) mode)



**AC Timing Test Points**



**External System Clock Timing**



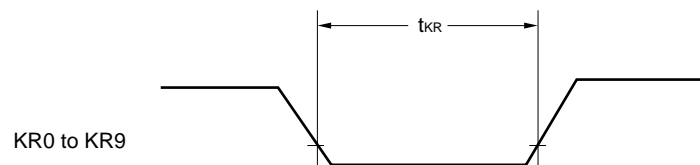
<R> **TI/TO Timing**



**Interrupt Request Input Timing**



**Key Interrupt Input Timing**



**$\overline{\text{RESET}}$  Input Timing**

## 2.5 Peripheral Functions Characteristics

### AC Timing Test Points



### 2.5.1 Serial array unit

#### (1) During communication at same potential (UART mode)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                       | Symbol | Conditions  | HS <sup>Note 1</sup> |                       | LS <sup>Note 2</sup> |                       | LV <sup>Note 3</sup> |                     | Unit |
|---------------------------------|--------|---|----------------------|-----------------------|----------------------|-----------------------|----------------------|---------------------|------|
|                                 |        |   | MIN.                 | MAX.                  | MIN.                 | MAX.                  | MIN.                 | MAX.                |      |
| Transfer rate <sup>Note 4</sup> |        | 2.4 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 6</sup> |                      | 5.3 <sup>Note 5</sup> |                      | 1.3                   |                      | 0.6                 | Mbps |
|                                 |        | 1.8 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 6</sup> |                      | 5.3 <sup>Note 5</sup> |                      | 1.3                   |                      | 0.6                 | Mbps |
|                                 |        | 1.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 6</sup> |                      | 5.3 <sup>Note 5</sup> |                      | 1.3 <sup>Note 5</sup> |                      | 0.6                 | Mbps |
|                                 |        | 1.6 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |                      | -                     |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 6</sup> |                      | -                     |                      | 1.3 <sup>Note 5</sup> |                      | 0.6                 | Mbps |

- Notes 1.** HS is condition of HS (high-speed main) mode.  
**2.** LS is condition of LS (low-speed main) mode.  
**3.** LV is condition of LV (low-voltage main) mode.  
**4.** Transfer rate in the SNOOZE mode is 4800 bps.  
**5.** The following conditions are required for low-voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.  
 2.4 V ≤ EV<sub>DD0</sub> < 2.7 V : MAX. 2.6 Mbps  
 1.8 V ≤ EV<sub>DD0</sub> < 2.4 V : MAX. 1.3 Mbps  
 1.6 V ≤ EV<sub>DD0</sub> < 1.8 V : MAX. 0.6 Mbps  
**6.** f<sub>CLK</sub> in each operating mode is as below.  
 HS (high-speed main) mode: f<sub>CLK</sub> = 32 MHz  
 LS (low-speed main) mode: f<sub>CLK</sub> = 8 MHz  
 LV (low-voltage main) mode: f<sub>CLK</sub> = 4 MHz

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode connection diagram (during communication at same potential)**



**UART mode bit width (during communication at same potential) (reference)**



- Remarks**
1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter   | Symbol                                 | Conditions   | HS <sup>Note 1</sup>        |      | LS <sup>Note 2</sup>        |      | LV <sup>Note 3</sup>        |      | Unit |
|---|--|--|-----------------------------|------|-----------------------------|------|-----------------------------|------|------|
|   |  |  | MIN.                        | MAX. | MIN.                        | MAX. | MIN.                        | MAX. |      |
| SCKp cycle time                                       | t <sub>KCY1</sub>                      | 2.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V    t <sub>KCY1</sub> ≥ 2/f <sub>CLK</sub> | 83.3                        |      | 250                         |      | 500                         |      | ns   |
| SCKp high-/low-level width                            | t <sub>KH1</sub> ,<br>t <sub>KL1</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V   | t <sub>KCY1</sub> /2<br>-10 |      | t <sub>KCY1</sub> /2<br>-50 |      | t <sub>KCY1</sub> /2<br>-50 |      | ns   |
| Slp setup time (to SCKp↑) <sup>Note 4</sup>           | t <sub>SIK1</sub>                      | 2.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V   | 33                          |      | 110                         |      | 110                         |      | ns   |
| Slp hold time (from SCKp↑) <sup>Note 4</sup>          | t <sub>KSI1</sub>                      | 2.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V   | 10                          |      | 10                          |      | 10                          |      | ns   |
| Delay time from SCKp↓ to SOp output <sup>Note 5</sup> | t <sub>KSO1</sub>                      | C = 20 pF <sup>Note 6</sup>  |                             | 10   |                             | 10   |                             | 10   | ns   |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time or Slp hold time becomes "from SCKp↓" when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**5.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes "from SCKp↑" when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**6.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),  
g: PIM and POM numbers (g = 1)

**2.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number,  
n: Channel number (mn = 00))



**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**  
**(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

| Parameter  | Symbol                                 | Conditions                        | HS <sup>Note 1</sup>                   |                              | LS <sup>Note 2</sup> |                              | LV <sup>Note 3</sup> |                              | Unit |    |
|--|--|-----------------------------------|--|------------------------------|----------------------|------------------------------|----------------------|------------------------------|------|----|
|  |  |                                   | MIN.                                   | MAX.                         | MIN.                 | MAX.                         | MIN.                 | MAX.                         |      |    |
| SCKp cycle time  | t <sub>KCY2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 125                          |                      | 500                          |                      | 1000                         | ns   |    |
|  |  | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 250                          |                      | 500                          |                      | 1000                         | ns   |    |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 500                          |                      | 500                          |                      | 1000                         | ns   |    |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 1000                         |                      | 1000                         |                      | 1000                         | ns   |    |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | –                            |                      | 1000                         |                      | 1000                         | ns   |    |
| SCKp high-/low-level width                               | t <sub>KH2</sub> ,<br>t <sub>KL2</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | t <sub>KCY2</sub> /2<br>–18  |                      | t <sub>KCY2</sub> /2<br>–50  |                      | t <sub>KCY2</sub> /2<br>–50  | ns   |    |
|  |  | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | t <sub>KCY2</sub> /2<br>–38  |                      | t <sub>KCY2</sub> /2<br>–50  |                      | t <sub>KCY2</sub> /2<br>–50  | ns   |    |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | t <sub>KCY2</sub> /2<br>–50  |                      | t <sub>KCY2</sub> /2<br>–50  |                      | t <sub>KCY2</sub> /2<br>–50  | ns   |    |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | t <sub>KCY2</sub> /2<br>–100 |                      | t <sub>KCY2</sub> /2<br>–100 |                      | t <sub>KCY2</sub> /2<br>–100 | ns   |    |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | –                            |                      | t <sub>KCY2</sub> /2<br>–100 |                      | t <sub>KCY2</sub> /2<br>–100 | ns   |    |
| Slp setup time<br>(to SCKp↑) <sup>Note 4</sup>           | t <sub>SIK2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | 44                           |                      | 110                          |                      | 110                          | ns   |    |
|  |  | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | 75                           |                      | 110                          |                      | 110                          | ns   |    |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | 110                          |                      | 110                          |                      | 110                          | ns   |    |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | 220                          |                      | 220                          |                      | 220                          | ns   |    |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |  | –                            |                      | 220                          |                      | 220                          | ns   |    |
| Slp hold time<br>(from SCKp↑) <sup>Note 4</sup>          | t <sub>SI2</sub>                       | 1.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |  | 19                           |                      | 19                           |                      | 19                           | ns   |    |
|  |  | 1.6 V ≤ EV <sub>DD</sub> ≤ 3.6 V  |  | –                            |                      | 19                           |                      | 19                           | ns   |    |
| Delay time from SCKp↓<br>to SOp output <sup>Note 5</sup> | t <sub>KS02</sub>                      | 1.7 V ≤ EV <sub>DD</sub> ≤ 3.6 V  | C = 30 pF <sup>Note 6</sup>            |                              | 25                   |                              | 25                   |                              | 25   | ns |
|  |  | 1.6 V ≤ EV <sub>DD</sub> ≤ 3.6 V  | C = 30 pF <sup>Note 6</sup>            |                              | –                    |                              | 25                   |                              | 25   | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** When DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 0, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 1. The Slp setup time or Slp hold time becomes “from SCKp↓” when DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 1, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 0.

**5.** When DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 0, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 1, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 0.

**6.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

## (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter  | Symbol                                 | Conditions                        |                                   | HS <sup>Note 1</sup>                |                            | LS <sup>Note 2</sup>                |                            | LV <sup>Note 3</sup>                |                            | Unit |
|--|--|-----------------------------------|-----------------------------------|-------------------------------------|----------------------------|-------------------------------------|----------------------------|-------------------------------------|----------------------------|------|
|  |  |                                   |                                   | MIN.                                | MAX.                       | MIN.                                | MAX.                       | MIN.                                | MAX.                       |      |
| SCKp cycle time <sup>Note 4</sup>                        | t <sub>KCY2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 16 MHz < f <sub>MCK</sub>         | 8/f <sub>MCK</sub>                  |                            | –                                   |                            | –                                   |                            | ns   |
|  |  |                                   | f <sub>MCK</sub> ≤ 16 MHz         | 6/f <sub>MCK</sub>                  |                            | 6/f <sub>MCK</sub>                  |                            | 6/f <sub>MCK</sub>                  |                            | ns   |
|  |  | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 6/f <sub>MCK</sub><br>and<br>500ns  |                            | 6/f <sub>MCK</sub><br>and<br>500ns  |                            | 6/f <sub>MCK</sub><br>and<br>500ns  |                            | ns   |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 6/f <sub>MCK</sub><br>and<br>750ns  |                            | 6/f <sub>MCK</sub><br>and<br>750ns  |                            | 6/f <sub>MCK</sub><br>and<br>750ns  |                            | ns   |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 6/f <sub>MCK</sub><br>and<br>1500ns |                            | 6/f <sub>MCK</sub><br>and<br>1500ns |                            | 6/f <sub>MCK</sub><br>and<br>1500ns |                            | ns   |
| 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                        |  | –                                 |                                   | 6/f <sub>MCK</sub><br>and<br>1500ns |                            | 6/f <sub>MCK</sub><br>and<br>1500ns |                            | ns                                  |                            |      |
| SCKp high-/low-level width                               | t <sub>KH2</sub> ,<br>t <sub>KL2</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | t <sub>KCY2</sub> /2<br>–8          |                            | t <sub>KCY2</sub> /2<br>–8          |                            | t <sub>KCY2</sub> /2<br>–8          |                            | ns   |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | t <sub>KCY2</sub> /2<br>–18         |                            | t <sub>KCY2</sub> /2<br>–18         |                            | t <sub>KCY2</sub> /2<br>–18         |                            | ns   |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | t <sub>KCY2</sub> /2<br>–66         |                            | t <sub>KCY2</sub> /2<br>–66         |                            | t <sub>KCY2</sub> /2<br>–66         |                            | ns   |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | –                                   |                            | t <sub>KCY2</sub> /2<br>–66         |                            | t <sub>KCY2</sub> /2<br>–66         |                            | ns   |
| Slp setup time<br>(to SCKp↑) <sup>Note 5</sup>           | t <sub>SIK2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 1/f <sub>MCK</sub><br>+20           |                            | 1/f <sub>MCK</sub><br>+30           |                            | 1/f <sub>MCK</sub><br>+30           |                            | ns   |
|  |  | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 1/f <sub>MCK</sub><br>+30           |                            | 1/f <sub>MCK</sub><br>+30           |                            | 1/f <sub>MCK</sub><br>+30           |                            | ns   |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 1/f <sub>MCK</sub><br>+40           |                            | 1/f <sub>MCK</sub><br>+40           |                            | 1/f <sub>MCK</sub><br>+40           |                            | ns   |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | –                                   |                            | 1/f <sub>MCK</sub><br>+40           |                            | 1/f <sub>MCK</sub><br>+40           |                            | ns   |
| Slp hold time<br>(from SCKp↑) <sup>Note 5</sup>          | t <sub>SIK2</sub>                      | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 1/f <sub>MCK</sub><br>+31           |                            | 1/f <sub>MCK</sub><br>+31           |                            | 1/f <sub>MCK</sub><br>+31           |                            | ns   |
|  |  | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | 1/f <sub>MCK</sub> +<br>250         |                            | 1/f <sub>MCK</sub> +<br>250         |                            | 1/f <sub>MCK</sub> +<br>250         |                            | ns   |
|  |  | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                   | –                                   |                            | 1/f <sub>MCK</sub> +<br>250         |                            | 1/f <sub>MCK</sub> +<br>250         |                            | ns   |
| Delay time from SCKp↓<br>to SOp output <sup>Note 6</sup> | t <sub>KSO2</sub>                      | C = 30 pF <sup>Note 7</sup>       | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                     | 2/f <sub>MCK</sub><br>+44  |                                     | 2/f <sub>MCK</sub><br>+110 |                                     | 2/f <sub>MCK</sub><br>+110 | ns   |
|  |  |                                   | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                     | 2/f <sub>MCK</sub><br>+75  |                                     | 2/f <sub>MCK</sub><br>+110 |                                     | 2/f <sub>MCK</sub><br>+110 | ns   |
|  |  |                                   | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                     | 2/f <sub>MCK</sub><br>+110 |                                     | 2/f <sub>MCK</sub><br>+110 |                                     | 2/f <sub>MCK</sub><br>+110 | ns   |
|  |  |                                   | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                     | 2/f <sub>MCK</sub><br>+220 |                                     | 2/f <sub>MCK</sub><br>+220 |                                     | 2/f <sub>MCK</sub><br>+220 | ns   |
|  |  |                                   | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V |                                     | –                          |                                     | 2/f <sub>MCK</sub><br>+220 |                                     | 2/f <sub>MCK</sub><br>+220 | ns   |

(Note, Caution and Remark are listed on the next page.)

- Notes**
1. HS is condition of HS (high-speed main) mode.
  2. LS is condition of LS (low-speed main) mode.
  3. LV is condition of LV (low-voltage main) mode.
  4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
  5. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  6. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  7. C is the load capacitance of the SOp output lines.

**Caution** Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM number (g = 0, 1)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**CSI mode connection diagram (during communication at same potential)**



**CSI mode serial transfer timing (during communication at same potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
  2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) During communication at same potential (simplified I<sup>2</sup>C mode) (1/2)(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                   | Symbol              | Conditions  | HS <sup>Note 1</sup>                          |                        | LS <sup>Note 2</sup>                          |                       | LV <sup>Note 3</sup>                          |                       | Unit |
|-----------------------------|---------------------|---|---|------------------------|---|-----------------------|---|-----------------------|------|
|                             |                     |   | MIN.  | MAX.                   | MIN.  | MAX.                  | MIN.  | MAX.                  |      |
| SCLr clock frequency        | f <sub>SCL</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ |   | 1000 <sup>Note 4</sup> |   | 400 <sup>Note 4</sup> |   | 400 <sup>Note 4</sup> | kHz  |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  |   | 400 <sup>Note 4</sup>  |   | 400 <sup>Note 4</sup> |   | 400 <sup>Note 4</sup> | kHz  |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  |   | 300 <sup>Note 4</sup>  |   | 300 <sup>Note 4</sup> |   | 300 <sup>Note 4</sup> | kHz  |
|                             |                     | 1.7 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  |   | 250 <sup>Note 4</sup>  |   | 250 <sup>Note 4</sup> |   | 250 <sup>Note 4</sup> | kHz  |
|                             |                     | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  |   | –                      |   | 250 <sup>Note 4</sup> |   | 250 <sup>Note 4</sup> | kHz  |
| Hold time when SCLr = "L"   | t <sub>LOW</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 475   |                        | 1150  |                       | 1150  |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1150  |                        | 1150  |                       | 1150  |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1550  |                        | 1550  |                       | 1550  |                       | ns   |
|                             |                     | 1.7 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1850  |                        | 1850  |                       | 1850  |                       | ns   |
|                             |                     | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | –   |                        | 1850  |                       | 1850  |                       | ns   |
| Hold time when SCLr = "H"   | t <sub>HIGH</sub>   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 475   |                        | 1150  |                       | 1150  |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1150  |                        | 1150  |                       | 1150  |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1550  |                        | 1550  |                       | 1550  |                       | ns   |
|                             |                     | 1.7 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1850  |                        | 1850  |                       | 1850  |                       | ns   |
|                             |                     | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | –   |                        | 1850  |                       | 1850  |                       | ns   |
| Data setup time (reception) | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 1/f <sub>MCK</sub> +<br>85 <sup>Note 5</sup>  |                        | 1/f <sub>MCK</sub> +<br>145 <sup>Note 5</sup> |                       | 1/f <sub>MCK</sub> +<br>145 <sup>Note 5</sup> |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1/f <sub>MCK</sub> +<br>145 <sup>Note 5</sup> |                        | 1/f <sub>MCK</sub> +<br>145 <sup>Note 5</sup> |                       | 1/f <sub>MCK</sub> +<br>145 <sup>Note 5</sup> |                       | ns   |
|                             |                     | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1/f <sub>MCK</sub> +<br>230 <sup>Note 5</sup> |                        | 1/f <sub>MCK</sub> +<br>230 <sup>Note 5</sup> |                       | 1/f <sub>MCK</sub> +<br>230 <sup>Note 5</sup> |                       | ns   |
|                             |                     | 1.7 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1/f <sub>MCK</sub> +<br>290 <sup>Note 5</sup> |                        | 1/f <sub>MCK</sub> +<br>290 <sup>Note 5</sup> |                       | 1/f <sub>MCK</sub> +<br>290 <sup>Note 5</sup> |                       | ns   |
|                             |                     | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | –   |                        | 1/f <sub>MCK</sub> +<br>290 <sup>Note 5</sup> |                       | 1/f <sub>MCK</sub> +<br>290 <sup>Note 5</sup> |                       | ns   |

(Notes, Caution and Remarks are listed on the next page.)

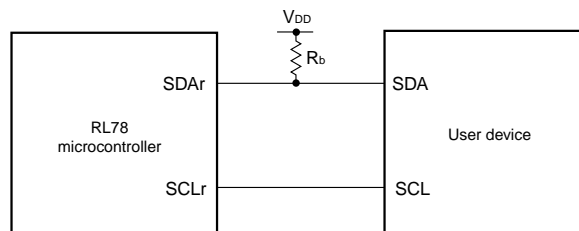
**(5) During communication at same potential (simplified I<sup>2</sup>C mode) (2/2)**  
 (T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                     | Symbol              | Conditions  | HS <sup>Note 1</sup> |      | LS <sup>Note 2</sup> |      | LV <sup>Note 3</sup> |      | Unit |
|-------------------------------|---------------------|---|----------------------|------|----------------------|------|----------------------|------|------|
|                               |                     |   | MIN.                 | MAX. | MIN.                 | MAX. | MIN.                 | MAX. |      |
| Data hold time (transmission) | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 0                    | 305  | 0                    | 305  | 0                    | 305  | ns   |
|                               |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 0                    | 355  | 0                    | 355  | 0                    | 355  | ns   |
|                               |                     | 1.8 V ≤ EV <sub>DD0</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 0                    | 405  | 0                    | 405  | 0                    | 405  | ns   |
|                               |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 0                    | 405  | 0                    | 405  | 0                    | 405  | ns   |
|                               |                     | 1.6 V ≤ EV <sub>DD0</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | -                    | -    | 0                    | 405  | 0                    | 405  | ns   |

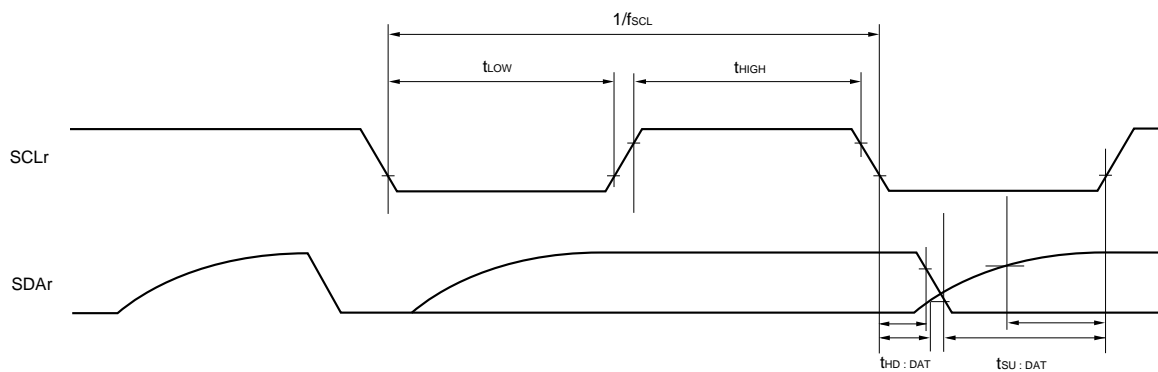
- Notes 1.** HS is condition of HS (high-speed main) mode.
- 2.** LS is condition of LS (low-speed main) mode.
- 3.** LV is condition of LV (low-voltage main) mode.
- 4.** The value must also be f<sub>CLK</sub>/4 or lower.
- 5.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

**Simplified I<sup>2</sup>C mode mode connection diagram (during communication at same potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**



- Remarks 1.** R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance
- 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)
- 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output)**  
(1/2)

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                       | Symbol | Conditions |  | HS <sup>Note 1</sup> |   | LS <sup>Note 2</sup> |                          | LV <sup>Note 3</sup> |                     | Unit |
|---------------------------------|--------|------------|--|----------------------|---|----------------------|--------------------------|----------------------|---------------------|------|
|                                 |        |            |  | MIN.                 | MAX.  | MIN.                 | MAX.                     | MIN.                 | MAX.                |      |
| Transfer rate <sup>Note 4</sup> |        | Reception  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V                   |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6      |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        |            |  |                      | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 7</sup> |                      | 5.3                      |                      | 1.3                 |      |
|                                 |        |            | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> |                      | f <sub>MCK</sub> /6   |                      | f <sub>MCK</sub> /6      |                      | f <sub>MCK</sub> /6 | bps  |
|                                 |        |            |  |                      | Theoretical value of the maximum transfer rate<br>f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 7</sup> |                      | 5.3<br><sup>Note 6</sup> |                      | 1.3                 |      |

- Notes 1.** HS is condition of HS (high-speed main) mode.  
**2.** LS is condition of LS (low-speed main) mode.  
**3.** LV is condition of LV (low-voltage main) mode.  
**4.** Transfer rate in the SNOOZE mode is 4800 bps.  
**5.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.  
**6.** The following conditions are required for low-voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.  
 2.4 V ≤ EV<sub>DD0</sub> < 2.7 V : MAX. 2.6 Mbps  
 1.8 V ≤ EV<sub>DD0</sub> < 2.4 V : MAX. 1.3 Mbps  
**7.** f<sub>CLK</sub> in each operating mode is as below.  
 HS (high-speed main) mode: f<sub>CLK</sub> = 32 MHz  
 LS (low-speed main) mode: f<sub>CLK</sub> = 8 MHz  
 LV (low-voltage main) mode: f<sub>CLK</sub> = 4 MHz

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

- Remarks 1.** V<sub>b</sub>[V]: Communication line voltage  
**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)  
**3.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output)**  
**(2/2)**

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter     | Symbol | Conditions   |  | HS <sup>Note 1</sup> |                | LS <sup>Note 2</sup> |                | LV <sup>Note 3</sup> |                | Unit |
|---------------|--------|--------------|--|----------------------|----------------|----------------------|----------------|----------------------|----------------|------|
|               |        |              |  | MIN.                 | MAX.           | MIN.                 | MAX.           | MIN.                 | MAX.           |      |
| Transfer rate |        | Transmission | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V                   |                      | Note 4         |                      | Note 4         |                      | Note 4         | bps  |
|               |        |              |  |                      | 1.2<br>Note 5  |                      | 1.2<br>Note 5  |                      | 1.2<br>Note 5  | Mbps |
|               |        |              | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> |                      | Note 7         |                      | Note 7         |                      | Note 7         | bps  |
|               |        |              |  |                      | 0.43<br>Note 8 |                      | 0.43<br>Note 8 |                      | 0.43<br>Note 8 | Mbps |

- Notes**
- HS is condition of HS (high-speed main) mode.
  - LS is condition of LS (low-speed main) mode.
  - LV is condition of LV (low-voltage main) mode.
  - The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> ≤ 3.6 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 4** above to calculate the maximum transfer rate under conditions of the customer.
- Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.
- The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

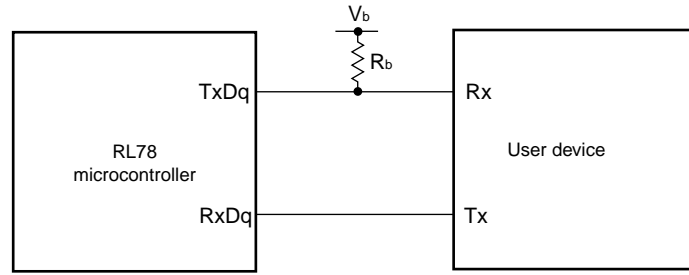
- This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

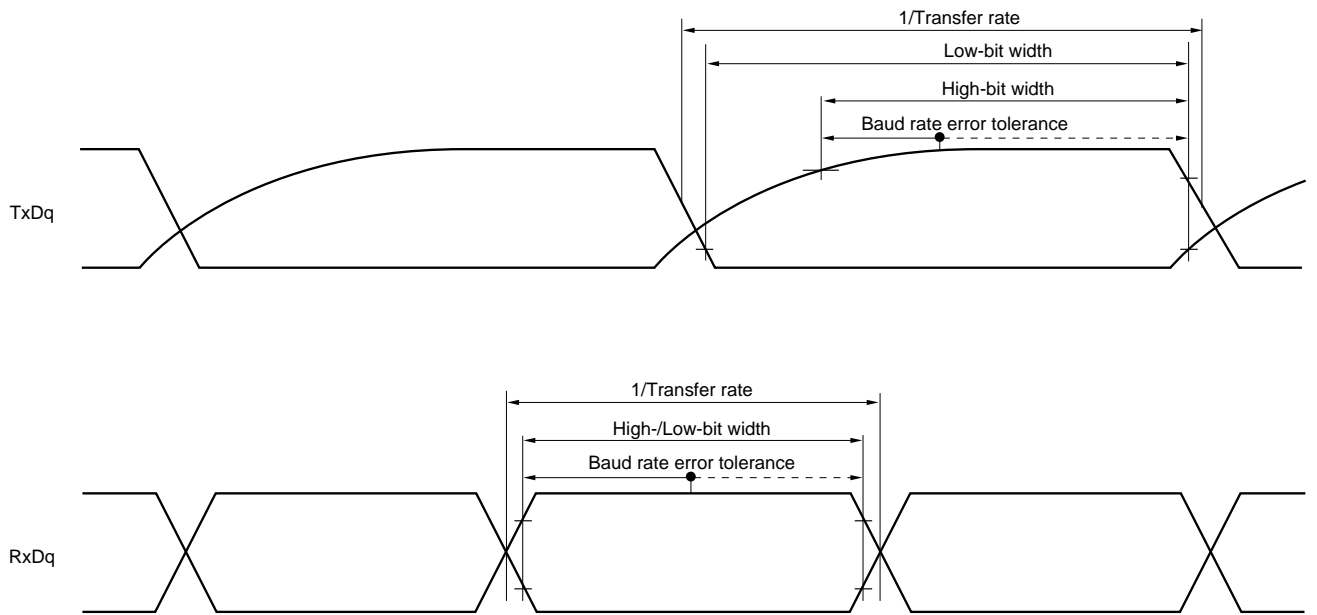
<R>



**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**



- Remarks**
1. R<sub>b</sub>[Ω]: Communication line (TxDq) pull-up resistance,  
C<sub>b</sub>[F]: Communication line (TxDq) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**

(T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter  | Symbol            | Conditions   | HS <sup>Note 1</sup>                   |      | LS <sup>Note 2</sup> |                        | LV <sup>Note 3</sup> |                        | Unit |    |
|--|-------------------|--|--|------|----------------------|------------------------|----------------------|------------------------|------|----|
|  |                   |  | MIN.                                   | MAX. | MIN.                 | MAX.                   | MIN.                 | MAX.                   |      |    |
| SCKp cycle time  | t <sub>KCY1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ | t <sub>KCY1</sub> ≥ 2/f <sub>CLK</sub> | 300  |                      | 1150                   |                      | 1150                   |      | ns |
| SCKp high-level width                                    | t <sub>KH1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    | t <sub>KCY1</sub> /2 –                 | 120  |                      | t <sub>KCY1</sub> /2 – | 120                  | t <sub>KCY1</sub> /2 – | 120  | ns |
| SCKp low-level width                                     | t <sub>KL1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    | t <sub>KCY1</sub> /2 –                 | 10   |                      | t <sub>KCY1</sub> /2 – | 50                   | t <sub>KCY1</sub> /2 – | 50   | ns |
| Slp setup time<br>(to SCKp↑) <sup>Note 4</sup>           | t <sub>SIK1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  | 121  |                      | 479                    |                      | 479                    |      | ns |
| Slp hold time<br>(from SCKp↑) <sup>Note 4</sup>          | t <sub>KSI1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  | 10   |                      | 10                     |                      | 10                     |      | ns |
| Delay time from SCKp↓ to<br>SOp output <sup>Note 4</sup> | t <sub>KSO1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  |      | 130                  |                        | 130                  |                        | 130  | ns |
| Slp setup time<br>(to SCKp↓) <sup>Note 5</sup>           | t <sub>SIK1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  | 33   |                      | 110                    |                      | 110                    |      | ns |
| Slp hold time<br>(from SCKp↓) <sup>Note 5</sup>          | t <sub>KSI1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  | 10   |                      | 10                     |                      | 10                     |      | ns |
| Delay time from SCKp↑ to<br>SOp output <sup>Note 5</sup> | t <sub>KSO1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ    |  |      | 10                   |                        | 10                   |                        | 10   | ns |

- Notes**
1. HS is condition of HS (high-speed main) mode.
  2. LS is condition of LS (low-speed main) mode.
  3. LV is condition of LV (low-voltage main) mode.
  4. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1.
  5. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

<R>

- Remarks**
1. R<sub>b</sub>[Ω]: Communication line (SCKp, SOp) pull-up resistance, C<sub>b</sub>[F]: Communication line (SCKp, SOp) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**(8) Communication at different potential (1.8V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

| Parameter             | Symbol            | Conditions  |  | HS <sup>Note 1</sup>          |      | LS <sup>Note 2</sup>          |      | LV <sup>Note 3</sup>          |      | Unit |
|-----------------------|-------------------|---|--|-------------------------------|------|-------------------------------|------|-------------------------------|------|------|
|                       |                   |   |  | MIN.                          | MAX. | MIN.                          | MAX. | MIN.                          | MAX. |      |
| SCKp cycle time       | t <sub>KCY1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 500                           |      | 1150                          |      | 1150                          |      | ns   |
|                       |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 4</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ | t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> | 1150                          |      | 1150                          |      | 1150                          |      | ns   |
| SCKp high-level width | t <sub>KH1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                       |  | t <sub>KCY1</sub> /2 –<br>170 |      | t <sub>KCY1</sub> /2 –<br>170 |      | t <sub>KCY1</sub> /2 –<br>170 |      | ns   |
|                       |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 4</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ    |  | t <sub>KCY1</sub> /2 –<br>458 |      | t <sub>KCY1</sub> /2 –<br>458 |      | t <sub>KCY1</sub> /2 –<br>458 |      | ns   |
| SCKp low-level width  | t <sub>KL1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                       |  | t <sub>KCY1</sub> /2 –<br>18  |      | t <sub>KCY1</sub> /2 –<br>50  |      | t <sub>KCY1</sub> /2 –<br>50  |      | ns   |
|                       |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 4</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ    |  | t <sub>KCY1</sub> /2 –<br>50  |      | t <sub>KCY1</sub> /2 –<br>50  |      | t <sub>KCY1</sub> /2 –<br>50  |      | ns   |

**Notes 1.** HS is condition of HS (high-speed main) mode.**2.** LS is condition of LS (low-speed main) mode.**3.** LV is condition of LV (low-voltage main) mode.**4.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

&lt;R&gt;

**Remarks 1.** R<sub>b</sub>[Ω]: Communication line (SCKp, SOp) pull-up resistance, C<sub>b</sub>[F]: Communication line (SCKp, SOp) load capacitance, V<sub>b</sub>[V]: Communication line voltage

**2.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**3.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

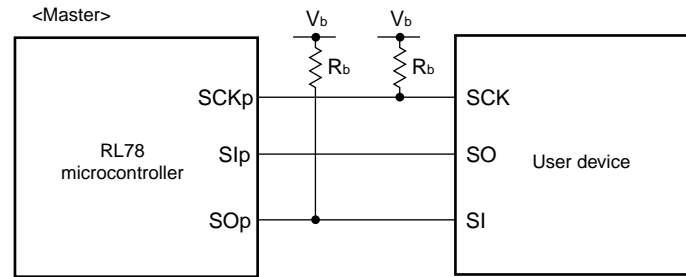
| Parameter  | Symbol            | Conditions   | HS <sup>Note 1</sup> |      | LS <sup>Note 2</sup> |      | LV <sup>Note 3</sup> |      | Unit |
|--|-------------------|--|----------------------|------|----------------------|------|----------------------|------|------|
|  |                   |  | MIN.                 | MAX. | MIN.                 | MAX. | MIN.                 | MAX. |      |
| Slp setup time<br>(to SCKp↑) <sup>Note 4</sup>           | t <sub>SIK1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    | 177                  |      | 479                  |      | 479                  |      | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ | 479                  |      | 479                  |      | 479                  |      | ns   |
| Slp hold time<br>(from SCKp↑) <sup>Note 4</sup>          | t <sub>SI1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    | 19                   |      | 19                   |      | 19                   |      | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ | 19                   |      | 19                   |      | 19                   |      | ns   |
| Delay time from SCKp↓ to<br>SOp output <sup>Note 4</sup> | t <sub>KSO1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    |                      | 195  |                      | 195  |                      | 195  | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ |                      | 483  |                      | 483  |                      | 483  | ns   |
| Slp setup time<br>(to SCKp↓) <sup>Note 5</sup>           | t <sub>SIK1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    | 44                   |      | 110                  |      | 110                  |      | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ | 110                  |      | 110                  |      | 110                  |      | ns   |
| Slp hold time<br>(from SCKp↓) <sup>Note 5</sup>          | t <sub>SI1</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    | 19                   |      | 19                   |      | 19                   |      | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ | 19                   |      | 19                   |      | 19                   |      | ns   |
| Delay time from SCKp↑ to<br>SOp output <sup>Note 5</sup> | t <sub>KSO1</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    |                      | 25   |                      | 25   |                      | 25   | ns   |
|  |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 6</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ |                      | 25   |                      | 25   |                      | 25   | ns   |

**Notes 1.** HS is condition of HS (high-speed main) mode.**2.** LS is condition of LS (low-speed main) mode.**3.** LV is condition of LV (low-voltage main) mode.**4.** When DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 0, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 1.**5.** When DAP<sub>m</sub>n = 0 and CKP<sub>m</sub>n = 1, or DAP<sub>m</sub>n = 1 and CKP<sub>m</sub>n = 0.**6.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

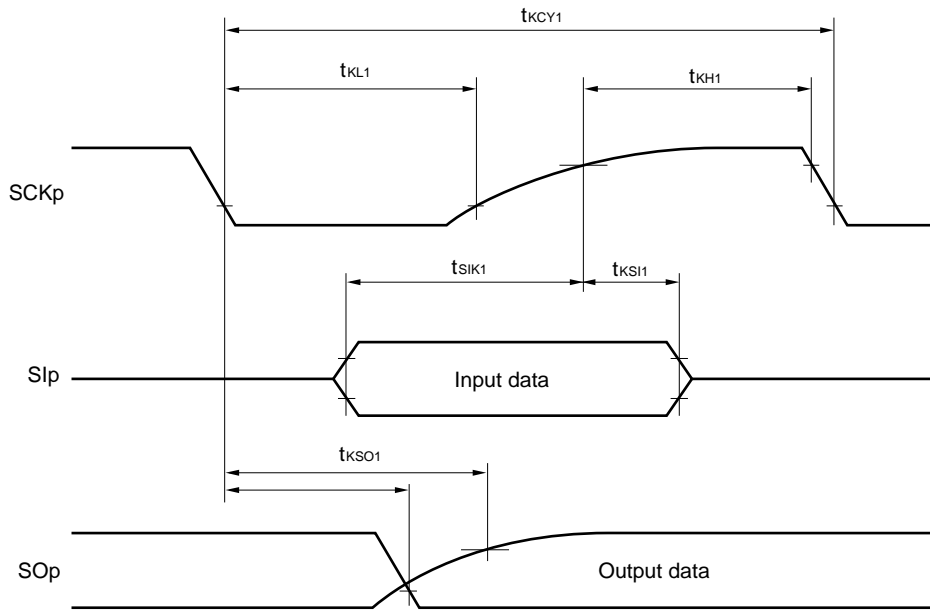
&lt;R&gt;

**(Remarks** are listed on the next page.)

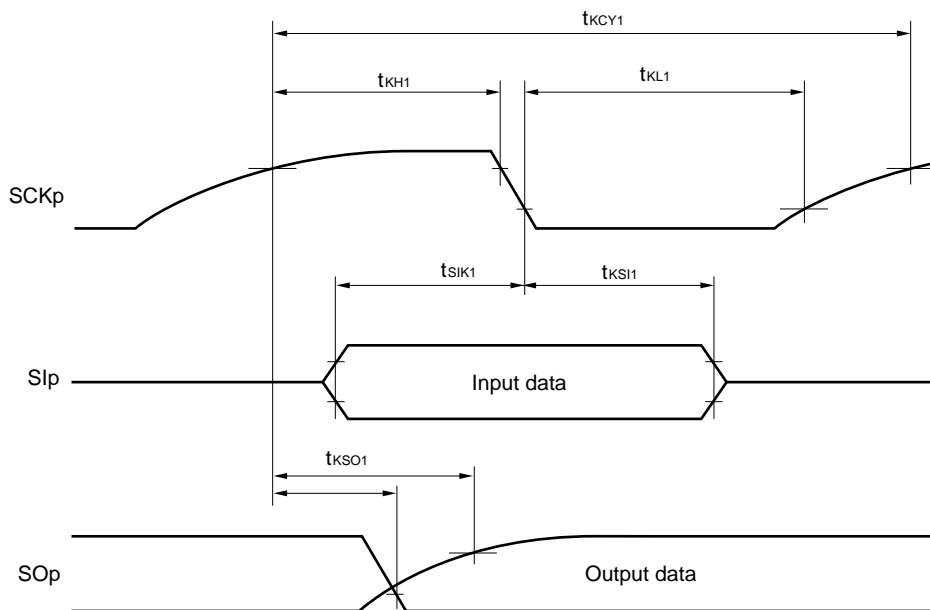
**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)  
(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter   | Symbol                                 | Conditions   | HS <sup>Note 1</sup>               |                             | LS <sup>Note 2</sup>         |                             | LV <sup>Note 3</sup>         |                             | Unit |
|---|--|--|------------------------------------|-----------------------------|------------------------------|-----------------------------|------------------------------|-----------------------------|------|
|   |  |  | MIN.                               | MAX.                        | MIN.                         | MAX.                        | MIN.                         | MAX.                        |      |
| SCKp cycle time <sup>Note 4</sup>                     | t <sub>KCY2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V   | 24 MHz < f <sub>MCK</sub>          | 20/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 20 MHz < f <sub>MCK</sub> ≤ 24 MHz | 16/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 16 MHz < f <sub>MCK</sub> ≤ 20 MHz | 14/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 8 MHz < f <sub>MCK</sub> ≤ 16 MHz  | 12/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   | 8/f <sub>MCK</sub>          |                              | 16/f <sub>MCK</sub>         |                              | –                           | ns   |
|   |  |  | f <sub>MCK</sub> ≤ 4 MHz           | 6/f <sub>MCK</sub>          |                              | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         | ns   |
|   |  | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup>   | 24 MHz < f <sub>MCK</sub>          | 48/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 20 MHz < f <sub>MCK</sub> ≤ 24 MHz | 36/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 16 MHz < f <sub>MCK</sub> ≤ 20 MHz | 32/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 8 MHz < f <sub>MCK</sub> ≤ 16 MHz  | 26/f <sub>MCK</sub>         |                              | –                           |                              | –                           | ns   |
|   |  |  | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   | 16/f <sub>MCK</sub>         |                              | 16/f <sub>MCK</sub>         |                              | –                           | ns   |
| f <sub>MCK</sub> ≤ 4 MHz                              | 10/f <sub>MCK</sub>                    |  | 10/f <sub>MCK</sub>                |                             | 10/f <sub>MCK</sub>          | ns                          |                              |                             |      |
| SCKp high-/low-level width                            | t <sub>KH2</sub> ,<br>t <sub>KL2</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V  | t <sub>KCY2</sub> /2<br>– 18       |                             | t <sub>KCY2</sub> /2<br>– 50 |                             | t <sub>KCY2</sub> /2<br>– 50 | ns                          |      |
|   |  | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup>  | t <sub>KCY2</sub> /2<br>– 50       |                             | t <sub>KCY2</sub> /2<br>– 50 |                             | t <sub>KCY2</sub> /2<br>– 50 | ns                          |      |
| Slp setup time (to SCKp↑) <sup>Note 6</sup>           | t <sub>SIK2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V  | 1/f <sub>MCK</sub><br>+ 20         |                             | 1/f <sub>MCK</sub><br>+ 30   |                             | 1/f <sub>MCK</sub><br>+ 30   | ns                          |      |
|   |  | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup>  | 1/f <sub>MCK</sub><br>+ 30         |                             | 1/f <sub>MCK</sub><br>+ 30   |                             | 1/f <sub>MCK</sub><br>+ 30   | ns                          |      |
| Slp hold time (from SCKp↑) <sup>Note 6</sup>          | t <sub>SI2</sub>                       |  | 1/f <sub>MCK</sub><br>+ 31         |                             | 1/f <sub>MCK</sub><br>+ 31   |                             | 1/f <sub>MCK</sub><br>+ 31   | ns                          |      |
| Delay time from SCKp↓ to SOp output <sup>Note 7</sup> | t <sub>KSO2</sub>                      | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ                    |                                    | 2/f <sub>MCK</sub><br>+ 214 |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |
|   |  | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ |                                    | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**5.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

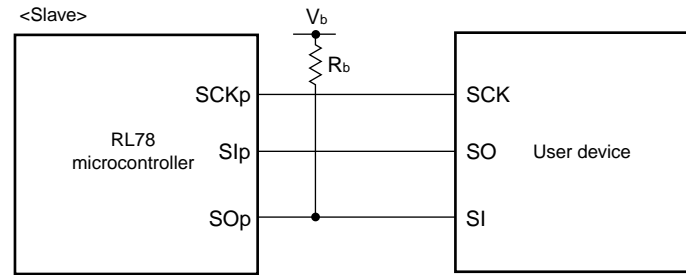
**6.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time or Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**7.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**Caution** Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

<R>

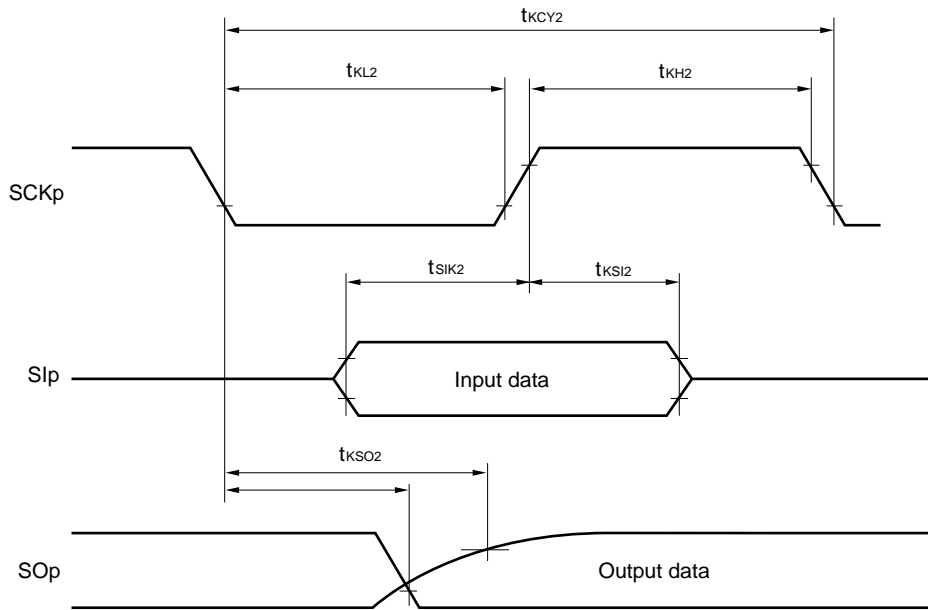
(Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

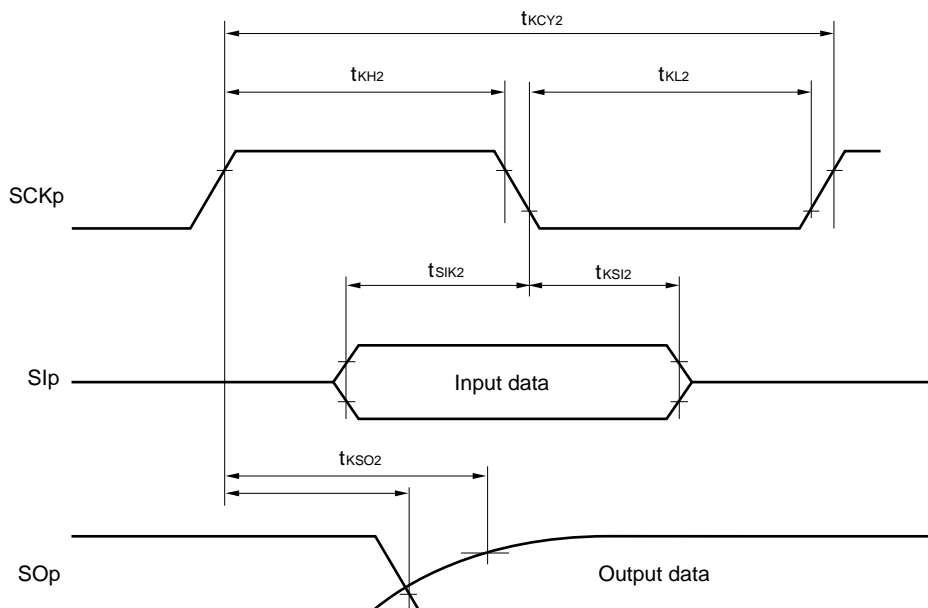
- Remarks**
1.  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  3.  $f_{\text{mck}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 02, 10))
  4. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.



**CSI mode serial transfer timing (slave mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
- 2.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode) (1/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

| Parameter                 | Symbol            | Conditions   | HS <sup>Note 1</sup> |                        | LS <sup>Note 2</sup> |                       | LV <sup>Note 3</sup> |                       | Unit |
|---------------------------|-------------------|--|----------------------|------------------------|----------------------|-----------------------|----------------------|-----------------------|------|
|                           |                   |  | MIN.                 | MAX.                   | MIN.                 | MAX.                  | MIN.                 | MAX.                  |      |
| SCLr clock frequency      | f <sub>SCL</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     |                      | 1000 <sup>Note 4</sup> |                      | 300 <sup>Note 4</sup> |                      | 300 <sup>Note 4</sup> | kHz  |
|                           |                   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    |                      | 400 <sup>Note 4</sup>  |                      | 300 <sup>Note 4</sup> |                      | 300 <sup>Note 4</sup> | kHz  |
|                           |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ |                      | 300 <sup>Note 4</sup>  |                      | 300 <sup>Note 4</sup> |                      | 300 <sup>Note 4</sup> | kHz  |
| Hold time when SCLr = "L" | t <sub>LOW</sub>  | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 475                  |                        | 1550                 |                       | 1550                 |                       | ns   |
|                           |                   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 1150                 |                        | 1550                 |                       | 1550                 |                       | ns   |
|                           |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 1550                 |                        | 1550                 |                       | 1550                 |                       | ns   |
| Hold time when SCLr = "H" | t <sub>HIGH</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 200                  |                        | 610                  |                       | 610                  |                       | ns   |
|                           |                   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 600                  |                        | 610                  |                       | 610                  |                       | ns   |
|                           |                   | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 610                  |                        | 610                  |                       | 610                  |                       | ns   |

(Notes, Caution and Remarks are listed on the next page.)

**(10) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

| Parameter                     | Symbol              | Conditions   | HS <sup>Note 1</sup>                          |      | LS <sup>Note 2</sup>                          |      | LV <sup>Note 3</sup>                          |      | Unit |
|-------------------------------|---------------------|--|---|------|---|------|---|------|------|
|                               |                     |  | MIN.  | MAX. | MIN.  | MAX. | MIN.  | MAX. |      |
| Data setup time (reception)   | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 1/f <sub>MCK</sub> +<br>135 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | ns   |
|                               |                     | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | ns   |
|                               |                     | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | 1/f <sub>MCK</sub> +<br>190 <sup>Note 6</sup> |      | ns   |
| Data hold time (transmission) | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 0   | 305  | 0   | 305  | 0   | 305  | ns   |
|                               |                     | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 0   | 355  | 0   | 355  | 0   | 355  | ns   |
|                               |                     | 1.8 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 0   | 405  | 0   | 405  | 0   | 405  | ns   |

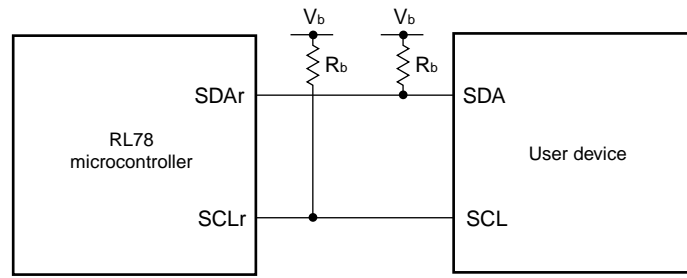
- Notes 1.** HS is condition of HS (high-speed main) mode.  
**2.** LS is condition of LS (low-speed main) mode.  
**3.** LV is condition of LV (low-voltage main) mode.  
**4.** The value must also be f<sub>CLK</sub>/4 or lower.  
**5.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.  
**6.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

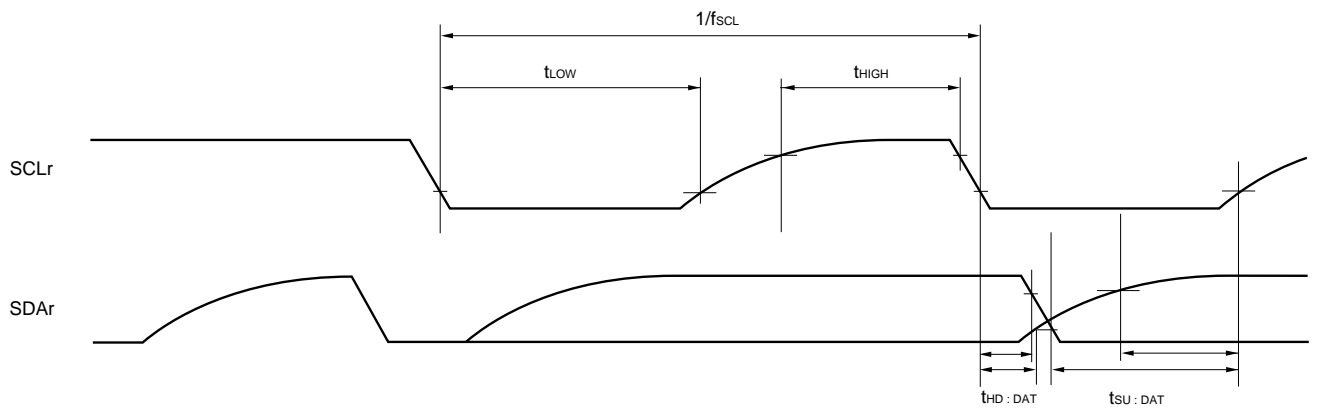
&lt;R&gt;

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**



- Remarks**
1. R<sub>b</sub>[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)
  3. f<sub>mcK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))
  4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

## 2.5.2 Serial interface IICA

(1) I<sup>2</sup>C standard mode(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                                       | Symbol              | Conditions                        | Standard Mode <sup>Note 1</sup> |      |                      |      |                      |      | Unit |
|---|---------------------|-----------------------------------|---------------------------------|------|----------------------|------|----------------------|------|------|
|   |                     |                                   | HS <sup>Note 2</sup>            |      | LS <sup>Note 3</sup> |      | LV <sup>Note 4</sup> |      |      |
|   |                     |                                   | MIN.                            | MAX. | MIN.                 | MIN. | MAX.                 | MIN. |      |
| SCLA0 clock frequency                           | f <sub>SCL</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 100  | 0                    | 100  | 0                    | 100  | kHz  |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 100  | 0                    | 100  | 0                    | 100  |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 100  | 0                    | 100  | 0                    | 100  |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 0                    | 100  | 0                    | 100  |      |
| Setup time of restart condition                 | t <sub>SU:STA</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.7                  |      | 4.7                  |      |      |
| Hold time <sup>Note 5</sup>                     | t <sub>HD:STA</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.0                  |      | 4.0                  |      |      |
| Hold time when SCLA0 = "L"                      | t <sub>LOW</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.7                  |      | 4.7                  |      |      |
| Hold time when SCLA0 = "H"                      | t <sub>HIGH</sub>   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.0                  |      | 4.0                  |      |      |
| Data setup time (reception)                     | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 250                             |      | 250                  |      | 250                  |      | ns   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 250                             |      | 250                  |      | 250                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 250                             |      | 250                  |      | 250                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 250                  |      | 250                  |      |      |
| Data hold time (transmission) <sup>Note 6</sup> | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 3.45 | 0                    | 3.45 | 0                    | 3.45 | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 3.45 | 0                    | 3.45 | 0                    | 3.45 |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                               | 3.45 | 0                    | 3.45 | 0                    | 3.45 |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               | –    | 0                    | 3.45 | 0                    | 3.45 |      |
| Setup time of stop condition                    | t <sub>SU:STO</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.0                             |      | 4.0                  |      | 4.0                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.0                  |      | 4.0                  |      |      |
| Bus-free time                                   | t <sub>BUF</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 4.7                             |      | 4.7                  |      | 4.7                  |      |      |
|   |                     | 1.6 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | –                               |      | 4.7                  |      | 4.7                  |      |      |

(Note and Remark are listed on the next page.)

(2) I<sup>2</sup>C fast mode, fast mode plus(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter                                       | Symbol              | Conditions                        | Fast Mode <sup>Note 7</sup> |      |                      |      |                      |      | Fast Mode Plus <sup>Note 8</sup> |      | Unit |
|---|---------------------|-----------------------------------|-----------------------------|------|----------------------|------|----------------------|------|----------------------------------|------|------|
|   |                     |                                   | HS <sup>Note 2</sup>        |      | LS <sup>Note 3</sup> |      | LV <sup>Note 4</sup> |      | HS <sup>Note 2</sup>             |      |      |
|   |                     |                                   | MIN.                        | MAX. | MIN.                 | MIN. | MAX.                 | MIN. | MAX.                             | MIN. |      |
| SCLA0 clock frequency                           | f <sub>SCL</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                           | 400  | 0                    | 400  | 0                    | 400  | 0                                | 1000 | kHz  |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                           | 400  | 0                    | 400  | 0                    | 400  | –                                |      |      |
| Setup time of restart condition                 | t <sub>SU:STA</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | 0.26                             |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | –                                |      |      |
| Hold time <sup>Note 5</sup>                     | t <sub>HD:STA</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | 0.26                             |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | –                                |      |      |
| Hold time when SCLA0 = "L"                      | t <sub>LOW</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 1.3                         |      | 1.3                  |      | 1.3                  |      | 0.5                              |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 1.3                         |      | 1.3                  |      | 1.3                  |      | –                                |      |      |
| Hold time when SCLA0 = "H"                      | t <sub>HIGH</sub>   | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | 0.26                             |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | –                                |      |      |
| Data setup time (reception)                     | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 100                         |      | 100                  |      | 100                  |      | 50                               |      | ns   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 100                         |      | 100                  |      | 100                  |      | –                                |      |      |
| Data hold time (transmission) <sup>Note 6</sup> | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                           | 0.9  | 0                    | 0.9  | 0                    | 0.9  | 0                                | 450  | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0                           | 0.9  | 0                    | 0.9  | 0                    | 0.9  | –                                |      |      |
| Setup time of stop condition                    | t <sub>SU:STO</sub> | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | 0.26                             |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 0.6                         |      | 0.6                  |      | 0.6                  |      | –                                |      |      |
| Bus-free time                                   | t <sub>BUF</sub>    | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 1.3                         |      | 1.3                  |      | 1.3                  |      | 0.5                              |      | μs   |
|   |                     | 1.8 V ≤ EV <sub>DD0</sub> ≤ 3.6 V | 1.3                         |      | 1.3                  |      | 1.3                  |      | –                                |      |      |

- Notes**
- In normal mode, use it with f<sub>CLK</sub> ≥ 1 MHz, 1.6 V ≤ EV<sub>DD</sub> ≤ 3.6 V.
  - HS is condition of HS (high-speed main) mode.
  - LS is condition of LS (low-speed main) mode.
  - LV is condition of LV (low-voltage main) mode.
  - The first clock pulse is generated after this period when the start/restart condition is detected.
  - The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
  - In fast mode, use it with f<sub>CLK</sub> ≥ 3.5 MHz, 1.8 V ≤ EV<sub>DD</sub> ≤ 3.6 V.
  - In fast mode plus, use it with f<sub>CLK</sub> ≥ 10 MHz, 2.7 V ≤ EV<sub>DD</sub> ≤ 3.6 V.

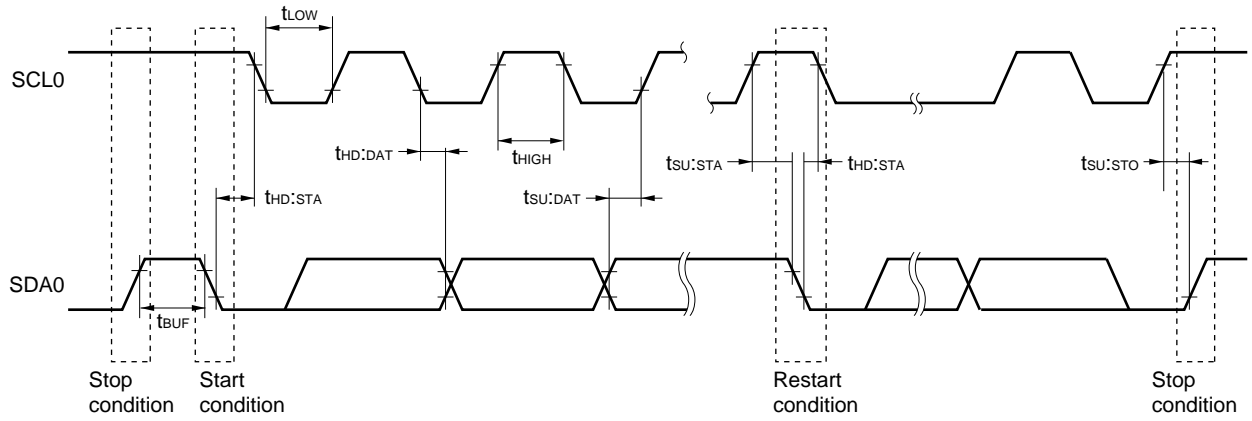
**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

IICA serial transfer timing



## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Division of A/D Converter Characteristics**

| Reference voltage<br>Input channel   | Reference voltage (+) = AV <sub>REFP</sub><br>Reference voltage (-) = AV <sub>REFM</sub> | Reference voltage (+) = AV <sub>DD</sub><br>Reference voltage (-) = AV <sub>SS</sub> | Reference voltage (+) = Internal<br>reference voltage<br>Reference voltage (-) = AV <sub>SS</sub> |
|--|--|--|---|
| High-accuracy channel; ANI0 to ANI12<br>(input buffer power supply: AV <sub>DD</sub> )                 | See 2.6.1 (1)<br>See 2.6.1 (2)   | See 2.6.1 (3)  | See 2.6.1 (6)   |
| Standard channel; ANI16 to ANI30<br>(input buffer power supply: V <sub>DD</sub> or EV <sub>DD0</sub> ) | See 2.6.1 (4)  | See 2.6.1 (5)  |   |
| Temperature sensor, internal<br>reference voltage output   | See 2.6.1 (4)  | See 2.6.1 (5)  | –   |

<R> (1) When reference voltage (+) = AV<sub>REFP</sub>/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV<sub>REFM</sub>/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

<R> (T<sub>A</sub> = -40 to +85°C, 2.4 V ≤ AV<sub>REFP</sub> ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>REFP</sub>, Reference voltage (-) = AV<sub>REFM</sub> = 0 V, HALT mode)

| Parameter   | Symbol            | Conditions                   | MIN.  | TYP. | MAX.               | Unit |
|---|-------------------|------------------------------|-------|------|--------------------|------|
| Resolution  | R <sub>ES</sub>   |                              |       |      | 12                 | bit  |
| Overall error <sup>Notes 1, 2, 3</sup>                | A <sub>INL</sub>  | 12-bit resolution            |       | ±1.7 | ±3.3               | LSB  |
| Conversion time                                       | t <sub>CONV</sub> | ADTYP = 0, 12-bit resolution | 3.375 |      |                    | μs   |
| Zero-scale error <sup>Notes 1, 2, 3</sup>             | E <sub>ZS</sub>   | 12-bit resolution            |       | ±1.3 | ±3.2               | LSB  |
| Full-scale error <sup>Notes 1, 2, 3</sup>             | E <sub>FS</sub>   | 12-bit resolution            |       | ±0.7 | ±2.9               | LSB  |
| Integral linearity error <sup>Notes 1, 2, 3</sup>     | I <sub>LE</sub>   | 12-bit resolution            |       | ±1.0 | ±1.4               | LSB  |
| Differential linearity error <sup>Notes 1, 2, 3</sup> | D <sub>LE</sub>   | 12-bit resolution            |       | ±0.9 | ±1.2               | LSB  |
| Analog input voltage                                  | V <sub>AIN</sub>  |                              | 0     |      | AV <sub>REFP</sub> | V    |

**Notes** 1. TYP. Value is the average value at AV<sub>DD</sub> = AV<sub>REFP</sub> = 3 V and T<sub>A</sub> = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

**Cautions** 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV<sub>REFP</sub> from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.



<R> (2) When reference voltage (+) = AV<sub>REFP</sub>/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV<sub>REFM</sub>/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>REFP</sub> ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>REFP</sub>, Reference voltage (-) = AV<sub>REFM</sub> = 0 V)

| Parameter                                      | Symbol            | Conditions  | MIN.  | TYP.   | MAX.                 | Unit |
|--|-------------------|---|---|--------|----------------------|------|
| Resolution                                     | RES               | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 8   |        | 12                   | bit  |
|  |                   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 8   |        | 10 <sup>Note 1</sup> |      |
|  |                   | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | g <sup>Note 2</sup>                                   |        |                      |      |
| Overall error <sup>Note 3</sup>                | AINL              | 12-bit resolution                                     | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±6.0                 | LSB  |
|  |                   | 10-bit resolution                                     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0                 |      |
|  |                   | 8-bit resolution                                      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.5                 |      |
| Conversion time                                | t <sub>CONV</sub> | ADTYP = 0,<br>12-bit resolution                       | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 3.375  |                      | μs   |
|  |                   | ADTYP = 0,<br>10-bit resolution <sup>Note 1</sup>     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 6.75   |                      |      |
|  |                   | ADTYP = 0,<br>8-bit resolution <sup>Note 2</sup>      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 13.5   |                      |      |
|  |                   | ADTYP = 1,<br>8-bit resolution                        | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 2.5625 |                      |      |
|  |                   |   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 5.125  |                      |      |
|  |                   |   | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 10.25  |                      |      |
| Zero-scale error <sup>Note 3</sup>             | E <sub>ZS</sub>   | 12-bit resolution                                     | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±4.5                 | LSB  |
|  |                   | 10-bit resolution                                     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±4.5                 |      |
|  |                   | 8-bit resolution                                      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 |      |
| Full-scale error <sup>Note 3</sup>             | E <sub>FS</sub>   | 12-bit resolution                                     | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±4.5                 | LSB  |
|  |                   | 10-bit resolution                                     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±4.5                 |      |
|  |                   | 8-bit resolution                                      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 |      |
| Integral linearity error <sup>Note 3</sup>     | ILE               | 12-bit resolution                                     | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 | LSB  |
|  |                   | 10-bit resolution                                     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5                 |      |
|  |                   | 8-bit resolution                                      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.0                 |      |
| Differential linearity error <sup>Note 3</sup> | DLE               | 12-bit resolution                                     | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5                 | LSB  |
|  |                   | 10-bit resolution                                     | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5                 |      |
|  |                   | 8-bit resolution                                      | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.0                 |      |
| Analog input voltage                           | V <sub>AIN</sub>  |   | 0   |        | AV <sub>REFP</sub>   | V    |

- Notes 1.** Cannot be used for lower 2 bit of ADCR register  
**2.** Cannot be used for lower 4 bit of ADCR register  
**3.** Excludes quantization error (±1/2 LSB).

<R> (3) When reference voltage (+) = AV<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), target for conversion: ANI0 to ANI12

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>DD</sub>, Reference voltage (-) = AV<sub>SS</sub> = 0 V)

| Parameter                                      | Symbol            | Conditions  | MIN.                             | TYP.   | MAX.                 | Unit |
|--|-------------------|---|----------------------------------|--------|----------------------|------|
| Resolution                                     | R <sub>ES</sub>   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V                  | 8                                |        | 12                   | bit  |
|  |                   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V                  | 8                                |        | 10 <sup>Note 1</sup> |      |
|  |                   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V                  | 8 <sup>Note 2</sup>              |        |                      |      |
| Overall error <sup>Note 3</sup>                | AINL              | 12-bit resolution                                 | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±7.5                 | LSB  |
|  |                   | 10-bit resolution                                 | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.5                 |      |
|  |                   | 8-bit resolution                                  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±3.0                 |      |
| Conversion time                                | t <sub>CONV</sub> | ADTYP = 0,<br>12-bit resolution                   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V | 3.375  |                      | μs   |
|  |                   | ADTYP = 0,<br>10-bit resolution <sup>Note 1</sup> | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V | 6.75   |                      |      |
|  |                   | ADTYP = 0,<br>8-bit resolution <sup>Note 2</sup>  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V | 13.5   |                      |      |
|  |                   | ADTYP = 1,<br>8-bit resolution                    | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V | 2.5625 |                      |      |
|  |                   |   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V | 5.125  |                      |      |
| 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V               | 10.25             |   |                                  |        |                      |      |
| Zero-scale error <sup>Note 3</sup>             | E <sub>ZS</sub>   | 12-bit resolution                                 | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±6.0                 | LSB  |
|  |                   | 10-bit resolution                                 | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0                 |      |
|  |                   | 8-bit resolution                                  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.5                 |      |
| Full-scale error <sup>Note 3</sup>             | E <sub>FS</sub>   | 12-bit resolution                                 | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±6.0                 | LSB  |
|  |                   | 10-bit resolution                                 | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0                 |      |
|  |                   | 8-bit resolution                                  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.5                 |      |
| Integral linearity error <sup>Note 3</sup>     | ILE               | 12-bit resolution                                 | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±3.0                 | LSB  |
|  |                   | 10-bit resolution                                 | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 |      |
|  |                   | 8-bit resolution                                  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5                 |      |
| Differential linearity error <sup>Note 3</sup> | DLE               | 12-bit resolution                                 | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 | LSB  |
|  |                   | 10-bit resolution                                 | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0                 |      |
|  |                   | 8-bit resolution                                  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5                 |      |
| <R> Analog input voltage                       | V <sub>AIN</sub>  |   | 0                                |        | AV <sub>DD</sub>     | V    |

**Notes 1.** Cannot be used for lower 2 bit of ADCR register

**2.** Cannot be used for lower 4 bit of ADCR register

**3.** Excludes quantization error (±1/2 LSB).

<R> (4) When reference voltage (+) = AV<sub>REFP</sub>/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV<sub>REFM</sub>/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, internal reference voltage, temperature sensor output voltage

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ AV<sub>REFP</sub> ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>REFP</sub>, Reference voltage (-) = AV<sub>REFM</sub> = 0 V)

| Parameter                                      | Symbol            | Conditions  | MIN.  | TYP.   | MAX.  | Unit |   |
|--|-------------------|---|---|--------|---|------|---|
| Resolution                                     | RES               | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V   | 8   |        | 12  | bit  |   |
|  |                   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V   | 8   |        | 10 <sup>Note 1</sup>                        |      |   |
|  |                   | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V   | g <sup>Note 2</sup>                                   |        |   |      |   |
| Overall error <sup>Note 3</sup>                | AINL              | 12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±7.0  | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.5  |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±3.0  |      |   |
| Conversion time                                | t <sub>CONV</sub> | ADTYP = 0,<br>12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 4.125  |   | μs   |   |
|  |                   | ADTYP = 0,<br>10-bit resolution <sup>Note 1</sup>   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 9.5    |   |      |   |
|  |                   | ADTYP = 0,<br>8-bit resolution <sup>Note 2</sup>  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 57.5   |   |      |   |
|  |                   | ADTYP = 1,<br>8-bit resolution  | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 3.3125 |   |      |   |
|  |                   |   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 7.875  |   |      |   |
|  |                   |   | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V | 54.25  |   |      |   |
| Zero-scale error <sup>Note 3</sup>             | E <sub>ZS</sub>   | 12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0  | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0  |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.5  |      |   |
| Full-scale error <sup>Note 3</sup>             | E <sub>FS</sub>   | 12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0  | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±5.0  |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.5  |      |   |
| Integral linearity error <sup>Note 3</sup>     | ILE               | 12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±3.0  | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0  |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5  |      |   |
| Differential linearity error <sup>Note 3</sup> | DLE               | 12-bit resolution   | 2.4 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0  | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±2.0  |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>REFP</sub> ≤ AV <sub>DD</sub> ≤ 3.6 V |        | ±1.5  |      |   |
| Analog input voltage                           | V <sub>AIN</sub>  |   | 0   |        | AV <sub>REFP</sub><br>and EV <sub>DD0</sub> | V    |   |
|  |                   | Internal reference voltage<br>(2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, HS (high-speed main) mode)        | V <sub>BGR</sub> <sup>Note 4</sup>                    |        |   |      | V |
|  |                   | Temperature sensor output voltage<br>(2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, HS (high-speed main) mode) | V <sub>TMPS25</sub> <sup>Note 4</sup>                 |        |   |      | V |

- Notes 1.** Cannot be used for lower 2 bit of ADCR register  
**2.** Cannot be used for lower 4 bit of ADCR register  
**3.** Excludes quantization error (±1/2 LSB).  
**4.** See 2.6.2 Temperature sensor, internal reference voltage output characteristics.

<R> (5) When reference voltage (+) = AV<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), target for conversion: ANI16 to ANI30, internal reference voltage, temperature sensor output voltage

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD0</sub> ≤ 3.6 V, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>DD</sub>, Reference voltage (-) = AV<sub>SS</sub> = 0 V)

| Parameter                                      | Symbol            | Conditions  | MIN.                                  | TYP.   | MAX.                                   | Unit |   |
|--|-------------------|---|---------------------------------------|--------|--|------|---|
| Resolution                                     | R <sub>ES</sub>   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V  | 8                                     |        | 12                                     | bit  |   |
|  |                   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V  | 8                                     |        | 10 <sup>Note 1</sup>                   |      |   |
|  |                   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V  | 8 <sup>Note 2</sup>                   |        |  |      |   |
| Overall error <sup>Note 3</sup>                | AINL              | 12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±8.5                                   | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±6.0                                   |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±3.5                                   |      |   |
| Conversion time                                | t <sub>CONV</sub> | ADTYP = 0,<br>12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 4.125  |  | μs   |   |
|  |                   |   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 9.5    |  |      |   |
|  |                   |   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 57.5   |  |      |   |
|  |                   | ADTYP = 1,<br>8-bit resolution  | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 3.3125 |  | μs   |   |
|  |                   |   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 7.875  |  |      |   |
|  |                   |   | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      | 54.25  |  |      |   |
| Zero-scale error <sup>Note 3</sup>             | E <sub>ZS</sub>   | 12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±8.0                                   | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±5.5                                   |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±3.0                                   |      |   |
| Full-scale error <sup>Note 3</sup>             | E <sub>FS</sub>   | 12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±8.0                                   | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±5.5                                   |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±3.0                                   |      |   |
| Integral linearity error <sup>Note 3</sup>     | ILE               | 12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±3.5                                   | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±2.5                                   |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±1.5                                   |      |   |
| Differential linearity error <sup>Note 3</sup> | DLE               | 12-bit resolution   | 2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±2.5                                   | LSB  |   |
|  |                   | 10-bit resolution   | 1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±2.5                                   |      |   |
|  |                   | 8-bit resolution  | 1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V      |        | ±2.0                                   |      |   |
| Analog input voltage                           | V <sub>AIN</sub>  |   | 0                                     |        | AV <sub>DD</sub> and EV <sub>DD0</sub> | V    |   |
|  |                   | Interanal reference voltage<br>(2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, HS (high-speed main) mode)       | V <sub>BGR</sub> <sup>Note 4</sup>    |        |  |      | V |
|  |                   | Temperature sensor output voltage<br>(2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, HS (high-speed main) mode) | V <sub>TMPS25</sub> <sup>Note 4</sup> |        |  |      | V |

- Notes**
- Cannot be used for lower 2 bit of ADCR register
  - Cannot be used for lower 4 bit of ADCR register
  - Excludes quantization error (±1/2 LSB).
  - See 2.6.2 Temperature sensor, internal reference voltage output characteristics.

<R> (6) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), target ANI pin: ANI0 to ANI12, ANI16 to ANI30

(T<sub>A</sub> = -40 to +85°C, 2.4 V ≤ V<sub>DD</sub> ≤ 3.6 V, 1.6 V ≤ EV<sub>DD</sub> ≤ V<sub>DD</sub>, 1.6 V ≤ AV<sub>DD</sub> ≤ V<sub>DD</sub>, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (-) = AV<sub>SS</sub> = 0 V, HS (high-speed main mode)

| Parameter                                    | Symbol               | Conditions                                       | MIN. | TYP. | MAX.             | Unit |
|--|----------------------|--|------|------|------------------|------|
| Resolution                                   | R <sub>ES</sub>      |  | 8    |      |                  | bit  |
| Conversion time                              | t <sub>CONV</sub>    | 8-bit resolution                                 | 16   |      |                  | μs   |
| Zero-scale error <sup>Note</sup>             | E <sub>ZS</sub>      | 8-bit resolution                                 |      |      | ±4.0             | LSB  |
| Integral linearity error <sup>Note</sup>     | ILE                  | 8-bit resolution                                 |      |      | ±2.0             | LSB  |
| Differential linearity error <sup>Note</sup> | DLE                  | 8-bit resolution                                 |      |      | ±2.5             | LSB  |
| Reference voltage (+)                        | AV <sub>REF(+)</sub> | = Internal reference voltage (V <sub>BGR</sub> ) | 1.38 | 1.45 | 1.5              | V    |
| Analog input voltage                         | V <sub>AIN</sub>     |  | 0    |      | V <sub>BGR</sub> | V    |

**Note** Excludes quantization error (±1/2 LSB).

### 2.6.2 Temperature sensor, internal reference voltage output characteristics

(T<sub>A</sub> = -40 to +85°C, 2.4 V ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, HS (high-speed main) mode)

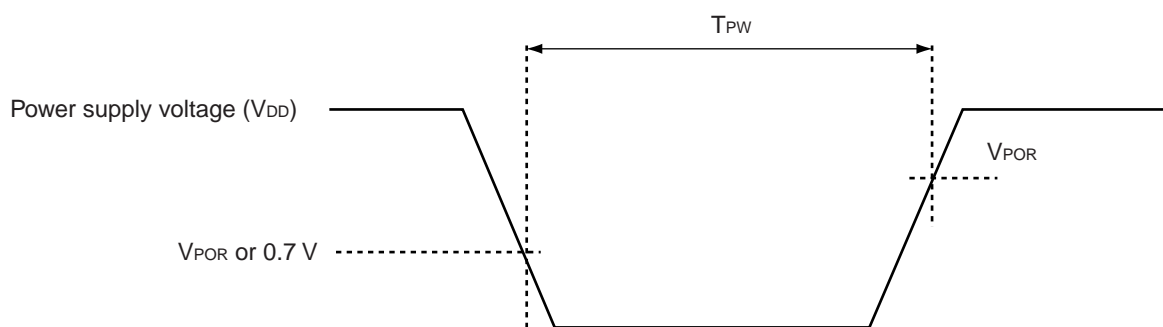
| Parameter                         | Symbol              | Conditions  | MIN. | TYP. | MAX. | Unit  |
|-----------------------------------|---------------------|---|------|------|------|-------|
| Temperature sensor output voltage | V <sub>TMP525</sub> | Setting ADS register = 80H, T <sub>A</sub> = +25°C                |      | 1.05 |      | V     |
| Internal reference voltage        | V <sub>BGR</sub>    | Setting ADS register = 81H  | 1.38 | 1.45 | 1.5  | V     |
| Temperature coefficient           | F <sub>VTMP5</sub>  | Temperature sensor output voltage that depends on the temperature |      | -3.6 |      | mV/°C |
| Operation stabilization wait time | t <sub>AMP</sub>    |   | 10   |      |      | μs    |

### 2.6.3 POR circuit characteristics

(T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V)

| Parameter                           | Symbol           | Conditions             | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|------------------|------------------------|------|------|------|------|
| Detection voltage                   | V <sub>POR</sub> | Power supply rise time | 1.47 | 1.51 | 1.55 | V    |
|                                     | V <sub>PDR</sub> | Power supply fall time | 1.46 | 1.50 | 1.54 | V    |
| Minimum pulse width <sup>Note</sup> | T <sub>PW</sub>  |                        | 300  |      |      | μs   |

**Note** This is the time required for the POR circuit to execute a reset when V<sub>DD</sub> falls below V<sub>PDR</sub>. When the microcontroller enters STOP mode or if the main system clock (f<sub>MAIN</sub>) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V<sub>DD</sub> rises to V<sub>POR</sub> after having fallen below 0.7 V.



## 2.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode****(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V)**

| Parameter            |                      | Symbol             | Conditions             | MIN. | TYP. | MAX. | Unit |
|----------------------|----------------------|--------------------|------------------------|------|------|------|------|
| Detection voltage    | Supply voltage level | V <sub>LVD2</sub>  | Power supply rise time | 3.07 | 3.13 | 3.19 | V    |
|                      |                      |                    | Power supply fall time | 3.00 | 3.06 | 3.12 | V    |
|                      |                      | V <sub>LVD3</sub>  | Power supply rise time | 2.96 | 3.02 | 3.08 | V    |
|                      |                      |                    | Power supply fall time | 2.90 | 2.96 | 3.02 | V    |
|                      |                      | V <sub>LVD4</sub>  | Power supply rise time | 2.86 | 2.92 | 2.97 | V    |
|                      |                      |                    | Power supply fall time | 2.80 | 2.86 | 2.91 | V    |
|                      |                      | V <sub>LVD5</sub>  | Power supply rise time | 2.76 | 2.81 | 2.87 | V    |
|                      |                      |                    | Power supply fall time | 2.70 | 2.75 | 2.81 | V    |
|                      |                      | V <sub>LVD6</sub>  | Power supply rise time | 2.66 | 2.71 | 2.76 | V    |
|                      |                      |                    | Power supply fall time | 2.60 | 2.65 | 2.70 | V    |
|                      |                      | V <sub>LVD7</sub>  | Power supply rise time | 2.56 | 2.61 | 2.66 | V    |
|                      |                      |                    | Power supply fall time | 2.50 | 2.55 | 2.60 | V    |
|                      |                      | V <sub>LVD8</sub>  | Power supply rise time | 2.45 | 2.50 | 2.55 | V    |
|                      |                      |                    | Power supply fall time | 2.40 | 2.45 | 2.50 | V    |
|                      |                      | V <sub>LVD9</sub>  | Power supply rise time | 2.05 | 2.09 | 2.13 | V    |
|                      |                      |                    | Power supply fall time | 2.00 | 2.04 | 2.08 | V    |
|                      |                      | V <sub>LVD10</sub> | Power supply rise time | 1.94 | 1.98 | 2.02 | V    |
|                      |                      |                    | Power supply fall time | 1.90 | 1.94 | 1.98 | V    |
|                      |                      | V <sub>LVD11</sub> | Power supply rise time | 1.84 | 1.88 | 1.91 | V    |
|                      |                      |                    | Power supply fall time | 1.80 | 1.84 | 1.87 | V    |
|                      |                      | V <sub>LVD12</sub> | Power supply rise time | 1.74 | 1.77 | 1.81 | V    |
|                      |                      |                    | Power supply fall time | 1.70 | 1.73 | 1.77 | V    |
|                      |                      | V <sub>LVD13</sub> | Power supply rise time | 1.64 | 1.67 | 1.70 | V    |
|                      |                      |                    | Power supply fall time | 1.60 | 1.63 | 1.66 | V    |
| Minimum pulse width  |                      | t <sub>LW</sub>    |                        | 300  |      |      | μs   |
| Detection delay time |                      |                    |                        |      |      | 300  | μs   |

**Caution** Set the detection voltage (V<sub>LVD</sub>) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

**HS (high-speed main) mode:** V<sub>DD</sub> = 2.7 to 3.6 V@1 MHz to 32 MHz

V<sub>DD</sub> = 2.4 to 3.6 V@1 MHz to 16 MHz

**LS (low-speed main) mode:** V<sub>DD</sub> = 1.8 to 3.6 V@1 MHz to 8 MHz

**LV (low-voltage main) mode:** V<sub>DD</sub> = 1.6 to 3.6 V@1 MHz to 4 MHz

**LVD Detection Voltage of Interrupt & Reset Mode**(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V)

| Parameter              | Symbol              | Conditions   | MIN.                         | TYP. | MAX. | Unit |   |
|------------------------|---------------------|--|------------------------------|------|------|------|---|
| Interrupt & reset mode | V <sub>LVD13</sub>  | VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage | 1.60                         | 1.63 | 1.66 | V    |   |
|                        | V <sub>LVD12</sub>  | LVIS1, LVIS0 = 1, 0                                  | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
|                        |                     |  | Falling interrupt voltage    | 1.70 | 1.73 | 1.77 | V |
|                        | V <sub>LVD11</sub>  | LVIS1, LVIS0 = 0, 1                                  | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
|                        |                     |  | Falling interrupt voltage    | 1.80 | 1.84 | 1.87 | V |
|                        | V <sub>LVD4</sub>   | LVIS1, LVIS0 = 0, 0                                  | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
|                        |                     |  | Falling interrupt voltage    | 2.80 | 2.86 | 2.91 | V |
|                        | V <sub>LVD11</sub>  | VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage | 1.80                         | 1.84 | 1.87 | V    |   |
|                        | V <sub>LVD10</sub>  | LVIS1, LVIS0 = 1, 0                                  | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
|                        |                     |  | Falling interrupt voltage    | 1.90 | 1.94 | 1.98 | V |
|                        | V <sub>LVD9</sub>   | LVIS1, LVIS0 = 0, 1                                  | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
|                        |                     |  | Falling interrupt voltage    | 2.00 | 2.04 | 2.08 | V |
|                        | V <sub>LVD2</sub>   | LVIS1, LVIS0 = 0, 0                                  | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
|                        |                     |  | Falling interrupt voltage    | 3.00 | 3.06 | 3.12 | V |
|                        | V <sub>LVD8</sub>   | VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage | 2.40                         | 2.45 | 2.50 | V    |   |
|                        | V <sub>LVD7</sub>   | LVIS1, LVIS0 = 1, 0                                  | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
|                        |                     |  | Falling interrupt voltage    | 2.50 | 2.55 | 2.60 | V |
|                        | V <sub>LVD6</sub>   | LVIS1, LVIS0 = 0, 1                                  | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
|                        |                     |  | Falling interrupt voltage    | 2.60 | 2.65 | 2.70 | V |
|                        | V <sub>LVD5</sub>   | VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage | 2.70                         | 2.75 | 2.81 | V    |   |
| V <sub>LVD4</sub>      | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage                         | 2.86                         | 2.92 | 2.97 | V    |   |
|                        |                     | Falling interrupt voltage                            | 2.80                         | 2.86 | 2.91 | V    |   |
| V <sub>LVD3</sub>      | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage                         | 2.96                         | 3.02 | 3.08 | V    |   |
|                        |                     | Falling interrupt voltage                            | 2.90                         | 2.96 | 3.02 | V    |   |

**Caution** Set the detection voltage (V<sub>LVD</sub>) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

**HS (high-speed main) mode:** V<sub>DD</sub> = 2.7 to 3.6 V@1 MHz to 32 MHz

V<sub>DD</sub> = 2.4 to 3.6 V@1 MHz to 16 MHz

**LS (low-speed main) mode:** V<sub>DD</sub> = 1.8 to 3.6 V@1 MHz to 8 MHz

**LV (low-voltage main) mode:** V<sub>DD</sub> = 1.6 to 3.6 V@1 MHz to 4 MHz

## 2.6.5 Supply voltage rise slope characteristics

(T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V)

| Parameter           | Symbol           | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------|------------------|------------|------|------|------|------|
| Supply voltage rise | SV <sub>DD</sub> |            |      |      | 54   | V/ms |

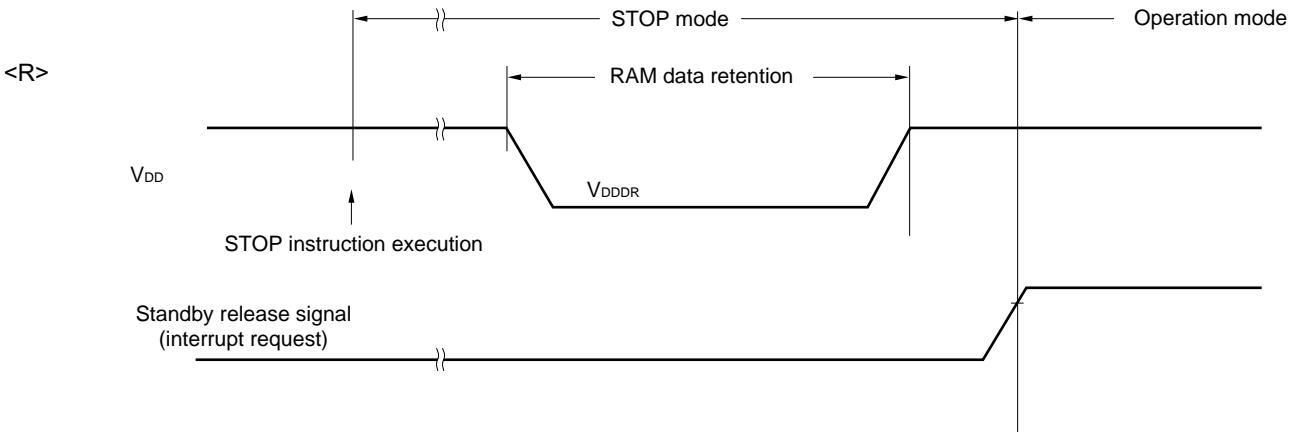
**Caution** Be sure to maintain the internal reset state until V<sub>DD</sub> reaches the operating voltage range specified in 2.4 AC Characteristics, by using the LVD circuit or external reset pin.

<R> 2.7 RAM Data Retention Characteristics

<R> (T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V)

| Parameter                     | Symbol            | Conditions | MIN.                 | TYP. | MAX. | Unit |
|-------------------------------|-------------------|------------|----------------------|------|------|------|
| Data retention supply voltage | V <sub>DDDR</sub> |            | 1.46 <sup>Note</sup> |      | 3.6  | V    |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



<R> 2.8 Flash Memory Programming Characteristics

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V)

| Parameter   | Symbol            | Conditions   | MIN.    | TYP.      | MAX. | Unit  |
|---|-------------------|--|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency             | f <sub>CLK</sub>  | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V                                  | 1       |           | 32   | MHz   |
| Number of code flash rewrites <sup>Notes 1, 2</sup> | C <sub>erwr</sub> | Retained for 20 years<br>T <sub>A</sub> = 85°C <sup>Note 3</sup> | 1,000   |           |      | Times |
| Number of data flash rewrites <sup>Notes 1, 2</sup> |                   | Retained for 1 years<br>T <sub>A</sub> = 25°C <sup>Note 3</sup>  |         | 1,000,000 |      |       |
|   |                   | Retained for 5 years<br>T <sub>A</sub> = 85°C <sup>Note 3</sup>  | 100,000 |           |      |       |
|   |                   | Retained for 20 years<br>T <sub>A</sub> = 85°C <sup>Note 3</sup> | 10,000  |           |      |       |

- Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.  
The retaining years are until next rewrite after the rewrite.
- 2.** When using flash memory programmer and Renesas Electronics self programming library
- 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.



### 2.9 Dedicated Flash Memory Programmer Communication (UART)

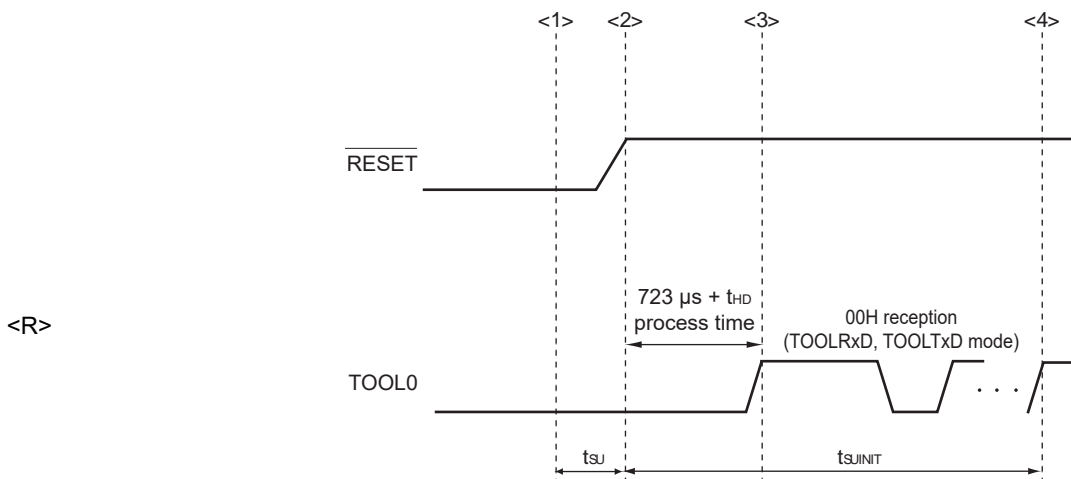
(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter     | Symbol | Conditions                      | MIN.    | TYP. | MAX. | Unit |
|---------------|--------|---------------------------------|---------|------|------|------|
| Transfer rate |        | During flash memory programming | 115.2 k |      | 1 M  | bps  |

### 2.10 Timing Specs for Switching Flash Memory Programming Modes

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Parameter   | Symbol              | Conditions   | MIN. | TYP. | MAX. | Unit |
|---|---------------------|--|------|------|------|------|
| How long from when an external reset ends until the initial communication settings are specified                              | t <sub>SUINIT</sub> | POR and LVD reset must end before the external reset ends. |      |      | 100  | ms   |
| How long from when the TOOL0 pin is placed at the low level until a external reset ends                                       | t <sub>SU</sub>     | POR and LVD reset must end before the external reset ends. | 10   |      |      | μs   |
| <R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time) | t <sub>HD</sub>     | POR and LVD reset must end before the external reset ends. | 1    |      |      | ms   |



- <1> The low level is input to the TOOL0 pin.
- <2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** t<sub>SUINIT</sub>: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t<sub>SU</sub>: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> t<sub>HD</sub>: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

### 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products G: Industrial applications  $T_A = -40$  to  $+105^\circ\text{C}$   
R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA  
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB  
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA  
R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

- Cautions**
1. The RL78/G1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $EV_{DD0}$  or  $EV_{SS0}$  pin, replace  $EV_{DD0}$  with  $V_{DD}$ , or replace  $EV_{SS0}$  with  $V_{SS}$ .
  3. Please contact Renesas Electronics sales office for derating of operation under  $T_A = +85^\circ\text{C}$  to  $+105^\circ\text{C}$ . Derating is the systematic reduction of load for the sake of improved reliability.

**Remark** When RL78/G1A is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$ , see 2. **ELECTRICAL SPECIFICATIONS** ( $T_A = -40$  to  $+85^\circ\text{C}$ ).

## 3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ ) (1/2)

| Parameter              | Symbols     | Conditions   | Ratings   | Unit |
|------------------------|-------------|--|---|------|
| Supply voltage         | $V_{DD}$    |  | -0.5 to +6.5  | V    |
|                        | $EV_{DD0}$  |  | -0.5 to +6.5  | V    |
|                        | $AV_{DD}$   |  | -0.5 to +4.6  | V    |
|                        | $AV_{REFP}$ |  | -0.3 to $AV_{DD} + 0.3$ <sup>Note 3</sup>   | V    |
|                        | $EV_{SS0}$  |  | -0.5 to +0.3  | V    |
|                        | $AV_{SS}$   |  | -0.5 to +0.3  | V    |
|                        | $AV_{REFM}$ |  | -0.3 to $AV_{DD} + 0.3$ <sup>Note 3</sup><br>and $AV_{REFM} \leq AV_{REFP}$       | V    |
| REGC pin input voltage | $V_{IREGC}$ | REGC   | -0.3 to +2.8<br>and -0.3 to $V_{DD} + 0.3$ <sup>Note 1</sup>                      | V    |
| Input voltage          | $V_{I1}$    | P00 to P06, P10 to P16, P30, P31, P40 to P43,<br>P50, P51, P70 to P77, P120, P140, P141                      | -0.3 to $EV_{DD0} + 0.3$<br>and -0.3 to $V_{DD} + 0.3$ <sup>Note 2</sup>          | V    |
|                        | $V_{I2}$    | P60 to P63 (N-ch open-drain)   | -0.3 to +6.5  | V    |
|                        | $V_{I3}$    | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$   | -0.3 to $V_{DD} + 0.3$ <sup>Note 2</sup>  | V    |
|                        | $V_{I4}$    | P20 to P27, P150 to P154   | -0.3 to $AV_{DD} + 0.3$ <sup>Note 2</sup>   | V    |
| Output voltage         | $V_{O1}$    | P00 to P06, P10 to P16, P30, P31, P40 to P43,<br>P50, P51, P60 to P63, P70 to P77, P120, P130,<br>P140, P141 | -0.3 to $EV_{DD0} + 0.3$ <sup>Note 2</sup>  | V    |
|                        | $V_{O2}$    | P20 to P27, P150 to P154   | -0.3 to $AV_{DD} + 0.3$ <sup>Note 2</sup>   | V    |
| Analog input voltage   | $V_{AI1}$   | ANI16 to ANI30   | -0.3 to $EV_{DD0} + 0.3$<br>and -0.3 to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 4</sup> | V    |
|                        | $V_{AI2}$   | ANI0 to ANI12  | -0.3 to $AV_{DD} + 0.3$<br>and -0.3 to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 4</sup>  | V    |

**Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu\text{F}$ ). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Must be 4.6 V or lower.

**4.** Do not exceed  $AV_{REF(+)} + 0.3$  V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.**  $AV_{REF(+)}$ : + side reference voltage of the A/D converter.

**3.**  $V_{SS}$ : Reference voltage

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ ) (2/2)**

| Parameter                        | Symbols                       | Conditions                   |  | Ratings     | Unit             |
|----------------------------------|-------------------------------|------------------------------|--|-------------|------------------|
| Output current, high             | $I_{OH1}$                     | Per pin                      | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141             | -40         | mA               |
|                                  |                               | Total of all pins<br>-170 mA | P00 to P04, P40 to P43, P120, P130, P140, P141   | -70         | mA               |
|                                  |                               |                              | P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,  | -100        | mA               |
|                                  | $I_{OH2}$                     | Per pin                      | P20 to P27, P150 to P154   | -0.1        | mA               |
|                                  |                               | Total of all pins            |  | -1.3        | mA               |
| Output current, low              | $I_{OL1}$                     | Per pin                      | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141 | 40          | mA               |
|                                  |                               | Total of all pins<br>170 mA  | P00 to P04, P40 to P43, P120, P130, P140, P141   | 70          | mA               |
|                                  |                               |                              | P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77                                       | 100         | mA               |
|                                  | $I_{OL2}$                     | Per pin                      | P20 to P27, P150 to P154   | 0.4         | mA               |
|                                  |                               | Total of all pins            |  | 6.4         | mA               |
|                                  | Operating ambient temperature | $T_A$                        | In normal operation mode   |             | -40 to +105      |
| In flash memory programming mode |                               |                              |  |             |                  |
| Storage temperature              | $T_{stg}$                     |                              |  | -65 to +150 | $^\circ\text{C}$ |

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Oscillator Characteristics

### 3.2.1 X1, XT1 oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter   | Resonator                           | Conditions                                   | MIN. | TYP.   | MAX. | Unit |
|---|-------------------------------------|--|------|--------|------|------|
| X1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>  | Ceramic resonator/crystal resonator | $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | 1.0  |        | 20.0 | MHz  |
|   |                                     | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 1.0  |        | 16.0 |      |
| XT1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup> | Crystal resonator                   |  | 32   | 32.768 | 35   | kHz  |

**Note** Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

### 3.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Oscillators   | Parameters | Conditions     |  | MIN. | TYP. | MAX. | Unit |
|---|------------|----------------|--|------|------|------|------|
| High-speed on-chip oscillator oscillation frequency <sup>Notes 1, 2</sup> | $f_{IH}$   |                |  | 1    |      | 32   | MHz  |
| High-speed on-chip oscillator oscillation frequency accuracy              |            | +85 to +105 °C | $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -2   |      | +2   | %    |
|   |            | -20 to +85 °C  | $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -1   |      | +1   | %    |
|   |            | -40 to -20 °C  | $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -1.5 |      | +1.5 | %    |
| Low-speed on-chip oscillator oscillation frequency                        | $f_{IL}$   |                |  |      | 15   |      | kHz  |
| Low-speed on-chip oscillator oscillation frequency accuracy               |            |                |  | -15  |      | +15  | %    |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

### 3.3 DC Characteristics

#### 3.3.1 Pin characteristics

<R> ( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ) (1/5)

| Items                                  | Symbol  | Conditions   | MIN.   | TYP. | MAX.  | Unit                   |    |
|--|---|--|--|------|-------|------------------------|----|
| Output current, high <sup>Note 1</sup> | I <sub>OH1</sub>  | Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141       | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ |      |       | -3.0 <sup>Note 2</sup> | mA |
|  |   | Total of P00 to P04, P40 to P43, P120, P130, P140, P141<br>(When duty $\leq 70\%$ <sup>Note 3</sup> )        | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ |      |       | -10.0                  | mA |
|  |   |  | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$    |      |       | -5.0                   | mA |
|  |   | Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,<br>(When duty $\leq 70\%$ <sup>Note 3</sup> ) | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ |      |       | -19.0                  | mA |
|  |   |  | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$    |      |       | -10.0                  | mA |
|  | Total of all pins<br>(When duty $\leq 70\%$ <sup>Note 3</sup> ) | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$   |  |      | -29.0 | mA                     |    |
|  | I <sub>OH2</sub>  | Per pin for P20 to P27, P150 to P154   | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$  |      |       | -0.1 <sup>Note 2</sup> | mA |
|  |   | Total of all pins<br>(When duty $\leq 70\%$ <sup>Note 3</sup> )  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$  |      |       | -1.3                   | mA |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the  $EV_{DD0}$ ,  $V_{DD}$  pins to an output pin.
  - However, do not exceed the total current value.
  - Specification under conditions where the duty factor  $\leq 70\%$ .  
The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$   
 <Example> Where  $n = 80\%$  and  $I_{OH} = -10.0\text{ mA}$   
 Total output current of pins =  $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> ( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ) (2/5)

| Items   | Symbol  | Conditions  | MIN.   | TYP. | MAX.                   | Unit                  |    |
|---|---|---|--|------|------------------------|-----------------------|----|
| Output current,<br>$I_{OL}$ <sup>Note 1</sup>                   | I <sub>OL1</sub>  | Per pin for P00 to P06, P10 to P16,<br>P30, P31, P40 to P43, P50, P51,<br>P70 to P77, P120, P130, P140, P141                  |  |      | 8.5 <sup>Note 2</sup>  | mA                    |    |
|   |   | Per pin for P60 to P63  |  |      | 15.0 <sup>Note 2</sup> | mA                    |    |
|   |   | Total of P00 to P04, P40 to P43, P120,<br>P130, P140, P141<br>(When duty $\leq 70\%$ <sup>Note 3</sup> )                      | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ |      |                        | 15.0                  | mA |
|   |   |   | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$    |      |                        | 9.0                   | mA |
|   |   | Total of P05, P06, P10 to P16, P30,<br>P31, P50, P51, P60 to P63,<br>P70 to P77<br>(When duty $\leq 70\%$ <sup>Note 3</sup> ) | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ |      |                        | 35.0                  | mA |
|   |   |   | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$    |      |                        | 20.0                  | mA |
|   | Total of all pins<br>(When duty $\leq 70\%$ <sup>Note 3</sup> ) |   |  |      | 50.0                   | mA                    |    |
|   | I <sub>OL2</sub>  | Per pin for P20 to P27, P150 to P154  |  |      |                        | 0.4 <sup>Note 2</sup> | mA |
| Total of all pins<br>(When duty $\leq 70\%$ <sup>Note 3</sup> ) |   | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$   |  |      | 5.2                    | mA                    |    |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the  $EV_{SS0}$  and  $V_{SS}$  pin.
  - However, do not exceed the total current value.
  - Specification under conditions where the duty factor  $\leq 70\%$ .

The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins =  $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ) (3/5)**

| Items               | Symbol    | Conditions   | MIN.   | TYP.          | MAX. | Unit          |   |
|---------------------|-----------|--|--|---------------|------|---------------|---|
| Input voltage, high | $V_{IH1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | Normal input buffer  | $0.8EV_{DD0}$ |      | $EV_{DD0}$    | V |
|                     | $V_{IH2}$ | P01, P03, P04, P10, P11, P13 to P16, P43   | TTL input buffer<br>$3.3\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ | 2.0           |      | $EV_{DD0}$    | V |
|                     |           |  | TTL input buffer<br>$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$    | 1.5           |      | $EV_{DD0}$    | V |
|                     | $V_{IH3}$ | P20 to P27, P150 to P154   |  | $0.7AV_{DD}$  |      | $AV_{DD}$     | V |
|                     | $V_{IH4}$ | P60 to P63   |  | $0.7EV_{DD0}$ |      | 6.0           | V |
|                     | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$                         |  | $0.8V_{DD}$   |      | $V_{DD}$      | V |
| Input voltage, low  | $V_{IL1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | Normal input buffer  | 0             |      | $0.2EV_{DD0}$ | V |
|                     | $V_{IL2}$ | P01, P03, P04, P10, P11, P13 to P16, P43   | TTL input buffer<br>$3.3\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ | 0             |      | 0.5           | V |
|                     |           |  | TTL input buffer<br>$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$    | 0             |      | 0.32          | V |
|                     | $V_{IL3}$ | P20 to P27, P150 to P154   |  | 0             |      | $0.3AV_{DD}$  | V |
|                     | $V_{IL4}$ | P60 to P63   |  | 0             |      | $0.3EV_{DD0}$ | V |
|                     | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$                         |  | 0             |      | $0.2V_{DD}$   | V |

**Caution** The maximum value of  $V_{IH}$  of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is  $EV_{DD0}$ , even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )** **(4/5)**

| Items                | Symbol           | Conditions   | MIN.   | TYP.             | MAX. | Unit |
|----------------------|------------------|--|--|------------------|------|------|
| Output voltage, high | V <sub>OH1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OH1} = -2.0\text{ mA}$   | $EV_{DD0} - 0.6$ |      | V    |
|                      |                  |  | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OH1} = -1.5\text{ mA}$   | $EV_{DD0} - 0.5$ |      | V    |
|                      | V <sub>OH2</sub> | P20 to P27, P150 to P154   | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ ,<br>$I_{OH2} = -100\ \mu\text{A}$ | $AV_{DD} - 0.5$  |      | V    |
| Output voltage, low  | V <sub>OL1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OL1} = 3.0\text{ mA}$    |                  | 0.6  | V    |
|                      |                  |  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OL1} = 1.5\text{ mA}$    |                  | 0.4  | V    |
|                      |                  |  | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OL1} = 0.6\text{ mA}$    |                  | 0.4  | V    |
|                      | V <sub>OL2</sub> | P20 to P27, P150 to P154   | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ ,<br>$I_{OL2} = 400\ \mu\text{A}$  |                  | 0.4  | V    |
|                      | V <sub>OL3</sub> | P60 to P63   | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OL3} = 3.0\text{ mA}$    |                  | 0.4  | V    |
|                      |                  |  | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$I_{OL3} = 2.0\text{ mA}$    |                  | 0.4  | V    |

**Caution** P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )** **(5/5)**

| Items                       | Symbol            | Conditions   | MIN.                             | TYP.                                  | MAX. | Unit          |     |            |
|-----------------------------|-------------------|--|----------------------------------|---------------------------------------|------|---------------|-----|------------|
| Input leakage current, high | I <sub>LIH1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141 | $V_i = EV_{DD0}$                 |                                       | 1    | $\mu\text{A}$ |     |            |
|                             | I <sub>LIH2</sub> | P137, $\overline{\text{RESET}}$  | $V_i = V_{DD}$                   |                                       | 1    | $\mu\text{A}$ |     |            |
|                             | I <sub>LIH3</sub> | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   | $V_i = V_{DD}$                   | In input port or external clock input | 1    | $\mu\text{A}$ |     |            |
|                             |                   |  |                                  | In resonator connection               | 10   | $\mu\text{A}$ |     |            |
|                             | I <sub>LIH4</sub> | P20 to P27, P150 to P154   | $V_i = AV_{DD}$                  |                                       | 1    | $\mu\text{A}$ |     |            |
| Input leakage current, low  | I <sub>LIL1</sub> | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141 | $V_i = EV_{SS0}$                 |                                       | -1   | $\mu\text{A}$ |     |            |
|                             | I <sub>LIL2</sub> | P137, $\overline{\text{RESET}}$  | $V_i = V_{SS}$                   |                                       | -1   | $\mu\text{A}$ |     |            |
|                             | I <sub>LIL3</sub> | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   | $V_i = V_{SS}$                   | In input port or external clock input | -1   | $\mu\text{A}$ |     |            |
|                             |                   |  |                                  | In resonator connection               | -10  | $\mu\text{A}$ |     |            |
|                             | I <sub>LIL4</sub> | P20 to P27, P150 to P154   | $V_i = AV_{SS}$                  |                                       | -1   | $\mu\text{A}$ |     |            |
| On-chip pull-up resistance  | R <sub>U</sub>    | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141             | $V_i = EV_{SS0}$ , In input port |                                       | 10   | 20            | 100 | k $\Omega$ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.3.2 Supply current characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = V_{SS0} = 0\text{ V}$ )

(1/3)

| Parameter   | Symbol                      | Conditions           |   |  |                  | MIN.                    | TYP. | MAX. | Unit |               |
|---|-----------------------------|----------------------|---|--|------------------|-------------------------|------|------|------|---------------|
| Supply current  | $I_{DD1}$ <sup>Note 1</sup> | Operating mode       | HS (high-speed main) mode <sup>Note 5</sup> | $f_{IH} = 32\text{ MHz}$ <sup>Note 3</sup>                                   | Basic operation  | $V_{DD} = 3.0\text{ V}$ |      | 2.1  |      | mA            |
|   |                             |                      |   |  | Normal operation | $V_{DD} = 3.0\text{ V}$ |      | 4.6  | 7.5  | mA            |
|   |                             |                      |   | $f_{IH} = 24\text{ MHz}$ <sup>Note 3</sup>                                   | Normal operation | $V_{DD} = 3.0\text{ V}$ |      | 3.7  | 5.8  | mA            |
|   |                             |                      |   |  | Normal operation | $V_{DD} = 3.0\text{ V}$ |      | 2.7  | 4.2  | mA            |
|   |                             |                      | HS (high-speed main) mode <sup>Note 5</sup> | $f_{MX} = 20\text{ MHz}$ <sup>Note 2</sup> ,<br>$V_{DD} = 3.0\text{ V}$      | Normal operation | Square wave input       |      | 3.0  | 4.9  | mA            |
|   |                             |                      |   |  |                  | Resonator connection    |      | 3.2  | 5.0  |               |
|   |                             |                      |   | $f_{MX} = 10\text{ MHz}$ <sup>Note 2</sup> ,<br>$V_{DD} = 3.0\text{ V}$      | Normal operation | Square wave input       |      | 1.9  | 2.9  | mA            |
|   |                             |                      |   |  |                  | Resonator connection    |      | 1.9  | 2.9  |               |
|   |                             |                      | Subsystem clock mode                        | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = -40^\circ\text{C}$ | Normal operation | Square wave input       |      | 4.1  | 4.9  | $\mu\text{A}$ |
|   |                             |                      |   |  |                  | Resonator connection    |      | 4.2  | 5.0  |               |
|   |                             |                      |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = +25^\circ\text{C}$ | Normal operation | Square wave input       |      | 4.2  | 4.9  | $\mu\text{A}$ |
|   |                             |                      |   |  |                  | Resonator connection    |      | 4.3  | 5.0  |               |
|   |                             |                      |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = +50^\circ\text{C}$ | Normal operation | Square wave input       |      | 4.3  | 5.5  | $\mu\text{A}$ |
|   |                             |                      |   |  |                  | Resonator connection    |      | 4.4  | 5.6  |               |
|   |                             |                      |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = +70^\circ\text{C}$ | Normal operation | Square wave input       |      | 4.5  | 6.3  | $\mu\text{A}$ |
|   |                             |                      |   |  |                  | Resonator connection    |      | 4.6  | 6.4  |               |
| $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = +85^\circ\text{C}$  | Normal operation            | Square wave input    |   | 4.8  | 7.7              | $\mu\text{A}$           |      |      |      |               |
|   |                             | Resonator connection |   | 4.9  | 7.8              |                         |      |      |      |               |
| $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 4</sup><br>$T_A = +105^\circ\text{C}$ | Normal operation            | Square wave input    |   | 6.9  | 19.7             | $\mu\text{A}$           |      |      |      |               |
|   |                             | Resonator connection |   | 7.0  | 19.8             |                         |      |      |      |               |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation ( $AMP_{HS1} = 1$ ). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $V_{DD} = 2.7\text{ V to }3.6\text{ V@1 MHz to }32\text{ MHz}$   
 $V_{DD} = 2.4\text{ V to }3.6\text{ V@1 MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )****(2/3)**

| Parameter                        | Symbol                      | Conditions                 |   |  | MIN.                    | TYP. | MAX.  | Unit          |               |
|----------------------------------|-----------------------------|----------------------------|---|--|-------------------------|------|-------|---------------|---------------|
| Supply current <sup>Note 1</sup> | $I_{DD2}$ <sup>Note 2</sup> | HALT mode                  | HS (high-speed main) mode <sup>Note 7</sup>                                   | $f_{IH} = 32\text{ MHz}$ <sup>Note 4</sup>                                   | $V_{DD} = 3.0\text{ V}$ |      | 0.54  | 2.90          | mA            |
|                                  |                             |                            |   | $f_{IH} = 24\text{ MHz}$ <sup>Note 4</sup>                                   | $V_{DD} = 3.0\text{ V}$ |      | 0.44  | 2.30          | mA            |
|                                  |                             |                            |   | $f_{IH} = 16\text{ MHz}$ <sup>Note 4</sup>                                   | $V_{DD} = 3.0\text{ V}$ |      | 0.40  | 1.70          | mA            |
|                                  |                             |                            | HS (high-speed main) mode <sup>Note 7</sup>                                   | $f_{MX} = 20\text{ MHz}$ <sup>Note 3</sup> ,<br>$V_{DD} = 3.0\text{ V}$      | Square wave input       |      | 0.28  | 1.90          | mA            |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.45  | 2.00          |               |
|                                  |                             |                            |   | $f_{MX} = 10\text{ MHz}$ <sup>Note 3</sup> ,<br>$V_{DD} = 3.0\text{ V}$      | Square wave input       |      | 0.19  | 1.02          | mA            |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.26  | 1.10          |               |
|                                  |                             |                            | Subsystem clock mode  | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = -40^\circ\text{C}$ | Square wave input       |      | 0.25  | 0.57          | $\mu\text{A}$ |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.44  | 0.76          |               |
|                                  |                             |                            |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = +25^\circ\text{C}$ | Square wave input       |      | 0.30  | 0.57          | $\mu\text{A}$ |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.49  | 0.76          |               |
|                                  |                             |                            |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = +50^\circ\text{C}$ | Square wave input       |      | 0.38  | 1.17          | $\mu\text{A}$ |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.57  | 1.36          |               |
|                                  |                             |                            |   | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = +70^\circ\text{C}$ | Square wave input       |      | 0.52  | 1.97          | $\mu\text{A}$ |
|                                  |                             |                            |   |  | Resonator connection    |      | 0.71  | 2.16          |               |
|                                  |                             |                            | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = +85^\circ\text{C}$  | Square wave input  |                         | 0.97 | 3.37  | $\mu\text{A}$ |               |
|                                  |                             |                            |   | Resonator connection   |                         | 1.16 | 3.56  |               |               |
|                                  |                             |                            | $f_{SUB} = 32.768\text{ kHz}$ <sup>Note 5</sup><br>$T_A = +105^\circ\text{C}$ | Square wave input  |                         | 3.01 | 15.37 | $\mu\text{A}$ |               |
| Resonator connection             |                             | 3.20                       |   | 15.56  |                         |      |       |               |               |
| $I_{DD3}$ <sup>Note 6</sup>      | STOP mode <sup>Note 8</sup> | $T_A = -40^\circ\text{C}$  |   |  |                         | 0.16 | 0.50  | $\mu\text{A}$ |               |
|                                  |                             | $T_A = +25^\circ\text{C}$  |   |  |                         | 0.23 | 0.50  |               |               |
|                                  |                             | $T_A = +50^\circ\text{C}$  |   |  |                         | 0.34 | 1.10  |               |               |
|                                  |                             | $T_A = +70^\circ\text{C}$  |   |  |                         | 0.46 | 1.90  |               |               |
|                                  |                             | $T_A = +85^\circ\text{C}$  |   |  |                         | 0.75 | 3.30  |               |               |
|                                  |                             | $T_A = +105^\circ\text{C}$ |   |  |                         | 2.94 | 15.30 |               |               |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). Including the current flowing into the RTC. However, not including the current flowing into the 12-bit interval timer, and watchdog timer.
  6. When subsystem clock is stopped. Not including the current flowing into the RTC, 12-bit interval timer, watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }16\text{ MHz}$
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$ )****(3/3)**

| Parameter                                      | Symbol                                    | Conditions  |  | MIN. | TYP. | MAX. | Unit          |
|--|---|---|--|------|------|------|---------------|
| Low-speed on-chip oscillator operating current | $I_{\text{FIL}}$ <sup>Note 1</sup>        |   |  |      | 0.20 |      | $\mu\text{A}$ |
| RTC operating current                          | $I_{\text{RTC}}$ <sup>Notes 1, 2, 3</sup> |   |  |      | 0.02 |      | $\mu\text{A}$ |
| 12-bit interval timer operating current        | $I_{\text{IT}}$ <sup>Notes 1, 2, 4</sup>  |   |  |      | 0.02 |      | $\mu\text{A}$ |
| Watchdog timer operating current               | $I_{\text{WDT}}$ <sup>Notes 1, 2, 5</sup> | $f_{\text{IL}} = 15\text{ kHz}$   |  |      | 0.22 |      | $\mu\text{A}$ |
| A/D converter operating current                | $I_{\text{ADC}}$ <sup>Notes 6, 7</sup>    | $\text{AV}_{\text{DD}} = 3.0\text{ V}$ , When conversion at maximum speed                                 |  |      | 420  | 720  | $\mu\text{A}$ |
| AVREF(+) current                               | $I_{\text{AVREF}}$ <sup>Note 8</sup>      | $\text{AV}_{\text{DD}} = 3.0\text{ V}$ , $\text{ADREFP1} = 0$ , $\text{ADREFP0} = 0$ <sup>Note 7</sup>    |  |      | 14.0 | 25.0 | $\mu\text{A}$ |
|  |   | $\text{AV}_{\text{REFP}} = 3.0\text{ V}$ , $\text{ADREFP1} = 0$ , $\text{ADREFP0} = 1$ <sup>Note 10</sup> |  |      | 14.0 | 25.0 | $\mu\text{A}$ |
|  |   | $\text{ADREFP1} = 1$ , $\text{ADREFP0} = 0$ <sup>Note 1</sup>   |  |      | 14.0 | 25.0 | $\mu\text{A}$ |
| A/D converter reference voltage current        | $I_{\text{ADREF}}$ <sup>Notes 1, 9</sup>  | $\text{V}_{\text{DD}} = 3.0\text{ V}$   |  |      | 75.0 |      | $\mu\text{A}$ |
| Temperature sensor operating current           | $I_{\text{TMPS}}$ <sup>Note 1</sup>       | $\text{V}_{\text{DD}} = 3.0\text{ V}$   |  |      | 75.0 |      | $\mu\text{A}$ |
| LVD operating current                          | $I_{\text{LVD}}$ <sup>Notes 1, 11</sup>   |   |  |      | 0.08 |      | $\mu\text{A}$ |
| BGO operating current                          | $I_{\text{BGO}}$ <sup>Notes 1, 12</sup>   |   |  |      | 2.5  | 12.2 | $\text{mA}$   |
| Self-programming operating current             | $I_{\text{FSP}}$ <sup>Notes 1, 13</sup>   |   |  |      | 2.5  | 12.2 | $\text{mA}$   |
| SNOOZE operating current                       | $I_{\text{SNOZ}}$                         | A/D converter operation ( $\text{AV}_{\text{DD}} = 3.0\text{ V}$ )  | The mode is performed <sup>Notes 1, 14</sup> |      | 0.50 | 1.10 | $\text{mA}$   |
|  |   |   | During A/D conversion <sup>Note 1</sup>      |      | 0.60 | 1.34 | $\text{mA}$   |
|  |   |   | During A/D conversion <sup>Note 7</sup>      |      | 420  | 720  | $\mu\text{A}$ |
|  |   | CSI/UART operation <sup>Note 1</sup>  |  |      | 0.70 | 1.54 | $\text{mA}$   |

(Notes and Remarks are listed on the next page.)

- <R> **Notes**
1. Current flowing to  $V_{DD}$ .
  2. When high-speed on-chip oscillator and high-speed system clock are stopped.
  3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either  $I_{DD1}$  or  $I_{DD2}$ , and  $I_{RTC}$ , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected,  $I_{FIL}$  should be added.  $I_{DD2}$  subsystem clock operation includes the operational current of the real-time clock.
  4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either  $I_{DD1}$  or  $I_{DD2}$ , and  $I_{IT}$ , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected,  $I_{FIL}$  should be added.
  5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$ , or  $I_{DD3}$  and  $I_{WDT}$  when the watchdog timer is in operation.
  6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$ ,  $I_{AVREF}$ ,  $I_{ADREF}$  when the A/D converter operates in an operation mode or the HALT mode.
  7. Current flowing to the  $AV_{DD}$ .
  8. Current flowing from the reference voltage source of A/D converter.
  9. Operation current flowing to the internal reference voltage.
  10. Current flowing to the  $AV_{REFP}$ .
  11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit is in operation.
  12. Current flowing only during data flash rewrite.
  13. Current flowing only during self programming.

- Remarks**
1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  2.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  3.  $f_{CLK}$ : CPU/peripheral hardware clock frequency
  4. Temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$



## 3.4 AC Characteristics

(T<sub>A</sub> = -40 to +105°C, AV<sub>DD</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)

| Items  | Symbol                                | Conditions                                       |   | MIN.                            | TYP.    | MAX. | Unit               |    |
|--|---------------------------------------|--|---|---------------------------------|---------|------|--------------------|----|
| Instruction cycle (minimum instruction execution time)           | T <sub>cy</sub>                       | Main system clock (f <sub>MAIN</sub> ) operation | HS (high-speed main) mode   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.03125 |      | 1                  | μs |
|  |                                       |  |   | 2.4 V ≤ V <sub>DD</sub> < 2.7 V | 0.0625  |      | 1                  | μs |
|  |                                       | Subsystem clock (f <sub>SUB</sub> ) operation    |   | 2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V | 28.5    | 30.5 | 31.3               | μs |
|  |                                       | In the self programming mode                     | HS (high-speed main) mode   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V | 0.03125 |      | 1                  | μs |
|  |                                       |  |   | 2.4 V ≤ V <sub>DD</sub> < 2.7 V | 0.0625  |      | 1                  | μs |
| External system clock frequency                                  | f <sub>EX</sub>                       | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V                  |   | 1.0                             |         | 20.0 | MHz                |    |
|  |                                       | 2.4 V ≤ V <sub>DD</sub> < 2.7 V                  |   | 1.0                             |         | 16.0 | MHz                |    |
|  | f <sub>EXS</sub>                      |  |   | 32                              |         | 35   | kHz                |    |
| External system clock input high-level width, low-level width    | t <sub>EXH</sub> , t <sub>EXL</sub>   | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V                  |   | 24                              |         |      | ns                 |    |
|  |                                       | 2.4 V ≤ V <sub>DD</sub> < 2.7 V                  |   | 30                              |         |      | ns                 |    |
|  | t <sub>EXHS</sub> , t <sub>EXLS</sub> |  |   | 13.7                            |         |      | μs                 |    |
| TI00, TI01, TI03 to TI07 input high-level width, low-level width | t <sub>TIH</sub> , t <sub>TIL</sub>   |  |   | 1/f <sub>MCK</sub> +10          |         |      | ns <sup>Note</sup> |    |
| TO00, TO01, TO03 to TO07 output frequency                        | f <sub>TO</sub>                       | HS (high-speed main) mode                        | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 8    | MHz                |    |
|  |                                       |  | 2.4 V ≤ EV <sub>DD0</sub> < 2.7 V                                       |                                 |         | 4    | MHz                |    |
| PCLBUZ0, PCLBUZ1 output frequency                                | f <sub>PCL</sub>                      | HS (high-speed main) mode                        | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       |                                 |         | 8    | MHz                |    |
|  |                                       |  | 2.4 V ≤ EV <sub>DD0</sub> < 2.7 V                                       |                                 |         | 4    | MHz                |    |
| Interrupt input high-level width, low-level width                | t <sub>INTH</sub> , t <sub>INTL</sub> | INTP0  | 2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V   | 1                               |         |      | μs                 |    |
|  |                                       | INTP1 to INTP11                                  | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V                                       | 1                               |         |      | μs                 |    |
| Key interrupt input high-level width, low-level width            | t <sub>KR</sub>                       | KR0 to KR9                                       | 2.4 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.4 V ≤ AV <sub>DD0</sub> ≤ 3.6 V | 250                             |         |      | ns                 |    |
| RESET low-level width  | t <sub>RSL</sub>                      |  |   | 10                              |         |      | μs                 |    |

**Note** The following conditions are required for low-voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.

2.4 V ≤ EV<sub>DD0</sub> < 2.7 V : MIN. 125 ns

**Remark** f<sub>MCK</sub>: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer clock select register 0 (TPS0) and timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

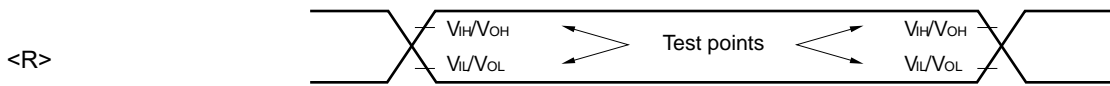
**Minimum Instruction Execution Time during Main System Clock Operation**

<R>

$T_{CY}$  vs  $V_{DD}$  (HS (high-speed main) mode)



**AC Timing Test Points**



**External System Clock Timing**



<R> **TI/TO Timing**



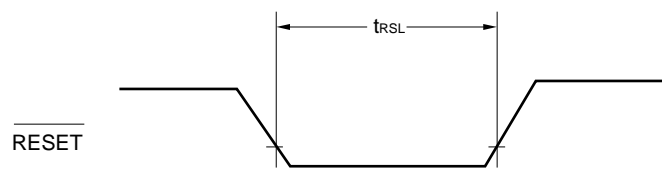
**Interrupt Request Input Timing**



**Key Interrupt Input Timing**



**$\overline{\text{RESET}}$  Input Timing**



### 3.5 Peripheral Functions Characteristics

#### AC Timing Test Points



#### 3.5.1 Serial array unit

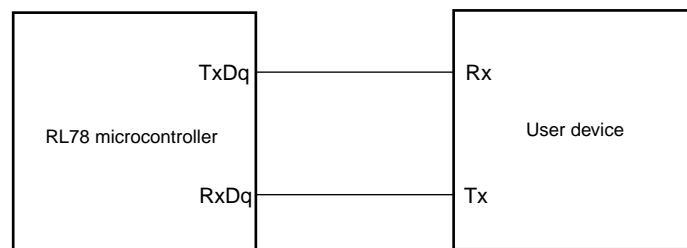
(1) During communication at same potential (UART mode) (dedicated baud rate generator output)  
 ( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )

| Parameter                       | Symbol | Conditions  | MIN. | TYP. | MAX.                  | Unit |
|---------------------------------|--------|---|------|------|-----------------------|------|
| Transfer rate <sup>Note 1</sup> |        |   |      |      | $f_{MCK}/12$          | bps  |
|                                 |        | Theoretical value of the maximum transfer rate<br>$f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$ |      |      | $2.6^{\text{Note 2}}$ | Mbps |

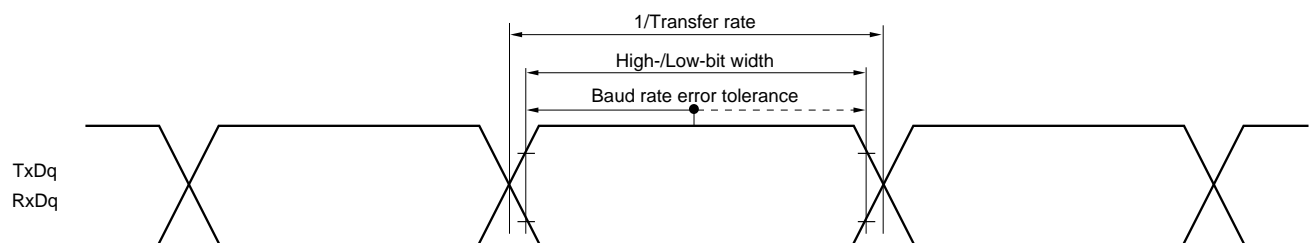
- Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps.  
**2.** The following conditions are required for low-voltage interface when  $EV_{DD0} < V_{DD}$ .  
 $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$  : MAX. 1.3 Mbps

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

#### UART mode connection diagram (during communication at same potential)



#### UART mode bit width (during communication at same potential) (reference)



- Remarks 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)  
**2.**  $f_{MCK}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter   | Symbol      | Conditions   | MIN.              | TYP. | MAX. | Unit |
|---|-------------|--|-------------------|------|------|------|
| SCKp cycle time   | $t_{KCY1}$  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ $t_{KCY1} \geq 4/f_{CLK}$ | 250               |      |      | ns   |
|   |             | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ $t_{KCY1} \geq 4/f_{CLK}$ | 500               |      |      | ns   |
| SCKp high-/low-level width  | $t_{KH1}$ , | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$                           | $t_{KCY1}/2 - 36$ |      |      | ns   |
|   | $t_{KL1}$   | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$                           | $t_{KCY1}/2 - 76$ |      |      | ns   |
| Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>            | $t_{SIK1}$  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$                           | 66                |      |      | ns   |
|   |             | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$                           | 113               |      |      | ns   |
| Slp hold time (from SCKp $\uparrow$ ) <sup>Note 1</sup>           | $t_{KSI1}$  |  | 38                |      |      | ns   |
| Delay time from SCKp $\downarrow$ to SOp output <sup>Note 2</sup> | $t_{KSO1}$  | $C = 30\text{ p}$ <sup>Note 3</sup>                                      |                   |      | 50   | ns   |

**Notes 1.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ . The Slp setup time or Slp hold time becomes "from SCKp $\downarrow$ " when  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

**2.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ . The delay time to SOp output becomes "from SCKp $\uparrow$ " when  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

**3.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

<R> (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)  
 ( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$ )

| Parameter  | Symbol                                 | Conditions   | MIN.   | TYP.                            | MAX. | Unit                  |                        |
|--|--|--|--|---------------------------------|------|-----------------------|------------------------|
| SCKp cycle time <sup>Note 1</sup>                                    | $t_{\text{KCY2}}$                      | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ | $16\text{ MHz} < f_{\text{MCK}}$                             | $16/f_{\text{MCK}}$             |      | ns                    |                        |
|  |  |  | $f_{\text{MCK}} \leq 16\text{ MHz}$                          | $12/f_{\text{MCK}}$             |      | ns                    |                        |
|  |  | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $12/f_{\text{MCK}}$ and<br>1000 |      | ns                    |                        |
| SCKp high-/low-level width   | $t_{\text{KH2}}$ ,<br>$t_{\text{KL2}}$ | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $t_{\text{KCY2}}/2-14$          |      | ns                    |                        |
|  |  | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $t_{\text{KCY2}}/2-16$          |      | ns                    |                        |
| Slp setup time<br>(to SCKp $\uparrow$ ) <sup>Note 2</sup>            | $t_{\text{SIK2}}$                      | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $1/f_{\text{MCK}} + 40$         |      | ns                    |                        |
|  |  | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $1/f_{\text{MCK}} + 60$         |      | ns                    |                        |
| Slp hold time<br>(from SCKp $\uparrow$ ) <sup>Note 2</sup>           | $t_{\text{KSI2}}$                      | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $1/f_{\text{MCK}}+62$           |      | ns                    |                        |
|  |  | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |  | $1/f_{\text{MCK}}+62$           |      | ns                    |                        |
| Delay time from SCKp $\downarrow$ to<br>SOp output <sup>Note 3</sup> | $t_{\text{KSO2}}$                      | $C = 30\text{ pF}$ <sup>Note 4</sup>                         | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |                                 |      | $2/f_{\text{MCK}}+66$ | ns                     |
|  |  |  | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ |                                 |      |                       | $2/f_{\text{MCK}}+113$ |

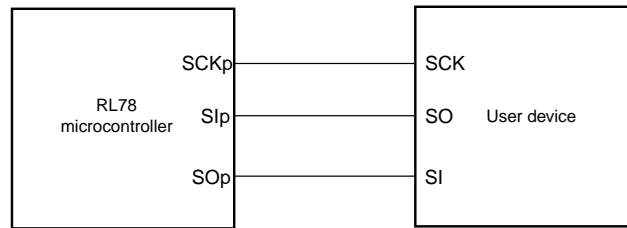
**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

- When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time or Slp hold time becomes "from SCKp $\downarrow$ " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp $\uparrow$ " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- C is the load capacitance of the SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
 g: PIM number (g = 0, 1)
- 2.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
 n: Channel number (mn = 00 to 03, 10, 11))

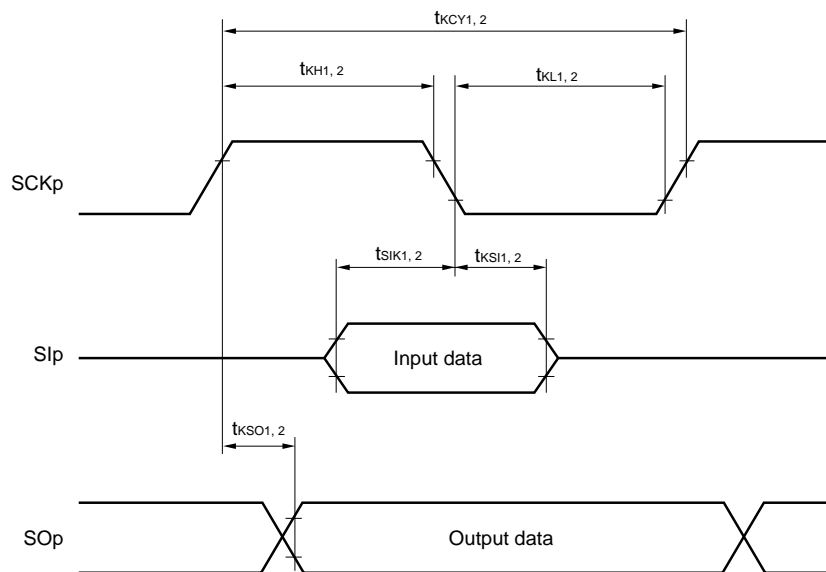
**CSI mode connection diagram (during communication at same potential)**



**CSI mode serial transfer timing (during communication at same potential)**  
 (When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ .)



**CSI mode serial transfer timing (during communication at same potential)**  
 (When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
  2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)



**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter                     | Symbol              | Conditions  | MIN.                                   | MAX.                  | Unit |
|-------------------------------|---------------------|---|--|-----------------------|------|
| SCLr clock frequency          | f <sub>SCL</sub>    | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ |  | 400 <sup>Note 1</sup> | kHz  |
|                               |                     | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$  |  | 100 <sup>Note 1</sup> | kHz  |
| Hold time when SCLr = "L"     | t <sub>LOW</sub>    | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 1200                                   |                       | ns   |
|                               |                     | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$  | 4600                                   |                       | ns   |
| Hold time when SCLr = "H"     | t <sub>HIGH</sub>   | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 1200                                   |                       | ns   |
|                               |                     | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$  | 4600                                   |                       | ns   |
| Data setup time (reception)   | t <sub>SU:DAT</sub> | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | $1/f_{MCK} +$<br>220 <sup>Note 2</sup> |                       | ns   |
|                               |                     | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$  | $1/f_{MCK} +$<br>580 <sup>Note 2</sup> |                       | ns   |
| Data hold time (transmission) | t <sub>HD:DAT</sub> | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 0                                      | 770                   | ns   |
|                               |                     | $2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$  | 0                                      | 1420                  | ns   |

**Notes 1.** The value must also be  $f_{CLK}/4$  or lower.

**2.** Set the  $f_{MCK}$  value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**



- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
  2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

**(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**  
**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter                       | Symbol | Conditions |   | MIN.  | TYP. | MAX.                  | Unit |
|---------------------------------|--------|------------|---|---|------|-----------------------|------|
| Transfer rate <sup>Note 1</sup> |        | Reception  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ |   |      | $f_{MCK}/12$          | bps  |
|                                 |        |            |   | Theoretical value of the maximum transfer rate<br>$f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$ |      | 2.6                   | Mbps |
|                                 |        |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ ,<br>$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$    |   |      | $f_{MCK}/12$          | bps  |
|                                 |        |            |   | Theoretical value of the maximum transfer rate<br>$f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$ |      | 2.6 <sup>Note 2</sup> | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps.

**2.** The following conditions are required for low-voltage interface when  $EV_{DD0} < V_{DD}$ .

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$  : MAX. 1.3 Mbps

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

<R>

**Remarks 1.**  $V_b[V]$ : Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10, 11)

**(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)**  
**(T<sub>A</sub> = -40 to +105°C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

| Parameter     | Symbol | Conditions   |  | MIN.  | TYP. | MAX.          | Unit                   |
|---------------|--------|--------------|--|---|------|---------------|------------------------|
| Transfer rate |        | Transmission | 2.7 V ≤ EV <sub>DD0</sub> ≤ 3.6 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V |   |      | <b>Note 1</b> | bps                    |
|               |        |              |  | Theoretical value of the maximum transfer rate<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ, V <sub>b</sub> = 2.3 V |      |               | 1.2 <sup>Note 2</sup>  |
|               |        |              | 2.4 V ≤ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V |   |      | <b>Note 3</b> | bps                    |
|               |        |              |  | Theoretical value of the maximum transfer rate<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 5.5 kΩ, V <sub>b</sub> = 1.6 V |      |               | 0.43 <sup>Note 4</sup> |

**Notes** 1. The smaller maximum transfer rate derived by using f<sub>mck</sub>/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> ≤ 3.6 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met.

See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f<sub>mck</sub>/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

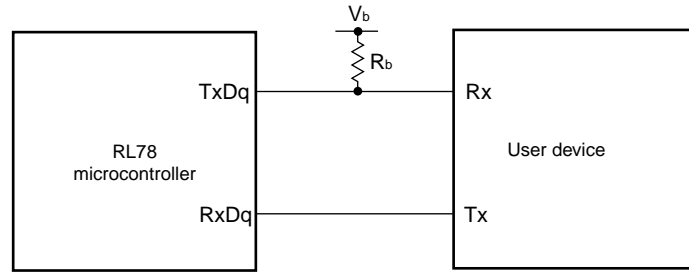
4. This value as an example is calculated when the conditions described in the “Conditions” column are met.

See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

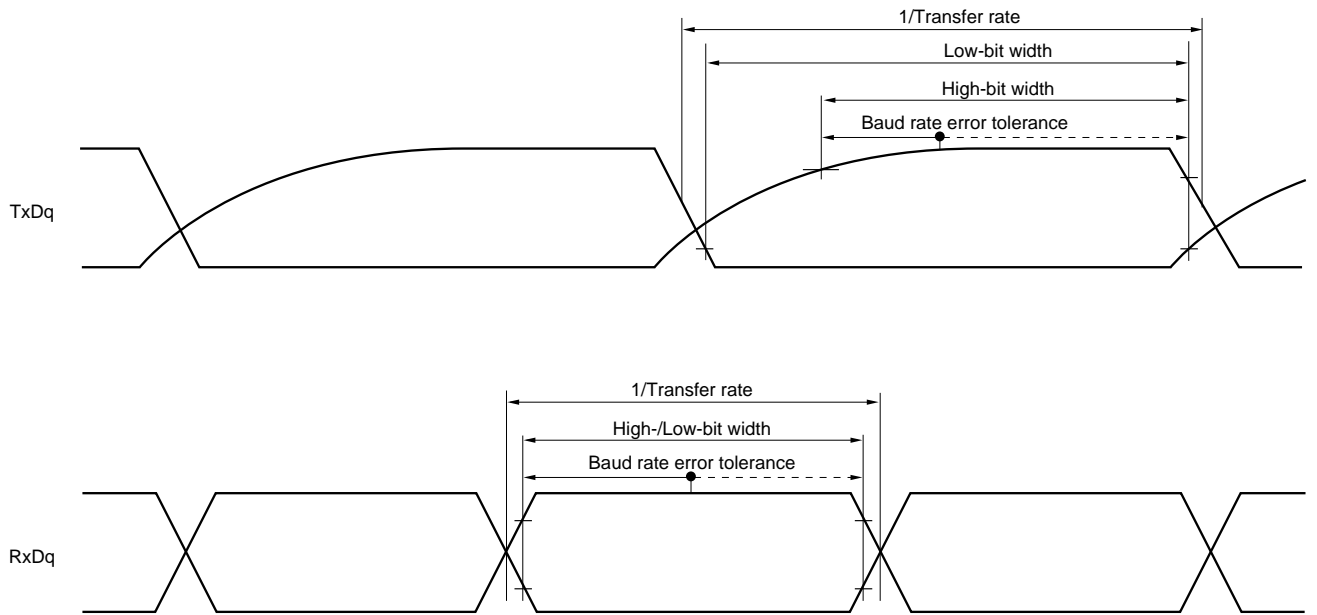
**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 25- to 48-pin products)/EV<sub>DD</sub> tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

<R>

**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**



- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)**  
**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter             | Symbol     | Conditions   | MIN.                      | TYP.               | MAX. | Unit |
|-----------------------|------------|--|---------------------------|--------------------|------|------|
| SCKp cycle time       | $t_{KCY1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1} \geq 4/f_{CLK}$ | 1000               |      | ns   |
|                       |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ ,<br>$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | $t_{KCY1} \geq 4/f_{CLK}$ | 2300               |      | ns   |
| SCKp high-level width | $t_{KH1}$  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                           | $t_{KCY1}/2 - 340$ |      | ns   |
|                       |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$       |                           | $t_{KCY1}/2 - 916$ |      | ns   |
| SCKp low-level width  | $t_{KL1}$  | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                           | $t_{KCY1}/2 - 36$  |      | ns   |
|                       |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$       |                           | $t_{KCY1}/2 - 100$ |      | ns   |

&lt;R&gt;

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

- Remarks**
- $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  - p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  - CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)**  
**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter  | Symbol     | Conditions  | MIN. | TYP. | MAX. | Unit |
|--|------------|---|------|------|------|------|
| Slp setup time<br>(to SCKp $\uparrow$ ) <sup>Note 1</sup>            | $t_{SIK1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 354  |      |      | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 958  |      |      | ns   |
| Slp hold time<br>(from SCKp $\uparrow$ ) <sup>Note 1</sup>           | $t_{KSH1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 38   |      |      | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 38   |      |      | ns   |
| Delay time from SCKp $\downarrow$ to<br>SOp output <sup>Note 1</sup> | $t_{KSO1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ |      |      | 390  | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |      |      | 966  | ns   |
| Slp setup time<br>(to SCKp $\downarrow$ ) <sup>Note 2</sup>          | $t_{SIK1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 88   |      |      | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 220  |      |      | ns   |
| Slp hold time<br>(from SCKp $\downarrow$ ) <sup>Note 2</sup>         | $t_{KSH1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 38   |      |      | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 38   |      |      | ns   |
| Delay time from SCKp $\uparrow$ to<br>SOp output <sup>Note 2</sup>   | $t_{KSO1}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ |      |      | 50   | ns   |
|  |            | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |      |      | 50   | ns   |

- Notes 1.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ .  
**2.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

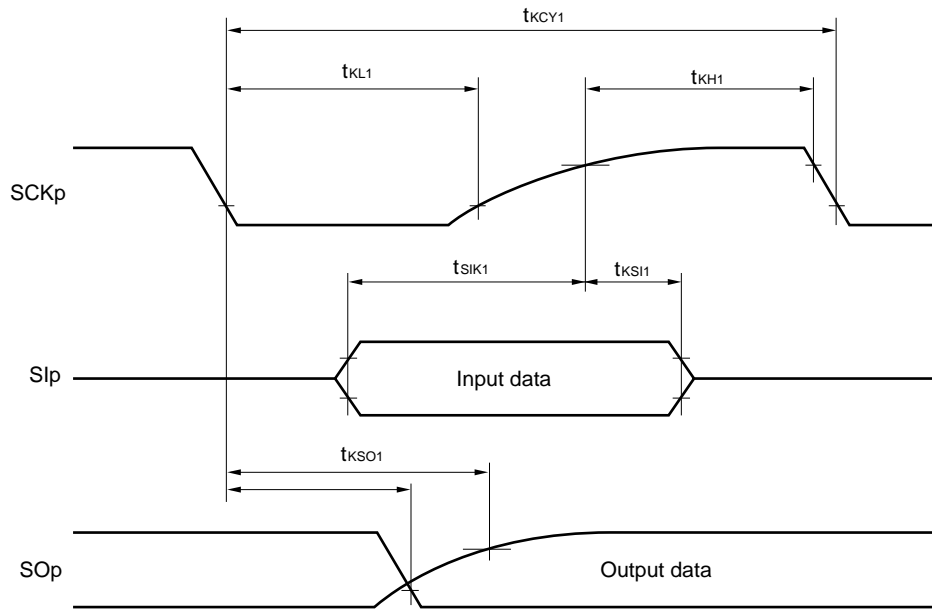
<R>

**CSI mode connection diagram (during communication at different potential)**

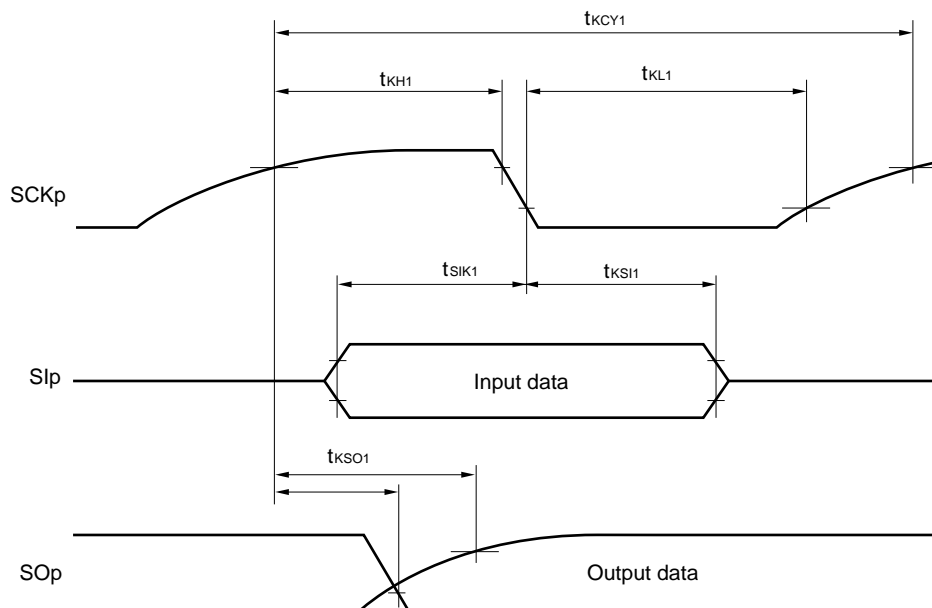


- Remarks 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage  
**2.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)  
**3.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.



(7) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)  
 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )

| Parameter  | Symbol                   | Conditions  | MIN.   | TYP.         | MAX.               | Unit |
|--|--------------------------|---|--|--------------|--------------------|------|
| SCKp cycle time <sup>Note 1</sup>                                    | $t_{KCY2}$               | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$   | $24\text{ MHz} < f_{MCK}$                    | $40/f_{MCK}$ |                    | ns   |
|  |                          |   | $20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$ | $32/f_{MCK}$ |                    | ns   |
|  |                          |   | $16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$ | $28/f_{MCK}$ |                    | ns   |
|  |                          |   | $8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$  | $24/f_{MCK}$ |                    | ns   |
|  |                          |   | $4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$   | $16/f_{MCK}$ |                    | ns   |
|  |                          |   | $f_{MCK} \leq 4\text{ MHz}$                  | $12/f_{MCK}$ |                    | ns   |
|  |                          | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ ,<br>$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$  | $24\text{ MHz} < f_{MCK}$                    | $96/f_{MCK}$ |                    | ns   |
|  |                          |   | $20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$ | $72/f_{MCK}$ |                    | ns   |
|  |                          |   | $16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$ | $64/f_{MCK}$ |                    | ns   |
|  |                          |   | $8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$  | $52/f_{MCK}$ |                    | ns   |
|  |                          |   | $4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$   | $32/f_{MCK}$ |                    | ns   |
|  |                          |   | $f_{MCK} \leq 4\text{ MHz}$                  | $20/f_{MCK}$ |                    | ns   |
| SCKp high-/low-level width   | $t_{KH2}$ ,<br>$t_{KL2}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$  | $t_{KCY2}/2 - 36$                            |              |                    | ns   |
|  |                          | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$   | $t_{KCY2}/2 - 100$                           |              |                    | ns   |
| Slp setup time<br>(to SCKp $\uparrow$ ) <sup>Note 2</sup>            | $t_{SIK2}$               | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$  | $1/f_{MCK} + 40$                             |              |                    | ns   |
|  |                          | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$   | $1/f_{MCK} + 60$                             |              |                    | ns   |
| Slp hold time<br>(from SCKp $\uparrow$ ) <sup>Note 2</sup>           | $t_{KSI2}$               |   | $1/f_{MCK} + 62$                             |              |                    | ns   |
| Delay time from SCKp $\downarrow$ to<br>SOp output <sup>Note 3</sup> | $t_{KSO2}$               | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ |  |              | $2/f_{MCK} + 428$  | ns   |
|  |                          | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |  |              | $2/f_{MCK} + 1146$ | ns   |

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

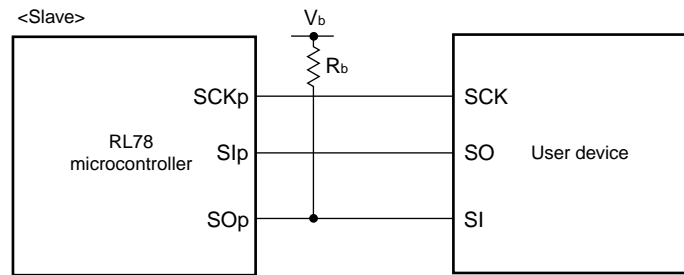
**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time or Slp hold time becomes "from SCKp $\downarrow$ " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp $\uparrow$ " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

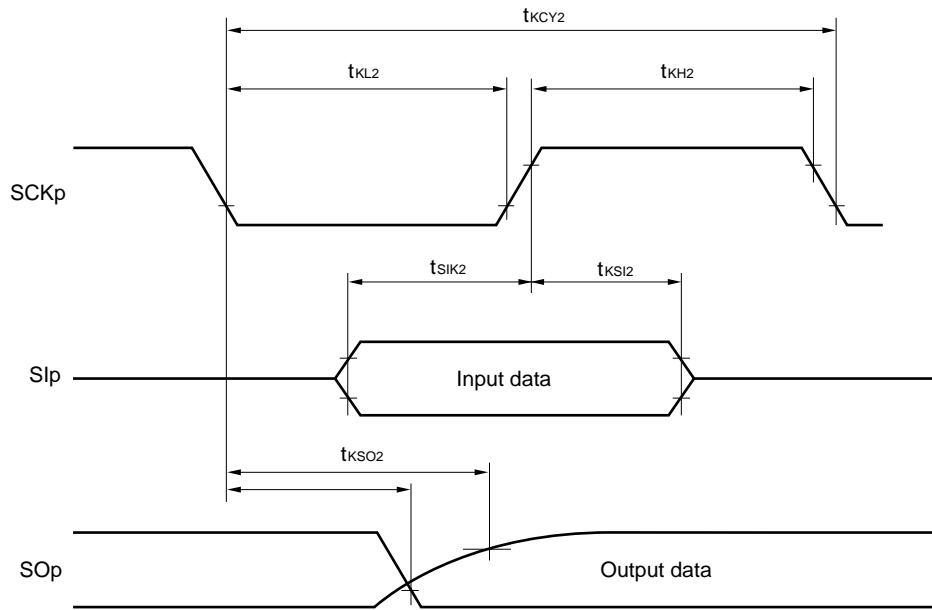
<R>

(Remarks are listed on the next page.)

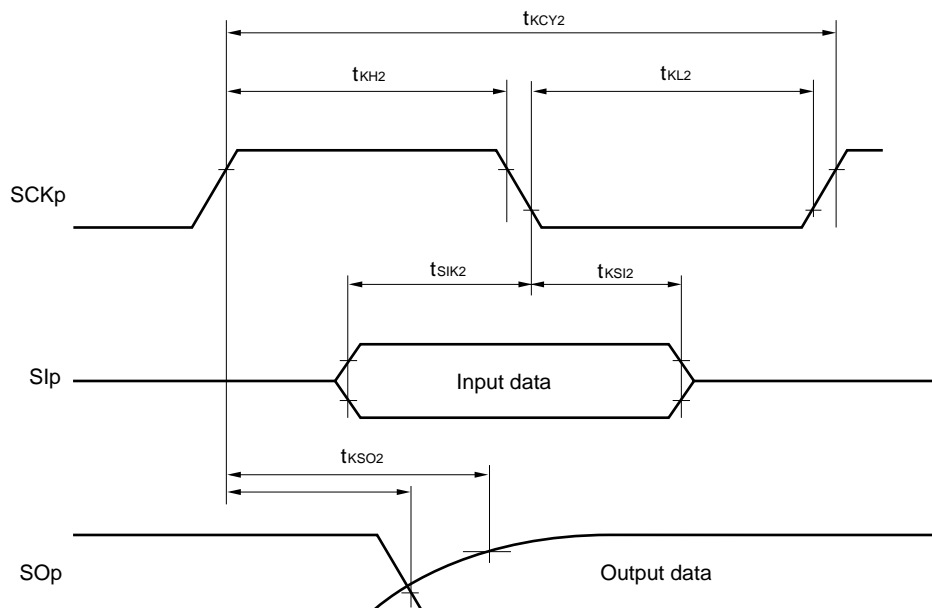
**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)
  3.  $f_{\text{mck}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 02, 10))
  4. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
- 2.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(8) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode) (1/2)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter                 | Symbol            | Conditions  | MIN. | MAX.                  | Unit |
|---------------------------|-------------------|---|------|-----------------------|------|
| SCLr clock frequency      | f <sub>SCL</sub>  | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 k $\Omega$  |      | 400 <sup>Note 1</sup> | kHz  |
|                           |                   | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 k $\Omega$ |      | 100 <sup>Note 1</sup> | kHz  |
|                           |                   | 2.4 V $\leq$ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V $\leq$ V <sub>b</sub> $\leq$ 2.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 k $\Omega$      |      | 100 <sup>Note 1</sup> | kHz  |
| Hold time when SCLr = "L" | t <sub>LOW</sub>  | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 k $\Omega$  | 1200 |                       | ns   |
|                           |                   | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 k $\Omega$ | 4600 |                       | ns   |
|                           |                   | 2.4 V $\leq$ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V $\leq$ V <sub>b</sub> $\leq$ 2.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 k $\Omega$      | 4650 |                       | ns   |
| Hold time when SCLr = "H" | t <sub>HIGH</sub> | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 k $\Omega$  | 500  |                       | ns   |
|                           |                   | 2.7 V $\leq$ EV <sub>DD0</sub> $\leq$ 3.6 V,<br>2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 k $\Omega$ | 2400 |                       | ns   |
|                           |                   | 2.4 V $\leq$ EV <sub>DD0</sub> < 3.3 V,<br>1.6 V $\leq$ V <sub>b</sub> $\leq$ 2.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 k $\Omega$      | 1830 |                       | ns   |

(Notes, Caution and Remarks are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode) (2/2)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )**

| Parameter                     | Symbol       | Conditions  | MIN.                                | MAX. | Unit |
|-------------------------------|--------------|---|-------------------------------------|------|------|
| Data setup time (reception)   | $t_{SU:DAT}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$  | $1/f_{MCK} + 340$ <sup>Note 2</sup> |      | ns   |
|                               |              | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | $1/f_{MCK} + 760$ <sup>Note 2</sup> |      | ns   |
|                               |              | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ ,<br>$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | $1/f_{MCK} + 570$ <sup>Note 2</sup> |      | ns   |
| Data hold time (transmission) | $t_{HD:DAT}$ | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$  | 0                                   | 770  | ns   |
|                               |              | $2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$ ,<br>$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ | 0                                   | 1420 | ns   |
|                               |              | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ ,<br>$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 0                                   | 1215 | ns   |

**Notes 1.** The value must also be  $f_{CLK}/4$  or lower.

**2.** Set the  $f_{MCK}$  value to keep the hold time of  $SCLr = "L"$  and  $SCLr = "H"$ .

**Caution** Select the TTL input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the  $SDAr$  pin and the N-ch open drain output ( $V_{DD}$  tolerance (When 25- to 48-pin products)/ $EV_{DD}$  tolerance (When 64-pin products)) mode for the  $SCLr$  pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

&lt;R&gt;

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**



- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)
  3.  $f_{mck}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))
  4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

### 3.5.2 Serial interface IICA

#### (1) I<sup>2</sup>C standard mode, fast mode

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$ )

| Parameter                                       | Symbol              | Conditions                                      | Standard Mode  |      | Fast Mode |      | Unit          |
|---|---------------------|---|--|------|-----------|------|---------------|
|   |                     |   | MIN.   | MAX. | MIN.      | MAX. |               |
| SCLA0 clock frequency                           | $f_{\text{SCL}}$    | Fast mode: $f_{\text{CLK}} \geq 3.5\text{ MHz}$ |  |      | 0         | 400  | kHz           |
|   |                     | Normal mode: $f_{\text{CLK}} \geq 1\text{ MHz}$ | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ | 0    | 100       |      |               |
| Setup time of restart condition                 | $t_{\text{SU:STA}}$ |   | 4.7  |      | 0.6       |      | $\mu\text{s}$ |
| Hold time <sup>Note 1</sup>                     | $t_{\text{HD:STA}}$ |   | 4.0  |      | 0.6       |      | $\mu\text{s}$ |
| Hold time when SCLA0 = "L"                      | $t_{\text{LOW}}$    |   | 4.7  |      | 1.3       |      | $\mu\text{s}$ |
| Hold time when SCLA0 = "H"                      | $t_{\text{HIGH}}$   |   | 4.0  |      | 0.6       |      | $\mu\text{s}$ |
| Data setup time (reception)                     | $t_{\text{SU:DAT}}$ |   | 250  |      | 100       |      | ns            |
| Data hold time (transmission) <sup>Note 2</sup> | $t_{\text{HD:DAT}}$ |   | 0  | 3.45 | 0         | 0.9  | $\mu\text{s}$ |
| Setup time of stop condition                    | $t_{\text{SU:STO}}$ |   | 4.0  |      | 0.6       |      | $\mu\text{s}$ |
| Bus-free time                                   | $t_{\text{BUF}}$    |   | 4.7  |      | 1.3       |      | $\mu\text{s}$ |

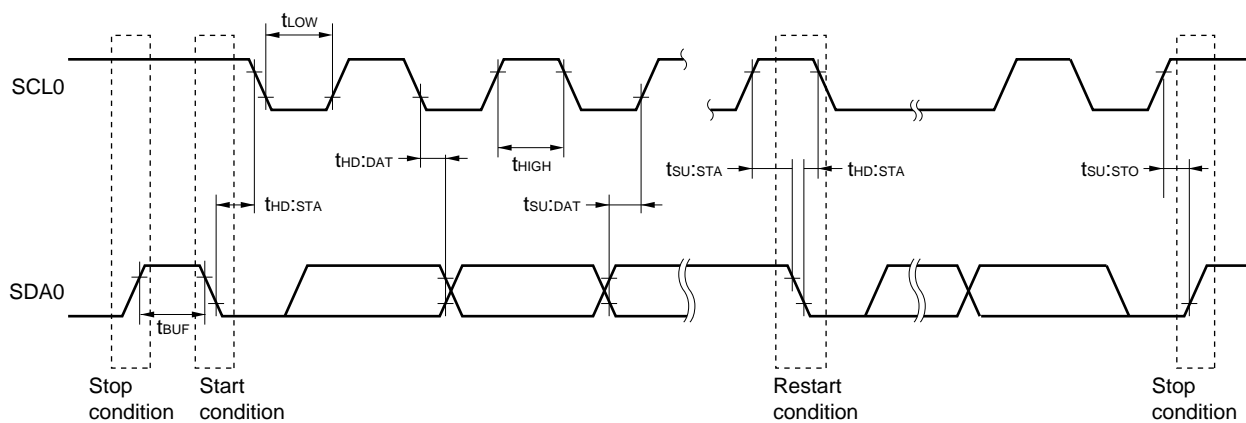
- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
  - The maximum value (MAX.) of  $t_{\text{HD:DAT}}$  is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of  $C_b$  (communication line capacitance) and the value of  $R_b$  (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode:  $C_b = 400\text{ pF}$ ,  $R_b = 2.7\text{ k}\Omega$

Fast mode:  $C_b = 320\text{ pF}$ ,  $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



### 3.6 Analog Characteristics

#### 3.6.1 A/D converter characteristics

**Division of A/D Converter Characteristics**

| Reference voltage<br>Input channel   | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $AV_{DD}$<br>Reference voltage (-) = $AV_{SS}$ | Reference voltage (+) = Internal<br>reference voltage<br>Reference voltage (-) = $AV_{SS}$ |
|--|--|--|--|
| High-accuracy channel; ANI0 to ANI12<br>(input buffer power supply: $AV_{DD}$ )          | See 3.6.1 (1)  | See 3.6.1 (2)  | See 3.6.1 (5)  |
| Standard channel; ANI16 to ANI30<br>(input buffer power supply: $V_{DD}$ or $EV_{DD0}$ ) | See 3.6.1 (3)  | See 3.6.1 (4)  |  |
| Temperature sensor, internal<br>reference voltage output                                 | See 3.6.1 (3)  | See 3.6.1 (4)  | –  |

<R> (1) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target for conversion: ANI2 to ANI12

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

| Parameter                                    | Symbol     | Conditions   | MIN.  | TYP. | MAX.        | Unit          |
|--|------------|--|-------|------|-------------|---------------|
| Resolution                                   | $R_{ES}$   | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                                       | 8.    |      | 12.         | bit           |
| Overall error <sup>Note</sup>                | $A_{INL}$  | 12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                  |       |      | $\pm 6.0$   | LSB           |
| Conversion time                              | $t_{CONV}$ | $ADTYP = 0$ ,<br>12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ | 3.375 |      |             | $\mu\text{s}$ |
| Zero-scale error <sup>Note</sup>             | $E_{ZS}$   | 12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                  |       |      | $\pm 4.5$   | LSB           |
| Full-scale error <sup>Note</sup>             | $E_{FS}$   | 12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                  |       |      | $\pm 4.5$   | LSB           |
| Integral linearity error <sup>Note</sup>     | $I_{LE}$   | 12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                  |       |      | $\pm 2.0$   | LSB           |
| Differential linearity error <sup>Note</sup> | $D_{LE}$   | 12-bit resolution<br>$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$                  |       |      | $\pm 1.5$   | LSB           |
| Analog input voltage                         | $V_{AIN}$  |  | 0     |      | $AV_{REFP}$ | V             |

**Note** Excludes quantization error ( $\pm 1/2$  LSB).



<R> (2) When reference voltage (+) =  $AV_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) =  $AV_{SS}$  (ADREFM = 0), target for conversion: ANI0 to ANI12

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{DD}$ , Reference voltage (-) =  $AV_{SS} = 0\text{ V}$ )

| Parameter                                    | Symbol     | Conditions                      |   | MIN.  | TYP. | MAX.      | Unit          |
|--|------------|---------------------------------|---|-------|------|-----------|---------------|
| Resolution                                   | $R_{ES}$   |                                 | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ | 8     |      | 12        | bit           |
| Overall error <sup>Note</sup>                | $A_{INL}$  | 12-bit resolution               | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |       |      | $\pm 7.5$ | LSB           |
| Conversion time                              | $t_{CONV}$ | ADTYP = 0,<br>12-bit resolution | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ | 3.375 |      |           | $\mu\text{s}$ |
| Zero-scale error <sup>Note</sup>             | $E_{ZS}$   | 12-bit resolution               | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |       |      | $\pm 6.0$ | LSB           |
| Full-scale error <sup>Note</sup>             | $E_{FS}$   | 12-bit resolution               | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |       |      | $\pm 6.0$ | LSB           |
| Integral linearity error <sup>Note</sup>     | $I_{LE}$   | 12-bit resolution               | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |       |      | $\pm 3.0$ | LSB           |
| Differential linearity error <sup>Note</sup> | $D_{LE}$   | 12-bit resolution               | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |       |      | $\pm 2.0$ | LSB           |
| Analog input voltage                         | $V_{AIN}$  |                                 |   | 0     |      | $AV_{DD}$ | V             |

**Note** Excludes quantization error ( $\pm 1/2$  LSB).

<R> (3) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target for conversion: ANI16 to ANI30, internal reference voltage, temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

| Parameter                                      | Symbol     | Conditions   |  | MIN.                           | TYP. | MAX.                          | Unit          |
|--|------------|--|--|--------------------------------|------|-------------------------------|---------------|
| Resolution                                     | $R_{ES}$   |  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ | 8                              |      | 12                            | bit           |
| Overall error <sup>Note 1</sup>                | $A_{INL}$  | 12-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 7.0$                     | LSB           |
| Conversion time                                | $t_{CONV}$ | $ADTYP = 0$ ,<br>12-bit resolution   | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ | 4.125                          |      |                               | $\mu\text{s}$ |
| Zero-scale error <sup>Note 1</sup>             | $E_{ZS}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 5.0$                     | LSB           |
| Full-scale error <sup>Note 1</sup>             | $E_{FS}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 5.0$                     | LSB           |
| Integral linearity error <sup>Note 1</sup>     | $I_{LE}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 3.0$                     | LSB           |
| Differential linearity error <sup>Note 1</sup> | $D_{LE}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 2.0$                     | LSB           |
| Analog input voltage                           | $V_{AIN}$  |  |  | 0.                             |      | $AV_{REFP}$<br>and $EV_{DD0}$ | V             |
|  |            | Internal reference voltage<br>( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , HS (high-speed main) mode)        |  | $V_{BGR}$ <sup>Note 2</sup>    |      |                               | V             |
|  |            | Temperature sensor output voltage<br>( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , HS (high-speed main) mode) |  | $V_{TMPS25}$ <sup>Note 2</sup> |      |                               | V             |

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** See 3.6.2 Temperature sensor, internal reference voltage output characteristics.

<R> (4) When reference voltage (+) =  $AV_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) =  $AV_{SS}$  (ADREFM = 0), target for conversion: ANI16 to ANI30, internal reference voltage, temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD0} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{DD}$ , Reference voltage (-) =  $AV_{SS} = 0\text{ V}$ )

| Parameter                                      | Symbol     | Conditions   |   | MIN.                           | TYP. | MAX.                     | Unit          |
|--|------------|--|---|--------------------------------|------|--------------------------|---------------|
| Resolution                                     | $R_{ES}$   |  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ | 8                              |      | 12                       | bit           |
| Overall error <sup>Note 1</sup>                | $A_{INL}$  | 12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 8.5$                | LSB           |
| Conversion time                                | $t_{CONV}$ | ADTYP = 0,<br>12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ | 4.125                          |      |                          | $\mu\text{s}$ |
| Zero-scale error <sup>Note 1</sup>             | $E_{ZS}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 8.0$                | LSB           |
| Full-scale error <sup>Note 1</sup>             | $E_{FS}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 8.0$                | LSB           |
| Integral linearity error <sup>Note 1</sup>     | $I_{LE}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 3.5$                | LSB           |
| Differential linearity error <sup>Note 1</sup> | $D_{LE}$   | 12-bit resolution  | $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ |                                |      | $\pm 2.5$                | LSB           |
| Analog input voltage                           | $V_{AIN}$  |  |   | 0                              |      | $AV_{DD}$ and $EV_{DD0}$ | V             |
|  |            | Internal reference voltage<br>( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , HS (high-speed main) mode)        |   | $V_{BGR}$ <sup>Note 2</sup>    |      |                          | V             |
|  |            | Temperature sensor output voltage<br>( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , HS (high-speed main) mode) |   | $V_{TMPS25}$ <sup>Note 2</sup> |      |                          | V             |

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** See 3.6.2 Temperature sensor, internal reference voltage output characteristics.

<R> (5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) =  $AV_{SS}$  (ADREFM = 0), target for conversion: ANI0 to ANI12, ANI16 to ANI30

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ,  $2.4\text{ V} \leq EV_{DD} \leq V_{DD}$ ,  $2.4\text{ V} \leq AV_{DD} \leq V_{DD}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) = Internal reference voltage, Reference voltage (-) =  $AV_{SS} = 0\text{ V}$ , HS (high-speed main) mode)

| Parameter                                    | Symbol        | Conditions                                 | MIN. | TYP. | MAX.      | Unit          |
|--|---------------|--|------|------|-----------|---------------|
| Resolution                                   | $R_{ES}$      |  | 8    |      |           | bit           |
| Conversion time                              | $t_{CONV}$    | 8-bit resolution                           | 16.0 |      |           | $\mu\text{s}$ |
| Zero-scale error <sup>Note</sup>             | $E_{ZS}$      | 8-bit resolution                           |      |      | $\pm 4.0$ | LSB           |
| Integral linearity error <sup>Note</sup>     | $I_{LE}$      | 8-bit resolution                           |      |      | $\pm 2.0$ | LSB           |
| Differential linearity error <sup>Note</sup> | $D_{LE}$      | 8-bit resolution                           |      |      | $\pm 2.5$ | LSB           |
| Reference voltage (+)                        | $AV_{REF(+)}$ | = Internal reference voltage ( $V_{BGR}$ ) | 1.38 | 1.45 | 1.50      | V             |
| Analog input voltage                         | $V_{AIN}$     |  | 0    |      | $V_{BGR}$ | V             |

**Note** Excludes quantization error ( $\pm 1/2$  LSB).

### 3.6.2 Temperature sensor, internal reference voltage output characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , HS (high-speed main) mode)

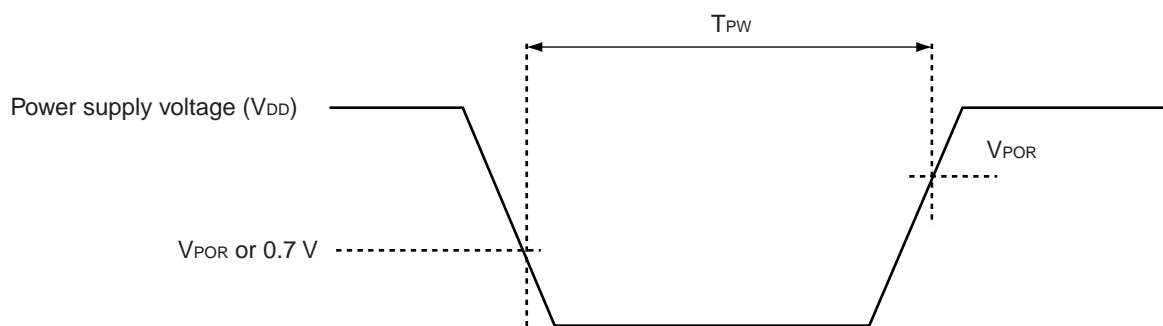
| Parameter                         | Symbol       | Conditions  | MIN. | TYP. | MAX. | Unit                       |
|-----------------------------------|--------------|---|------|------|------|----------------------------|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$             |      | 1.05 |      | V                          |
| Internal reference voltage        | $V_{BGR}$    | Setting ADS register = 81H  | 1.38 | 1.45 | 1.5  | V                          |
| Temperature coefficient           | $F_{VTMPS}$  | Temperature sensor output voltage that depends on the temperature |      | -3.6 |      | $\text{mV}/^\circ\text{C}$ |
| Operation stabilization wait time | $t_{AMP}$    |   | 10   |      |      | $\mu\text{s}$              |

### 3.6.3 POR circuit characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                           | Symbol    | Conditions             | MIN. | TYP. | MAX. | Unit          |
|-------------------------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage                   | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V             |
|                                     | $V_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V             |
| Minimum pulse width <sup>Note</sup> | $T_{PW}$  |                        | 300  |      |      | $\mu\text{s}$ |

**Note** This is the time required for the POR circuit to execute a reset when  $V_{DD}$  falls below  $V_{PDR}$ . When the microcontroller enters STOP mode or if the main system clock ( $f_{MAIN}$ ) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before  $V_{DD}$  rises to  $V_{POR}$  after having fallen below 0.7 V.



## 3.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{PDR} \leq V_{DD} \leq 3.6$  V,  $V_{SS} = 0$  V)**

| Parameter            | Symbol     | Conditions             | MIN. | TYP. | MAX. | Unit          |
|----------------------|------------|------------------------|------|------|------|---------------|
| Detection voltage    | $V_{LVD2}$ | Power supply rise time | 3.01 | 3.13 | 3.25 | V             |
|                      |            | Power supply fall time | 2.94 | 3.06 | 3.18 | V             |
|                      | $V_{LVD3}$ | Power supply rise time | 2.90 | 3.02 | 3.14 | V             |
|                      |            | Power supply fall time | 2.85 | 2.96 | 3.07 | V             |
|                      | $V_{LVD4}$ | Power supply rise time | 2.81 | 2.92 | 3.03 | V             |
|                      |            | Power supply fall time | 2.75 | 2.86 | 2.97 | V             |
|                      | $V_{LVD5}$ | Power supply rise time | 2.70 | 2.81 | 2.92 | V             |
|                      |            | Power supply fall time | 2.64 | 2.75 | 2.86 | V             |
|                      | $V_{LVD6}$ | Power supply rise time | 2.61 | 2.71 | 2.81 | V             |
|                      |            | Power supply fall time | 2.55 | 2.65 | 2.75 | V             |
|                      | $V_{LVD7}$ | Power supply rise time | 2.51 | 2.61 | 2.71 | V             |
|                      |            | Power supply fall time | 2.45 | 2.55 | 2.65 | V             |
| Minimum pulse width  | $t_{LW}$   |                        | 300  |      |      | $\mu\text{s}$ |
| Detection delay time |            |                        |      |      | 300  | $\mu\text{s}$ |

**Remark**  $V_{LVD(n-1)} > V_{LVDn}$ :  $n = 3$  to  $7$ **LVD Detection Voltage of Interrupt & Reset Mode****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{PDR} \leq V_{DD} \leq 3.6$  V,  $V_{SS} = 0$  V)**

| Parameter              | Symbol     | Conditions   | MIN.                         | TYP. | MAX. | Unit |   |
|------------------------|------------|--|------------------------------|------|------|------|---|
| Interrupt & reset mode | $V_{LVD5}$ | VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage | 2.64                         | 2.75 | 2.86 | V    |   |
|                        | $V_{LVD4}$ | LVIS1, LVIS0 = 1, 0                                  | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
|                        |            |  | Falling interrupt voltage    | 2.75 | 2.86 | 2.97 | V |
|                        | $V_{LVD3}$ | LVIS1, LVIS0 = 0, 1                                  | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
|                        |            |  | Falling interrupt voltage    | 2.85 | 2.96 | 3.07 | V |

**Caution** Set the detection voltage ( $V_{LVD}$ ) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

**HS (high-speed main) mode:**  $V_{DD} = 2.7$  to  $3.6$  V@1 MHz to 32 MHz

$V_{DD} = 2.4$  to  $3.6$  V@1 MHz to 16 MHz

## 3.6.5 Supply voltage rise slope characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)**

| Parameter           | Symbol    | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------|-----------|------------|------|------|------|------|
| Supply voltage rise | $SV_{DD}$ |            |      |      | 54   | V/ms |

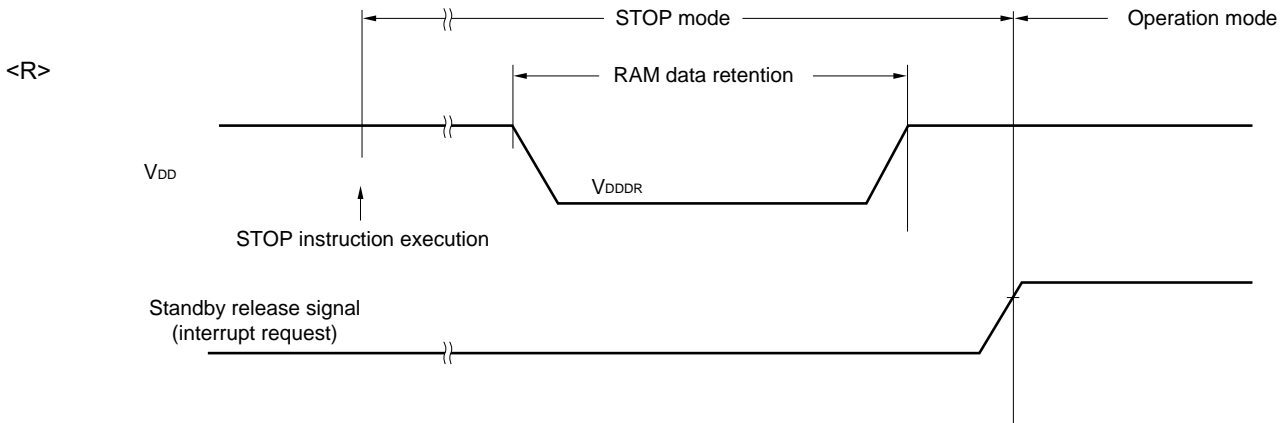
**Caution** Be sure to maintain the internal reset state until  $V_{DD}$  reaches the operating voltage range specified in 3.4 AC Characteristics, by using the LVD circuit or external reset pin.

<R> 3.7 RAM Data Retention Characteristics

<R> ( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

| Parameter                     | Symbol     | Conditions | MIN.                 | TYP. | MAX. | Unit |
|-------------------------------|------------|------------|----------------------|------|------|------|
| Data retention supply voltage | $V_{DDDR}$ |            | 1.44 <sup>Note</sup> |      | 3.6  | V    |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4$  V  $\leq V_{DD} \leq 3.6$  V,  $V_{SS} = 0$  V)

| Parameter  | Symbol     | Conditions  | MIN.    | TYP.      | MAX. | Unit  |
|--|------------|---|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency                | $f_{CLK}$  | $2.4$ V $\leq V_{DD} \leq 3.6$ V                  | 1       |           | 32   | MHz   |
| Number of code flash rewrites <sup>Notes 1, 2, 3</sup> | $C_{erwr}$ | Retained for 20 years<br>$T_A = 85^\circ\text{C}$ | 1,000   |           |      | Times |
| Number of data flash rewrites <sup>Notes 1, 2, 3</sup> |            | Retained for 1 years<br>$T_A = 25^\circ\text{C}$  |         | 1,000,000 |      |       |
|  |            | Retained for 5 years<br>$T_A = 85^\circ\text{C}$  | 100,000 |           |      |       |
|  |            | Retained for 20 years<br>$T_A = 85^\circ\text{C}$ | 10,000  |           |      |       |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer and Renesas Electronics self programming library
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. This temperature is the average value at which data are retained.

<R>

### 3.9 Dedicated Flash Memory Programmer Communication (UART)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )

| Parameter     | Symbol | Conditions                      | MIN.    | TYP. | MAX. | Unit |
|---------------|--------|---------------------------------|---------|------|------|------|
| Transfer rate |        | During flash memory programming | 115.2 k |      | 1 M  | bps  |

### 3.10 Timing Specs for Switching Flash Memory Programming Modes

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ )

| Parameter   | Symbol        | Conditions   | MIN. | TYP. | MAX. | Unit          |
|---|---------------|--|------|------|------|---------------|
| How long from when an external reset ends until the initial communication settings are specified                              | $t_{SUIINIT}$ | POR and LVD reset must end before the external reset ends. |      |      | 100  | ms            |
| How long from when the TOOL0 pin is placed at the low level until a external reset ends                                       | $t_{SU}$      | POR and LVD reset must end before the external reset ends. | 10   |      |      | $\mu\text{s}$ |
| <R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time) | $t_{HD}$      | POR and LVD reset must end before the external reset ends. | 1    |      |      | ms            |



- <1> The low level is input to the TOOL0 pin.
- <2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{SUIINIT}$ : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

$t_{SU}$ : How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R>  $t_{HD}$ : How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

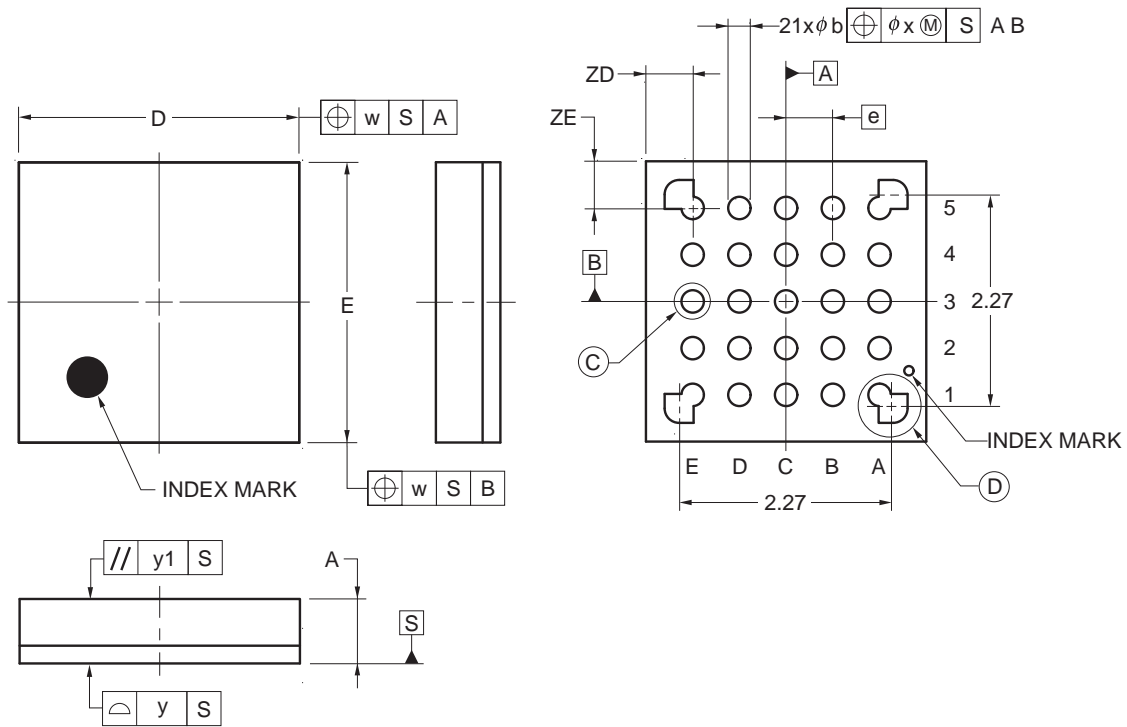
### 4. PACKAGE DRAWINGS

#### 4.1 25-pin products

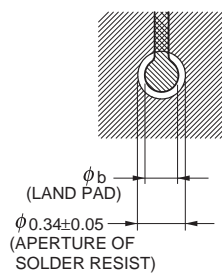
R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

|     |                           |                     |                      |                       |
|-----|---------------------------|---------------------|----------------------|-----------------------|
| <R> | <b>JEITA Package Code</b> | <b>RENESAS Code</b> | <b>Previous Code</b> | <b>MASS (Typ) [g]</b> |
|     | P-WFLGA25-3x3-0.50        | PWLG0025KA-A        | P25FC-50-2N2-3       | 0.01                  |

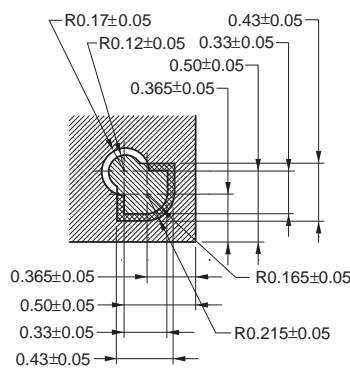
Unit: mm



DETAIL OF © PART



DETAIL OF © PART



| ITEM | DIMENSIONS |
|------|------------|
| D    | 3.00±0.10  |
| E    | 3.00±0.10  |
| w    | 0.20       |
| e    | 0.50       |
| A    | 0.69±0.07  |
| b    | 0.24±0.05  |
| x    | 0.05       |
| y    | 0.08       |
| y1   | 0.20       |
| ZD   | 0.50       |
| ZE   | 0.50       |

© 2014 Renesas Electronics Corporation. All rights reserved.





4.3 48-pin products

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB  
 R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGF, R5F10EGEGFB

|                    |              |                |                 |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16            |



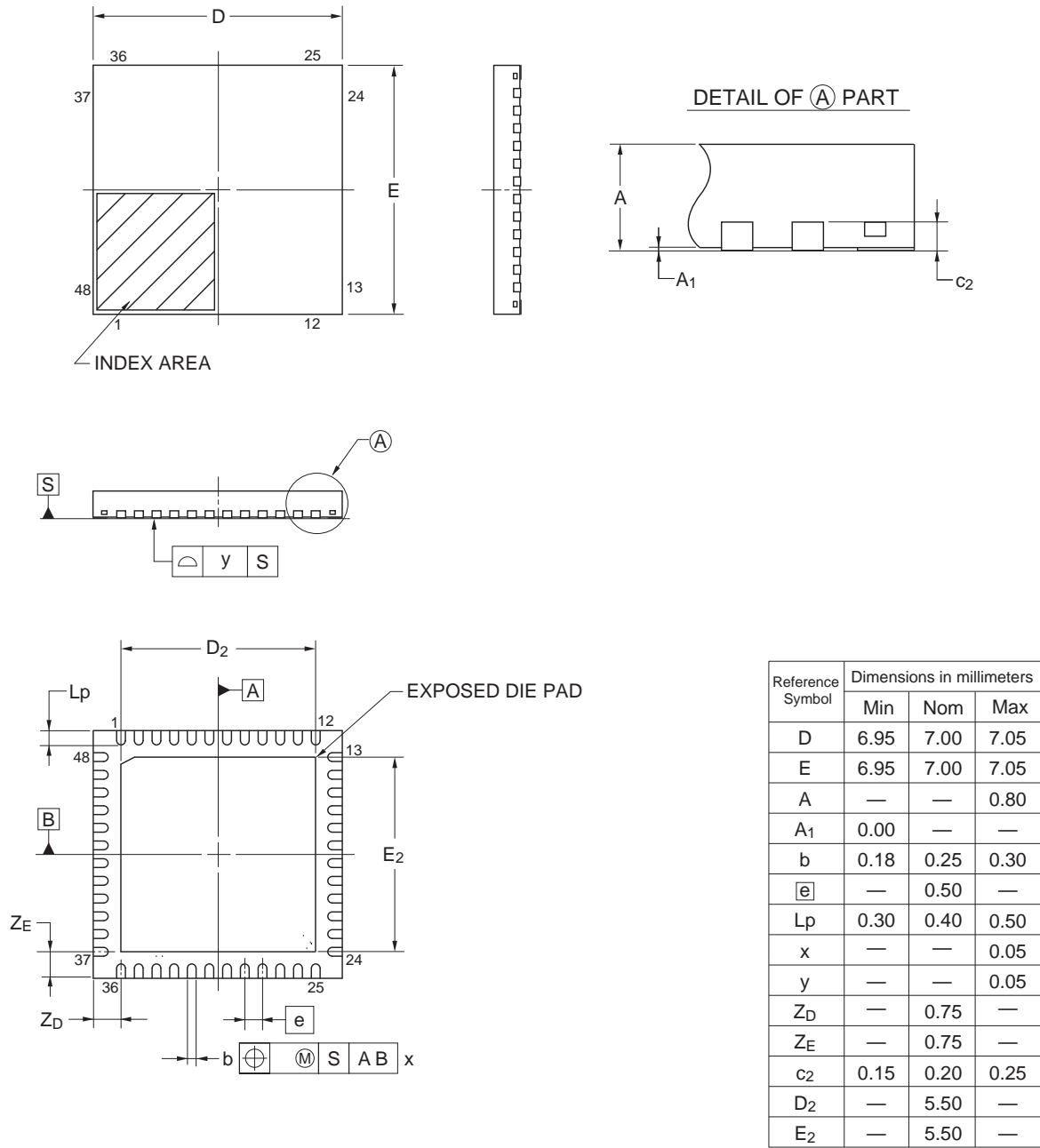
**NOTE**  
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA  
 R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA

<R>

| JEITA Package Code | RENESAS Code | Previous Code             | MASS (Typ) [g] |
|--------------------|--------------|---------------------------|----------------|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-7 | 0.13           |

Unit: mm

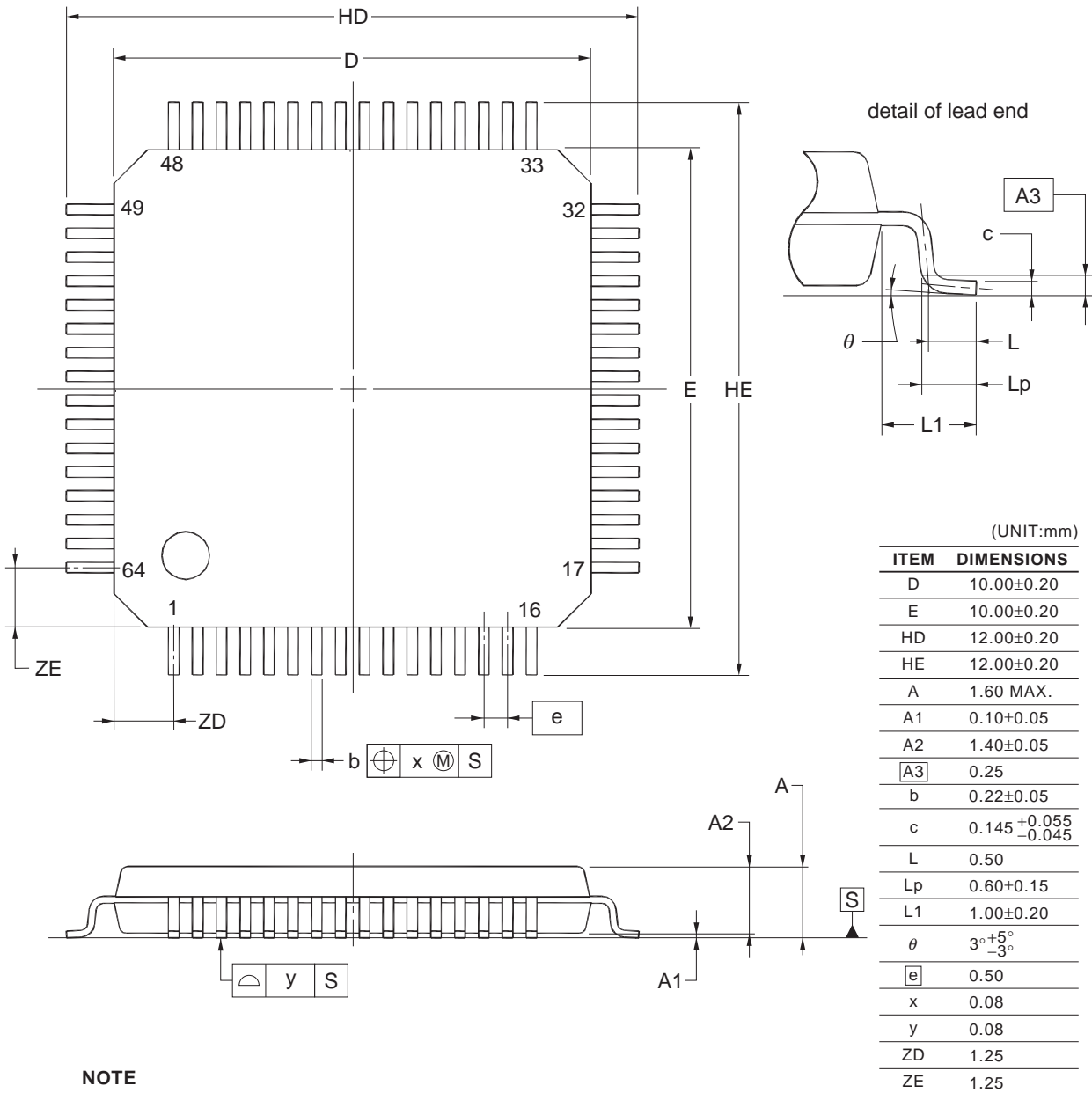


© 2015 Renesas Electronics Corporation. All rights reserved.

4.4 64-pin products

R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB  
 R5F10ELCGFB, R5F10ELDGF B, R5F10ELEGFB

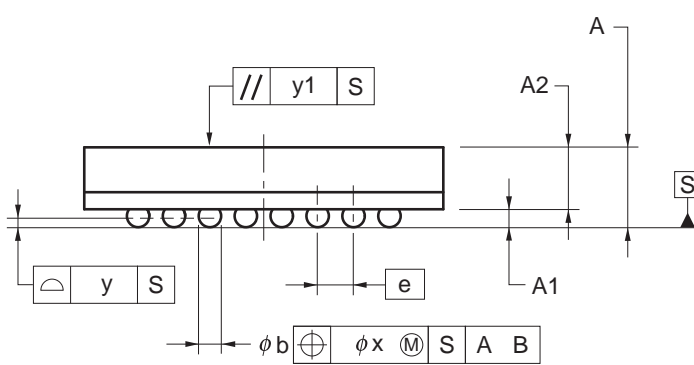
|                      |              |                |                 |
|----------------------|--------------|----------------|-----------------|
| JEITA Package Code   | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35            |



**NOTE**  
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

|                    |              |                |                 |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-VFBGA64-4x4-0.40 | PVBG0064LA-A | P64F1-40-AA2-2 | 0.03            |



(UNIT:mm)

| ITEM | DIMENSIONS |
|------|------------|
| D    | 4.00±0.10  |
| E    | 4.00±0.10  |
| w    | 0.15       |
| A    | 0.89±0.10  |
| A1   | 0.20±0.05  |
| A2   | 0.69       |
| e    | 0.40       |
| b    | 0.25±0.05  |
| x    | 0.05       |
| y    | 0.08       |
| y1   | 0.20       |
| ZD   | 0.60       |
| ZE   | 0.60       |

©2012 Renesas Electronics Corporation. All rights reserved.

## Revision History

## RL78/G1A Data Sheet

| Rev.         | Date  | Description            |  |
|--------------|---|------------------------|--|
|              |   | Page                   | Summary  |
| 0.01         | Dec 26, 2011  | -                      | First Edition issued   |
| 1.00         | Sep 25, 2013  | p.1                    | Modification of 1.1 Features   |
|              |   | p.4                    | Modification of Table 1-1. List of Ordering Part Numbers   |
|              |   | p.6                    | Modification of Remark 3 to 1.3.2 32-pin products.   |
|              |   | p.13                   | Modification of 1.5.2 32-pin products.   |
|              |   | p.14                   | Modification of 1.5.3 48-pin products.   |
|              |   | p.16                   | Modification of 1.6 Outline of Functions   |
|              |   | p.21                   | Modification of 2.2.1 X1, XT1 oscillator characteristics   |
|              |   | p.31, 32               | Modification of Note 1 in 2.3.2 Supply current characteristics                                   |
|              |   | p.34, 35               | Modification of Minimum Instruction Execution Time during Main System Clock Operation            |
|              |   | p.37                   | Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics                |
|              |   | p.46 to 58             | Modification of Caution to 2.5.1 Serial array unit.  |
|              |   | p.63 to 68             | Modification of 2.6.1 A/D converter characteristics  |
|              |   | p.71                   | Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics      |
|              |   | p.71                   | Modification of 2.8 Flash Memory Programming Characteristics                                     |
| p.72         | Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes                            |                        |  |
| p.73 to 117  | Addition of 3 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$ ) |                        |  |
| p.118 to 123 | Modification of 4. PACKAGE DRAWINGS   |                        |  |
| 2.10         | Nov 30, 2016  | p.4                    | Modification of Table 1-1. List of Ordering Part Numbers   |
|              |   | p.5 to 10              | Modification of the position of the index mark in 1.3.1 25-pin products to 1.3.4 64-pin products |
|              |   | p.6                    | Modification of Remark 3   |
|              |   | p.13                   | Modification of 1.5.2 32-pin products  |
|              |   | p.14                   | Modification of 1.5.3 48-pin products  |
|              |   | p.16                   | Modification of description in 1.6 Outline of Functions  |
|              |   | p.21                   | Modification of 2.2.1 X1, XT1 oscillator characteristics   |
|              |   | p.31, 32               | Modification of Note 1 in 2.3.2 Supply current characteristics                                   |
|              |   | p.34, 35               | Modification of Minimum Instruction Execution Time during Main System Clock Operation            |
|              |   | p.36                   | Modification of AC Timing Test Points and TI/TO Timing   |
|              |   | p.38                   | Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics                |
|              |   | p.48, 50 to 52, 55, 59 | Modification of Caution in 2.5.1 Serial array unit   |
|              |   | p.64 to 69             | Modification of conditions of 2.6.1 A/D converter characteristics                                |
|              |   | p.72                   | Renamed to 2.7 RAM Data Retention Characteristics, and modification of note and figure           |
| p.72         | Modification of 2.8 Flash Memory Programming Characteristics  |                        |  |

| Rev.  | Date                                | Description                   |  |
|-------|-------------------------------------|-------------------------------|--|
|       |                                     | Page                          | Summary  |
| 2.10  | Nov 30, 2016                        | p.73                          | Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes         |
|       |                                     | p.77                          | Modification of 3.2.1 X1, XT1 oscillator characteristics                               |
|       |                                     | p.78, 79                      | Modification of 3.3.1 Pin characteristics  |
|       |                                     | p.88                          | Modification of 3.3.2 Supply current characteristics                                   |
|       |                                     | p.90                          | Modification of Minimum Instruction Execution Time during Main System Clock Operation  |
|       |                                     | p.91                          | Modification of AC Timing Test Points and TI/TO Timing                                 |
|       |                                     | p.93                          | Modification of AC Timing Test Points in 3.5 Peripheral Functions Characteristics      |
|       |                                     | p.95                          | Modification of 3.5.1 Serial array unit  |
|       |                                     | p.99, 100, 102, 103, 105, 109 | Modification of Caution in 2.5.1 Serial array unit                                     |
|       |                                     | p.112 to 116                  | Modification of 3.6.1 (1) to (5)   |
|       |                                     | p.118                         | Renamed to 3.7 RAM Data Retention Characteristics, and modification of note and figure |
|       |                                     | p.118                         | Addition of note 4 to 3.8 Flash Memory Programming Characteristics                     |
|       |                                     | p.119                         | Modification of 3.10 Timing Specs for Switching Flash Memory Programming Modes         |
|       |                                     | p.120                         | Modification of 4.1 25-pin products  |
| p.123 | Modification of 4.3 48-pin products |                               |  |

All trademarks and registered trademarks are the property of their respective owners

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

|  |
|--|
| Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc. |
|--|

## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.



## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.  
Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

#### Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

#### Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

#### Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics India Pvt. Ltd.

No.77C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

#### Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## Renesas Electronics:

[R5F10ELCAFB#V0](#) [R5F10EGCANA#U0](#) [R5F10EGEAFB#V0](#) [R5F10EBEANA#U0](#) [R5F10EGCAFB#V0](#)  
[R5F10E8EALA#U0](#) [R5F10ELDABF#V0](#) [R5F10FLCANA#U0](#) [R5F10FMDAFB#V0](#) [R5F10FMCAFB#V0](#)  
[R5F10FMEAFB#V0](#) [R5F10ELDABG#U0](#) [R5F10EGCGFB#V0](#) [R5F10EGEANA#U0](#) [R5F10EGEGFB#V0](#)  
[R5F10E8CALA#U0](#) [R5F10EGDANA#U0](#) [R5F10FLDANA#U0](#) [R5F10FLEANA#U0](#) [R5F10EGDAFB#V0](#)  
[R5F10ELCABG#U0](#) [R5F10ELEAFB#V0](#) [R5F10ELEGFB#V0](#) [R5F10EBAANA#U0](#) [R5F10EGAANA#U0](#)  
[R5F10E8AALA#U0](#) [R5F10ELEABG#U0](#) [R5F10E8DALA#U0](#) [R5F10EBCANA#U0](#) [R5F10EBDANA#U0](#)  
[R5F10EGAAFB#V0](#) [R5F10ELEGFB#X0](#) [R5F10E8AALA#W0](#) [R5F10E8AGLA#U0](#) [R5F10E8AGLA#W0](#)  
[R5F10E8CALA#W0](#) [R5F10E8CGLA#U0](#) [R5F10E8CGLA#W0](#) [R5F10ELEGBG#U0](#) [R5F10ELEGBG#W0](#)  
[R5F10ELDGBG#U0](#) [R5F10ELDGBG#W0](#) [R5F10ELDGFB#V0](#) [R5F10ELDGFB#X0](#) [R5F10ELEABG#W0](#)  
[R5F10ELEAFB#X0](#) [R5F10ELCGBG#U0](#) [R5F10ELCGBG#W0](#) [R5F10ELCGFB#V0](#) [R5F10ELCGFB#X0](#)  
[R5F10ELDABG#W0](#) [R5F10ELDABF#X0](#) [R5F10EGEANA#W0](#) [R5F10EGEGFB#X0](#) [R5F10EGEGNA#U0](#)  
[R5F10EGEGNA#W0](#) [R5F10ELCABG#W0](#) [R5F10ELCAFB#X0](#) [R5F10EGDANA#W0](#) [R5F10EGDGFB#W0](#)  
[R5F10EGDGFB#X0](#) [R5F10EGDGNA#U0](#) [R5F10EGDGNA#W0](#) [R5F10EGEAFB#X0](#) [R5F10EGCAFB#X0](#)  
[R5F10EGCANA#W0](#) [R5F10EGCGFB#X0](#) [R5F10EGCGNA#U0](#) [R5F10EGCGNA#W0](#) [R5F10EGDAFB#X0](#)  
[R5F10EGAAFB#X0](#) [R5F10EGAANA#W0](#) [R5F10EGAGFB#V0](#) [R5F10EGAGFB#X0](#) [R5F10EGAGNA#U0](#)  
[R5F10EGAGNA#W0](#) [R5F10EBDANA#W0](#) [R5F10EBDGNA#U0](#) [R5F10EBDGNA#W0](#) [R5F10EBEANA#W0](#)  
[R5F10EBEGNA#U0](#) [R5F10EBEGNA#W0](#) [R5F10EBAANA#W0](#) [R5F10EBAGNA#U0](#) [R5F10EBAGNA#W0](#)  
[R5F10EBCANA#W0](#) [R5F10EBCGNA#U0](#) [R5F10EBCGNA#W0](#) [R5F10E8DALA#W0](#) [R5F10E8DGLA#U0](#)  
[R5F10E8DGLA#W0](#) [R5F10E8EALA#W0](#) [R5F10E8EGLA#U0](#) [R5F10E8EGLA#W0](#)

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,  
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А