FXLS8471Q

3-Axis, Linear Accelerometer

Rev. 3.0 — 13 June 2019 Product data sheet

1 General description

FXLS8471Q is a small, low-power, 3-axis, linear accelerometer in a 3 mm x 3 mm x 1 mm QFN package. FXLS8471Q has dynamically selectable acceleration full-scale ranges of ±2 *g*/±4 *g*/±8 *g* and 14 bits of resolution. Output data rates (ODR) are programmable from 1.563 Hz to 800 Hz. I^2C and SPI serial digital interfaces are provided along with several user programmable event detection functions that can be used to reduce the overall system power consumption by off-loading the host processor. FXLS8471Q is guaranteed to operate over the extended temperature range of –40 °C to +105 °C.

2 Features and benefits

- 1.95 V to 3.6 V VDD supply voltage, 1.62 V to 3.6 V VDDIO voltage
- ±2 *g*/±4 *g*/±8 *g* dynamically selectable acceleration full-scale ranges
- Output Data Rates (ODR) from 1.563 Hz to 800 Hz
- Low noise: typically 99 µg/Hz in low-noise mode @ 200-Hz bandwidth
- 14-bit ADC resolution: 0.244 mg/LSB in ±2 *g* full-scale range
- Embedded programmable acceleration event functions
  - Freefall and motion detection
  - Transient detection
  - Vector-Magnitude change detection
  - Pulse and tap detection (single and double)
  - Orientation detection (portrait/landscape)
- Programmable automatic ODR change using Auto-Wake and return to Sleep functions to save power
- 192-byte FIFO buffer, capable of storing up to 32 samples of X/Y/Z data
- Supports SPI interface at up to 1 MHz; I^2C Normal (100 kHz) and Fast modes (400 kHz)
- Integrated self-test function
- Integrated temperature sensor with 8-bit output resolution

3 Typical applications

Automotive convenience and security

- Tilt sensing, orientation detection, vibration sensing
- Navigation applications

Industrial IOT

- Asset tracking
- Equipment monitoring: vibration analysis, machine health

Medical

- Patient and activity monitors

Consumer devices

- Wearables
- Portable electronics

4 Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
FXLS8471Q	–40 °C to +105 °C	VQFN16	plastic, very thin quad flatpack; no leads; 16 terminals; 0.5 mm pitch; 3 mm x 3 mm x 1 mm body	SOT1676-1

5 Block Diagram

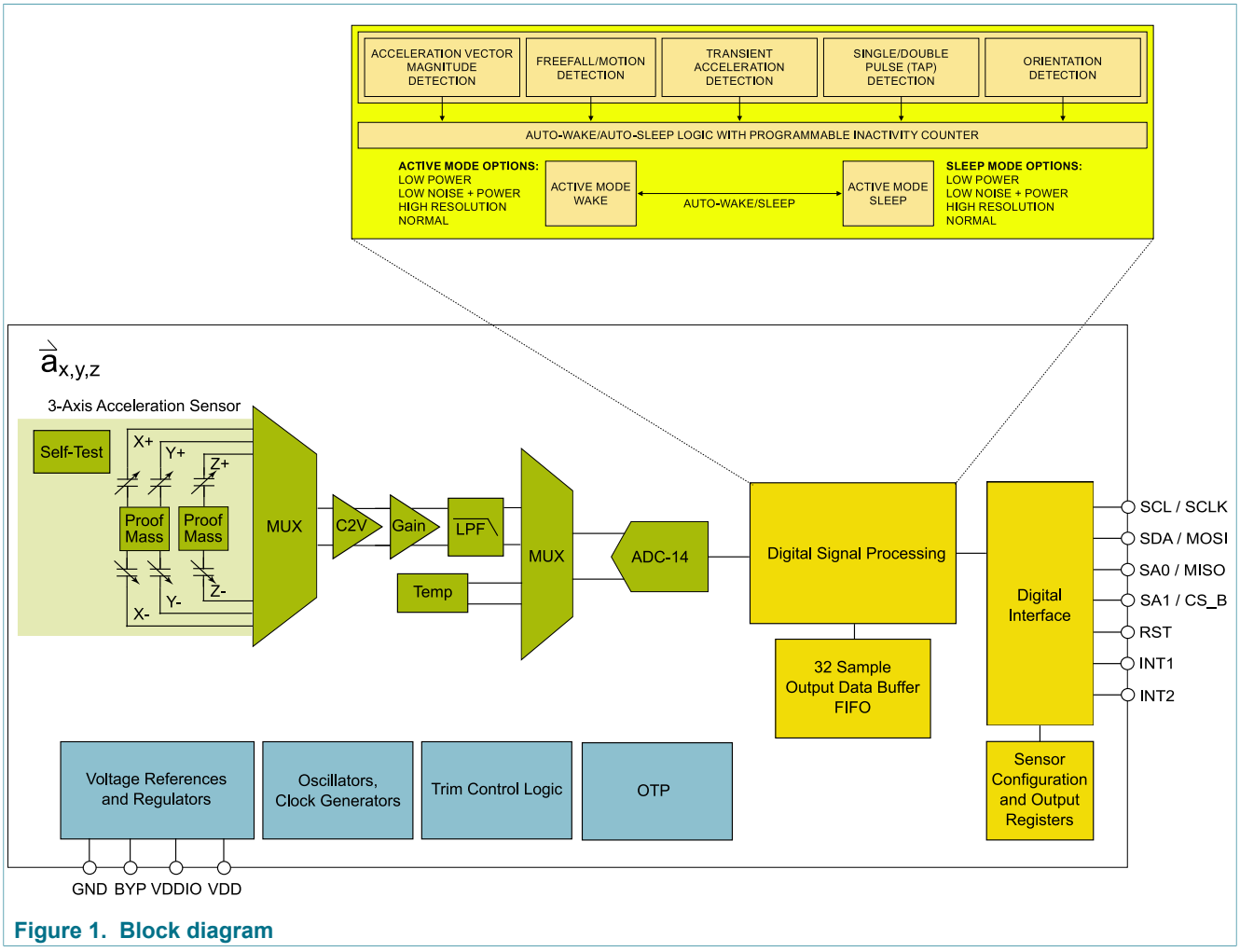


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

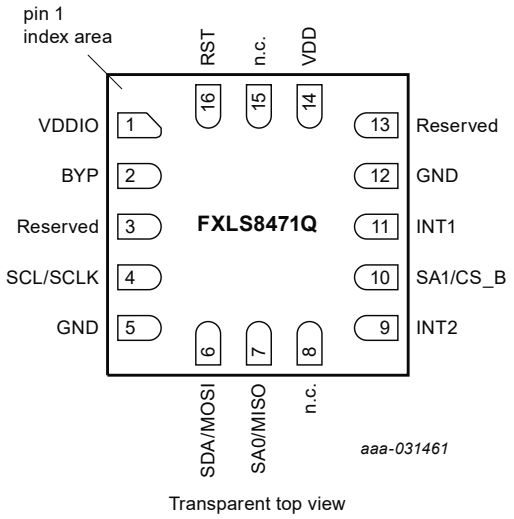


Figure 2. Pinning

6.2 Pin description

Table 2. Pin Description

Symbol	Pin	Description
VDDIO	1	Interface power supply
BYP	2	Internal regulator output bypass capacitor connection
Reserved	3	Test reserved, connect to GND
SCL/SCLK	4	I^2C Serial Clock/SPI Clock
GND	5	Ground
SDA/MOSI	6	I^2C Serial Data/SPI Master Out, Slave In
SA0/MISO[1]	7	I^2C address selection bit 0/SPI Master In, Slave Out
n.c.	8	Internally not connected
INT2	9	Interrupt 2
SA1/CS_B	10	I^2C address selection bit 1[2]/SPI Chip Select (active low)
INT1	11	Interrupt 1
GND	12	Ground
Reserved	13	Test reserved, connect to GND
VDD	14	Power supply
N/C	15	Internally not connected
RST	16	Reset input, active high. Connect to GND if unused

[1] The SA0 pin is also used to select the desired serial interface mode during POR and also after a hard/soft reset event. See Section 10.2.3 for more information

[2] See Table 4 for I^2C address options selectable using the SA0 and SA1 pins.

7 Orientation

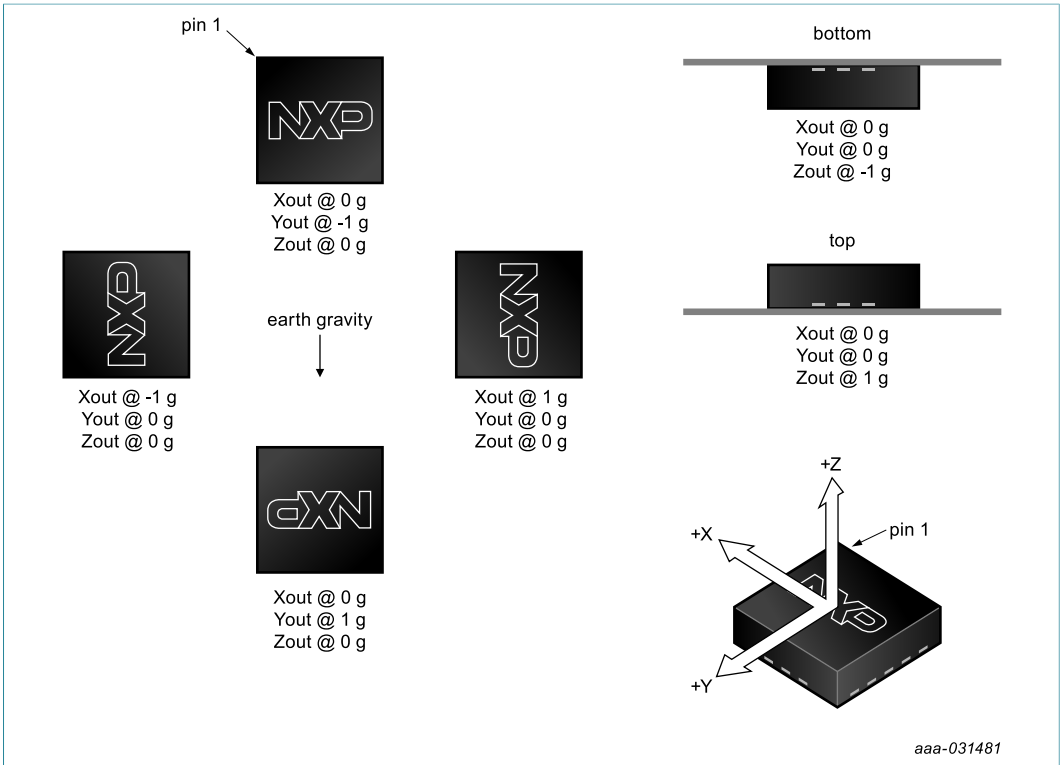


Figure 3. Product orientation and axis orientation

8 Electrical connections

Device power is supplied through the VDD pin. Power supply decoupling capacitors (100 nF ceramic plus 4.7 µF bulk) should be placed as close as possible to pin 14 of the device. The digital interface supply voltage (VDDIO) should be decoupled with a 100 nF ceramic capacitor placed as close as possible to pin 1 of the device.

The digital control signals SCL, SDA, SA0, SA1 and RST are not tolerant of voltages exceeding VDDIO + 0.3 V. If VDDIO is removed, these pins will clamp any logic signals through their internal ESD protection diodes.

The function and timing of the two interrupt pins (INT1 and INT2) are user programmable through the I^2C/SPI interface. The SDA and SCL I^2C connections are open drain and therefore require a pullup resistor as shown in the application diagram in Figure 4. The INT1 and INT2 pins may also be configured for open-drain operation. If they are configured for open drain, external pullup resistors are required.

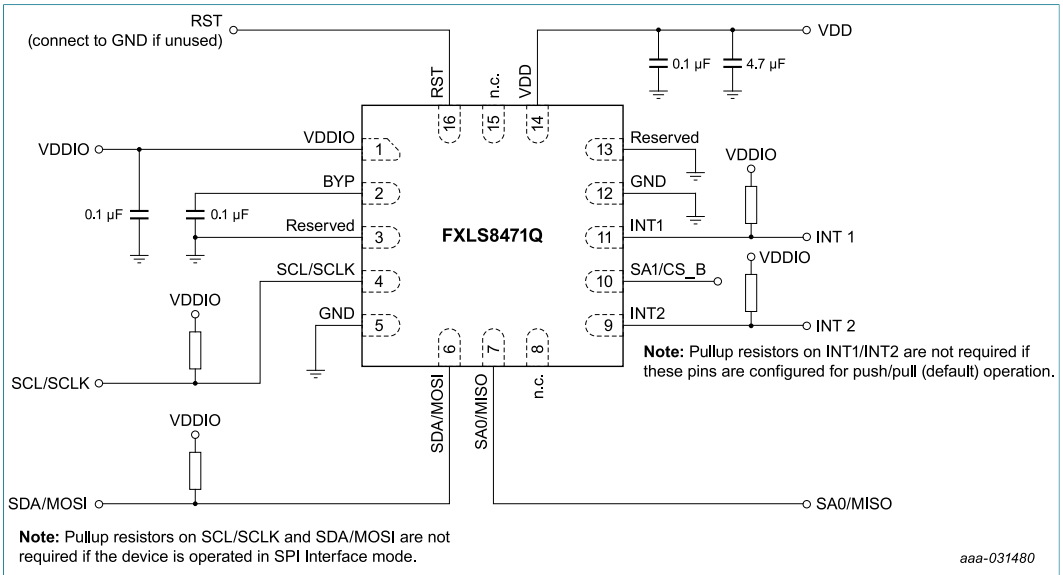


Figure 4. Electrical connection

9 Terminology

9.1 Sensitivity

Sensitivity is represented in mg/LSB; the accelerometer sensitivity changes with the full-scale range selected by the user. Accelerometer sensitivity is 0.244 mg/LSB in 2 *g* mode, 0.488 mg/LSB in 4 *g* mode, and 0.976 mg/LSB in 8 *g* mode.

9.2 Zero-*g* offset

Zero-*g* offset describes the deviation of an actual output signal from the ideal output signal while the sensor is stationary. A sensor stationary on a horizontal surface will measure 0 *g* in X-axis and 0 *g* in Y-axis, whereas the Z-axis will measure 1 *g*. A deviation from an ideal value in this case is called *Zero-g offset*. Offset is, to some extent, a result of stress on the MEMS sensor. Therefore, the offset can slightly change after mounting the sensor onto a printed circuit board, or after exposure to extensive mechanical stress.

9.3 Self-test

Self-test can be used to verify the transducer and signal chain functionality without the need to apply an acceleration stimulus. When the accelerometer self-test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case the sensor X, Y, and Z outputs will exhibit a change in DC levels related to the selected full-scale range (sensitivity). When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic self-test force.

10 Digital interfaces

10.1 I²C interface characteristics

Table 3. I²C slave timing values[1]

Symbol	Parameter	I²C fast mode		Unit
		Min	Max	
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	Bus free time between stop and start condition	1.3	—	µs
$t_{HD;STA}$	(Repeated) start hold time	0.6	—	µs
$t_{SU;STA}$	(Repeated) start setup time	0.6	—	µs
$t_{SU;STO}$	STOP condition setup time	0.6	—	µs
$t_{HD;DAT}$	SDA data hold time [2]	0.05	0.9	µs
$t_{VD;DAT}$	SDA valid time [2] [3]	—	0.9	µs
$t_{VD;ACK}$	SDA valid acknowledge time [2] [4]	—	0.9	µs
$t_{SU;DAT}$	SDA setup time	100	—	ns
t_{LOW}	SCL clock low time	1.3	—	µs
t_{HIGH}	SCL clock high time	0.6	—	µs
t_r	SDA and SCL rise time [5]	20 + 0.1 C_b	300	ns
t_f	SDA and SCL fall time [5]	20 + 0.1 C_b	300	ns
t_{SP}	Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	0	50	ns

[1] All values referred to VIH (min) and VIL (max) levels
[2] This device does not stretch the low period (t_{LOW}) of the SCL signal.
[3] $t_{VD;DAT}$ = time for data signal from SCL low to SDA output.
[4] $t_{VD;ACK}$ = time for acknowledgement signal from SCL low to SDA output (high or low, depending on which one is worse)
[5] C_b = total capacitance of one bus line in pF.

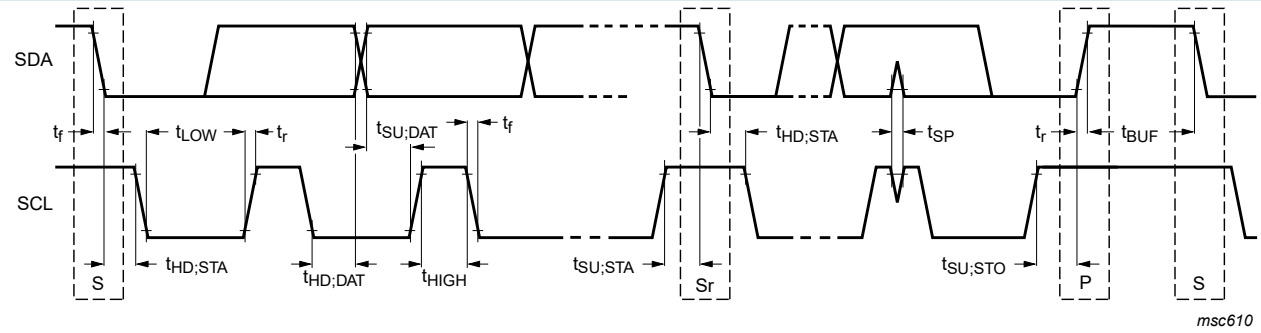


Figure 5. I²C slave timing diagram

10.1.1 General I²C operation

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I²C interface

is compliant with fast mode (400 kHz), and normal mode (100 kHz) I^2C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See Table 4 for more information.

A transaction on the bus is started through a start condition (ST) signal, which is defined as a high-to-low transition on the data line while the SCL line is held high. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all master devices recognize clock stretching. This device does not employ clock stretching.

A low to high transition on the SDA line while the SCL line is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer

The slave addresses that may be assigned to the FXLS8471Q part are 1Ch, 1Dh, 1Eh, or 1Fh. The selection is made through the logic level of the SA1 and SA0 inputs, as shown in Table 4.

Table 4. I^2C slave address

SA1	SA0	Slave address
0	0	1Eh
0	1	1Dh
1	0	1Ch
1	1	1Fh

10.1.2 I^2C read/write operations

Single-byte read

The master (or MCU) transmits a start condition (ST) to the FXLS8471Q, followed by the slave address, with the R/W bit set to "0" for a write, and the FXLS8471Q sends an acknowledgment. Then the master (or MCU) transmits the address of the register to read and the FXLS8471Q sends an acknowledgment. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXLS8471Q then acknowledges and

transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

Multiple-byte read

When performing a multi-byte or burst read, the FXLS8471Q automatically increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXLS8471Q acknowledgment (AK) is received until a no acknowledge (NAK) occurs from the master followed by a stop condition (SP) signaling an end of transmission.

Single-byte write

To start a write command, the master transmits a start condition (ST) to the FXLS8471Q, followed by the slave address with the R/W bit set to "0" for a write, and the FXLS8471Q sends an acknowledgment. Then the master (or MCU) transmits the address of the register to write to, and the FXLS8471Q sends an acknowledgment. Then the master (or MCU) transmits the 8-bit data to write to the designated register and the FXLS8471Q sends an acknowledgment that it has received the data. Because this transmission is complete, the master transmits a stop condition (SP) to end the data transfer. The data sent to the FXLS8471Q is now stored in the appropriate register.

Multiple-byte write

The FXLS8471Q automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXLS8471Q acknowledgment (ACK) is received.

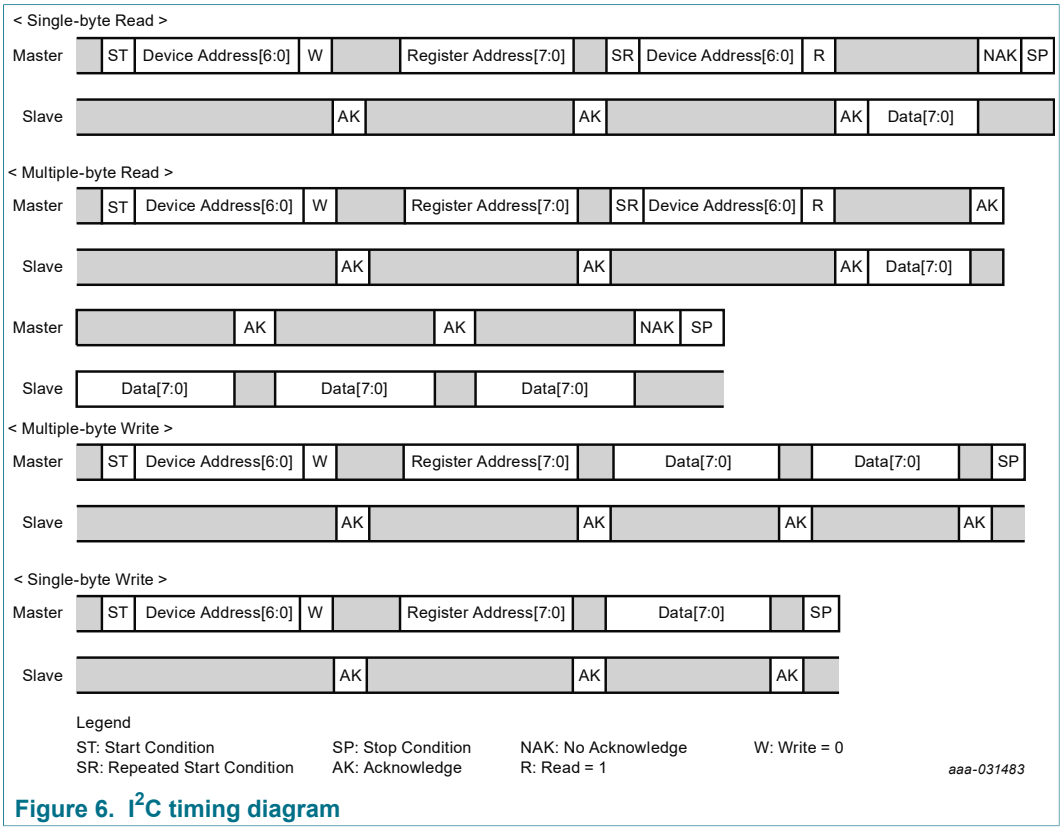


Figure 6. I²C timing diagram

10.2 SPI interface characteristics

SPI interface is a classical master/slave serial port. The FXLS8471Q is always considered as the slave and thus is never initiating the communication.

Table 5 and Figure 7 describe the timing requirements for correct operation.

Table 5. SPI timing

Function	Symbol	Min	Max	Unit
Operating Frequency	Of	—	1	MHz
SCLK Period	tSCLK	1000	—	ns
SCLK High time	tCLKH	500	—	ns
SCLK Low time	tCLKL	500	—	ns
CS_B lead time	tSCS	65	—	ns
CS_B lag time	tHCS	65	—	ns
MOSI data setup time	tSET	25	—	ns
MOSI data hold time	tHOLD	75	—	ns
MISO data valid (after SCLK low edge)	tDDLY	—	500	ns
Width CS High	tWCS	100	—	ns

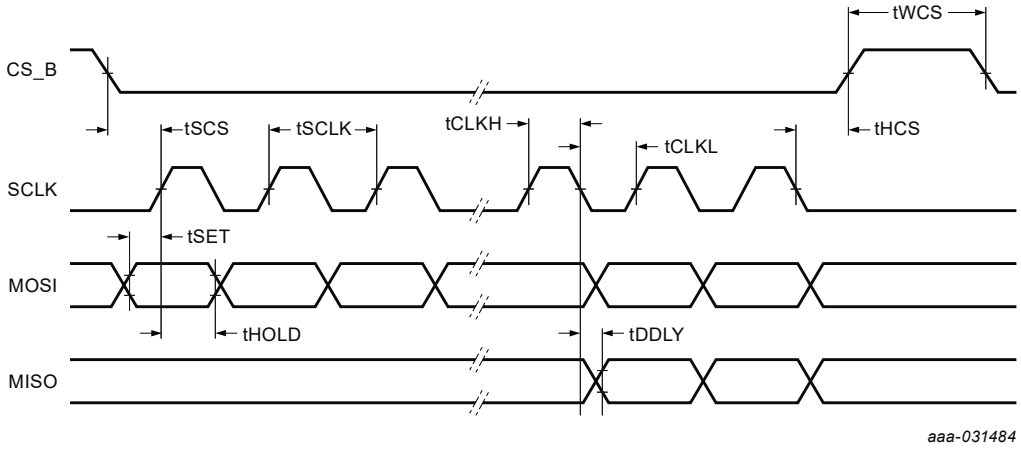


Figure 7. SPI timing diagram

10.2.1 General SPI operation

The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.

A write operation is initiated by transmitting a 1 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Data to be written starts in the third serialized byte. The order of the bits is as follows:

Byte 0: R/W,ADDR[6],ADDR[5],ADDR[4],ADDR[3],ADDR[2],ADDR[1],ADDR[0],
Byte 1: ADDR[7],X,X,X,X,X,X,X,
Byte 2: DATA[7],DATA[6],DATA[5],DATA[4],DATA[3],DATA[2],DATA[1],DATA[0].

Multiple bytes of DATA can be transmitted. The X indicates a bit that is ignored by the part. The register address is auto-incremented, so that the next clock edges will latch the data for the next register. When desired, the rising edge on CS_B stops the SPI communication.

The FXLS8471Q SPI configuration is as follows:

- Polarity: rising/falling
- Phase: sample/setup
- Order: MSB first

Data is sampled during the rising edge of SCLK and set up during the falling edge of SCLK.

10.2.2 SPI READ/WRITE operations

A READ operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits are ignored by the part. The read data is deserialized from the MISO pin.

Similarly a WRITE operation is initiated by transmitting a 1 for the R/W bit. After the first and second serialized bytes multiple-data bytes can be transmitted into consecutive registers, starting from the indicated register address in ADDR[7:0].

A SPI transaction is started by asserting the CS_B pin (high-to-low transition), and ended by deasserting the CS_B pin (low-to-high transition).

R/W bit followed by ADDR[6:0]	ADDR[7] followed by 7 ''don't care'' bits	Data0	Data1	-	Datan

(1) Data bytes must be transmitted to the slave (FXLS8471Q) using the MOSI pin by the master when R/W = 1. Data bytes will be transmitted by the slave (FXLS8471Q) to the master using the MISO pin when R/W = 0. The first two bytes are always transmitted by the master using the MOSI pin. That is, a transaction is always initiated by master.

aaa-032115

Figure 8. SPI single-burst read/write transaction diagram

The registers embedded inside FXLS8471Q are accessed through either an I^2C, or a SPI serial interface. To enable either interface the VDDIO line must be connected to the interface supply voltage. If VDD is not present and VDDIO is present FXLS8471Q is in shutdown mode and communications on the interface are ignored. If VDDIO is held high, VDD can be powered off and the communications pins will be automatically placed in a high impedance state. This will allow communications to continue on the bus with other devices while the FXLS8471Q is powered down.

Table 6. Serial interface pin descriptions

Pin Name	Pin Description
VDDIO	Digital interface power
SA1/CS_B	I^2C second least significant bit of device address/SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI	I^2C serial data/SPI master serial data out slave serial data in
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave out

10.2.3 I^2C/SPI auto detection

FXLS8471Q employs an interface mode auto-detection circuit that will select either I^2C or SPI interface mode based on the state of the SA0 pin during power up or when exiting reset. Once set for I^2C or SPI operation, the device will remain in I^2C or SPI mode until the device is reset or powered down and the auto-detection process is repeated. Note that when SPI interface mode is desired, care must be taken to ensure that no other slave device drives the common SA0/MISO pin during the 1 ms period after a hard or soft reset or power-up event.

Table 7. I^2C/SPI auto detection

SA0	Interface mode
GND	I^2C
VDDIO	I^2C
Floating	SPI

10.2.4 Power supply sequencing and I^2C/SPI mode auto-detection

FXLS8471Q does not have any specific power supply sequencing requirements between VDD and VDDIO voltage supplies to ensure correct power-up and operation. To ensure correct operation of the I^2C/SPI auto-detection function, VDDIO should be applied before or at the same time as VDD. If this order cannot be maintained, the user should either pulse the RST line high or power cycle the VDD rail in order to force the auto-detect function to restart and correctly identify the desired interface. FXLS8471Q will indicate completion of the reset sequence by toggling the INT1 pin from logic high to low to high over a 500 ns period. If the INT1 pin was already low prior to the reset event, it will only go high, and not toggle.

11 Absolute maximum ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Maximum ratings

Symbol	Rating	Value	Unit
g_{max}	Maximum acceleration (all axes, 100 µs)	5000	*g*
VDD_{max}	Supply voltage, interface supply voltage	–0.3 to +3.6	V
$VDDIO_{max}$	Supply voltage, IO voltage	–0.3 to +3.6	V
VIN_{max}	Input voltage on any control pin (SA0/MISO, SA1/CS_B, SCL/SCLK, SDA/MOSI, RST)	–0.3 to VDDIO + 0.3	V
D_{drop}	Drop-test height	1.8	m
T_{STG}	Storage temperature range	–40 to +125	°C

Table 9. ESD and latchup protection characteristics

Symbol	Rating	Value	Unit
HBM	Human body model	±2000	V
MM	Machine model	±200	V
CDM	Charge device model	±500	V
I_{LU}	Latchup current at T = 105 °C (per AEC-Q100-004)	±100	mA

CAUTION

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part or cause the part to otherwise fail.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Improper handling can cause permanent damage to the part.

12 Mechanical characteristics

Table 10. Mechanical characteristics

VDD = 1.8 to 3.3 V, VDDIO = 1.8 V, T = 25 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Parameter	Test conditions	Symbol	Min	Typ	Max	Unit
Measurement range[1]	±2 *g* mode	FSR		±2		*g*
	±4 *g* mode			±4		
	±8 *g* mode			±8		
Sensitivity	±2 *g* mode, –40°C to 105°C	SEN	3686	4096	4506	LSB/*g*
			0.220	0.244	0.268	mg/LSB
	±4 *g* mode, –40°C to 105°C		1843	2048	2253	LSB/*g*
			0.439	0.488	0.537	mg/LSB
	±8 *g* mode, –40°C to 105°C		922	1024	1126	LSB/*g*
			0.878	0.976	1.074	mg/LSB
Sensitivity change with temperature[1]	±2 *g*, ±4 *g*, ±8 *g* modes	TCS		±0.01		%/°C
Sensitivity accuracy	@ 25°C	SEN-TOL	–10	±2.5	+10	%SEN
Zero-*g* level offset accuracy[2]	±2 *g*, ±4 *g*, ±8 *g* ranges, 25 °C	OFF_{RT}		±20		mg
	±2 *g* range, –40 °C to 105 °C	OFF_{OT-2G}	–80		+80	
Zero-*g* level offset accuracy post-board mount[3]	±2 *g*, ±4 *g*, ±8 *g* modes	OFF_{PBM}		±30		mg
Zero-*g* level change versus temperature[1]	–40°C to 85°C	TCO_{TR1}		±0.2		mg/°C
	–40°C to 105°C	TCO_{TR2}		±0.3		
Cross-axis sensitivity	Over ±1 *g* range in Normal mode	CAS		±0.5		%FS
Nonlinearity (deviation from straight line)[4][5]	Over ±1 *g* range in Normal mode	NL		±0.5		%FSR
Self-Test output change[6] X Y Z	±2 *g* range, –40 °C to 105 °C	$STOC_{OT}$	192 270 1275		1000 1000 6000	LSB
Output noise density[4][7]	ODR = 400 Hz, normal mode	ND_{NM}		126		µg/√Hz
	ODR = 400 Hz, low-noise mode[1]	ND_{LNM}		99		µg/√Hz
Operating temperature range		Top	–40		+105	°C

[1] Dynamic range is limited to ±4 *g* when in the low-noise mode.
[2] Before board mount.
[3] Post-board mount offset specifications are based on a 2-layer PCB design.
[4] Determined through bench evaluation (small number of typical devices measured at room temperature).
[5] After post-board mount corrections for sensitivity, cross axis and offset. Refer to AN4399 for more information.
[6] Self-test is only exercised along one direction for each sensitive axis.
[7] Measured using earth's gravitational field (1 *g*) with the device oriented horizontally (+Z axis up) and stationary.

13 Electrical characteristics

Table 11. Electrical characteristics

VDD = 1.8 to 3.3 V, VDDIO = 1.8 V, T = 25 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage		VDD	1.95	3.3	3.6	V
Interface supply voltage		VDDIO	1.62	3.3	3.6	V
I_{DD} in low-power mode, 25 °C	ODR = 12.5 Hz	Idd_{LPM-RT}		8		µA
	ODR = 100 Hz			35		
	ODR = 400 Hz			130		
I_{DD} in normal mode, 25 °C	ODR = 50 Hz	Idd_{NM-RT}		35		µA
	ODR = 200 Hz			130		
	ODR = 800 Hz			240		
I_{DD} in normal mode, –40 °C to 105 °C	ODR = 400 Hz	Idd_{NM-OT}			150	µA
	ODR = 800 Hz				274	
Peak current during boot sequence	VDD = 2.5 V; 25 °C; 1ms max duration, using the recommended bypass capacitors	Idd_{BOOT}			3	mA
Value of capacitor on BYP pin	–40°C to 105°C	C_{BYP}	75	100	470	nF
Standby mode current, 25°C	Standby mode	$Idd_{STBY-RT}$		2		µA
Standby mode current, –40 °C to 105 °C	Standby mode; –40 to +105 °C	$Idd_{STBY-OT}$			13.5	µA
Digital high-level input voltage RST pin		VIH_{RST}	1.04			V
Digital low-level input voltage RST pin		VIL_{RST}			0.68	V
Digital high-level input voltage SCL/SCLK, SDA/MOSI, SA0/MISO, SA1/CS_B		VIH	0.75*VDDIO			V
Digital low-level input voltage SCL/SCLK, SDA/MOSI, SA0/MISO, SA1/CS_B		VIL			0.3*VDDIO	V
High-level output voltage INT1, INT2, SDA/MOSI	I_O = 500 µA	VOH	0.9*VDDIO			V
Low-level output voltage INT1, INT2, SDA/MOSI	I_O = 500 µA	VOL			0.1*VDDIO	V
SCL, SDA pin leakage	25°C			1.0		nA
	–40°C to 105°C			10		
SCL, SDA pin capacitance				3		pf
VDD rise time			0.001		1000	ms
Boot time[1]		T_{BOOT}			1000	µs
Turn-on time 1[2]		$T_{POR→ACT}$		2/ODR + 2		ms
Turn-on time 2[3]		$T_{STBY→ACT}$		2/ODR + 1		ms
ODR accuracy				±2		%
Operating temperature range		T_{OP}	–40		+105	°C

[1] Time from VDDIO on and VDD > VDD min until I^2C/SPI interface ready for operation.
[2] Time to obtain valid data from power-down mode to Active mode.
[3] Time to obtain valid data from Standby mode to Active mode.

14 Temperature sensor characteristics

Table 12. Temperature characteristics

VDD = 1.8 to 3.3 V, VDDIO = 1.8 V, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Parameter	Test conditions	Symbol	Min	Typ	Max	Unit
Output data width	—	n_{TEMP}		8		bits
Measurement range	—	FSR_{TEMP}		–40 to +125		°C
Sensitivity	—	SEN_{TEMP}		0.96		°C/LSB
Sensitivity tolerance	—	$SEN_{TOL-TEMP}$		±2.5		%
Nominal ambient temperature at zero output code	TEMP_OUT = 00h			25		°C

15 Modes of operation

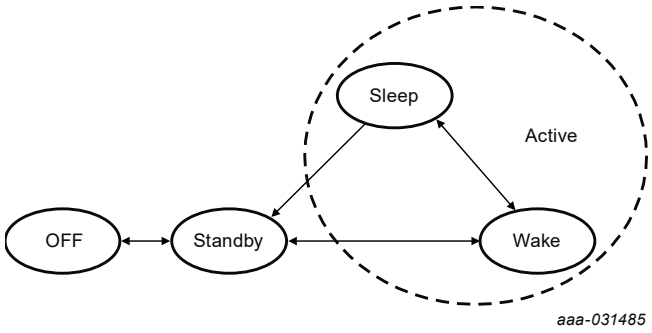


Figure 9. FXLS8471Q power mode transition diagram

Table 13. Mode of operation description

Mode	I^2C/SPI Bus state	VDD	VDDIO	Function description
OFF	Powered down	< 1.8 V	VDDIO can be > VDD	The device is powered off. All analog and digital blocks are shutdown. I^2C bus inhibited.
Standby	I^2C/SPI communication with FXLS8471Q is possible	ON	VDDIO = High VDD = High Active bit is cleared	Only digital blocks are enabled. Analog subsystem is disabled. Internal clocks disabled.
Active (Wake/Sleep)	I^2C/SPI communication with FXLS8471Q is possible	ON	VDDIO = High VDD = High Active bit is set	All blocks are enabled (digital and analog).

All register contents are preserved when transitioning from Active to Standby mode, but some registers are reset when transitioning from Standby to Active. These registers are noted in Table 1. The Sleep and Wake modes are active modes. For more information on how to use the Sleep and Wake modes and configuring the device to transition between them, refer to Section 16 "Embedded functionality" or NXP application note AN4074.

16 Embedded functionality

FXLS8471Q is a low-power, digital output, 3-axis sensor with both I^2C and SPI interfaces. Extensive embedded functionality is provided to detect inertial events at low power, with the ability to notify the host processor of an event using either of the two programmable interrupt pins. The embedded functionality includes:

- 8-bit or 14-bit acceleration data that includes high-pass filtered data, including the option to employ a high-pass filter on the output.
- Four different oversampling options for the output data. The oversampling settings allow the end user to optimize the resolution (noise) versus power trade-off in a given application.
- A low-noise mode that functions independently of the oversampling modes for even higher resolution
- Low-power, auto-wake/sleep function for conserving power in portable battery powered applications
- Pulse-detection circuit, which can be used to detect directional single and double taps
- Directional motion-event and free-fall-event detection with programmable threshold and debounce time
- Transient detection with programmable threshold and debounce time. Transient detection can employ either a high-pass filter or use the difference between reference and current sample values.
- Orientation detection with programmable hysteresis for smooth transitions between portrait/landscape orientations
- Vector-magnitude change event detection with programmable reference, threshold, and debounce time values

Many different configurations of the above functions are possible to suit the needs of the end application. Separate application notes are available to further explain the different configuration settings and potential use cases.

16.1 Factory calibration

FXLS8471Q is factory calibrated for sensitivity and offset on each axis. The trim values are stored in NonVolatile Memory (NVM). On startup, the trim parameters are read from NVM and applied to the internal compensation circuitry. After mounting the device to the PCB, the user can further adjust the accelerometer offsets through the OFF_X/Y/Z registers. For more information on accelerometer calibration, refer to NXP application note AN4069.

16.2 8-bit or 14-bit data

The measured acceleration data is stored in the OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB registers as two's complement 14-bit numbers. The most significant 8-bits of each axis are stored in the OUT_X/Y/Z_MSB registers, so applications needing only 8-bit results simply read these three registers and ignore the OUT_X/Y/Z_LSB registers. To do this, the *f_read* mode bit in CTRL_REG1 must be set.

When the full-scale range is set to 2 *g*, the measurement range is –2 *g* to +1.999 *g*, and each count corresponds to 0.244 mg at ±14-bits resolution. When the full-scale is set to 8 *g*, the measurement range is –8 *g* to +7.996 *g*, and each count corresponds to 0.976 mg. The resolution is reduced by a factor of 64 if only the 8-bit results are used

(CTRL_REG1[*f_read*] = 1). For further information on the different data formats and modes, please refer to NXP application note AN4076.

16.3 Low-power modes versus high-resolution modes

FXLS8471Q can be optimized for lower power or higher resolution of the accelerometer output data. High resolution is achieved by setting the lnoise bit in register 2Ah. This improves the resolution (by lowering the noise), but be aware that the dynamic range becomes fixed at ±4 *g* when this bit is set. This will affect all internal embedded functions (scaling of thresholds, etc.) and reduce noise. Another method for improving the resolution of the data is through oversampling. One of the oversampling schemes of the output data can be activated when CTRL_REG2[*mods*] = 0b, which improves the resolution of the output data without affecting the internal embedded functions or usable dynamic range.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When CTRL_REG2[*mods*] = 0b, the lowest power is achieved, at the expense of higher noise. In general, the lower the selected ODR and OSR, the lower the power consumption. For more information on how to configure the device in low-power or high-resolution modes and understand the benefits and trade-offs, please refer to NXP application note AN4075.

16.4 Auto-Wake and Auto-Sleep modes

FXLS8471Q can be configured to transition between sample rates (with their respective current consumptions) based on the status of the embedded interrupt event generators in the device. The advantage of using the auto-wake/sleep is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the sleep mode (lower current) when the device does not require higher sampling rates. Auto-wake refers to the device being triggered by one of the interrupt event functions to transition to a higher sample rate. This may also interrupt the processor to transition from a sleep mode to a higher power mode.

Sleep mode occurs when none of the enabled interrupt event functions has detected an interrupt within the user-defined, time-out period. The device will then transition to the specified lower sample rate. It can also alert the processor to go into a lower power mode to save power during this period of inactivity. Refer to AN4074 for more detailed information on configuring the Auto-Wake/Sleep function.

16.5 Free-fall and Motion event detection

The freefall/motion detection block can be configured to detect low-g (freefall) or high-g (motion) events utilizing the A_FFMT_CFG[a_ffmt_oae] bit.

In low-g detect mode (A_FFMT_CFG[a_ffmt_oae] = 0) a low-g condition will need to occur on all enabled axes (ex. X, Y and Z) for the A_FFMT_SRC[a_ffmt_ea] bit to be affected. And, in high-g detect mode (A_FFMT_CFG[a_ffmt_oae] = 1) a high-g condition occurring in any of the enabled axes (ex. X, Y or Z) will suffice to affect the A_FFMT_SRC[a_ffmt_ea] bit.

The detection threshold(s) are programed in register 17h (A_FFMT_THS) for common threshold operation, and 73h to 78h (A_FFMT_THS_X/Y/Z) for individual axis threshold operation.

A_FFMT_CFG[a_ffmt_ele] bit determines the behavior of A_FFMT_SRC[a_ffmt_ea] bit in response to the desired acceleration event (low-g/high-g). When A_FFMT_CFG[a_ffmt_ele] = 1, the freefall or motion event is latched and the A_FFMT_SRC[a_ffmt_ea] flag can only be cleared by reading the A_FFMT_SRC register. When A_FFMT_CFG[a_ffmt_ele] = 0, freefall or motion events are not latched, and the A_FFMT_SRC[a_ffmt_ea] bit reflects the real-time status of the event detection.

A_FFMT_THS[a_ffmt_dbcntm] bit determines the debounce filtering behavior of the logic that sets the A_FFMT_SRC[a_ffmt_ea] bit. See Figure 17 for details.

It is possible to enable/disable each axis used in the freefall/motion detection function by configuring bits A_FFMT_CFG[a_ffmt_xefe], A_FFMT_CFG[a_ffmt_yefe], and A_FFMT_CFG[a_ffmt_zefe].

The freefall/motion detection function has the option to use a common 7-bit unsigned threshold for each of the X, Y, and Z axes, or individual unsigned 13-bit thresholds for each axis. When A_FFMT_THS_X_MSB[a_ffmt_ths_xyz_en] = 0, the 7-bit threshold value stored in register 17h is used as a common 7-bit threshold for the X, Y, and Z axes. When a_ffmt_ths_xyz_en = 1, each axis may be programmed with an individual 13-bit threshold (stored in the A_FFMT_X/Y/Z MSB and LSB registers).

16.5.1 Free fall detection

The detection of free fall involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is below a user-specified threshold for a user-definable amount of time. Typically, the usable threshold ranges are between ±100 mg and ±500 mg.

16.5.2 Motion detection

Motion detection is often used to alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold for a set amount of time, the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to indicate whether the condition exists for longer than a set amount of time (that is, 100 ms or longer). There is also directional data available in the source register to detect the direction of the motion that generated the interrupt. This is useful for applications such as directional shake or flick detection, and can also assist gesture detection algorithms by indicating that a motion gesture has started.

16.6 Transient detection

FXLS8471Q integrates an acceleration transient detection function that incorporates a high-pass filter. Acceleration data goes through the high-pass filter, eliminating the DC tilt/offset and low frequency acceleration changes. The high-pass filter cutoff can be set by the user to four different frequencies which are dependent on the selected output data rate. A higher cutoff frequency ensures that DC and slowly changing acceleration data will be filtered out, allowing only the higher frequencies to pass. The transient detection feature can be used in the same manner as the motion detection by bypassing the high-pass filter. There is an option in the configuration register to do this. This adds more flexibility to cover the various customer use cases.

Many applications use the accelerometer's static acceleration readings (that is, tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high-frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the dynamic acceleration. The transient detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (2Eh). Registers 1Dh to 20h are used for configuring the transient detection function. The source register contains directional data to determine the direction of the transient acceleration, either positive or negative. For further information of the embedded transient detection function along with specific application examples and recommended configuration settings, refer to NXP application note AN4461.

16.7 Pulse detection

FXLS8471Q has embedded single/double and directional pulse detection. This function employs several timers for programming the pulse width time and the latency between pulses. The detection thresholds are independently programmable for each axis. The acceleration data input to the pulse detection circuit can be put through both high and low-pass filters, allowing for greater flexibility in discriminating between pulse and tap events. The PULSE_SRC register provides information on the axis, direction (polarity), and single/double event status for the detected pulse or tap. For more information on how to configure the device for pulse detection, refer to NXP application note AN4072.

16.8 Orientation detection

FXLS8471Q has an embedded orientation detection algorithm with the ability to detect all six orientations. The transition angles and hysteresis are programmable, allowing for a smooth transition between portrait and landscape orientations.

The angle at which the device no longer detects the orientation change is referred to as the "Z-lockout angle". The device operates down to 29° from the flat position. All angles are accurate to ±2°.

For further information on the orientation detection function refer to NXP application note AN4068.

16.9 Acceleration vector-magnitude detection

FXLS8471Q incorporates an acceleration vector-magnitude change detection block that can be configured to generate an interrupt when the acceleration magnitude exceeds a preset threshold for a programmed debounce time. The function can be configured to operate in absolute or relative modes, and can also act as a wake to sleep or sleep-to-wake transition source. This function is useful for detecting acceleration transients when operated in absolute mode, or for detecting changes in orientation when operated in relative mode. Refer to NXP application note AN4692.

17 Register Map

Table 14. Register address map

Auto-Increment addresses:

A. *STATUS[f_mode] = 00, CTRL_REG1[f_read] = 0*

B. *STATUS[f_mode] > 00, CTRL_REG1[f_read] = 0*

C. *STATUS[f_mode] = 00, CTRL_REG1[f_read] = 1*

D. *STATUS[f_mode] > 00, CTRL_REG1[f_read] = 1*

Name	Type	Register address	Auto-increment address				Default hex value	Comment	
			A	B	C	D			
STATUS[1][2]	R	00h	01h				00h	Real-time, data-ready status or FIFO status (DR_STATUS or F_STATUS)	
OUT_X_MSB[1][2]	R	01h	02h	01h	03h	01h	—	[7:0] are 8 MSBs of 14-bit sample.	Root pointer to XYZ FIFO data.
OUT_X_LSB[1][2]	R	02h	03h		00h		—	[7:2] are 6 LSBs of 14-bit sample	
OUT_Y_MSB[1][2]	R	03h	04h		05h	00h	—	[7:0] are 8 MSBs of 14-bit sample	
OUT_Y_LSB[1][2]	R	04h	05h		00h		—	[7:2] are 6 LSBs of 14-bit sample	
OUT_Z_MSB[1][2]	R	05h	06h		00h		—	[7:0] are 8 MSBs of 14-bit sample	
OUT_Z_LSB[1][2]	R	06h	00h		00h		—	[7:2] are 6 LSBs of 14-bit sample	
Reserved	—	07h to 08h	—				—	Reserved, do not modify	
F_SETUP[1][3]	R/W	09h	0Ah				00h	FIFO setup	
TRIG_CFG	R/W	0Ah	0Bh				00h	FIFO event trigger configuration register	
SYSMOD[1][2]	R	0Bh	0Ch				00h	Current system mode	
INT_SOURCE[1][2]	R	0Ch	0Dh				00h	Interrupt status	
WHO_AM_I[1]	R	0Dh	0Eh				6Ah	Device ID	
XYZ_DATA_CFG[1][4]	R/W	0Eh	0Fh				00h	Acceleration dynamic range and filter enable settings	
HP_FILTER_CUTOFF[1][4]	R/W	0Fh	10h				00h	Pulse detection high-pass and low-pass filter enable bits. High-pass filter cutoff frequency selection	
PL_STATUS[1][2]	R	10h	11h				00h	Landscape/Portrait orientation status	
PL_CFG[1][4]	R/W	11h	12h				80h	Landscape/Portrait configuration.	
PL_COUNT[1][3]	R/W	12h	13h				00h	Landscape/Portrait debounce counter	
PL_BF_ZCOMP[1][4]	R/W	13h	14h				00h	Back/Front Trip angle threshold	
PL_THS_REG[1][4]	R/W	14h	15h				1Ah	Portrait to Landscape Trip Threshold angle and hysteresis settings	
A_FFMT_CFG[1][4]	R/W	15h	16h				00h	Free-fall/Motion function configuration	
A_FFMT_SRC[1][2]	R	16h	17h				00h	Free-fall/Motion event source register	
A_FFMT_THS[1][3]	R/W	17h	18h				00h	Free-fall/Motion threshold register	
A_FFMT_COUNT[1][3]	R/W	18h	19h				00h	Free-fall/Motion debounce counter	

Name	Type	Register address	Auto-increment address				Default hex value	Comment
			A	B	C	D		
Reserved	—	19h to 1Ch	—				—	Reserved, do not modify
TRANSIENT_CFG[1][4]	R/W	1Dh	1Eh				00h	Transient function configuration
TRANSIENT_SRC[1][2]	R	1Eh	1Fh				00h	Transient event status register
TRANSIENT_THS[1][3]	R/W	1Fh	20h				00h	Transient event threshold
TRANSIENT_COUNT[1][3]	R/W	20h	21h				00h	Transient debounce counter
PULSE_CFG[1][4]	R/W	21h	22h				00h	Pulse function configuration
PULSE_SRC[1][2]	R	22h	23h				00h	Pulse function source register
PULSE_THSX[1][3]	R/W	23h	24h				00h	X-axis pulse threshold
PULSE_THSY[1][3]	R/W	24h	25h				00h	Y-axis pulse threshold
PULSE_THSZ[1][3]	R/W	25h	26h				00h	Z-axis pulse threshold
PULSE_TMLT[1][4]	R/W	26h	27h				00h	Time limit for pulse detection
PULSE_LTCY[1][4]	R/W	27h	28h				00h	Latency time for second pulse detection
PULSE_WIND[1][4]	R/W	28h	29h				00h	Window time for second pulse detection
ASLP_COUNT[1][4]	R/W	29h	2Ah				00h	In activity counter setting for Auto-Sleep
CTRL_REG1[1][4]	R/W	2Ah	2Bh				00h	System ODR, accelerometer OSR, operating mode
CTRL_REG2[1][4]	R/W	2Bh	2Ch				00h	Self-Test, Reset, accelerometer OSR and Sleep mode settings
CTRL_REG3[1][4]	R/W	2Ch	2Dh				00h	Sleep mode interrupt wake enable, interrupt polarity, push-pull/open-drain configuration
CTRL_REG4[1][4]	R/W	2Dh	2Eh				00h	Interrupt enable register
CTRL_REG5[1][4]	R/W	2Eh	2Fh				00h	Interrupt pin (INT1/INT2) map
OFF_X[1][4]	R/W	2Fh	30h				00h	X-axis accelerometer offset adjust
OFF_Y[1][4]	R/W	30h	31h				00h	Y-axis accelerometer offset adjust
OFF_Z[1][4]	R/W	31h	32h				00h	Z-axis accelerometer offset adjust
Reserved	R/W	32h to 50h	—				—	Reserved, do not modify
TEMP_OUT	R	51h	—				—	Temperature sensor output data
Reserved	R/W	52h to 5Ah	—				—	Reserved, do not modify
CTRL_REG6	R/W	5Bh	5Ch				00h	Temperature sensor enable/disable control
CTRL_REG7	R/W	5Ch	5Dh				00h	Temperature sensor auto-increment address range inclusion enable/disable
Reserved	R/W	5Dh to 5Eh	—				—	Reserved, do not modify
A_VECM_CFG	R/W	5Fh	60h				00h	Acceleration vector-magnitude configuration register
A_VECM_THS_MSB	R/W	60h	61h				00h	Acceleration vector-magnitude threshold MSB
A_VECM_THS_LSB	R/W	61h	62h				00h	Acceleration vector-magnitude threshold LSB

Name	Type	Register address	Auto-increment address				Default hex value	Comment
			A	B	C	D		
A_VECM_CNT	R/W	62h	63h				00h	Acceleration vector-magnitude debounce count
A_VECM_INITX_MSB	R/W	63h	64h				00h	Acceleration vector-magnitude X-axis reference value MSB
A_VECM_INITX_LSB	R/W	64h	65h				00h	Acceleration vector-magnitude X-axis reference value LSB
A_VECM_INITY_MSB	R/W	65h	66h				00h	Acceleration vector-magnitude Y-axis reference value MSB
A_VECM_INITY_LSB	R/W	66h	67h				00h	Acceleration vector-magnitude Y-axis reference value LSB
A_VECM_INITZ_MSB	R/W	67h	68h				00h	Acceleration vector-magnitude Z-axis reference value MSB
A_VECM_INITZ_LSB	R/W	68h	69h				00h	Acceleration vector-magnitude Z-axis reference value LSB
Reserved	—	69h to 72h	—				—	Reserved, do not modify
A_FFMT_THS_X_MSB	R/W	73h	74h				00h	X-axis FMT threshold MSB
A_FFMT_THS_X_LSB	R/W	74h	75h				00h	X-axis FFMT threshold LSB
A_FFMT_THS_Y_MSB	R/W	75h	76h				00h	Y-axis FFMT threshold MSB
A_FFMT_THS_Y_LSB	R/W	76h	77h				00h	Y-axis FFMT threshold LSB
A_FFMT_THS_Z_MSB	R/W	77h	78h				00h	Z-axis FFMT threshold MSB
A_FFMT_THS_Z_LSB	R/W	78h	79h				00h	Z-axis FFMT threshold LSB
Reserved	—	79h to FFh	—				—	Reserved, do not modify

[1] Register contents are preserved when transitioning from Active to Standby mode.
[2] Register contents are reset when transitioning from Standby to Active mode.
[3] Register contents can be modified anytime in Standby or Active mode. A write to this register will cause a reset of the corresponding internal system debounce counter.
[4] Modification of this register's contents can only occur when device is in Standby mode, except the FS[1:0] bit fields in CTRL_REG1 register.

Note: *The auto-increment addressing is only enabled when registers are read using burst-read mode when the device is configured for I^2C or SPI. The auto-increment address is automatically reset to 00h in I^2C mode when a stop condition is detected. In SPI mode there is no stop condition and the auto-increment address is not automatically reset to 00h.*

18 Register descriptions by functional block

18.1 Device configuration registers

18.1.1 STATUS register (address 00h)

Table 15. STATUS register (address 00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DR_STATUS or F_STATUS							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 16. STATUS register (address 00h) bit description

Field	Description
F_SETUP[f_mode] = 00h	register 00h → DR_STATUS
F_SETUP[f_mode] > 00h	register 00h → F_STATUS

The STATUS register aliases allow for the contiguous burst read of both status and current acceleration sample/FIFO data using the auto-increment addressing mechanism in both 8- and 14-bit modes.

18.1.2 DR_STATUS register (address 00h)

Data-Ready Status when F_SETUP[*f_mode*] = 00h

This STATUS register provides the acquisition status information on a per-sample basis, and reflects real-time updates to the OUT_X, OUT_Y, and OUT_Z registers.

When the FIFO subsystem data output register driver is disabled (F_SETUP[*f_mode*] = 00h), this register indicates the real-time status information of the accelerometer X, Y, and Z axes sample data.

Table 17. DR_STATUS register (address 00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	zyxow	zow	yow	xow	zyxdr	zdr	ydr	xdr
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 18. DR_STATUS register (address 00h) bit description

Bit	Symbol	Description
7	zyxow	X-, Y-, Z-axis data overwrite **0 —** No data overwrite has occurred (reset value) **1 —** Previous X, Y, Z data was overwritten by new X, Y, Z data before it was completely read zyxow is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (that is, OUT_X, OUT_Y, and OUT_Z) has been overwritten. zyxow is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, and OUT_Z_MSB) are read.

Bit	Symbol	Description
6	zow	Z-axis data overwrite **0 —** No data overwrite has occurred (reset value) **1 —** Previous Z-axis data was overwritten by new Z-axis data before it was read zow is set to 1 whenever a new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. zow is cleared anytime OUT_Z_MSB register is read.
5	yow	Y-axis data overwrite **0 —** No data overwrite has occurred (reset value) **1 —** Previous Y-axis data was overwritten by new Y-axis data before it was read yow is set to 1 whenever a new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. yow is cleared anytime OUT_Y_MSB register is read.
4	xow	X-axis data overwrite **0 —** No data overwrite has occurred (reset value) **1 —** Previous X-axis data was overwritten by new X-axis data before it was read xow is set to 1 whenever a new X-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. xow is cleared anytime OUT_X_MSB register is read.
3	zyxdr	X-, Y-, Z-axis new data ready **0 —** No new set of data ready (reset value) **1 —** New set of data is ready zyxdr signals that a new acquisition for any of the enabled channels is available. zyxdr is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read.
2	zdr	Z-axis new data available **0 —** No new Z-axis data is ready (reset value) **1 —** New Z-axis data is ready zdr is set to 1 whenever a new Z-axis data acquisition is completed. zdr is cleared anytime the OUT_Z_MSB register is read.
1	ydr	Y-axis new data available **0 —** No new Y-axis data ready (reset value) **1 —** New Y-axis data is ready ydr is set to 1 whenever a new Y-axis data acquisition is completed. ydr is cleared anytime the OUT_Y_MSB register is read.
0	xdr	X-axis new data available **0 —** No new X-axis data ready (reset value) **1 —** New X-axis data is ready xdr is set to 1 whenever a new X-axis data acquisition is completed. xdr is cleared anytime the OUT_X_MSB register is read.

18.1.3 F_STATUS register (address 00h)

FIFO Status when F_SETUP[f_mode] = 00h.

If the FIFO subsystem data output register driver is enabled, the status register indicates the current status information of the FIFO subsystem.

Table 19. F_STATUS register (address 00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	f_ovf	f_wmrk_flag	f_cnt[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 20. FIFO flag event descriptions

f_ovf	f_wmrk_flag	Event description
0	X	No FIFO overflow events detected.
1	X	FIFO overflow event detected.
X	0	No FIFO watermark event detected.
X	1	A FIFO Watermark event was detected indicating that a FIFO sample count greater than watermark value has been reached. If F_SETUP[f_mode] = 11h, a FIFO trigger event was detected.

The f_ovf and f_wmrk_flag flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit in the interrupt source register (INT_SOURCE) by reading the F_STATUS register. In this case, the INT_SOURCE[src_fifo] bit will be set again when the next data sample enters the FIFO.

Therefore, the f_ovf bit will remain asserted while the FIFO has overflowed and the f_wmrk_flag bit will remain asserted while the f_cnt value is equal to or greater than then f_wmrk value.

Table 21. F_STATUS register (address 00h) bit description

Bit	Symbol	Description
5 to 0	f_cnt[5:0]	These bits indicate the number of acceleration samples currently stored in the FIFO buffer. Count 00 0000 indicates that the FIFO is empty. **00 0000 —** FIFO sample counter (reset value) **00 0001 to 10 0000 —** 1 to 32 samples stored in FIFO

18.1.4 TRIG_CFG register (address 0Ah)

FIFO trigger configuration register. After the interrupt flag of the enabled event in TRIG_CFG is set, the FIFO (when configured in Trigger mode) is gated at the time of the interrupt event preventing the further collection of data samples. This allows the host processor to analyze the data leading up to the event detection (up to 32 samples). For detailed information on how to utilize the FIFO and the various trigger events, see NXP application note AN4073.

Table 22. TRIG_CFG register (address 0Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	trig_trans	trig_lndprt	trig_pulse	trig_ffmt	trig_a_vecm	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. TRIG_CFG register (address 0Ah) bit description

Bit	Symbol	Description
5	trig_trans	Transient interrupt FIFO trigger enable **0 —** Transient interrupt FIFO trigger disabled (reset value) **1 —** Transient interrupt FIFO trigger enabled
4	trig_lndprt	Landscape/Portrait orientation interrupt FIFO trigger enable **0 —** Landscape/Portrait orientation interrupt FIFO trigger disabled (reset value) **1 —** Landscape/Portrait orientation interrupt FIFO trigger enabled

Bit	Symbol	Description
3	trig_pulse	Pulse interrupt FIFO trigger enable **0 —** Pulse interrupt FIFO trigger disabled (reset value) **1 —** Pulse interrupt FIFO trigger enabled
2	trig_ffmt	Free-fall/motion interrupt FIFO trigger enable **0 —** Free-fall/motion interrupt FIFO trigger disabled (reset value) **1 —** Free-fall/motion interrupt FIFO trigger enabled
1	trig_a_vecm	Acceleration vector-magnitude FIFO trigger enable **0 —** Acceleration vector-magnitude FIFO trigger disabled (reset value) **1 —** Acceleration vector-magnitude FIFO trigger enabled

18.1.5 SYSMOD register (address 0Bh)

The SYSMOD register indicates the current device operating mode. Applications using the Auto-Sleep/Auto-Wake mechanism can use this register to synchronize their application with the device operating mode. The system mode register also indicates the status of the FIFO gate error flag and the time elapsed since the FIFO gate error flag was asserted.

Table 24. SYSMOD register (address 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	fgerr	fgt[4:0]					sysmod[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 25. SYSMOD register (address 0Bh) bit description

Bit	Symbol	Description
7	fgerr	FIFO gate error **0 —** No FIFO gate error detected (reset value) **1 —** FIFO gate error was detected Emptying the FIFO buffer clears the *fgerr* bit in the SYSMOD register. See Section 18.1.10 for more information on configuring the FIFO Gate function.
6 to 2	fgt[4:0]	Number of ODR time units since *fgerr* was asserted. Reset when *fgerr* is cleared
1 to 0	sysmod[1:0]	System mode **00 —** Standby mode (reset value) **01 —** Wake mode **10 —** Sleep mode

18.1.6 INT_SOURCE register (address 0Ch)

Interrupt source register. The bits that are set (logic '1') indicate which function has asserted its interrupt and conversely bits that are cleared (logic '0') indicate which function has not asserted its interrupt.

Reading the INT_SOURCE register does not clear any interrupt status bits, except for src_a_vecm. See Table 26 and Table 27. The respective interrupt flag bits are reset by reading the appropriate source register for the function that generated the interrupt.

Table 26. INT_SOURCE register (address 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	src_aslp	src_fifo	src_trans	src_lndprt	src_pulse	src_ffmt	src_a_vecm	src_drdy
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 27. INT_SOURCE register (address 0Ch) bit description

Bit	Symbol	Description
7	src_aslp	Auto-Sleep/Wake interrupt status **0 —** No Wake-to-Sleep or Sleep-to-Wake system mode transition interrupt event has occurred **1 —** An interrupt event that can cause a Wake to Sleep or Sleep to Wake system mode transition has occurred The "Wake-to-Sleep" transition occurs when a period of inactivity that exceeds the user-specified time limit (ASLP_COUNT) has been detected, thus causing the system to transition to a user-specified low ODR setting. A "Sleep-to-Wake" transition occurs when the user-specified interrupt event has awakened the system, thus causing the system to transition to the user-specified higher ODR setting. Reading the SYSMOD register will clear the *src_aslp* bit.
6	src_fifo	FIFO interrupt status **0 —** No FIFO interrupt event has occurred **1 —** A FIFO interrupt event such as an overflow or watermark (F_STATUS[f_cnt] = F_STATUS[f_wmrk]) event has occurred This bit is cleared by reading the F_STATUS register.
5	src_trans	Transient interrupt status **0 —** No transient event has occurred **1 —** An acceleration transient value greater than user-specified threshold has occurred This bit is asserted whenever TRANSIENT_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the TRANSIENT_SRC register.
4	src_lndprt	Landscape/Portrait orientation interrupt status **0 —** No change in orientation status was detected **1 —** An interrupt was generated due to a change in the device orientation status This bit is asserted whenever PL_STATUS[*newlp*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
3	src_pulse	Pulse interrupt status **0 —** No pulse event was detected **1 —** An interrupt was generated due to single- and/or double-pulse event This bit is asserted whenever PULSE_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
2	src_ffmt	Free-fall/motion interrupt status **0 —** No free-fall or motion event was detected **1 —** The free-fall/motion function interrupt is active This bit is asserted whenever PULSE_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the A_FFMT_SRC register.
1	src_a_vecm	Accelerometer vector-magnitude interrupt status **0 —** No interrupt has been generated **1 —** An interrupt was generated due to acceleration vector-magnitude function This bit is cleared by reading this register (INT_SOURCE).

Bit	Symbol	Description
0	src_drdy	Data-ready interrupt status **0 —** No data available to read **1 —**This bit indicates that new accelerometer data is available to read. The *src_drdy* interrupt flag is cleared by reading the OUT_X, OUT_Y, and OUT_Z registers. This data can be retrieved using a 6-byte burst read starting from the address 01h (OUT_X_MSB).

18.1.7 WHO_AM_I register (address 0Dh)

Table 28. WHO_AM_I register (address 0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	who_am_i[7:0]							
Reset	0	1	1	0	1	0	1	0
Access	R	R	R	R	R	R	R	R

Table 29. WHO_AM_I register (address 0Dh) bit description

Bit	Symbol	Description
7 to 0	who_am_i[7:0]	Device identifier

18.1.8 CTRL_REG1 register (address 2Ah)

Note: *Except for Standby mode selection, the device must be in Standby mode to change any of the other bit fields within CTRL_REG1 (address 2Ah).*

Table 30. CTRL_REG1 register (address 2Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	aslp_rate[1:0]		dr[2:0]			lnoise	f_read	active
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 31. CTRL_REG1 register (address 2Ah) bit description

Bit	Symbol	Description
7 to 6	aslp_rate[1:0]	Configures the auto-wake sample frequency when the device is in Sleep mode. See Table 32 and Table 34 for more information.
5 to 3	dr[2:0]	Output data rate selection See Table 33 and Table 35 for more information.
2	lnoise	Reduced noise and full-scale range mode (analog gain times 2). **0 —** Normal mode **1 —** Reduced noise mode; Note that the FSR setting is restricted to a ±4 *g* in this mode (lnoise = 1).
1	f_read	Fast-read mode **0 —** Normal mode **1 —** Fast-read mode Data format is limited to the 8-bit MSB for accelerometer output data. The auto-address pointer will skip over the LSB address for each axes sample data when performing a burst read operation.
0	active	Standby/Active **0 —** Standby mode **1 —** Active mode

Table 32. Sleep mode poll rate description - CTRL_REG6 = 00h

aslp_rate[1:0]	Frequency (Hz)
00	50
01	12.5
10	6.25
11	1.56

It is important to note that when the device is in Auto-Sleep mode, the system ODR and data rate for all the system functional blocks is overridden by the sleep data rate set by the aslp_rate field.

Table 33 shows the various system output data rates (ODR) that can be selected using the dr[2:0] bits.

Table 33. System output data rate selection - CTRL_REG6 = 00h

dr[2:0]	ODR (Hz)	Period (ms)
000	800.0	1.25
001	400.0	2.5
010	200.0	5
011	100.0	10
100	50.0	20
101	12.5	80
110	6.25	160
111	1.5625	640

The *active* bit selects between Standby mode and Active mode. The default value is 0 (Standby mode) on reset.

The *lnoise* bit selects between normal full dynamic range mode and a high sensitivity, low-noise mode. In low-noise mode the maximum signal that can be measured is ±4 g.

Note: *In low-noise mode, a threshold value set above 4 g will not be reached, even if the physical input acceleration exceeds this value.*

The *f_read* bit selects between normal and fast-read modes where the auto-increment counter will also skip over each axis's LSB data bytes when *f_read* = 1. All of the acceleration data MSBs can be read out with a single 3-byte burst read starting at the OUT_X_MSB register when f_read = 1.

Note: *The f_read bit can only be changed while F_SETUP[f_mode] = 0.*

When temperature measurements are desired, the host must set CTRL_REG6 to the value 03h, which enables the measurement. This will cause the ODR to divide by a factor of 2 as shown in Table 34 and Table 35.

Table 34. Sleep mode poll rate description – CTRL_REG6 = 03h

aslp_rate[1:0]	Frequency (Hz)
00	25
01	6.25
10	3.125
11	0.781

Table 35. System output data rate selection – CTRL_REG6 = 03h

dr[2:0]	ODR (Hz)	Period (ms)
000	400.0	2.5
001	200.0	5
010	100.0	10
011	50.0	20
100	25	40
101	6.25	160
110	3.125	320
111	0.781	1280

18.1.9 CTRL_REG2 register (address 2Bh)

Table 36. CTRL_REG2 register (address 2Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	st	rst	—	smods[1:0]		slpe	mods[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 37. CTRL_REG2 register (address 2Bh) bit description

Bit	Symbol	Description
7	st	Self-test enable **0 —** Self-Test disabled **1 —** Self-Test enabled The *st* bit activates the accelerometer self-test function. When *st* is set to 1, a change will occur in the device output levels for each axis, allowing the host application to check the functionality of the transducer and measurement signal chain.

Bit	Symbol	Description
6	rst	Software reset **0 —** Device reset disabled **1 —** Device reset enabled The *rst* bit is used to initiate a software reset. The reset mechanism can be enabled in both Standby and Active modes. When the *rst* bit is set, the boot mechanism resets all functional block registers and loads the respective internal registers with their default values. After setting the *rst* bit, the system will automatically transition to Standby mode. Therefore, if the system was already in Standby mode, the reboot process will immediately begin; otherwise, if the system was in Active mode the boot mechanism will automatically transition the system from Active mode to Standby mode, only then can the reboot process begin. A system reset can also be initiated by pulsing the external RST pin high. ***Note:*** *The current revision of FXLS8471Q silicon, as identified by a WHO_AM_I value of 6Ah, has an errata associated with the software reset mechanism when the device is operated in SPI mode. Refer to Section 22 for further information and a suggested workaround.* The I^2C and SPI communication systems are also reset to avoid corrupted data transactions. The host application should allow 1 ms between issuing a software (setting *rst* bit) or hardware (pulsing RST pin) reset and attempting communications with the device over the I^2C or SPI interfaces. When the SPI interface mode is desired and multiple devices are present on the bus, make sure that the bus is quiet (all slave device MISO pins are high-z) during this 1 ms period to ensure the device does not inadvertently enter I^2C mode. See Section 10.2.3 for further information about the interface mode auto-detection circuit. At the end of the boot process, the *rst* bit is automatically cleared in hardware.
4 to 3	smods[1:0]	Accelerometer sleep mode OSR mode selection This setting, along with the CTRL_REG1[aslp_rate] ODR setting determines the sleep mode power and noise for acceleration measurements. See Table 38 and Table 39 for more information.
2	slpe	Auto-Sleep mode **0 —** Auto-Sleep is not enabled **1 —** Auto-Sleep is enabled When SLPE = 1, a transition between Sleep mode and Wake mode results in a FIFO flush and a reset of internal functional block counters. All functional block status information is preserved except where otherwise indicated. For further information, refer to Section 18.1.10.
1 to 0	mods[1:0]	Accelerometer wake mode OSR mode selection. This setting, along with the ODR selection (CTRL_REG1[dr]) determines the wake mode power and noise for acceleration measurements. See Table 38 and Table 39 for more information.

Table 38. CTRL_REG2[smods/mods] oversampling modes

smods[1:0]/mods[1:0]	Power mode
00	Normal
01	Low Noise, Low Power
10	High Resolution
11	Low Power

Table 39. Oversampling ratio versus oversampling mode

	Accelerometer OSR			
ODR (Hz)	Normal	Low Noise, Low Power	High Resolution	Low Power
1.5625	128	32	1024	16
6.25	32	8	256	4
12.5	16	4	128	2
50	4	4	32	2

	Accelerometer OSR			
ODR (Hz)	Normal	Low Noise, Low Power	High Resolution	Low Power
100	4	4	16	2
200	4	4	8	2
400	4	4	4	2
800	2	2	2	2

18.1.10 CTRL_REG3 - interrupt control register (address 2Ch)

Table 40. CTRL_REG3 [interrupt control register] (address 2Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	fifo_gate	wake_trans	wake_lndprt	wake_pulse	wake_ffmt	wake_ a_vecm	ipol	pp_od
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 41. CTRL_REG3 [Interrupt control register] (address 2Ch) bit descriptions

Bit	Symbol	Description
7	fifo_gate	FIFO gate **0 —** FIFO gate is bypassed. FIFO is flushed upon the system mode transitioning from Wake-to-Sleep mode or from Sleep-to-Wake mode. **1 —** The FIFO input buffer is blocked from accepting new samples when transitioning from "Wake-to-Sleep" mode or from "Sleep-to-Wake" mode until the FIFO is flushed.[1] Although the system transitions from "Wake-to-Sleep" or from "Sleep-to-Wake" the contents of the FIFO buffer are preserved. New data samples are ignored until the FIFO is emptied by the host application. If the *fifo_gate* bit is set to logic '1' and the FIFO buffer is not emptied before the arrival of the next sample, then the SYSMOD[*fgerr*] will be asserted. The SYSMOD[*fgerr*] bit remains asserted as long as the FIFO buffer remains unemptied. Emptying the FIFO buffer clears the SYS_MOD[*fgerr*] register.
6	wake_tran	**0 —** Transient function is disabled in Sleep mode **1 —** Transient function is enabled in Sleep mode and can generate an interrupt to wake the system
5	wake_lndprt	**0 —** Orientation function is disabled Sleep mode. **1 —** Orientation function is enabled in Sleep mode and can generate an interrupt to wake the system
4	wake_pulse	**0 —** Pulse function is disabled in Sleep mode **1 —** Pulse function is enabled in Sleep mode and can generate an interrupt to wake the system
3	wake_ffmt	**0 —** Free-fall/motion function is disabled in Sleep mode **1 —** Free-fall/motion function is enabled in Sleep mode and can generate an interrupt to wake the system
2	wake_a_vecm	**0 —** Acceleration vector-magnitude function is disabled in Sleep mode **1 —** Acceleration vector-magnitude function is enabled in Sleep mode and can generate an interrupt to wake the system

Bit	Symbol	Description
1	ipol	INT1/INT2 interrupt logic polarity **0 —** Active low (reset value) **1 —** Active high The *ipol* bit selects the logic polarity of the interrupt signals output on the INT1 and INT2 pins.
0	pp_od	INT1/INT2 push-pull or open-drain output mode selection **0 —** Push-pull (reset value) **1 —** Open-drain The open-drain configuration can be used for connecting multiple interrupt signals on the same interrupt line but will require an external pullup resistor to function correctly.

[1] The FIFO contents are flushed whenever the system ODR changes in order to prevent the mixing of FIFO data from different ODR periods.

18.1.11 CTRL_REG4 - interrupt enable register (address 2Dh)

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flag to the system's interrupt controller. The interrupt controller routes the enabled interrupt signals to either the INT1 or INT2 pins depending on the settings made in CTRL_REG5.

Table 42. CTRL_REG4 [Interrupt enable register] (address 2Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	int_en_aslp	int_en_fifo	int_en_trans	int_en_ lndprt	int_en_ pulse	int_en_ffmt	int_en_ a_vecm	int_en_drdy
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43. CTRL_REG4 [Interrupt enable register] (address 2Dh) bit descriptions

Bit	Symbol	Description
7	int_en_aslp	Sleep interrupt enable **0 —** Auto-Sleep/Wake interrupt disabled **1 —** Auto-Sleep/Wake interrupt enabled
6	int_en_fifo	FIFO interrupt enable **0 —** FIFO interrupt disabled **1 —** FIFO interrupt enabled
5	int_en_trans	Transient interrupt enable **0 —** Transient interrupt disabled **1 —** Transient interrupt enabled
4	int_en_lndprt	Orientation interrupt enable **0 —** Orientation (Landscape/Portrait) interrupt disabled **1 —** Orientation (Landscape/Portrait) interrupt enabled
3	int_en_pulse	Pulse interrupt enable **0 —** Pulse detection interrupt disabled **1 —** Pulse detection interrupt enabled

Bit	Symbol	Description
2	int_en_ffmt	Free-fall/motion interrupt enable **0** — Free-fall/motion interrupt disabled **1** — Free-fall/motion interrupt enabled
1	int_en_a_vecm	Acceleration vector-magnitude interrupt enable **0** — Acceleration vector-magnitude interrupt disabled **1** — Acceleration vector-magnitude interrupt enabled
0	int_en_drdy	Data-ready interrupt enable **0** — Data-ready interrupt disabled **1** — Data-ready interrupt enabled

18.1.12 CTRL_REG5 - interrupt routing configuration register (address 2Eh)

Table 44. CTRL_REG5 [Interrupt Routing Configuration Register] (address 2Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	int_cfg_aslp	int_cfg_fifo	int_cfg_ trans	int_cfg_ lndprt	int_cfg_ pulse	int_cfg_ffmt	int_cfg_ a_vecm	int_cfg_drdy
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 45. CTRL_REG5 [Interrupt Routing Configuration Register] (address 2Eh) bit descriptions

Bit	Symbol	Description
7	int_cfg_aslp	Sleep interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
6	int_cfg_fifo	FIFO interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
5	int_cfg_trans	Transient detection interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
4	int_cfg_lndprt	Orientation detection interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
3	int_cfg_pulse	Pulse detection interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
2	int_cfg_ffmt	Free-fall/motion detection interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin
1	int_cfg_a_vecm	Acceleration vector-magnitude interrupt routing **0** — Interrupt is routed to INT2 pin **1** — Interrupt is routed to INT1 pin

Bit	Symbol	Description
0	int_cfg_drdy	INT1/INT2 configuration. **0 —** Interrupt is routed to INT2 pin **1 —** Interrupt is routed to INT1 pin

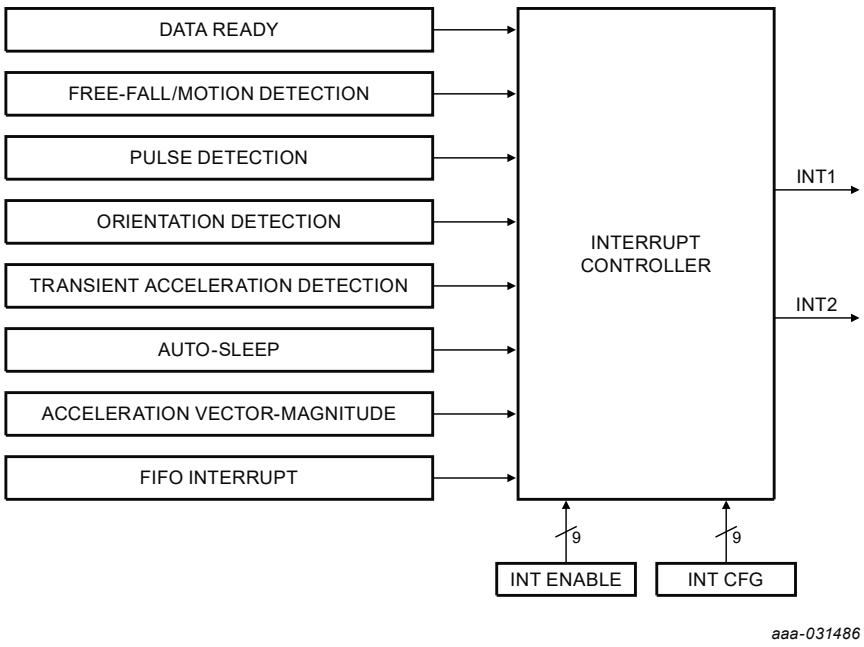


Figure 10. Interrupt controller block diagram

The system's interrupt controller uses the corresponding bit field in the CTRL_REG5 register to determine the routing for the INT1 and INT2 interrupt pins. For example, if the *int_cfg_drdy* bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1. All interrupt signals routed to either INT1 or INT2 are logically OR'ed together as illustrated in Figure 11, thus one or more functional blocks can assert an interrupt pin simultaneously; therefore, a host application responding to an interrupt should read the INT_SOURCE register to determine the source(s) of the interrupt(s).

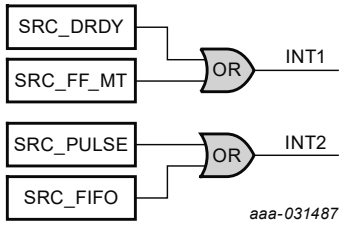


Figure 11. INT1/INT2 event flag logic example

18.1.13 CTRL_REG6 - register (address 5Bh)

Table 46. CTRL_REG6 register (address 5Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	reserved	reserved	reserved	reserved	reserved	adc_in[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 47. CTRL_REG6 register (address 5Bh) bit descriptions

Bit	Symbol	Description
0 to 1	adc_in[1:0]	ADC measurement selection **00 —** Only acceleration inputs (X,Y,Z) are scanned and converted by the ADC (reset value) **01 —** Reserved – do not use **10 —** Reserved – do not use **11 —** Both acceleration and temperature (X,Y,Z,T) inputs are scanned and converted by the ADC

18.1.14 CTRL_REG7 - register (address 5Ch)

Table 48. CTRL_REG7 register (address 5Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	reserved	iainc_mode	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49. CTRL_REG7 register (address 5Ch) bit descriptions

Bit	Symbol	Description
5	ainc_mode	Measurement data read-out addressing control **0 —** Disable secondary output data auto-increment mode (reset value) **1 —** Enable secondary output data auto-increment mode When the temperature sensor is enabled, and the application makes use of the internal drdy flag to produce a data read interrupt, a “dummy” read of register 33h is required to properly clear the drdy event flag and allow the following interrupt cycle to proceed. With ainc_mode = 1 and fast-read mode disabled (**CTRL_REG1**[f_read] = 0), the register read address pointer will automatically advance to register 33h during a burst read operation after reading register 06h (OUT_Z_LSB), allowing the data ready flag to be automatically cleared when reading the acceleration data without the need to perform a second, dedicated read cycle on address 33h. ***Note:*** *Regardless of the selected auto-increment mode, the value read from register 33h is always a “don’t care” value and can be safely discarded.*

18.2 Auto-Sleep trigger register

18.2.1 ASLP_COUNT register (address 29h)

The ASLP_COUNT register sets the minimum time period of event flag inactivity required to initiate a change from the current active mode ODR value specified in CTRL_REG1[*dr*] to the Sleep mode ODR value specified in CTRL_REG1[*aslp_rate*], provided that CTRL_REG2[*slpe*] = 1.

See Table 53 for functional blocks that can be monitored for inactivity in order to trigger the return-to-sleep event.

Table 50. ASLP_COUNT register (address 29h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	aslp_cnt[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 51. ASLP_COUNT register (address 29h) bit description

Bit	Symbol	Description
7 to 0	aslp_cnt[7:0]	See Table 52 for details.

Table 52. ASLP_COUNT relationship with ODR

Output data rate	Maximum inactivity time (s)	ODR time step (ms)	ASLP_COUNT step (ms)
800	81	1.25	320
400	81	2.5	320
200	81	5	320
100	81	10	320
50	81	20	320
12.5	81	80	320
6.25	81	160	320
1.56	163	640	640
0.781	163	1280	640

Table 53. Sleep/Wake mode gates and triggers

Interrupt source	Event restarts time and delays Return-to-Sleep	Event will Wake-from-Sleep
SRC_FIFO	Yes	No
SRC_TRANS	Yes	Yes
SRC_LNDPRT	Yes	Yes
SRC_PULSE	Yes	Yes

Interrupt source	Event restarts time and delays Return-to-Sleep	Event will Wake-from-Sleep
SRC_FFMT	Yes	Yes
SRC_ASLP	No[1]	No[1]
SRC_DRDY	No	No
SRC_AVECM	Yes	Yes

[1] If the *fifo_gate* bit is set to logic '1', the assertion of the SRC_ASLP interrupt does not prevent the system from transitioning to Sleep or from Wake mode; instead it prevents the FIFO buffer from accepting new sample data until the host application flushes the FIFO buffer.

The interrupt sources listed in Table 53 affect the auto-sleep, return to sleep and wake from sleep mechanism only if they have been previously enabled. The functional block event flags that are bypassed while the system is in Auto-Sleep mode are temporarily disabled and are automatically re-enabled when the device returns from Auto-Sleep mode (that is, wakes up), except for the data ready function.See Section Section 18.1.10 "CTRL_REG3 - interrupt control register (address 2Ch)" for more information.

If any of the interrupt sources listed under the Return-to-Sleep column is asserted before the sleep counter reaches the value specified in ASLP_COUNT, then all sleep mode transitions are terminated and the internal sleep counter is reset. If none of the interrupts listed under the Return-to-Sleep column are asserted within the time limit specified by the ASLP_COUNT register, the system will transition to the Sleep mode and use the ODR value specified in CTRL_REG1[*aslp_rate*].

If any of the interrupt sources listed under the "Wake-from-Sleep" column are asserted, then the system will transition out of the low sample rate Auto-Sleep mode to the user-specified fast sample rate, provided that the user-specified wake event function is enabled in register CTRL_REG3.

If the Auto-Sleep interrupt is enabled, a transition from Active mode to Sleep mode, and vice-versa, will generate an interrupt.

If CTRL_REG3[*fifo_gate*] = 1, transitioning to Auto-Sleep mode will preserve the FIFO contents, set SYSMOD[*fgerr*] (FIFO Gate error), and stop new acquisitions. The system will wait for the FIFO buffer to be emptied by the host application before new samples can be acquired.

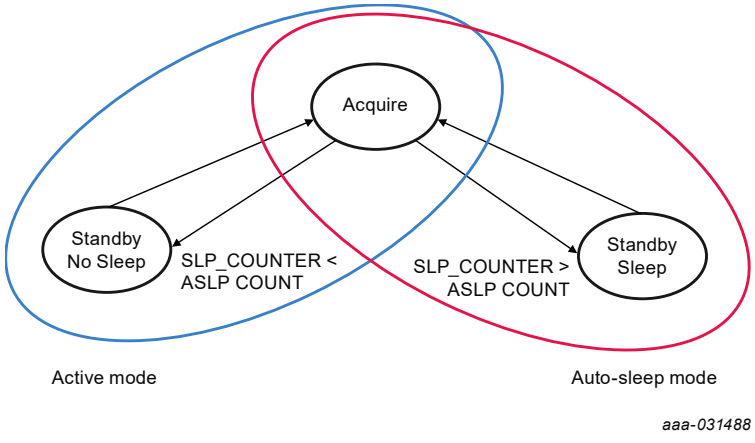


Figure 12. Auto-sleep state transition diagram

18.3 Temperature register

18.3.1 TEMP_OUT register (address 51h)

When the temperature sensor measurement is enabled (**CTRL_REG6** = 03h), this register contains the 8-bit two's complement temperature output value, which is updated at the ODR interval along with the acceleration data. With the temperature sensor enabled, if the application uses the drdy flag to trigger a data read operation, a dummy read of register 33h must also be made to clear the drdy flag for the next interrupt cycle.

When the **TEMP_OUT** register contains the value 00h, the measured temperature is nominally 25 °C. The measurement range is from –40 to 125 °C. As the offset is not factory trimmed, a variation in output from ideal, and device-to-device, will be observed for a given input temperature. The sensitivity is nominally 0.96 °C/LSB and is also not factory trimmed. Please see Table 12 for further information on the temperature sensor performance characteristics.

If absolute accuracy is important in the end application, NXP suggests performing a post-assembly single-point calibration and correcting the offset error within the host software.

Note that the temperature sensor ADC measurement is only performed when **CTRL_REG6** = 03h; this configuration value can be programmed along with the other **CTRL_REG**x parameters before entering the Active measurement mode.

Enabling the temperature sensor output will result in the selected ODR being reduced by a factor of 2, making the maximum nominal ODR 400 Hz and minimum 0.781 Hz.

It is suggested to read the **TEMP_OUT** register immediately after the **OUT_X/Y/Z** registers using a single byte read operation.

Table 54. TEMP_OUT register (address 51h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	temp_out[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

18.4 Output data registers

18.4.1 OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB registers (addresses 01h to 06h)

These registers contain the X-axis, Y-axis, and Z-axis 14-bit left-justified sample data expressed as two's complement numbers.

The sample data output registers store the current sample data if the FIFO buffer function is disabled. However, if the FIFO buffer function is enabled, the sample data output registers then point to the head of the FIFO buffer, which contains up to the previous 32 X, Y, and Z data samples.

The data is read out in the following order.

- Xmsb, Xlsb, Ymsb, Ylsb, Zmsb, Zlsb for CTRL_REG1[*f_read*] = 0
- Xmsb, Ymsb, Zmsb for CTRL_REG1[*f_read*] = 1.

If the CTRL_REG1[*f_read*] bit is set, auto-increment will skip over the LSB registers. This will shorten the data acquisition from 6 bytes to 3 bytes. If the LSB registers are directly addressed, the LSB information can still be read regardless of the CTRL_REG1[*f_read*] register setting.

If the FIFO data output register driver is enabled (F_SETUP[*f_mode*] > 00), register 01h points to the head of the FIFO buffer, while registers 02h, 03h, 04h, 05h, 06h return a value of zero when read directly.

The DR_STATUS registers, OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are located in the auto-incrementing address range of 00h to 06h, allowing all of the acceleration data to be read in a single-burst read of 6 bytes starting at the OUT_X_MSB register.

Table 55. OUT_X_MSB register (address 01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	xd[13:6]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 56. OUT_X_LSB register (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	xd[5:0]						—	—
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 57. OUT_Y_MSB register (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	yd[13:6]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 58. OUT_Y_LSB register (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	yd[5:0]						—	—
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 59. OUT_Z_MSB register (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	zd[13:6]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 60. OUT_Z_LSB register (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	zd[5:0]						—	—
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

18.5 FIFO registers

18.5.1 F_SETUP register (address 09h)

Table 61. F_SETUP register (address 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	f_mode[1:0]		f_wmrk[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 62. F_SETUP register (address 09h) bit descriptions

Bit	Symbol	Description
7 to 6	f_mode[1:0][1][2][3]	FIFO buffer operating mode **00 —** FIFO is disabled. (reset value) **01 —** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample. **10 —** FIFO stops accepting new samples when overflowed. **11 —** FIFO trigger mode. The FIFO is flushed whenever the FIFO is disabled, during an automatic ODR change (Auto-Wake/Sleep), or on a transition from Standby mode to Active mode. Disabling the FIFO (*f_mode* = 0b00) resets the F_STATUS[*f_ovf*], F_STATUS[*f_wmrk_flag*], F_STATUS[*f_cnt*] status flags to zero. A FIFO overflow event (that is, F_STATUS[*f_cnt]* = 32) will assert the F_STATUS[*f_ovf*] flag.
5 to 0	f_wmrk[5:0][2]	FIFO sample count watermark **00 0000 —** FIFO watermark event flag generation is disabled (reset value) These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag F_STATUS[*f_wmk_flag*] is raised when FIFO sample count F_STATUS[*f_cnt]* value is equal to or greater than the *f_ wmrk* watermark. Setting the f_wmrk to 0b00 0000 will disable the FIFO watermark event flag generation. This field is also used to set the number of pretrigger samples in trigger mode (*f_mode* = 0b).

[1] This bit field can be written in Active mode.
[2] This bit field can be written in Standby mode.
[3] The FIFO mode (*f_mode*) cannot be switched between operational modes (01, 10 and 11).

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data.

The FIFO update rate is dictated by the selected system ODR. In Active mode, the ODR is set by CTRL_REG1[*dr*] and when Auto-Sleep is active, the ODR is set by CTRL_REG1[*aslp_rate*] bit fields.

When data is read from the FIFO buffer, the oldest sample data in the buffer is returned and also deleted from the head of the FIFO, while the FIFO sample count is decremented

by one. It is assumed that the host application will use the I^2C or SPI burst read transactions to dump the FIFO contents. If the FIFO X, Y, and Z data is not completely read in one burst read transaction, the next read will start at the next FIFO location X-axis data. If the Y or Z data is not read out in the same burst transaction as the X-axis data, it will be lost.

In Trigger mode, the FIFO is operated as a circular buffer and will contain up to the 32 most recent acceleration data samples. The oldest sample is discarded and replaced by the current sample, until a FIFO trigger event occurs. After a trigger event occurs, the FIFO will continue to accept samples only until overflowed, after which point the newest sample data is discarded. For more information on using the FIFO buffer and the various FIFO operating modes, refer to NXP application note AN4073.

18.6 Sensor data configuration registers

18.6.1 XYZ_DATA_CFG register (address 0Eh)

The XYZ_DATA_CFG register is used to configure the desired acceleration full-scale range, and also to select whether the output data is passed through the high-pass filter.

Table 63. XYZ_DATA_CFG register (address 0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	—	hpf_out	—	—	fs[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 64. XYZ_DATA_CFG register (address 0Eh) bit descriptions

Bit	Symbol	Description
4	hpf_out	Enable high-pass filter on acceleration output data **0 —** High-pass filter is disabled (reset value) **1 —** Output data is high-pass filtered
1 to 0	fs[1:0]	Accelerometer full-scale range selection. See Table 65.

Table 65. Accelerometer full-scale range selection

fs[1:0]	Sensitivity	Full-scale range
00	±0.244 mg/LSB	±2 *g*
01	±0.488 mg/LSB	±4 *g*
10	±0.976 mg/LSB	±8 *g*
11	Reserved	—

18.7 High-pass filter register

18.7.1 HP_FILTER_CUTOFF register (address 0Fh)

High-pass filter cutoff frequency setting register.

Table 66. HP_FILTER_CUTOFF register (address 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	pulse_ hpf_byp	pulse_ lpf_en	—	—	sel[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 67. HP_FILTER_CUTOFF register (address 0Fh) bit descriptions

Bit	Symbol	Description
5	pulse_hpf_byp	Bypass high-pass filter for pulse processing function **0 —** HPF enabled for pulse processing **1 —** HPF bypassed for pulse processing
4	pulse_lpf_en	Enable low-pass filter for pulse processing function **0 —** LPF disabled for pulse processing **1 —** LPF enabled for pulse processing
1 to 0	sel[1:0]	HPF cutoff frequency selection See Table 59.

Table 68. HP_FILTER_CUTOFF

	High-pass cutoff frequency (Hz)							
ODR (Hz)	sel[1:0] = 0b00				sel[1:0] = 0b			
	Normal	LPLN	High Resolution	Low Power	Normal	LPLN	High Resolution	Low Power
800	16	16	16	16	8	8	8	8
400	16	16	16	8	8	8	8	4
200	8	8	16	4	4	4	8	2
100	4	4	16	2	2	2	8	1
50	2	2	16	1	1	1	8	0.5
12.5	2	0.5	16	0.25	1	0.25	8	0.125
6.25	2	0.25	16	0.125	1	0.125	8	0.063
1.56	2	0.063	16	0.031	1	0.031	8	0.016
ODR (Hz)	sel[1:0] = 0b				sel[1:0] = 0b			
	Normal	LPLN	High Resolution	Low Power	Normal	LPLN	High Resolution	Low Power
800	4	4	4	4	2	2	2	2
400	4	4	4	2	2	2	2	1
200	2	2	4	1	1	1	2	0.5
100	1	1	4	0.5	0.5	0.5	2	0.25
50	0.5	0.5	4	0.25	0.25	0.25	2	0.125
12.5	0.5	0.125	4	0.063	0.25	0.063	2	0.031

ODR (Hz)	High-pass cutoff frequency (Hz)							
	sel[1:0] = 0b00				sel[1:0] = 0b			
	Normal	LPLN	High Resolution	Low Power	Normal	LPLN	High Resolution	Low Power
6.25	0.5	0.063	4	0.031	0.25	0.031	2	0.016
1.56	0.5	0.016	4	0.008	0.25	0.008	2	0.004

18.8 Portrait/Landscape detection registers

The FXLS8471Q is capable of detecting six orientations: Landscape Left, Landscape Right, Portrait Up, and Portrait Down with Z-lockout feature as well as Face Up and Face Down orientation as shown in Figure 13, Figure 14 and Figure 15. For more details on the meaning of the different user-configurable settings and for example code, refer to NXP application note AN4068.

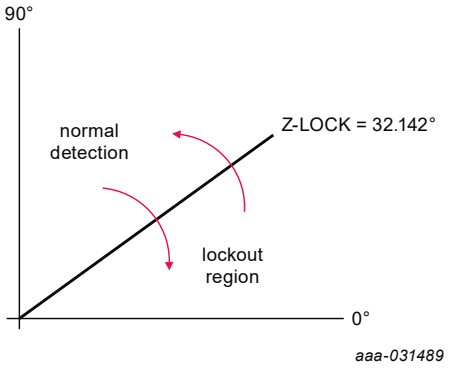


Figure 13. Illustration of Z-tilt angle lockout transition

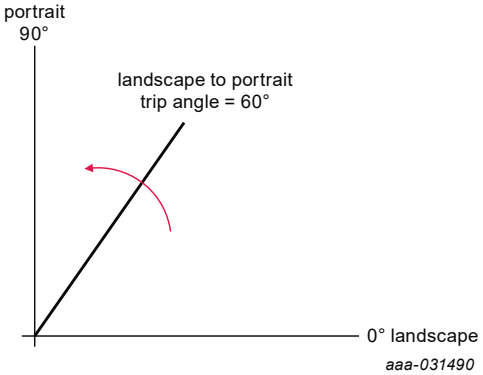


Figure 14. Illustration of landscape to portrait transition

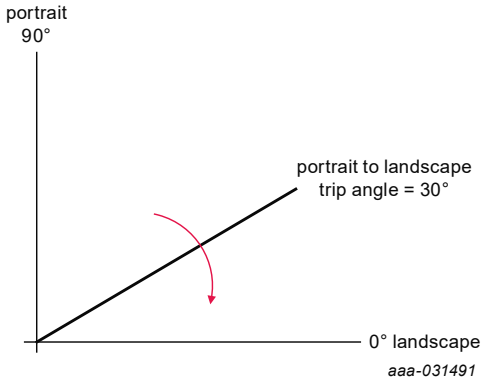


Figure 15. Illustration of portrait to landscape transition

18.8.1 PL_STATUS register (address 10h)

This status register can be read to get updated information on any change in orientation by reading bit 7, or the specifics of the orientation by reading the other bits. For further understanding of Portrait Up, Portrait Down, Landscape Left, Landscape Right, Back and Front orientations, see Figure 3. The interrupt is cleared when reading the PL_STATUS register.

Table 69. PL_STATUS register (address 10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	newlp	lo	—	—	—	lapo[1:0]		bafro
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 70. PL_STATUS register (address 10h) bit descriptions

Bit	Symbol	Description
7	newlp	Landscape/Portrait status change flag. **0 —** No change **1 —** BAFRO and/or LAPO and/or Z-tilt lockout value has changed
6	lo	Z-tilt angle lockout. **0 —** Lockout condition has not been detected. **1 —** Z-tilt lockout trip angle has been exceeded. Lockout condition has been detected.
2 to 1	lapo[1:0][1]	Landscape/Portrait orientation. **00 —** Portrait up: equipment standing vertically in the normal orientation **01 —** Portrait down: equipment standing vertically in the inverted orientation **10 —** Landscape right: equipment is in landscape mode to the right **11 —** Landscape left: equipment is in landscape mode to the left
0	bafro	Back or front orientation. **0 —** Front: equipment is in the front facing orientation **1 —** Back: equipment is in the back facing orientation

[1] The default power-up state is *bafro*(Undefined), *lapo*(Undefined), and no lockout for orientation function.

The *newlp* bit is set to 1 after the first orientation detection after a Standby to Active transition, and whenever a change in *lo*, *bafro*, or *lapo* occurs. The *newlp* bit is cleared anytime the PL_STATUS register is read. *lapo, bafro* and *lo* continue to change when *newlp* is set. The current orientation is locked if the absolute value of the acceleration experienced on any of the three axes is greater than 1.25 *g*.

18.8.2 PL_CFG register (address 11h)

This register enables the Portrait/Landscape function and sets the behavior of the debounce counter.

Table 71. PL_CFG register (address 11h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	dbcntm	pl_en	—	—	—	—	—	—
Reset	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 72. PL_CFG register (address 11h) bit descriptions

Bit	Symbol	Description
7	dbcntm	Debounce counter mode selection **0 —** Decrements debounce whenever condition of interest is no longer valid. **1 —** Clears counter whenever condition of interest is no longer valid. (reset value)
6	pl_en	Portrait/Landscape detection enable **0 —** Portrait/Landscape detection is disabled. (reset value) **1 —** Portrait/Landscape detection is enabled.

18.8.3 PL_COUNT register (address 12h) register

This register sets the debounce count for the orientation state transition. The minimum debounce latency is determined by the system ODR value and the value of the PL_COUNT register. Any change to the system ODR or a transition from active-to-standby (or vice-versa) resets the internal debounce counters.

Table 73. PL_COUNT register (address 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	dbnce[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 74. PL_COUNT register (address 12h) bit descriptions

Bit	Symbol	Description
7 to 0	dbnce[7:0]	Sets the debounce count for the orientation state transition See Table 75.

Table 75. PL_Count Relationship with the ODR

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

18.8.4 PL_BF_ZCOMP register (address 13h)

Back/Front and Z-tilt angle compensation register

Table 76. PL_BF_ZCOMP register (address 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	bkfr[1:0]		—	—	—	zlock[2:0]		
Reset	1	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. PL_BF_ZCOMP register (address 13h) bit descriptions

Bit	Symbol	Description
7 to 6	bkfr[1:0]	Back/front trip angle threshold. See Table 79 for more information. Default: **0b** → **±70°**. Step size is 5°. Range: ±(65° to 80°).
2 to 0	zlock[2:0]	Z-lock angle threshold. Range is from approximately 13° to 44°. Step size is approximately 4°. See Table 78 for more information. Default value: **04h** → **~28°**. Maximum value: **07h** → **~44°**.

Table 78. Z-lockout angle definitions

zlock[2:0]	Resultant angle (min) for positions between Landscape and Portrait	Resultant angle (max) for ideal Landscape or Portrait
000	13.6°	14.5°
001	17.1°	18.2°
010	20.7°	22.0°
011	24.4°	25.9°
100	28.1°	30.0°

zlock[2:0]	Resultant angle (min) for positions between Landscape and Portrait	Resultant angle (max) for ideal Landscape or Portrait
101	32.0°	34.2°
110	36.1°	38.7°
111	40.4°	43.4°

Table 79. Back/Front orientation definitions

bkfr[1:0]	Back to Front transition	Front to Back transition
00	Z < 80° or Z > 280°	Z > 100° and Z < 260°
01	Z < 75° or Z > 285°	Z > 105° and Z < 255°
10	Z < 70° or Z > 290°	Z > 110° and Z < 250°
11	Z < 65° or Z > 295°	Z > 115° and Z < 245°

18.8.5 PL_THS_REG register (address 14h)

Portrait to landscape trip threshold register.

Table 80. PL_THS_REG register (address 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pl_ths[4:0]					hys[2:0]		
Reset	0	0	0	1	1	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 81. PL_BF_ZCOMP register (address 13h) bit descriptions

Bit	Symbol	Description
7 to 3	pl_ths[4:0]	See Table 82.
2 to 0	hys[2:0]	See Table 83.

Table 82. Threshold angle lookup table

pl_ths[4:0]	Threshold angle
0 0111	15°
0 1001	20°
0 1100	30°
0 1101	35°
0 1111	40°
1 0000	45°
1 0011	55°
1 0100	60°
1 0111	70°

pl_ths[4:0]	Threshold angle
1 1001	75°

Table 83. Trip angles versus hysteresis settings

hys[2:0]	Landscape to Portrait trip angle	Portrait to Landscape trip angle
000	45°	45°
001	49°	41°
010	52°	38°
011	56°	34°
100	59°	31°
101	62°	28°
110	66°	24°
111	69°	21°

Table 84. Portrait/Landscape ideal orientation definitions

Symbol	Description
PU	y ~ –1 *g*, x ~ 0
PD	y ~ +1 *g*, x ~ 0
LR	y ~ 0, x ~ +1 *g*
LL	y ~ 0, x ~ –1 *g*

18.9 Free-fall and Motion event detection

The freefall/motion detection block can be configured to detect low-g (freefall) or high-g (motion) events utilizing the A_FFMT_CFG[a_ffmt_oae] bit.

In low-g detect mode (A_FFMT_CFG[a_ffmt_oae] = 0) a low-g condition will need to occur on all enabled axes (ex. X, Y and Z) for the A_FFMT_SRC[a_ffmt_ea] bit to be affected. And, in high-g detect mode (A_FFMT_CFG[a_ffmt_oae] = 1) a high-g condition occurring in any of the enabled axes (ex. X, Y or Z) will suffice to affect the A_FFMT_SRC[a_ffmt_ea] bit.

The detection threshold(s) are programed in register 17h (A_FFMT_THS) for common threshold operation, and 73h to 78h (A_FFMT_THS_X/Y/Z) for individual axis threshold operation.

A_FFMT_CFG[a_ffmt_ele] bit determines the behavior of A_FFMT_SRC[a_ffmt_ea] bit in response to the desired acceleration event (low-g/high-g). When A_FFMT_CFG[a_ffmt_ele] = 1, the freefall or motion event is latched and the A_FFMT_SRC[a_ffmt_ea] flag can only be cleared by reading the A_FFMT_SRC register. When A_FFMT_CFG[a_ffmt_ele] = 0, freefall or motion events are not latched, and the A_FFMT_SRC[a_ffmt_ea] bit reflects the real-time status of the event detection.

A_FFMT_THS[a_ffmt_dbcntm] bit determines the debounce filtering behavior of the logic that sets the A_FFMT_SRC[a_ffmt_ea] bit. See Figure 17 for details.

It is possible to enable/disable each axis used in the freefall/motion detection function by configuring bits A_FFMT_CFG[a_ffmt_xefe], A_FFMT_CFG[a_ffmt_yefe], and A_FFMT_CFG[a_ffmt_zefe].

The freefall/motion detection function has the option to use a common 7-bit unsigned threshold for each of the X, Y, and Z axes, or individual unsigned 13-bit thresholds for each axis. When A_FFMT_THS_X_MSB[a_ffmt_ths_xyz_en] = 0, the 7-bit threshold value stored in register 17h is used as a common 7-bit threshold for the X, Y, and Z axes. When a_ffmt_ths_xyz_en = 1, each axis may be programmed with an individual 13-bit threshold (stored in the A_FFMT_X/Y/Z MSB and LSB registers).

18.9.1 A_FFMT_CFG register (address 15h)

Free-fall/motion configuration register.

Table 85. A_FFMT_CFG register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ele	a_ffmt_oae	a_ffmt_zefe	a_ffmt_yefe	a_ffmt_xefe	—	—	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 86. A_FFMT_CFG register (address 15h) bit descriptions

Bit	Symbol	Description
7	a_ffmt_ele	**0 —** Event flag latch disabled (reset value) **1 —** Event flag latch enabled a_ffmt_ele denotes whether the enabled event flag will be latched in the A_FFMT_SRC register or the event flag status in the A_FFMT_SRC will indicate the real-time status of the event. If *a_ffmt_ele* bit is set to a logic '1', then the event flags are frozen when the *a_ffmt_ea* bit gets set, and are cleared by reading the A_FFMT_SRC source register.
6	a_ffmt_oae	Motion detect/free-fall detect logic selection. **0 —** Free-fall flag (logical AND combination of low-*g* X-, Y-, Z-axis event flags) (reset value) **1 —** Motion flag (logical OR combination of high-*g* X-, Y-, Z event flags) a_ffmt_oae bit allows the selection between motion (logical OR combination of high-*g* X-, Y-, Z-axis event flags) and free-fall (logical AND combination of low-*g* X-, Y-, Z-axis event flags) detection.
5	a_ffmt_zefe	**0 —** Event detection disabled (reset value) **1 —** Raise event flag on measured Z-axis acceleration above/below threshold. a_ffmt_zefe enables the detection of a high- or low-*g* event when the measured acceleration data on Z-axis is above/below the threshold set in the A_FFMT_THS register. If *a_ffmt_ele* is set to logic '1', new event flags are blocked from updating the A_FFMT_SRC register.
4	a_ffmt_yefe	**0 —** Event detection disabled (reset value) **1 —** Raise event flag on measured Y-axis acceleration above/below threshold. a_ffmt_yefe enables the detection of a high- or low-*g* event when the measured acceleration data on Y-axis is above/below the threshold set in the A_FFMT_THS register. If *a_ffmt_ele* bit is set to logic '1', new event flags are blocked from updating the A_FFMT_SRC register.

Bit	Symbol	Description
3	a_ffmt_xefe	**0 —** Event detection disabled (reset value) **1 —** Raise event flag on measured X-axis acceleration above/below threshold. a_ffmt_xefe enables the detection of a high- or low-*g* event when the measured acceleration data on X-axis is above/below the threshold set in the A_FFMT_THS register. If *a_ffmt_ele* bit is set to logic '1', new event flags are blocked from updating the A_FFMT_SRC register.

18.9.2 A_FFMT_SRC register (address 16h)

Freefall/motion source register. Read-only register.

The free-fall/motion source register keeps track of the acceleration event that is triggering (or has triggered, in case of A_FFMT_CFG[a_ffmt_ele] = 1) the event flag. In particular A_FFMT_SRC[a_ffmt_ea] is set to a logic '1' when the logical combination of acceleration event flags specified in A_FFMT_CFG register is true. This bit is used in combination with the values in CTRL_REG4[int_en_ffmt] and CTRL_REG5[int_cfg_ffmt] register bits to generate the free-fall/motion interrupts.

Table 87. A_FFMT_SRC register (address 16h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ea	—	a_ffmt_zhe	a_ffmt_zhp	a_ffmt_yhe	a_ffmt_yhp	a_ffmt_xhe	a_ffmt_xhp
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 88. A_FFMT_SRC register (address 16h) bit descriptions

Bit	Symbol	Description
7	a_ffmt_ea	Event active flag **0 —** No event flag has been asserted (reset value) **1 —** One or more event flag has been asserted. See the description of the A_FFMT_CFG[*a_ffmt_oae*] bit to determine the effect of the 3-axis event flags on the *a_ffmt_ea* bit.
5	a_ffmt_zhe	Z-high event flag **0 —** Event detected (reset value) **1 —** Z-high event has been detected This bit always reads zero if the *a_ffmt_zefe* control bit is set to zero
4	a_ffmt_zhp	Z-high event polarity flag **0 —** Z event was positive *g* (reset value) **1 —** Z event was negative *g* This bit always reads zero if the *a_ffmt_zefe* control bit is set to zero
3	a_ffmt_yhe	Y-high event flag **0 —** No event detected (reset value) **1 —** Y-high event has been detected This bit always reads zero if the *a_ffmt_yefe* control bit is set to zero
2	a_ffmt_yhp	Y-high event polarity flag **0 —** Y event detected was positive *g* (reset value) **1 —** Y event was negative *g* This bit always reads zero if the *a_ffmt_yefe* control bit is set to zero

Bit	Symbol	Description
1	a_ffmt_xhe	X-high event flag **0 —** No event detected (reset value) **1 —** X-high event has been detected This bit always reads zero if the *a_ffmt_xefe* control bit is set to zero
0	a_ffmt_xhp	X-high event polarity flag. Default value: 0 **0 —** X event was positive *g* (reset value) **1 —** X event was negative *g* This bit always reads zero if the *a_ffmt_xefe* control bit is set to zero

18.9.3 A_FFMT_THSxxxxxx registers (addresses 17h, 73h to 78h)

Free-fall/motion detection threshold registers.

Table 89. A_FFMT_THS register (address 17h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_dbcntm	ths[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 90. A_FFMT_THS register (address 17h) bit descriptions

Bit	Symbol	Description
7	a_ffmt_dbcntm	The fucntion uses *a_ffmt_dbcntm* to set the acceleration FFMT debounce counter clear mode independent of the value of the *a_ffmt_ths_xyz_en*. *a_ffmt_dbcntm* bit configures the way in which the debounce counter is reset when the inertial event of interest is momentarily not true. When *a_ffmt_dbcntm* bit is a logic '1', the debounce counter is cleared to 0 whenever the inertial event of interest is no longer true (part b, Figure 17) while if the *a_ffmt_dbcntm* bit is set to logic '0' the debounce counter is decremented by 1 whenever the inertial event of interest in longer true (part c, Figure 17) until the debounce counter reaches 0 or the inertial event of interest become active. The decrementing of the debounce counter acts to filter out irregular or spurious events, which might impede the correct detection of desired inertial events.
6 to 0	ths[6:0]	Free-fall/motion detection threshold **000 0000 —** (reset value) Resolution is fixed at 63 mg/LSB, irrespective of the device full-scale range selection.

Table 91. A_FFMT_THS_X_MSB register (address 73h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ths_xyz_en	a_ffmt_ths_x[12:6]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 92. A_FFMT_THS_X_MSB register (address 73h) bit descriptions

Bit	Symbol	Description
7	a_ffmt_ths_xyz_en	For *a_ffmt_ths_xyz_en* = 0, the function uses the *ffmt_ths*[6:0] value located in register 17h[6:0] as a common threshold for the X-, Y-, and Z-axis acceleration detection. The common unsigned 7-bit acceleration threshold has a fixed resolution of 63 mg/LSB, with a range of 0 to 127 counts. For *a_ffmt_ths_xyz_en* = 1 the function ignores the common 7-bit G_FFMT_THS value located in register 17h when executing the FFMT function, and the following independent threshold values are used for each axis: A_FFMT_THS_X_MSB and A_FFMT_THS_X_LSB are used for the X-axis acceleration threshold, A_FFMT_THS_Y_MSB and A_FFMT_THS_Y_LSB for the Y-axis acceleration threshold, A_FFMT_THS_Z_MSB and A_FFMT_THS_Z_LSB for the Z-axis acceleration threshold. The A_FFMT_THS_X/Y/Z thresholds are 13-bit unsigned values that have the same resolution as the accelerometer output data determined by XYZ_DATA_CFG fs [1:0]. The *a_ffmt_ths_xyz_en* and *a_ffmt_trans_ths_en* bits must not be enabled simultaneously, as incorrect function operation will result.
6 to 0	a_ffmt_ths_x[12:6]	7-bit MSB of X-axis acceleration threshold

Table 93. A_FFMT_THS_X_LSB register (address 74h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ths_x[5:0]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 94. A_FFMT_THS_X_LSB register (address 74h) bit descriptions

Bit	Symbol	Description
5 to 0	a_ffmt_ths_x[5:0]	6-bit LSB of X-axis acceleration threshold

Table 95. A_FFMT_THS_Y_MSB register (address 75h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ trans_ths_en	a_ffmt_ths_y[12:6]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 96. A_FFMT_THS_Y_MSB register (address 75h) bit descriptions

Bit	Symbol	Description
7	a_ffmt_trans_ths_en	The *a_ffmt_trans_ths_en* bits must not be enabled simultaneously, as incorrect function operation will result.
12 to 6	a_ffmt_ths_y[12:6]	7-bit MSB of X-axis acceleration threshold

Table 97. A_FFMT_THS_Y_LSB register (address 76h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ths_y[5:0]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 98. A_FFMT_THS_Y_LSB register (address 76h) bit descriptions

Bit	Symbol	Description
5 to 0	a_ffmt_ths_y[5:0]	6-bit LSB of Y-axis acceleration threshold

Table 99. A_FFMT_THS_Z_MSB register (address 77h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	a_ffmt_ths_z[12:6]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 100. A_FFMT_THS_Z_MSB register (address 77h) bit descriptions

Bit	Symbol	Description
12 to 6	a_ffmt_ths_z[12:6]	7-bit LSB of Z-axis acceleration threshold

Table 101. A_FFMT_THS_Z_LSB register (address 78h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_ths_z[5:0]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 102. A_FFMT_THS_Z_LSB register (address 78h) bit descriptions

Bit	Symbol	Description
5 to 0	a_ffmt_ths_z[5:0]	6-bit LSB of Z-axis acceleration threshold

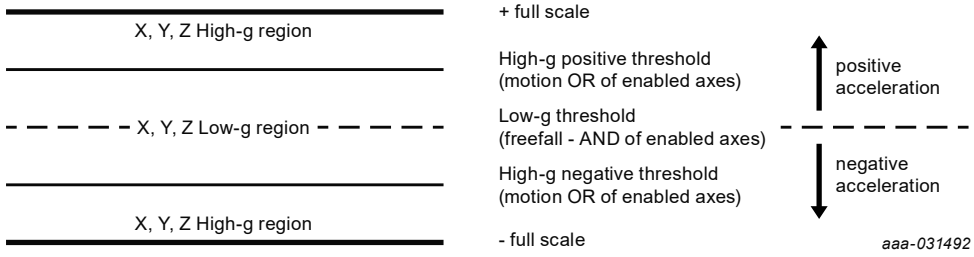


Figure 16. A_FFMT_THS high and low-*g* level

A_FFMT_THS contains the unsigned 7-bit threshold value used by the free-fall/motion detection functional block and is used to detect either low-*g* (free fall) or high-*g* (motion) events depending on the setting of G_FFMT_CFG[*f_ffmt_oae*]. If *g_ffmt_oae* = 0, the event is detected when the absolute value of all the enabled axes are below the threshold value. When *g_ffmt_oae* = 1, the event is detected when the absolute value of any of the enabled axes is above the threshold value. See Figure 16 for an illustration of the free-fall/motion event detection thresholds. If A_FFMT_THS_X_MSB[*a_ffmt_ths_xyz_en*] = 1, the behavior is identical, except that each axis can be programmed with an individual 13-bit threshold (stored in the A_FFMT_X/Y/Z MSB and LSB registers).

18.9.4 A_FFMT_COUNT register (address 18h)

The debounce count register for free-fall/motion detection events sets the number of debounce counts for acceleration sample data matching the user-programmed conditions for either a free-fall or motion detection event required before the interrupt is triggered.

Table 103. A_FFMT_COUNT register (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_ffmt_count[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 104. A_FFMT_COUNT register (address 18h) bit description

Bit	Symbol	Description
7 to 0	a_ffmt_count[7:0]	*a_ffmt_count* defines the minimum number of debounce sample counts required for the detection of a free-fall or motion event. A_FFMT_THS[*ffmt_dbcntm*] determines the behavior of the counter when the condition of interest is momentarily not true.

When the internal debounce counter reaches the A_FFMT_COUNT value a free-fall/motion event flag is set. The debounce counter will never increase beyond the A_FFMT_COUNT value. The time step used for the debounce sample count depends on the ODR chosen. See Table 105.

Table 105. A_FFMT_COUNT relationship with the ODR

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

For example, an ODR of 100 Hz and an A_ FFMT_COUNT value of 15h would result in a minimum debounce response time of 150 ms.

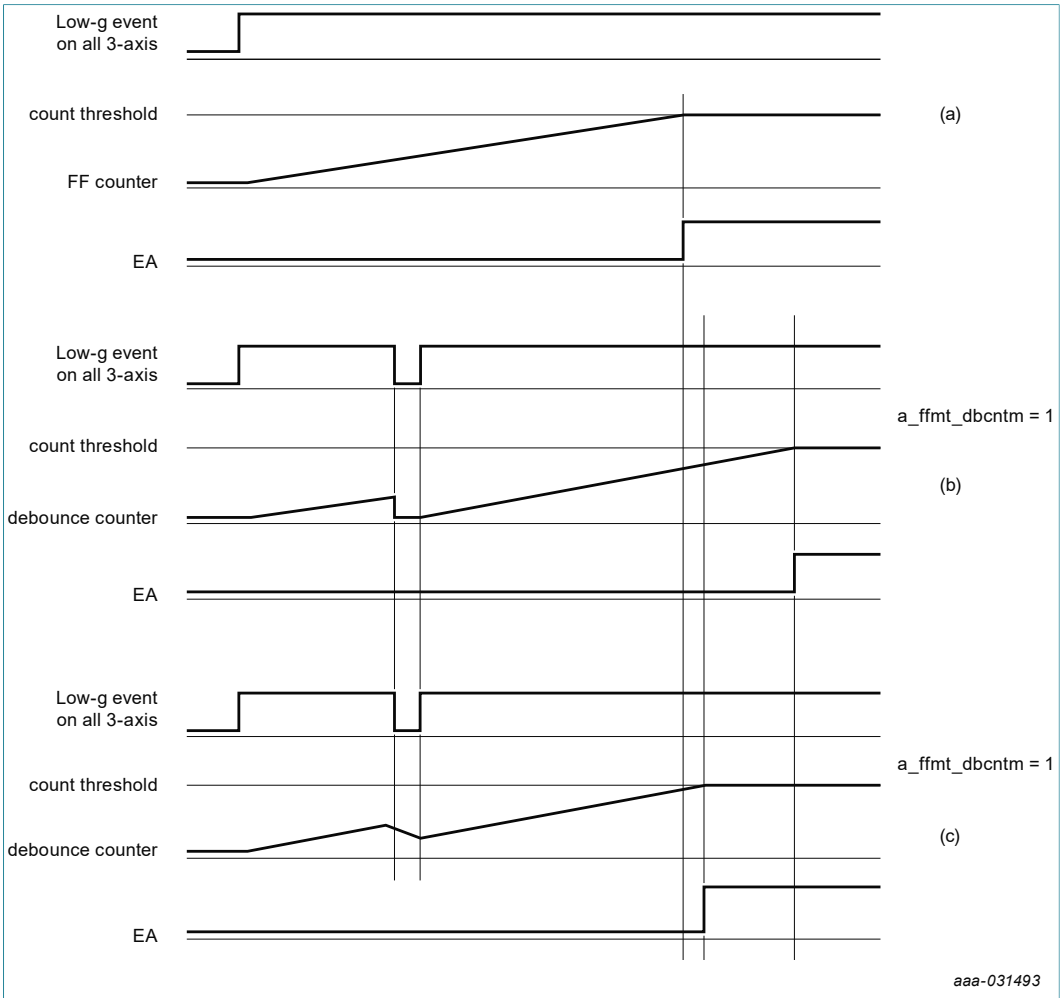


Figure 17. Behavior of the A_FFMT debounce counter in relation to the a_ffmt_dbcntm setting

18.10 Accelerometer vector-magnitude function registers

The accelerometer vector-magnitude function is an inertial-event detection function available to assist host software algorithms in detecting motion events.

If $\sqrt{(a\_x\_out - a\_x\_ref)^2 + (a\_y\_out - a\_y\_ref)^2 + (a\_z\_out - a\_z\_ref)^2} > A\_VECM\_THS$ for a time period greater than the value stored in A_VECM_CNT, the vector-magnitude change event flag is triggered.

a_x_out, a_y_out, and a_z_out are the current accelerometer output values, and a_x_ref, a_y_ref, and a_z_ref are the reference values stored internally in the ASIC for each axis or in A_VECM_INIT_X/Y/Z registers if A_VECM_CFG[*a_vecm_initm*] is set.

Note that the x_ref, y_ref, and z_ref values are not directly visible to the host application through the register interface. Refer to NXP application note AN4458.

18.10.1 A_VECM_CFG register (address 5Fh)

Table 106. A_VECM_CFG register (address 5Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	a_vecm_ele	a_vecm_initm	a_vecm_updm	a_vecm_en	—	—	—
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 107. A_VECM_CFG register (address 5Fh) bit descriptions

Bit	Symbol	Description
6	a_vecm_ele	Control bit *a_vecm_ele* defines the event latch enable mode. Event latching is disabled for *a_vecm_ele* = 0. In this case, the vector-magnitude interrupt flag is in updated real time and is cleared when the condition for triggering the interrupt is no longer true. The setting and clearing of the event flag is controlled by the A_VECM_CNT register's programmed debounce time. For *a_vecm_ele* = 1, the interrupt flag is latched in and held until the host application reads the INT_SOURCE register (0Ch).
5	a_vecm_initm	Control bit *a_vecm_initm* defines how the initial reference values (x_ref, y_ref, and z_ref) are chosen. For *a_vecm_initm* = 0 the function uses the current x/y/z accelerometer output data at the time when the vector magnitude function is enabled. For *a_vecm_initm* = 1 the function uses the data from A_VECM_INIT_X/Y/Z registers as the initial reference values.
4	a_vecm_updm	Control bit *a_vecm_updm* defines how the reference values are updated once the vector-magnitude function has been triggered. For *a_vecm_updm* = 0, the function updates the reference value with the current x, y, and z accelerometer output data values. For *a_vecm_updm* = 1, the function does not update the reference values when the interrupt is triggered. Instead the function continues to use the reference values that were loaded when the function was enabled. If both *a_vecm_initm* and *a_vecm_updm* are set to logic '1', the host software can manually update the reference values in real time by writing to the A_VECM_INITX/Y/Z registers.
3	a_vecm_en	The accelerometer vector-magnitude function is enabled by setting *a_vecm_en* = 1, and disabled by clearing this bit (reset value). The reference values are loaded with either the current X/Y/Z acceleration values or the values stored in the A_VECM_INIT_X/Y/Z registers, depending on the state of the *a_vecm_initm* bit. ***Note:*** *The vector-magnitude function will only perform correctly up to a maximum ODR of 400 Hz.*

18.10.2 A_VECM_THS_MSB register (address 60h)

Table 108. A_VECM_THS_MSB register (address 60h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_dbcntm	—	—	a_vecm_ths[12:8]				
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. A_VECM_THS_MSB register (address 60h) bit descriptions

Bit	Symbol	Description
7	a_vecm_dbcntm	Control bit *a_vecm_dbcntm* defines how the debounce timer is reset when the condition for triggering the interrupt is no longer true. **0 —** The debounce counter is decremented by 1 when the vector-magnitude result is below the programmed threshold value. **1 —** The debounce counter is cleared when the vector-magnitude result is below the programmed threshold value.
4 to 0	a_vecm_ths[12:8]	Five MSBs of the 13-bit unsigned A_VECM_THS value. The threshold resolution is equal to the selected accelerometer resolution as set in XYZ_DATA_CFG[*fs*].

18.10.3 A_VECM_THS_LSB register (address 61h)

Table 110. A_VECM_THS_LSB register (address 61h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_ths[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 111. A_VECM_THS_LSB bit description

Bit	Symbol	Description
7 to 0	a_vecm_ths[7:0]	Vector-magnitude function debounce count value.

18.10.4 A_VECM_CNT register (address 62h)

Table 112. A_VECM_CNT register (address 62h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_cnt[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 113. A_VECM_CNT bit description

Bit	Symbol	Description
7 to 0	a_vecm_cnt[7:0]	Vector-magnitude function debounce count value.

The debounce timer period is determined by the ODR selected in CTRL_REG1 (and CTRL_REG6, as enabling the temperature sensor output effectively halves the ODR selected in CTRL_REG1); it is equal to the number indicated in A_VECM_CNT register multiplied by the ODR period, i.e., 1/ODR. For example, a value of 16 in A_VECM_CNT with an effective ODR of 400 Hz will result in a debounce period of 40 ms.

18.10.5 A_VECM_INITX_MSB register (address 63h)

Table 114. A_VECM_INITX_MSB register (address 63h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	a_vecm_initx[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 115. A_VECM_INITX_MSB register (address 63h) bit description

Bit	Symbol	Description
5 to 0	a_vecm_initx[13:8]	Most significant 6 bits of the signed 14-bit initial X-axis value to be used as ref_x when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.10.6 A_VECM_INITX_LSB register (address 64h)

Table 116. A_VECM_INITX_LSB register (address 64h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_initx[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 117. A_VECM_INITX_LSB register (address 64h) bit description

Bit	Symbol	Description
7 to 0	a_vecm_initx[7:0]	LSB of the signed 14-bit initial X-axis value to be used as ref_x when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.10.7 A_VECM_INITY_MSB register (address 65h)

Table 118. A_VECM_INITY_MSB register (address 65h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	a_vecm_inity[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 119. A_VECM_INITY_MSB register (address 65h) bit description

Bit	Symbol	Description
5 to 0	a_vecm_inity[13:8]	Most significant 6 bits of the signed 14-bit initial Y-axis value to be used as ref_y when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.10.8 A_VECM_INITY_LSB register (address 66h)

Table 120. A_VECM_INITY_LSB register (address 66h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_inity[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 121. A_VECM_INITY_LSB register (address 66h) bit description

Bit	Symbol	Description
7 to 0	a_vecm_inity[7:0]	LSB of the signed 14-bit initial Y-axis value to be used as ref_y when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.10.9 A_VECM_INITZ_MSB register (address 67h)

Table 122. A_VECM_INITZ_MSB register (address 67h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	a_vecm_initz[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 123. A_VECM_INITZ_MSB register (address 67h) bit description

Bit	Symbol	Description
5 to 0	a_vecm_initz[13:8]	Most significant 6 bits of the signed 14-bit initial Z-axis value to be used as ref_z when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.10.10 A_VECM_INITZ_LSB register (address 68h)

Table 124. A_VECM_INITZ_LSB register (address 68h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	a_vecm_initz[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 125. A_VECM_INITZ_LSB bit description

Bit	Symbol	Description
7 to 0	a_vecm_initz[7:0]	LSB of the signed 14-bit initial Z-axis value to be used as ref_z when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

18.11 Transient (AC) acceleration detection registers

The transient detection function is similar to the free-fall/motion detection function with the exception that a high-pass filter can be used to eliminate the DC offset from the acceleration data. There is an option to disable the high-pass filter, which causes the transient detection function to work in a similar manner to the motion detection function.

The transient detection function can be configured to signal an interrupt when the high-pass filtered acceleration delta values for any of the enabled axes exceeds the threshold programmed in TRANSIENT_THS for the debounce time programmed in TRANSIENT_COUNT. For more information on how to use and configure the transient detection function refer to NXP application note AN4461.

18.11.1 TRANSIENT_CFG register (address 1Dh)

Table 126. TRANSIENT_CFG register (address 1Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	—	tran_ele	tran_zefe	tran_yefe	tran_xefe	tran_hpf_byp
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 127. TRANSIENT_CFG register (address 1Dh) bit descriptions

Bit	Symbol	Description
4	tran_ele	Transient event flag latch **0 —** Event flag latch disabled; the transient interrupt flag reflects the real-time status of the function. (reset value) **1 —** Event flag latch enabled; the transient interrupt event flag is latched and a read of the TRANSIENT_SRC register is required to clear the event flag.
3	tran_zefe	Z-axis transient event flag **0 —** Z-axis event detection disabled (reset value) **1 —** Z-axis event detection enabled. Raise event flag on Z-axis acceleration value greater than threshold.
2	tran_yefe	Y-axis transient event flag enable **0 —** Y-axis event detection disabled (reset value) **1 —** Y-axis event detection enabled. Raise event flag on Y-axis acceleration value greater than threshold.
1	tran_xefe	X-axis transient event flag enable **0 —** X-axis event detection disabled (reset value) **1 —** X-axis event detection enabled. Raise event flag on X-axis acceleration value greater than threshold.
0	tran_hpf_byp	Transient function high-pass filter bypass **0 —** High-pass filter is applied to accelerometer data input to the transient function. (reset value) **1 —** High-pass filter is not applied to accelerometer data input to the transient function.

18.11.2 TRANSIENT_SRC register (address 1Eh)

Transient event flag source register. This register provides the event status of the enabled axes and polarity (directional) information.

Table 128. TRANSIENT_SRC register (address 1Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	tran_ea	tran_zef	tran_zpol	tran_yef	tran_ypol	tran_xef	trans_xpol
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 129. TRANSIENT_SRC register (address 1Eh) bit descriptions

Bit	Symbol	Description
6	tran_ea	Transient event active flag **0 —** No transient event active flag has been asserted. (reset value) **1 —** One or more transient event active flags has been asserted.
5	tran_zef	Z-axis transient event active flag **0 —** Z-axis event flag is not active. (reset value) **1 —** Z-axis event flag is active; Z-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
4	tran_zpol	Z-axis event flag polarity **0 —** Z-axis event was above positive threshold value. (reset value) **1 —** Z-axis event was below negative threshold value.
3	tran_yef	Y-axis transient event active flag **0 —** Y-axis event flag is not active. (reset value) **1 —** Y-axis event flag is active; Y-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
2	tran_ypol	Y-axis event flag polarity. **0 —** Y-axis event was above positive threshold value. (reset value) **1 —** Y-axis event was below negative threshold value.
1	tran_xef	X-axis transient event active flag **0 —** X-axis event flag is not active. (reset value) **1 —** X-axis event flag is active; X-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
0	tran_xpol	X-axis event flag polarity. **0 —** X-axis event was above positive threshold value. (reset value) **1 —** X-axis event was below negative threshold value.

When TRANSIENT_CFG[*tran_ele*] = 1, the TRANSIENT_SRC event flag(s) and polarity bits are latched when the interrupt event is triggered, allowing the host application to determine which event flag(s) originally triggered the interrupt. When TRANSIENT_CFG[*tran_ele*] = 0, events that occur after the event that originally triggered the interrupt will update the flag and polarity bits. However, once set, the flags can only be cleared by reading the TRANSIENT_SRC register.

18.11.3 TRANSIENT_THS register (address 1Fh)

The TRANSIENT_THS register determines the debounce counter behavior and also sets the transient event detection threshold. It is possible to use A_FFMT_THS_X/Y/Z MSB and LSB registers to set transient acceleration thresholds for individual axes using the *a_ffmt_trans_ths_en* bit in A_FFMT_THS_Y_MSB register.

Table 130. TRANSIENT_THS register (address 1Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	tr_dbcntm	tr_ths[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 131. TRANSIENT_THS register (address 1Fh) bit descriptions

Bit	Symbol	Description
7	tr_dbcntm	Debounce counter mode selection. **0 —** Decrements debounce counter when the transient event condition is not true during the current ODR period. (reset value) **1 —** Clears debounce counter when the transient event condition is not true during the current ODR period.
6 to 0	tr_ths[6:0]	Transient event threshold This register has a resolution of 63 mg/LSB regardless of the full-scale range setting made in XYZ_DATA_CFG[*fs*]. If CTRL_REG1[*lnoise*] = 1, the maximum acceleration measurement range is ±4 *g*.

The tr_ths[6:0] value is a 7-bit unsigned number, with a fixed resolution of 63 mg/LSB corresponding to a ±8 *g* measurement range. The resolution does not change with the full-scale range setting made in XYZ_DATA_CFG[*fs*]. If CTRL_REG1[*lnoise*] = 1, the measurement range is fixed at ±4 *g*, regardless of the settings made in XYZ_DATA_CFG.

18.11.4 TRANSIENT_COUNT register (address 20h)

The TRANSIENT_COUNT register sets the minimum number of debounce counts needed to trigger the transient event interrupt flag when the measured acceleration value exceeds the threshold set in TRANSIENT_THS for any of the enabled axes.

Table 132. TRANSIENT_COUNT register (address 20h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	tr_count[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 133. TRANSIENT_COUNT register (address 20h) bit description

Bit	Symbol	Description
7 to 0	tr_count[7:0)	Transient function debounce count value.

The time step for the transient detection debounce counter is set by the value of the system ODR and power mode as shown in Table 134.

Table 134. TRANSIENT_COUNT relationship with the ODR

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

An ODR of 100 Hz and a TRANSIENT_COUNT value of 15, when accelerometer OSR is set to normal using CTRL_REG2, would result in minimum debounce response time of 150 ms.

18.12 Pulse detection registers

18.12.1 PULSE_CFG register (address 21h)

This register configures the pulse event detection function.

Table 135. PULSE_CFG register (address 21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pls_dpa	pls_ele	pls_zdpefe	pls_zspefe	pls_ydpefe	pls_yspefe	pls_xdpefe	pls_xspefe
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 136. PULSE_CFG register (address 21h) bit descriptions

Bit	Symbol	Description
7	pls_dpa	Double-pulse abort **0 —** Double-pulse detection is not aborted if the start of a pulse is detected during the time period specified by the PULSE_LTCY register. (reset value) **1 —** Setting the *pls_dpa* bit momentarily suspends the double-tap detection, if the start of a pulse is detected during the time period specified by the PULSE_LTCY register and the pulse ends before the end of the time period specified by the PULSE_LTCY register.
6	pls_ele	Pulse event flag latch **0 —** Event flag latch disabled (reset value) **1 —** Event flag latch enabled When enabled, a read of the PULSE_SRC register is needed to clear the event flag.

Bit	Symbol	Description
5	pls_zdpefe	Event flag enable on double-pulse event on Z-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of double-pulse event on Z-axis
4	pls_zspefe	Event flag enable on single-pulse event on Z-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of single-pulse event on Z-axis
3	pls_ydpefe	Event flag enable on double-pulse event on Y-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of double-pulse event on Y-axis
2	pls_yspefe	Event flag enable on single-pulse event on Y-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of single-pulse event on Z-axis
1	pls_xdpefe	Event flag enable on double-pulse event on X-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of double-pulse event on X-axis
0	pls_xspefe	Event flag enable on single-pulse event on X-axis **0 —** Event detection disabled (reset value) **1 —** Raise event flag on detection of single-pulse event on X-axis

18.12.2 PULSE_SRC register (address 22h)

This register indicates the status bits for the pulse detection function.

Table 137. PULSE_SRC register (address 22h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pls_src_ea	pls_src_axz	pls_src_axy	pls_src_axx	pls_src_dpe	pls_src_polz	pls_src_poly	pls_src_polx
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 138. PULSE_SRC register (address 22h) bit descriptions

Bit	Symbol	Description
7	pls_src_ea	Event active flag **0 —** No interrupt has been generated (reset value) **1 —** One or more interrupt events have been generated
6	pls_src_axz	Z-axis event flag **0 —** No interrupt. (reset value) **1 —** Z-axis event has occurred
5	pls_src_axy	Y-axis event flag **0 —** No interrupt. (reset value) **1 —** Y-axis event has occurred
4	pls_src_axx	X-axis event flag **0 —** No interrupt. (reset value) **1 —** X-axis event has occurred

Bit	Symbol	Description
3	pls_src_dpe	Double pulse on first event **0 —** Single-pulse event triggered interrupt (reset value) **1 —** Double-pulse event triggered interrupt
2	pls_src_polz	Pulse polarity of Z-axis event **0 —** Pulse event that triggered interrupt was positive (reset value) **1 —** Pulse event that triggered interrupt was negative
1	pls_src_poly	Pulse polarity of Y-axis event **0 —** Pulse event that triggered interrupt was positive (reset value) **1 —** Pulse event that triggered interrupt was negative
0	pls_src_polx	Pulse polarity of X-axis event. **0 —** Pulse event that triggered interrupt was positive (reset value) **1 —** Pulse event that triggered interrupt was negative

18.12.3 PULSE_THSX register (address 23h)

The PULSE_THSX register defines the threshold used by the system to start the pulse-event detection procedure. Threshold values are unsigned 7-bit numbers with a fixed resolution of 0.063 *g*/LSB, corresponding to an 8 *g* acceleration full-scale range. The full-scale range is fixed at 8 *g* for the pulse detection function, regardless of the settings made in XYZ_DATA_CFG[*fs*].

Table 139. PULSE_THSX register (address 23h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	pls_thsx[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 140. PULSE_THSX register (address 23h) bit description

Bit	Symbol	Description
6 to 0	pls_thsx[6:0]	Pulse threshold for X-axis

18.12.4 PULSE_THSY register (address 24h)

The PULSE_THSY register defines the threshold used by the system to start the pulse-event detection procedure. Threshold values are unsigned 7-bit numbers with a fixed resolution of 0.063 *g*/LSB, corresponding to an 8 *g* acceleration full-scale range. The full-scale range is fixed at 8 *g* for the pulse detection function, regardless of the settings made in XYZ_DATA_CFG[*fs*].

Table 141. PULSE_THSY register (address 24h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	pls_thsy[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 142. PULSE_THSY register (address 24h) bit description

Bit	Symbol	Description
6 to 0	pls_thsy[6:0]	Pulse threshold for Y-axis

18.12.5 PULSE_THSZ register (address 25h)ULSE_THSZ register (address 25h) bit allocation

The PULSE_THSZ register defines the threshold used by the system to start the pulse-event detection procedure. Threshold values are unsigned 7-bit numbers with a fixed resolution of 0.063 *g*/LSB, corresponding to an 8 *g* acceleration full-scale range. The full-scale range is fixed at 8 *g* for the pulse detection function, regardless of the settings made in XYZ_DATA_CFG[*fs*].

Bit	7	6	5	4	3	2	1	0
Symbol	—	pls_thsz[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 143. PULSE_THSZ register (address 25h) bit description

Bit	Symbol	Description
6 to 0	pls_thsz[6:0]	Pulse threshold for Z-axis

18.12.6 PULSE_TMLT register (address 26h)

Table 144. PULSE_TMLT register (address 26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pls_tmlt[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 145. PULSE_TMLT register (address 26h) bit description

Bit	Symbol	Description
7 to 0	pls_tmlt[7:0]	*pls_tmlt*[7:0] defines the maximum time interval that can elapse between the start of the acceleration on the selected channel exceeding the specified threshold and the end when the channel acceleration goes back below the specified threshold.

Minimum time step for the pulse-time limit is defined in Table 146 and Table 147. Maximum time for a given ODR is "Minimum time step x 255".

Table 146. Time step for PULSE_TMLT with HP_FILTER_CUTOFF[pls_hpf_en] = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

Table 147. Time step for PULSE_TMLT with HP_FILTER_CUTOFF[pls_hpf_en] = 0

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.159	0.159	0.159	0.159	0.625	0.625	0.625	0.625
400	0.159	0.159	0.159	0.319	0.625	0.625	0.625	1.25
200	0.319	0.319	0.159	0.638	1.25	1.25	0.625	2.5
100	0.638	0.638	0.159	1.28	2.5	2.5	0.625	5
50	1.28	1.28	0.159	2.55	5	5	0.625	10
12.5	1.28	5.1	0.159	10.2	5	20	0.625	40
6.25	1.28	5.1	0.159	10.2	5	20	0.625	40
1.56	1.28	5.1	0.159	10.2	5	20	0.625	40

An ODR setting of 400 Hz, when the accelerometer OSR is set to normal using CTRL_REG2, results in a maximum pulse-time limit of (0.625 ms * 255) = 159 ms.

18.12.7 PULSE_LTCY register (address 27h)

Table 148. PULSE_LTCY register (address 27h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pls_ltcy[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 149. PULSE_LTCY register (address 27h) bit description

Bit	Symbol	Description
7 to 0	pls_ltcy[7:0]	*pls_ltcy*[7:0] defines the time interval that starts after the first pulse detection where the pulse-detection function ignores the start of a new pulse.

Minimum time step for the pulse latency is defined in Table 150 and Table 151. Maximum time is "(time step @ ODR and power mode) x 255".

Table 150. Time step for PULSE_LTCY with HP_FILTER_CUTOFF[pls_hpf_en] = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	40.8	1.276	81.6	40	160	5	320
1.56	10.2	40.8	1.276	81.6	40	160	5	320

Table 151. Time step for PULSE_LTCY with HP_FILTER_CUTOFF[pls_hpf_en] = 0

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	10.2	0.318	20.4	10	40	1.25	80
1.56	2.56	10.2	0.318	20.4	10	40	1.25	80

18.12.8 PULSE_WIND register (address 28h)

Table 152. PULSE_WIND register (address 28h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	pls_wind[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 153. PULSE_WIND register (address 28h) bit description

Bit	Symbol	Description
7 to 0	pls_wind[7:0]	*pls_wind*[7:0] defines the maximum interval of time that can elapse after the end of the latency interval in which the start of the second pulse event must be detected provided the device has been configured for double pulse detection. The detected second pulse width must be shorter than the time limit constraint specified by the PULSE_TMLT register, but the end of the double pulse need not finish within the time specified by the PULSE_WIND register.

The time step for the pulse-window counter varies with the selected ODR and power modes as defined in Table 154 and Table 155. The maximum time value is equal to "(time step @ ODR and power mode) x 255".

Table 154. Time step for PULSE_WIND with HP_FILTER_CUTOFF[pls_hpf_en] = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	40.8	1.276	81.6	40	160	5	320
1.56	10.2	40.8	1.276	81.6	40	160	5	320

Table 155. Time step for PULSE_WIND with HP_FILTER_CUTOFF[pls_hpf_en] = 0

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	10.2	0.318	20.4	10	40	1.25	80
1.56	2.56	10.2	0.318	20.4	10	40	1.25	80

18.13 Offset correction registers

The 8-bit two's complement offset correction registers are used to remove the sensor zero-*g* offset on the X, Y, and Z axes after device board mount. The resolution of the offset registers is 2 mg per LSB, with an effective offset adjustment range of –256 mg to +254 mg for each axis. The acceleration vectors represented in these registers will be

added to the acceleration vectors acquired by the ASIC from the transducer prior to being written to the output data registers (registers 01h through 06h). For example, to correct for an offset of 60 mg, a value representing –60 mg (= –60 mg/2 mg/LSB = –30 LSB), which is E2h in 8-bit two's complement representation, should be written to the offset register.

For more information on how to calibrate the 0 *g* offset, refer to NXP application note AN4069.

Note: *Accelerometer offset registers can only be modified when the device is in standby mode. See* M_CTRL_REG1 register (address 5Bh).

18.13.1 OFF_X register (address 2Fh)

Table 156. OFF_X register (address 2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	off_x[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 157. OFF_X register (address 2Fh) bit description

Bit	Symbol	Description
7 to 0	off_x[7:0]	X-axis offset correction value expressed as an 8-bit two's complement number.

18.13.2 OFF_Y register (address 30h)

Table 158. OFF_Y register (address 30h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	off_y[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 159. OFF_Y register (address 30h) bit description

Bit	Symbol	Description
7 to 0	off_y[7:0]	Y-axis offset correction value expressed as an 8-bit two's complement number.

18.13.3 OFF_Z register (address 31h)

Table 160. OFF_Z register (address 31h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	off_z[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 161. OFF_Z register (address 31h) bit description

Bit	Symbol	Description
7 to 0	off_z[7:0]	Z-axis offset correction value expressed as an 8-bit two's complement number.

19 Mounting guidelines for the Quad Flat No-Lead (QFN) package

Printed Circuit Board (PCB) layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process.

These guidelines are for soldering and mounting the Quad Flat No-Lead (QFN) package inertial sensors to PCBs. The purpose is to minimize the stress on the package after board mounting. The FXLS8471Q uses the QFN package platform. This section describes suggested methods of soldering these devices to the PCB for consumer applications.

NXP application note AN1902, "Quad Flat Pack No-Lead (QFN) Micro Dual Flat Pack No-Lead (DFN)" discusses the QFN package used by the FXLS8471Q, PCB design guidelines for using QFN packages and temperature profiles for reflow soldering.

19.1 Overview of soldering considerations

Information provided here is based on experiments executed on QFN devices. As they cannot represent exact conditions present at a customer site, the information provided herein should be used for guidance only and further process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

The QFN package is compliant with the RoHS standards. Refer to NXP application note AN4077 for more information.

19.2 Halogen content

This package is designed to be Halogen free, exceeding most industry and customer standards. Halogen free means that no homogeneous material within the assembled package will contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

19.3 PCB mounting recommendations

- The PCB land should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 18.
- No additional via pattern underneath package.
- PCB land pad is 0.8 mm by 0.3 mm as shown in Figure 18.
- Solder mask opening = PCB land pad edge + 0.113 mm larger all around.
- Stencil opening = PCB land pad – 0.015 mm smaller all around = 0.77 mm by 0.27 mm.
- Stencil thickness is 100 or 125 µm.
- Do not place any components or vias at a distance less than 2 mm from the package land area. This might cause additional package stress if it is too close to the package land area.

- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on the NC pads in order to have same length of exposed trace for all pads.
- Use a standard pick and place process and equipment. Do not use a hand soldering process.
- Do not use a screw down or stacking to fix the PCB into an enclosure as this could bend the PCB, putting stress on the package.
- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.
- No copper traces or fills on component mounting layer directly under the package. This will cause planarity issues with board mount. NXP QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

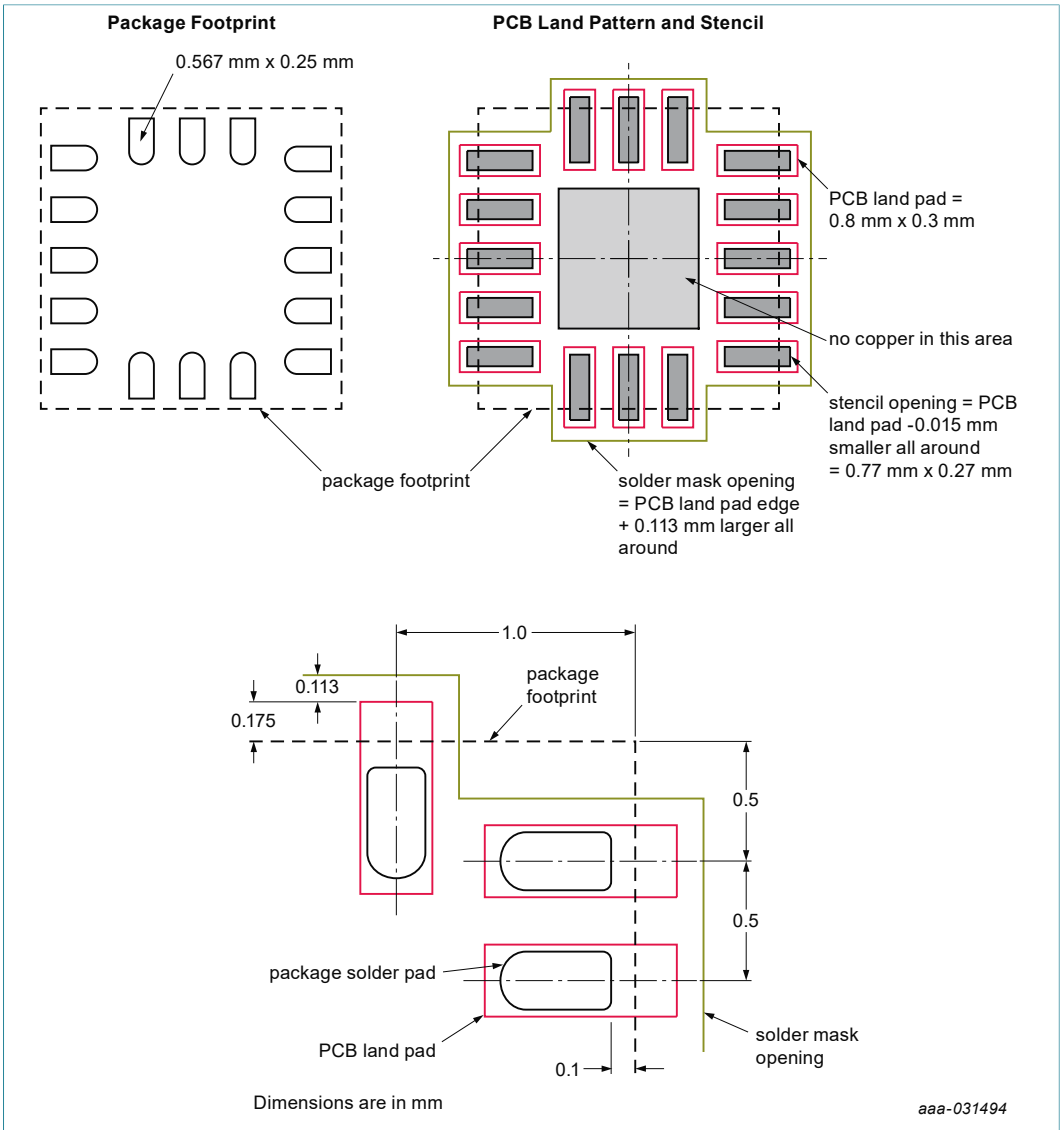


Figure 18. Recommended PCB land pattern, solder mask, and stencil opening near package footprint

20 Thermal characteristics

Table 162. Thermal characteristics

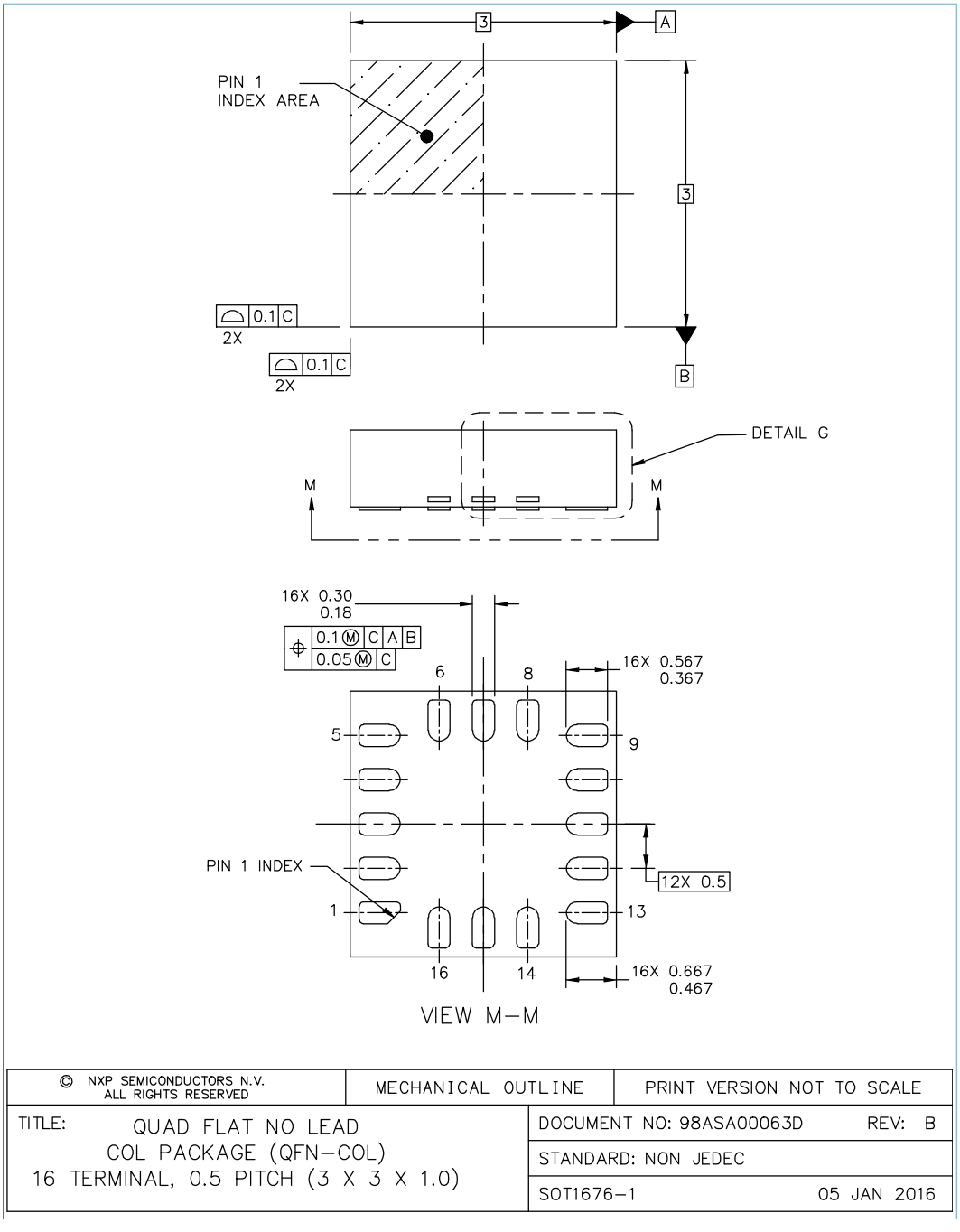
Rating	Description	Symbol	Value	Unit
Junction-to-ambient, natural convection[1][2]	Single-layer board	$R_{\theta JA}$	163	°C/W
Junction-to-ambient, natural convection[1][3]	Four-layer board (two signals, two planes)		70	
Junction-to-board[4]	—	$R_{\theta JB}$	33	°C/W
Junction-to-case (top)[5]	—	$R_{\theta JCTop}$	84	°C/W
Junction-to-package (top)[6]	Natural convection	Ψ_{JT}	6	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
[3] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

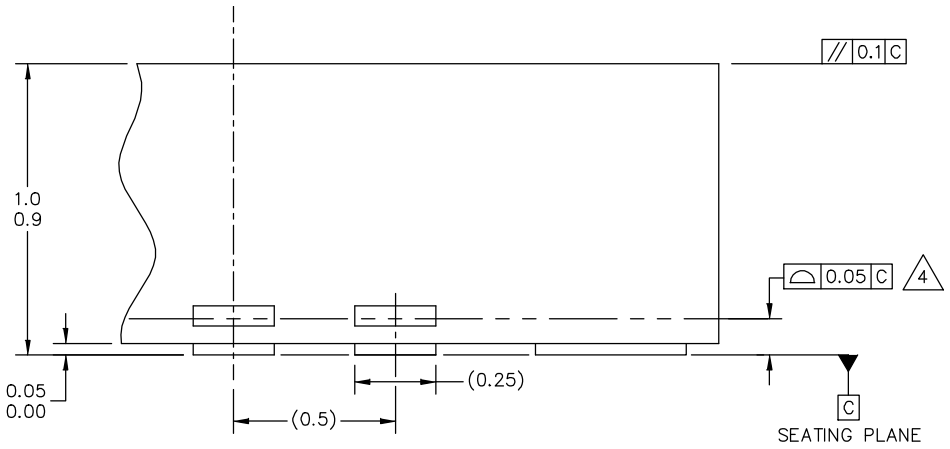
21 Package information

This drawing is located at

https://www.nxp.com/packages/SOT1676-1.



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QUAD FLAT NO LEAD COL PACKAGE (QFN–COL) 16 TERMINAL, 0.5 PITCH (3 X 3 X 1.0)	DOCUMENT NO: 98ASA00063D	REV: B
	STANDARD: NON JEDEC	
	SOT1676–1	05 JAN 2016



DETAIL G

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QUAD FLAT NO LEAD COL PACKAGE (QFN–COL) 16 TERMINAL, 0.5 PITCH (3 X 3 X 1.0)	DOCUMENT NO: 98ASA00063D	REV: B
	STANDARD: NON JEDEC	
	SOT1676–1	05 JAN 2016

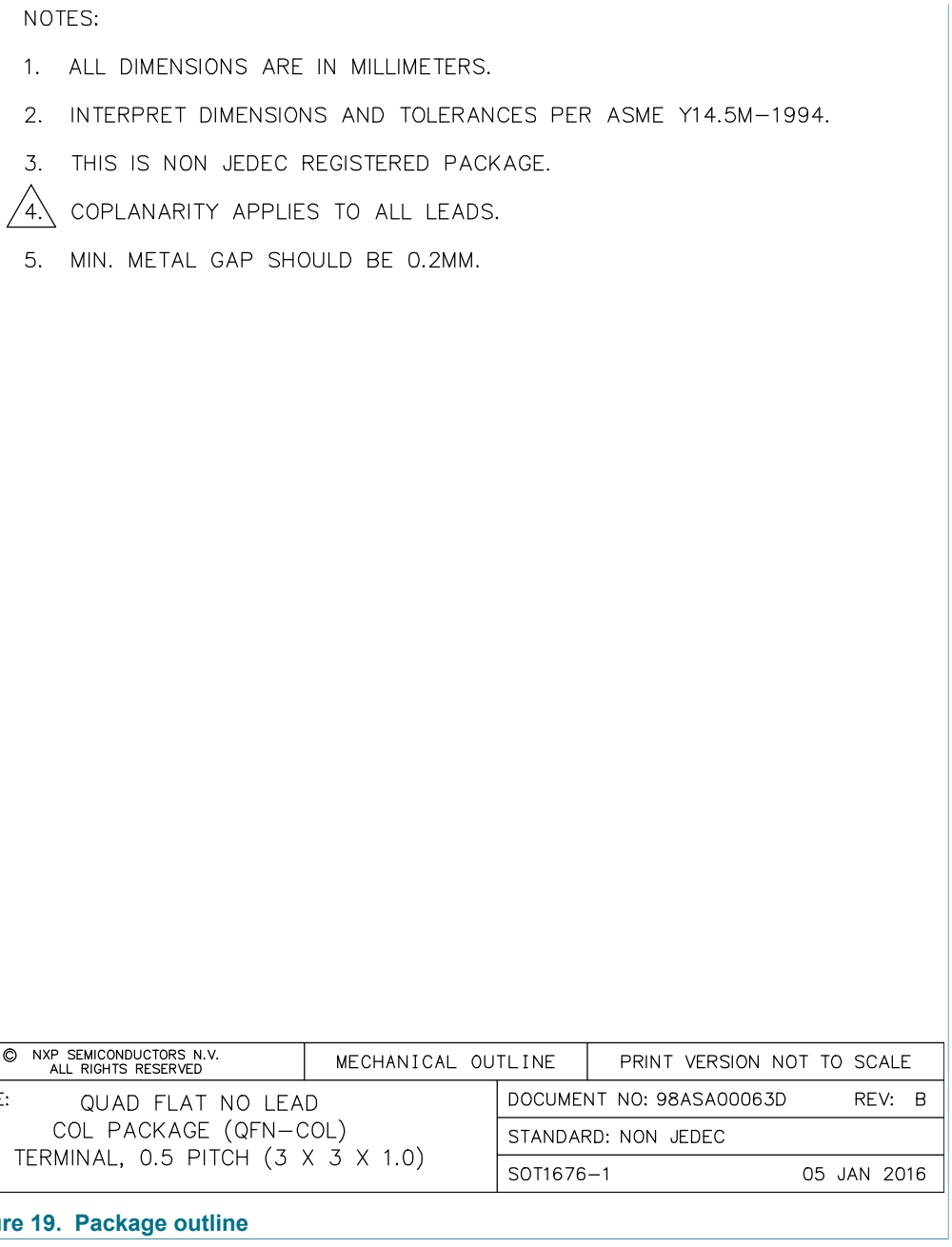


Figure 19. Package outline

22 Appendix A — Chip errata

22.1 SPI Mode soft-reset using CTRL_REG2 (2Bh), bit 6

22.1.1 Description

Following a soft-reset command, issued by setting CTRL_REG2[*rst*] = 1, certain device-specific parameters do not get updated correctly from NVM, causing inaccurate data output and incorrect WHO_AM_I (0Dh) register content. This behavior happens only in SPI mode and not in I^2C mode.

22.1.2 Workaround

Avoid using soft-reset in SPI mode by alternately utilizing the hardware RESET pin.

23 Revision history

Table 163. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FXLS8471Q v.3.0	20190613	Product data sheet	—	FXLS8471Q v.2.0
Modifications	• Section 1, Section 2: Removed "AEC-Q100, Grade 2 qualified" from each section. • Section 11, revised as follows: – Table 9: Revised I_{LU} as follows: – Removed the rating "Latchup current at T = 85 °C" and associated value "±100." – Revised the rating "Latchup current at T = 105 °C" to "Latchup current at T = 105 °C (per AEC-Q100-004)." – Revised the value from "±TBD" to "±100." – Revised the first caution icon folllowing Table 9. • Section 21, Figure 19: Revised package outline drawing from SOT1680-1 (98ASA00318D) to SOT1676-1 (98ASA00063D).			
FXLS8471Q v.2.0	20181120	Product data sheet	—	FXLS8471Q v.1.5
FXLS8471Q v.1.5	2015 June	Product data sheet	—	FXLS8471Q v.1.4
FXLS8471Q v.1.4	2015 March	Product data sheet	—	FXLS8471Q v.1.3
FXLS8471Q v.1.3	2015 January	Product data sheet	—	FXLS8471Q v.1.2
FXLS8471Q v.1.2	2014 November	Product data sheet	—	FXLS8471Q v.1.1
FXLS8471Q v.1.1	2013 August	Product data sheet	—	FXLS8471Q v.1.0
FXLS8471Q v.1.0	2013 August	Product data sheet	—	—

24 Legal information

24.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

24.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

24.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected

to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

24.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

NXP — is a trademark of NXP B.V.

Tables

Tab. 1. Ordering information 2
Tab. 2. Pin Description 3
Tab. 3. I2C slave timing values 6
Tab. 4. I2C slave address 7
Tab. 5. SPI timing 9
Tab. 6. Serial interface pin descriptions 11
Tab. 7. I2C/SPI auto detection 11
Tab. 8. Maximum ratings 12
Tab. 9. ESD and latchup protection characteristics 12
Tab. 10. Mechanical characteristics 13
Tab. 11. Electrical characteristics 14
Tab. 12. Temperature characteristics 15
Tab. 13. Mode of operation description 15
Tab. 14. Register address map 20
Tab. 15. STATUS register (address 00h) bit allocation 23
Tab. 16. STATUS register (address 00h) bit description 23
Tab. 17. DR_STATUS register (address 00h) bit allocation 23
Tab. 18. DR_STATUS register (address 00h) bit description 23
Tab. 19. F_STATUS register (address 00h) bit allocation 24
Tab. 20. FIFO flag event descriptions 25
Tab. 21. F_STATUS register (address 00h) bit description 25
Tab. 22. TRIG_CFG register (address 0Ah) bit allocation 25
Tab. 23. TRIG_CFG register (address 0Ah) bit description 25
Tab. 24. SYSMOD register (address 0Bh) bit allocation 26
Tab. 25. SYSMOD register (address 0Bh) bit description 26
Tab. 26. INT_SOURCE register (address 0Ch) bit allocation 27
Tab. 27. INT_SOURCE register (address 0Ch) bit description 27
Tab. 28. WHO_AM_I register (address 0Dh) bit allocation 28
Tab. 29. WHO_AM_I register (address 0Dh) bit description 28
Tab. 30. CTRL_REG1 register (address 2Ah) bit allocation 28
Tab. 31. CTRL_REG1 register (address 2Ah) bit description 28
Tab. 32. Sleep mode poll rate description - CTRL_REG6 = 00h 29
Tab. 33. System output data rate selection - CTRL_REG6 = 00h 29
Tab. 34. Sleep mode poll rate description – CTRL_REG6 = 03h 30
Tab. 35. System output data rate selection – CTRL_REG6 = 03h 30
Tab. 36. CTRL_REG2 register (address 2Bh) bit allocation 30
Tab. 37. CTRL_REG2 register (address 2Bh) bit description 30
Tab. 38. CTRL_REG2[smods/mods] oversampling modes 31
Tab. 39. Oversampling ratio versus oversampling mode 31
Tab. 40. CTRL_REG3 [interrupt control register] (address 2Ch) bit allocation 32
Tab. 41. CTRL_REG3 [Interrupt control register] (address 2Ch) bit descriptions 32
Tab. 42. CTRL_REG4 [Interrupt enable register] (address 2Dh) bit allocation 33
Tab. 43. CTRL_REG4 [Interrupt enable register] (address 2Dh) bit descriptions 33
Tab. 44. CTRL_REG5 [Interrupt Routing Configuration Register] (address 2Eh) bit allocation 34
Tab. 45. CTRL_REG5 [Interrupt Routing Configuration Register] (address 2Eh) bit descriptions 34
Tab. 46. CTRL_REG6 register (address 5Bh) bit allocation 36
Tab. 47. CTRL_REG6 register (address 5Bh) bit descriptions 36
Tab. 48. CTRL_REG7 register (address 5Ch) bit allocation 36
Tab. 49. CTRL_REG7 register (address 5Ch) bit descriptions 36
Tab. 50. ASLP_COUNT register (address 29h) bit allocation 37
Tab. 51. ASLP_COUNT register (address 29h) bit description 37
Tab. 52. ASLP_COUNT relationship with ODR 37
Tab. 53. Sleep/Wake mode gates and triggers 37
Tab. 54. TEMP_OUT register (address 51h) bit allocation 39
Tab. 55. OUT_X_MSB register (address 01h) bit allocation 40
Tab. 56. OUT_X_LSB register (address 02h) bit allocation 40
Tab. 57. OUT_Y_MSB register (address 03h) bit allocation 40
Tab. 58. OUT_Y_LSB register (address 04h) bit allocation 40
Tab. 59. OUT_Z_MSB register (address 05h) bit allocation 40
Tab. 60. OUT_Z_LSB register (address 06h) bit allocation 41
Tab. 61. F_SETUP register (address 09h) bit allocation 41
Tab. 62. F_SETUP register (address 09h) bit descriptions 41
Tab. 63. XYZ_DATA_CFG register (address 0Eh) bit allocation 42

Tab. 64. XYZ_DATA_CFG register (address 0Eh) bit descriptions 42
Tab. 65. Accelerometer full-scale range selection 42
Tab. 66. HP_FILTER_CUTOFF register (address 0Fh) bit allocation 43
Tab. 67. HP_FILTER_CUTOFF register (address 0Fh) bit descriptions 43
Tab. 68. HP_FILTER_CUTOFF 43
Tab. 69. PL_STATUS register (address 10h) bit allocation 45
Tab. 70. PL_STATUS register (address 10h) bit descriptions 45
Tab. 71. PL_CFG register (address 11h) bit allocation 46
Tab. 72. PL_CFG register (address 11h) bit descriptions 46
Tab. 73. PL_COUNT register (address 12h) bit allocation 46
Tab. 74. PL_COUNT register (address 12h) bit descriptions 46
Tab. 75. PL_Count Relationship with the ODR 47
Tab. 76. PL_BF_ZCOMP register (address 13h) bit allocation 47
Tab. 77. PL_BF_ZCOMP register (address 13h) bit descriptions 47
Tab. 78. Z-lockout angle definitions 47
Tab. 79. Back/Front orientation definitions 48
Tab. 80. PL_THS_REG register (address 14h) bit allocation 48
Tab. 81. PL_BF_ZCOMP register (address 13h) bit descriptions 48
Tab. 82. Threshold angle lookup table 48
Tab. 83. Trip angles versus hysteresis settings 49
Tab. 84. Portrait/Landscape ideal orientation definitions 49
Tab. 85. A_FFMT_CFG register (address 15h) bit allocation 50
Tab. 86. A_FFMT_CFG register (address 15h) bit descriptions 50
Tab. 87. A_FFMT_SRC register (address 16h) bit allocation 51
Tab. 88. A_FFMT_SRC register (address 16h) bit descriptions 51
Tab. 89. A_FFMT_THS register (address 17h) bit allocation 52
Tab. 90. A_FFMT_THS register (address 17h) bit descriptions 52
Tab. 91. A_FFMT_THS_X_MSB register (address 73h) bit allocation 52
Tab. 92. A_FFMT_THS_X_MSB register (address 73h) bit descriptions 53
Tab. 93. A_FFMT_THS_X_LSB register (address 74h) bit allocation 53
Tab. 94. A_FFMT_THS_X_LSB register (address 74h) bit descriptions 53
Tab. 95. A_FFMT_THS_Y_MSB register (address 75h) bit allocation 53
Tab. 96. A_FFMT_THS_Y_MSB register (address 75h) bit descriptions 53
Tab. 97. A_FFMT_THS_Y_LSB register (address 76h) bit allocation 54
Tab. 98. A_FFMT_THS_Y_LSB register (address 76h) bit descriptions 54
Tab. 99. A_FFMT_THS_Z_MSB register (address 77h) bit allocation 54
Tab. 100. A_FFMT_THS_Z_MSB register (address 77h) bit descriptions 54
Tab. 101. A_FFMT_THS_Z_LSB register (address 78h) bit allocation 54
Tab. 102. A_FFMT_THS_Z_LSB register (address 78h) bit descriptions 54
Tab. 103. A_FFMT_COUNT register (address 18h) bit allocation 55
Tab. 104. A_FFMT_COUNT register (address 18h) bit description 55
Tab. 105. A_FFMT_COUNT relationship with the ODR 55
Tab. 106. A_VECM_CFG register (address 5Fh) bit allocation 57
Tab. 107. A_VECM_CFG register (address 5Fh) bit descriptions 57
Tab. 108. A_VECM_THS_MSB register (address 60h) bit allocation 57
Tab. 109. A_VECM_THS_MSB register (address 60h) bit descriptions 58
Tab. 110. A_VECM_THS_LSB register (address 61h) bit allocation 58
Tab. 111. A_VECM_THS_LSB bit description 58
Tab. 112. A_VECM_CNT register (address 62h) bit allocation 58
Tab. 113. A_VECM_CNT bit description 58
Tab. 114. A_VECM_INITX_MSB register (address 63h) bit allocation 59
Tab. 115. A_VECM_INITX_MSB register (address 63h) bit description 59
Tab. 116. A_VECM_INITX_LSB register (address 64h) bit allocation 59
Tab. 117. A_VECM_INITX_LSB register (address 64h) bit description 59
Tab. 118. A_VECM_INITY_MSB register (address 65h) bit allocation 59
Tab. 119. A_VECM_INITY_MSB register (address 65h) bit description 59
Tab. 120. A_VECM_INITY_LSB register (address 66h) bit allocation 60
Tab. 121. A_VECM_INITY_LSB register (address 66h) bit description 60
Tab. 122. A_VECM_INITZ_MSB register (address 67h) bit allocation 60
Tab. 123. A_VECM_INITZ_MSB register (address 67h) bit description 60
Tab. 124. A_VECM_INITZ_LSB register (address 68h) bit allocation 60
Tab. 125. A_VECM_INITZ_LSB bit description 60
Tab. 126. TRANSIENT_CFG register (address 1Dh) bit allocation 61
Tab. 127. TRANSIENT_CFG register (address 1Dh) bit descriptions 61

Tab. 128. TRANSIENT_SRC register (address 1Eh) bit allocation 62
Tab. 129. TRANSIENT_SRC register (address 1Eh) bit descriptions 62
Tab. 130. TRANSIENT_THS register (address 1Fh) bit allocation 63
Tab. 131. TRANSIENT_THS register (address 1Fh) bit descriptions 63
Tab. 132. TRANSIENT_COUNT register (address 20h) bit allocation 63
Tab. 133. TRANSIENT_COUNT register (address 20h) bit description 63
Tab. 134. TRANSIENT_COUNT relationship with the ODR 64
Tab. 135. PULSE_CFG register (address 21h) bit allocation 64
Tab. 136. PULSE_CFG register (address 21h) bit descriptions 64
Tab. 137. PULSE_SRC register (address 22h) bit allocation 65
Tab. 138. PULSE_SRC register (address 22h) bit descriptions 65
Tab. 139. PULSE_THSX register (address 23h) bit allocation 66
Tab. 140. PULSE_THSX register (address 23h) bit description 66
Tab. 141. PULSE_THSY register (address 24h) bit allocation 66
Tab. 142. PULSE_THSY register (address 24h) bit description 67
Tab. 143. PULSE_THSZ register (address 25h) bit description 67
Tab. 144. PULSE_TMLT register (address 26h) bit allocation 67
Tab. 145. PULSE_TMLT register (address 26h) bit description 67
Tab. 146. Time step for PULSE_TMLT with HP_FILTER_CUTOFF[pls_hpf_en] = 1 68
Tab. 147. Time step for PULSE_TMLT with HP_FILTER_CUTOFF[pls_hpf_en] = 0 68
Tab. 148. PULSE_LTCY register (address 27h) bit allocation 68
Tab. 149. PULSE_LTCY register (address 27h) bit description 68
Tab. 150. Time step for PULSE_LTCY with HP_FILTER_CUTOFF[pls_hpf_en] = 1 69
Tab. 151. Time step for PULSE_LTCY with HP_FILTER_CUTOFF[pls_hpf_en] = 0 69
Tab. 152. PULSE_WIND register (address 28h) bit allocation 69
Tab. 153. PULSE_WIND register (address 28h) bit description 70
Tab. 154. Time step for PULSE_WIND with HP_FILTER_CUTOFF[pls_hpf_en] = 1 70
Tab. 155. Time step for PULSE_WIND with HP_FILTER_CUTOFF[pls_hpf_en] = 0 70
Tab. 156. OFF_X register (address 2Fh) bit allocation 71
Tab. 157. OFF_X register (address 2Fh) bit description 71
Tab. 158. OFF_Y register (address 30h) bit allocation 71
Tab. 159. OFF_Y register (address 30h) bit description 71
Tab. 160. OFF_Z register (address 31h) bit allocation 71
Tab. 161. OFF_Z register (address 31h) bit description 72
Tab. 162. Thermal characteristics 74
Tab. 163. Revision history 79

Figures

Fig. 1. Block diagram 2
Fig. 2. Pinning 3
Fig. 3. Product orientation and axis orientation 4
Fig. 4. Electrical connection 5
Fig. 5. I2C slave timing diagram 6
Fig. 6. I2C timing diagram 9
Fig. 7. SPI timing diagram 10
Fig. 8. SPI single-burst read/write transaction diagram 11
Fig. 9. FXLS8471Q power mode transition diagram 15
Fig. 10. Interrupt controller block diagram 35
Fig. 11. INT1/INT2 event flag logic example 35
Fig. 12. Auto-sleep state transition diagram 38
Fig. 13. Illustration of Z-tilt angle lockout transition 44
Fig. 14. Illustration of landscape to portrait transition 44
Fig. 15. Illustration of portrait to landscape transition 45
Fig. 16. A_FFMT_THS high and low-g level 54
Fig. 17. Behavior of the A_FFMT debounce counter in relation to the a_ffmt_dbcntm setting 56
Fig. 18. Recommended PCB land pattern, solder mask, and stencil opening near package footprint 73
Fig. 19. Package outline 75

Contents

1 General description 1
2 Features and benefits 1
3 Typical applications 1
4 Ordering information 2
5 Block Diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 Orientation 4
8 Electrical connections 4
9 Terminology 5
9.1 Sensitivity 5
9.2 Zero-g offset 5
9.3 Self-test 5
10 Digital interfaces 6
10.1 I2C interface characteristics 6
10.1.1 General I2C operation 6
10.1.2 I2C read/write operations 7
10.2 SPI interface characteristics 9
10.2.1 General SPI operation 10
10.2.2 SPI READ/WRITE operations 10
10.2.3 I2C/SPI auto detection 11
10.2.4 Power supply sequencing and I2C/SPI mode auto-detection 11
11 Absolute maximum ratings 12
12 Mechanical characteristics 13
13 Electrical characteristics 14
14 Temperature sensor characteristics 15
15 Modes of operation 15
16 Embedded functionality 16
16.1 Factory calibration 16
16.2 8-bit or 14-bit data 16
16.3 Low-power modes versus high-resolution modes 17
16.4 Auto-Wake and Auto-Sleep modes 17
16.5 Free-fall and Motion event detection 17
16.5.1 Free fall detection 18
16.5.2 Motion detection 18
16.6 Transient detection 18
16.7 Pulse detection 19
16.8 Orientation detection 19
16.9 Acceleration vector-magnitude detection 19
17 Register Map 20
18 Register descriptions by functional block 23
18.1 Device configuration registers 23
18.1.1 STATUS register (address 00h) 23
18.1.2 DR_STATUS register (address 00h) 23
18.1.3 F_STATUS register (address 00h) 24
18.1.4 TRIG_CFG register (address 0Ah) 25
18.1.5 SYSMOD register (address 0Bh) 26
18.1.6 INT_SOURCE register (address 0Ch) 26
18.1.7 WHO_AM_I register (address 0Dh) 28
18.1.8 CTRL_REG1 register (address 2Ah) 28
18.1.9 CTRL_REG2 register (address 2Bh) 30
18.1.10 CTRL_REG3 - interrupt control register (address 2Ch) 32
18.1.11 CTRL_REG4 - interrupt enable register (address 2Dh) 33
18.1.12 CTRL_REG5 - interrupt routing configuration register (address 2Eh) 34
18.1.13 CTRL_REG6 - register (address 5Bh) 36
18.1.14 CTRL_REG7 - register (address 5Ch) 36
18.2 Auto-Sleep trigger register 37
18.2.1 ASLP_COUNT register (address 29h) 37
18.3 Temperature register 39
18.3.1 TEMP_OUT register (address 51h) 39
18.4 Output data registers 39
18.4.1 OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB registers (addresses 01h to 06h) 39
18.5 FIFO registers 41
18.5.1 F_SETUP register (address 09h) 41
18.6 Sensor data configuration registers 42
18.6.1 XYZ_DATA_CFG register (address 0Eh) 42
18.7 High-pass filter register 42
18.7.1 HP_FILTER_CUTOFF register (address 0Fh) 42
18.8 Portrait/Landscape detection registers 44
18.8.1 PL_STATUS register (address 10h) 45
18.8.2 PL_CFG register (address 11h) 46
18.8.3 PL_COUNT register (address 12h) register 46
18.8.4 PL_BF_ZCOMP register (address 13h) 47
18.8.5 PL_THS_REG register (address 14h) 48
18.9 Free-fall and Motion event detection 49
18.9.1 A_FFMT_CFG register (address 15h) 50
18.9.2 A_FFMT_SRC register (address 16h) 51
18.9.3 A_FFMT_THSxxxxxx registers (addresses 17h, 73h to 78h) 52
18.9.4 A_FFMT_COUNT register (address 18h) 55
18.10 Accelerometer vector-magnitude function registers 56
18.10.1 A_VECM_CFG register (address 5Fh) 57
18.10.2 A_VECM_THS_MSB register (address 60h) ... 57
18.10.3 A_VECM_THS_LSB register (address 61h) 58
18.10.4 A_VECM_CNT register (address 62h) 58
18.10.5 A_VECM_INITX_MSB register (address 63h) 59
18.10.6 A_VECM_INITX_LSB register (address 64h) 59
18.10.7 A_VECM_INITY_MSB register (address 65h) 59
18.10.8 A_VECM_INITY_LSB register (address 66h) 60
18.10.9 A_VECM_INITZ_MSB register (address 67h) 60
18.10.10 A_VECM_INITZ_LSB register (address 68h) ... 60
18.11 Transient (AC) acceleration detection registers 61
18.11.1 TRANSIENT_CFG register (address 1Dh) 61
18.11.2 TRANSIENT_SRC register (address 1Eh) 62
18.11.3 TRANSIENT_THS register (address 1Fh) 63

18.11.4 TRANSIENT_COUNT register (address 20h) 63
18.12 Pulse detection registers 64
18.12.1 PULSE_CFG register (address 21h) 64
18.12.2 PULSE_SRC register (address 22h) 65
18.12.3 PULSE_THSX register (address 23h) 66
18.12.4 PULSE_THSY register (address 24h) 66
18.12.5 PULSE_THSZ register (address 25h)ULSE_ THSZ register (address 25h) bit allocation 67
18.12.6 PULSE_TMLT register (address 26h) 67
18.12.7 PULSE_LTCY register (address 27h) 68
18.12.8 PULSE_WIND register (address 28h) 69
18.13 Offset correction registers 70
18.13.1 OFF_X register (address 2Fh) 71
18.13.2 OFF_Y register (address 30h) 71
18.13.3 OFF_Z register (address 31h) 71
19 Mounting guidelines for the Quad Flat No-Lead (QFN) package 72
19.1 Overview of soldering considerations 72
19.2 Halogen content 72
19.3 PCB mounting recommendations 72
20 Thermal characteristics 74
21 Package information 75
22 Appendix A — Chip errata 78
22.1 SPI Mode soft-reset using CTRL_REG2 (2Bh), bit 6 78
22.1.1 Description 78
22.1.2 Workaround 78
23 Revision history 79
24 Legal information 80

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 June 2019
Document identifier: FXLS8471Q

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А