

# 74HC4094; 74HCT4094

## 8-stage shift-and-store bus register

Rev. 8 — 14 November 2018

Product data sheet

## 1. General description

The 74HC4094; 74HCT4094 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to-HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Complies with JEDEC standard JESD7A
- Input levels:
  - For 74HC4094: CMOS level
  - For 74HCT4094: TTL level
- Low-power dissipation
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

## 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4094D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4094D				
74HC4094DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4094DB				
74HC4094PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 5. Functional diagram

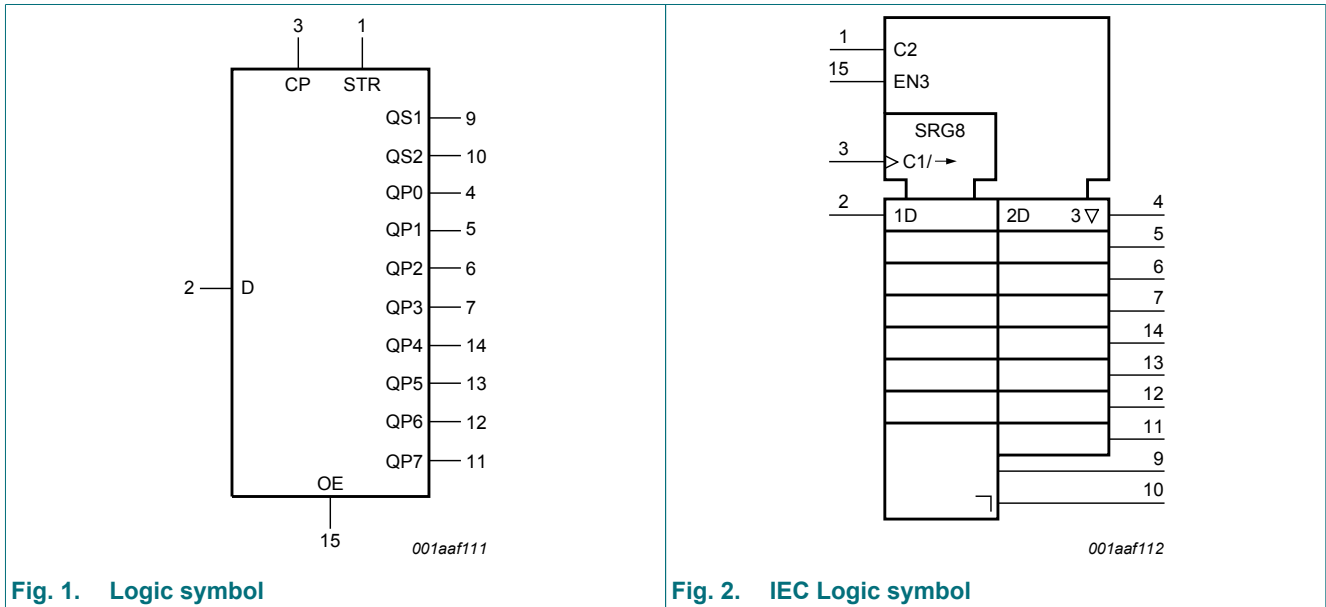


Fig. 1. Logic symbol

Fig. 2. IEC Logic symbol

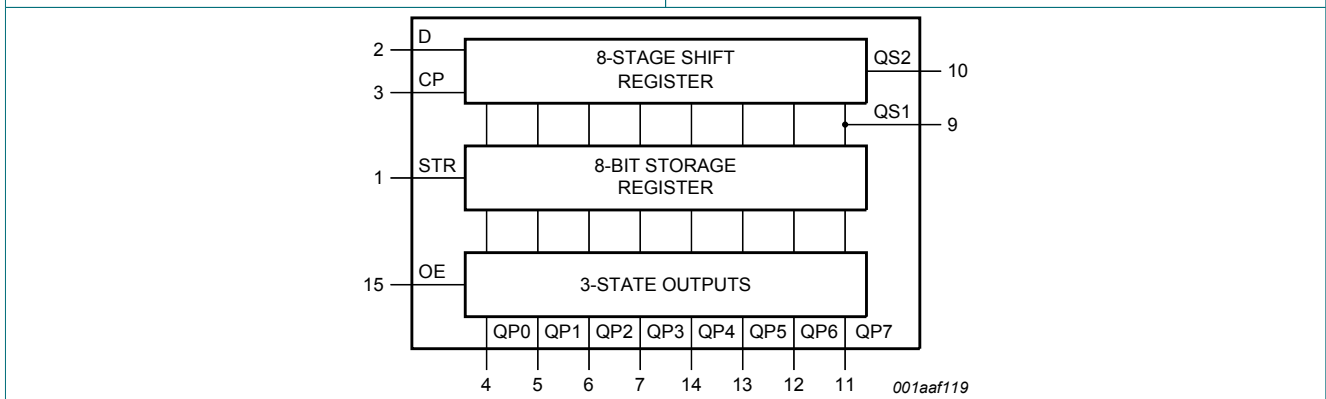


Fig. 3. Functional diagram

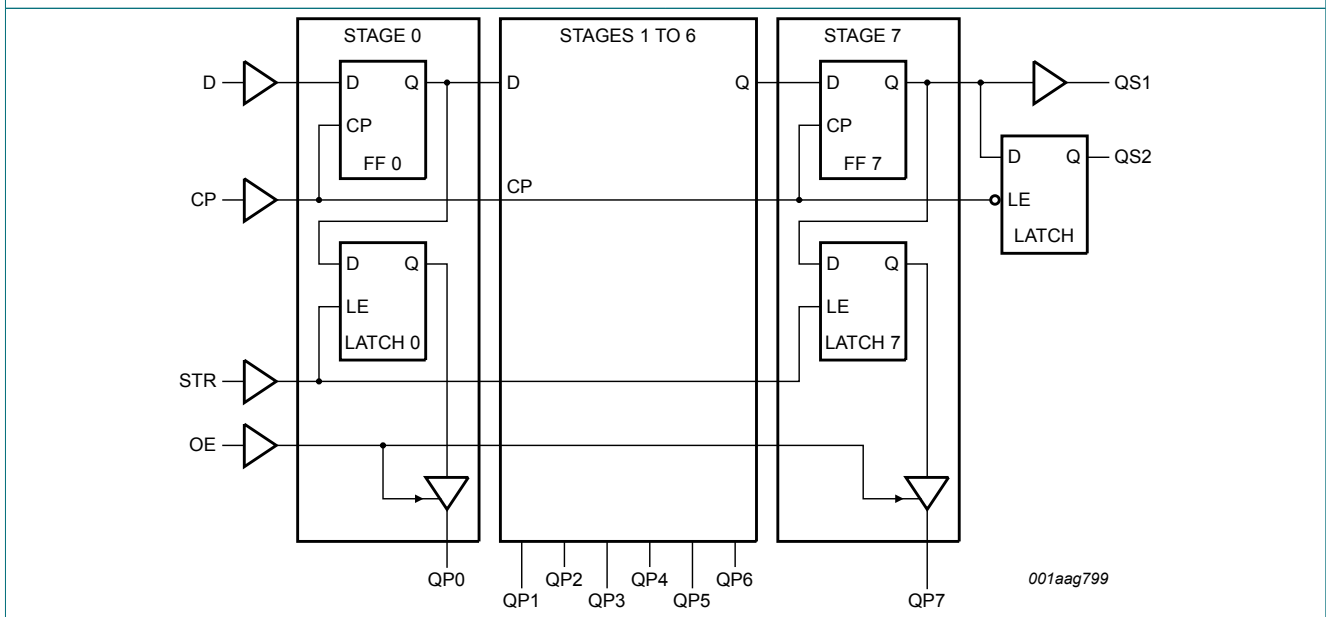
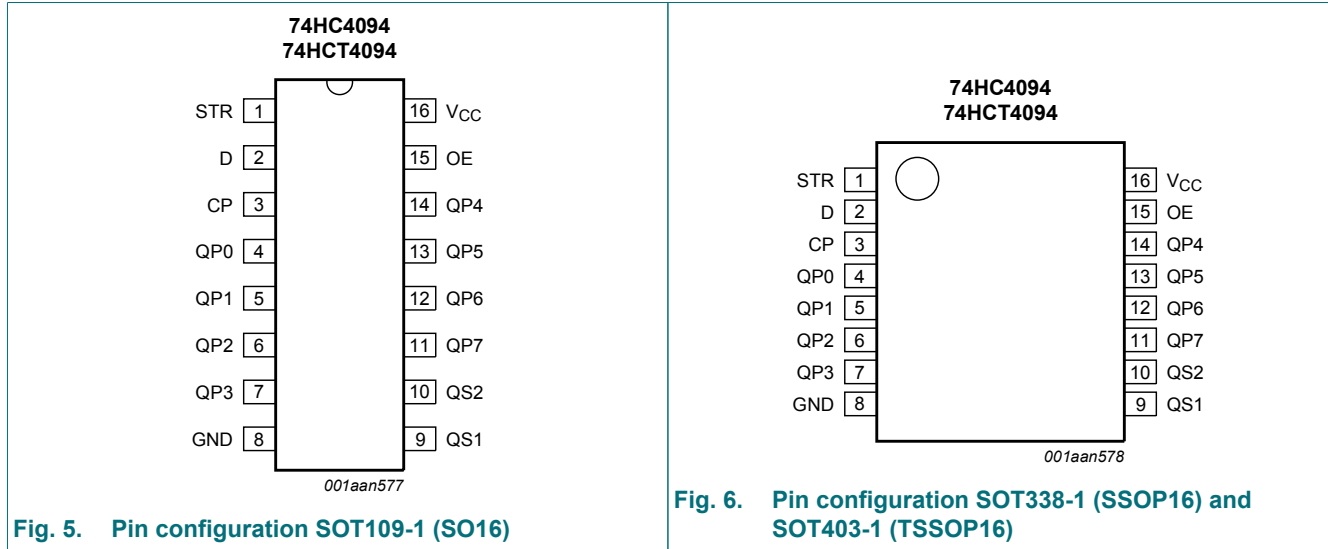


Fig. 4. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
GND	8	ground supply voltage
QS1, QS2	9, 10	serial output
OE	15	output enable input
V <sub>CC</sub>	16	supply voltage

## 7. Functional description

**Table 3. Function table**

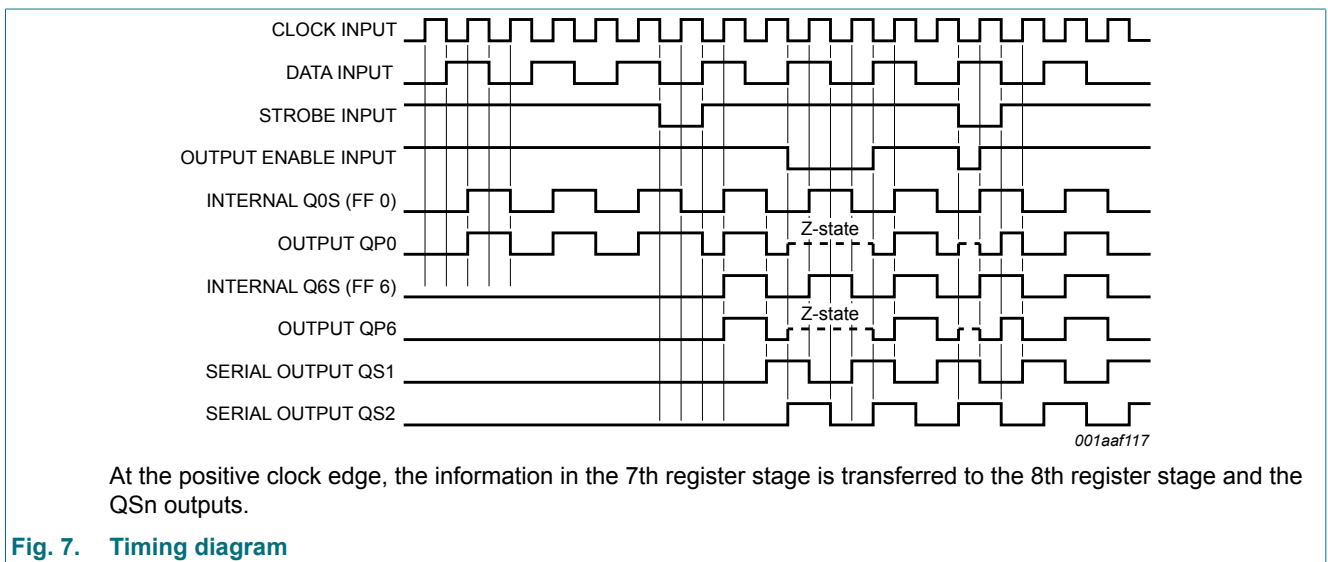
H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = HIGH-impedance OFF-state; NC = no change;

↑ = positive-going transition; ↓ = negative-going transition;

Q6S = the data in register stage 6 before the LOW to HIGH clock transition;

Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

Inputs				Parallel outputs		Serial outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn - 1	Q6S	NC
↑	H	H	H	H	QPn - 1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S



**Fig. 7. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	SO16, SSOP16 and TSSOP16 packages [1]	-	500	mW

[1] For SO16:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

For SSOP16 and TSSOP16 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4094			74HCT4094			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4094</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT4094</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		per input pin; STR input	-	100	360	-	450	-	490	µA
		per input pin; OE input	-	150	540	-	675	-	735	µA
		per input pin; CP input	-	150	540	-	675	-	735	µA
	per input pin; D input	-	40	144	-	180	-	196	µA	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see Fig. 12.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4094</b>										
$t_{pd}$	propagation delay	CP to QS1; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
		CP to QS2; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	44	135	-	170	-	205	ns
		$V_{CC} = 4.5$ V	-	16	27	-	34	-	41	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	13	23	-	29	-	35	ns
		CP to QPn; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	63	195	-	245	-	295	ns
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	33	-	42	-	50	ns
		STR to QPn; see Fig. 9 [1]								
$V_{CC} = 2.0$ V	-	58	180	-	225	-	270	ns		
$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	17	31	-	38	-	46	ns		
$t_{en}$	enable time	OE to QPn; see Fig. 10 [1]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
$t_{dis}$	disable time	OE to QPn; see Fig. 10 [1]								
		$V_{CC} = 2.0$ V	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	15	25	-	31	-	38	ns
		$V_{CC} = 6.0$ V	-	12	21	-	26	-	32	ns
$t_t$	transition time	QPn and QSn; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns



Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	14	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	4	-	17	-	20	-	ns
		STR HIGH; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	80	14	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns
V <sub>CC</sub> = 6.0 V	14	4	-	17	-	20	-	ns		
t <sub>su</sub>	set-up time	D to CP; see Fig. 11								
		V <sub>CC</sub> = 2.0 V	50	14	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	5	-	13	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	9	4	-	11	-	13	-	ns
		CP to STR; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	100	28	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	10	-	25	-	30	-	ns
V <sub>CC</sub> = 6.0 V	17	8	-	21	-	26	-	ns		
t <sub>h</sub>	hold time	D to CP; see Fig. 11								
		V <sub>CC</sub> = 2.0 V	3	-6	-	3	-	3	-	ns
		V <sub>CC</sub> = 4.5 V	3	-2	-	3	-	3	-	ns
		V <sub>CC</sub> = 6.0 V	3	-2	-	3	-	3	-	ns
		CP to STR; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	0	-14	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-5	-	0	-	0	-	ns
V <sub>CC</sub> = 6.0 V	0	-4	-	0	-	0	-	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	6.0	28	-	4.8	-	4.0	-	MHz
		V <sub>CC</sub> = 4.5 V	30	87	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	95	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	103	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [2]	-	83	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT4094</b>										
$t_{pd}$	propagation delay	CP to QS1; see <a href="#">Fig. 8</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	23	39	-	49	-	59	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	19	-	-	-	-	-	ns
		CP to QS2; see <a href="#">Fig. 8</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	21	36	-	45	-	54	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	18	-	-	-	-	-	ns
		CP to QPn; see <a href="#">Fig. 8</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	25	43	-	54	-	65	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	21	-	-	-	-	-	ns
		STR to QPn; see <a href="#">Fig. 9</a> [1]								
$V_{CC} = 4.5\text{ V}$	-	22	39	-	49	-	59	ns		
$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	19	-	-	-	-	-	ns		
$t_{en}$	enable time	OE to QPn; see <a href="#">Fig. 10</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	20	35	-	44	-	53	ns
$t_{dis}$	disable time	OE to QPn; see <a href="#">Fig. 10</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	21	35	-	44	-	53	ns
$t_t$	transition time	QPn and QSn; see <a href="#">Fig. 8</a> [1]								
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
$t_W$	pulse width	CP HIGH or LOW; see <a href="#">Fig. 8</a>								
		$V_{CC} = 4.5\text{ V}$	16	7	-	20	-	24	-	ns
		STR HIGH; see <a href="#">Fig. 9</a>								
$V_{CC} = 4.5\text{ V}$	16	5	-	20	-	24	-	ns		
$t_{su}$	set-up time	Dn to CP; see <a href="#">Fig. 11</a>								
		$V_{CC} = 4.5\text{ V}$	10	4	-	13	-	15	-	ns
		CP to STR; see <a href="#">Fig. 9</a>								
$V_{CC} = 4.5\text{ V}$	20	9	-	25	-	30	-	ns		
$t_h$	hold time	Dn to CP; see <a href="#">Fig. 11</a>								
		$V_{CC} = 4.5\text{ V}$	4	0	-	4	-	4	-	ns
		CP to STR; see <a href="#">Fig. 9</a>								
$V_{CC} = 4.5\text{ V}$	0	-4	-	0	-	0	-	ns		
$f_{max}$	maximum frequency	CP; see <a href="#">Fig. 8</a>								
		$V_{CC} = 4.5\text{ V}$	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	86	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}; f = 1\text{ MHz}; V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [2]	-	92	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

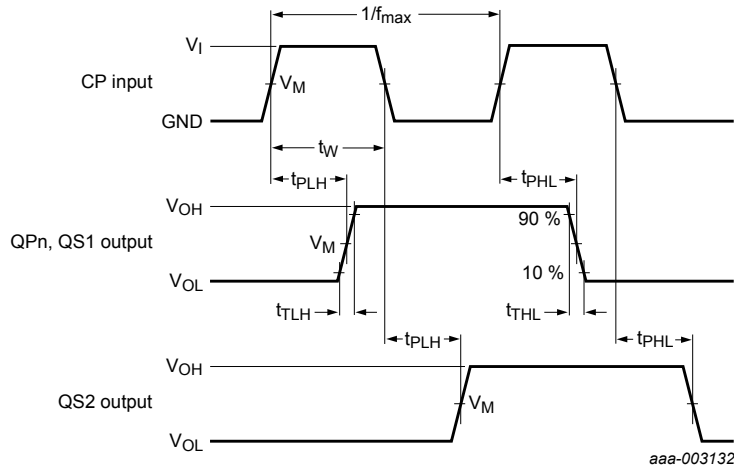
[2]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;  $C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V; N = number of inputs switching;  $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

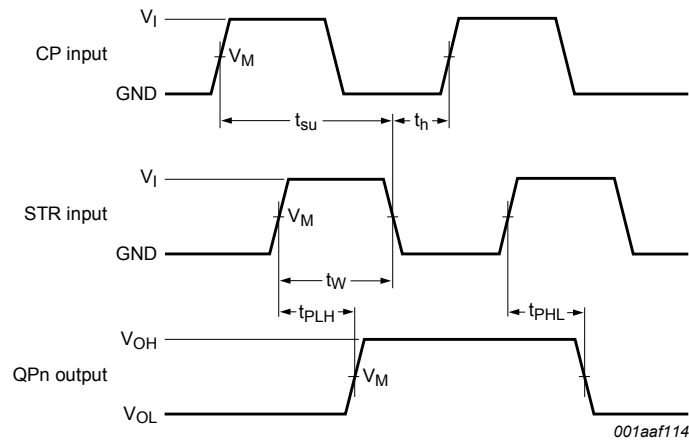
11.1. Waveforms and test circuits



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

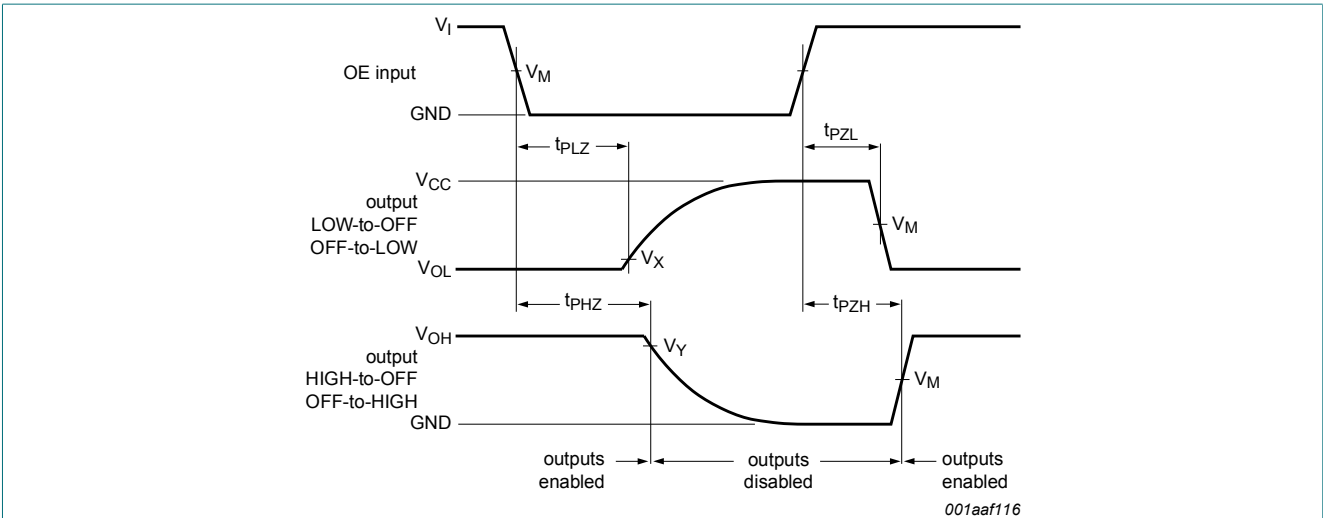
**Fig. 8.** Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

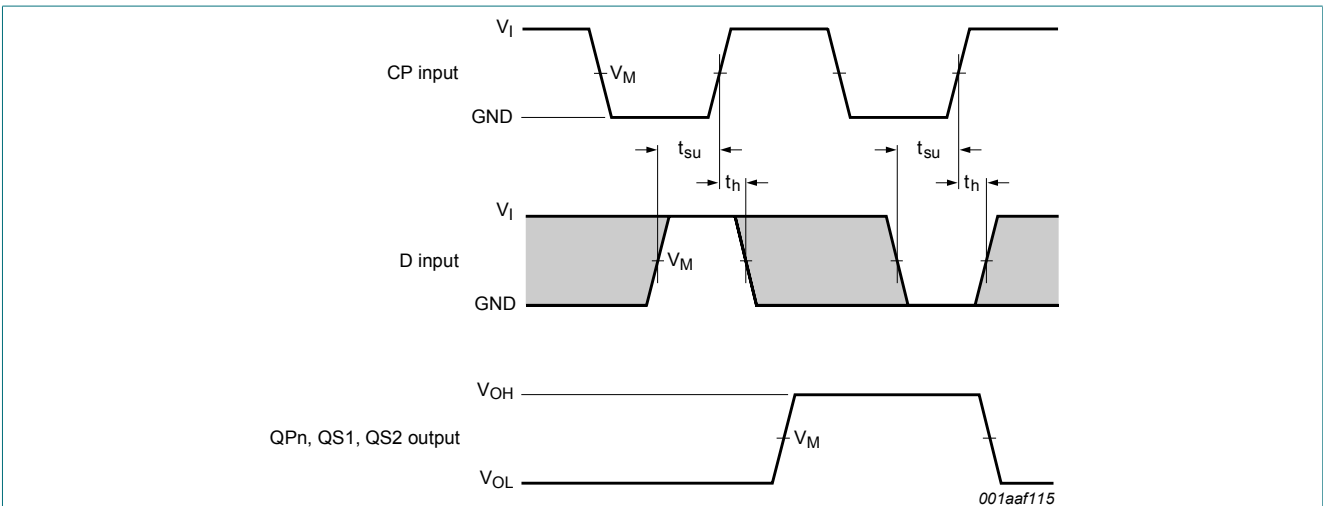
**Fig. 9.** Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 10. Enable and disable times**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 11. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC4094	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{OH}$	$0.9V_{OH}$
74HCT4094	1.3 V	1.3 V	$0.1V_{OH}$	$0.9V_{OH}$

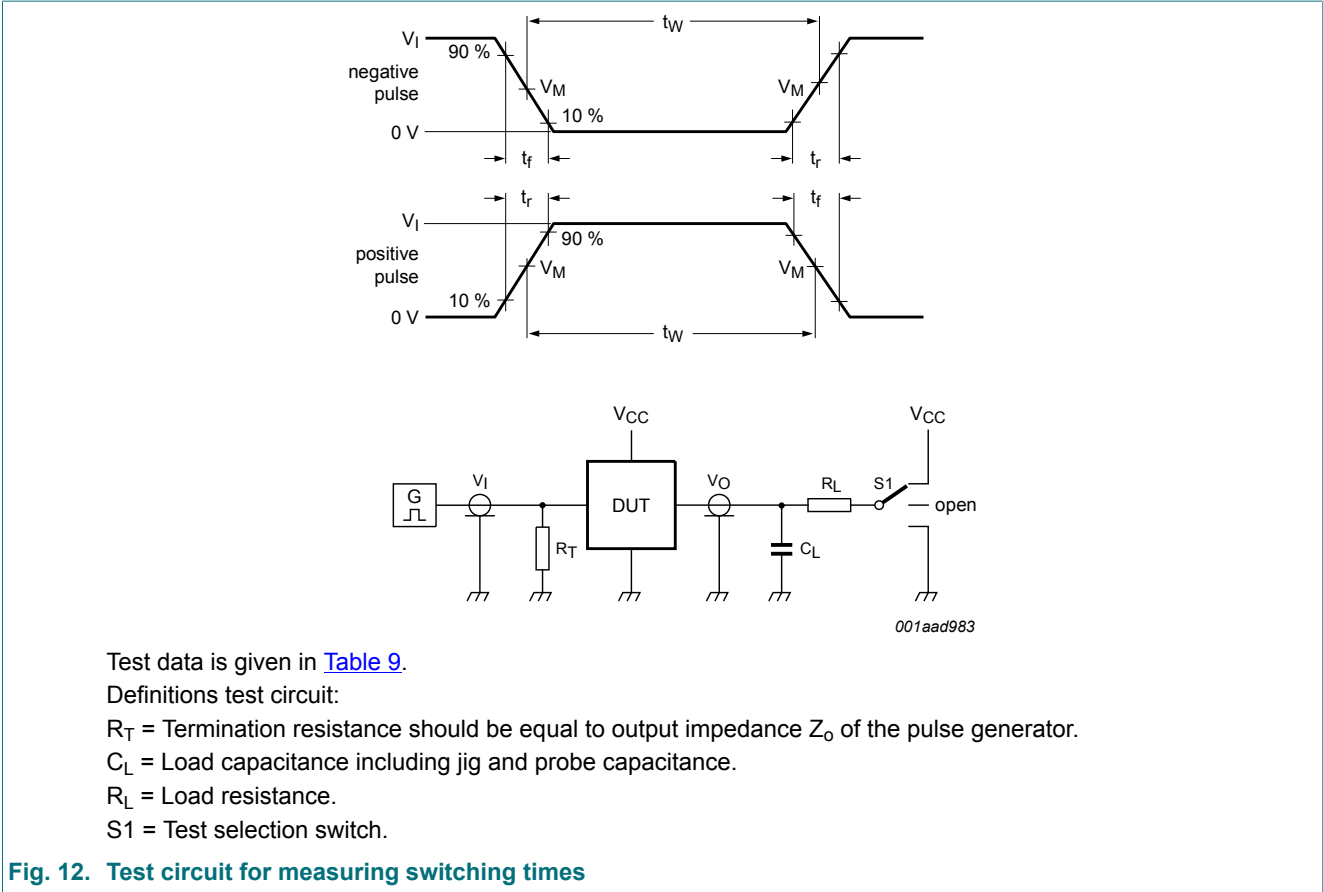


Fig. 12. Test circuit for measuring switching times

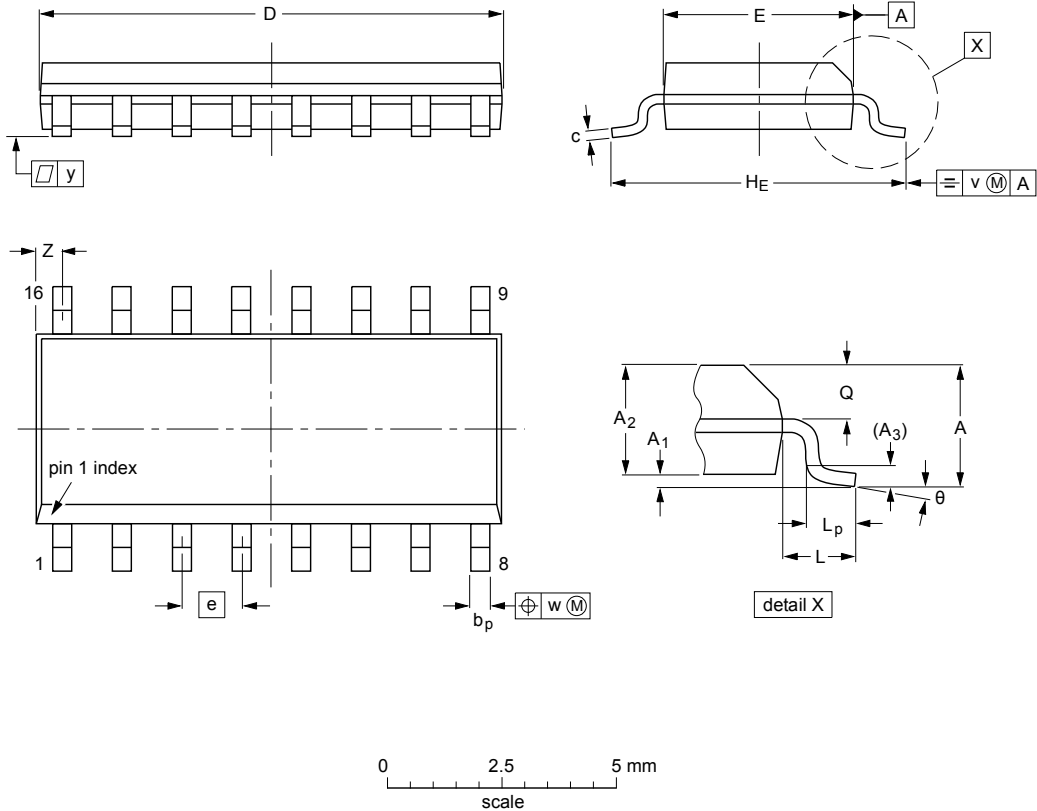
Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC4094	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT4094	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

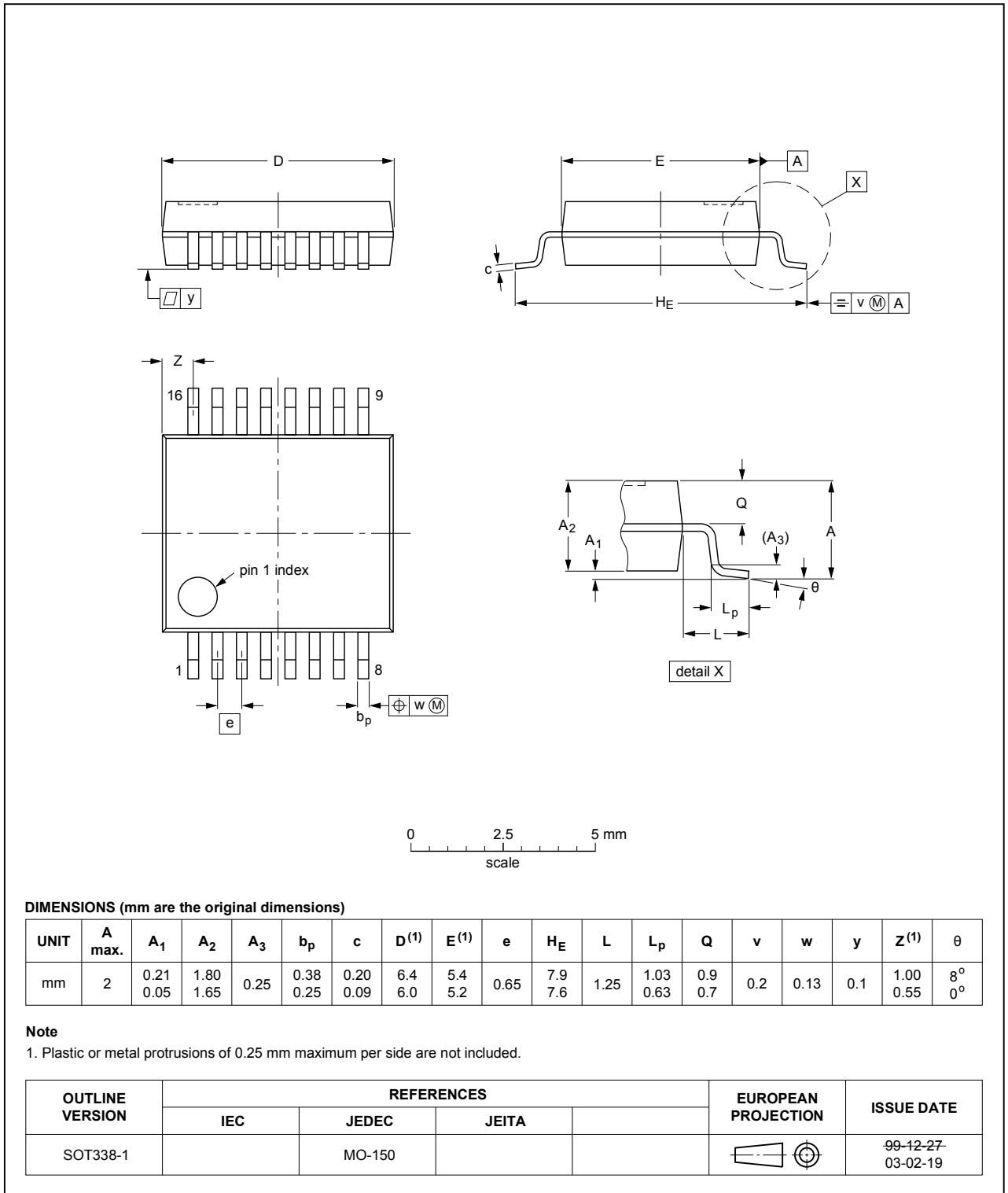
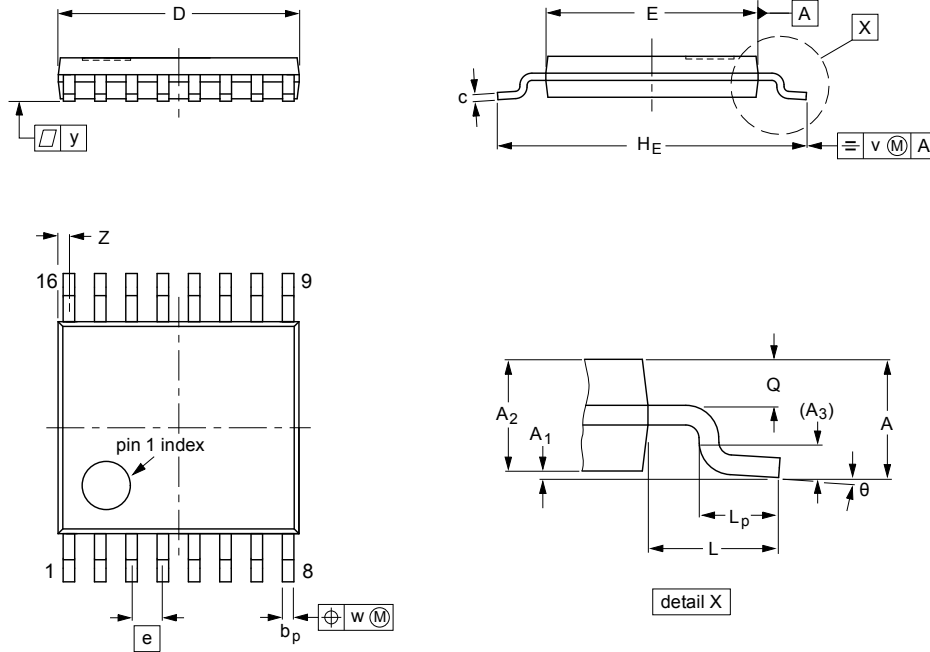


Fig. 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Fig. 15. Package outline SOT403-1 (TSSOP16)



## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4094 v.8	20181114	Product data sheet	-	74HC_HCT4094 v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Fig. 7</a> corrected.</li> </ul>			
74HC_HCT4094 v.7	20160210	Product data sheet	-	74HC_HCT4094 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4094N and 74HCT4094N (SOT38-4) removed.</li> </ul>			
74HC_HCT4094 v.6	20121231	Product data sheet	-	74HC_HCT4094 v.5
Modifications:	<ul style="list-style-type: none"> <li>General description updated.</li> </ul>			
74HC_HCT4094 v.5	20120628	Product data sheet	-	74HC_HCT4094 v.4
Modifications:	<ul style="list-style-type: none"> <li><math>V_X</math> and <math>V_Y</math> measurement points added to Table 8.</li> </ul>			
74HC_HCT4094 v.4	20111219	Product data sheet	-	74HC_HCT4094 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74HC_HCT4094 v.3	20110214	Product data sheet	-	74HC_HCT4094_CNV v.2
74HC_HCT4094_CNV v.2	19970901	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

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<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Applications</b> .....	<b>1</b>
<b>4. Ordering information</b> .....	<b>1</b>
<b>5. Functional diagram</b> .....	<b>2</b>
<b>6. Pinning information</b> .....	<b>3</b>
6.1. Pinning.....	3
6.2. Pin description.....	3
<b>7. Functional description</b> .....	<b>4</b>
<b>8. Limiting values</b> .....	<b>5</b>
<b>9. Recommended operating conditions</b> .....	<b>5</b>
<b>10. Static characteristics</b> .....	<b>6</b>
<b>11. Dynamic characteristics</b> .....	<b>8</b>
11.1. Waveforms and test circuits.....	11
<b>12. Package outline</b> .....	<b>14</b>
<b>13. Abbreviations</b> .....	<b>17</b>
<b>14. Revision history</b> .....	<b>17</b>
<b>15. Legal information</b> .....	<b>18</b>

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