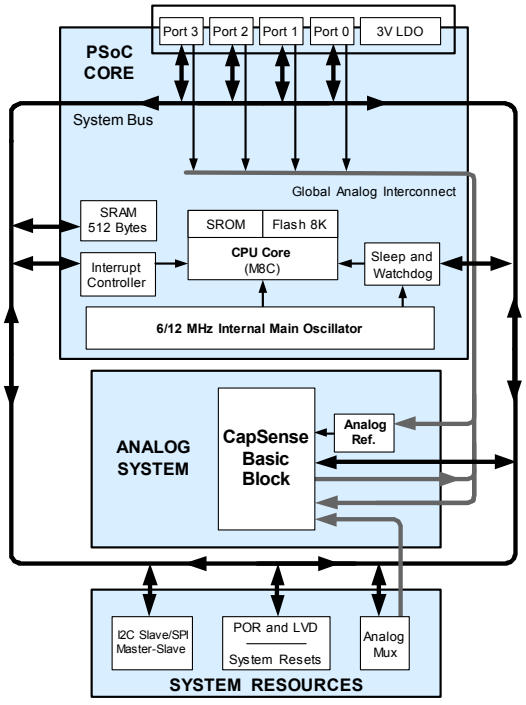
CY8C20224/CY8C20324
CY8C20424/CY8C20524

CapSense® PSoC® Programmable System-on-Chip™

Features

- Low power, configurable CapSense®
  - Configurable capacitive sensing elements
  - operating voltage
  - Operating voltage: 2.4 V to 5.25 V
  - Low operating current
    - Active 1.5 mA (at 3.0 V, 12 MHz)
    - Sleep 2.8 µA (at 3.3 V)
  - Supports up to 25 capacitive buttons
  - Supports one slider
  - Up to 10 cm proximity sensing
  - Supports up to 28 general-purpose I/O (GPIO) pins
    - Drive LEDs and other outputs
  - Configurable LED behavior (fading, strobing)
  - LED color mixing (RBG LEDs)
  - Pull-up, high Z, open-drain, and CMOS drive modes on all GPIOs
  - Internal ±5.0% 6 or12 MHz main oscillator
  - Internal low-speed oscillator at 32 kHz
  - Low external component count
    - No external crystal or oscillator components
    - No external voltage regulator required
- High-performance CapSense
  - Ultra fast scan speed —1 kHz (nominal)
  - Reliable finger detection through 5 mm thick acrylic
  - Excellent EMI and AC noise immunity
- Industry best flexibility
  - 8 KB flash program storage 50,000 erase and write cycles
  - 512-bytes SRAM data storage
  - Bootloader for ease of field reprogramming
  - Partial flash updates
  - Flexible flash protection modes
  - Interrupt controller
  - In-system serial programming (ISSP)
  - Free complete development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator and programmer
    - Full-speed emulation
    - Complex breakpoint structure
    - 128 KB trace memory
- Additional system resources
  - Configurable communication speeds
  - I^2C slave
  - SPI master and SPI slave
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit

Logic Block Diagram



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PSoC® Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip controller devices. These devices are designed to replace multiple traditional MCU based system components with one, low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture enables the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family is comprised of three main areas: core, system resources, and CapSense analog system. A common, versatile bus enables connection between I/O and the analog system. Each CY8C20x24 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a 2-MIPS, 8-bit Harvard-architecture microprocessor.

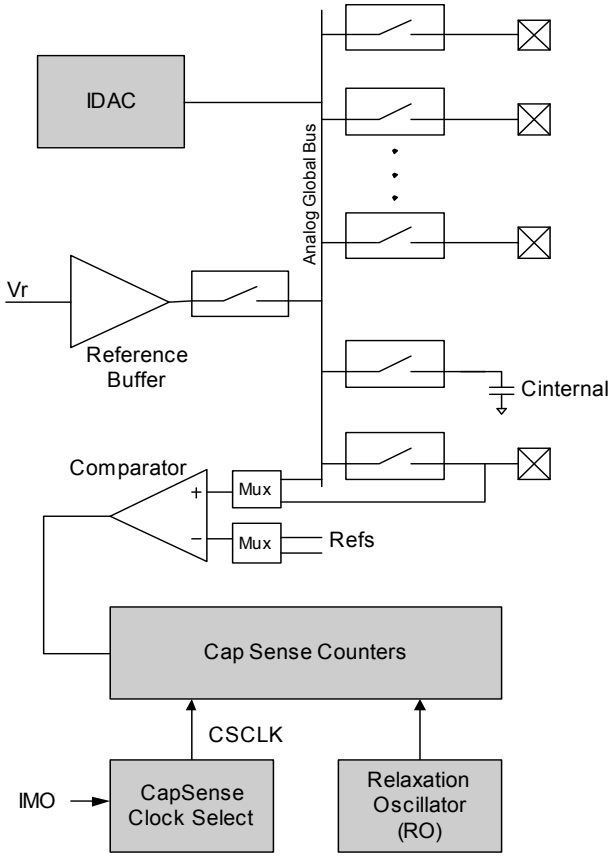
System resources provide additional capability, such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The analog system is composed of the CapSense PSoC block and an internal 1.8-V analog reference. Together, they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. The analog multiplexer system in the CY8C20x24 device family is optimized for basic CapSense functionality. It supports sensing of CapSense buttons, proximity sensors, and a single slider. Other multiplexer applications include:

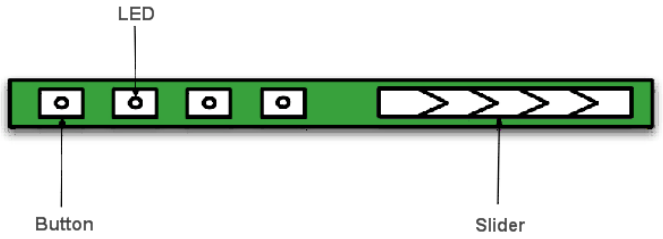
- Capacitive slider interface.
- Chip-wide mux that enables analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal to noise signal level requirements application notes, which are found in http://www.cypress.com > Design Resources > Application Notes. In general, and unless otherwise noted in the relevant application notes, the minimum signal-to-noise ratio (SNR) requirement for CapSense applications is 5:1.

Typical Application

Figure 2 illustrates a typical application: CapSense multimedia keys for a notebook computer with a slider, four buttons, and four LEDs.

Figure 2. CapSense Multimedia Button-Board Application



Additional System Resources

System resources, some of which are previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection (LVD) and power on reset (POR). Brief statements describing the merits of each system resource follow.

- The I^2C slave and SPI master-slave module provides 50, 100, or 400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- LVD interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.8-V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

Getting Started

This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, an EzI2Cs User Module configures the I^2C block in PSoC. Using these parameters, you can establish the slave address and I^2C speed. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals

Pinouts

This section describes, lists, and illustrates the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC device pins and pinout configurations.

The CY8C20x24 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 3. CY8C20224 16-pin PSoC Device

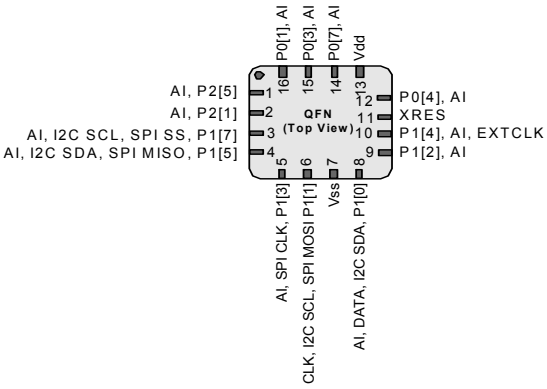


Table 1. 16-pin Part Pinout (COL)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[1], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating input
16	I/O	I	P0[1]	Integrating input

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
1. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

24-pin Part Pinout

Figure 4. CY8C20324 24-pin PSoC Device

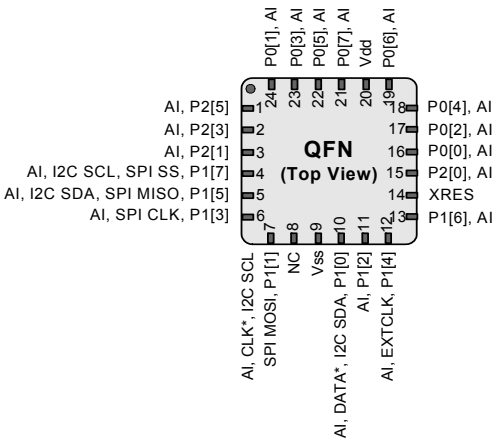


Table 2. 24-pin Part Pinout (QFN [2])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
5	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
6	I_{OH}	I	P1[3]	SPI CLK
7	I_{OH}	I	P1[1]	CLK[3], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		V_{SS}	Ground connection
10	I_{OH}	I	P1[0]	DATA[3], I^2C SDA
11	I_{OH}	I	P1[2]	
12	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
13	I_{OH}	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	
20	Power		V_{DD}	Supply voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating input
24	I/O	I	P0[1]	Integrating input
CP	Power		Vss	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes
2. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
3. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

28-pin Part Pinout

Figure 5. CY8C20524 28-pin PSoC Device

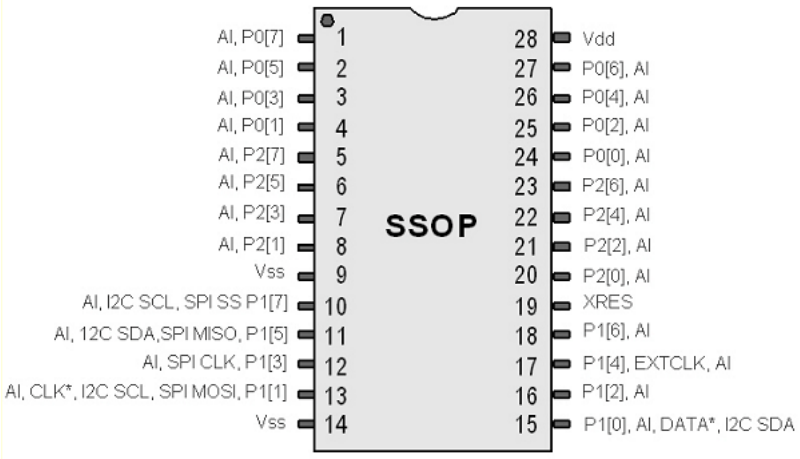


Table 3. 28-pin Part Pinout (SSOP)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	
2	I/O	I	P0[5]	
3	I/O	I	P0[3]	Integrating input
4	I/O	I	P0[1]	Integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	
8	I/O	I	P2[1]	
9	Power		V_{SS}	Ground connection
10	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
11	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
12	I_{OH}	I	P1[3]	SPI CLK
13	I_{OH}	I	P1[1]	CLK[4], I^2C SCL, SPL MOSI
14	Power		V_{SS}	Ground connection
15	I_{OH}	I	P1[0]	Data[4], I^2C SDA
16	I_{OH}	I	P1[2]	
17	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
18	I_{OH}	I	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	
28	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
4. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

32-pin Part Pinout

Figure 6. CY8C20424 32-pin PSoC Device

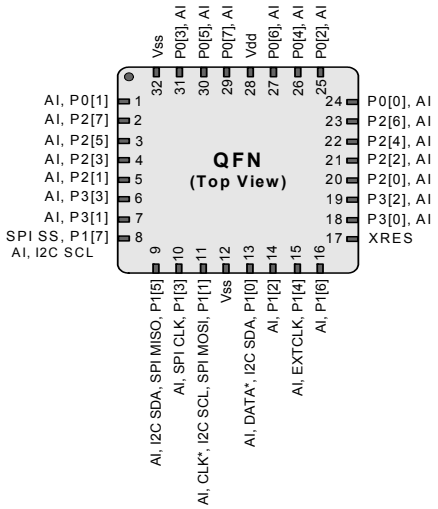


Table 4. 32-pin Part Pinout (QFN [5])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[1]	Integrating Input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground connection
13	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
5. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
6. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Table 4. 32-pin Part Pinout (QFN [5]) *(continued)*

Pin No.	Digital	Analog	Name	Description
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

48-pin OCD Part Pinout

The 48-pin QFN part table and pin diagram is for the CY8C20024 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. **It is NOT available for production**.

Figure 7. CY8C20024 OCD PSoC Device

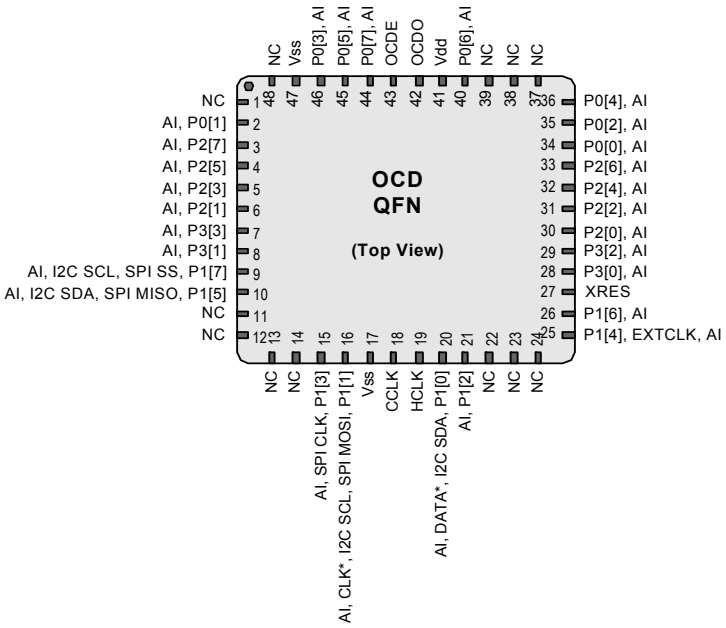


Table 5. 48-pin OCD Part Pinout (QFN [7])

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	Integrating Input
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11			NC	No connection
12			NC	No connection
13			NC	No connection
14			NC	No connection
15	I_{OH}	I	P1[3]	SPI CLK
16	I_{OH}	I	P1[1]	CLK[8], I^2C SCL, SPI MOSI
17	Power		Vss	Ground connection
18			CCLK	OCD CPU clock output
19			HCLK	OCD high speed clock output
20	I_{OH}	I	P1[0]	DATA[8], I^2C SDA

Notes

7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
8. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Table 5. 48-pin OCD Part Pinout (QFN [7]) *(continued)*

Pin No.	Digital	Analog	Name	Description
21	I_{OH}	I	P1[2]	
22			NC	No connection
23			NC	No connection
24			NC	No connection
25	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
26	I_{OH}	I	P1[6]	
27	Input		XRES	Active high external reset with internal pull-down
28	I/O	I	P3[0]	
29	I/O	I	P3[2]	
30	I/O	I	P2[0]	
31	I/O	I	P2[2]	
32	I/O	I	P2[4]	
33	I/O	I	P2[6]	
34	I/O	I	P0[0]	
35	I/O	I	P0[2]	
36	I/O	I	P0[4]	
37			NC	No connection
38			NC	No connection
39			NC	No connection
40	I/O	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			OCDO	OCD odd data output
43			OCDE	OCD even data I/O
44	I/O	I	P0[7]	
45	I/O	I	P0[5]	
46	I/O	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection
48			NC	No connection
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.

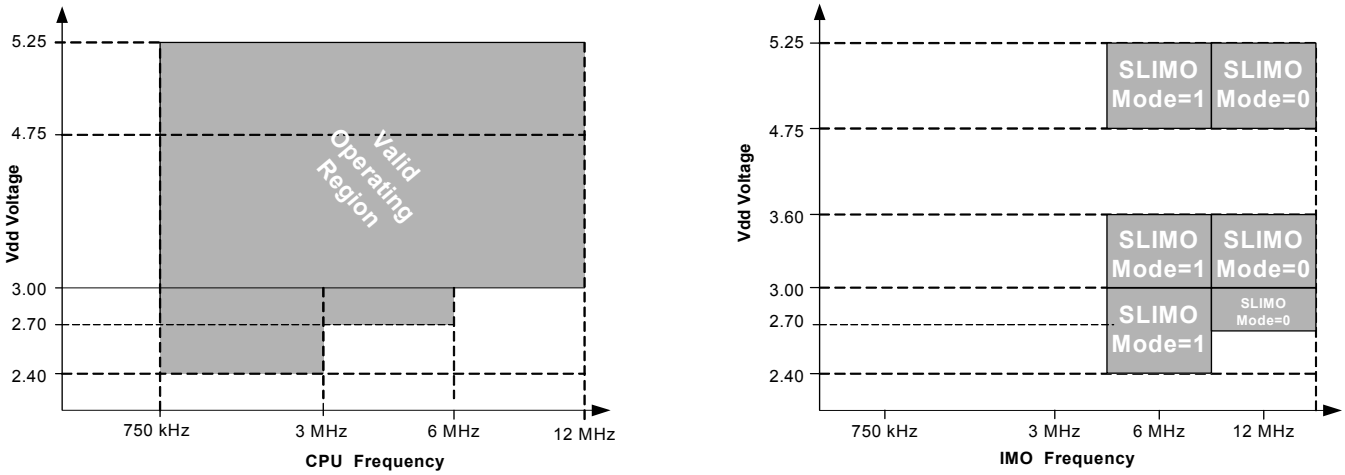
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices. For the latest electrical specifications, visit the web at http://www.cypress.com/psoc.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where noted.

Refer to Table 16 on page 19 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 8. Voltage versus CPU Frequency and IMO Frequency Trim Options



Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 31 on page 30. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 8. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz.
I_{SB27}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.

DC GPIO Specifications

Unless otherwise noted, Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 9. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 85 °C, maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ TA ≤ 85 °C, maximum of 20 mA source current in all I/Os.

Table 9. 5 V and 3.3 V DC GPIO Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 0, 2, or 3 pins	1	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OH4}	High level source current, port 1 pins with LDO regulator disabled	5	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low voltage	–	–	0.8	V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_{IH}	Input high voltage	2.0	–		V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

Table 10. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.2$	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.5$	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 1 pins with LDO regulator disabled	2	–	–	mA	$V_{OH} = V_{DD} – 0.5$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	IOL = 5 mA, maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} ≤ 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} ≤ 3.0 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA

Table 10. 2.7 V DC GPIO Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

DC Analog Mux Bus Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 11. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	Vdd ≥ 2.7 V 2.4 V ≤ Vdd ≤ 2.7 V

DC Low Power Comparator Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 12. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1.0	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC POR and LVD Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 13. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
VPPOR0	PORLEV[1:0] = 00b	–	2.36	2.40	V	
VPPOR1	PORLEV[1:0] = 01b	–	2.60	2.65	V	
VPPOR2	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
VLVD0	VM[2:0] = 000b	2.39	2.45	2.51[9]	V	
VLVD1	VM[2:0] = 001b	2.54	2.71	2.78[10]	V	
VLVD2	VM[2:0] = 010b	2.75	2.92	2.99[11]	V	
VLVD3	VM[2:0] = 011b	2.85	3.02	3.09	V	
VLVD4	VM[2:0] = 100b	2.96	3.13	3.20	V	
VLVD5	VM[2:0] = 101b	–	–	–	V	
VLVD6	VM[2:0] = 110b	–	–	–	V	
VLVD7	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
9. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
10. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
11. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 14. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[12]	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[13]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC I^2C Specifications[14]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes
12. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.
13. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
14. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[15]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[16]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
15. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
16. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

Table 17. 2.7 V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1A}	CPU frequency (2.7 V nominal)	0.75	–	3.25	MHz	2.4 V < V_{DD} < 3.0 V.
F_{CPU1B}	CPU frequency (2.7 V minimum)	0.75	–	6.3	MHz	2.7 V < V_{DD} < 3.0 V.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	–	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[17]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$		–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[18]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
17. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

AC GPIO Specifications

Table 18 an d Table 19 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

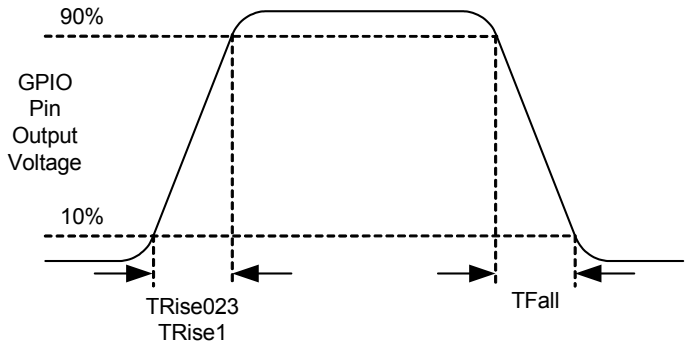
Table 18. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	6	MHz	Normal strong mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	80	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

Table 19. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	1.5	MHz	Normal Strong Mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	100	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%

Figure 9. GPIO Timing Diagram



AC Comparator Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 20. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V 2.4 V < V_{CC} < 3.0 V

AC Low Power Comparator Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 21. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC External Clock Specifications

Table 22, Table 23, and Table 24 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 22. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 23. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 24. 2.7 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{OSCEXT1A}$	Frequency with CPU clock divide by 1 (2.7 V nominal)	0.75	–	3.08	MHz	2.4 V < V_{DD} < 3.0 V. Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
$F_{OSCEXT1B}$	Frequency with CPU clock divide by 1 (2.7 V minimum)	0.75	–	6.3	MHz	2.7 V < V_{DD} < 3.0 V. Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
$F_{OSCEXT2A}$	Frequency with CPU clock divide by 2 or greater (2.7 V nominal)	1.5	–	6.35	MHz	2.4 V < V_{DD} < 3.0 V. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

Table 24. 2.7 V AC External Clock Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{OSCEXT2B}$	Frequency with CPU clock divide by 2 or greater (2.7 V minimum)	1.5	–	12.6	MHz	2.7 V < V_{DD} < 3.0 V. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	3.6 < V_{DD}
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM_HOT}$	Flash block erase + Flash block write time	–	–	100	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM_COLD}$	Flash block erase + Flash block write time	–	–	200	ms	–40 °C ≤ Tj ≤ 0 °C

AC I²C Specifications

Table 26 and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for V_{DD} ≥ 3.0 V

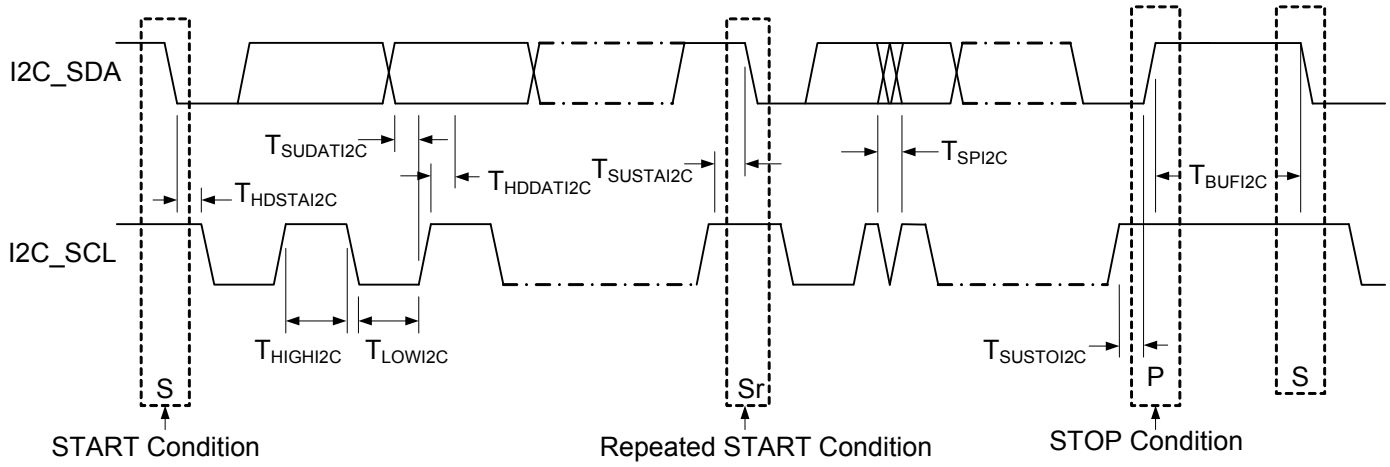
Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[19]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns	

Table 27. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not supported)

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Note
19. A Fast Mode I²C bus device is used in a Standard Mode I²C bus system but the requirement T_{SUDAT} ≥ 250 ns is met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + T_{SUDAT} = 1000 + 250 = 1250 ns (according to the Standard Mode I²C bus specification) before the SCL line is released.

Figure 10. Definition for Timing for Fast or Standard Mode on the I²C Bus



AC SPI Specifications

Table 28. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	12	MHz
DC	SCLK duty cycle		–	50	–	%
t_{SETUP}	MISO to SCLK setup time		40	–	–	ns
t_{HOLD}	SCLK to MISO hold time		40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
t_{OUT_H}	MOSI high time		40	–	–	ns

Table 29. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	4	MHz
t_{LOW}	SCLK low time		41.67	–	–	ns
t_{HIGH}	SCLK high time		41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
t_{SS_MISO}	SS high to MISO valid		–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
t_{SS_HIGH}	SS high time		–	–	50	ns
t_{SS_CLK}	Time from SS low to first SCLK		2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high		2/SCLK	–	–	ns

Ordering Information

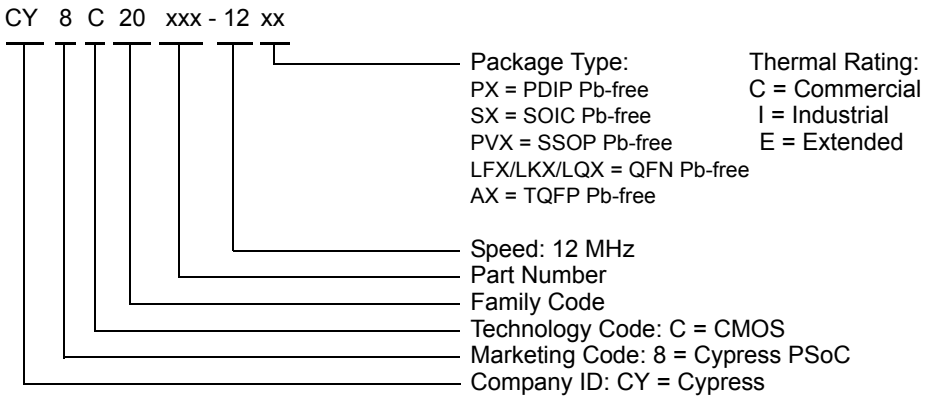
Table 30 lists the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices key package features and ordering codes.

Table 30. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Maximum Number of Buttons	Maximum Number of Sliders	Maximum Number of LEDs	Configurable LED Behavior (Fade, Strobe)	Proximity Sensing
16-pin (3 × 3 mm 0.60 Max) COL	CY8C20224-12LKXI	8 K	512	10	1	13	Yes	Yes
16-pin (3 × 3 mm 0.60 Max) COL (Tape and Reel)	CY8C20224-12LKXIT	8 K	512	10	1	13	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN	CY8C20324-12LQXI	8 K	512	17	1	20	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN (Tape and Reel)	CY8C20324-12LQXIT	8 K	512	17	1	20	Yes	Yes
28-pin (210-Mil) SSOP	CY8C20524-12PVXI	8 K	512	21	1	24	Yes	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C20524-12PVXIT	8 K	512	21	1	24	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXI	8 K	512	25	1	28	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXIT	8 K	512	25	1	28	Yes	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

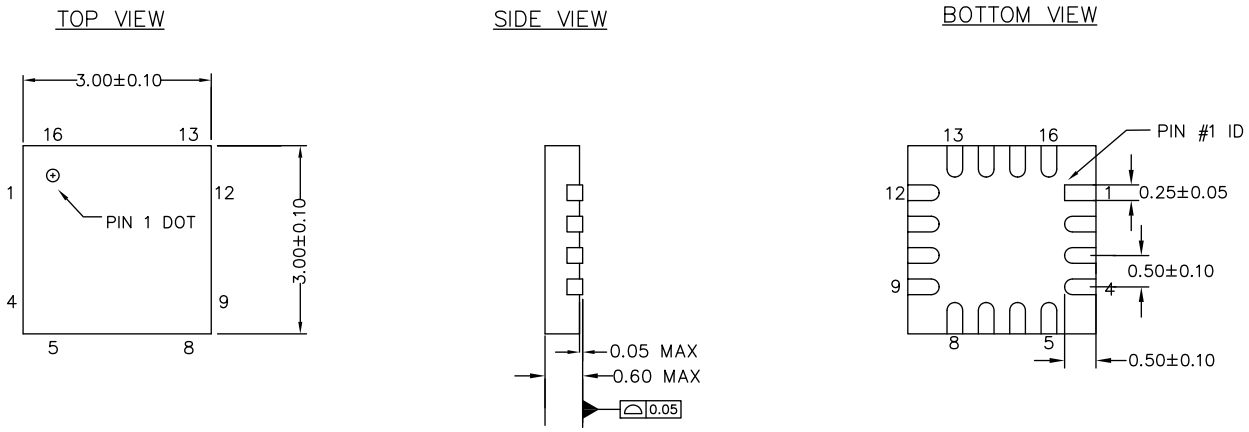


Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

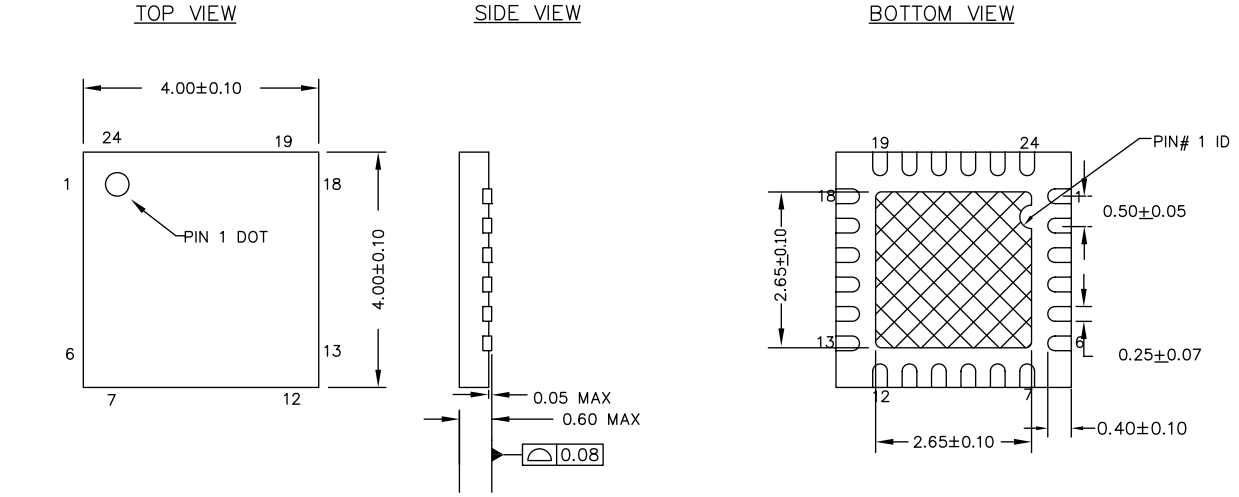
Figure 11. 16-pin Chip On-Lead (3 × 3 × 0.6 mm) (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 12. 24-pin QFN (4 × 4 × 0.55 mm) 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937

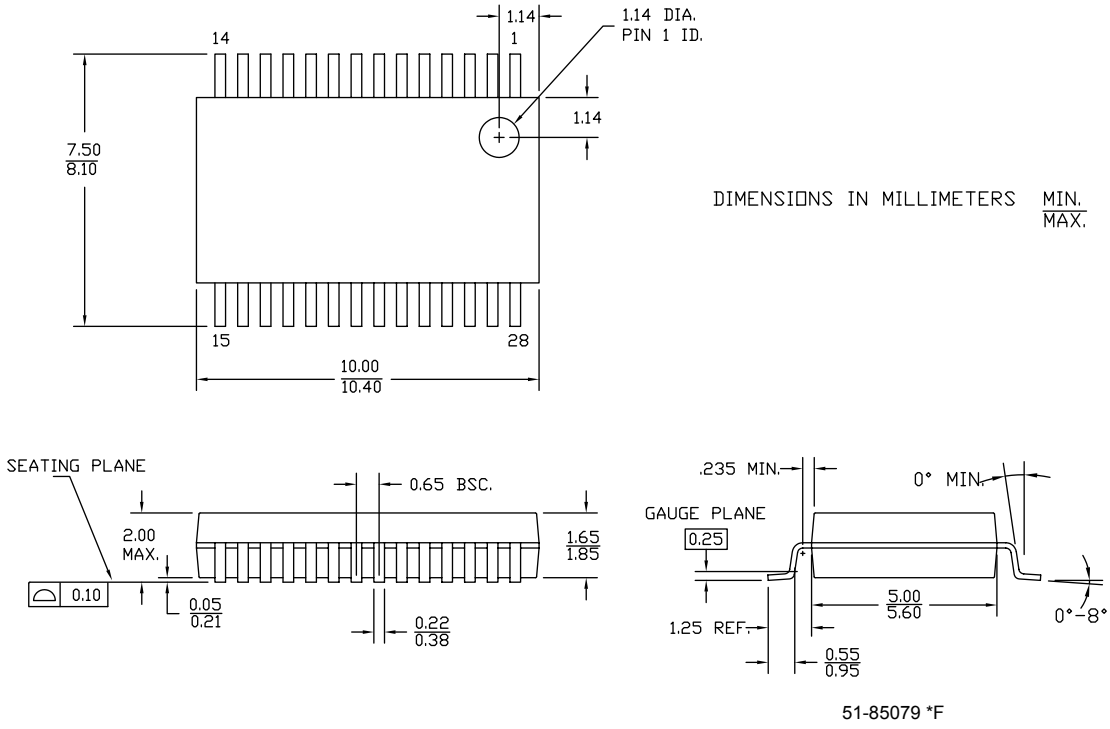


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

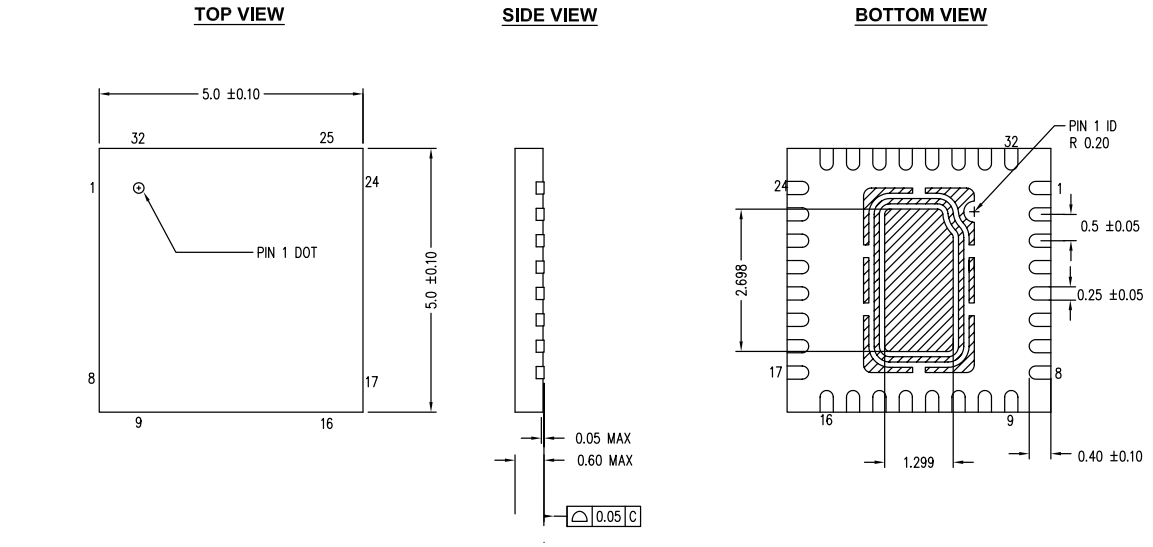
001-13937 *F

Figure 13. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

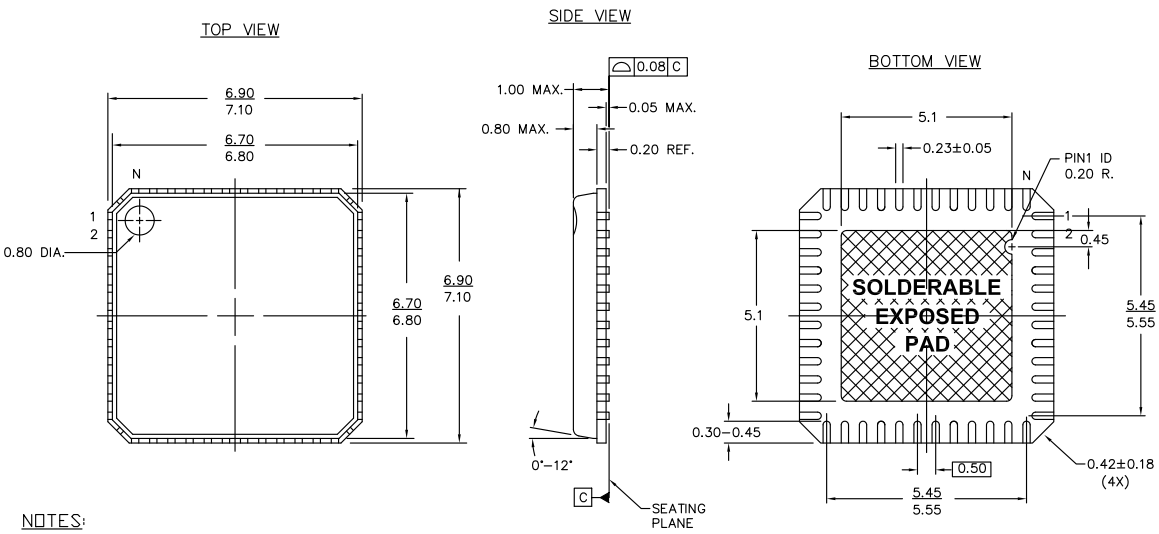
Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 15. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Subcon Punch Type Package) Package Outline, 001-12919



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *D

Important For information on the preferred dimensions for mounting the QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 31. Thermal Impedances Per Package

Package	Typical θ_{JA} [20]
16-pin COL	46 °C/W
24-pin QFN[21]	25 °C/W
28-pin SSOP	96 °C/W
32-pin QFN[21]	27 °C/W
48-pin QFN[21]	28 °C/W

Solder Reflow Specifications

Table 32 lists the minimum solder reflow peak temperature to achieve good solderability.

Table 32. Solder Reflow Specifications

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
16-pin COL	260 °C	30 s
24-pin QFN	260 °C	30 s
28-pin SSOP	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes
20. $T_J = T_A$ + Power x θ_{JA}.
21. To achieve the thermal impedance specified for the QFN package, the center thermal pad is soldered to the PCB ground plane.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- Two CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 33. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [22]	Foot Kit [23]	Prototyping Module	Adapter [24]
CY8C20224-12LKXI	16-pin COL	Not available	Not available	CY3210-20X34	–
CY8C20324-12LQXI	24-pin QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-20X34	AS-24-28-01ML-6
CY8C20524-12PVXI	28-pin SSOP	CY3250-20534	CY3250-28SSOP-FK	CY3210-20X34	–

Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details of each of these tools are found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on emulating the circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer application note AN2323 “Build a PSoC Emulator into Your Board”.

Notes
22. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
23. Foot kit includes surface mount feet that is soldered to the target PCB.
24. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is found at http://www.emulation.com.

Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PGA	programmable gain amplifier
CPU	central processing unit	POR	power on reset
EEPROM	electrically erasable programmable read-only memory	PPOR	precision power on reset
GPIO	general purpose I/O	PSoC®	Programmable System-on-Chip
ICE	in-circuit emulator	PWM	pulse width modulator
IDAC	current DAC	QFN	quad flat no leads
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPI™	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO		WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LVD	low voltage detect	XRES	external reset
MCU	microcontroller unit		

Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 35 lists the units of measures.

Table 35. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	millisecond
pF	picofarad	ns	nanosecond
kHz	kilohertz	ps	picosecond
MHz	megahertz	µV	microvolts
kΩ	kilohm	mV	millivolts
Ω	ohm	V	volts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary *(continued)*

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

Glossary *(continued)*

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Glossary *(continued)*

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C20224/CY8C20324/CY8C20424/CY8C20524, CapSense® PSoC® Programmable System-on-Chip™ Document Number: 001-41947				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1734104	YHW / AESA	See ECN	New parts and document (Revision **).
*A	2542938	RLRM / AESA	07/28/2008	Corrected Ordering Information format. Updated package diagram 001-13937 to Rev *B. Updated to new template.
*B	2610469	SNV / PYRS	11/20/08	Updated V_{OH5}, V_{OH7}, and V_{OH9} specifications.
*C	2634376	DRSW	01/12/09	Changed status from Preliminary to Final. Removed the part number CY3250-20234QFN from the 'CY8C20224-12LKXI' flex-pod kit Changed title from CapSense™ Multimedia PSoC® Mixed-Signal Array to CapSense™ Multimedia PSoC® Programmable System-on-Chip™ Added -12 to the CY8C20524 parts in the Ordering Information table Updated 'Development Tools' and 'Designing with PSoC Designer' sections on pages 4 and 5 Updated 'Development Tools Selection' section on page 30 Changed 16-Pin from QFN to COL
*D	2693024	DPT / PYRS	04/16/2009	Added devices CY8C20424-12LQXI and CY8C20424-12LQXIT in the Ordering Information table Added 32-Pin Sawn QFN package diagram
*E	2717566	DRSW / AESA	06/11/2009	Updated AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 (page 19), TWRITE specifications (page 22) Added IOH & IOL (page 16), Flash endurance note (page 18), DCILO (page 19), F32K_U (page 19), TPOWERUP (page 19), TERASEALL (page 22), TPROGRAM_HOT (page 22), and TPROGRAM_COLD (page 22) specifications Added AC SPI Master and Slave Specifications
*F	2899195	CFW / ISW	03/26/2010	Updated Ordering Information. Updated Package Diagrams.
*G	3037121	CFW	09/24/2010	Updated title to read AC Comparator Specifications and also updated table caption to read "AC Comparator Specifications" in the same section. Minor edits. Updated to new template.
*H	3049675	BTK	10/06/2010	Removed AC analog mux bus specifications. Updated Development Tools and Designing with PSoC Designer sections.
*I	3072668	NJF	10/27/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changed were made to I^2C Timing Diagram. Updated for clearer understanding. Updated to new template.
*J	3112469	ARVM	12/16/10	Updated Ordering Information: Updated part numbers.
*K	3182773	MATT	03/01/11	No technical updates. Completing Sunset Review.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	3638597	BVI	06/06/2012	Updated Getting Started: Updated description. Updated Application Notes: Updated description. Updated Development Kits: Updated description. Updated Training: Updated description. Updated CYPros Consultants: Updated description. Updated Solutions Library: Updated description. Updated Technical Support: Updated description. Updated AC SPI Specifications: Updated Table 28: Renamed "t_{OUT_HIGH}" as "t_{OUT_H}" in "Symbol" column. Updated Table 29: Removed t_{SCLK} parameter and its details. Added F_{SCLK} parameter and its details. Updated Packaging Dimensions: spec 001-09116 – Changed revision from *E to *F. spec 001-13937 – Changed revision from *C to *D. spec 51-85079 – Changed revision from *D to *E. spec 001-12919 – Changed revision from *B to *C. Updated Solder Reflow Specifications: Updated Table 32: Replaced "Time at Maximum Temperature" with "Time at Maximum Peak Temperature" in column heading and updated details in that column. Updated Development Tool Selection: Updated Software: Updated PSoC Designer: Updated description. Updated PSoC Designer: Updated description. Updated Reference Documents: Removed spec 001-17397 and spec 001-14503 from the list as these specs are obsolete.
*M	4311264	VAIR	03/19/2014	Updated Designing with PSoC Designer: Updated Configure User Modules: Updated description (Replaced references of PWM User Module with EzI2Cs User Module). Updated Packaging Dimensions: spec 001-09116 – Changed revision from *F to *J. spec 001-13937 – Changed revision from *D to *E. spec 001-48913 – Changed revision from *B to *D. spec 001-12919 – Changed revision from *C to *D.
*N	5625819	DCHE	02/09/2017	Updated Packaging Dimensions: spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*O	5988009	AESATMP9	12/08/2017	Updated logo and copyright.

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