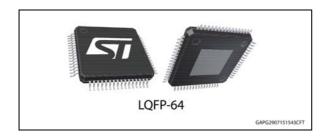


## Automotive door actuator driver with embedded LIN

#### Datasheet - production data



#### **Features**

- AEC-Q100 qualified
- 1 half bridge for 7.5 A load (R<sub>ON</sub> = 100 mΩ)
- 1 half bridge for 7.5 A load (R<sub>ON</sub> = 150 mΩ)
- 2 half bridges for 3 A load (R<sub>ON</sub> = 300 mΩ)
- 1 configurable high-side driver for up to 1.5 A (R<sub>ON</sub> = 500 mΩ) or 0.35 A (R<sub>ON</sub> = 1600 mΩ) load
- 1 configurable high-side driver for 0.8 A (R<sub>ON</sub> = 800 mΩ) or 0.35 A (R<sub>ON</sub> = 1600 mΩ) load
- 3 configurable high-side drivers for 0.15 A/0.35 A (R<sub>ON</sub> =2 Ω)
- 1 configurable high-side driver for 0.25 A/0.5 A (R<sub>ON</sub> = 2 Ω)
- 4 configurable high-side drivers for 0.15 A/0.25 A (R<sub>ON</sub> = 5 Ω)
- Internal 10bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (OUT15 & OUT\_HS / both P-channel) to supply e.g. external contacts
- Programmable soft-start function to drive loads with higher inrush currents as current limitation value (for OUT1-6, OUT7, OUT8 and OUT\_HS) with thermal expiration feature
- All the embedded outputs come with protection and supervision features:
  - Current Monitor (high-side only)
  - Open-load

- Overcurrent
- Thermal warning
- Thermal shutdown
- Fully protected driver for external MOSFETs in H-bridge configuration
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- Separated (Isolated) fail-safe block with 2 LS (R<sub>ON</sub> = 1 Ω) to pull down the gates of the external HS MOSFETs
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- Embedded and programmable VS duty cycle adjustment for LED driver outputs

# **Applications**

Door zone applications.

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Description L99DZ120

# 1 Description

The L99DZ120 is a door zone systems IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN physical communication layers.

The two low-drop voltage regulators of the devices supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability. In addition 8 high-side drivers to supply LEDs, 2 high-side drivers to supply bulbs increase the system integration level.

Up to 3 DC motors and 4 external MOS transistors in H-bridge configuration can be driven. All outputs are SC protected and implement an open-load diagnosis.

The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.



# 2 Block diagram and pin descriptions

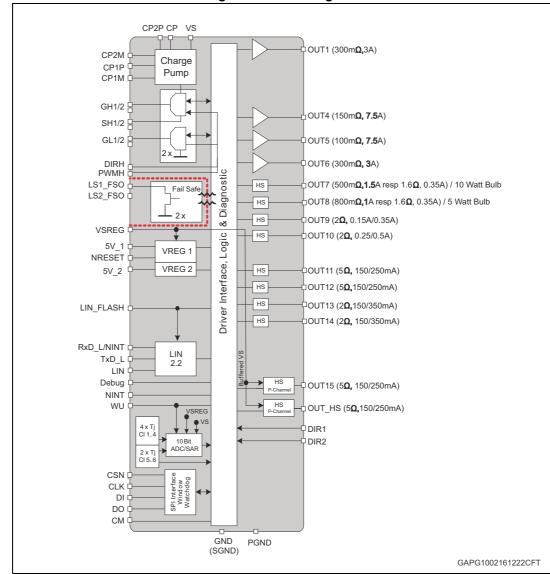


Figure 1. Block diagram

Table 1. Pin definitions and functions

Pin	Symbol	Function
1	WU	Wake-up Input: Input pin for static or cyclic monitoring of external contacts
2	CP2M	Charge pump pin for capacitor 2, negative side
3	CP2P	Charge pump pin for capacitor 2, positive side
4	СР	Charge pump output
5	CP1P	Charge pump pin for capacitor 1, positive side
6	CP1M	Charge pump pin for capacitor 1, negative side



Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
7	NC	Not connected
8	NC	Not connected
9	OUT14	High-side-driver output to drive LEDs
10	OUT13	High-side-driver output to drive LEDs
11	OUT12	High-side-driver output to drive LEDs
12	OUT9	High-side-driver output to drive LEDs
13	OUT10	High-side-driver-output
14	OUT11	High-side-driver output to drive LEDs
15	LS1_FSO	Fail Safe low-side switch (Active low)
16	LS2_FSO	Fail Safe low-side switch (Active low)
17	VS	Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving, the full current at the outputs all pins of VS must be connected externally!
18	VS; 2nd pin	Current capability (pin description see above)
19	OUT7	High-side-driver output to drive LEDs or a 10 Watt bulb (programmable R <sub>dson</sub> )
20	OUT6	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
21	OUT1	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
22	NC	Not connected
23	OUT5	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to $V_{\rm S}$ , low-side driver from GND to output)
24	OUT5; 2nd pin	Current capability (pin description see above)
25	$V_{SREG}$	Power supply voltage to supply the internal voltage regulators, OUT15 and the OUT_HS (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.
26	OUT_HS	High-side-driver output to drive LEDs or to supply contacts



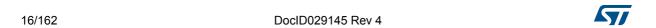
Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
27	OUT4	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V <sub>S</sub> , low-side driver from GND to output)
28	OUT4; 2 <sup>nd</sup> pin	Current capability (pin description see above)
29	NC	Not connected
30	VS; 3rd pin	Current capability (for the pin description see above)
31	OUT15	High-side-driver output to drive LEDs
32	PGND	Power GND
33	OUT8	High-side-driver output to drive LEDs or a 5 Watt bulb (programmable $R_{dson}$ )
34	NC	Not connected
35	SGND	Signal Ground
36	СМ	Current monitor output: depending on the selected multiplexer bits $CM\_SEL\_x$ ( $CR$ 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio
37	NC	Not connected
38	CLK	SPI: serial clock input
39	DO	SPI: serial data output (push pull output stage)
40	DI	SPI: serial data input
41	CSN	SPI: chip select not input
42	TxD_L	LIN Transmit data input
43	RxD_L/NINT	RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)
44	LIN_FLASH	LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)
45	NC	Not connected
46	DIR1	Direct Drive Input 1
47	PWMH	PWMH input: this input signal can be used to control the H-bridge Gate Drivers.
48	DIRH	Direction Input: this input controls the H-bridge Drivers for the external MOSFETs
49	DIR2	Direct Drive Input 2
50	NRESET	NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to 5V_1)
51	5V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller
52	NC	Not connected



Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
53	NINT	Interrupt output (low active; push-pull output stage) to indicate V <sub>SREG</sub> early warning (Active mode); indicates wake-up events from V1_standby mode
54	NC	Not connected
55	NC	Not connected
56	Debug	Debug input to deactivate the window watchdog (high active)
57	LIN	LIN bus line
58	5V_2	Voltage regulator 2 output: 5 V supply for external loads (potentiometer, sensors). V2 is protected against reverse supply
59	GL1	Gate driver for PowerMOS low-side switch in half-bridge 1
60	SH1	Source of high-side switch in half-bridge 1
61	GH1	Gate driver for PowerMOS high-side switch in half-bridge 1
62	GH2	Gate driver for PowerMOS high-side switch in half-bridge 2
63	SH2	Source of high-side switch in half-bridge 2
64	GL2	Gate driver for PowerMOS low-side switch in half-bridge 2



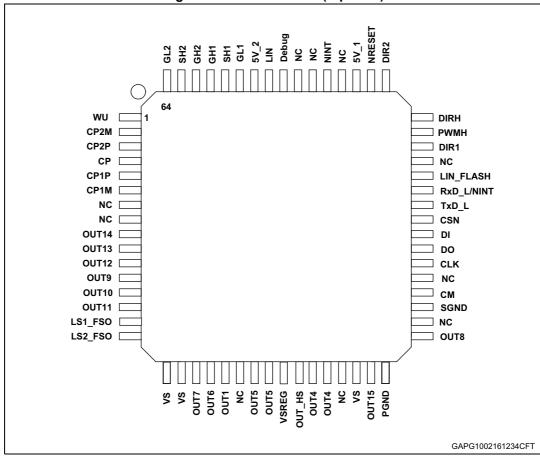


Figure 2. Pin connection (top view)



# 3 Electrical specifications

# 3.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter / test condition	Value [DC voltage]	Unit
\/ \/	DC supply voltage / "jump start"	-0.3 to +28	V
V <sub>S,</sub> V <sub>SREG</sub>	Load dump	-0.3 to +40	V
5V_1	Stabilized supply voltage, logic supply	-0.3 to 6.5 V1 < V <sub>SREG</sub>	V
5V_2 <sup>(1)</sup>	Stabilized supply voltage	-0.3 to +28 <sup>(2)</sup>	V
V <sub>DI</sub> , V <sub>CLK</sub> V <sub>CSN</sub> V <sub>DO</sub> , V <sub>RXDL/NINT</sub> , V <sub>NRESET</sub> , V <sub>CM</sub> , V <sub>DIR</sub> , V <sub>DIR2</sub> , V <sub>PWMH</sub> , V <sub>DIRH</sub> , V <sub>INT</sub>	Logic input / output voltage range	-0.3 to V1+0.3	٧
V <sub>LIN_FLASH</sub> , V <sub>TXDL</sub>	Multi Level Inputs	-0.3 to 40	V
V <sub>Debug</sub>	Debug input pin voltage range	-0.3 to 40	٧
V <sub>LS1_FSO</sub> , V <sub>LS2_FSO</sub>	Output voltage range of Fail-Safe low-side Switches	-0.3 to 35	V
V	DC Wake up input voltage / "jump start"	-0.3 to +28	٧
V <sub>WU</sub>	Load dump	-0.3 to +40	V
V <sub>LIN</sub>	LIN bus I/O voltage range	-20 to +40	٧
I <sub>Input</sub> <sup>(3)</sup>	Current injection into V <sub>S</sub> related input pins	20	mA
I <sub>OUT_INJ</sub> (3)	Current injection into V <sub>S</sub> related outputs	20	mA
V <sub>OUTn</sub> , V <sub>out_HS</sub>	Output voltage (n = 1 to 15)	-0.3 to V <sub>S</sub> +0.3	V
V <sub>GH1</sub> , V <sub>GH2</sub> (V <sub>Gxy</sub> )	High Voltage Signal Pins	$V_{Sxy}$ -0.3 to $V_{Sxy}$ +13; $V_{CP}$ +0.3	<b>V</b>
V <sub>GL1,</sub> V <sub>GL2</sub> , (V <sub>Gxy</sub> )	High Voltage Signal Pins	V <sub>Sxy</sub> -0.3 to V <sub>Sxy</sub> +13; V <sub>CP</sub> -0.3V to +12V; Vcp+0.3V	٧
	High Voltage Signal Pins	-1 to 40	V
$V_{SH1}, V_{SH2} (V_{Sxy})$	High Voltage Signal Pins; single pulse with t <sub>max</sub> = 200ns	-5 to 40	V
V <sub>CP1P</sub>	High Voltage Signal Pins	V <sub>S</sub> -0.3 to V <sub>S</sub> +14	V
V <sub>CP2P</sub>	High Voltage Signal Pins	V <sub>S</sub> -0.6 to V <sub>S</sub> +14	V

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Table 2. Absolute maximum ratings (continued)

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V <sub>CP1M</sub> , V <sub>CP2M</sub>	High Voltage Signal Pins	-0.3 to V <sub>S</sub> +0.3	V
V	High Voltage Signal Pin V <sub>S</sub> ≤ 26 V	V <sub>S</sub> -0.3 to V <sub>S</sub> +14	V
V <sub>CP</sub>	High Voltage Signal Pin V <sub>S</sub> > 26 V	V <sub>S</sub> -0.3 to +40	V
lout9, lout10, lout11, lout12, lout13, lout14, lout15, lout_нs		±1.25	A
I <sub>OUT8</sub>	Output current <sup>(2)</sup>	±2.5	Α
I <sub>OUT7</sub>		±5	Α
I <sub>OUT1,6</sub>		±5	Α
I <sub>OUT4,5</sub>		±10	Α
	Maximum cumulated current at V <sub>S</sub> drawn by OUT1 <sup>(2)</sup>	±7.5	Α
	Maximum cumulated current at V <sub>S</sub> drawn by OUT8 & OUT10 <sup>(2)</sup>	±2.5	Α
	Maximum cumulated current at V <sub>S</sub> drawn by OUT4 <sup>(2)</sup>	±10	Α
I <sub>VScum</sub>	Maximum cumulated current at V <sub>S</sub> drawn by OUT5 <sup>(2)</sup>	±10	Α
	Maximum cumulated current at V <sub>S</sub> drawn by OUT6 & OUT7 <sup>(2)</sup>	±7.5	Α
I <sub>VScum</sub>	Maximum cumulated current at V <sub>S</sub> drawn by OUT9, OUT11, OUT12, OUT13, OUT14, OUT15 and CP	±2.5	А
I <sub>VSREG</sub>	Maximum current at V <sub>SREG</sub> pin <sup>(2)</sup> (5V_1. 5V_2 and OUT_HS)	±2.5	Α
	Maximum cumulated current at PGND drawn by OUT1 & OUT6 <sup>(2)</sup>	±7.5	Α
I <sub>PGNDcum</sub>	Maximum cumulated current at PGND drawn by OUT5 <sup>(2)</sup>	±12.5	Α
	Maximum cumulated current at PGND drawn by OUT4 <sup>(2)</sup>	±12.5	Α
I <sub>SGND</sub>	Maximum current at SGND <sup>(2)</sup>	±1.25	Α
GND pins	PGND versus SGND	-0.3 to 0.3	V

<sup>1.</sup>  $5V_2$  is robust against SC to 28 V only in case  $V_{\mbox{SREG}}$  is supplied.

Note:

All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!



<sup>2.</sup> Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.

<sup>3.</sup> Guaranteed by design.

Note:

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

# 3.2 ESD protection

Table 3. ESD protection

Parameter	Value	Unit
All pins <sup>(1)</sup>	+/-2	kV
All power output pins <sup>(2)</sup> : OUT1 – OUT15, OUT_HS	+/-4	kV
LIN	+/-8 <sup>(2)</sup> +/-10 <sup>(3)</sup> +/-6 <sup>(4)</sup>	kV
All pins <sup>(5)</sup>	+/-500	V
Corner pins <sup>(5)</sup>	+/-750 <sup>(6)</sup>	V
All pins <sup>(7)</sup>	+/- 200	V

- 1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
- 2. HBM with all none zapped pins grounded.
- 3. Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
- Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
- 5. Charged device model.
- $6. \quad \text{For WU, these limits are referred to one-zap stress; in case of three-zap stress, the limits are +750 V/-400 V.}\\$
- 7. Machine model; C = 220 pF, R = 0  $\Omega$ .

### 3.3 Thermal data

Table 4. Operating junction temperature

Symbol	Parameter	Value	Unit
T <sub>j</sub>	Operating junction temperature	-40 to 175	°C

All parameters are guaranteed in the junction temperature range -40 to 150°C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175°C).

Note: Parameters limits at higher junction temperatures than 150°C may change respect to what is specified as per the standard temperature range.

Note: Device functionality at high junction temperature is guaranteed by characterization.

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Symbol	Parameter		Min.	Тур.	Max.	Unit
$T_W$	Thermal overtemperature warning threshold	$T_j^{(1)}$	140	150	160	°C
T <sub>SD1</sub>	Thermal shutdown junction temperature 1	T <sub>j</sub> <sup>(1)</sup> Cluster 1-4 Cluster 5-6	165 165	175 175	185 190	°C
T <sub>SD2</sub>	Thermal shutdown junction temperature 2	T <sub>j</sub> <sup>(1)</sup>	175	185	195	°C
T <sub>SD12hys</sub>	memai shataown janetion temperature 2	Hysteresis		5		°C
T <sub>jtft</sub>	Thermal warning / shutdown filter time			32		μs

Table 5. Temperature warning and thermal shutdown

#### 3.3.1 LQFP64 thermal data

Devices belonging to L99DZxxx family embed a multitude of junctions (i.e. Outputs based on a PowerMOSFET stage) housed in a relatively small piece of silicon. The most complex device contains, among all the described features, 6 half-bridges (12 N-Channel PowerMOS), 10 high-sides and two voltage regulators; all the other derivatives, even if smaller than the family super set device, still contain a significant number of junctions.

For this reason, using the Thermal Impedance of a single junction (i.e. voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics.

Thermal information is provided as temperature reading by different clusters placed close to the most dissipative junctions.

Some representative and realistic worst-case thermal profiles are described in the below paragraph.

Following measurement methods can be easily implemented, by final user, for a specific activation profile.

#### L99DZ120 thermal profiles

#### **Profile 1**

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation)
- OUT14: 300 Ω resistor (DC activation)



<sup>1.</sup> Non-overlapping.

#### Cyclic activation

- OUT4 OUT5: 3,3  $\Omega$  resistor placed across those outputs
  - 10 activations of Lock/Un-lock (250 ms ON Lock; 500 ms wait; 250 ms ON Un-lock unlock; 500 ms wait)
- OUT5 OUT6: 10 Ω resistor placed across those outputs
  - (250 ms ON Safe Lock; 500 ms wait; 250 ms ON Safe unlock; 500 ms wait)

#### Test execution:

Once thermal equilibrium is reached with all DC load active, the "Cyclic Activation" sequence is applied.

Temperature reading is logged just at the end of the whole sequence.

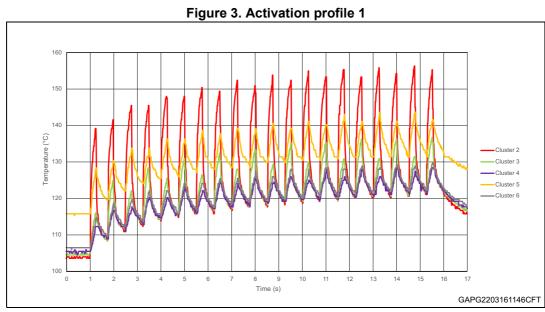


Figure 4. Activation profile 1 (first cycle)

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Note:

All curves are plotted interpolating measured samples with 15 ms of period.

#### **Profile 2**

Battery Voltage: 16V, Ambient temperature start: 85°C

#### DC activation

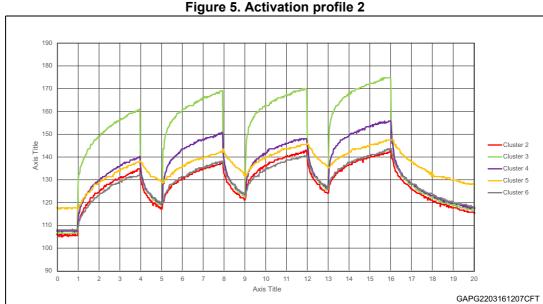
- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300  $\Omega$  resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation
- OUT14: 300  $\Omega$  resistor (DC activation)

#### Cyclic activation

- OUT1 OUT6: 6,8 Ω resistor placed across those outputs
  - 2 activations (3s ON; 1s OFF; 2x)

#### Test execution:

Once thermal equilibrium is reached with all DC load active, the "Cyclic Activation" sequence is applied.



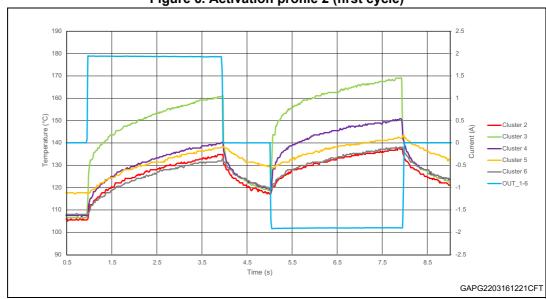


Figure 6. Activation profile 2 (first cycle)

All curves are plotted interpolating measured samples with 15 ms of period. Note:

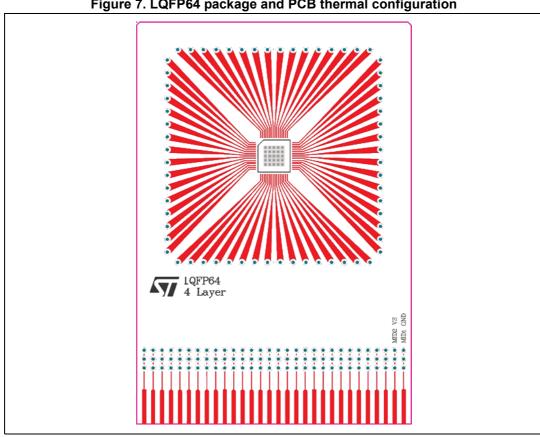


Figure 7. LQFP64 package and PCB thermal configuration

Note:

Layout condition for Thermal Characterization (board finishing thickness 1.5 mm +/- 10%, board four layers, board dimension 77 mm x 114 mm, board material FR4, Cu thickness 0,070 mm for outer layers, 0.0035 mm for inner layers, thermal vias separation 1.2 mm).

### 3.4 Electrical characteristics

## 3.4.1 Supply and supply monitoring

All SPI communication, logic and oscillator parameters are working down to  $V_{SREG} = 3.5 \text{ V}$  and parameters are as specified in the following chapters (guaranteed by design).

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for V<sub>SREG</sub>< V<sub>POR</sub>)
- Reset threshold correctly detected

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 6. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
$V_{SUV}$	V <sub>S</sub> undervoltage threshold	V <sub>S</sub> increasing / decreasing	4.7		5.4	V
V <sub>hyst_UV</sub>	V <sub>S</sub> undervoltage hysteresis		0.04	0.1	0.2	V
V	V <sub>S</sub> overvoltage threshold	V <sub>S</sub> increasing	20		22.5	V
$V_{SOV}$	v <sub>S</sub> overvoltage tilleshold	V <sub>S</sub> decreasing	18.5		5.4 0.2 22.5 22.5 1.5 4.9 0.2 22.5 22.5 1.5 14 30	V
V <sub>hyst_OV</sub>	V <sub>S</sub> overvoltage hysteresis		0.5	1	1.5	V
V <sub>SREG_UV</sub>	V <sub>SREG</sub> undervoltage threshold	V <sub>SREG</sub> increasing / decreasing	4.2		4.9	V
V <sub>hyst_UV</sub>	V <sub>SREG</sub> undervoltage hysteresis		0.04	0.1	0.2	V
M	V averyaltage threehold	V <sub>SREG</sub> increasing	20		22.5	V
V <sub>SREG_OV</sub>	V <sub>SREG</sub> overvoltage threshold	V <sub>SREG</sub> decreasing	18.5	4 0.1 0.2 0 22.5 5 22.5 5 1 1.5 64	V	
V <sub>hyst_OV</sub>	V <sub>SREG</sub> overvoltage hysteresis		0.5	1	1.5	V
t <sub>ovuv_filt</sub>	V <sub>S</sub> /V <sub>SREG</sub> over/undervoltage filter time			64		μs
I <sub>V(act)</sub>	Current consumption in Active mode	$V_S = V_{SREG} = 12 \text{ V};$ TXD LIN = high; V1 = ON; V2 = ON; HS/LS Driver OFF; CP = ON		11	14	mA
I <sub>V(BAT)</sub>	Current consumption in V <sub>bat</sub> _standby mode <sup>(1)</sup>	V <sub>S</sub> = 12 V; Both voltage regulators deactivated; HS/LS Driver OFF	8	16	30	μΑ
I <sub>V(BAT)</sub> CS	Current consumption in V <sub>bat</sub> _standby mode with cyclic sense enabled <sup>(1)</sup>	$V_S$ = 12 V; Both voltage regulators deactivated; T = 50 ms, $t_{ON}$ = 100 µs	30	80	130	μА
I <sub>V(BAT)CW</sub>	Current consumption in V <sub>bat</sub> _standby mode with cyclic wake enabled <sup>(1)</sup>	V <sub>S</sub> = 12 V; Both voltage regulators deactivated during standby phase	30	80	130	μA

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
	Current consumption in V <sub>1</sub> _standby mode <sup>(1)</sup>	$V_S$ = 12 V; Voltage regulator V1 active; (I <sub>V1</sub> = 0); HS/LS Driver OFF	16	50	70	μΑ
I <sub>V(V1stby)</sub>	Current consumption in V <sub>1</sub> _standby mode <sup>(1)</sup> <sup>(2)</sup>	$V_S$ = 12 V; Voltage regulator V1 active; (I <sub>V1</sub> = I <sub>CMP</sub> ); HS/LS Driver OFF			196	μΑ
	Current consumption in V <sub>1</sub> _standby mode <sup>(1)</sup>	$V_S$ = 12V; Voltage regulator V1 active; (I <sub>V1</sub> = I <sub>PEAK</sub> ); HS/LS Driver OFF			436	μΑ
I <sub>qLIN</sub>	Quiescent current adder for LIN wake up activated	Guaranteed by design		0		μΑ
I <sub>OUT_HS</sub>	Additional bias quiescent current for switched on OUT_HS or OUT15 by DIR or Timer; value for 1 output	Guaranteed by design		620	1100	μΑ
I <sub>OUTHS_DIR</sub>	Quiescent current adder if OUT_HS and/or OUT15 are configured for Direct Drive; value during output off	Guaranteed by design		0	5	μΑ
I <sub>timer</sub>	Quiescent current adder if timer1 and/or timer 2 are active to provide interrupt on NINT upon timer expiration	Guaranteed by design		65	110	μΑ

Table 6. Supply and supply monitoring (continued)

#### 3.4.2 **Oscillator**

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>i</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 7. Oscillator

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
f <sub>CLK1</sub> <sup>(1)</sup>	Oscillation frequency OSC1		1.66	2.0	2.34	MHz
f <sub>CLK2</sub> <sup>(1)</sup>	Oscillation frequency OSC2		30.4	32.0	33.6	MHz

OSC1: charge pump, SPI, output drivers, watchdog OSC2: ADC

#### Power-on reset (V<sub>SREG</sub>) 3.4.3

All outputs open;  $T_i$  = -40 °C to 150 °C, unless otherwise specified.



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<sup>1.</sup> Conditions for specified current consumption:  $-V_{LIN} > (V_S-1.5 \text{ V})$   $-V_{WU} < 1 \text{ V or } V_{WU} > (V_S-1.5 \text{ V})$ 

<sup>2.</sup> I<sub>q</sub> = I<sub>q0</sub> + 2% \* I<sub>LOAD</sub> (see also Figure 8: Voltage regulator V1 characteristics (quiescent current and accuracy)

Table 8. Power-on reset (V<sub>SREG</sub>)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>POR_R</sub>	V <sub>POR</sub> threshold	V <sub>SREG</sub> rising		3.45	4.5	V
V <sub>POR_F</sub>	V <sub>POR</sub> threshold	V <sub>SREG</sub> falling <sup>(1)</sup>	2.45		3.5	V

<sup>1.</sup> This threshold is valid if  $V_{\mbox{\footnotesize SREG}}$  had already reached  $V_{\mbox{\footnotesize POR\_R(max)}}$  previously.

# 3.4.4 Voltage regulator V1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 4.5 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 9. Voltage regulator V1

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V1	Output voltage	V <sub>SREG</sub> = 13.5V		5.0		V
V <sub>SREG_absmin</sub>	V <sub>SREG</sub> absolute minimum value for controlling NRESET output	V <sub>SREG</sub> rising/falling			2	V
V1_ <sub>low_acc</sub>	Output voltage tolerance low accuracy mode	$I_{LOAD}$ = 0 mA to $I_{CMP}$ ; (Active mode) or $I_{LOAD}$ = 0 mA to $I_{PEAK}$ (V1stdby); $V_{SREG}$ = 13.5 V	-3		3	%
V1_ <sub>hi_acc</sub>	Output voltage tolerance high accuracy mode	$I_{LOAD} = I_{CMP}$ to 100 mA; (Active mode) or $I_{LOAD} = I_{PEAK}$ to 100 mA (V1stdby); $V_{SREG} = 13.5 \text{ V}$	-2		2	%
V1_ <sub>250mA</sub>	Output voltage tolerance (100 to 250mA)	I <sub>LOAD</sub> = 250 mA; V <sub>SREG</sub> = 13.5 V	-3		3	%
		$I_{LOAD}$ = 50 mA; $V_{SREG}$ = 5 V		0.2	0.4	V
V <sub>DP1</sub>	Drop-out Voltage	$I_{LOAD}$ = 100 mA; $V_{SREG}$ = 5 V		0.3	0.5	V
		$I_{LOAD}$ = 150 mA; $V_{SREG}$ = 5 V		0.45	0.6	V
I <sub>CC1</sub>	Output current in Active mode	Max. continuous load current			250	mA
I <sub>CCmax1</sub>	Short circuit output current	Current limitation	340	600	900	mA
C <sub>load1</sub>	Load capacitor1	Ceramic (+/- 20%)	0.22 <sup>(1)</sup>			μF
t <sub>TSD</sub>	V1 deactivation time after thermal shut-down			1		sec
I <sub>CMP_ris</sub>	Current comp. rising thresh	Rising current	2	4	6	mA
I <sub>CMP_fal</sub>	Current comp. falling threshold	Falling current	1.4	2.8	4.2	mA



Table 9. Voltage regulator V1 (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I <sub>CMP_hys</sub>	Current comp. Hysteresis			1.2		mA
I <sub>Peak_ris</sub> <sup>(2)</sup>	Current comp. rising thresh.	Rising current	6	12	18	mA
I <sub>Peak_fal</sub> <sup>(2)</sup>	Current comp. falling threshold	Falling current	5	10	15	mA
I <sub>Peak_hys</sub> <sup>(2)</sup>	Current comp. Hysteresis			2		mA
V1 <sub>fail</sub>	V1 fail threshold	V1 forced		2		V
t <sub>V1fail</sub>	V1 fail filter time			2		μs
t <sub>V1short</sub>	V1 short filter time			4		ms
t <sub>V1FS</sub>	V1 Fail-Safe Filter Time			2		ms
t <sub>V1off</sub>	V1 deactivation time after 8 consecutive WD failures	Tested by scan	150	200	250	ms

Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2 μF capacitor is recommended to minimize the DPI stress in the application.

Active & V1stdby mode:
High accuracy (V1 = 5V +-2%)

Active & V1stdby mode:
High accuracy (V1 = 5V +-2%)

Active & V1stdby mode:
High accuracy (V1 = 5V +-2%)

Slope = 2% \* ILoad

I<sub>CMP</sub>

I<sub>Peak</sub>

GAPG0408151630CFT

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<sup>2.</sup> In Active mode, V1 regulator is switched to high accuracy mode, dropping below the I<sub>CMP</sub> threshold regulator switches to low accuracy mode.

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### 3.4.5 Voltage regulator V2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 4.5 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 10. Voltage regulator V2

**Symbol Parameter Test condition** Min. Max. Unit Typ. ٧ V2 Output voltage V<sub>SREG</sub> = 13.5 V 5.0 Output voltage tolerance  $I_{LOAD}$  = 1 mA;  $V_{SREG}$  = 13.5 V %  $V2_{1mA}$ -6.5 6.5 (0 to 1 mA) Output voltage tolerance  $I_{LOAD}$  = 25 mA;  $V_{SREG}$  = 13.5 V -3 3 % V2 <sub>25mA</sub> (1 to 25 mA) Output voltage tolerance  $I_{LOAD}$  = 50 mA;  $V_{SREG}$  = 13.5 V 4 % V2\_50mA -4 (25 to 50 mA) Output voltage tolerance  $I_{LOAD}$  = 100 mA;  $V_{SREG}$  = 13.5 V -4 4 % V2\_100mA (50 to 100 mA) ٧  $I_{LOAD}$  = 25 mA;  $V_{SREG}$  = 5.25 V 0.3 0.4  $I_{LOAD}$  = 50 mA;  $V_{SREG}$  = 5.25 V 0.4 8.0 ٧  $V_{DP2}$ Drop-out voltage ٧  $I_{LOAD}$  = 100 mA;  $V_{SREG}$  = 13.5 V 1.6 Output current in Active Max. continuous load current 50 mΑ  $I_{CC2}$ mode Short circuit output **Current limitation** 100 150 250 mΑ I<sub>CCmax2</sub> current 0.22 (1) C<sub>load</sub> Load capacitor Ceramic (+/- 20%) μF V2 fail threshold  $V2_{fail}$ V2 forced

### 3.4.6 Reset output

t<sub>V2fail</sub>

t<sub>V2short</sub>

V2 fail filter time

V2 short filter time

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4V \le V_{SREG} \le 28V$ ;  $T_i = -40$  °C to 150 °C, unless otherwise specified.

Table 11. Reset output

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>RT1falling</sub>	Reset threshold voltage1	V <sub>V1</sub> decreasing	3.25	3.5	3.7	V
V <sub>RT2falling</sub>	Reset threshold voltage2	V <sub>V1</sub> decreasing	3.55	3.8	4	٧
V <sub>RT3falling</sub>	Reset threshold voltage3	V <sub>V1</sub> decreasing	3.75	4.0	4.2	٧



μs

<sup>1.</sup> Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor is recommended to minimize the DPI stress in the application.

Table 11. Reset output (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>RT4falling</sub>	Reset threshold voltage4	V <sub>V1</sub> decreasing	4.1	4.3	4.5	٧
V <sub>RTrising</sub>	Reset threshold voltage4	V <sub>V1</sub> increasing	4.67	4.8	4.87	٧
V <sub>RESET</sub>	Reset Pin low output voltage	V1 > 1 V; I <sub>RESET</sub> = 5 mA		0.2	0.4	٧
R <sub>RESET</sub>	Reset pull up int. resistor		10	20	30	kΩ
t <sub>RR</sub>	Reset reaction time	I <sub>LOAD</sub> = 1 mA	6		40	μs
t <sub>UV1</sub>	V1 undervoltage filter time			16		μs
t <sub>V1R</sub>	Reset pulse duration (V1 undervoltage and V1 power on reset)		1.5	2.0	2.5	ms
t <sub>WDR</sub>	Reset pulse duration (watchdog failure)		3	4	5	ms

# 3.4.7 Watchdog timing

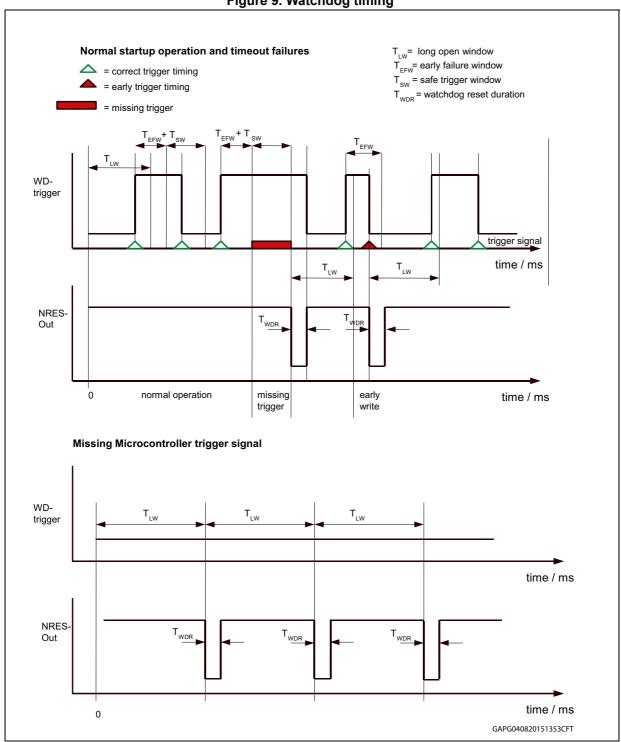
4.5 V  $\leq$  V  $_{SREG}$   $\leq$  28 V; T  $_{j}$  = -40  $^{\circ}$ C to 150  $^{\circ}$ C, unless otherwise specified.

Table 12. Watchdog timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>LW</sub>	Long open window		160	200	240	ms
T <sub>EFW1</sub>	Early Failure Window 1				4.5	ms
T <sub>LFW1</sub>	Late Failure Window 1		20			ms
T <sub>SW1</sub>	Safe Window 1		7.5		12	ms
T <sub>EFW2</sub>	Early Failure Window 2				22.3	ms
T <sub>LFW2</sub>	Late Failure Window 2		100			ms
T <sub>SW2</sub>	Safe Window 2		37.5		60	ms
T <sub>EFW3</sub>	Early Failure Window 3				45	ms
T <sub>LFW3</sub>	Late Failure Window 3		200			ms
T <sub>SW3</sub>	Safe Window 3		75		120	ms
T <sub>EFW4</sub>	Early Failure Window 4				90	ms
T <sub>LFW4</sub>	Late Failure Window 4		400			ms
T <sub>SW4</sub>	Safe Window 4		150		240	ms



Figure 9. Watchdog timing





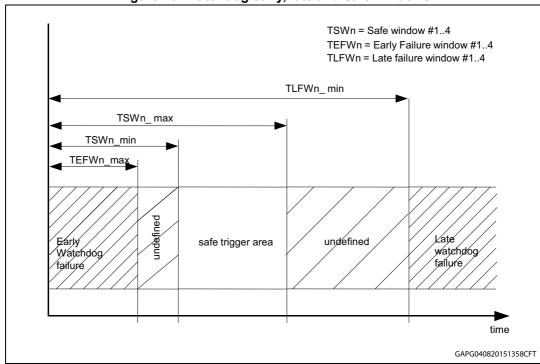


Figure 10. Watchdog early, late and safe windows

### 3.4.8 Current monitor output (CM)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified

**Symbol Parameter Test condition** Min. Max. Unit Тур. V<sub>1</sub>-1V  $V_{CM}$ Functional voltage range 0 ٧ Current monitor output ratio:  $\rm I_{CM}/I_{OUT1,4,5,6~and~7}$  (low onresistance) 1/10000  $0~V \leq V_{\text{CM}} \leq (V_1 - 1~V)$  $I_{CMr}$  $I_{CM}/I_{OUT8}$  (low on-resistance) 1/6500 I<sub>CM</sub>/I<sub>OUT 7,8</sub> (high on-resistance) 1/2000 1/1000 I<sub>CM</sub>/I<sub>OUT9,10,11,12,13,14,15</sub> and HS

Table 13. Current monitor output (CM)

Unit **Symbol Parameter Test condition** Min. Тур. Max.  $0 \ V \le V_{CM} \le (V_1 - 1 \ V);$  $I_{OUTmin} = 500 \text{ mA};$ Current monitor accuracy  $I_{OUT4,5max}$ =7.4 A; accl<sub>CMOUT1,4,5,6</sub> and 7 (low on- $I_{OUT1,6max} = 2.9 A;$ resistance)  $I_{OUT7max} = 1.4 A$  $\overline{0 \text{ V}} \le V_{\text{CM}} \le (V_1 - 1 \text{ V});$ 4% + 1% 8% + 2% Current monitor accuracy I<sub>CM acc</sub> FS<sup>(1)</sup> FS<sup>(1)</sup>  $I_{OUTmin} = 100 \text{ mA};$ accl<sub>CMOUT 8</sub> (low on-resistance) I<sub>OUT8max</sub>=0.9 A  $0 \ V \le V_{CM} \le (V_1 - 1 \ V);$ Current monitor accuracy I<sub>OUT.min</sub> = 100 mA; I<sub>OUT11,12</sub> accl<sub>CMOUT9,10,11,12,13,14,15</sub>,HS <sub>15 HS</sub> = 0.2 A; I<sub>OUT7,8</sub> and OUT7.8 (high on-resistance)  $_{\text{max}} = 0.3 \text{ A}$  $0 \ V \le V_{CM} \le (V_1 - 1 \ V);$  $I_{OUTmin} = 2 * I_{OLD};$ Current monitor accuracy  $I_{OUT4.5max} = 7.4 A;$ accl<sub>CMOUT1,4,5,6 and 7</sub> (low onresistance)  $I_{OUT1,6max} = 2.9 A;$  $I_{OUT7max} = 1.4 A$  $0 \text{ V} \le \text{V}_{\text{CM}} \le (\text{V}_1 - 1 \text{ V});$  $\text{I}_{\text{OUTmin}} = 2 * \text{I}_{\text{OLD}};$ Current monitor accuracy 4% + 1% 8% + 2% FS<sup>(1)</sup> accl<sub>CMOUT 8</sub>(low on-resistance) FS<sup>(1)</sup>  $I_{OUT8max} = 0.9 A$ I<sub>CM acc\_2ol</sub>  $0 \ V \le V_{CM} \le (V_1 - 1 \ V);$ Current monitor accuracy  $I_{OUT.min} = 2 * I_{OLD};$  $I_{OUT9,13,14max} = 0.3 A;$  $\operatorname{accl}_{CMOUT9,11,12,13,14,15,\; HS}$  and OUT7,8 (high on-resistance)  $I_{OUT11,12,15 \text{ HS}} = 0.2 \text{ A};$  $I_{OUT7,8 \text{ max}} = 0.3 \text{ A}$  $0 \text{ V} \le \text{V}_{\text{CM}} \le (\text{V}_1 - 1 \text{ V});$  $I_{\text{OUT.min}} = 2 * I_{\text{OLD}};$ 4% + 1% Current monitor accuracy 8% + 4% FS<sup>(1)</sup> FS<sup>(1)</sup> accl<sub>CMOUT10</sub>  $I_{OUT10max} = 0.4 A$ Current monitor blanking time 32 μs t<sub>cmb</sub>

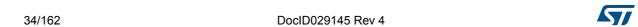
Table 13. Current monitor output (CM) (continued)

#### 3.4.9 Charge pump

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28V; T<sub>i</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 14. Charge pump electrical characteristics

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>CP</sub>	Charge pump output voltage	$V_S = 6 \text{ V}, I_{CP} = -15 \text{ mA}$	V <sub>S</sub> +6	V <sub>S</sub> +7		V
	Charge pump output voltage	$V_{S} \ge 10 \text{ V, I}_{CP} = -15 \text{ mA}$	V <sub>S</sub> +11	V <sub>S</sub> +12	V <sub>S</sub> +13.5	V
I <sub>CP</sub>	Charge pump output current <sup>(1)</sup>	$V_{CP} = V_S + 10 \text{ V};$ $V_S = 13.5 \text{ V};$ $C_1 = C_2 = C_{CP} = 100 \text{ nF}$	22.5			mA



<sup>1.</sup> FS (full scale) = I<sub>OUTmax</sub> \* I<sub>CMr</sub>

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I <sub>CPlim</sub>	Charge pump output current limitation <sup>(2)</sup>	$V_{CP} = V_S;$ $V_S = 13.5 V;$ $C_1 = C_2 = C_{CP} = 100 nF$			70	mA
V <sub>CP_low</sub>	Charge pump low threshold voltage		V <sub>S</sub> +4.5	V <sub>S</sub> +5	V <sub>S</sub> +5.5	٧
T <sub>CP</sub>	Charge pump low filter time			64		μs
f <sub>CP</sub>	Charge Pump frequency			400		kHz

Table 14. Charge pump electrical characteristics (continued)

# 3.4.10 Outputs OUT1 - OUT15, OUT\_HS

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V, all outputs open;  $T_i = -40$  °C to 150 °C, unless otherwise specified.

Table 15. Outputs OUT1 - OUT15, OUT\_HS

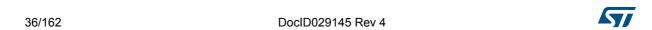
Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
r	On-resistance to supply or	$V_S = 13.5 \text{ V}; T_j = 25 \text{ °C};$ $I_{OUT1,6} = \pm 1.5 \text{A}$		300		mΩ
<sup>r</sup> ON OUT1,6	GND	$V_S = 13.5V; T_j = 130$ °C $I_{OUT1,6} = \pm 1.5 A$			600	mΩ
r	On-resistance to supply or	$V_S = 13.5V; T_j = 25 ^{\circ}C;$ $I_{OUT4} = \pm 3 ^{\circ}A$		150		mΩ
<sup>r</sup> on out4	GND	$V_S$ = 13.5 V; $T_j$ = 130 °C; $I_{OUT4}$ = ±3 A			300	mΩ
r	On-resistance to supply or	$V_S = 13.5 \text{ V; T}_j = 25^{\circ}\text{C;}$ $I_{OUT5} = \pm 3 \text{ A}$		100		mΩ
<sup>F</sup> ON OUT5	GND	$V_S$ = 13.5 V; $T_j$ = 130 °C; $I_{OUT5}$ = 3 A			200	mΩ
	On-resistance to supply in	V <sub>S</sub> = 13.5 V; T <sub>j</sub> = 25 °C; I <sub>OUT7</sub> = -0.8 A		500		mΩ
<sup>F</sup> ON OUT7	low resistance mode	V <sub>S</sub> = 13.5 V; T <sub>j</sub> = 130 °C; I <sub>OUT7</sub> = -0.8 A			1000	mΩ
	On-resistance to supply in	V <sub>S</sub> = 13.5 V; T <sub>j</sub> = 25°C; I <sub>OUT7</sub> = -0.2 A		1600		mΩ
	high resistance mode	V <sub>S</sub> = 13.5 V; T <sub>j</sub> = 130 °C; I <sub>OUT7</sub> = -0.2 A			3200	mΩ

<sup>1.</sup>  $I_{CP}$  is the minimum current the device can provide to an external circuit without  $V_{CP}$  going below  $V_S$  + 10 V.

<sup>2.</sup>  $I_{CPlim}$  is the maximum current, which flows out of the device in case of a short to  $V_{S}$ .

Table 15. Outputs OUT1 - OUT15, OUT\_HS (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
	On-resistance to supply in	$V_S$ = 13.5 V; $T_j$ = 25 °C; $I_{OUT8}$ = -0.4 A		800		mΩ
r	low resistance mode	V <sub>S</sub> = 13.5 V; T <sub>j</sub> = 130 °C; I <sub>OUT8</sub> = -0.4 A			1600	mΩ
<sup>r</sup> on out8	On-resistance to supply in	$V_S = 13.5 \text{ V}; T_j = 25 \text{ °C};$ $I_{OUT8} = -0.2 \text{ A}$		1600		mΩ
	high resistance mode	$V_S = 13.5 \text{ V; T}_j = 130 \text{ °C;}$ $I_{OUT8} = -0.2 \text{ A}$			3200	mΩ
	On-resistance to supply	$V_S = 13.5 \text{ V}; T_j = 25 \text{ °C};$ $I_{OUT9,10,13,14} = -75 \text{ mA}$		2000		mΩ
<sup>r</sup> ON OUT9,10,13,14	On-resistance to supply	$V_S = 13.5 \text{ V}; T_j = 130 \text{ °C};$ $I_{OUT9,10,13,14} = -75 \text{ mA}$			4000	mΩ
r		$V_S = 13.5 \text{ V}; T_j = 25 \text{ °C};$ $I_{OUT11,12,15, \text{ HS}} = -75 \text{ mA}$		5		Ω
FON OUT11,12,15, HS	On-resistance to supply	$V_S = 13.5 \text{ V; T}_j = 130 \text{ °C;}$ $I_{OUT11,12,15, \text{ HS}} = -75 \text{ mA}$			10	Ω
	Switched-off output current	V <sub>OUT</sub> = 0 V; standby mode	-5			μA
IQLH	high-side drivers of OUT7- 15, OUT_HS	V <sub>OUT</sub> = 0 V; active mode	-10			μΑ
1.	Switched-off output current	V <sub>OUT</sub> = 0 V; standby mode	-5			μΑ
IQLH	high-side drivers of OUT1-6	V <sub>OUT</sub> = 0 V; Active mode	-100			μΑ
	Switched-off output current	V <sub>OUT</sub> = V <sub>S</sub> ; standby mode			165	μΑ
I <sub>QLL</sub>	low-side drivers of OUT1-6	$V_{OUT} = V_S - 0.5 V$ ; active mode	-100			μΑ



# 3.4.11 Power outputs switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 16. Power outputs switching times

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
	Output delay time high-side driver on (OUT <sub>1,4,5,6</sub> )	V <sub>S</sub> = 13.5 V; V <sub>1</sub> = 5 V; corresponding low-side driver is not active <sup>(1)(2)(3)</sup>	15	40	80	μs
t <sub>d</sub> ON H	Output delay time high-side driver on (OUT <sub>7,8</sub> )	(from CSN 50% to OUT 50%) see <i>Figure 20</i>	20	40	90	μs
t	Output delay time high-side driver off (OUT <sub>1,4,5,6</sub> )	$V_S = 13.5 \text{ V}; V_1 = 5 \text{ V}$ $^{(1)(2)(3)}$ (from CSN 50% to OUT 50%) see <i>Figure 20</i>	50	150	300	μs
<sup>t</sup> d OFF H	Output delay time high-side driver off (OUT <sub>7,8</sub> )		20	70	130	μs
t <sub>d ON H</sub>	Output delay time high-side driver on (OUT9OUT15, OUT_HS)	$V_S/V_{SREG}$ = 13.5 V; $V_1$ = 5 V; (from CSN 80% to OUT 80%)			30	μs
t <sub>d OFF H</sub>	Output switch off delay time high- side driver on (OUT9OUT15, OUT_HS)	V <sub>S</sub> /V <sub>SREG</sub> = 13.5 V; V <sub>1</sub> = 5 V; (from CSN 80% to OUT 20%)			35	μs
t <sub>d</sub> on L	Output delay time low-side driver (OUT <sub>1-6</sub> ) on	$V_S = 13.5 \text{ V}; V_1 = 5 \text{ V};$ corresponding high-side driver is not active $^{(1)(2)(3)}$ (from CSN 50% to OUT 50%) see <i>Figure 20</i>	15	30	70	μs
t <sub>d OFF L</sub>	Output delay time low-side driver (OUT <sub>1-6</sub> ) off	$V_S = 13.5 \text{ V}; V_1 = 5 \text{ V}$ $^{(1)(2)(3)}$ (from CSN 50% to OUT 50%) see <i>Figure 20</i>	40	150	300	μs
t <sub>d HL</sub>	Cross current protection time	t <sub>cc ONLS_OFFHS</sub> - t <sub>d OFF H</sub> <sup>(4)</sup>	50	200	400	μs
t <sub>d LH</sub>	(OUT <sub>1-6</sub> )	t <sub>cc ONHS_OFFLS</sub> - t <sub>d OFF L</sub> (4)				į ·
dV <sub>OUT</sub> /dt	Slew rate of OUT <sub>1</sub> -OUT <sub>8</sub>	$V_S = 13.5 \text{ V}; V_1 = 5 \text{ V}$ $(1)(2)(3)$	0.1	0.2	0.6	V/µs
dVmax/dt	Maximum external applied slew rate on OUT1-OUT6 without switching on the LS and HS (only in Active mode)	Guaranteed by design	20			V/µs
dV <sub>OUT</sub> /dt	Slew rate of OUT9-OUT15, OUT_HS	$V_S/V_{SREG} = 13.5 \text{ V};$ $V_1 = 5 \text{ V}^{(1)(2)(3)}$		2		V/µs
f <sub>PWMx</sub> (00)	PWM switching frequency	$V_S/V_{SREG} = 13.5 \text{ V};$ $V_1 = 5 \text{ V}$		100		Hz
f <sub>PWMx</sub> (01)	PWM switching frequency	$V_S/V_{SREG} = 13.5 \text{ V};$ $V_1 = 5 \text{ V}$		200		Hz



Table 16. Power outputs switching times (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
f <sub>PWMx</sub> (10)	PWM switching frequency	$V_S/V_{SREG} = 13.5 \text{ V};$ $V_1 = 5 \text{ V}$		330		Hz
f <sub>PWMx</sub> (11)	PWM switching frequency	V <sub>S</sub> /V <sub>SREG</sub> = 13.5 V; V <sub>1</sub> = 5 V		500		Hz

- 1.  $R_{LOAD}$  = 16  $\Omega$  at  $OUT_{1,6}$  and  $OUT_{7,8}$  in low on-resistance mode
- 2.  $R_{LOAD} = 4 \Omega \text{ at } OUT_{4,5}$
- 3. R<sub>LOAD</sub> = 128  $\Omega$  at OUT<sub>4,9,10,11,12,13,15,15,HS</sub> and OUT<sub>7,8</sub> in high on-resistance mode
- 4.  $t_{CC}$  is the switch-on delay time if complement in half bridge has to switch off

## 3.4.12 Over Current Recovery settings

Table 17. Half bridges (OUT1, OUT4, OUT5 and OUT6) OCR timing parameters

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Tblanking		Guaranteed by Design	33	40	47	μs
Tocr_hb	Over current filter time for half bridges	Guaranteed by Design	26	32	38	μs
Toff_hb	OFF Time for half bridges OCR_FREQ=0	Guaranteed by Design	218	264	310	μs
	OFF Time for half bridges OCR_FREQ=1	Guaranteed by Design	106	128	150	μs

Table 18. High-side (OUT7, OUT8 and OUT\_HS) OCR timing parameters

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Tblanking		Guaranteed by Design	33	40	47	μs
Tocr_hs	Over current filter time for high-side	Guaranteed by Design	53	64	75	μs
Toff_hs	OFF Time for high-side OCR_FREQ=0	Guarantood by Dosign	398	480	562	μs
	OFF Time for high-side OCR_FREQ=1	Guaranteed by Design	192	232	272	μs

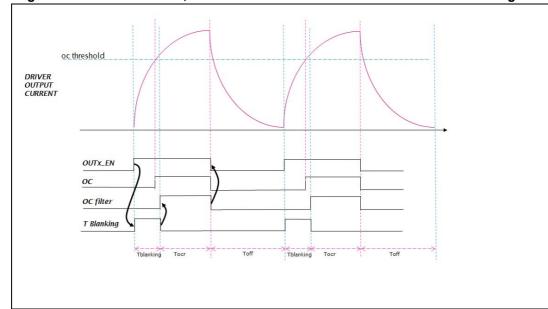
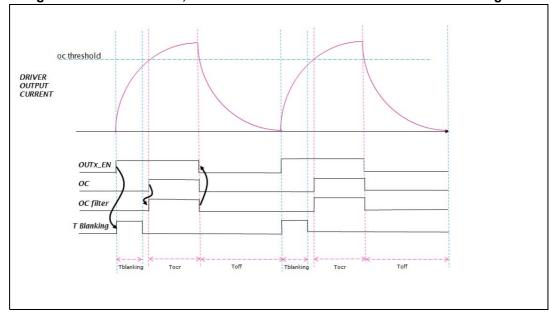


Figure 11. Hard Short case, the OC threshold is reached before end of blanking time

Figure 12. Overload case, the OC threshold is reached after end of blanking time



## 3.4.13 Current monitoring

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 19. Current monitoring

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I <sub>OC1</sub>  ,  I <sub>OC6</sub>		$V_S = 13.5 \text{ V}$ ; V1 = 5 V; sink and source	3		5	Α
I <sub>OC4</sub>	Overcurrent threshold HS & LS	$V_S$ = 13.5 V; V1 = 5 V; sink and source; $T_j$ = -40 °C to 70 °C	7.5		10	А
		$V_S = 13.5 \text{ V}; V1 = 5 \text{ V}; \text{ sink}$ and source; $T_j = 130 \text{ °C}$	6		10	Α
I <sub>OC5_1</sub>			3	4	5	Α
I <sub>OC5_2</sub>		$V_S$ = 13.5 V; V1 = 5 V; sink and source	4.5	6	7.5	Α
I <sub>OC5_3</sub>			7.5		10	Α
lla sal	Overcurrent threshold HS in low on- resistance mode		1.5		2.5	Α
loc7	Overcurrent threshold HS in high on-resistance mode	chreshold HS in low on- ode  chreshold HS in high chreshold HS in high chreshold HS in high  threshold HS in low  V <sub>S</sub> /V <sub>SREG</sub> = 13.5 V; V <sub>1</sub> = 5 V; source	0.35		0.65	Α
	Overcurrent threshold HS in low on- resistance mode		0.7		1.3	А
	Overcurrent threshold HS in high on-resistance mode		0.35		0.65	Α
ll <sub>OC9</sub> l,	Overcurrent threshold HS in high current mode		0.35		0.7	Α
I <sub>OC13</sub>  ,  I <sub>OC14</sub>	Overcurrent threshold to HS in low current mode		0.15		0.3	А
	Overcurrent threshold HS in high current mode		0.5		1	А
I <sub>OC10</sub>	Overcurrent threshold HS in low current mode		0.25		0.5	А
I <sub>OC11</sub>  ,  I <sub>OC12</sub>  ,	Overcurrent threshold HS in high current mode		0.25		0.5	Α
I <sub>OC15</sub>  ,  I <sub>OC_HS</sub>	Overcurrent threshold HS in low current mode		0.15		0.3	А
	Auto magaziami tima a limit	OUT1 to OUT6		100		ms
t <sub>AR</sub>	Auto recovery time limit	OUT7, OUT8, OUT_HS		120		ms
I <sub>OLD1</sub>  ,  I <sub>OLD6</sub>	- Under-current threshold HS & LS	V <sub>S</sub> = 13.5 V; V <sub>1</sub> = 5 V; sink	10	30	80	mA
I <sub>OLD4</sub>  ,  I <sub>OLD5</sub>	Onder-current uneshou no a Lo	and source	60	150	300	mA



Unit **Symbol Parameter Test condition** Min. Тур. Max. Under-current threshold HS in low 15 40 60 mΑ on-resistance mode |I<sub>OLD7</sub>| Under-current threshold HS in high 5 10 15 mΑ on-resistance mode Under-current threshold HS in low 10 30 45 mΑ on-resistance mode |I<sub>OLD8</sub>| Under-current threshold HS in high 5 10 15 mA on-resistance mode Under-current threshold HS in high 6 12 mΑ  $I_{OLD9}$ , current mode  $V_S/V_{SREG} = 13.5 V;$  $|I_{OLD13}|$  $V_1 = 5 V$ ; source Under-current threshold HS in low  $|I_{OLD14}|$ 0.5 4 mΑ current mode Under -current threshold HS in high 10 30 mΑ current mode |I<sub>OLD10</sub>| Under -current threshold HS in low 0.3 4 mΑ current mode Under -current threshold HS in high  $|I_{OLD11}|,$ 6 12 mΑ current mode  $|I_{OLD12}|,$  $|I_{OLD15}|$ Under -current threshold HS in low 0.85 4 mΑ |I<sub>OLD\_HS</sub>| current mode Duration of open-load Filter time of open-load signal condition to set the status 150 200 250 μs t<sub>OL\_out</sub> bit

Table 19. Current monitoring (continued)

## 3.4.14 H-bridge driver

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40°C to 150 °C, unless otherwise specified.

Table 20. H-bridge driver

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit		
Drivers for external high-side PowerMOS								
I <sub>GHx(Ch)</sub>	Average charge current (charge stage)	T <sub>j</sub> = 25 °C		0.3		Α		
D.	On-resistance (discharge-	$V_{SHx} = 0 \text{ V; } I_{GHx} = 50 \text{ mA;}$ $T_j = 25 \text{ °C}$	6	10	14	Ω		
R <sub>GHx</sub>	stage)	$V_{SHx} = 0 \text{ V; } I_{GHx} = 50 \text{ mA;}$ $T_j = 130 \text{ °C}$		14	20	Ω		
V <sub>GHHx</sub>	Gate-on voltage	$V_S = SH = 6 V; I_{CP} = 15 mA$	V <sub>SHx</sub> + 6			٧		
		V <sub>S</sub> = SH = 12 V; I <sub>CP</sub> = 15 mA	V <sub>SHx</sub> + 8	V <sub>SHx</sub> + 10	V <sub>SHx</sub> + 11.5	٧		



Tab	le 20.	H-bridge	driver	(conti	inued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit		
R <sub>GSHx</sub>	Passive gate-clamp resistance	V <sub>GHx</sub> = 0.5 V		15		kΩ		
Drivers for external low-side Power-MOS								
I <sub>GLx(Ch)</sub>	Average charge-current (charge stage)	T <sub>j</sub> = 25 °C		0.3		Α		
D	On-resistance (discharge-stage)	$V_{SLx} = 0 \text{ V; } I_{GHx} = 50 \text{ mA;}$ $T_j = 25 \text{ °C}$	6	10	14	Ω		
$R_{GLx}$		$V_{SLx} = 0 \text{ V; } I_{GHx} = 50 \text{ mA;}$ $T_j = 130 \text{ °C}$		14	20	Ω		
V.	Cata on voltage	V <sub>S</sub> = 6 V; I <sub>CP</sub> = 15 mA	V <sub>SLx</sub> + 6			٧		
$V_{GHLx}$	Gate-on voltage	V <sub>S</sub> = 12 V; I <sub>CP</sub> = 15 mA	V <sub>SLx</sub> + 8	V <sub>SLx</sub> + 10	V <sub>SLx</sub> + 11.5	V		
R <sub>GSLx</sub>	Passive gate-clamp resistance			15		kΩ		

## 3.4.15 Gate drivers for the external Power-MOS switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 21. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
T <sub>G(HL)xHL</sub>	Propagation delay time high to low (switch mode <sup>(1)</sup>	$V_S = 13.5 \text{ V; } V_{SHx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		1.5		μs
T <sub>G(HL)xLH</sub>	Propagation delay time low to high (switch mode) <sup>(1)</sup>	$V_S = 13.5 \text{ V}; V_{SLx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		1.5		μs
I <sub>GHxrmax</sub>	Maximum source current (current mode)	$V_S = 13.5 \text{ V; } V_{SHx} = 0;$ $V_{GHx} = 1 \text{ V;}$ SLEW<4:0> = 1 F <sub>H</sub>		32		mA
I <sub>GHxfmax</sub>	Maximum sink current (current mode)	$V_S = 13.5 \text{ V}, V_{SHx} = 0;$ $V_{GHx} = 2 \text{ V};$ SLEW<4:0> = 1 F <sub>H</sub>		32		mA
dl <sub>IGHxr</sub>	Source current accuracy	V <sub>S</sub> = 13.5 V; V <sub>SHx</sub> = 0; V <sub>GHx</sub> = 1 V	See	Figure 14: ranges	IGHxr	
dl <sub>IGHxf</sub>	Sink current accuracy	V <sub>S</sub> = 13.5 V; V <sub>SHx</sub> = 0; V <sub>GHx</sub> = 2 V	See	Figure 15: ranges	' IGHxf	
V <sub>DSHxrSW</sub>	Switching voltage (V <sub>S</sub> -V <sub>SH</sub> ) between current mode and switch mode (rising)	V <sub>S</sub> = 13.5 V		2.8		V
V <sub>DSHxfSW</sub>	Switching voltage (V <sub>S</sub> -V <sub>SH</sub> ) between switch mode and current mode (falling)	V <sub>S</sub> = 13.5 V		2.8		V



Table 21. Gate drivers for the external Power-MOS switching times (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t0 <sub>GHxr</sub>	Rise time (switch mode)	$V_S = 13.5 \text{ V}; V_{SHx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		45		ns
t0 <sub>GHxf</sub>	Fall time (switch mode)	$V_S = 13.5 \text{ V}; V_{SHx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		85		ns
t0 <sub>GLxr</sub>	Rise time	$V_S = 13.5 \text{ V}; V_{SLx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		45		ns
t0 <sub>GLxf</sub>	Fall time	$V_S = 13.5 \text{ V}; V_{SLx} = 0;$ $R_G = 0 \Omega; C_G = 2.7 \text{ nF}$		85		ns
tccp <sub>0001</sub>	Programmable cross-current protection time			500		ns
tccp <sub>0010</sub>	Programmable cross-current protection time			750		ns
tccp <sub>0011</sub>	Programmable cross-current protection time			1000		ns
tccp <sub>0100</sub>	Programmable cross-current protection time			1250		ns
tccp <sub>0101</sub>	Programmable cross-current protection time			1500		ns
tccp <sub>0110</sub>	Programmable cross-current protection time			1750		ns
tccp <sub>0111</sub>	Programmable cross-current protection time			2000		ns
tccp <sub>1000</sub>	Programmable cross-current protection time			2250		ns
tccp <sub>1001</sub>	Programmable cross-current protection time			2500		ns
tccp <sub>1010</sub>	Programmable cross-current protection time			2750		ns
tccp <sub>1011</sub>	Programmable cross-current protection time			3000		ns
tccp <sub>1100</sub>	Programmable cross-current protection time			3250		ns
tccp <sub>1101</sub>	Programmable cross-current protection time			3500		ns
tccp <sub>1110</sub>	Programmable cross-current protection time			3750		ns
tccp <sub>1111</sub>	Programmable cross-current protection time			4000		ns
f <sub>PWMH</sub>	PWMH switching frequency	$V_S$ = 13.5 V; $V_{SLx}$ = 0; $R_G$ = 0 $\Omega$ ; $C_G$ = 2.7 nF; PWMH-Duty-Cycle = 50%; tccp configured as 0001			50	kHz



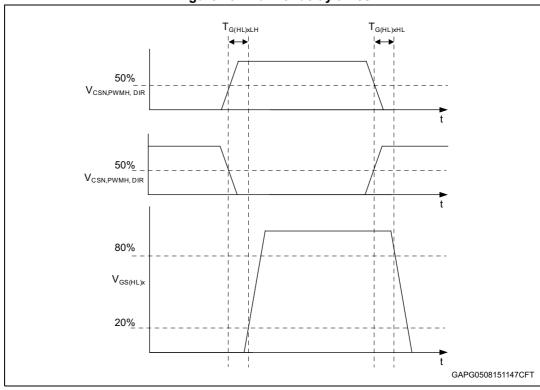
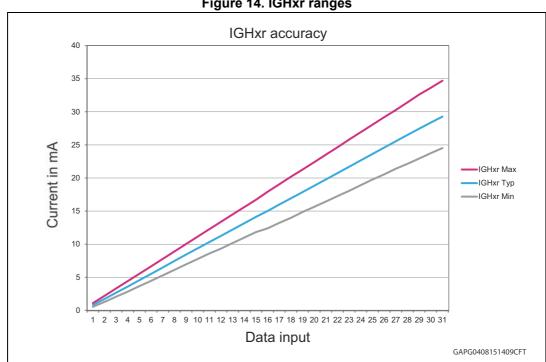


Figure 13. H-driver delay times





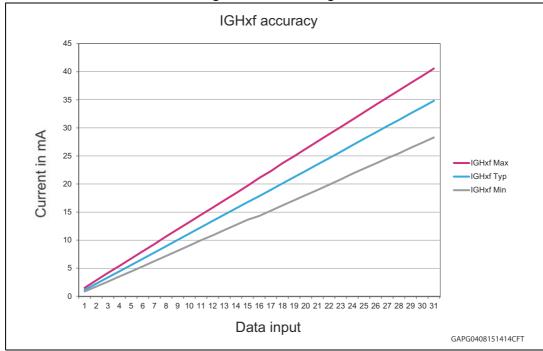


Figure 15. IGHxf ranges

## 3.4.16 Drain source monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40°C to 150 °C, unless otherwise specified.

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>SCd1_HB</sub>	Drain-source threshold voltage		0.375	0,5	0.625	V
V <sub>SCd2_HB</sub>	Drain-source threshold voltage		0.6	0,75	0.9	V
V <sub>SCd3_HB</sub>	Drain-source threshold voltage		0,85	1	1,15	V
V <sub>SCd4_HB</sub>	Drain-source threshold voltage		1,06	1,25	1,43	V
V <sub>SCd5_HB</sub>	Drain-source threshold voltage		1,27	1,5	1,73	V
V <sub>SCd6_HB</sub>	Drain-source threshold voltage		1,49	1,75	2,01	V
V <sub>SCd7_HB</sub>	Drain-source threshold voltage		1,7	2	2,3	V
t <sub>SCd_HB</sub>	Drain-source monitor filter time			6		μs
t <sub>scs_HB</sub>	Drain-source comparator settling time	$V_S$ = 13.5 V; $V_{SH}$ = jump from GND to $V_S$			5	μs

Table 22. Drain source monitoring external H-bridge

## 3.4.17 Open-load monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  28 V; 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.



Table 23. Open-load monitoring external H-bridge

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>ODSL</sub>	Low-side drain-source monitor low off-threshold voltage	V <sub>SLx</sub> = 0 V; V <sub>S</sub> = 13.5 V		0.15 V <sub>S</sub>		V
V <sub>ODSH</sub>	Low-side drain-source monitor high off-threshold voltage	V <sub>SLx</sub> = 0 V; V <sub>S</sub> = 13.5 V		0.85 V <sub>S</sub>		V
V <sub>OLSHx</sub>	Output voltage of selected SHx in open-load test mode	V <sub>SLx</sub> = 0 V; V <sub>S</sub> = 13.5 V		0.5 V <sub>S</sub>		V
R <sub>pdOL</sub>	Pull-down resistance of the non-selected <i>SHx</i> pin in open-load mode	V <sub>SLx</sub> = 0 V; V <sub>S</sub> = 13.5 V; V <sub>SHX</sub> = 4.5 V		20		kΩ
t <sub>OL_HB</sub>	Open-load filter time			2		ms

### 3.4.18 Fail safe low-side switch

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The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>S</sub>  $\leq$  18 V; T<sub>j</sub> = 40 °C to 150 °C, unless otherwise specified.

Table 24. Fail safe low-side switch

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>OUT_max</sub>	Max output voltage in case of missing supply	I <sub>OUT</sub> = 1 mA; V <sub>S</sub> = V <sub>SREG</sub> = 0 V		2	2.5	V
Resour	DC output resistance	I <sub>LOAD</sub> = 250 mA; T <sub>j</sub> = 25 °C		1.4		Ω
R <sub>DSON</sub>	DC output resistance	I <sub>LOAD</sub> = 250 mA; T <sub>j</sub> = 130 °C			2.2	Ω
I <sub>OLimit</sub>	Overcurrent limitation	8 V < V <sub>S</sub> < 16 V	500		1500	mA
t <sub>ONHL</sub>	Turn on delay time to 10% V <sub>OUT</sub>				100	μs
t <sub>OFFLH</sub>	Turn off delay time to 90% V <sub>OUT</sub>				100	μs
t <sub>SCF</sub>	Short circuit filter time			64		μs
dV <sub>max</sub> /dt	Maximum external applied slew rate on LS1_FSO and LS2_FSO without switching on LS	Guaranteed by design	60			V/µs



## 3.4.19 Wake up input WU

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  28 V; T<sub>i</sub> = 40 °C to 150 °C, unless otherwise specified.

Table 25. Wake-up inputs

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>WUthn</sub>	Wake-up negative edge threshold voltage		0.4 V <sub>SREG</sub>	0.45 V <sub>SREG</sub>	0.5 V <sub>SREG</sub>	V
V <sub>WUthp</sub>	Wake-up positive edge threshold voltage		0.5 V <sub>SREG</sub>	0.55 V <sub>SREG</sub>	0.6 V <sub>SREG</sub>	V
V <sub>HYST</sub>	Hysteresis		0.05 V <sub>SREG</sub>	0.1 V <sub>SREG</sub>	0.15 V <sub>SREG</sub>	V
t <sub>WU_stat</sub>	Static wake filter time			64		μs
I <sub>WU_stdby</sub>	Input current in standby mode	V <sub>WU</sub> < 1 V or V <sub>WU</sub> > (V <sub>SREG</sub> – 1.5 V)	5	30	60	μA
R <sub>WU_act</sub>	Input resistor to GND in Active mode and in Standby mode during Wake-up input sensing		80	160	300	kΩ
t <sub>WU_cyc</sub>	Cyclic wake filter time			16		μs

### 3.4.20 LIN transceiver

LIN 2.2 compliant for bit-rates up to 20 kBit/s SAE J2602 compatible.

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V; T<sub>junction</sub> = -40 °C to 150°C unless otherwise specified.

Table 26. LIN transmit data input: pin TxD

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>TXDLOW</sub>	Input voltage dominant level	Active mode	1.0			V
V <sub>TXDHIGH</sub>	Input voltage recessive level	Active mode			2.3	٧
V <sub>TXDHYS</sub>	V <sub>TXDHIGH</sub> -V <sub>TXDLOW</sub>	Active mode	0.2			٧
R <sub>TXDPU</sub>	TXD pull up resistor	Active mode	13	29	46	kΩ

Table 27. LIN receive data output: pin RxD

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
$V_{RXDLOW}$	Output voltage dominant level	Active mode		0.2	0.5	V
V <sub>RXDHIGH</sub>	Output voltage recessive level	Active mode	V1-0.5	V1-0.2		٧



Table 28. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
	Receiver threshold voltage		0.4	0.45	0.5	0
$V_{THdom}$	recessive to dominant state		V <sub>SREG</sub>	V <sub>SREG</sub>	V <sub>SREG</sub>	V
V <sub>Busdom</sub>	Receiver dominant state				0.4V <sub>SRE</sub>	٧
V <sub>THrec</sub>	Receiver threshold voltage dominant to recessive state		0.5 V <sub>SREG</sub>	0.55 V <sub>SREG</sub>	0.6 V <sub>SREG</sub>	٧
V <sub>Busrec</sub>	Receiver recessive state		0.6 V <sub>SREG</sub>			V
V <sub>THhys</sub>	Receiver threshold hysteresis: V <sub>THrec</sub> -V <sub>THdom</sub>		0.07 V <sub>SREG</sub>	0.1 V <sub>SREG</sub>	0.175 V <sub>SREG</sub>	V
V <sub>THcnt</sub>	Receiver tolerance center value: (V <sub>THrec</sub> +V <sub>THdom</sub> )/2		0.475 V <sub>SREG</sub>	0.5 V <sub>SREG</sub>	0.525 V <sub>SREG</sub>	V
V <sub>THwkup</sub>	Activation threshold for wake-up comparator		1.0	1.5	2	٧
V <sub>THwkdwn</sub>	Activation threshold for wake-up comparator		V <sub>SREG</sub> - 3.5	V <sub>SREG</sub> - 2.5	V <sub>SREG</sub> - 1.5	٧
t <sub>LINBUS</sub>	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom		64		μs
t <sub>dom_LIN</sub>	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom-rec	28			μs
I <sub>LINDomSC</sub>	Transmitter input current limit in dominant state	$V_{TXD} = V_{TXDLOW};$ $V_{LIN} = V_{BATMAX} = 18 \text{ V}$	40	100	180	mA
I <sub>bus_PAS_dom</sub>	Input leakage current at the receiver incl. pull-up resistor	$V_{TXD} = V_{TXDHIGH}; V_{LIN} = 0 V;$ $V_{BAT} = 12 V; Slave mode$	-1			mA
I <sub>bus_PAS_rec</sub>	Transmitter input current in recessive state	In standby modes; $V_{TXD} = V_{TXDHIGH}$ ; $V_{LIN} > 8 V$ ; $V_{BAT} < 18 V$ ; $V_{LIN} \ge V_{BAT}$			20	μA
I <sub>bus_NO_GND</sub>	Input current if loss of GND at device	GND = V <sub>SREG</sub> ; 0 V < V <sub>LIN</sub> < 18 V; V <sub>BAT</sub> = 12 V	-1		1	mA
	Input current if loss of V <sub>BAT</sub>	GND = V <sub>S</sub> ; 0 V < V <sub>LIN</sub> < 18 V Tj=-40 °C105 °C <sup>(1)</sup>			30	μA
I <sub>bus</sub>	at device	GND = V <sub>S</sub> ; 0 V < V <sub>LIN</sub> < 18 V Tj= 130 °C <sup>(2)</sup>			35	μA
V <sub>LINdom</sub>	LIN voltage level in dominant state	Active mode; $V_{TXD} = V_{TXDLOW}$ ; $R_{bus} = 500 \Omega$			1.2	V
V <sub>LINrec</sub>	LIN voltage level in recessive state	Active mode; $V_{TXD} = V_{TXDHIGH}$ ; $I_{LIN} = 10 \ \mu A$	0.8*V <sub>S</sub>			V
R <sub>LINup</sub>	LIN output pull up resistor	V <sub>LIN</sub> = 0 V	20	40	60	kΩ
C <sub>LIN</sub>	LIN input capacitance	Guaranteed by design			100	pF

- 1. 105°C is the maximum junction temperature of an unpowered device according to this test condition within the specified ambient temperature range
- 2. Used for device test only

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V  $\leq$  V<sub>S</sub>  $\leq$  28V; T<sub>j</sub> = -40 °C to 150 °C, unless otherwise specified.

Table 29. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>RXpd</sub>	Receiver propagation delay time	$\begin{split} t_{RXpd} &= \text{max}(t_{RXpdf}, t_{RXpdf}); \\ t_{RXpdf} &= t(0.5 \text{ V}_{RXD})\text{-}t(0.45 \text{ V}_{LIN}); \\ t_{RXpdr} &= t(0.5 \text{ V}_{RXD})\text{-}t(0.55 \text{ V}_{LIN}); \\ \text{V}_{SREG} &= 12 \text{ V}; \text{ C}_{RXD}\text{=}20 \text{ pF}; \\ \text{R}_{bus} &= 1 \text{ k}\Omega, \text{ C}_{bus} = 1 \text{ nF}; \text{ R}_{bus} = 660 \ \Omega, \\ \text{C}_{bus} &= 6.8 \text{ nF}; \text{ R}_{bus} = 500 \ \Omega, \\ \text{C}_{bus} &= 10 \text{ nF} \end{split}$			6	μs
t <sub>RXpd_sym</sub>	Symmetry of receiver propagation delay time (rising vs. falling edge)	$t_{RXpd\_sym} = t_{RXpdr} - t_{RXpdf}; V_{SRE} = 12 V;$ $R_{bus} = 1 k\Omega; C_{bus} = 1 nF; C_{RXD} = 20 pF$	-2		2	μs
D1	Duty Cycle 1	$\begin{split} & TH_{Rec}(max) = 0.744 * V_{SREG}; \\ & TH_{Dom}(max) = 0.581 * V_{SREG}; \\ & V_{SREG} = 7 \text{ to } 18 \text{ V, } t_{bit} = 50  \mu\text{s;} \\ & D1 = t_{bus\_rec}(min) \text{ / } (2 \text{ x } t_{bit}); \\ & R_{bus} = 1 \text{ k}\Omega, C_{bus} = 1 \text{ nF; } R_{bus} = 660 \Omega, \\ & C_{bus} = 6.8 \text{ nF; } R_{bus} = 500 \Omega, \\ & C_{bus} = 10 \text{ nF} \end{split}$	0.396			
D2	Duty Cycle 2	$\begin{split} & TH_{Rec}(min) = 0.422^* \ V_{SREG}; \\ & TH_{Dom}(min) = 0.284^* \ V_{SREG}; \\ & V_{SREG} = 7.6 \ to \ 18 \ V, \ t_{bit} = 50 \ \mu s; \\ & D2 = t_{bus\_rec}(max) \ / \ (2 \ x \ t_{bit}); \\ & R_{bus} = 1 \ k\Omega, \ C_{bus} = 1 \ nF; \ R_{bus} = 660 \ \Omega, \\ & C_{bus} = 6.8 \ nF; \ R_{bus} = 500 \ \Omega, \\ & C_{bus} = 10 \ nF \end{split}$			0.581	
D3	Duty Cycle 3	$\begin{split} & \text{TH}_{\text{Rec}}(\text{max}) = 0.778^* \ \text{V}_{\text{SREG}}; \\ & \text{TH}_{\text{Dom}}(\text{max}) = 0.616^* \ \text{V}_{\text{SREG}}; \\ & \text{V}_{\text{SREG}} = 7 \\ & \text{to 18 V, t}_{\text{bit}} = 96 \ \mu\text{s}; \\ & \text{D3} = \text{t}_{\text{bus}\_\text{rec}}(\text{min}) \ / \ (2 \ \text{x} \ \text{t}_{\text{bit}}); \\ & \text{R}_{\text{bus}} = 1 \ \text{k}\Omega, \ C_{\text{bus}} = 1 \ \text{nF}; \ \text{R}_{\text{bus}} = 660 \ \Omega, \\ & \text{C}_{\text{bus}} = 6.8 \ \text{nF}; \ \text{R}_{\text{bus}} = 500 \ \Omega, \\ & \text{C}_{\text{bus}} = 10 \ \text{nF} \end{split}$	0.417			
D4	Duty Cycle 4	$\begin{split} & TH_{Rec}(min) = 0.389^* \ V_{SREG}; \\ & TH_{Dom}(min) = 0.251^* \ V_{SREG}; \\ & V_{SREG} = 7.6 \ to \ 18 \ V, \ t_{bit} = 96 \ \mu s; \\ & D4 = t_{bus\_rec}(max) \ / \ (2 \ x \ t_{bit}); \\ & R_{bus} = 1 \ k\Omega, \ C_{bus} = 1 \ nF; \ R_{bus} = 660 \ \Omega, \\ & C_{bus} = 6.8 \ nF; \ R_{bus} = 500 \ \Omega, \\ & C_{bus} = 10 \ nF \end{split}$			0.590	
t <sub>dom(TXDL)</sub>	TXDL dominant time- out			12		ms



Table 2	29. LIN transceiver timing (continue	a)	
ter	Test condition	Min.	Тур.

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>LIN</sub>	LIN permanent recessive time-out			40		μs
t <sub>dom(bus)</sub>	LIN Bus permanent dominant time-out			12		ms

 $V_{\text{\tiny LIN}}$ time GAPG0608151126CFT

Figure 16. LIN transmit, receive timing

### SPI 3.4.21

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V <  $V_{SREG}$  < 18 V; V1 = 5 V; all outputs open;  $T_j$  = -40 °C to 150 °C, unless otherwise specified.

Table 30. Input: CSN

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>CSNLOW</sub>	Input voltage low level	Normal mode	1.0			V
V <sub>CSNHIGH</sub>	Input voltage high level	Normal mode			2.3	٧
V <sub>CSNHYS</sub>	V <sub>CSNHIGH</sub> - V <sub>CSNLOW</sub>	Normal mode	0.2			٧
I <sub>CSNPU</sub>	CSN Pull up resistor	Normal mode	13	29	46	kΩ

Table 31. Inputs: CLK, DI

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>set</sub>	Delay time from standby to Active mode	Time until SPI, ADC and OUT15/OUT_HS are operative		10		μs
t <sub>set_CP</sub>	Delay time from standby to Active mode	Time until power stages that are supplied by the CP are operative	560	750	960	μs



145.5 51							
Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit	
V <sub>in_L</sub>	Input low level		1.0			V	
V <sub>in_H</sub>	Input high level				2.3	V	
V <sub>in_Hyst</sub>	Input hysteresis		0.2			V	
I <sub>pdin</sub>	Pull down current at input	V <sub>in</sub> = 1.5 V	5	30	60	μΑ	
C <sub>in</sub> <sup>(1)</sup>	Input capacitance at input CSN, CLK, DI and PWM <sub>1,2</sub>	Guaranteed by design			15	pF	
f <sub>CLK</sub>	SPI input frequency at CLK				4	MHz	

Table 31. Inputs: CLK, DI (continued)

Table 32. DI, CLK and CSN timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>CLK</sub>	Clock period		250			ns
t <sub>CLKH</sub>	Clock high time		100			ns
t <sub>CLKL</sub>	Clock low time		100			ns
t <sub>set_CSN</sub>	CSN setup time, CSN low before rising edge of CLK		150			ns
t <sub>set_CLK</sub>	CLK setup time, CLK high before rising edge of CSN		150			ns
t <sub>set_DI</sub>	DI setup time		25			ns
t <sub>hold_DI</sub>	DI hold time		25			ns
t <sub>r_in</sub>	Rise time of input signal DI, CLK, CSN				25	ns
t <sub>f_in</sub>	Fall time of input signal DI, CLK, CSN				25	ns

Note: See Figure 18: SPI input timing.

Table 33. Output: DO

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>DOL</sub>	Output low level	I <sub>DO</sub> = -4 mA			0.5	V
V <sub>DOH</sub>	Output high level	I <sub>DO</sub> = 4 mA	V1 - 0.5			V
I <sub>DOLK</sub>	3-state leakage current	V <sub>CSN</sub> = V1, 0 V < V <sub>DO</sub> < V1	-10		10	μΑ
C <sub>DO</sub>	3-state input capacitance	Guaranteed by design		10	15	pF



<sup>1.</sup> Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 34. DO timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>r DO</sub>	DO rise time	$C_L = 50 \text{ pF}; I_{LOAD} = -1 \text{ mA}$			25	ns
t <sub>f DO</sub>	DO fall time	$C_L = 50 \text{ pF}; I_{LOAD} = -1 \text{ mA}$			25	ns
t <sub>en DO tri L</sub>	DO enable time from 3-state to low level	$C_L$ = 50 pF; $I_{LOAD}$ = -1 mA; pull-up load to V1		50	100	ns
t <sub>dis DO L tri</sub>	DO disable time from low level to 3-state	$C_L$ = 50 pF; $I_{LOAD}$ = -1 mA; pull-up load to V1		50	100	ns
t <sub>en DO tri H</sub>	DO enable time from 3-state to high level	C <sub>L</sub> = 50 pF; I <sub>LOAD</sub> = -1 mA; pull-down load to GND		50	100	ns
t <sub>dis DO H tri</sub>	DO disable time from high level to 3-state	$C_L$ = 50 pF; $I_{LOAD}$ = -1 mA; pull-down load to GND		50	100	ns
t <sub>d DO</sub>	DO delay time	$V_{DO}$ < 0.3 V1; $V_{DO}$ > 0.7 V1; $C_L$ = 50 pF		30	60	ns

Note: See Figure 19: SPI output timing.

Table 35. CSN timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>CSN_HI,min</sub>	Minimum CSN high time, active mode	Transfer of SPI-command to Input Register	6			μs
t <sub>CSNfail</sub>	CSN low timeout		20	35	50	ms

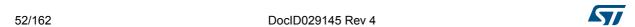
Note: See Figure 20: SPI CSN - output timing.

## 3.4.22 Input LIN\_FLASH for Flash mode

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6V \le V_{SREG} \le 18$ ; V1 = 5 V;  $T_j = -40 \,^{\circ}\text{C}$  to  $150 \,^{\circ}\text{C}$ .

Table 36. Inputs LIN\_FLASH for Flash mode

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>flashL</sub>	Input low level (V <sub>LIN_FLASH</sub> for exit from Flash mode)		6.1	7.25	8.4	٧
$V_{flashH}$	Input high level (V <sub>LIN_FLASH</sub> for transition into Flash mode)		7.4	8.4	9.4	٧
V <sub>flashHYS</sub>	Input voltage hysteresis		0.6	0.8	1.0	٧



## 3.4.23 Inputs DIR, DIRH, PWMH

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V; T<sub>i</sub> = -40 °C to 150 °C.

Table 37. Inputs DIR, DIRH, PWMH

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>IL</sub>	Input voltage low level	V <sub>SREG</sub> = 13.5 V	1			V
V <sub>IH</sub>	Input voltage high level	V <sub>SREG</sub> = 13.5 V			2.3	٧
V <sub>IHYS</sub>	Input hysteresis	V <sub>SREG</sub> = 13.5 V	0.2			٧
I <sub>in</sub>	Input pull-down current	V <sub>SREG</sub> = 13.5 V	5	30	60	μA

## 3.4.24 Debug input

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V; T<sub>i</sub> = -40 °C to 150 °C.

Table 38. Debug input

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>dIL</sub>	Input voltage low level	V <sub>SREG</sub> = 13.5 V	1			V
V <sub>dIH</sub>	Input voltage high level	V <sub>SREG</sub> = 13.5 V			2.3	٧
V <sub>dIHYS</sub>	Input hysteresis	V <sub>SREG</sub> = 13.5 V	0.2			٧
R <sub>din</sub>	Pull-down resistor	V <sub>DEBUG</sub> = 6 to 18 V	2.5	5	7.5	kΩ

### 3.4.25 ADC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V, T<sub>i</sub> = -40 °C to 150 °C.

**Table 39. ADC characteristics** 

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>con</sub>	Conversion time			2.5		μs
f <sub>ADC</sub>	Clock frequency (see f <sub>clk</sub> 2)			8		MHz
		Voltage divider + reference <sup>(1)</sup>	-2		2	
		Overall accuracy for WU input: WU = 22 V	-3		3	
Acc	Accuracy	Overall accuracy for WU input: WU = 18 V	-3.5		3.5	%
		Overall accuracy for WU input: WU = 6 V	-4		4	
		Overall accuracy for WU input: WU = 4.5 V	-4.6		4.6	



Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
IE <sub>I</sub> I	Integral linearity error				4	LSB
IE <sub>D</sub> I	Differential linearity error				2	LSB
V <sub>AINVS</sub>	Conversion voltage range (V <sub>S</sub> , V <sub>SREG</sub> & WU)		1		22	V
V <sub>AINTemp</sub>	Conversion voltage range (T <sub>CL</sub> 1T <sub>CL</sub> 6)		0		2	V

Table 39. ADC characteristics (continued)

## 3.4.26 Temperature diode characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V, T<sub>i</sub> = -40 °C to 150 °C

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>TROOM 1-6</sub>	T <sub>SENSE</sub> output voltage at 25 °C	V <sub>S</sub> = 12 V; T = 25 °C	_	1.4		V
V <sub>TSENSE1-6</sub>	T <sub>SENSE</sub> output voltage 1 - 8	T = 25 °C; T = 130 °C; T = -40 °C	_	-4		mV/K

Table 40. Temperature diode characteristics

## 3.4.27 Interrupt outputs

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V, T<sub>i</sub> = -40 °C to 150 °C

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
$V_{INTL}$	Output low level	I <sub>INT</sub> = -4 mA			0.5	V
V <sub>INTH</sub>	Output high level	I <sub>INT</sub> = 4 mA	V1 - 0.5			V
I <sub>INTLK</sub>	3-state leakage current	0 V < V <sub>INT</sub> < V1	-10		10	μA
t <sub>Interrupt</sub>	Interrupt pulse duration (NINT, RxD_L/NINT)			56		μS
t <sub>Int_react</sub>	Interrupt reaction time	Tested by scan chain	6		40	μs

**Table 41. Interrupt outputs** 



<sup>1.</sup> Guaranteed by design.

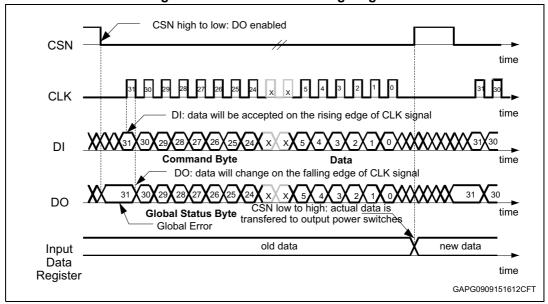
### 3.4.28 Timer1 and Timer2

6 V  $\leq$  V<sub>SREG</sub>  $\leq$  18 V; T<sub>i</sub> = -40 °C to 150 °C

Table 42. Timer1 and Timer2

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
ton 1	Timer on time			0.1		ms
ton 2	Timer on time			0.3		ms
ton 3	Timer on time			1		ms
ton 4	Timer on time			10		ms
ton 5	Timer on time			20		ms
T1	Timer period			10		ms
T2	Timer period			20		ms
Т3	Timer period			50		ms
T4	Timer period			100		ms
T5	Timer period			200		ms
Т6	Timer period			500		ms
T7	Timer period			1000		ms
Т8	Timer period			2000		ms

Figure 17. SPI – transfer timing diagram



The SPI can be driven by a micro controller with its SPI peripheral running in the following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.



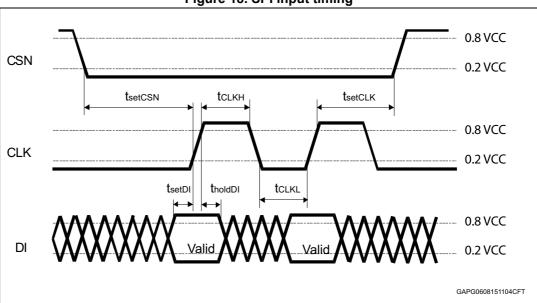


Figure 18. SPI input timing

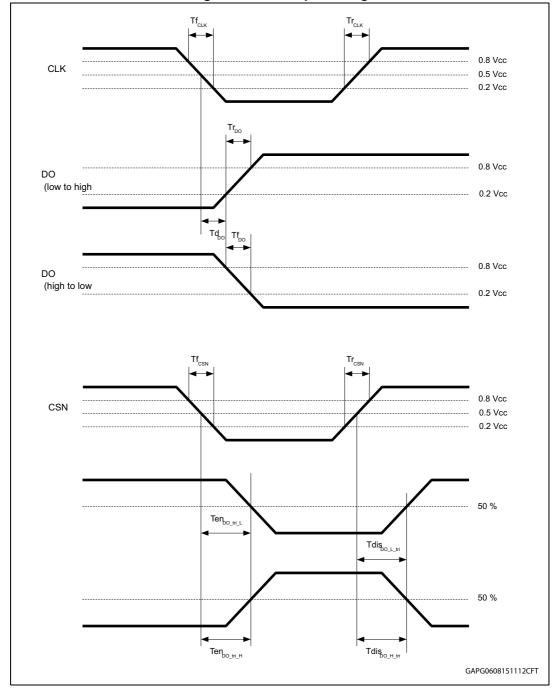


Figure 19. SPI output timing

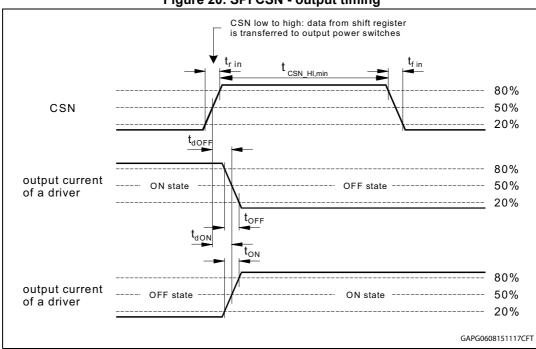
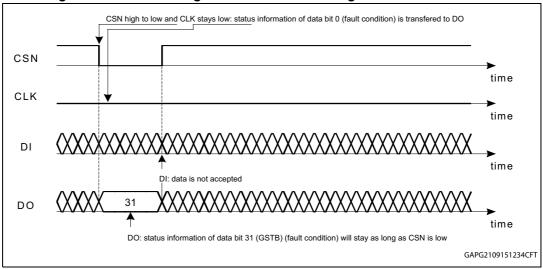


Figure 20. SPI CSN - output timing





## 3.4.29 SGND loss comparator

 $T_i$  = -40 °C to 150 °C, unless otherwise specified.

Table 43. SGND loss comparator

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V <sub>SGNDloss</sub>	V <sub>SGND</sub> loss threshold	(V <sub>SGND</sub> – V <sub>PGND</sub> )	100	270	500	mV
t <sub>SGNDloss</sub>	V <sub>SGND</sub> loss filter time		5	7	9	μs



# 4 Application information

# 4.1 Supply V<sub>S</sub>, V<sub>SREG</sub>

V<sub>SREG</sub> supplies voltage regulators V1 and V2, all internal regulated voltages for analog and digital functionality, LIN and both P-channel high-side switches OUT15 and OUT\_HS.

All other high-sides, Fail Safe block and the charge pump are supplied by V<sub>S</sub>.

In case the  $V_{SREG}$  pin is disconnected, all power outputs connected to  $V_S$  are automatically switched off.

## 4.2 Voltage regulators

The device contains two independent and fully protected low drop voltage regulators designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors >220 nF.

### 4.2.1 Voltage regulator: V1

The V1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current to supply the system microcontroller. The V1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode. The V1 voltage regulator is supplied by pin  $V_{SREG}$ .

In addition, the V1 regulator supplies the devices internal loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors >220 nF.

In case the device temperature exceeds the TSD1 threshold (either cluster or grouped mode) the V1 regulator remains on. The micro controller has the possibility for interaction or error logging. If the chip temperature exceeds the TSD2 threshold (TSD2 > TSD1), V1 will be deactivated and all wakeup sources (LIN, WU and Timer) are disabled. After  $t_{TSD}$ , the voltage regulator will restart automatically. If the restart fails 7 times within one minute the devices enter the Forced Vbat\_standby mode. The status bit FORCED\_SLEEP\_TSD2/V1SC (SR1) is set.

## 4.2.2 Voltage regulator: V2

The voltage regulator V2 is supplied by pin  $V_{SREG}$  and can supply additional 5 V loads such as sensors or potentiometers. The maximum continuous load current is 50 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short-circuit (short to ground and battery supply voltage)
- Reverse biasing



### 4.2.3 Voltage regulator failure

The V1, and V2 regulator output voltages are monitored.

In case of a drop below the failure thresholds (V1 < V1<sub>fail</sub> for t >  $t_{V1fail}$ , V2 < V2<sub>fail</sub> for t >  $t_{V2fail}$ ), the failure bits V1FAIL, V2FAIL (SR 2) are latched.

## 4.2.4 Short to ground detection

At turn-on of the V1 and V2 regulators, a short-to-GND condition is detected by monitoring the regulator output voltage.

If V1 or V2 is below the V1<sub>fail</sub> (or V2<sub>fail</sub>) threshold for  $t > t_{V1short}$  ( $t > t_{V2short}$ ) after turn-on, the devices will identify a short circuit condition at the related regulator will be switched off.

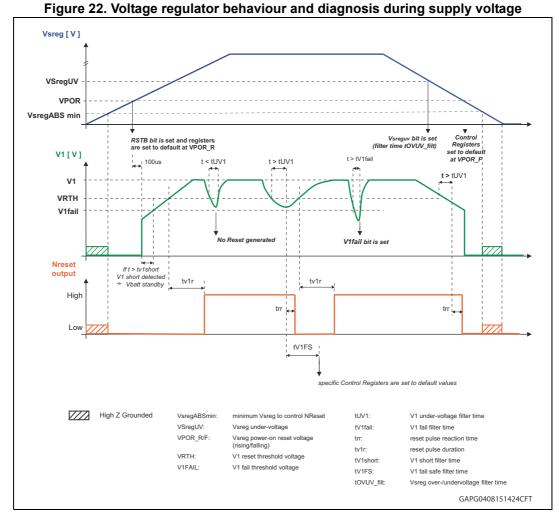
In case of V1 short-to-GND the device enters Forced Vbat\_standby mode automatically. Bits FORCED\_SLEEP\_TSD2/V1SC and (SR 1) V1FAIL (SR 2) are set.

In case of a V2 short-to-GND failure the V2SC (SR 2) and V2FAIL (SR 2) bits are set.

Once the output voltage of the corresponding regulator exceeded the  $V1_{fail}$  ( $V2_{fail}$ ) threshold the short-to-ground detection is disabled. In case of a short-to-ground condition, the regulator is switched off due to thermal shutdown. V1 is switched off at TSD2, V2 is switched off at TSD1.



## 4.2.5 Voltage regulator behavior



# 4.3 Operating modes

The devices can be operated in the following operating modes:

- Active
- LIN Flash
- V1\_standby
- VBAT\_standby
- Debug

### 4.3.1 Active mode

All functions are available and the device is controlled by SPI.

### 4.3.2 Flash mode

To program the system microcontroller via LIN bus signals, the devices can be operated in LIN Flash mode. The watchdog is disabled in this mode.

The Flash mode is entered by applying an external voltage at the pin:

• V<sub>LIN FLASH</sub> ≥ V<sub>FlashH</sub> (LIN Flash mode)

In LIN Flash mode the maximum bitrate is increased to 100 kbit/s automatically (LIN\_HS\_EN = 1).

A transition from Flash mode to V1\_standby or Vbat\_standby mode is not possible.

At exit from Flash modes ( $V_{LIN\_FLASH} < V_{FlashL}$ ) no NReset pulse is generated. The watchdog starts with a Long Open Window ( $t_{IW}$ ).

### 4.3.3 SW-debug mode

To allow software debugging, the watchdog can be deactivated by applying an external voltage to the DEBUG input pin ( $V_{debug} > V_{diH}$ ).

In Debug mode, all device functionality and Operating modes are available. The watchdog is deactivated. At Exit from Debug mode ( $V_{debug} < V_{diL}$ ) the watchdog starts with a Long Open Window.

Note:

The device includes a test mode. This mode is activated by a dedicated sequence which includes a high voltage at the Debug Pin. The Debug Pin must be kept at nominal voltage levels in order to avoid accidental activation of the test mode.

### 4.3.4 V1\_standby mode

The transition from Active mode to V1 standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the V1 voltage regulator remains active.

After the V1\_standby command (CSN low to high transition), the device enters V1\_standby mode immediately and the watchdog starts a Long Open Window ( $t_{LW}$ ). The watchdog is deactivated as soon as the V1 load current drops below the  $I_{CMP}$  threshold ( $I_{V1} < I_{cmp}$  fal).

The V1 load current monitoring can be deactivated by setting ICMP = 1. In this configuration the watchdog will be deactivated upon transition into V1\_standby mode without monitoring the V1 load current.

Writing ICMP (CR 34) = 1 is only possible with the first SPI command after setting ICMP\_CONFIG\_EN (Config Reg) = 1.

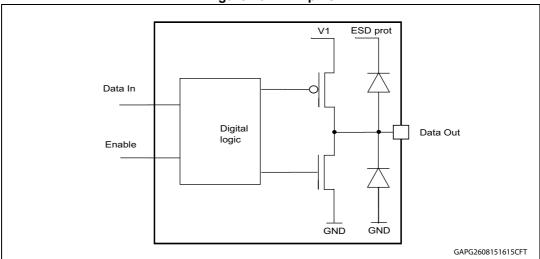
The ICMP\_CONFIG\_EN bit is reset to 0 automatically with the next SPI command.

Power outputs (except OUT\_HS & OUT15) are switched off in V1\_standby mode. OUT\_HS & OUT15 remain in the configuration programmed prior to the standby command in order to enable (cyclic) supply of external contacts. The timer signal (Timer1 or Timer2) can be mirrored to the NINT output pin during V1\_standby mode.

LIN transmitter (TxDL) is off.

### 4.3.5 Interrupt

Figure 23. NINT pins



### RxDL/NINT indicates:

 a wake-up event from V1\_standby mode and the programmable timer interrupt RxDL/NINT pin is pulled low for t = t<sub>interrupt</sub>.

### NINT indicates:

In Active mode:

 $V_{SREG}$  dropped below the programmed early warning threshold in Control Register 3 ( $V_{SREG}$  <  $V_{SREG}$  =  $V_{SREG}$  <  $V_{SREG}$  =  $V_{SREG$ 

- Programmable timer interrupt; An NINT pulse is generated at the beginning of the timer on-time (Timer 1 or Timer2)
- Wake-up from V1\_standby mode by any wake-up source

NINT is pulled low for  $t = t_{interrupt}$ 

In case of increasing V1 load current during V1\_standby mode ( $I_{V1} > I_{cmp\_ris}$ ), the device remains in standby mode and the watchdog starts with a Long Open Window. No Interrupt signal is generated.

### 4.3.6 VBAT\_standby mode

The transition from Active mode to Vbat\_standby mode is initiated by an SPI command. In Vbat\_standby mode, the voltage regulators V1 and V2 (depending on configuration in CR 1), the power outputs (except OUT15 and OUT\_HS) as well as LIN transmitter are switched off.

An NReset pulse is generated upon wake-up from Vbat\_standby mode.

# 4.4 Wake-up from Standby modes

A wake-up from standby mode will switch the device to Active mode. This can be initiated by one or more of the following events:



Wake up source	Description	
LIN bus activity	Always enabled	
Level change of WU	Can be configured or disabled by SPI	
I <sub>V1</sub> >I <sub>cmp_ris</sub>	Device remains in $V1\_standby\ mode$ but watchdog is enabled (If $I_{CMP} = 0$ ). No interrupt is generated.	
Timer Interrupt / Wake up of μC by TIMER	Programmable by SPI:  - V <sub>1</sub> _standby mode: device wakes up after programmable timer expiration. NINT and RxDL/NINT interrupt signals are generated  - V <sub>bat</sub> _standby mode: device wakes up after programmable timer expiration, V1 regulator is turned on and NReset signal is generated	
SPI Access	Always active (except in V <sub>BAT_STANDBY</sub> <i>mode</i> )  Wake up event: CSN is low and first rising edge on CLK	

Table 44. Wake-up events description

### 4.4.1 Wake up input

The WU input can be configured as wake-up source. The wake-up input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level.

For static contact monitoring, a filter time of  $t_{WU\_STAT}$  is implemented. The filter is started when the input voltage passes the specified threshold  $V_{WU\_THP}$  or  $V_{WU\_THN}$ .

Cyclic contact monitoring allows periodical activation of the wake-up input to read the status of the external contact. The periodical activation can be configured to Timer 1 or Timer 2. The input signal is filtered with a filter time of  $t_{WU\_CYC}$  after a delay (80% of the configured Timer on-time). A Wake-up will be processed if the status has changed versus the previous cycle. The buffered output OUT\_HS can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

In standby modes, the input WU is configurable with an internal pull-up or pull-down current source according to the setup of the external contact. In Active mode the inputs have an internal pull down resistor ( $R_{WU\_act}$ ) and the input status can be read by SPI. Static sense should be configured before the read operation is started in order to reflect the actual input level.

# 4.5 Functional overview (truth table)

Table 45. Status of different functions/features vs operating modes

Function	Comments	Operating modes		
		Active mode	V <sub>1</sub> -standby static mode (cyclic sense)	V <sub>bat</sub> -standby static mode (cyclic sense)
Voltage regulator V1	V <sub>OUT</sub> = 5 V	On	On <sup>(1)</sup>	Off
Voltage regulator V2	V <sub>OUT</sub> = 5 V	On/ Off <sup>(2)</sup>	On <sup>(2)</sup> / Off	On <sup>(2)</sup> / Off
Reset generator		On	On	Off



Table 45. Status of different functions/features vs operating modes (continued)

	Comments	Operating modes		
Function		Active mode	V <sub>1</sub> -standby static mode (cyclic sense)	V <sub>bat</sub> -standby static mode (cyclic sense)
Window watchdog	V <sub>1</sub> monitor	On	Off (on if $I_{V1} > I_{CMP}$ and $I_{CMP} = 0$ )	Off
Wake up		Off	Active <sup>(3)</sup>	Active <sup>(3)</sup>
HS-cyclic supply	Oscillator time base	On / Off	On <sup>(2)</sup> / Off	On <sup>(2)</sup> / Off
LIN	LIN 2.2a	On	Off <sup>(4)</sup>	Off <sup>(4)</sup>
Oscillator OSC1	2 MHz	On	On/Off <sup>(5)</sup>	On/Off <sup>(5)</sup>
Oscillator OSC2	32 MHz	ON	Off	Off
V <sub>SREG-Monitor</sub>		On	(6)	(6)
V <sub>S-Monitor</sub>		On	Off	Off
H-bridge Gate Driver, bridge drivers, all high-side drivers (except OUT_HS & OUT15) supplied by V <sub>S</sub>		On/ Off <sup>(2)</sup>	Off	Off
Fail-safe low-side switches		On/ Off <sup>(7)</sup>	On	On
Short circuit protection for fail-safe low-side switches (in case LS is switched on)		On	On	On
OUT_HS & OUT15 (P-channel HS) supplied by V <sub>SREG</sub>		On/ Off <sup>(2)</sup>	On/ Off <sup>(2)</sup>	On/ Off <sup>(2)</sup>
Charge pump		On	Off	Off
ADC (SPI read out and V <sub>SREG</sub> early warning interrupt)		On	Off	Off
Thermal shutdown TSD2		On	On	Off
Thermal shutdown TSD1x for OUT_HS and OUT15 (P-channel HS)		On	On/ Off <sup>(2)</sup>	On/ Off <sup>(2)</sup>

- 1. Supply the processor in low current mode.
- 2. According to SPI setting and DIR.
- 3. Unless disabled by SPI.
- 4. The bus state is internally stored when going to standby mode. A change of bus state will lead to a wake-up after exceeding of internal filter time.
- 5. ON, if cyclic sense is enabled or during wake-up request.
- 6. Cyclic activation = pulsed ON during cyclic sense.
- 7. ON in Fail-Safe mode; if standby mode is entered with active Fail-safe mode the output remains ON in standby mode.



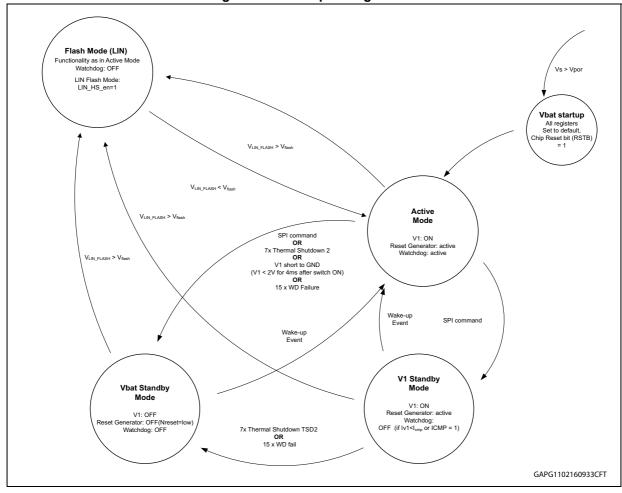


Figure 24. Main operating modes

# 4.6 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle.

After power-on or standby mode, the watchdog is started with a timeout (Long Open Window  $t_{LW}$ ). The timeout allows the micro controller to run its own setup and then to start the window watchdog by setting TRIG (CR1,ConfigReg) =1

Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit TRIG (CR1,Config Reg) within the safe trigger area  $T_{SWX}$ .

The trigger time is configurable by SPI. A correct watchdog trigger signal will immediately start the next cycle. After 8 watchdog failures in sequence, the V1 regulator is switched off for  $t_{V1OFF}$ . After 7 additional watchdog failures the V1 regulator is turned off permanently and the device goes into Forced Vbat\_standby mode. The status bit FORCED\_SLEEP\_WD (SR 1) is set. A wake-up is possible by LIN.

After wake-up from Forced Vbat\_standby mode and the watchdog trigger still fails, the device enters Forced Vbat\_standby mode again after one Long Open Window.

This actually produces an additional watchdog failure but the watchdog fail counter will remain at maximum value of 15 failures.

This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

In case of a Watchdog failure, the power outputs and V2 are switched off and the status bit WDFAIL (SR 1) is set to 1. A reset pulse is generated at NReset output and the device enters Fail-safe mode. Control registers are set to their Fail Safe values and the Fail-safe low-side switches are turned on. Please refer to chapter Section 4.7: Fail-safe mode for more details.

The following diagrams illustrate the Watchdog behavior of the devices. The diagrams are split into 3 parts. The first diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. *Figure 27: Watchdog in Flash mode* shows the transition in and out of Flash modes. *Figure 25, Figure 26* and *Figure 27* can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

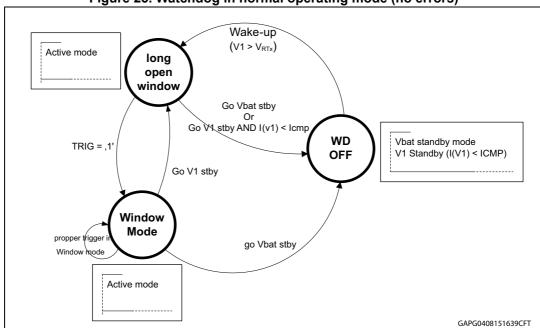


Figure 25. Watchdog in normal operating mode (no errors)



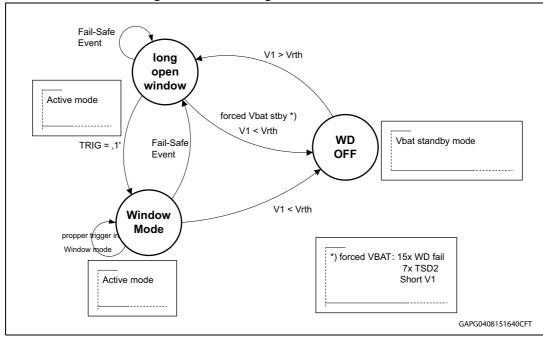
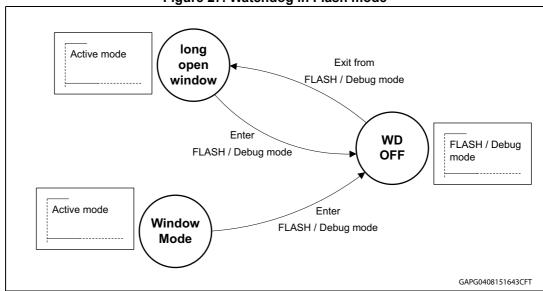


Figure 26. Watchdog with error conditions





Note:

Whenever the device is operated without servicing the mandatory watchdog trigger events, a sequence of 15 consecutive reset events is performed and the device enters the Forced\_Vbat\_Stby mode with bit FORCED\_SLEEP\_WD in SR1 set.

If the device is woken up after such a forced VBAT\_Standby condition and the watchdog is still not serviced, the device, after one long open watchdog window will re-enter the same Forced\_Vbat\_Stby mode until the next wake up event. In this case, an additional watchdog failure is generated, but the fail counter is not cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

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### 4.6.1 Change watchdog timing

The watchdog trigger time is configured by setting WD\_TIME\_x (CR 2). Writing to these bits is possible only using the first SPI command after setting WD\_CONFIG\_EN = 1 (Config Reg). The WD\_CONFIG\_EN bit is reset to 0 automatically with the next SPI command.

### 4.7 Fail-safe mode

### 4.7.1 Temporary failures

The devices enter Fail-safe mode in case of:

- Watchdog failure
- V1 turn on failure
  - V1 short (V1 < V1<sub>fail</sub> for t >  $t_{V1short}$ )
- V1 failure (V1 < V<sub>RTxfalling</sub> for t > t<sub>V1FS</sub>)
- Thermal Shutdown TSD2

The Fail Safe functionality is also available in V1\_Standby mode. During V1\_Standby mode the Fail Safe mode is entered in the following cases:

- V1 failure (V1 < V<sub>RTxfalling</sub> for t > t<sub>V1FS</sub>)
- Watchdog failure (if watchdog still running due to I<sub>V1</sub> > I<sub>cmp fal</sub>)
- Thermal Shutdown TSD2

In Fail Safe mode the devices return to a fail safe state. The Fail Safe condition is indicated to the system in the Global Status Byte. The conditions during Fail Safe mode are:

- All outputs beside LS1 FSO and LS2 FSO are turned off
- All Control Registers are set to fail safe default values
- Write operations to Control Registers are blocked until the Fail Safe condition is cleared. The following bits are not WRITE protected:
  - TRIG (CR1<bit 0>, Config Register <bit 0>): watchdog trigger bit
  - V2\_x (CR1<bit 4:5>): Voltage Regulator V2 control
  - CR2 (bit <8:23>): Timer1 and Timer2 settings
  - OUT\_HS\_x (CR5 <bit 0:3>): OUT\_HS configuration
  - OUT15 x (CR6<bit 0:3>): OUT15 configuration
  - PWMx\_freq\_y (CR12): PWM frequency configuration
  - PWMx DC y (CR13 CR17): PWM duty cycle configuration
- LIN transmitter and SPI remain on (transmitters are deactivated in case of thermal shutdown TSD1 (TSD1 cluster 5 or 6 in cluster mode)
- Corresponding Failure Bits in Status Registers are set
- FS Bit (Global Status Byte) is set
- LS1 FSO and LS2 FSO will be turned on
- Charge pump is switched off

If the Fail Safe mode was entered it keeps active until the Fail safe condition is removed and the Fail Safe was read by SPI. Depending on the root cause of the Fail Safe operation, the actions to exit Fail safe mode are as shown in the following table.



Failure source	Failure condition	Diagnosis	Exit from Fail-safe mode
Microcontroller (oscillator)	Watchdog early write failure or expired window	FS (Global Status Byte) =1; WDFAIL (SR 1) =1; WDFAIL_CNT_x (SR 1) = n+1	TRIG (CR 1) = 1 during long open window Read&Clear SR1
V1	Short at turn-on	FS (Global Status Byte) =1; FORCED_SLEEP_TSD2/V1SC (SR 1) =1	Wake-up; Read&Clear <i>SR1</i>
	Undervoltage	FS (Global Status Byte) = 1; V1UV (SR 1) = 1; V1fail (SR 2) = 1 <sup>(1)</sup>	V1 >V <sub>RTrising</sub> ; Read&Clear <i>SR1</i>
Temperature	$T_j > T_{SD2}$	FS (Global Status Byte) = 1; TW (SR 2) = 1; TSD1 (SR 1) =1; TSD2 (SR 1) =1	T <sub>j</sub> < T <sub>SD2</sub> ; Read&Clear <i>SR1</i>

Table 46. Temporary failures description

### 4.7.2 Non-recoverable failures – forced Vbat standby mode

If the Fail-safe condition persists and all attempts to return to normal system operation fail, the devices enter the *Forced* Vbat\_standby mode in order to prevent damage to the system. The Forced Vbat\_standby mode can be terminated by any wake-up source. The root cause of the Forced Vbat\_standby mode is indicated in the SPI Status Registers.

In Forced Vbat\_standby mode, all Control Registers are set to power-on default values except:

CP\_DITH\_DIS (Config. Reg <bit 5>)

The Forced Vbat\_standby mode is entered in case of:

- Multiple watchdog failures: FORCED\_SLEEP\_WD (SR 1) = 1 (15 x watchdog failure)
- Multiple thermal shutdown 2: FORCED\_SLEEP\_TSD2/V1SC (SR 1) = 1 (7 x TSD2)
- V1 short at turn-on (V1 < V1<sub>fail</sub> for t > t<sub>V1short</sub>): FORCED\_SLEEP\_TSD2/V1SC (SR 1) = 1

Table 47. Non-recoverable failure

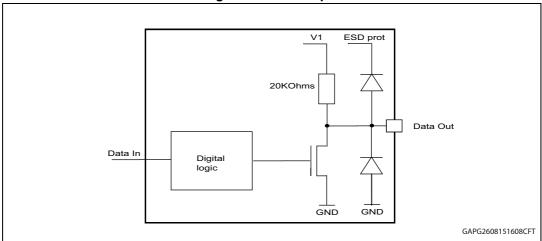
Failure source	Failure condition	Diagnosis	Exit from Fail-safe mode
Microcontroller (Oscillator)	15 consecutive Watchdog Failures	FS (Global Status Byte) = 1; WDFAIL (SR 1) = 1; FORCED_SLEEP_WD (SR 1) = 1	Wake-up; TRIG (CR 1) = 1 during long open window; Read&Clear SR1
V1	Short at turn-on	FS (Global Status Byte) = 1; FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up; Read&Clear SR1
Temperature	7 times TSD2	FS (Global Status Byte) =1; TW (SR 2) = 1; TSD1 (SR 1) = 1; TSD2 (SR 1) = 1; FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up; Read&Clear SR1



<sup>1.</sup> If V1 < V1<sub>fail</sub> (for t >  $t_{V1fail}$ ). The Fail-safe Bit is located in the Global Status Register.

## 4.8 Reset output (NReset)

Figure 28. NReset pin



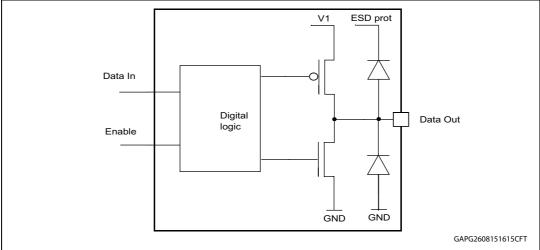
If V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output *NReset* is pulled up to V1 by an internal pull-up resistor after a reset delay time (t<sub>V1R</sub>). This is necessary for a defined start of the micro controller when the application is switched on. Since the *NReset* output is realized as an open drain output it is also possible to connect an external *NReset* open drain *NReset* source to the output. As soon as the NReset is released by the devices the watchdog starts with a long open window.

A reset pulse is generated in case of:

- V1 drops below V<sub>RTxfalling</sub> (configurable by SPI) for t > t<sub>UV1</sub>
- Watchdog failure
- Turn-on of the V1 regulator (V<sub>SREG</sub> Power-on or wake-up from Vbat\_standby mode)

### 4.9 LIN Bus Interface

Figure 29. RxDL pin



### 4.9.1 Features

- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- LIN Cell has been designed according to "Hardware requirements for transceivers (version 1.3)"
- Bitrate up to 20 kbit/s
- Dedicated LIN Flash mode with bitrate up to 100 kbit/s
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Micro controller Interface with CMOS-compatible I/O pins
- Internal pull-up resistor
- Receive-only mode
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Wake-up behaviour according to LIN2.2a and Hardware Requirements for LIN, CAN and Flexray Interfaces (version 1.3)

At  $V_{SREG} > V_{POR}$  (i.e.  $V_{SREG}$  power-on reset threshold), the LIN transceiver is enabled. The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal shutdown 1
- V<sub>SREG</sub> overvoltage/ undervoltage

The LIN receiver is not disabled in case of any failure condition.

The default bitrate of the transceiver allows communication up to 20 kbit/s. To enable fast flashing via the LIN bus, the transceiver can be operated in high speed mode by setting bit LIN HS EN (Config Reg) = 1. This feature is enabled automatically in LIN Flash mode.

### 4.9.2 Error handling

The devices LIN transceiver provides the following 3 error handling features.

### **Dominant TxDL time out**

If TXD\_L is in dominant state (low) for  $t > t_{dom(TXDL)}$  the transmitter will be disabled, the status bit LIN\_TXD\_DOM (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

The TxD dominant timeout detection can be disabled via SPI (LIN\_TXD\_TOUT\_EN = 0).

### **Permanent recessive**

If TXD\_L changes to dominant (low) state but RXD\_L signal does not follow within t <  $t_{LIN}$  the transmitter will be disabled, the status bit LIN\_PERM\_REC (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

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#### Permanent dominant

If the bus state is dominant (low) for t > tdom(bus) a bus permanent dominant failure will be detected. The status bit LIN PERM DOM (SR 2) will be set.

The transmitter will not be disabled.

#### 4.9.3 Wake up from Standby modes

In low power modes (V1 standby mode and Vbat standby mode) the devices can receive two types of wake up signals from the LIN bus (configurable by SPI bit LIN WU CONFIG (Config Reg)):

- Recessive-Dominant-recessive pattern with  $t > t_{dom\ LIN}$  (default, according to LIN 2.2a)
- State Change recessive-to-dominant or dominant-to-recessive (according to LIN 2.1)

#### Pattern Wake-up (default)

Figure 30. Wake-up behavior according to LIN 2.2a Voltage at LIN-Pin of LIN Physical Layer device LIN recessive 0.6 V<sub>Supply</sub> t <sub>dom LIN</sub>  $0.4 V_{\text{Supply}}$ LIN dominant sleep mode ' standby mode \* \* or similar mode naming GAPG0508151156CFT

#### Status change wake-up - Recessive-to-dominant

Normal wake-up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t > t<sub>LINBUS</sub>, will switch the devices to Active mode.

#### Status change wake-up - Dominant-to-recessive

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for  $t > t_{I \text{ INBUS}}$ , will switch the devices to Active mode.

#### 4.9.4 Receive-only mode

The LIN transmitter can be disabled in Active mode by setting the bit LIN\_REC\_ONLY (CR2). In this mode it is possible to listen to the bus but not sending to it.



### 4.10 Serial Peripheral Interface (ST SPI Standard)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output pins and one input pin is needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin reflects the global error flag (fault condition) of the device.

Chip Select Not (CSN)

The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started.

The state during CSN = 0 is called a communication frame.

If CSN = low for  $t > t_{CSNfail}$  the DO output is switched to high impedance in order not to block the signal line for other SPI nodes.

Serial Data In (DI)

The input Pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

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### 4.11 Power supply failure

### 4.11.1 V<sub>S</sub> supply failure

### V<sub>S</sub> overvoltage

If the supply voltages V<sub>S</sub> reaches the overvoltage threshold V<sub>SOV</sub>:

- · LIN remains enabled
- OUT1 to OUT\_14 are turned off (default).
   The shutdown of outputs may be disabled by SPI (VS\_OV\_SD\_EN (CR 3) = 0)
- Charge pump is disabled (and is switched on automatically in case the supply voltage recovers to normal operating voltage)
- H-bridge gate driver is switched into sink condition
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VS\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VS\_OV (SR 2).
  - VS\_LOCK\_EN (CR 3) = 0: outputs turned on automatically after V<sub>S</sub> overvoltage condition has recovered.
- The overvoltage bit VS\_OV (SR 2) is set and can be cleared with a 'Read&Clear' command. The overvoltage bit is reset automatically if VS\_LOCK\_EN (CR 3) = 0 and the overvoltage condition has recovered.

#### V<sub>S</sub> undervoltage

If the supply voltage  $V_S$  drops below the under voltage threshold voltage ( $V_{SUV}$ ):

- · LIN remains enabled
- OUT1 to OUT14 are turned off (default).
- The shutdown of outputs may be disabled by SPI (VS\_UV\_SD\_EN (CR 3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VS\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VS\_UV (SR 2).
  - VS\_LOCK\_EN (CR 3) = 0: outputs turned on automatically after V<sub>S</sub> undervoltage condition has recovered.
- The undervoltage bit VS\_UV (SR 2) is set and can be cleared with a 'Read&Clear' command. The undervoltage bit is removed automatically if VS\_LOCK\_EN (CR 3) = 0 and the undervoltage condition has recovered.



### 4.11.2 V<sub>SREG</sub> supply failure

#### **V<sub>SREG</sub>** overvoltage

If the supply voltages V<sub>SREG</sub> reaches the overvoltage threshold V<sub>SREG</sub> OV:

- · LIN is switched to high impedance
- OUT15 and OUT\_HS are turned off (default).
   The shutdown of outputs may be disabled by SPI (V<sub>SREG OV SD EN</sub> (CR 3) = 0)
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VSREG\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VSREG\_OV (SR 2).
  - VSREG\_LOCK\_EN (CR 3) = 0: outputs turned on automatically after V<sub>SREG</sub> overvoltage condition has recovered.
- The overvoltage bit VSREG\_OV (SR 2) is set and can be cleared with a 'Read&Clear' command. The overvoltage bit is reset automatically if VSREG\_LOCK\_EN (CR 3) = 0 and the overvoltage condition has recovered.

#### V<sub>SREG</sub> undervoltage

If the supply voltage V<sub>SREG</sub> drops below the under voltage threshold voltage (V<sub>SREG UV</sub>):

- LIN is switched to high impedance
- OUT15 and OUT\_HS are turned off (default).
- The shutdown of outputs may be disabled by SPI (VSREG\_UV\_SD\_EN (CR 3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VSREG\_LOCK\_EN (CR 3) = 1: outputs are off until Read&Clear VSREG\_UV (SR 2).
  - VSREG\_LOCK\_EN (CR 3) = 0: Outputs turned on automatically after V<sub>SREG</sub> undervoltage condition has recovered.
- The undervoltage bit VSREG\_UV (SR 2) is set and can be cleared with a 'Read&Clear' command. The undervoltage bit is removed automatically if VSREG\_LOCK\_EN (CR 3) = 0 and the undervoltage condition has recovered.

# 4.12 Temperature warning and thermal shutdown

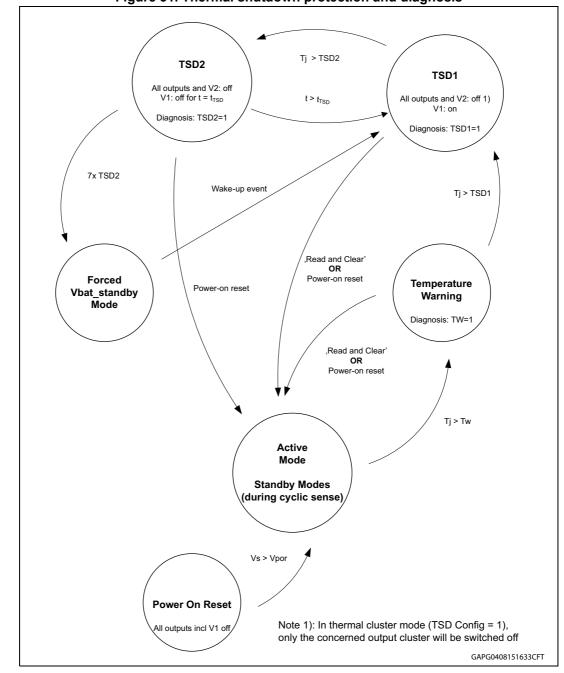


Figure 31. Thermal shutdown protection and diagnosis

Note:

The Thermal State machine will recover the same state as before entering Standby mode. In case of a TSD2 it will enter TSD1 state.

### 4.13 Power outputs OUT1..15 and OUT HS

The component provides a total of 4 half bridges outputs OUT1, OUT4-6 to drive motors and 10 stand alone high-side outputs OUT7..15 and OUT\_HS to drive e.g. LED's, bulbs or to supply contacts. All high-side outputs beside OUT\_HS and OUT15 are supplied by the pin VS and OUT\_HS and OUT15 are supplied by the buffered supply  $V_{SREG}$ . OUT\_HS is intended to be used as contact supply. Beside OUT15 and OUT\_HS the high-side switches can be activated only in case of running charge pump. OUT15 and OUT\_HS can be activated also in standby modes.

All high-side and low-side outputs switch off in case of:

- V<sub>S</sub> (V<sub>SREG</sub>) overvoltage and undervoltage (depending on configuration, see Section 4.11.2: V<sub>SREG</sub> supply failure)
- Overcurrent (depending on configuration, auto recovery mode (see below)
- Overtemperature (TSD1x/ cluster or single mode)
- Fail safe event
- Loss of GND at SGND pin

In case of overcurrent or overtemperature (TSD1\_CLx (SR 6)) condition, the drivers will switch off. The relevant status bit will be latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared. In case overvoltage/ undervoltage condition, the drivers will be switched off. The relevant status bit will be latched and can be read and optionally cleared by SPI. If VSREG\_LOCK\_EN (CR 3) respectively VS\_LOCK\_EN (CR 3) are set, the drivers remain off until the status is cleared. If the VS\_LOCK\_EN or VSREG\_LOCK\_EN) bit is set to 0, the drivers will switch on automatically if the error condition disappears. Undervoltage and overvoltage shutdown can be disabled by SPI. In case of open-load condition, the relevant status register will be latched. The status can be read and optionally cleared by SPI. The high and low-side outputs are not switched off in case of open-load condition.

For OUT1, OUT4-8 and OUT\_HS the auto recovery feature (OUTx\_OCR (CR 7)) can be enabled; half-bridges and high-side drivers have different Auto recovery frequencies (frecx\_hs and frecx\_hb). If these bits are set to 1 the driver will automatically restart from an overload condition. This overload recovery feature is intended for loads which have an initial current higher than the overcurrent limit of the output (e.g. Inrush current of cold light bulbs). The SPI bits OUTx\_OCR\_ALERT (SR4) indicate that the output reached auto-recovery condition.

Note:

The maximum voltage and current applied to the high-side Outputs is specified in the 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions. In case of outputs switch off due to loss of ground at SGND pin, the device has to be re-started through a power off on both  $V_S$  and  $V_{SREG}$ 

Each of the stand alone high-side driver outputs OUT7 ... OUT15 and OUT\_HS can be driven with an internally generated PWM signal, an internal Timer or with DIR1 respectively DIR2. See *Table 48*.

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OUTx\_3 OUTx\_2 OUTx 1 OUTx 0 Description **OFF** ON Timer1 output is controlled by timer1; starting with ON phase after timer restart Timer2 output is controlled by timer2; starting with ON phase after timer restart PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8 PWM9 PWM10 DIR1 DIR2 

Table 48. Power output settings

### 4.14 Auto-recovery alert and thermal expiration

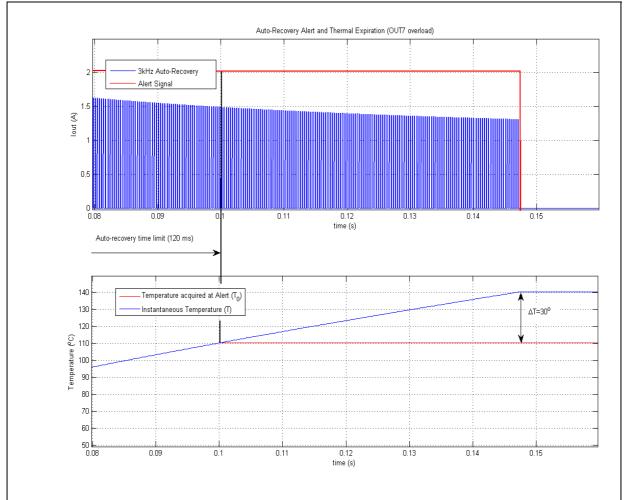
The thermal expiration feature provides a robust protection against possible microcontroller malfunction, switching off a given channel if continuously driven in auto-recovery. If the temperature of the related cluster increases by more than 30  $^{\circ}$ C after reaching the auto-recovery time  $t_{AR}$ , the channel is switched off. The thermal expiration status bit OUTx\_TH\_EX (SR 3) is set.

During auto-recovery condition, OUTx\_OCR\_ALERT (SR 4) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

The thermal expiration feature is controlled by SPI (OUTx\_OCR\_THX\_EN (CR 8).



Figure 32. Example of long auto-recovery on OUT7. Temperature acquisition starts after  $t_{AR}$ , thermal expiration occurs after a  $\Delta T = 30^{\circ}$ 



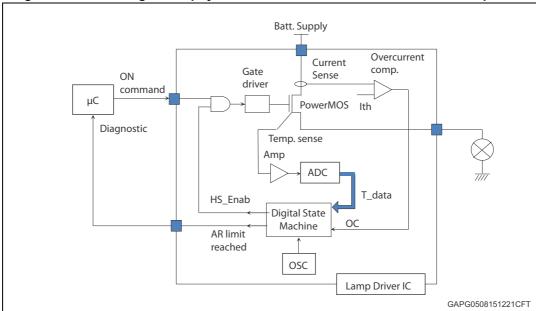


Figure 33. Block diagram of physical realization of AR alert and thermal expiration

### 4.15 Charge pump

The charge pump uses two external capacitors, which are switched with  $f_{CP}$ . The output of the charge pump has a current limitation. In standby mode and after a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than  $T_{CP}$ , the power-MOS outputs and the EC-control are switched off. The H-bridge MOSFET gate drivers are switched to resistive low and CP\_LOW (SR 2) is set. This bit has to be cleared to reactivate the drivers. If the bit CP\_LOW\_CONFIG (Configuration Register 0x3F) is set to '1', CP\_LOW (SR2) behaves as a 'live' bit and the outputs are re-activated automatically upon recovery of the charge pump output voltage.

In case of reaching the overvoltage shutdown threshold  $V_{SOV}$  the charge pump is disabled and automatically restarted after  $V_{S}$  recovered to normal operating voltage.

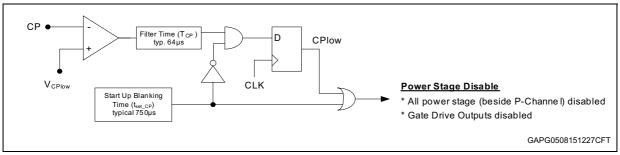


Figure 34. Charge pump low filtering and start up implementation

### 4.16 Inductive loads

Each of the half bridges is built by internally connected high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can



be driven at the outputs OUT1 and OUT4-6 without external freewheeling diodes. The high-side drivers OUT7 to OUT15 and OUT\_HS are intended to drive resistive loads only. Therefore only a limited energy (E < 1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 100  $\mu$ H) an external freewheeling diode connected between GND and the corresponding output is required.

### 4.17 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for  $t > t_{OL\_OUT}$  the corresponding open-load bit OUTx\_OL (SR 5) is set in the status register.

#### 4.18 Overcurrent detection

An overcurrent condition is detected after a filter time (see *Figure 11* and *Figure 12*) and is indicated by the status bit OUTx\_OC (SR 3). In case of overcurrent, the corresponding driver switches off to reduce the power dissipation and to protect the integrated circuit. If the outputs are not configured in recovery mode, the microcontroller has to clear the relevant status bits to reactivate the corresponding drivers.

#### 4.19 Current monitor

The current monitor sources a current image of the power stage output current at the current monitor pin CM, which has a fixed ratio ( $I_{CMr}$ ) of the instantaneous current of the selected high-side driver. The signal at output CM is blanked for  $t_{cmb}$  after switching on the driver until the correct settlement of the circuitry. The bits CM\_SELx (CR 7) define which of the outputs is multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-load or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). The current monitor output is enabled after the current-monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high impedance mode. The current monitor can be deactivated by CM\_EN (CR 7).

### 4.20 PWM mode of the power outputs

Description see Section 7.3: Status register overview.

### 4.21 Cross-current protection

The four half-bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half-bridge will be automatically delayed by the crosscurrent protection time. After the crosscurrent protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.



# 4.22 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors) can be driven by using the programmable soft-start function (i.e. overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit OUTx\_OCR (CR 7). If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition.

The PWM frequency is defined by setting OCR\_FREQ (CR7).

The device itself cannot distinguish between a real overload (e.g. short-circuit condition) and a load characterized by operation currents exceeding the short-circuit threshold.

Examples are non-linear loads like a light bulb used on the HS outputs or a motor used on the half bridge output with inrush and stall currents that shall be limited by the auto recovery feature.

For the bulb, a real overload condition can only be qualified by time. For overload detection the microcontroller can switch on the light bulbs by setting the overcurrent recovery bit for the first e.g. 50 ms. After clearing the recovery bit, the output will be switched off automatically if the overload condition remains.

For the half bridges the high current can be present during all motor activation and another SW strategy must be applied to identify a SC to GND or Supply. Before running the motor e.g. with a first SPI command all bridges LS are switched on (without auto recovery functionality / cleared overcurrent recovery bit), all HS are switched off and a SC to Battery can be diagnosed. With a next SPI command, all HS are switched on (without auto recovery functionality/ cleared overcurrent recovery bit) and all LS are switched off. In this sequence, a short to GND can be diagnosed. If in both sequences no overload condition is identified, the motor can be run by switching on the relevant HS and LS each configured in auto recovery mode (see *Figure 35*). Such sequence can be applied before any motor activation to identify SC just before operating the motor (in case the delay due to the 2 additional SPI commands is not limiting the application) or in case of power up of the system resp. applied on a certain time base.



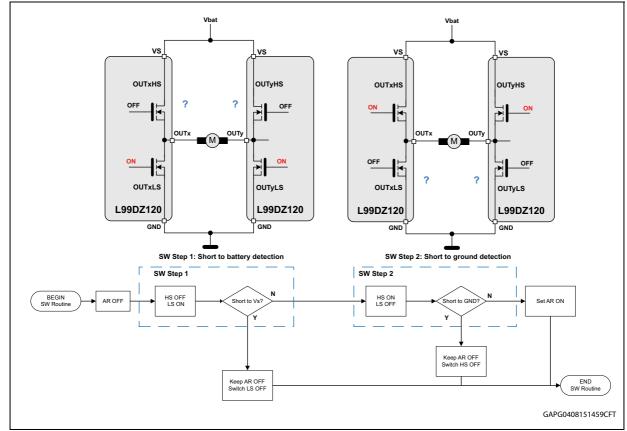


Figure 35. Software strategy for half bridges before applying auto-recovery mode

As soon as an output reaches auto-recovery condition, OUTx\_OCR\_ALERT (SR 4)) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

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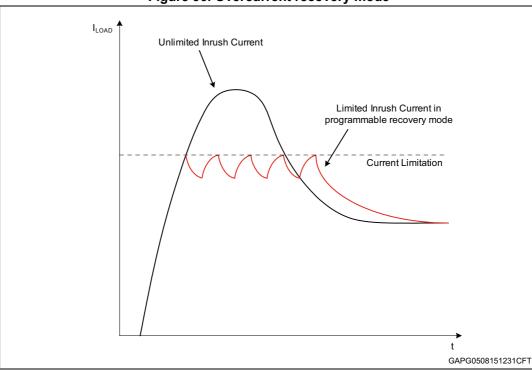


Figure 36. Overcurrent recovery mode

### 4.23 H-bridge control

The PWMH and DIRH inputs control the drivers of the external H-bridge transistors. In single Motor mode the motor direction can be chosen with the direction input (DIRH), the duty cycle<sup>(a)</sup> and frequency with the PWMH input (single mode). With the SPI bits SD (CR 10) and SDS (CR 10) four different slow-decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors. Unconnected inputs are defined by internal pull-down current.

a. If tccp is programmed to 4  $\mu s$  and frequency to 50 kHz, max duty cycle achievable is 92%.



DocID029145 Rev 4

	Con pir		Cor	itrol	bits		Fail	ure l	bits		C	utpu	ıt pin	s			
Nb	DIRH	<b>PWMH</b>	HEN	as	SOS	CP_LOW	<b>^0_S</b> ^	\n^s\	Sa	TSD1	GH1	GL1	СН2	GL2	Motor config	Comment	
1	х	Х	0	х	Х	х	х	х	Х	Х	RL	RL	RL	RL		H-bridge disabled	
2	Х	Х	1	Х	Х	1	0	0	0	0	RL	RL	RL	RL		Charge pump voltage too low	
3	Х	Х	1	Х	Х	0	Х	Х	Х	1	RL	RL	RL	RL		Thermal shutdown	
4	Х	Х	1	Х	Х	0	1	0	0	0	L	L	L	L		Overvoltage	
5	Х	Х	1	Х	Х	0	0	0	1	0	L <sup>(1)</sup>	L <sup>(1)</sup>	L <sup>(1)</sup>	L <sup>(1)</sup>		Short-circuit <sup>(1)</sup>	
6	0	1	1	Х	Х	0	0	0	0	0	L	Η	Н	L		Bridge H2/L1 on	
7	x	0	1	0	0	0	0	0	0	0	L	I	L	Н	Single	Slow-decay mode LS1 and LS2 on	
8	0	0	1	0	1	0	0	0	0	0	L	Ι	Ш	L	Olligic	Slow-decay mode LS1 on	
9	1	0	1	0	1	0	0	0	0	0	L	Ш	Ш	Н		Slow-decay mode LS2 on	
10	1	1	1	х	Х	0	0	0	0	0	Н	Ш	L	Н		Bridge H1/L2 on	
11	х	0	1	1	0	0	0	0	0	0	Н	L	Н	L		Slow-decay mode HS1 and HS2 on	
12	0	0	1	1	1	0	0	0	0	0	L	L	Н	L		Slow-decay mode HS1 on	
13	1	0	1	1	1	0	0	0	0	0	Н	L	L	L		Slow-decay mode HS2 on	

Table 49. H-bridge control truth table

During watchdog long-open window, the H-bridge drivers are forced off until the first valid watchdog trigger in window mode (setting TRIG = 0 during safe window). The Control Registers remain accessible during long open window.

### 4.24 H-bridge driver slew-rate control

The rising and falling slope of the drivers for the external high-side Power-MOS can be slew rate controlled. If this mode is enabled the gate of the external high-side Power-MOS is driven by a current source instead of a low-impedance output driver switch as long as the drain-source voltage over this Power-MOS is below the switch threshold. The current is programmed using the bits SLEW\_x<4:0> (CR 10), which represent a binary number. This number is multiplied by the minimum current step. This minimum current step is the maximum source-/sink-current ( $I_{GHxrmax}$  /  $I_{GHxfmax}$ ) divided by 31. Programming SLEW\_x <4:0> to 0 disables the slew rate control and the output is driven by the low-impedance output driver switch.



<sup>1.</sup> Only the H-bridge leg (low-side and high-side), in which one MOSFET is in short-circuit condition is switched off. Both MOSFETs of the other H-bridge leg remain active and driven by DIRH and PWMH.

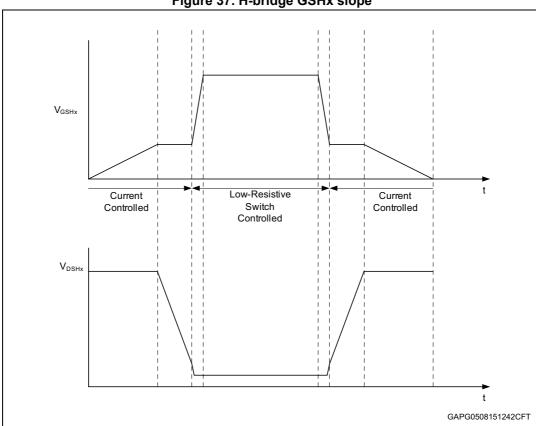


Figure 37. H-bridge GSHx slope

#### 4.25 Resistive low

The resistive output mode protects the devices and the H-bridge in the standby mode and in some failure modes (thermal shutdown TSD1 (SR 1), charge pump low CP\_LOW (SR 2) and DI pin stuck at '1' SPI\_INV\_CMD (SR 2)). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is switched into sink condition for 32  $\mu$ s to 64  $\mu$ s to ensure a fast switch-off of the H-bridge transistor. If slew rate control is enabled, the sink condition is slew-rate controlled. Afterwards the driver is switched into the resistive output mode (resistive path to source).

### 4.26 Short circuit detection / drain source monitoring

The Drain - Source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage-drop over the external MOSFET exceeds the configurable threshold voltage  $V_{SCd\_HB}$  (DIAG\_x (CR 10) for longer  $t > t_{SCd\_HB}$  the corresponding gate driver switches off the external MOSFET and the corresponding drain source monitoring flag DS\_MON\_x (SR 2) is set. The DSMON\_x bits have to be cleared through the SPI to reactivate the gate drivers. This monitoring is only active while the corresponding gate driver is activated. If a drain-source monitor event is detected, the corresponding gate-driver remains activated for at maximum the filter time. When the gate driver switches on, the drain-source comparator requires the specified settling time until the drain-source monitoring is valid. During this time, this drain-source



monitor event may start the filter time. The threshold voltage  $V_{SCd\_HB}$  can be programmed using the SPI bits DIAG\_x (CR 10).

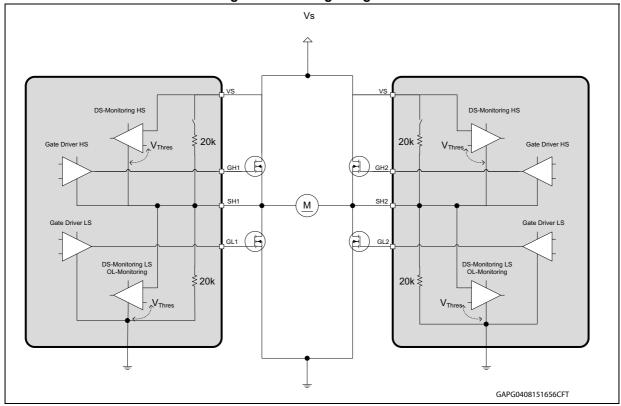


Figure 38. H-bridge diagnosis

# 4.27 H-bridge monitoring in off-mode

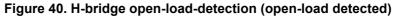
The drain source voltages of the H-bridge driver external transistors can be monitored, while the transistors are switched off. If either bit OL\_H1L2 (CR 10) or OL\_H2L1 (CR 10) is set to 1, while bit HEN (CR 1) = 1, the H-drivers enter resistive low mode and the drain-source voltages can be monitored. Since the pull-up resistance is equal to the pull-down resistance on both sides of the bridge a voltage of 2/3  $V_S$  on the pull-up highside and 1/3  $V_S$  on the low-side is expected, if they drive a low-resistive inductive load (e.g. motor). If the drain source voltage on each of these Power-MOS is less than 1/6  $V_S$ , the drain-source monitor bit of the associated driver is set.

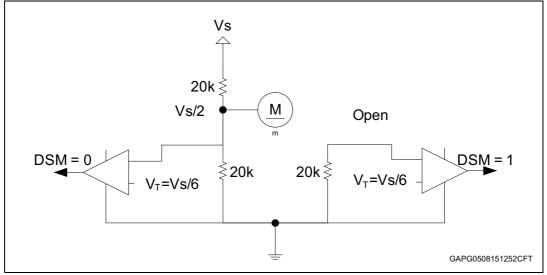
The open-load filter time is t<sub>OL HB</sub>.

577

20k | Vs/3 | Vs/3 | Vs/3 | Vs/3 | Vs/6 | VT=Vs/6 | VT=Vs

Figure 39. H-bridge open-load-detection (no open-load detected)





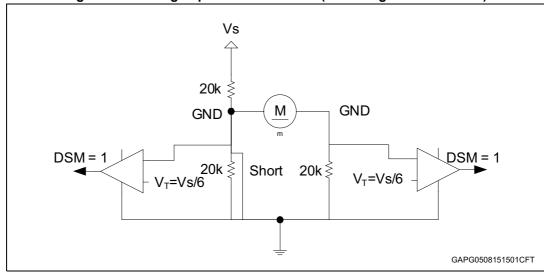


Figure 41. H-bridge open-load-detection (short to ground detected)

Figure 42. H-bridge open-load detection (short to V<sub>S</sub> detected)

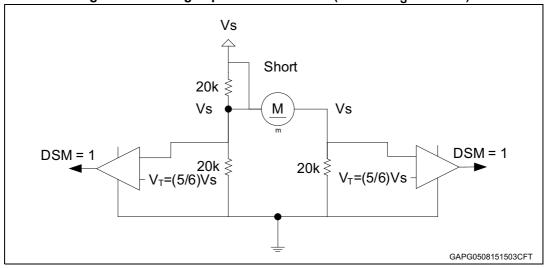


Table 50. H-bridge monitoring in off-mode

		Control b	its	Failur	e bits	Comments
Nb	OL H1L2	OL H2L1	H OLTH High	DSMON LS1	DSMON LS2	
1	0	0	0	0	0	Drain-Source monitor disabled
2	1	0	х	0	0	No open-load detected
3	1	0	0	0	1	Open-load SH2
4	1	0	0	1	1	Short to GND
5	1	0	1	1	1	Short to VS
6	0	1	х	0	0	No open-load detected
7	0	1	0	1	0	Open-load SH1

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	iable community in our mode (community)											
		Control b	its	Failur	e bits	Comments						
Nb	OL H1L2	OL H2L1	H OLTH High	DSMON LS1	DSMON LS2							
8	0	1	0	1	1	Short to GND						
9	0	1	1	1	1	Short to VS						

Table 50. H-bridge monitoring in off-mode (continued)

### 4.28 Programmable cross current protection

The external PowerMOSFETs transistors in H-bridge (two half-bridges) configuration are switched on with an additional delay time  $t_{CCP}$  to prevent cross current in the halfbridge. The cross current protection time  $t_{CCP}$  can be programmed with the SPI bits COPT\_x<3:0> (CR 10). The timer is started when the gate driver is switched on in the device.

The PWMH module has 2 timers to configure locking time for high-side and freewheeling low-side. The programmable time  $t_{\text{CCP-TIM1}}$  /  $t_{\text{CCP-TIM2}}$  is the same. Sequence for switching in PWM mode is the following:

- HS switch off after locking t<sub>CCP-TIM1</sub>
- LS switch on after 2nd locking t<sub>CCP-TIM1</sub>
- HS switch on after locking t<sub>CCP-TIM2</sub> which starts with rising edge on PWM input

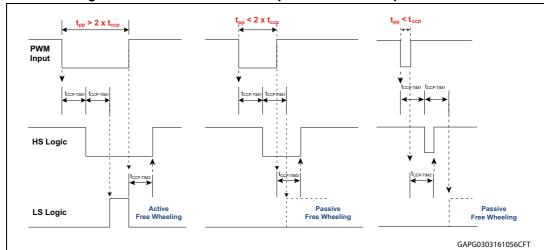


Figure 43. PWMH cross current protection time implementation

### 4.29 Power window H-bridge safety switch off block

The two LS Switches LS1\_FSO and LS2\_FSO are intended to be used to switch off the gates of the external high-side MOSFETs in the power window h-bridge if a fatal error happens. This block must work also in case the MOSFET driver and the according control blocks on the chip are destroyed. Therefore it is necessary to have a complete separated safety block on the device, which has it's own supply and GND connection, separated from the other supplies and GNDs. In the block is implemented an own voltage regulator and oscillator.



The safety block is surrounded by a GND isolation ring realized by deep trench isolation. The LS driver must work down to a lower voltage than the other circuits. The block has its own internal supply and an own oscillator for monitoring the failure signals (WWD, V1 fail, SPI fail & Tj) which are Manchester encoded and decoupled by high ohmic resistances. In case of fail-safe event, both LS switches LS1\_FSO and LS2\_FSO are switched on.

In case of entering V1 standby mode or Vbat standby mode both fail safe low-side switches are switched on to minimize the current drawn by the fail safe block (e.g. oscillator is switched off and Manchester Encoding is deactivated). Short circuit protection to V<sub>S</sub> is active in both standby modes limiting the current to I<sub>OLimit</sub> for a filter of t<sub>SCF</sub>.

After this filter time the fail-safe switches are switched off and LSxFSO OC (SR 3) is set. To reactivate the low-side functionality this bit has to be set back by a read and clear command. In case of V<sub>S</sub> loss the fail safe switches are biased by their own output voltage to turn on the low-side switches down to VOUT max.

To allow verification of the Fail-Safe path, the low-side switches LS1 FSO and LS2 FSO can be turned on by SPI (Configuration Register 0x3F bit 4: FS FORCED)

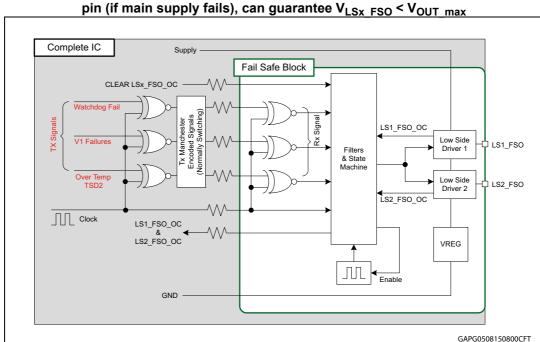


Figure 44. LSx\_FSO: low-side driver "passively" turned on, taking supply from output pin (if main supply fails), can guarantee  $V_{LSx FSO} < V_{OUT max}$ 



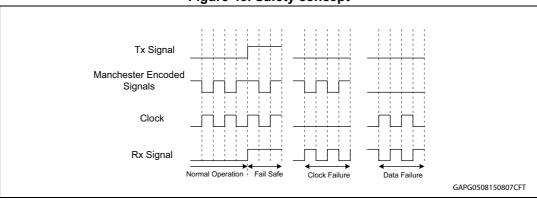


Figure 45. Safety concept

### 4.30 Temperature warning and shutdown

If any of the cluster (see Section 4.31: Thermal clusters) junction temperatures rises above the temperature warning threshold TW, the temperature warning flag TW (SR 2) is set after the temperature warning filter time  $t_{jtft}$  and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold (TSD1), the thermal shutdown bit TSD1 (SR 1) is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The gates of the H-bridge is discharged by the 'Resistive Low' mode. After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after  $t_{jtft}$ . Once this bit is set and the temperature is above the temperature shutdown threshold, temperature shutdown is detected after  $t_{jtft}$  and the outputs are switched off. Therefore the minimum time after which the outputs are switched off after the bits have been cleared in case the temperature is still above the thermal shutdown threshold is twice the thermal warning/ thermal shutdown filter time  $t_{itft}$ .

#### 4.31 Thermal clusters

In order to provide an advanced on-chip temperature control, the power outputs are grouped in six clusters with dedicated thermal sensors. The sensors are suitably located on the device (see *Figure 46: Thermal clusters identification*). In case the temperature of an output cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shut down (all other outputs remain active). Each output cluster has a dedicated temperature warning and shutdown flag (SR 6) and the cluster temperature can be read out by SPI.

Hence, the thermal cluster concept allows to identify a group of outputs in which one or more channels are in overload condition.

If thermal shutdown has occurred within an output cluster, or if temperature is rising within a cluster, it may be desired to identify which of the output (s) is (are) determining the temperature increase. An additional evaluation, based on current monitoring and cluster temperature read-out, supports identification of the outputs mainly contributing to the temperature increase. The cluster temperatures are available in SR 7, SR 8 and SR 9 and can be calculated from the binary coded register value using the following formula:

Decimal code = (350 - Temp) / 0.488



Example:

 $T = -40 \,^{\circ}C \Rightarrow$  decimal code is 799 (0x31F)

 $T = 25 \,^{\circ}C \Rightarrow$  decimal code is 666 (0x29A)

Thermal clusters can be configured using bit TSD\_CONFIG (Config Reg):

- Standard mode (default): as soon as any cluster reaches thermal threshold the device is switched off. V1 regulator remains on and is switched off reaching TSD2.
- Cluster mode: only the cluster which reached shutdown temperature is switched off.

If Cluster Th\_CL6 (global) or Cluster Th\_CL5 (Voltage Regulators) reachTSD1, the whole device is OFF (beside V1).

Note:

Clusters related to power outputs (clusters 1 to 4, see Figure 46: Thermal clusters identification) will be managed digitally only, by mean of the ADC conversion of related thermal sensors, while clusters 5 and 6 will be managed in an analog way (comparators) since ADC can be off, e.g. in V1\_standby mode. Temperature reading provided by ADC may differ from real junction temperature of a specific output due to spatial placement of thermal sensor. Such an effect is more visible during fast thermal increases of junction temperature.

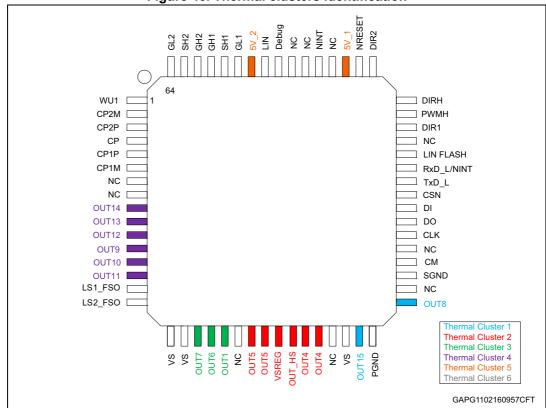


Figure 46. Thermal clusters identification

5

Th_CL1	Th_CL2	Th_CL3	Th_CL4	Th_CL5	Th_CL6
5 W Driver + OUT15	Door lock + OUT_HS	OUT1 + OUT6	10W driver high ohmic channels	VREG 1 VREG 2	Global
	TW & TSD1 Both digitally managed	TW & TSD1 Both digitally managed		TW digitally managed TSD1 & TSD2 Both analog managed	TW digitally managed TSD1 Analog managed

Table 51. Thermal cluster definition

### 4.32 V<sub>S</sub> compensation (duty cycle adjustment) module

All stand-alone HS outputs can be programmed to calculate some internal duty cycle adjustment to adapt the duty cycle to a changing supply voltage at  $V_S$ . This feature is aimed to avoid LED brightness flickering in case of alternating supply voltage. The correction of the duty cycle is based on the following formula:

#### **Equation 1: Duty cycle correction**

$$DutyCycle = \frac{V_{th} - V_{LED}}{V_{Bat} - V_{LED}} \times DC_{nom}$$

V<sub>th</sub> = Duty cycle reference voltage: defined as 10 V

V<sub>Bat</sub> = Reference voltage: defined as voltage at pin VS

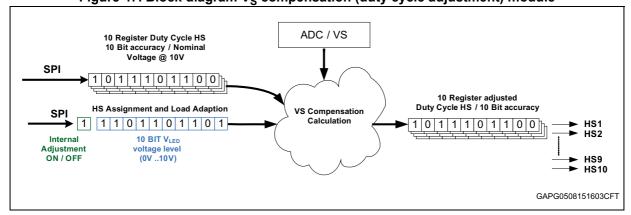
 $V_{LED}$  = Voltage drop on the external LED

DC<sub>nom</sub> = Nominal Duty Cycle programmed by SPI< PWMx DCx>

To be compatible to different LED load characteristics the value for  $V_{LED}$  can be programmed for each output by a dedicated control register OUT7\_VLED ... OUT\_HS\_VLED (CR 18 to CR 22). Auto compensation features can be activated for all HS outputs each by setting OUTx\_AUTOCOMP\_EN (CR 18 to CR 22).

The programmed LED voltage (OUTx\_V\_LED (CR18 to CR22)) must be lower than  $V_{th}$  (10 V).

Figure 47. Block diagram V<sub>S</sub> compensation (duty cycle adjustment) module





### 4.33 Analog digital converter

Voltage signals  $V_S$ ,  $V_{SREG}$ ,  $V_{WU}$  and TH\_CL1..6 are read out sequentially. The voltage signals are multiplexed to an ADC. The ADC is realized as a 10 Bit SAR, that is sampled with the main clock  $f_{clk2}$  /  $f_{ADC}$ .

Each channel will be converted with a conversion time tcon, therefore an update of the ADC value is available every  $t_{con}$  \* 9. In case of WU is directly connected to Clamp 30, the input must be protected by a series resistance of typical  $1k\Omega$  to sustain reverse battery condition.

Vin WU 1000k 3.3V VSREG 100k 10pF 9 Channel Mux THCL2 THCL4 THCL5 THCL6 VREF = 2V SPI Register 10 Bit SAR GAPG0408151647CFT

Figure 48. Sequential ADC Read Out for  $V_{SREG}$ ,  $V_{S}$ , WU and THCL1 ..THCL6

### 5 Serial Peripheral Interface (SPI)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK. This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output Pins and one input Pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin will reflect the global error flag (fault condition) of the device.

Chip Select Not (CSN)

The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame. If CSN = low for t >  $t_{CSNfail}$  the DO output will be switched to high impedance in order to not block the signal line for other SPI nodes.

Serial Data In (DI)

The input Pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note:

Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

#### 5.1 ST SPI 4.0

The ST-SPI is a standard used in ST Automotive ASSP devices.



This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, failsafe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The devices Serial Peripheral Interface are compliant to the ST SPI Standard Rev. 4.0.

### 5.1.1 Physical layer

CSN
SCK
SDI
SDO

L99DZ120

GAPG1102161003CFT

Figure 49. SPI pin description

### 5.2 Signal description

Chip Select Not (CSN)

The communication interface is de-selected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected.

Serial Clock (SCK)

This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).

Serial Data Input (SDI)

This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).

Serial Data Output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).



Data In

Digital logic

Data Out

GAPG2608151615CFT

Figure 50. SDO pin

#### 5.2.1 Clock and Data Characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in the following mode:

CPOL = 0

CPHA = 0

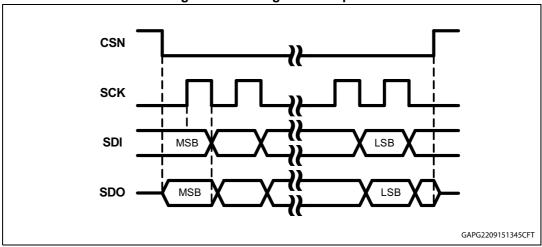


Figure 51. SPI signal description

The communication frame starts with the falling edge of the CSN (Communication Start). SCK has to be low.

The SDI data is then latched at all following rising SCK edges into the internal shift registers. After Communication Start the SDO will leave 3-state mode and present the MSB of the data shifted out to SDO. At all following falling SCK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place (e.g. correct number of SCK cycles, access to a valid address), the requested operation according to the Operating Code will be performed (Write or Clear operation).

#### 5.2.2 Communication protocol

#### **SDI Frame**

The devices Data-In Frame consist of 32-bit (OpCode (2 bits) + Address (6 bits) + Data Byte 3 + Data Byte 2 + Data Byte 1). The first two transmitted bits (MSB, MSB-1) contain the Operation Code which represents the instruction which will be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation will be performed. The subsequent bytes contain the payload.

OPCODE **ADDRESS** DATA Byte 3 OC021 OC1 Α5 A3 A2 A0 23 22 20 19 18 17 16 MSB DATA Byte 2 14 13 12 11 15 9 **DATA Byte 1** 6 5 4 3 2 0 LSB time GAPG2209151357CFT

Figure 52. SDI Frame

#### **Operating code**

The operating code is used to distinguish between different access modes to the registers of the slave device.

OC1	OC0	Description
0	0	Write Operation
0	1	Read Operation
1	0	Read & Clear Operation
1	1	Read Device Information

Table 52. Operation codes

A Write Operation will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data). Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

A Read Operation shifts out the data present in the addressed register at Communication Start. The payload data will be ignored and internal data will not be modified. In addition a Burst Read can be performed.



A Read & Clear Operation will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to '1'. Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

Note:

Status registers which change status during communication could be cleared by the actual Read & Clear Operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status it is recommended just clear status registers which are already reported in the previous communication (Selective Bitwise Clear).

#### **Advanced operation codes**

To provide the separate write of all control registers and the bitwise clear of all status registers, two Advanced Operation Codes can be used to set all control registers to the default value and to clear all status registers. A 'set all control registers to default' command is performed when an OpCode '11' at address b'111111 is performed.

Note:

Please consider that potential device specific write protected registers cannot be cleared with this command in therefore a device Power-on-Reset is needed.

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

#### Data-in payload

The Payload (Data Byte 1 to Data Byte 3) is the data transferred to the devices with every SPI communication. The Payload always follows the OpCode and the Address bits. For Write access the Payload represents the new data written to the addressed register. For Read & Clear operations the Payload defines which bits of the adressed Status Register will be cleared. In case of a '1' at the corresponding bit position the bit will be cleared.

For a Read Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to '0'.

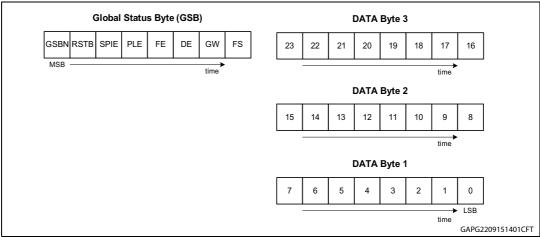
#### **SDO frame**

The data-out frame consists of 32-bit (GSB + Data Byte 1 to 3).

The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the Communication Start. These 8-bit are transmitted at every SPI transaction. The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge. This could lead to an inconsistency in data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after.



Figure 53. SDO frame



#### Global Status Byte (GSB)

The bits (Bit0 to Bit4) represent a logical OR combination of bits located in the Status Registers. Therefore no direct Read & Clear can be performed on these bits inside the GSB.

Table 53. Global Status Byte

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS

#### **Global Status Bit Not (GSBN)**

The GSBN is a logical NOR combination of Bit 24 to Bit 30. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.

#### Reset Bit (RSTB)

The RSTB indicates a device reset. In case this bit is set, specific internal Control Registers are set to default and kept in that state until the bit is cleared. The RSTB bit is cleared after a Read & Clear of all the specific bits in the Status Registers which caused the reset event.

#### SPI Error (SPIE)

The SPIE is a logical OR combination of errors related to a wrong SPI communication.

#### **Physical Layer Error (PLE)**

The PLE is a logical OR combination of errors related to the LIN transceiver.

#### **Functional Error (FE)**

The FE is a logical OR combination of errors coming from functional blocks (e.g. high-side overcurrent).

#### **Device Error (DE)**

The DE is a logical OR combination of errors related to device specific blocks (e.g. VS overvoltage, overtemperature



#### **Global Warning (GW)**

The GW is a logical OR combination of warning flags (e.g. thermal warning).

#### Fail Safe (FS)

The FS bit indicates that the device was forced into a safe state due to mistreatment or fundamental internal errors (e.g. Watchdog failure, Voltage regulator failure).

#### **Data-Out Payload**

The Payload (Data Bytes 1 to 3) is the data transferred from the slave device with every SPI communication to the master device. The Payload always follows the OpCode and the address bits of the actual shifted in data (In-frame-Response).

#### 5.2.3 Address definition

Table 54. Device application access

Operating Code								
OC1	OC0							
0	0							
0	1							
1	0							

Table 55. Device information read access

Operating Code								
OC1	OC0							
1	1							

Table 56. RAM address range

RAM Address	Description	Access		
3FH	Configuration Register	R/W		
3CH	Status Register 12	R/C		
32H	Status Register 2	R/C		
31H	Status Register 1	R/C		
22H	Control Register 34	R/W		
1DH	Control Register 29	R/W		
02H	Control Register 2	R/W		

Table 56. RAM address range (continued)

RAM Address	Description	Access
01H	Control Register 1	R/W
00H	reserved	

Table 57. ROM address range

ROM Address	Description	Access
3FH	<advanced op.=""></advanced>	W
3EH	<gsb options=""></gsb>	R
20H	<spi cpha="" test=""></spi>	R
16H	<wd 4="" bit="" pos.=""></wd>	R
15H	<wd 3="" bit="" pos.=""></wd>	R
14H	<wd 2="" bit="" pos.=""></wd>	R
13H	<wd 1="" bit="" pos.=""></wd>	R
12H	<wd 2="" type=""></wd>	R
11H	<wd 1="" type=""></wd>	R
10H	<spi mode=""></spi>	R
0AH	<silicon ver.=""></silicon>	R
06H	<device no.5=""></device>	R
05H	<device no.4=""></device>	R
04H	<device no.3=""></device>	R
03H	<device no.2=""></device>	R
02H	<device no.1=""></device>	R
01H	<device family=""></device>	R
00H	<company code=""></company>	R

### Information registers

The *Device Information Registers* can be read by using OpCode '11'. After shifting out the GSB the 8-bit wide payload will be transmitted. By reading *Device Information Registers* a communication width which is minimum 16-bit plus a multiple by 8 can be used. After shifting out the GSB followed by the 8-bit wide payload a series of '0' is shifted out at the SDO.



**Table 58. Information Registers Map** 

	Tubio dei illioniation regiotore illap										
ROM Adress	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<advanced op.=""></advanced>										
3EH	<gsb options=""></gsb>	R	$\rightarrow$	0	0	0	0	0	0	0	0
20H	<spi cpha="" test=""></spi>	R	$\rightarrow$	0	1	0	1	0	1	0	1
16H	<wd 4="" bit="" pos.=""></wd>	R	$\rightarrow$				C	OH			
15H	<wd 3="" bit="" pos.=""></wd>	R	$\rightarrow$				7F	-H			
14H	<wd 2="" bit="" pos.=""></wd>	R	$\rightarrow$				C	ЭH			
13H	<wd 1="" bit="" pos.=""></wd>	R	$\rightarrow$				41	ΙΗ			
12H	<wd 2="" type=""></wd>	R	$\rightarrow$	91H							
11H	<wd 1="" type=""></wd>	R	$\rightarrow$				28	ЗН			
10H	<spi mode=""></spi>	R	$\rightarrow$				В	DΗ			
			$\rightarrow$								
0AH	<silicon ver.=""></silicon>	R	$\rightarrow$		major r	evision			minor r	evision	
			$\rightarrow$								
06H	<device no.5=""></device>	R				l	_99DZ1	20: 01H	1		
05H	<device no.4=""></device>	R	$\rightarrow$				06	SH			
04H	<device no.3=""></device>	R	$\rightarrow$	4DH							
03H	<device no.2=""></device>	R	$\rightarrow$	41H							
02H	<device no.1=""></device>	R	$\rightarrow$	55H							
01H	<device family=""></device>	R	$\rightarrow$				01	ΙΗ			
00H	<company code=""></company>	R	$\rightarrow$				00	Ή			

### **Device Identification Registers**

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD Power Management)

<Device No. 1>: 55H

<Device No. 2>: 41H

<Device No. 3>: 4DH

<Device No. 4>: 06H

<Device No. 5>: for L99DZ120: 01H

#### **SPI** modes

By reading out the <SPI mode> register general information of SPI usage of the *Device Application Registers* can be read.



Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	DL2	DL1	DL0	0	0	S1	S0
1	0	1	1	0	0	0	0

<SPI mode>: B0H (Burst mode read available, 32-bit, no data consistency check)

#### **SPI Burst Read**

Table 60. Burst Read Bit

Bit 7	Description
0	BR not available
1	BR available

The SPI Burst Read bit indicates if a burst read operation is implemented. The intention of a Burst Read is e.g. used to perform a device internal memory dump to the SPI Master.

The start of the Burst Read is like a normal Read Operation. The difference is, that after the SPI Data Length the CSN is not pulled high and the SCK will be continuously clocked. When the normal SCK max count is reached (SPI Data Length) the consecutive addressed data will be latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatic incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached. The SPI Burst Read is limited by the CSN low timeout.

#### **SPI Data Length**

The SPI Data Length value indicates the length of the SCK count monitor which is running for all accesses to the Device Application Registers. In case a communication frame with an SCK count is not equal to the reported one it will lead to a SPI Error and the data will be rejected.

Table 61. SPI Data Length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
0	1	1	32-bit SPI
1	1	1	64-bit SPI

**Data Consistency Check (Parity/CRC)** 

N/A



**Table 62. Data Consistency Check** 

Bit 1	Bit 0	Description
S1	S0	
0	0	not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

#### **Watchdog Definition**

In case a watchdog is implemented the default settings can be read out via the *Device Information Registers*.

Table 63. WD Type/Timing

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WD1	WD0						
<wd 1="" 2="" type=""></wd>	0	0	Register is not used					
<wd 1="" type=""></wd>	0	1	WT5	WT4	WT3	WT2	WT1	WT0
		1	1	0	1	0	0	0
	Watchdog Timeout / Long Open Window WT[5:0] * 5n						)] * 5ms	
<wd 2="" type=""></wd>	1	0	OW2	OW1	OW0	CW2	CW1	CW0
	1	0	0	1	0	0	0	1
			Open Window OW[2:0] * 5ms			Closed Window CW[2:0] * 5ms		
<wd 1="" 2="" type=""></wd>	1	1	Invalid					

<sup>&</sup>lt;WD Type 1>: 28H (Long Open Window: 200ms)

<WD Type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] times 5ms defines the typical Closed Window time and OW[2:0] times 5ms defines the typical Open Window time.



<sup>&</sup>lt;WD Type 2>: 91H (Open Window. 10ms, Closed Window: 5ms)

<sup>&</sup>lt;WD Type 1> indicates the Long Open Window (timeout) which is opened at the start of the watchdog. The binary value of WT[5:0] times 5ms indicates the typical value of the Timeout Time.

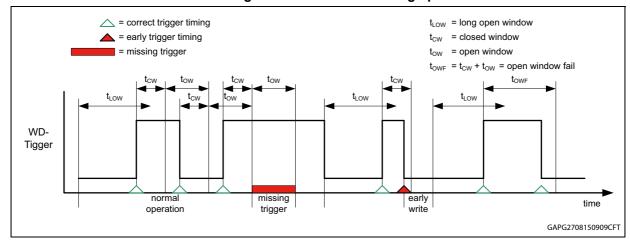


Figure 54. Window watchdog operation

The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 64. WD bit position

Table 04. WD bit position								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WB1	WB0						
<wd bit="" pos.="" x=""></wd>	0	0			Register is	s not used		
<wd bit="" pos.="" x=""></wd>	0	1	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
<wd 1="" bit="" pos.=""></wd>	0	1	0	0	0	0	0	1
<wd 3="" bit="" pos.=""></wd>	0	1	1	1	1	1	1	1
	Defines the register addresses of the WD trigger bits							
<wd bit="" pos.="" x=""></wd>	1	0	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
			Defines the stop address of the address range (previous <wd bit="" pos.="" x=""> is a WB = '01'). The consecutive <wd bit="" pos.="" x=""> has to be a WB = '11'</wd></wd>					
<wd bit="" pos.="" x=""></wd>	1	1	0	WBP 4	WBP3	WBP2	WBP1	WBP0
<wd 2="" bit="" pos.=""></wd>	1	1	0	0	0	0	0	0
<wd 4="" bit="" pos.=""></wd>	1	1	0	0	0	0	0	0
				Defines the binary bit position of the WD trigger bit within the register				

<sup>&</sup>lt; WD bit pos 1>: 41H; watchdog trigger bit located at address 01H (CR1)



<sup>&</sup>lt;WD bit pos 2>: C0H; watchdog trigger bit location is bit0

<sup>&</sup>lt;WD bit pos 3>: 7FH;watchdog trigger bit located at address 3FH (Config Register)

<sup>&</sup>lt;WD bit pos 4>: C0H; watchdog trigger bit location is bit0

### **Device Application Registers (RAM)**

The *Device Application Registers* are all registers accessible using OpCode '00', '01' and '10'. The functions of these registers are defined in the device specification.

#### 5.2.4 Protocol failure detection

To realize a protocol which covers certain failsafe requirements a basic set of failure detection mechanisms is implemented.

#### **Clock monitor**

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI Data Length an SPIE is reported with the next command and the actual communication is rejected.

By accessing the Device Information Registers (OpCode = '11') the Clock Monitor is set to a minimum of 16 SCK edges plus a multiple by 8 (e.g. 16, 25, 32, ...). Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE. For a SPI Burst Read also the SPI Data Length plus multiple numbers of Payloads SCK edges are assumed as a valid communication.

### SCK Polarity (CPOL) check

To detect the wrong polarity access via SCK the internal Clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI Error reported in the next communication and the actual data is rejected.

#### SCK Phase (CPHA) check

To verify, that the SCK Phase of the SPI master is set correctly a special Device Information Register is implemented. By reading this register the data must be 55H. In case AAH is read the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

#### **CSN timeout**

By pulling CSN low the SDO is set active and leaves its 3-state condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to 3-state condition.

#### SDI stuck at GND

As a communication with data all-'0' and OpCode '00' on address b'000000 cannot be distinguished between a valid command and a SDI stuck at GND this communication is not allowed. Nevertheless, in case a stuck at GND is detected the communication will be rejected and the SPIE will be set with the next communication.

#### SDI stuck at HIGH

As a communication with data all-'1' and OpCode '11' on address b'111111 cannot be distinguished between a valid command and a SDI stuck at HIGH this communication is not



allowed. In case a stuck at HIGH is detected the communication will be rejected and the SPIE will be set with the next communication.

### SDO stuck @

The SDO stuck at GND and stuck at HIGH have to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all-'0' or all -'1' reports a stuck at error.



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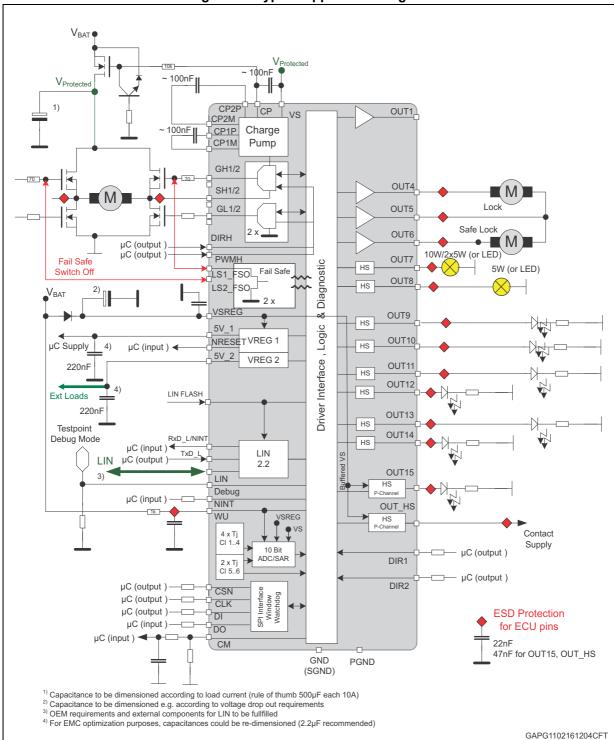


Figure 55. Typical application diagram



# 7 SPI Registers

# 7.1 Global Status Byte GSB

Table 65. Global Status Byte (GSB)

	31	30	29	28	27	26	25	24
Bit name	GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS
Reset	1	0	0	0	0	0	0	0
Access				R				

Table 66. GSB signals description

Bit	Name	Description
31	GSBN	Global Status Bit Inverted The GSBN is a logically NOR combination of GSB Bits 24 to Bit 30 <sup>(1)</sup> . This bit can also be used as Global Status Flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low. 0: error detected (1 or several GSB bits from 24 to 30 are set) 1: no error detected (default after Power-on) Specific failures may be masked in the Configuration Register 0x3F. A masked failure will still be reported in the GSB by the related failure flag, however it is not reflected in the GSBN (bit 31).
30	RSTB	Reset The RSTB indicates a device reset and it is set in case of the following events:  - VPOR (SR1 - 0x31)  - WDFAIL (SR1 - 0x31)  - V1UV (SR1 - 0x31)  - FORCED_SLEEP_TSD2/V1SC (SR1 - 0x31) 0: no reset signal has been generated (default) 1: Reset signal has been generated RSTB is cleared by a <i>Read &amp; Clear</i> command to all bits in <i>Status Register 1</i> causing the Reset event.
29	SPIE <sup>(2)</sup>	SPI Error Bit The SPIE indicates errors related to a wrong SPI communication.  - SPI_INV_CMD (SR2 - 0x32)  - SPI_SCK_CNT (SR2 - 0x32) The bit is also set in case of an SPI CSN Time-out detection 0: no error (default) 1: error detected SPIE is cleared by a valid SPI command.

Table 66. GSB signals description (continued)

Bit	Name	Description
28	PLE <sup>(2)</sup>	Physical Layer Error The PLE is a logical OR combination of errors related to the LIN transceiver.  - LIN_PERM_DOM (SR2 - 0x32)  - LIN_TXD_DOM (SR2 - 0x32)  - LIN_PERM_REC (SR2 - 0x32)  0: no error (default)  1: error detected PLE is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status</i>
27	FE	Functional Error Bit The FE is a logical OR combination of errors coming from functional blocks.  V2SC (SR2 - 0x32)  DSMON_HSx (SR2 - 0x32)  DSMON_LSx (SR2 - 0x32)  OUTxHS_OC TH EX (SR3 - 0x33)  OUTxLS_OC TH EX (SR3 - 0x33)  OUTHS_OC TH EX (SR3 - 0x33)  OUTx_OC (SR3 - 0x33)  LSxFS_OC (SR3 - 0x33)  OUTxHS_OL (SR5 - 0x35)  OUTxLS_OL (SR5 - 0x35)  OUTx_OL (SR5 - 0x35)  OUTx_OL (SR5 - 0x35)  OUTHS_OL (SR5 - 0x35)  OUTHS_OL (SR5 - 0x35)  OUTHS_OL (SR5 - 0x35)  OUTHS_OL (SR5 - 0x35)  Iterror detected  FE is cleared by a Read & Clear command to all related bits in Status Registers 2, 3, 4, 5
26	DE	Device Error Bit  DE is a logical OR combination of global errors related to the device.  - VS_OV (SR2 - 0x32)  - VS_UV (SR2 - 0x32)  - VSREG_OV (SR2 - 0x32)  - VSREG_UV (SR2 - 0x32)  - CP_LOW (SR2 - 0x32)  - TSD1_CLx (SR6 - 0x36)  0: no error (default)  1: error detected  DE is cleared by a Read & Clear command to all related bits in Status Registers 2 and 6

Table 66. GSB signals description (continued)

Bit	Name	Description
25	GW <sup>(2)</sup>	Global Warning Bit GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions.  - VSREG_EW (SR2 - 0x32)  - V1_FAIL (SR2 - 0x32)  - V2_FAIL (SR2 - 0x32)  - TW <sup>(3)</sup> (SR2 - 0x32)  - SPI_INV_CMD (SR2 - 0x32)  - SPI_SCK_CNT (SR2 - 0x32)  0: no error (default) 1: error detected GW is cleared by a <i>Read &amp; Clear</i> command to all related bits in <i>Status Register 2</i> .
24	FS	Fail Safe The FS bit indicates the device was forced into a safe state due to the following failure conditions:  - WDFAIL (SR1 - 0x31)  - V1UV (SR1 - 0x31)  - TSD2 (SR1 - 0x31)  - FORCED_SLEEP_TSD/V1SC (SR1 - 0x31)  All Control Registers are set to default  Control Registers are blocked for WRITE access except the following bits:  - TRIG (CR1 - 0x01)  - V2_0 (CR1 - 0x01)  - V2_1 (CR1 - 0x01)  - Timer settings (bits 823) (CR2 - 0x02)  - OUTHS_x (bits 03) (CR5 - 0x05)  - OUT15_x (bits 03) (CR6 - 0x06)  - CR12 (0x0C) to CR17 (0x11); PWM frequency and duty cycles 0: Fail Safe inactive (default) 1: Fail Safe active FS is cleared upon exit from Fail-Safe mode (refer to chapter 'Fail-Safe mode')

- 1. Individual failure flags may be masked in the Configuration Register (0x3F).
- 2. Bit may be masked in the Configuration Register (0x3F), i.e. the bit will not be included in the Global Status Bit (GSBN).
- Open-load status flags may be masked in the Configuration register (0x3F), i.e. the open-load flag will be included in the FE flag, but will not set the GSBN. TW failure status flags may be masked in the Configuration register (0x3F), i.e. the TW flag will be included in the GW flag, but will not set the GSBN.

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# 7.2 Control register overview

Table 67. Control register overview

													В			51 V IC										40
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x00				ı	ı	ı					ı	F	Rese	erve	d	ı				ı						
0x01	CR1	Reserved	WU_EN	Reserved	WU_PU	boyaged	Neserved	WU_FILT_1	WU_FILT_0	TIMER_NINT_WAKE_SEL	TIMER_NINT_EN			Re	serv	ved			HEN	V2_1	V2_0	PARITY	STBY_SEL	GO_STBY	TRIG	R/W
0x02	CR2	T1_RESTART	T1_DIR	T1_ON_2	T1_0N_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	T2_RESTART	T2_DIR	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	LIN_REC_ONLY	LIN_TXD_TOUT_EN	0000	000	V1_RESET_1	V1_RESET_0	WD_TIME_1	WD_TIME_0	R/W
0x03	CR3	VSREG_LOCK_EN	VS_LOCK_EN	VSREG_OV_SD_EN	VSREG_UV_SD_EN	VS_OV_SD_EN	VS_UV_SD_EN			F	Rese	erved	d			VSREG_EWTH_9	VSREG_EWTH_8	VSREG_EWTH_7	VSREG_EWTH_6	VSREG_EWTH_5	VSREG_EWTH_4	VSREG_EWTH_3	VSREG_EWTH_2	VSREG_EWTH_1	VSREG_EWTH_0	R/W
0x04	CR4	Doggood	ואפספו אפת	OUT1_HS	OUT1_LS				F	Rese	erve	d				OUT4_HS	OUT4_LS	portioned	ואפספו אפת	SH_2TUO	ST_STUO	00000	ואפספו אפת	SH_9TUO	ST_9TUO	R/W
0x05	CR5	0UT7_3	2_7TUO	0UT7_1	0_7TU0	OUT8_3	OUT8_2	0UT8_1	0_8TUO	F	Rese	erve	t	OUT10_3	OUT10_2	OUT10_1	0_01TUO	F	Rese	erve	d	OUTHS_3	S_ZTHTUO	0UTHS_1	O_ZHTUO	R/W
0x06	CR6	OUT9_3	OUT9_2	OUT9_1	0_6TUO	OUT11_3	OUT11_2	OUT11_1	OUT11_0	OUT12_3	OUT12_2	OUT12_1	OUT12_0	OUT13_3	OUT13_2	OUT13_1	OUT13_0	OUT14_3	OUT14_2	OUT14_1	OUT14_0	OUT15_3	OUT15_2	OUT15_1	OUT15_0	R/W
0x07	CR7	OUT1_OCR	0000	אמאון אמר	OUT4_OCR	OUT5_OCR	OUT6_OCR	OUT7_OCR	OUT8_OCR	OUTHS_OCR		F	Rese	erve	d		OCR_FREQ	OUT5_OC1	OUT5_OC0	CM_EN	Reserved	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0	R/W

Table 67. Control register overview (continued)

											3-		В	erv it		(00			<del>,</del>							
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x08	CR8	OUT1_OCR_THX_EN		Reserved	OUT4_OCR_THX_EN	OUT5_OCR_THX_EN	OUT6_OCR_THX_EN	OUT7_OCR_THX_EN	OUT8_OCR_THX_EN	OUTHS_OCR_THX_EN							Re	serv	⁄ed							R/W
0x09	CR9	OUT7_RDSON	OUT8_RDSON		F	Rese	erve	d		OUTHS_OL	OUT15_OL	OUT14_OL	OUT13_OL	OUT12_OL	OUT11_OL	OUT10_OL	OUT9_OL	OUTHS_OC	OUT15_OC	OUT14_OC	OUT13_OC	OUT12_OC	OUT11_OC	OUT10_OC	OUT9_OC	R/W
0x0A	CR10	DIAG_2	DIAG_1	DIAG_0			Re	serv	/ed			SD	SDS	COPT_3	COPT_2	COPT_1	COPT_0	н_огтн_нісн	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0	R/W
0x0B	CR11		ı		1							F	Rese	rve	d							1			1	R/W
0x0C	CR12	PMW1_FREQ_1	PMW1_FREQ_0	PMW2_FREQ_1	PMW2_FREQ_0	PMW3_FREQ_1	PMW3_FREQ_0	PMW4_FREQ_1	PMW4_FREQ_0	PMW5_FREQ_1	PMW5_FREQ_0	PMW6_FREQ_1	PMW6_FREQ_0	PMW7_FREQ_1	PMW7_FREQ_0	PMW8_FREQ_1	PMW8_FREQ_0	PMW9_FREQ_1	PMW9_FREQ_0	PMW10_FREQ_1	PMW10_FREQ_0	F	Rese	erve	d	R/W
0x0D	CR13	portional	חפא פו אפר	PWM1_DC_9	PWM1_DC_8	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	Dovingo	200	PWM2_DC_9	PWM2_DC_8	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	R/W
0x0E	CR14	portional	אפאפו	PWM3_DC_9	PWM3_DC_8	PWM3_DC_7	PWM3_DC_6	PWM3_DC_5	PWM3_DC_4	PWM3_DC_3	PWM3_DC_2	PWM3_DC_1	PWM3_DC_0	70/2000	555	PWM4_DC_9	PWM4_DC_8	PWM4_DC_7	PWM4_DC_6	PWM4_DC_5	PWM6_DC_4 PWM4_DC_4	PWM4_DC_3	PWM4_DC_2	PWM4_DC_1	PWM4_DC_0	R/W
0x0F	CR15	0000	מפאבו אפט	PWM5_DC_9	PWM5_DC_8	PWM5_DC_7	PWM5_DC_6	PWM5_DC_5	PWM5_DC_4	PWM5_DC_3	PWM5_DC_2	PWM5_DC_1	PWM5_DC_0	Dovingo		PWM6_DC_9	PWM6_DC_8	PWM6_DC_7	PWM6_DC_6	PWM6_DC_5	PWM6_DC_4	PWM6_DC_3	PWM6_DC_2	PWM6_DC_1	PWM6_DC_0	R/W



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Table 67. Control register overview (continued)

							0 01						В	it				iiuc								0
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x10	CR16	portional	חשא ושפשע	PWM7_DC_9	PWM7_DC_8	PWM7_DC_7	PWM7_DC_6	PWM7_DC_5	PWM7_DC_4	PWM7_DC_3	PWM7_DC_2	PWM7_DC_1	PWM7_DC_0	portioned	חפאם אפת	PWM8_DC_9	PWM8_DC_8	PWM8_DC_7	PWM8_DC_6	PWM8_DC_5	PWM8_DC_4	PWM8_DC_3	PWM8_DC_2	PWM8_DC_1	PWM8_DC_0	R/W
0x11	CR17	portional	אפאפו אפת	PWM9_DC_9	PWM9_DC_8	PWM9_DC_7	PWM9_DC_6	PWM9_DC_5	PWM9_DC_4	PWM9_DC_3	PWM9_DC_2	PWM9_DC_1	PWM9_DC_0	boynoad	Nesel ved	PWM10_DC_9	PWM10_DC_8	PWM10_DC_7	PWM10_DC_6	PWM10_DC_5	PWM10_DC_4	PWM10_DC_3	PWM10_DC_2	PWM10_DC_1	PWM10_DC_0	R/W
0x12	CR18	Reserved	OUT7_AUTOCOMP_EN	OUT7_VLED_9	OUT7_VLED_8	OUT7_VLED_7	OUT7_VLED_6	OUT7_VLED_5	OUT7_VLED_4	OUT7_VLED_3	OUT7_VLED_2	OUT7_VLED_1	OUT7_VLED_0	Reserved	OUT8_AUTOCOMP_EN	OUT8_VLED_9	OUT8_VLED_8	OUT8_VLED_7	OUT8_VLED_6	OUT8_VLED_5	OUT8_VLED_4	OUT8_VLED_3	OUT8_VLED_2	OUT8_VLED_1	OUT8_VLED_0	R/W
0x13	CR19	Reserved	OUT9_AUTOCOMP_EN	OUT9_VLED_9	OUT9_VLED_8	OUT9_VLED_7	OUT9_VLED_6	OUT9_VLED_5	OUT9_VLED_4	OUT9_VLED_3	OUT9_VLED_2	OUT9_VLED_1	OUT9_VLED_0	Reserved	OUT10_AUTOCOMP_EN	OUT10_VLED_9	OUT10_VLED_8	OUT10_VLED_7	OUT10_VLED_6	OUT10_VLED_5	OUT10_VLED_4	OUT10_VLED_3	OUT10_VLED_2	OUT10_VLED_1	OUT10_VLED_0	R/W
0x14	CR20	Reserved	OUT11_AUTOCOMP_EN	OUT11_VLED_9	OUT11_VLED_8	OUT11_VLED_7	OUT11_VLED_6	OUT11_VLED_5	OUT11_VLED_4	OUT11_VLED_3	OUT11_VLED_2	OUT11_VLED_1	OUT11_VLED_0	Reserved	OUT12_AUTOCOMP_EN	OUT12_VLED_9	OUT12_VLED_8	OUT12_VLED_7	OUT12_VLED_6	OUT12_VLED_5	OUT12_VLED_4	OUT12_VLED_3	OUT12_VLED_2	OUT12_VLED_1	OUT12_VLED_0	R/W

Table 67. Control register overview (continued)

													В	it												6
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x15	CR21	Reserved	OUT13_AUTOCOMP_EN	OUT13_VLED_9	OUT13_VLED_8	OUT13_VLED_7	OUT13_VLED_6	OUT13_VLED_5	OUT13_VLED_4	OUT13_VLED_3	OUT13_VLED_2	OUT13_VLED_1	OUT13_VLED_0	Reserved	OUT14_AUTOCOMP_EN	OUT14_VLED_9	OUT14_VLED_8	OUT14_VLED_7	OUT14_VLED_6	OUT14_VLED_5	OUT14_VLED_4	OUT14_VLED_3	OUT14_VLED_2	OUT14_VLED_1	OUT14_VLED_0	R/W
0x16	CR22	Reserved	OUT15_AUTOCOMP_EN	OUT15_VLED_9	OUT15_VLED_8	OUT15_VLED_7	OUT15_VLED_6	OUT15_VLED_5	OUT15_VLED_4	OUT15_VLED_3	OUT15_VLED_2	OUT15_VLED_1	OUT15_VLED_0	Reserved	OUTHS_AUTOCOMP_EN	OUTHS_VLED_9	OUTHS_VLED_8	OUTHS_VLED_7	OUTHS_VLED_6	OUTHS_VLED_5	OUTHS_VLED_4	OUTHS_VLED_3	OUTHS_VLED_2	OUTHS_VLED_1	OUTHS_VLED_0	R/W
0x22	CR34										Re	serv	ed										SP_OFF	ICMP	WD_EN	R/W
0x3F	Conf Reg	WU_CONFIG	LIN_WU_CONFIG	LIN_HS_EN	TSD_CONFIG	Reserved	MQ	ICMP_CONFIG_EN	WD_CONFIG_EN	MASK_OL_HS1	MASK_OL_LS1	MASK_TW	Reserved	MASK_OL	MASK_SPIE	MASK_PLE	MASK_GW	CP_OFF_EN	CP_LOW_CONFIG	CP_DITH_DIS	FS_FORCED		Reserved		TRIG	R/W

Note: All reserved bits (RES) are read-only (R) and will be read as '0'. Writing '1' to a reserved bit is ignored and does not cause an SPI error.

# 7.3 Status register overview

Table 68. Status register overview

														it	046											Access
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31	SR1	Reserved	WU_STATE	Reserved	WU_WAKE	Reserved	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR	R
0x32	SR2	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC		Re	serv	ed		DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	WT	V2SC	V2FAIL	V1FAIL	VSREG_EW	VSREG_OV	VSREG_UV	vo_sv	VS_UV	R
0x33	SR3	OUT1_HS_OC_TH_EX	OUT1_LS_OC_TH_EX	F	Rese	erved	d	OUT4_HS_OC_TH_EX	OUT4_LS_OC_TH_EX	OUT5_HS_OC_TH_EX	OUT5_LS_OC_TH_EX	OUT6_HS_OC_TH_EX	OUT6_LS_OC_TH_EX	OUT7_OC_TH_EX	OUT8_OC_TH_EX	OUT9_OC	OUT10_0C	OUT11_0C	OUT12_OC	OUT13_OC	OUT14_OC	OUT15_OC	OUTHS_OC_TH_EX	LS2FSO_OC	LS1FSO_OC	R
0x34	SR4	OUT1_HS_OCR_ALERT	OUT1_LS_OCR_ALERT	F	Rese	eserved			OUT4_LS_OCR_ALERT	OUT5_HS_OCR_ALERT	OUT5_LS_OCR_ALERT	OUT6_HS_OCR_ALERT	OUT6_LS_OCR_ALERT	OUT7_OCR_ALERT	OUT8_OCR_ALERT			Re	serv	ed 'ed			OUTHS_OCR_ALERT	Control	000	R
0x35	SR5	OUT1_HS_OL	OUT1_LS_OL	F	Rese	served			OUT4_LS_OL	OUT5_HS_OL	OUT5_LS_OL	OUT6_HS_OL	OUT6_LS_OL	OUT7_OL	OUT8_OL	OUT9_OL	OUT10_OL	OUT11_OL	OUT12_OL	OUT13_OL	OUT14_OL	OUT15_OL	OUTHS_OL	Portugue	000000000000000000000000000000000000000	R

Table 68. Status register overview (continued)

													В	it												Access
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x36	SR6	WD_TIMER_STATE_1	WD_TIMER_STATE_0			F	Rese	erve	d			TW_CL6	TW_CL5	TW_CL4	TW_CL3	TW_CL2	TW_CL1	700 E	צפאפו אפס	TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1	R
0x37	SR7	Doynood	אם אם אם	TEMP_CL2_9	TEMP_CL2_8	TEMP_CL2_7	TEMP_CL2_6	TEMP_CL2_5	TEMP_CL2_4	TEMP_CL2_3	TEMP_CL2_2	TEMP_CL2_1	TEMP_CL2_0	boynoad	Nesel ved	TEMP_CL1_9	TEMP_CL1_8	TEMP_CL1_7	TEMP_CL1_6	TEMP_CL1_5	TEMP_CL1_4	TEMP_CL1_3	TEMP_CL1_2	TEMP_CL1_1	TEMP_CL1_0	R
0x38	SR8	Doyngood	אמס אפר	TEMP_CL4_9	TEMP_CL4_8	TEMP_CL4_7	TEMP_CL4_6	TEMP_CL4_5	TEMP_CL4_4	TEMP_CL4_3	TEMP_CL4_2	TEMP_CL4_1	TEMP_CL4_0	Doynood	ויפספו אפת	TEMP_CL3_9	TEMP_CL3_8	TEMP_CL3_7	TEMP_CL3_6	TEMP_CL3_5	TEMP_CL3_4	TEMP_CL3_3	TEMP_CL3_2	TEMP_CL3_1	TEMP_CL3_0	R
0x39	SR9	Doynood	חם אום פטע	TEMP_CL6_9	TEMP_CL6_8	TEMP_CL6_7	TEMP_CL6_6	TEMP_CL6_5	TEMP_CL6_4	TEMP_CL6_3	VSREG_2 TEMP_CL6_2 TEMP_CL4_	TEMP_CL6_1	TEMP_CL6_0	portional	וופסטו אפט	TEMP_CL5_9	TEMP_CL5_8	TEMP_CL5_7	TEMP_CL5_6	TEMP_CL5_5	TEMP_CL5_4	TEMP_CL5_3	TEMP_CL5_2	TEMP_CL5_1	TEMP_CL5_0	R
0x3A	SR10	Doynosod	מפוני מיני	VSREG_9	VSREG_8	VSREG_7	VSREG_6	VSREG_5	VSREG_4	VSREG_3	VSREG_2	VSREG_1	VSREG_0					ı	Rese	erve	d					R
0x3B	SR11	postago	מפת אפת	6 SV	VS_8	VS_7	NS_6	VS_5	VS_4	VS_3	VS_2	VS_1	0_SV	boynoad	ואפאפו אפת	6_UWV	WWU_8	VWU_7	9_UWV	VWU_5	VWU_4	vwu_3	VWU_2	VWU_1	VWU_0	R

# 7.4 Control registers

## 7.4.1 Control Register CR1 (0x01)

### Table 69. Control Register CR1

												. · · ·												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	WU_EN	Reserved	WU_PU	Dayyaaa	000000	WU_FILT_1	WU_FILT_0	TIMER_NIONT_WAKE_SEL	TIMER_NINT_EN			Re	serv	red			HEN	V2_1	V2_0	PARITY	STBY_SEL	GO_STBY	TRIG
Reset	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R	R/W	F	?									R/	W								

### Table 70. CR1 signals description

Bit	Name	Description
23	Reserved	_
22	WU_EN	Wake-up Input 1 (WU) enable <sup>(1)</sup> 0: WU disabled 1: WU enabled (default)
21	Reserved	_
20	WU_PU	Wake-up Input1 Pull-up/down configuration: configuration of internal current source <sup>(1)</sup> 0: pull-down (default) 1: pull-up
19	Reserved	
18	Neserveu	
17	WU_FILT_1	Wake-up Input1 Filter configuration Bits: configuration of input filter <sup>(1)</sup>
16	WU_FILT_0	See Table 71: Wake-up input1 filter configuration
15	TIMER_NINT_WAKE_SEL	Select Timer for NINT / Wake: select timer for periodic interrupt in standby modes 0: Timer 2 (default) 1: Timer 1

Table 70. CR1 signals description (continued)

Bit	Name	Description
14	TIMER_NINT_EN	Timer NINT enable: enable timer interrupt in standby modes 0: timer interrupt disabled (default) 1: timer interrupt enabled V1_standby mode: periodic NINT pulse generated by timer (NINT pulse at start of timer on-phase) Vbat_standby mode: device wakes up after timer expiration and generates NReset
13:7	Reserved	_
6	HEN	Enable H-bridge  0: H-bridge disabled (default)  1: H-bridge enabled  Refer to chapter <i>H-bridge Control</i> for details
5	V2_1	Voltage Regulator V2 Configuration
4	V2_0	See Table 72: Voltage regulator V2 configuration
3	PARITY	PARITY: Standby Command Parity Bit
2	STBY_SEL	STBY SEL: Select Standby mode
1	GO_STBY	GO_STBY: Execute transition into Standby mode The STBY_SEL and GO_STBY bits are protected by a parity check. The bits STBY_SEL, GO_STBY and PARITY must represent an even number of '1', otherwise the command is ignored and the SPI_INV_CMD bit is set.  Table 73: Standby transition configuration shows the valid settings. All other settings are invalid; command will be ignored and SPI_INV_CMD will be set. The GO_STBY bit is not cleared automatically after wake-up.
0	TRIG	Watchdog Trigger Bit

<sup>1.</sup> Setting is only valid if input is configured as wake-up input in Configuration Register (0x3F).

Table 71. Wake-up input1 filter configuration

idolo i ii iidalo de inedici intol consiguidado.											
WU_FILT_1	WU_FILT_0										
0	0	Wake-up inputs monitored in static mode (filter time twu_stat) (default)									
0	1	Wake- up inputs monitored in cyclic mode with Timer2 (filter time: $t_{WU\_cyc}$ ; blanking time 80% of timer ON time)									
1	0	Wake- up inputs monitored in cyclic mode with Timer1 (filter time: $t_{WU\_cyc}$ ; blanking time 80% of timer ON time)									
1	1	Invalid setting; command will be ignored and SPI INV CMD will be set									

Table 72. Voltage regulator V2 configuration

V2_1	V2_0	
0	0	V2 OFF in all modes (default)
0	1	V2 ON in Active mode; OFF in Standby modes



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### Table 72. Voltage regulator V2 configuration (continued)

V2_1	V2_0	
1	0	V2 ON in Active and V1_standby mode; OFF in Vbat_standby mode
1	1	V2 ON in all modes

### Table 73. Standby transition configuration

PARITY	STBY_SEL	GO_STBY									
0	1	1	Go to V1 standby								
1	0	1	Go to Vbat_standby								
0	0	0	No transition to standby								
1	1	0	No transition to standby								

### 7.4.2 Control Register CR2 (0x02)

### Table 74. Control Register CR2

								<i>-</i>				<u>J</u> -												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	T1_RESTART	T1_DIR	T1_ON_2	1_0N_1T	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	T2_RESTART	T2_DIR	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	LIN_REC_ONLY	LIN_TXD_TOUT_EN	beyoseA		V1_RESET_1	V1_RESET_0	WD_TIME_1	WD_TIME_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Access												R/W		•	•									

#### Table 75. CR2 signals description

Bit	Name	Description
23	T1_RESTART	Timer 1 Restart: Restart of Timer 1 0: timer is running with period and on-time according to configuration (default) 1: restart of timer at CSN low to high transition; starting with ON phase <sup>(1)</sup> Bit is automatically reset with next SPI frame.
22	T1_DIR1	
21	T1_ON_2	T1_DIR1: Timer 1 Direct Drive by DIR1 T1 ON x: Timer 1 On-Time Bits
20	T1_ON_1	Configuration of Timer 1 on-time, for details see <i>Table 76</i> and <i>Figure 56</i>
19	T1_ON_0	

Table 75. CR2 signals description (continued)

Bit	Name	Description
18	T1_PER_2	Configuration of Timer 1 Period
17	T1_PER_1	000: T1 (default)
16	T1_PER_0	001: T2 010: T3 011: T4 100: T5 101: T6 110: T7 111: T8
15	T2_RESTART	Timer 2 Restart: restart of timer 2 0: timer is running with period and on-time according to configuration (default) 1: restart of timer at CSN low to high transition; starting with ON phase <sup>(1)</sup> Bit is automatically reset with next SPI frame.
14	T2_DIR1	
13	T2_ON_2	T2_DIR1: Timer 2 Direct Drive by DIR1
12	T2_ON_1	T2_ON_x: Timer 2 On-Time Bits Configuration of Timer 2 on-time, for details see <i>Table 76</i> and <i>Figure 56</i>
11	T2_ON_0	,
10	T2_PER_2	Configuration of Timer 2 Period
9	T2_PER_1	000: T1 (default) 001: T2
8	T2_PER_0	010: T2 010: T3 011: T4 100: T5 101: T6 110: T7 111: T8
7	LIN_REC_ONLY	LIN Transceiver Receive Only mode 0: LIN receive only mode disabled (default) 1: LIN receive only mode enabled
6	LIN_TXD_TOUT_EN	LIN TxD Timeout Enable 0: LIN TxD timeout detection disabled 1: LIN TxD timeout detection enabled (default)
5:4	Reserved	

Table 75. CR2 signals description (continued)

Bit	Name	Description
3	V1_RESET_1	Voltage Regulator V1 Reset Threshold
2	V1_RESET_0	00: Vrt4 (default) 01: Vrt3 10: Vrt2 11: Vrt1 thresholds are monitored in Active mode and V1_standby mode
1	WD_TIME_1	Watchdog Trigger Time
0	WD_TIME_0	00: TSW1 (default) 01: TSW2 10: TSW3 11: TSW4 Writing to WD_TIME_x is blocked unless WD CONFIG EN = 1. The modified WD Trigger Time is valid immediately after the Write command (CSN transition low-high). The watchdog timer is reset when the trigger time is modified (restart at CSN transition low-high).

Timer restart behavior:
Write to CR2 when Tx\_ON\_x and Tx\_PERx remain unchanged:
Tx\_RESTART = 1: timers restart at end of SPI frame, starting with ON time
Tx\_RESTART = 0: write operation to CR2 has no effect on timers
Write to CR2 when Tx\_ON\_x and Tx\_PERx are modified
Tx\_RESTART = 1: timers restart at end of SPI frame, starting with ON time and according to new setting (ON time and period) period)

Tx\_RESTART = 0: behavior is not defined; if a predictable behavior is needed, it is recommended to set Tx\_RESTART = 1

Table 76. Configuration of Timer x on-time

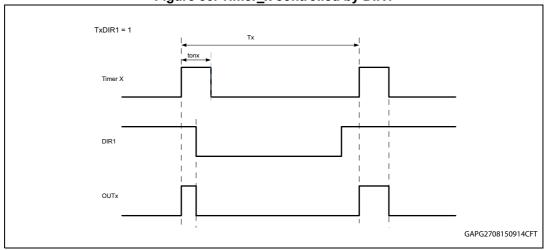
Tx_DIR1	Tx_ON_2	Tx_ON_1	Tx_ON_0							
0	0	0	0	ton1 (default)						
0	0	0	1	ton2						
0	0	1	0	ton3						
0	0	1	1	ton4						
0	1	0	0	ton5						
0	1	0	1							
0	1	1	0	Invalid setting; command will be ignored and SPI INV CMD will be set						
0	1	1	1							
1 <sup>(1)</sup>	0	0	0	ton1 controlled by DIR1 input signal (logical AND)						
1 <sup>(1)</sup>	0	0	1	ton2 controlled by DIR1 input signal (logical AND)						
1 <sup>(1)</sup>	0	1	0	ton3 controlled by DIR1 input signal (logical AND)						
1 <sup>(1)</sup>	0	1	1	ton4 controlled by DIR1 input signal (logical AND)						
1 <sup>(1)</sup>	1	0	0	ton5 controlled by DIR1 input signal (logical AND)						

Table 76. Configuration of Timer x on-time (continued)

Tx_DIR1	Tx_ON_2	Tx_ON_1	Tx_ON_0	
1 <sup>(1)</sup>	1	0	1	
1 <sup>(1)</sup>	1	1	0	Invalid setting; command will be ignored and SPI INV CMD will be set
1 <sup>(1)</sup>	1	1	1	

Tx\_DIR1 = 1 is only valid for OUT7-OUT15 and OUT\_HS control; the DIR1 signal has no influence for WU monitoring if WU is monitored by timer.

Figure 56. Timer\_x controlled by DIR1



### 7.4.3 Control Register CR3 (0x03)

Table 77. Control Register CR3

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	VSREG_LOCK_EN	VS_LOCK_EN	VSREG_OV_SD_EN	VSREG_UV_SD_EN	VS_OV_SD_EN	VS_UV_SD_EN		Reserved							VSREG_EWTH_9	VSREG_EWTH_8	VSREG_EWTH_7	VSREG_EWTH_6	VSREG_EWTH_5	VSREG_EWTH_4	VSREG_EWTH_3	VSREG_EWTH_2	VSREG_EWTH_1	VSREG_EWTH_0
Reset	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access												R/W												

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Table 78. CR3 signals description

Bit	Name	Description
23	VSREG_LOCK_EN	V <sub>SREG</sub> lockout enable: Lockout of V <sub>SREG</sub> related outputs after V <sub>SREG</sub> overvoltage/ undervoltage shutdown  0: V <sub>SREG</sub> related Outputs are turned on automatically and status bits (VSREG_UV, VSREG_OV) are cleared  1: V <sub>SREG</sub> related Outputs remain turned off until status bits (VSREG_UV, VSREG_OV) are cleared (default)  Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions
22	VS_LOCK_EN	$\label{eq:VS} V_S \ \text{lockout enable: Lockout of V}_S \ \text{related outputs after V}_S \ \text{over/undervoltage} \\ \text{shutdown} \\ 0: V_S \ \text{related Outputs are turned on automatically and status bits (VS_UV, VS_OV) are cleared} \\ 1: V_S \ \text{related Outputs remain turned off until status bits (VS_UV, VS_OV) are cleared (default)} \\ \text{Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions} \\$
21	VSREG_OV_SD_EN	V <sub>SREG</sub> overvoltage shutdown enable: shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> overvoltage 0: no shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> overvoltage 1: shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> overvoltage (default)
20	VSREG_UV_SD_EN	V <sub>SREG</sub> undervoltage shutdown enable: shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> undervoltage 0: no shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> undervoltage 1: shutdown of V <sub>SREG</sub> related outputs in case of V <sub>SREG</sub> undervoltage (default) In case of V1 undervoltage due to VSREG_UV, the device enters Fail-Safe mode and the outputs are turned off
19	VS_OV_SD_EN	$V_S$ overvoltage shutdown enable: shutdown of $V_S$ related outputs in case of $V_S$ overvoltage 0: no shutdown of $V_S$ related outputs in case of $V_S$ overvoltage if charge pump output voltage is still sufficient (until CPLOW threshold is reached) 1: shutdown of $V_S$ related outputs in case of $V_S$ overvoltage (default)
18	VS_UV_SD_EN	$V_S$ undervoltage shutdown enable: shutdown of $V_S$ related outputs in case of $V_S$ undervoltage 0: no shutdown $V_S$ related of outputs in case of $V_S$ undervoltage 1: shutdown of $V_S$ related outputs in case of $V_S$ undervoltage (default) In case of V1 undervoltage due to VS_UV, the device enters Fail-Safe mode and the outputs are turned off
17:10	Reserved	Reserved

Table 78. CR3 signals description (continued)

Bit	Name	Description
9	VSREG_EW_TH_9	
8	VSREG_EW_TH_8	
7	VSREG_EW_TH_7	
6	VSREG_EW_TH_6	V <sub>SREG</sub> early warning threshold.  At V <sub>SREG</sub> < VSREG_EW_TH, an interrupt is generated at NINT and status bit
5	VSREG_EW_TH_5	VSREG_EW in SR2 is set (in Active mode)
4	VSREG_EW_TH_4	000000000: 0 V (default) feature deactivated
3	VSREG_EW_TH_3	 1111111111: V <sub>AINVS</sub>
2	VSREG_EW_TH_2	Alinvs
1	VSREG_EW_TH_1	
0	VSREG_EW_TH_0	

## 7.4.4 Control Register CR4 (0x04)

Table 79. Control Register CR4

												U												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name		Reserved	OUT1_HS	OUT1_LS				F	Rese	erve	d				OUT4_HS	OUT4_LS	Posopyod	>	OUT5_HS	OUT5_LS	Doggood	ואפאפו אפת	опте_нѕ	OUT6_LS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

Table 80. CR4 signals description

Bit	Name	Description
23:22	Reserved	Reserved
21	OUT1_HS	OUT1 high-side Driver control 0: OUT1_HS is turned off (default) 1: OUT1_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.
20	OUT1_LS	OUT1 low-side Driver control 0: OUT1_LS is turned off (default) 1: OUT1_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.
19:10	Reserved	Reserved

Table 80. CR4 signals description (continued)

Bit	Name	Description						
9	OUT4_HS	OUT4 high-side Driver control 0: OUT4_HS is turned off (default) 1: OUT4_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.						
8	OUT4_LS	OUT4 low-side Driver control 0: OUT4_LS is turned off (default) 1: OUT4_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.						
7:6	Reserved	Reserved						
5	OUT5_HS	OUT5 high-side Driver control 0: OUT5_HS is turned off (default) 1: OUT5_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.						
4	OUT5_LS	OUT5 low-side Driver control 0: OUT5_LS is turned off (default) 1: OUT5_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.						
3:2	Reserved	Reserved						
1	OUT6_HS	OUT6 high-side Driver control 0: OUT6_HS is turned off (default) 1: OUT6_HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously.						
0	OUT6_LS	OUT6 low-side Driver control 0: OUT6_LS is turned off (default) 1: OUT6_LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously.						

## 7.4.5 Control Register CR5 (0x05)

**Table 81. Control Register CR5** 

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT7_3	OUT7_2	OUT7_1	0_7TU0	OUT8_3	OUT8_2	OUT8_1	OUT8_0	Reserved				OUT10_3	OUT10_2	OUT10_1	OUT10_0	Reserved				OUTHS_3	OUTHS_2	OUTHS_1	OUTHS_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 82. CR5 signals description

Bit	Name	Description
23	OUT7_3	
22	OUT7_2	OUT7 Configuration Bits: high-side Driver OUT7 Configuration
21	OUT7_1	For OUT7 bits configuration see <i>Table 83: OUTx Configuration bits</i>
20	OUT7_0	
19	OUT8_3	
18	OUT8_2	OUT8 Configuration Bits: high-side Driver OUT8 Configuration
17	OUT8_1	For OUT8 bits configuration see <i>Table 83: OUTx Configuration bits</i>
16	OUT8_0	
15:12	Reserved	_
11	OUT10_3	
10	OUT10_2	OUT10 Configuration Bits: high-side Driver OUT10 Configuration
9	OUT10_1	For OUT10 bits configuration see <i>Table 83: OUTx Configuration bits</i>
8	OUT10_0	
7:4	Reserved	
3	OUTHS_3	
2	OUTHS_2	OUTHS Configuration Bits: high-side Driver OUTHS Configuration
1	OUTHS_1	For OUTHS bits configuration see Table 83: OUTx Configuration bits
0	OUTHS_0	

Table 83. OUTx Configuration bits

OUTx_3	OUTx_2	OUTx_1	OUTx_0	Description
0	0	0	0	Off (default)
0	0	0	1	On
0	0	1	0	Timer1
0	0	1	1	Timer2
0	1	0	0	PWM1
0	1	0	1	PWM2
0	1	1	0	PWM3
0	1	1	1	PWM4
1	0	0	0	PWM5
1	0	0	1	PWM6
1	0	1	0	PWM7
1	0	1	1	PWM8
1	1	0	0	PWM9

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Table 83. OUTx Configuration bits (continued)

OUTx_3	OUTx_2	OUTx_1	OUTx_0	Description
1	1	0	1	PWM10
1	1	1	0	DIR1
1	1	1	1	DIR2

## 7.4.6 Control Register CR6 (0x06)

Table 84. Control Register CR6

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT9_3	OUT9_2	OUT9_1	0_6TUO	OUT11_3	OUT11_2	OUT11_1	OUT11_0	OUT12_3	OUT12_2	OUT12_1	OUT12_0	OUT13_3	OUT13_2	OUT13_1	OUT13_0	OUT14_3	OUT14_2	OUT14_1	OUT14_0	OUT15_3	OUT15_2	OUT15_1	OUT15_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

Table 85. CR6 signals description

Bit	Name	Description					
23	OUT9_3						
22	OUT9_2	OUT9 Configuration Bits: high-side Driver OUT9 Configuration					
21	OUT9_1	For OUT9 bits configuration see Table 83: OUTx Configuration bits					
20	OUT9_0						
19	OUT11_3						
18	OUT11_2	OUT11 Configuration Bits: high-side Driver OUT11 Configuration					
17	OUT11_1	For OUT11 bits configuration see <i>Table 83: OUTx Configuration bits</i>					
16	OUT11_0						
15	OUT12_3						
14	OUT12_2	OUT12 Configuration Bits: high-side Driver OUT12 Configuration					
13	OUT12_1	For OUT12 bits configuration see <i>Table 83: OUTx Configuration bits</i>					
12	OUT12_0						
11	OUT13_3						
10	OUT13_2	OUT13 Configuration Bits: high-side Driver OUT13 Configuration					
9	OUT13_1						
8	OUT13_0						

Table 85. CR6 signals description (continued)

Bit	Name	Description					
7	OUT14_3						
6	OUT14_2	OUT14 Configuration Bits: high-side Driver OUT14 Configuration					
5	OUT14_1	For OUT14 bits configuration see <i>Table 83: OUTx Configuration bits</i>					
4	OUT14_0						
3	OUT15_3						
2	OUT15_2	OUT15 Configuration Bits: high-side Driver OUT15 Configuration					
1	OUT15_1	For OUT15 bits configuration see <i>Table 83: OUTx Configuration bits</i>					
0	OUT15_0						

## 7.4.7 Control Register CR7 (0x07)

### Table 86. Control Register CR7

												- 5												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_OCR	Reserved		OUT4_OCR	OUT5_OCR	OUT6_OCR	OUT7_OCR	OUT8_OCR	OUTHS_OCR		F	Rese	erved	d		OCR_FREQ	OUT5_OC1	OUT5_OC0	CM_EN	Reserved	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Access		R/W																						

#### Table 87. CR7 signals description

Bit	Name	Description										
23	OUT1_OCR	Overcurrent recovery for OUT1 0: overcurrent recovery is turned off (default) 1: overcurrent recovery is turned on										
22:21	Reserved	_										
20	OUT4_OCR											
19	OUT5_OCR	Overcurrent recovery for OUTx										
18	OUT6_OCR	0: overcurrent recovery is turned off (default)										
17	OUT7_OCR	1: overcurrent recovery is turned on										
16	OUT8_OCR											
15	OUTHS_OCR	Overcurrent recovery for OUTHS  0: overcurrent recovery is turned off (default)  1: overcurrent recovery is turned on										
14:9	Reserved	_										

Table 87. CR7 signals description (continued)

Bit	Name	Description
8	OCR_FREQ	Overcurrent recovery frequency 0: freq0 (default) 1: freq1
7	OUT5_OC1	Overcurrent Threshold for OUT5
6	OUT5_OC0	00: IOC5_3 overcurrent threshold 3 (default) 01: IOC5_1 overcurrent threshold 1 10: IOC5_2 overcurrent threshold 2 11: IOC5_3 overcurrent threshold 3
5	CM_EN	Current monitor: 0: off (3-state) 1: on (default)
4	Reserved	_
3	CM_SEL_3	Current Monitor Select Bits.
2	CM_SEL_2	A current image of the selected binary coded output is multiplexed to the CM output. If a corresponding output does not exist, the current monitor is deactivated.
1	CM_SEL_1	0000: OUT1
0	CM_SEL_0	0001: invalid configuration 0010: invalid configuration 0011: OUT4 0100: OUT5 0101: OUT6 0110: OUT7 0111: OUT8 1000: OUT9 1001: OUT10 1010: OUT11 1011: OUT12 1100: OUT13 1101: OUT14 1110: OUT15 1111: OUT_HS

# 7.4.8 Control Register CR8 (0x08)

### Table 88. Control Register CR8

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_OCR_THX_EN	Reserved		OUT4_OCR_THX_EN	OUT5_OCR_THX_EN	OUT6_OCR_THX_EN	OUT7_OCR_THX_EN	OUT8_OCR_THX_EN	OUTHS_OCR_THX_EN							Re	esrve	ed						
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

### Table 89. CR8 signals description

Bit	Name	Description
23	OUT1_OCR_THX_EN	Enable Overcurrent Recovery with Thermal Expiration for OUTx.  0: Overcurrent Recovery with Thermal Expiration is off  1: Overcurrent Recovery with Thermal Expiration is on (default)  The output is turned off after Thermal Expiration.
22:21	Reserved	_
20	OUT4_OCR_THX_EN	
19	OUT5_OCR_THX_EN	Enable Overcurrent Recovery with Thermal Expiration for OUTx.
18	OUT6_OCR_THX_EN	Overcurrent Recovery with Thermal Expiration is off     Overcurrent Recovery with Thermal Expiration is on (default)
17	OUT7_OCR_THX_EN	The output is turned off after Thermal Expiration.
16	OUT8_OCR_THX_EN	
15	OUTHS_OCR_THX_EN	Enable Overcurrent Recovery with Thermal Expiration for OUTHS.  0: Overcurrent Recovery with Thermal Expiration is off  1: Overcurrent Recovery with Thermal Expiration is on (default) The output is turned off after Thermal Expiration.
14:0	Reserved	_

# 7.4.9 Control Register CR9 (0x09)

### Table 90. Control Register CR9

							<b></b>																	
	23	22	21	1 20 19 18 17 16						14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT7_RDSON	OUT8_RDSON		R	eser	ved			OUTHS_OL	OUT15_OL	OUT14_OL	OUT13_OL	OUT12_OL	OUT11_OL	OUT10_OL	OUT9_OL	OUTHS_OC	OUT15_OC	OUT14_OC	OUT13_OC	OUT12_OC	OUT11_0C	OUT10_OC	OUT9_OC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

### Table 91. CR9 signals description

		able 91. CR9 signals description								
Bit	Name	Description								
23	OUT7_RDSON	Select Rdson for OUT7 0: r <sub>on_low</sub> (default) 1: r <sub>on_high</sub>								
22	OUT8_RDSON	Select Rdson for OUT8  0: r <sub>on_low</sub> (default)  1: r <sub>on_high</sub>								
21:16	Reserved	_								
15	OUTHS_OL									
14	OUT15_OL									
13	OUT14_OL									
12	OUT13_OL	Open-load Threshold for OUTx								
11	OUT12_OL	0: I <sub>OLD1</sub> ; high-current mode (default) 1: I <sub>OLD1</sub> ; low-current mode								
10	OUT11_OL	925.								
9	OUT10_OL									
8	OUT9_OL									
7	OUTHS_OC									
6	OUT15_OC									
5	OUT14_OC									
4	OUT13_OC	Overcurrent Threshold for OUTx  O: I <sub>OC</sub> ; high-current mode (default)								
3	OUT12_OC	1: l <sub>OC</sub> ; low-current mode (default)								
2	OUT11_OC									
1	OUT10_OC									
0	OUT9_OC									

# 7.4.10 Control Register CR10 (0x0A)

Table 92. Control Register CR10

												- 3												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	DIAG_2	DIAG_1	DIAG_0			Res	serve	ed			SD	SOS	COPT_3	COPT_2	COPT_1	COPT_0	н-огтн-нісн	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0
Reset	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
Access		R/W																						

Table 93. CR10 signals description

		Table 93. CR10 signals description
Bit	Name	Description
23	DIAG_2	Drain-source monitoring threshold for external H-bridge
22	DIAG_1	000: V <sub>SCd1_HB</sub>
21	DIAG_0	- 001: V <sub>SCd2_HB</sub> 010: V <sub>SCd3_HB</sub> 011: V <sub>SCd4_HB</sub> 100: V <sub>SCd5_HB</sub> 101: V <sub>SCd6_HB</sub> 110: V <sub>SCd7_HB</sub> 111: V <sub>SCd7_HB</sub> (default)
20:14	Reserved	_
13	SD	Slow decay
12	SDS	Slow decay single
11	COPT_3	Cross current protection time
10	COPT_2	0000: not allowed
9	COPT_1	0001: tccp <sub>0001</sub> 0010: tccp <sub>0010</sub>
8	COPT_0	0011: tccp <sub>0011</sub> 0100: tccp <sub>0100</sub> 0101: tccp <sub>0110</sub> 0110: tccp <sub>0111</sub> 1000: tccp <sub>1000</sub> 1001: tccp <sub>1000</sub> 1001: tccp <sub>1001</sub> 1010: tccp <sub>1010</sub> 1011: tccp <sub>1011</sub> 1100: tccp <sub>1110</sub> 1111: tccp <sub>1111</sub> 1110: tccp <sub>1110</sub> 1111: tccp <sub>1111</sub> 1111: tccp <sub>1111</sub> (default)
7	H_OLTH_HIGH	H-bridge OL high threshold (5/6 * V <sub>S</sub> ) select
		_

Table 93. CR10 signals description (continued)

Bit	Name	Description
6	OL_H1L2	Test open-load condition between H1 and L2
5	OL_H2L1	Test open-load condition between H2 and L1
4	SLEW_4	
3	SLEW_3	Binary coded slew rate of H-bridge (bit0 = LSB; bit4 = MSB)
2	SLEW_2	00000: Control disabled (default)
1	SLEW_1	11111: I <sub>GHxmax</sub>
0	SLEW_0	

### 7.4.11 Control Register CR11 (0x0B)

### Table 94. Control Register CR11

												_												
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name											Re	serv	ed											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Access		R/W																						

### Table 95. CR11 signals description

Bit	Name	Description
23:0	Reserved	_

## 7.4.12 Control Register CR12 (0x0C)

### Table 96. Control Register CR12

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	PMW1_FREQ_1	PMW1_FREQ_0	PMW2_FREQ_1	PMW2_FREQ_0	PMW3_FREQ_1	PMW3_FREQ_0	PMW4_FREQ_1	PMW4_FREQ_0	PMW5_FREQ_1	PMW5_FREQ_0	PMW6_FREQ_1	PMW6_FREQ_0	PMW7_FREQ_1	PMW7_FREQ_0	PMW8_FREQ_1	PMW8_FREQ_0	PMW9_FREQ_1	PMW9_FREQ_0	PMW10_FREQ_1	PMW10_FREQ_0	F	Rese	erved	i
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

Table 97. CR12 signals description

Bit	Name	Description
23	PMW1_FREQ_1	Frequency of PWM channel PWM1
22	PMW1_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
21	PMW2_FREQ_1	Frequency of PWM channel PWM2
20	PMW2_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
19	PMW3_FREQ_1	Frequency of PWM channel PWM3
18	PMW3_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
17	PMW4_FREQ_1	Frequency of PWM channel PWM4
16	PMW4_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
15	PMW5_FREQ_1	Frequency of PWM channel PWM5
14	PMW5_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
13	PMW6_FREQ_1	Frequency of PWM channel PWM6
12	PMW6_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
11	PMW7_FREQ_1	Frequency of PWM channel PWM7
10	PMW7_FREQ_0	00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
9	PMW8_FREQ_1	Frequency of PWM channel PWM8
8	PMW8_FREQ_0	- 00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)

Table 97. CR12 signals description (continued)

Bit	Name	Description
7	PMW9_FREQ_1	Frequency of PWM channel PWM9
6	PMW9_FREQ_0	00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
5	PMW10_FREQ_1	Frequency of PWM channel PWM10
4	PMW10_FREQ_0	00: f <sub>PWMx</sub> (00) (default) 01: f <sub>PWMx</sub> (01) 10: f <sub>PWMx</sub> (10) 11: f <sub>PWMx</sub> (11)
3:0	Reserved	_

### 7.4.13 Control Register CR13 (0x0D) to CR17 (0x11)

Table 98. Control Register CR13 to CR17

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name		Keserved	PWMx_DC_9	PWMx_DC_8	PWMx_DC_7	PWMx_DC_6	PWMx_DC_5	PWMx_DC_4	PWMx_DC_3	PWMx_DC_2	PWMx_DC_1	PWMx_DC_0	boynood	חסא וספסעו	PWMy_DC_9	PWMy_DC_8	PWMy_DC_7	PWMy_DC_6	PWMy_DC_5	PWMy_DC_4	PWMy_DC_3	PWMy_DC_2	PWMy_DC_1	PWMy_DC_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

Where:

$$x = 1 + (z * 2), z = 0 to 4$$

$$y = 2 + (z * 2), z = 0 to 4$$

Table 99. CR13 to CR17 signals description

Bit	Name	Description
23:22	Reserved	_

Table 99. CR13 to CR17 signals description (continued)

Bit	Name	Description
21	PWMx_DC_9	
20	PWMx_DC_8	
19	PWMx_DC_7	
18	PWMx_DC_6	Binary coded on-dutycycle of PWM channel PWMx (bit12 = LSB; bit21 = MSB)
17	PWMx_DC_5	00 0000 0000: duty cycle 0% (default)
16	PWMx_DC_4	xx xxxx xxxx: duty cycle 100%/1023 x register value
15	PWMx_DC_3	11 1111 1111. duty cycle 100%
14	PWMx_DC_2	
13	PWMx_DC_1	
12	PWMx_DC_0	
11:10	Reserved	_
9	PWMy_DC_9	
8	PWMy_DC_8	
7	PWMy_DC_7	
6	PWMy_DC_6	Binary coded on-dutycycle of PWM channel PWMy (bit0 = LSB; bit9 = MSB)
5	PWMy_DC_5	00 0000 0000: duty cycle 0% (default) xx xxxx xxxx: duty cycle 100%/1023 x register value
4	PWMy_DC_4	11 1111 1111. Duty cycle 100%
3	PWMy_DC_3	Binary coded on-dutycycle of PWM channel PWMy
2	PWMy_DC_2	
1	PWMy_DC_1	
0	PWMy_DC_0	

### 7.4.14 Control Register CR18 (0x12) to CR22 (0x16)

Table 100. Control Register CR18

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	OUTx_AUTOCOMP_EN	OUTx_VLED_9	OUTx_VLED_8	OUTx_VLED_7	OUTx_VLED_6	OUTx_VLED_5	OUTx_VLED_4	OUTx_VLED_3	OUTx_VLED_2	OUTx_VLED_1	OUTX_VLED_0	Reserved	OUTy_AUTOCOMP_EN	OUTy_VLED_9	OUTy_VLED_8	OUTy_VLED_7	OUTy_VLED_6	OUTy_VLED_5	OUTy_VLED_4	OUTy_VLED_3	OUTy_VLED_2	OUTy_VLED_1	OUTy_VLED_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access		R/W																						

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Where:

x = 7 + (z \* 2), z = 0 to 4

y = 8 + (z \* 2), z = 0 to 4

Table 101. CR18 to CR22 signals description

Bit	Name	Description
23	Reserved	_
22	OUTx_AUTOCOMP_EN	Setting this bit to '1' enables the automatic V <sub>S</sub> compensation for OUTx
21	OUTx_VLED_9	
20	OUTx_VLED_8	
19	OUTx_VLED_7	
18	OUTx_VLED_6	Binary coded nominal LED voltage of OUTx (bit12 = LSB; bit21 = MSB)
17	OUTx_VLED_5	00 0000 0000: V <sub>LED</sub> = 0 V (default)
16	OUTx_VLED_4	xx xxxx xxxx: V <sub>LED</sub> = V <sub>AINVS</sub> /1023 x register value 01 1101 0000: V <sub>LED</sub> = V <sub>AINVS</sub>
15	OUTx_VLED_3	V <sub>LED</sub> is clamped at 10 V (0x1D0h)
14	OUTx_VLED_2	
13	OUTx_VLED_1	
12	OUTx_VLED_0	
11	Reserved	_
10	OUTy_AUTOCOMP_EN	Setting this bit to '1' enables the automatic V <sub>S</sub> compensation for OUTy
9	OUTy_VLED_9	
8	OUTy_VLED_8	
7	OUTy_VLED_7	
6	OUTy_VLED_6	Binary coded nominal LED voltage of OUTy (bit0 = LSB; bit9 = MSB)
5	OUTy_VLED_5	00 0000 0000: V <sub>LED</sub> = 0 V (default)
4	OUTy_VLED_4	xx xxxx xxxx: V <sub>LED</sub> = V <sub>AINVS</sub> /1023 x register value 01 1101 0000: V <sub>LED</sub> = V <sub>AINVS</sub>
3	OUTy_VLED_3	V <sub>LED</sub> is clamped at 10 V (0x1D0h)
2	OUTy_VLED_2	
1	OUTy_VLED_1	
0	OUTy_VLED_0	

## 7.4.15 Control Register CR34 (0x22)

### Table 102. Control Register CR34

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name		Reserved									CP_OFF	ICMP	WD_EN											
Reset	0											0	0	0	0	1								
Access		R/W																						

### Table 103. CR34 signals description

Bit	Name	Description
23:3	Reserved	_
2	CP_OFF	Charge pump control  0: Enabled; charge pump on in active mode (default)  1: Disabled; charge pump off in active mode  setting CP_OFF = 1 is only possible when CP_OFF_EN = 1
1	ICMP	V1 load current supervision  0: Enabled; Watchdog is disabled in V1 Standby when I <sub>v1</sub> < I <sub>CMP</sub> (default)  1: Disabled; watchdog is disabled upon transition into V1_standby mode setting ICMP = 1 is only possible when ICMP_config_en = 1
0	WD_EN	Watchdog Enable 0: Watchdog disabled 1: Watchdog enabled (default)

### 7.4.16 Configuration Register (0x3F)

#### Table 104. Configuration Register

							DIC		. •	<b>7</b> 11111	gui	utio		vg.	J.C.									
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WU_CONFIG	LIN_WU_CONFIG	LIN_HS_EN	TSD_CONFIG	Reserved	MQ	ICMP_CONFIG_EN	WD_CONFIG_EN	MASK_OL_HS1	MASK_OL_LS1	MASK_TW	Reserved	MASK_OL	MASK_SPIE	MASK_PLE	WASK_GW	CP_OFF_EN	CP_LOW_CONFIG	CP_DITH_DIS	FS_FORCED		Reserved		TRIG
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access		R/W																						

Table 105. CR signals description

Bit	Name	Description
23	WU_CONFIG	Configuration of input pin WU Input configured as wake-up input 0: WU configured as wake-up input 1: WU configured for input voltage measurement (default)
22	LIN_WU_CONFIG	Configuration of LIN wake-up behaviour  0: wake up at recessive - dominant - recessive with t <sub>dom</sub> > t <sub>dom_LIN</sub> (default) (according to LIN 2.2a and Hardware Requirements for Transceivers version 1.3)  1: wake up at recessive - dominant transition
21	LIN_HS_EN	Configuration of LIN transceiver bit rate 0: LIN transceiver in normal communication mode (20kbit/s) (default) 1: LIN transceiver in high speed mode for fast Flashing (115kbit/s)
20	TSD_CONFIG	Configuration of thermal shutdown behaviour  0: in case of TSD1 all power stages are switched off (default)  1: selective shut down of power stage cluster
19	Reserved	
18	DM	H-bridge configuration 0: single motor mode (default) 1: reserved
17	ICMP_CONFIG_EN	ICMP configuration Enable  0: writing ICMP = 1 is blocked (writing ICMP=0 is possible); (default)  1: writing ICMP = 1 is possible with next SPI command bit is automatically reset to 0 after next SPI command
16	WD_CONFIG_EN	Watchdog configuration Enable 0: writing to WD Configuration (CR2 [0:1] is blocked (default) 1: writing to WD Configuration Bits is possible with next SPI command bit is automatically reset to 0 after next SPI command
15	MASK_OL_HS1	Mask Open-load HS1 0: Open-load condition at HS1 is not masked (default) 1: Open-load condition at HS1 is masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
14	MASK_OL_LS1	Mask Open-load LS1 0: Open-load condition at LS1 is not masked (default) 1: Open-load condition at LS1 is masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
13	MASK_TW	Mask Thermal Warning 0: Thermal warning is not masked (default) 1: Thermal warning is masked i.e. it is reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)

Table 105. CR signals description (continued)

Table 105. CR signals description (continued)		
Bit	Name	Description
12	Reserved	_
11	MASK_OL	Mask open-load  0: Open-load condition at all outputs are not masked (default)  1: Open-load condition at all outputs are masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
10	MASK_SPIE	Mask SPI error 0: SPI errors are not masked (default) 1: SPI errors are masked i.e. reported as am SPI Error (GSB bit 5) but not as a Global Error (GSB bit 7)
9	MASK_PLE	Mask physical layer error 0: Physical Layer Errors are not masked (default) 1: Physical Layer Errors are masked i.e. reported as a Physical Layer Error (GSB bit 4) but not as a Global Error (GSB bit 7)
8	MASK_GW	Mask global warning 0: Global Warning conditions are not masked (default) 1: Global Warning conditions are masked i.e. reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)
7	CP_OFF_EN	Charge pump control enable  0: writing CP_OFF = 1 is blocked (writing CP OFF = 0 is possible); (default)  1: writing CP_OFF = 1 is possible with next SPI command  Bit is automatically reset to 0 after next SPI command
6	CP_LOW_CONFIG	Charge pump low configuration 0: CP_low (SR 2, bit 9) is latched and outputs are off until R&C (default) 1: CP_low (SR 2, bit 9) is a 'live' bit; outputs are re-activated automatically upon recovery of the charge pump output voltage
5	CP_DITH_DIS	Charge pump clock dithering 0: CP clock dithering is enabled; (default) 1: CP clock dithering is disabled
4	FS_FORCED	Force LSx_FSO ON LSx_FSO low-side outputs are forced ON (to allow diagnosis of the fail-safe path) 0: LSx_FSO outputs are controlled by the Fail-safe logic (default) 1: LSx_FSO outputs are forced ON and the device enters Fail-Safe mode; no NReset is generated
3:1	Reserved	

# 7.5 Status Registers

# 7.5.1 Status Register SR1 (0x31)

### Table 106. Status Register SR1 (0x31)

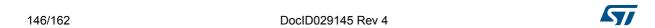
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	WU_STATE	Reserved	WU_WAKE	Reserved	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR
Access	R/C	R				R										R	/C							

### Table 107. SR1 signals description

Bit	Name	Description
23	Reserved	_
22	WU_STATE	State of WU input 0: input level is low 1: input level is high The bit shows the momentary status of WU and cannot be cleared ("Live bit") Note: The status is only valid if WU is configured as wake-up input in Configuration Register (0x3F). Otherwise this bit remains at his previous logic state.
21	Reserved	_
20	WU_WAKE	Wake-up by WU: shows wake up source  1: wake-up  Bits are latched until a "Read and clear" command
19	Reserved	_
18	WAKE_LIN	Wake-up by LIN: shows wake up source  1: wake-up  Bits are latched until a "Read and clear" command
17	WAKE_TIMER	Wake-up by Timer: shows wake up source  1: wake-up  Bits are latched until a "Read and clear" command
16	DEBUG_ACTIVE	Debug Mode Active: indicates Device is in Debug mode  1: Debug mode  The bit shows the momentary status and cannot be cleared ("Live bit")

Table 107. SR1 signals description (continued)

Bit	Name	Description
15	V1UV	Indicates undervoltage condition at voltage regulator V1 (V1 < V <sub>RTx</sub> )  1: undervoltage  Bit is latched until a "Read and clear" command
14	V1_RESTART_2	Indicates the number of TSD2 events which caused a restart of voltage
13	V1_RESTART_1	regulator V1 Bits cannot be cleared; counter will be cleared automatically if no additional
12	V1_RESTART_0	TSD2 event occurs within 1 minute.
11	WDFAIL_CNT_3	
10	WDFAIL_CNT_2	Indicates number of subsequent watchdog failures.
9	WDFAIL_CNT_1	Bits cannot be cleared; will be cleared with a valid watchdog trigger
8	WDFAIL CNT_0	
7	DEVICE_STATE_1	State from which the device woke up
6	DEVICE_STATE_0	<ul> <li>00: Active Mode after Read&amp;Clear command or after Flash Mode state</li> <li>01: Active mode after wake-up from V1_standby mode (before Read&amp;Clear command)</li> <li>10: Active Mode after Power-on or after wake-up from Vbat_standby Mode (before Read&amp;Clear command)</li> <li>11: Flash mode (LIN Flash mode)</li> <li>Bit is latched until a "Read and clear" command</li> <li>After a "read and clear access", the device state will be updated</li> </ul>
5	TSD2	Thermal Shutdown 2 was reached Bit is latched until a "Read and clear" command
4	TSD1	Thermal Shutdown 1 was reached (Logical Or combination of all TSD1_CLx; see status register SR6).  This bit cannot be cleared directly. It is reset if the corresponding TSD1_CLx bits in SR6 are cleared.
3	FORCED_SLEEP_ TSD2/V1SC	Device entered Forced Vbat_standby mode due to:  - Thermal shutdown or  - Short circuit on V1 during startup Bit is latched until a "Read and clear" command
2	FORCED_SLEEP_WD	Device entered Forced Vbat_standby mode due to multiple watchdog failures Bit is latched until a "Read and clear" command
1	WDFAIL	Watchdog failure Bit is latched until a "Read and clear" command
0	VPOR	V <sub>S</sub> Power-on Reset threshold (VPOR) reached Bit is latched until a "Read and clear" command



# 7.5.2 Status Register SR2 (0x32)

### Table 108. Status Register SR2 (0x32)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC		Res	erve	ed		DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	ML	V2SC	V2FAIL	V1FAIL	VSREG_EW	VSREG_OV	VSREG_UV	∧o⁻s∧	∧n⁻s∧
Access	R/C												R					R	/C					

### Table 109. SR2 signals description

Bit	Name	Description
23	LIN_PERM_DOM	LIN bus signal is dominant for t > t <sub>dom(bus)</sub> Bit is latched until a "Read and clear" command
22	LIN_TXD_DOM	TxDL pin is dominant for t > t <sub>dom(TXDL)</sub> The LIN transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command
21	LIN_PERM_REC	LIN bus signal does not follow TxDL within t <sub>LIN</sub> The LIN transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command
20:16	Reserved	
15	DSMON_HS2	
14	DSMON_HS1	Drain-Source Monitoring '1' indicates a short-circuit or open-load condition was detected
13	DSMON_LS2	Bit is latched until a "Read and clear" command
12	DSMON_LS1	
11	SPI_INV_CMD	Invalid SPI command '1' indicates one of the following conditions was detected:  - access to undefined address  - Write operation to Status Register  - DI stuck at '0' or '1'  - CSN timeout  - Parity failure  - invalid or undefined setting The SPI frame is ignored Bit is latched until a "Read and clear" command
10	SPI_SCK_CNT	SPI clock counter '1' indicates an SPI frame with wrong number of CLK cycles was detected Bit is latched until a valid SPI frame
9	CP_LOW	Charge pump voltage low '1' indicates that the charge pump voltage is too low Bit is latched until a "Read and clear" command

Table 109. SR2 signals description (continued)

Bit	Name	Description
8	TW	Thermal warning '1' indicates the temperature has reached the thermal warning threshold (logical OR combination of bits TW_CLx in SR6) Bit is latched until a "Read and clear" command
7	V2SC	V2 short circuit detection '1' indicates a short circuit to GND condition of V2 at turn-on of the regulator (V2 < V2_fail for t > $t_{v2\_short}$ ) Bit is latched until a "Read and clear" command
6	V2FAIL	V2 failure detection '1' indicates a V2 fail event occurred since last readout (V2 < V2_fail for t > $t_{v2\_fail}$ ) Bit is latched until a "Read and clear" command
5	V1FAIL	V1 failure detection '1' indicates a V1 fail event occurred since last readout (V1 < V1_fail for t > t <sub>V1_fail</sub> ) Bit is latched until a "Read and clear" command
4	VSREG_EW	V <sub>SREG</sub> early warning '1' indicates the voltage at V <sub>SREG</sub> has reached the early warning threshold (configured in CR3) In Active mode, an interrupt pulse is generated at NINT Bit is latched until a "Read and clear" command. Bit needs a "Read and clear" command after wake-up from standby modes
3	VSREG_OV	V <sub>SREG</sub> overvoltage '1' indicates the voltage at V <sub>SREG</sub> has reached the overvoltage threshold Bit is latched until a "Read and clear" command
2	VSREG_UV	V <sub>SREG</sub> undervoltage '1' indicates the voltage at V <sub>SREG</sub> has reached the undervoltage threshold Bit is latched until a "Read and clear" command
1	VS_OV	$\rm V_S$ overvoltage '1' indicates the voltage at $\rm V_S$ has reached the overvoltage threshold Bit is latched until a "Read and clear" command
0	VS_UV	$\rm V_S$ undervoltage '1' indicates the voltage at $\rm V_S$ has reached the undervoltage threshold Bit is latched until a "Read and clear" command

# 7.5.3 Status Register SR3 (0x33)

Table 110. Status Register SR3 (0x33)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OC_TH_EX	OUT1_LS_OC_TH_EX		Reser	ved		OUT4_HS_OC_TH_EX	OUT4_LS_OC_TH_EX	OUT5_HS_OC_TH_EX	OUT5_LS_OC_TH_EX	OUT6_HS_OC_TH_EX	OUT6_LS_OC_TH_EX	OUT7_OC_TH_EX	OUT8_OC_TH_EX	OUT9_OC	OUT10_OC	OUT11_OC	OUT12_OC	OUT13_OC	OUT14_OC	OUT15_OC	OUTHS_OC_TH_EX	LS2FSO_OC	LS1FSO_OC
Access		R/C																						

Table 111. SR3 signals description

		able 111. One signals description
Bit	Name	Description
23	OUT1_HS_OC_TH_EX	Overcurrent shutdown
22	OUT1_LS_OC_TH_EX	'1' indicates the output was shut down due to overcurrent condition.  If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):  Bit is set upon overcurrent condition and output is turned off.  If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):  In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1'  In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):  Bit is set after thermal expiration and output is turned off  Bit is latched until a "Read and clear" command
21:18	Reserved	_
17	OUT4_HS_OC_TH_EX	Overcurrent shutdown
16	OUT4_LS_OC_TH_EX	'1' indicates the output was shut down due to overcurrent condition.
15	OUT5_HS_OC_TH_EX	If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):  Bit is set upon overcurrent condition and output is turned off.
14	OUT5_LS_OC_TH_EX	If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):
13	OUT6_HS_OC_TH_EX	In case of overcurrent condition this bit is not set. The output goes into
12	OUT6_LS_OC_TH_EX	Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1' In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):
11	OUT7_OC_TH_EX	Bit is set after thermal expiration and output is turned off
10	OUT8_OC_TH_EX	Bit is latched until a "Read and clear" command

Table 111. SR3 signals description (continued)

Bit	Name	Description
9	OUT9_OC	
8	OUT10_OC	
7	OUT11_OC	Overcurrent shutdown
6	OUT12_OC	'1' indicates the output was shut down due to overcurrent condition.
5	OUT13_OC	Bit is latched until a "Read and clear" command
4	OUT14_OC	
3	OUT15_OC	
2	OUTHS_OC_TH_EX	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition.  If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0):  Bit is set upon overcurrent condition and output is turned off.  If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1):  In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1'  In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1):  Bit is set after thermal expiration and output is turned off  Bit is latched until a "Read and clear" command
1	LS2FSO_OC	Overcurrent shutdown
0	LS1FSO_OC	'1' indicates the output was shut down due to overcurrent condition. Bit is latched until a "Read and clear" command

## 7.5.4 Status Register SR4 (0x34)

Table 112. Status Register SR4 (0x34)

											3													
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OCR_ALERT	OUT1_LS_OCR_ALERT		Resei	rved		OUT4_HS_OCR_ALERT	OUT4_LS_OCR_ALERT	OUT5_HS_OCR_ALERT	OUT5_LS_OCR_ALERT	OUT6_HS_OCR_ALERT	OUT6_LS_OCR_ALERT	OUT7_OCR_ALERT	OUT8_OCR_ALERT			Re	serv	ed .			OUTHS_OCR_ALERT	Reserved	>
Access				R											R/C				R	R/	C			

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Table 113. SR4 signals description

Bit	Name	Description
23	OUT1_HS_OCR_ALERT	Autorecovery Alert
22	OUT1_LS_OCR_ALERT	'1' indicates that the output reached the overcurrent threshold and is in autorecovery mode Bit is not latched and cannot be cleared.
21:18	Reserved	_
17	OUT4_HS_OCR_ALERT	
16	OUT4_LS_OCR_ALERT	
15	OUT5_HS_OCR_ALERT	Autorecovery Alert
14	OUT5_LS_OCR_ALERT	'1' indicates that the output reached the overcurrent threshold and is in
13	OUT6_HS_OCR_ALERT	autorecovery mode
12	OUT6_LS_OCR_ALERT	Bit is not latched and cannot be cleared.
11	OUT7_OCR_ALERT	
10	OUT8_OCR_ALERT	
9:3	Reserved	_
2	OUTHS_OCR_ALERT	Autorecovery Alert '1' indicates that the output reached the overcurrent threshold and is in autorecovery mode Bit is not latched and cannot be cleared.
1:0	Reserved	_

# 7.5.5 Status Register SR5 (0x35)

#### Table 114. Status Register SR5 (0x35)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OL	OUT1_LS_OL		Reser	ved		OUT4_HS_OL	OUT4_LS_OL	OUT5_HS_OL	OUT5_LS_OL	OUT6_HS_OL	OUT6_LS_OL	OUT7_OL	OUT8_OL	OUT9_OL	OUT10_OL	OUT11_OL	OUT12_OL	OUT13_OL	OUT14_OL	OUT15_OL	OUTHS_OL	Doynoso	>
Access												R/C												

#### Table 115. SR5 signals description

Bit	Name	Description
23	OUT1_HS_OL	Open-load
22	OUT1_LS_OL	'1' indicates an open-load condition was detected at the output Bit is latched until a "Read and clear" command
21:18	Reserved	_

Table 115. SR5 signals description (continued)

Bit	Name	Description
17	OUT4_HS_OL	
16	OUT4_LS_OL	
15	OUT5_HS_OL	
14	OUT5_LS_OL	
13	OUT6_HS_OL	
12	OUT6_LS_OL	
11	OUT7_OL	
10	OUT8_OL	Open-load '1' indicates an open-load condition was detected at the output
9	OUT9_OL	Bit is latched until a "Read and clear" command
8	OUT10_OL	
7	OUT11_OL	
6	OUT12_OL	
5	OUT13_OL	
4	OUT14_OL	
3	OUT15_OL	
2	OUTHS_OL	
1:0	Reserved	

## 7.5.6 Status Register SR6 (0x36)

Table 116. Status Register SR6 (0x36)

														•										
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WD_TIMER_STATE_1	WD_TIMER_STATE_0			R	eser	ved				TW_CL6	TW_CL5	TW_CL4	LW_CL3	TW_CL2	TW_CL1	700	עפאפו	TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1
Access	F	?		R/C																				

Table 117. SR6 signals description

Bit	Name	Description
23	WD_TIMER_STATE_1	Watchdog timer status
22	WD_TIMER_STATE_0	00: 0 - 33% 01: 33 - 66% 11: 66 - 100%

Table 117. SR6 signals description (continued)

Bit	Name	Description
21:14	Reserved	_
13	TW_CL6	
12	TW_CL5	
11	TW_CL4	Thermal warning for Cluster x
10	TW_CL3	'1' indicates Cluster x has reached the thermal warning threshold Bit is latched until a "Read and clear" command
9	TW_CL2	
8	TW_CL1	
7:6	Reserved	_
5	TSD1_CL6	
4	TSD1_CL5	Thermal shutdown of Cluster x
3	TSD1_CL4	'1' indicates Cluster x has reached the thermal shutdown threshold (TSD1) and
2	TSD1_CL3	the output cluster was shut down
1	TSD1_CL2	Bit is latched until a "Read and clear" command
0	TSD1_CL1	

## 7.5.7 Status Register SR7 (0x37) to SR9 (0x39)

Table 118. Status Register SR7 (0x37) to SR9 (0x39)

									٠ ٦			•		•		•		,						
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Peserved	•	TEMP_CLx_9	TEMP_CLx_8	TEMP_CLx_7	TEMP_CLx_6	TEMP_CLx_5	TEMP_CLx_4	TEMP_CLx_3	TEMP_CLx_2	TEMP_CLx_1	TEMP_CLx_0	beynesed		TEMP_CLy_9	TEMP_CLy_8	TEMP_CLy_7	TEMP_CLy_6	TEMP_CLy_5	TEMP_CLy_4	TEMP_CLy_3	TEMP_CLy_2	TEMP_CLy_1	TEMP_CLy_0
Access	R/	С			•		R						R	/C					F	₹				

Where:

$$x = 2 + (z * 2), z = 0 to 2$$

$$y = 1 + (z * 2), z = 0 to 2$$

Table 119. SR7 to SR9 signals description

Bit	Name	Description
23:22	Reserved	_

Table 119. SR7 to SR9 signals description (continued)

Bit	Name	Description								
21	TEMP_CLx_9									
20	TEMP_CLx_8									
19	TEMP_CLx_7									
18	TEMP_CLx_6									
17	TEMP_CLx_5	Temperature Cluster x: Binary coded voltage of temperature diode for cluster x (bit12 = LSB; bit21 = MSB) (see Section 4.31: Thermal clusters)								
16	TEMP_CLx_4	Bits cannot be cleared.								
15	TEMP_CLx_3									
14	TEMP_CLx_2									
13	TEMP_CLx_1									
12	TEMP_CLx_0									
11:10	Reserved	_								
9	TEMP_CLy_9									
8	TEMP_CLy_8									
7	TEMP_CLy_7									
6	TEMP_CLy_6									
5	TEMP_CLy_5	Temperature Cluster y: binary coded voltage of temperature diode for cluster y (bit0 = LSB; bit9 = MSB) (see Section 4.31: Thermal clusters)								
4	TEMP_CLy_4	Bits cannot be cleared.								
3	TEMP_CLy_3									
2	TEMP_CLy_2									
1	TEMP_CLy_1									
0	TEMP_CLy_0									

## 7.5.8 Status Register SR10 (0x3A)

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#### Table 120. Status Register SR10 (0x3A)

					-						· • •			,	,	,								
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		VSREG_9	VSREG_8	VSREG_7	VSREG_6	VSREG_5	VSREG_4	VSREG_3	VSREG_2	VSREG_1	VSREG_0					ı	Rese	erve	d				
Access	R/	С					R					R/C												

### Table 121. SR10 signals description

Bit	Name	Description
23:22	Reserved	_



Table 121. SR10 signals description (continued)

Bit	Name	Description
21	VSREG_9	
20	VSREG_8	
19	VSREG_7	
18	VSREG_6	Binary coded voltage at V <sub>SREG</sub> pin (bit12 = LSB; bit21 = MSB)
17	VSREG_5	00 0000 0000: 0V
16	VSREG_4	xx xxxx xxxx: V <sub>AINVS</sub> /1023 x register value 11 1111 1111: V <sub>AINVS</sub>
15	VSREG_3	Bits cannot be cleared.
14	VSREG_2	
13	VSREG_1	
12	VSREG_0	
11:0	Reserved	_

# 7.5.9 Status Register SR11 (0x3B)

Table 122. Status Register SR11 (0x3B)

										_	- 3			,		,								
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		6 <sup>-</sup> S/	8_SV	VS_7	9 <sup>-</sup> S/	VS_5	VS_4	VS_3	VS_2	VS_1	0 <sup>-</sup> S/	Doynood	>	6 <sup>-</sup> NMN	8_UWV	7_UWV	9_UWV	VWU_5	VWU_4	vwu_3	VWU_2	1_UWV	0_UWV
Access	R/	С					R						R	/C					F	٦ _				

Table 123. SR11 signals description

Bit	Name	Description	
23:22	Reserved	_	
21	VS_9		
20	VS_8		
19	VS_7		
18	VS_6	Binary coded voltage at $V_S$ pin (bit12 = LSB; bit21 = MSB) 00 0000 0000: 0V xx xxxxx xxxx: $V_{AINVS}/1023$ x register value 11 1111 1111: $V_{AINVS}$ Bits cannot be cleared.	
17	VS_5		
16	VS_4		
15	VS_3		
14	VS_2		
13	VS_1		
12	VS_0		
11:10	Reserved	_	

Table 123. SR11 signals description (continued)

Bit	Name	Description
9	VWU_9	
8	VWU_8	
7	VWU_7	
6	VWU_6	Binary coded voltage at WU pin (bit0 = LSB; bit9 = MSB)
5	VWU_5	00 0000 0000: 0V xx xxxx xxxx: V <sub>AINVS</sub> /1023 x register value 11 1111 1111: V <sub>AINVS</sub> Bits cannot be cleared.
4	VWU_4	
3	VWU_3	
2	VWU_2	
1	VWU_1	
0	VWU_0	

L99DZ120 Package information

#### **Package information** 8

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

#### LQFP-64 package information 8.1

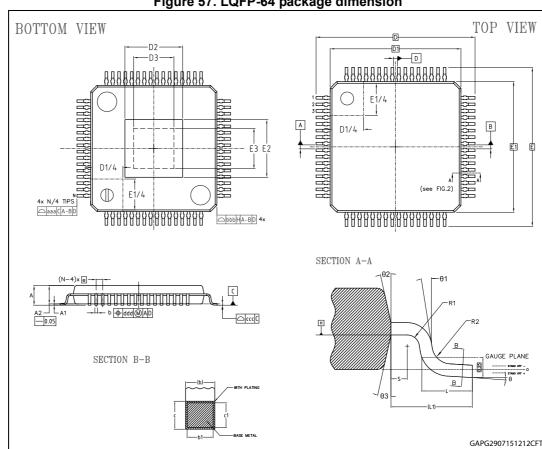


Figure 57. LQFP-64 package dimension

Table 124. LQFP-64 mechanical data

Symbol	Millimeters		
Symbol	Min.	Тур.	Max.
Θ	0°	3.5°	6°
Θ1	0°	9°	12°
Θ2	11°	12°	13°
Θ3	11°	12°	13°

Package information L99DZ120

Table 124. LQFP-64 mechanical data (continued)

Millimeters			
Min.	Тур.	Max.	
		1.60	
0.05		0.15	
1.35	1.40	1.45	
		0.27	
0.17	0.20	0.23	
0.09		0.20	
0.09	0.127	0.16	
12.00 BSC			
10.00 BSC			
		6.85	
5.7			
0.50 BSC			
12.00 BSC			
10.00 BSC			
		4.79	
3.3			
0.45	0.60	0.75	
1.00			
64			
0.08			
0.08		0.20	
0.20			
Tolerance of fo	orm and position		
	0.20		
0.20			
0.08			
0.08			
	0.05 1.35 0.17 0.09 0.09 5.7 5.7 0.08 0.08 0.08	Min. Typ.  0.05 1.35 1.40  0.17 0.20 0.09 0.09 0.127 12.00 BSC 10.00 BSC  5.7  0.50 BSC 12.00 BSC 10.00 BSC  1	

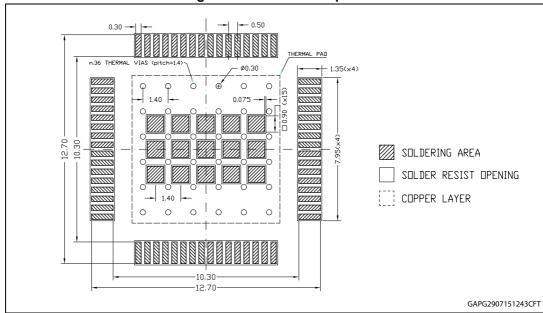


Figure 58. LQFP-64 footprint

## 8.2 LQFP-64 marking information

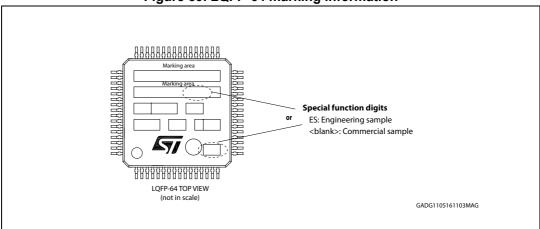


Figure 59. LQFP-64 marking information

Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Order code L99DZ120

# 9 Order code

Table 125. Device summary

Package	Order codes		
rackage	Tray	Tape and reel	
LQFP-64 epad	L99DZ120	L99DZ120-TR	

L99DZ120 Revision history

# 10 Revision history

Table 126. Document revision history

Date	Revision	Changes
27-Apr-2016	1	Initial release.
11-May-2016	2	Updated Section 3.3.1: LQFP64 thermal data Updated Table 19 Updated Table 21 Updated Table 39 Updated Figure 59 Updated Section 4.14: Auto-recovery alert and thermal expiration Updated Section 4.22: Programmable soft-start function to drive loads with higher inrush current Updated Figure 43 Updated Table 113
12-Sep-2016	3	Updated Table 28
22-Nov-2016	4	Added AEC-Q100 qualified in Features. Updated Table 3: ESD protection, Added Section 3.4.12: Over Current Recovery settings Updated Section 4.22: Programmable soft-start function to drive loads with higher inrush current Added Table 17: Half bridges (OUT1, OUT4, OUT5 and OUT6) OCR timing parameters and Table 18: High-side (OUT7, OUT8 and OUT_HS) OCR timing parameters Updated Table 19: Current monitoring Updated Table 109: SR2 signals description Updated Table 123: SR11 signals description

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