

## General Description

The MIC1232 is a low-current microprocessor supervisor for monitoring 5V systems. The device features logic selectable (TOL) reset thresholds of 5% or 10% of 5V; a pushbutton reset input (/PBRST); a watchdog timer with three-state selectable (TD) timeout periods of 150ms, 600ms, or 1.2s; a fixed reset timeout period of 250ms (min); and active-low open-drain reset (/RST) and active-high push-pull reset (RST) outputs. The /RST output maintains a valid reset condition for  $V_{CC}$  as low as 1.4V.

The MIC1232 asserts a reset condition if the supply voltage drops below the reset threshold, the pushbutton reset is asserted low, or the watchdog timer does not see a high-to-low transition on the watchdog timer input within the watchdog timer period. A reset condition is held for the reset timeout period of 250ms (min) after the pushbutton input is released or after the supply voltage increases above the reset threshold voltage.

The MIC1232 is a drop-in replacement for the DS1232, MAX1232, and TC1232. It consumes a low 18 $\mu$ A (typ) of supply current, 40 $\mu$ A (max). This is one-tenth the max current of the DS1232, and one-quarter the max current of the MAX1232 and TC1232. It operates over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range and is available in the Pb-Free 8-pin SOIC and PDIP packages.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

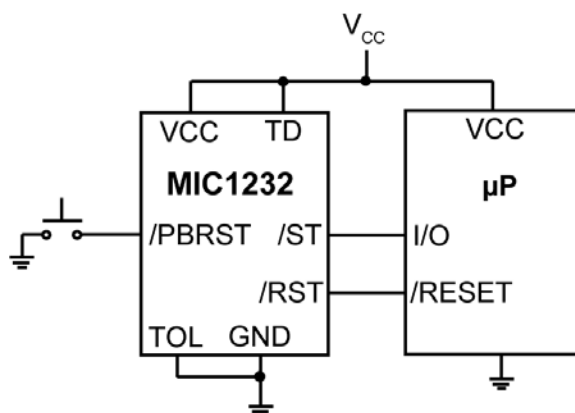
## Features

- Low-current version of DS1232/MAX1232/TC1232/CAT1232
- Low current: 18 $\mu$ A (typ), 40 $\mu$ A (max)
- Selectable threshold (TOL): 5% or 10% of 5V
- Selectable watchdog timer (TD): 150ms, 600ms, 1.2s
- Power OK/Reset time delay: 250ms (min)
- Debounced pushbutton reset input (/PBRST)
- Dual complementary reset outputs
  - Active-low, open-drain reset output
  - Active-high, push-pull reset output
- Available in Pb-Free 8-pin SOIC and PDIP packages
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range
- Pin-for-Pin compatible with MIC1832/DS1832/CAT1832

## Applications

- Automotive systems
- Intelligent systems
- Critical microprocessor power monitoring
- Battery powered computers
- Controllers

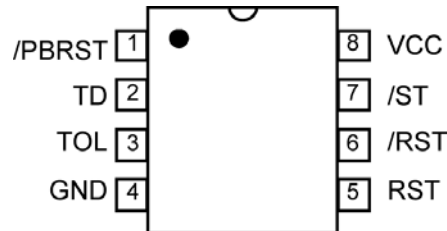
## Typical Application



## Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC1232NY	-40° to +85°C	8-Pin PDIP	Pb-Free
MIC1232MY	-40° to +85°C	8-Pin SOIC	Pb-Free

## Pin Configuration



8-Pin PDIP  
8-Pin SOIC

## Pin Description

Pin Number	Pin Name	Pin Function
1	/PBRST	Pushbutton Reset input: This input is debounced and can be driven with external logic signals or by using a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the /PBRST pin are ignored; any pulse with a duration of 20ms or greater is guaranteed to cause a reset.
2	TD	Time Delay input: This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a normal value of 150ms. When TD = open, the watchdog timeout period is set to a nominal value of 600ms. When TD = V <sub>CC</sub> , the watchdog period is 1.2s nominally.
3	TOL	Tolerance Select input: This input selects whether 5% or 10% of V <sub>CC</sub> is used as the reset threshold voltage. When TOL = 0V, the 5% tolerance level is selected and when TOL = V <sub>CC</sub> , a 10% tolerance level is selected.
4	GND	IC ground pin, 0V reference.
5	RST	RST is asserted high if either V <sub>CC</sub> goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after V <sub>CC</sub> exceeds the reset threshold, after the watch times out, or after /PBRST goes high.
6	/RST	/RST is asserted low if either V <sub>CC</sub> goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. /RST remains asserted for one reset timeout period after V <sub>CC</sub> exceeds the reset threshold, after the watch times out, or after /PBRST goes high. Open-drain output.
7	/ST	Input to watchdog timer. If /ST does not see a transition from high to low within the watchdog timeout period, RST and /RST will be asserted.
8	VCC	Primary supply input, +5V.

**Absolute Maximum Ratings<sup>(1)</sup>**

Terminal Voltage	
$V_{CC}$ .....	-0.3V to +6.0V
All other inputs .....	-0.3V to ( $V_{CC} + 0.3V$ )
Input Current	
$V_{CC}$ .....	250mA
GND, all other inputs .....	25mA
Lead Temperature (soldering, 10sec.) .....	300°C
Storage Temperature ( $T_s$ ) .....	-65°C to 150°C
ESD Rating <sup>(3)</sup> .....	see Note 3

**Operating Ratings<sup>(2)</sup>**

Operating Temperature Range	
MIC1232M/N .....	-40°C to +85°C

**Electrical Characteristics**

$V_{CC} = 4.5\text{ V to }5.5\text{V}$ ;  $T_A = \text{Operating Temperature Range}$ ; **bold** values indicate  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless noted.

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range	$V_{CC}$	4.5		5.5	V
Supply Current	$I_{CC}$ <sup>(4)</sup>		18	<b>40</b>	$\mu\text{A}$
/ST and /PBRST Input Levels	$V_{IH}$ <sup>(5)</sup>	<b>2.0</b>		<b><math>V_{CC} + 0.3</math></b>	V
	$V_{IL}$	<b>-0.3</b>		<b>0.8</b>	V
Input Leakage	$I_{IL}$			<b><math>\pm 1</math></b>	$\mu\text{A}$
Output Source Current, RST	$V_{OH} = 2.4V$	<b>1.0</b>	10		mA
Output Sink Current, /RST, RST	$V_{OL} = 0.4V$	<b>2.0</b>	10		mA
$V_{CC}$ 5% Trip Point (Reset Threshold Voltage)	TOL = GND	<b>4.5</b>	4.62	<b>4.74</b>	V
$V_{CC}$ 10% Trip Point (Reset Threshold Voltage)	TOL = $V_{CC}$	<b>4.25</b>	4.37	<b>4.49</b>	V
Input Capacitance, /ST, TOL	$C_{IN}$ <sup>(6)</sup>			5	pF
Output Capacitance, /RST, RST	$C_{OUT}$ <sup>(6)</sup>			7	pF

**Notes:**

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
- $I_{CC}$  is measured with outputs open and inputs within 0.5V of supply rails.
- /PBRST has an internal pull-up resistor to  $V_{CC}$  (typ. 40k $\Omega$ ).
- Guaranteed by design.

## AC Electrical Characteristics

$V_{IN} = 4.5V$  to  $5.5V$ ;  $T_A$  = Operating Temperature Range; **bold** values indicate  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Parameter	Condition	Min	Typ	Max	Units
/PBRST Min. Pulse Width, $t_{PB}$	/PBRST = $V_{IL}^{(1)}$	<b>20</b>			ms
/PBRST Delay, $t_{PBD}$		<b>1</b>	4	<b>20</b>	ms
Reset Active Time, $t_{RST}$		<b>250</b>	610	<b>1000</b>	ms
/ST Pulse Width, $t_{ST}$		<b>20</b>			ns
/ST Timeout Period, $t_{TD}$	TD = 0V	<b>62.5</b>	150	<b>250</b>	ms
	TD = Open	<b>250</b>	600	<b>1000</b>	ms
	TD = $V_{CC}$	<b>500</b>	1200	<b>2000</b>	ms
$V_{CC}$ Fall Time, $t_F$		<b>10</b>			$\mu s$
$V_{CC}$ Rise Time, $t_R$		<b>0</b>			ns
$V_{CC}$ Detect to /RST Low and RST High, $t_{RPD}$	$V_{CC}$ Falling <sup>(2)</sup>		50	<b>150</b>	$\mu s$
$V_{CC}$ Detect to /RST Low and RST Low, $t_{RPD}$	$V_{CC}$ Falling <sup>(3)</sup>	<b>250</b>	610	<b>1000</b>	ms

### Notes:

1. /PBRST must be held low for a minimum of 20ms to guarantee a reset.
2.  $V_{CC}$  falling at  $1.66mV/\mu s$ .
3. /RST has an open drain output

## Timing Diagrams

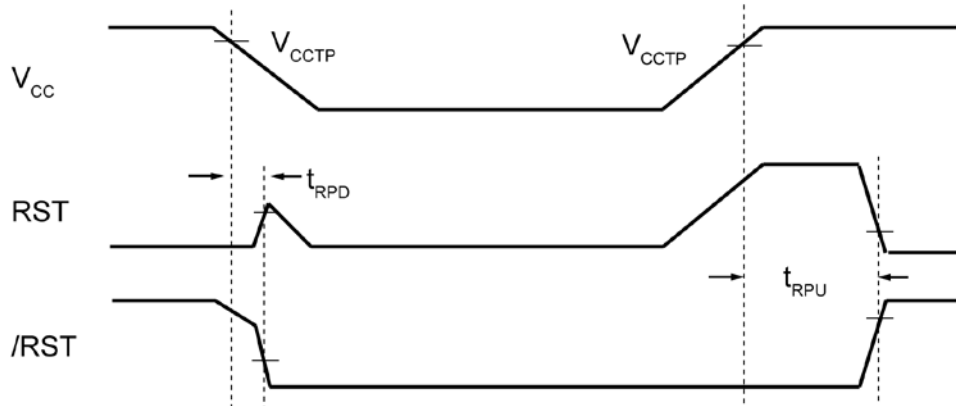


Figure 1. Power-Up/Power-Down Sequence

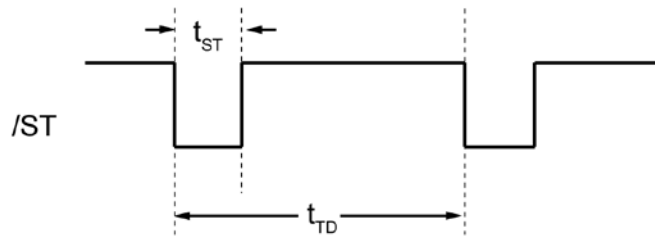


Figure 2. Watchdog Input

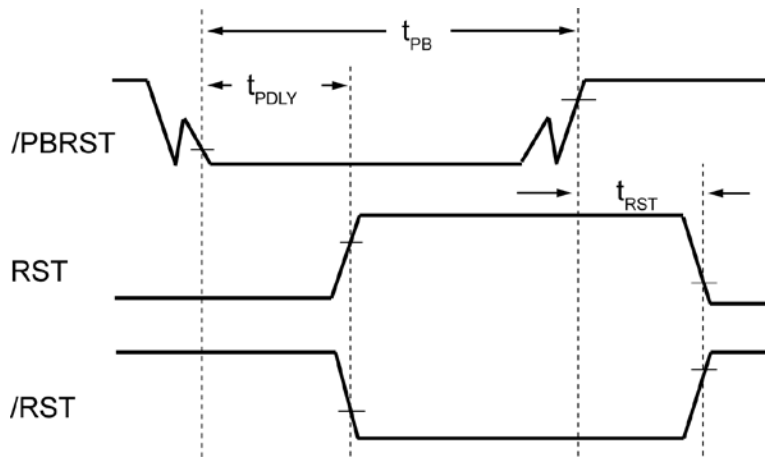


Figure 3. Pushbutton Reset

## Application Information

### Power Monitor

The /RST and RST pins are asserted whenever  $V_{CC}$  falls below the reset threshold voltage determined by the TOL pin. A 5% tolerance level (4.62V reset threshold voltage) can be selected by connecting the TOL pin to ground. A 10% tolerance level can be selected by connecting the TOL pin to  $V_{CC}$ . The reset pins will remain asserted for a period of 250ms after  $V_{CC}$  has risen above the reset threshold voltage. The reset function ensures that the microprocessor is properly reset and powers up into a known condition after a power failure. /RST will remain valid with  $V_{CC}$  as low as 1.4V.

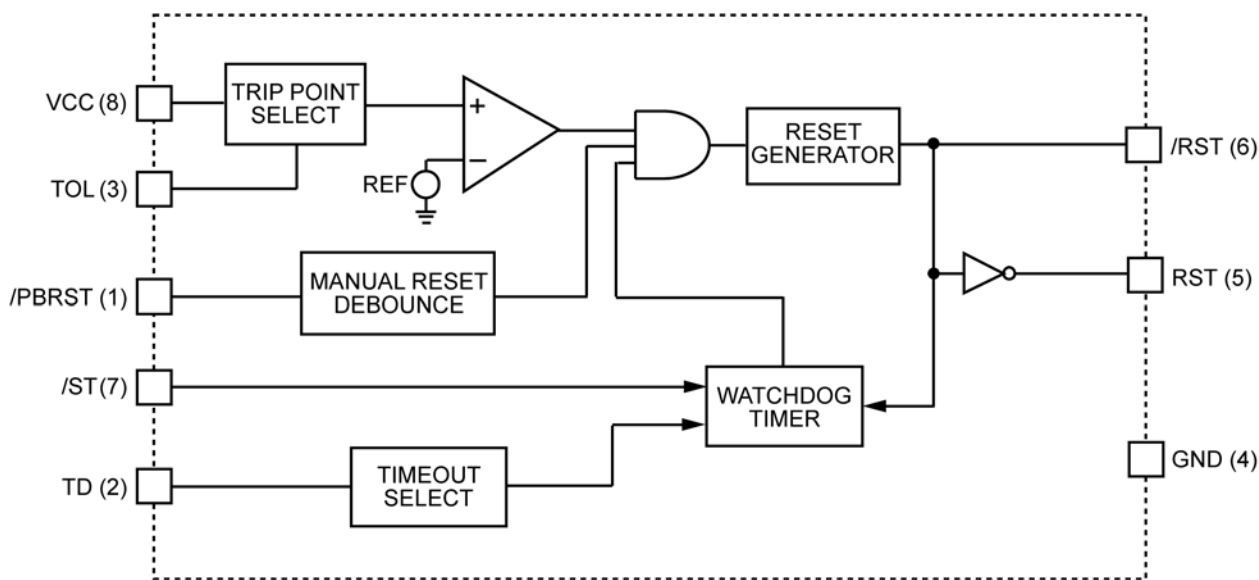
### Watchdog Timer

The microprocessor can be mounted by connecting the /ST pin (watchdog input) to a bus line or I/O line. If a high-to-low does not occur on the /ST pin within the watchdog timeout period determined by the TD pin (see the Electrical Characteristics Table), the /RST and the RST will remain asserted for 250ms. A minimum pulse of 20ns or any transition high-to-low on the /ST pin resets the watchdog timer. The watchdog timer is reset if /ST sees a valid transition within the watchdog timeout period.

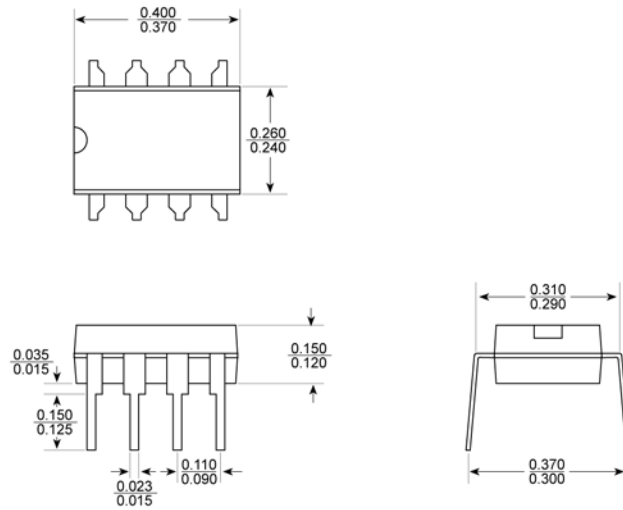
### Pushbutton Reset Input

The /PBRST input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The /PBRST input recognizes any pulse that is 20ms or longer in duration and ignores all pulses that are less than 1ms in duration.

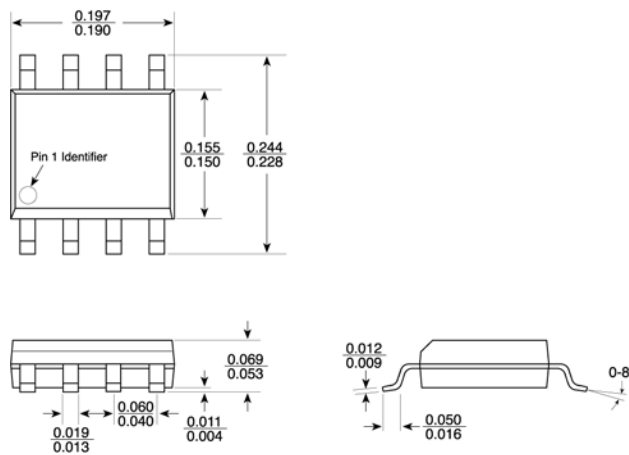
## Block Diagram



## Package Information<sup>(1)</sup>



**8-Pin DIP (N)**



**8-Pin SOIC (M)**

**Note:**

1. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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