

NL17SZU04

Single Unbuffered Inverter

The NL17SZU04 is a single unbuffered inverter in two tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

Features

- Tiny SOT-353 and SOT-553 Packages
- Source/Sink ± 16 mA at 4.5 V V_{CC}
- Over-Voltage Tolerant Inputs and Outputs
- Pin For Pin with NC7SZU04P5X, TC7SZU04FU and TC7SZU04AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

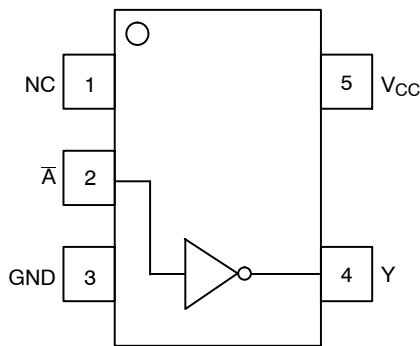


Figure 1. Pinout (Top View)

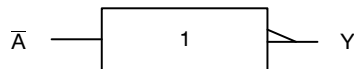


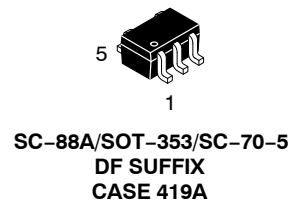
Figure 2. Logic Symbol



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<http://onsemi.com>

MARKING DIAGRAMS



L6 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(*Note: Microdot may be in either location)

PIN ASSIGNMENT

Pin	Function
1	NC
2	\bar{A}
3	GND
4	Y
5	V_{CC}

FUNCTION TABLE

Input	Output $Y = \bar{A}$
A	Y
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current	-50	mA
I _{OK}	DC Output Diode Current	-50	mA
I _{OUT}	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance SC-88A/SOT-353 (Note 1) SOT-553	350 496	°C/W
P _D	Power Dissipation in Still Air at 85°C SC-88A/SOT-353 SOT-553	186 135	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	Class IC Class A N/A	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
3. Tested to EIA/JESD22-A115-A, rated to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V _{CC}	DC Supply Voltage (Operating) Data Retention Only	1.65 1.5	5.5 5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	5.5	V
T _A	Operating Temperature Range	-40	+85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.0 V ±0.3 V V _{CC} = 5.0 V ±0.5 V	0 0	100 20	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.85	0.85 V _{CC}			0.85 V _{CC}		V
			2.3 to 5.5	0.8 V _{CC}			0.8 V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65 to 1.85			0.15 V _{CC}		0.15 V _{CC}	V
			2.3 to 5.5			0.2 V _{CC}		0.2 V _{CC}	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OH} = -100 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -3 mA	1.65	1.29	1.52		1.29		
		I _{OH} = -4 mA	2.3	1.9	2.1		1.9		
		I _{OH} = -6 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -8 mA	3.0	2.4	2.7		2.4		
		I _{OH} = -12 mA	3.0	2.3	2.5		2.3		
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{OH}	I _{OL} = 100 μA	1.65 to 5.5			0.1		0.1	V
		I _{OL} = 3 mA	1.65		0.08		0.24		
		I _{OL} = 4 mA	2.3		0.20		0.3		
		I _{OL} = 6 mA	2.7		0.22		0.4		
		I _{OL} = 8 mA	3.0		0.28		0.4		
		I _{OL} = 12 mA	3.0		0.38		0.55		
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C		-40°C ≤ T _A ≤ 85°C		Units
				Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.8 ± 0.15	1.0	11.7	1.0	12.1	ns
		R _L = 1 MΩ, C _L = 15 pF	2.5 ± 0.2	0.8	6.2	0.8	6.5	
		R _L = 1 MΩ, C _L = 15 pF	3.3 ± 0.3	0.5	4.5	0.5	4.8	
		R _L = 500 Ω, C _L = 50 pF		1.0	6.0	1.0	6.5	
		R _L = 1 MΩ, C _L = 15 pF	5.0 ± 0.5	0.5	3.9	0.5	1.0	
		R _L = 500 Ω, C _L = 50 pF		0.8	5.0	0.8	5.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	6.5	pF
		10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	10	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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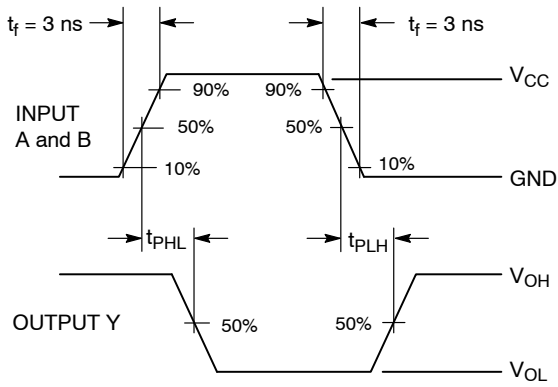
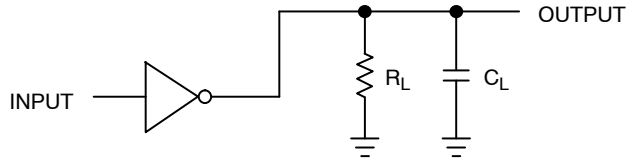


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping [†]
NL17SZU04DFT2G	SC-88A/SOT-353/SC-70-5 (Pb-Free)	3000 / Tape & Reel
NLV17SZU04DFT2G*	SC-88A/SOT-353/SC-70-5 (Pb-Free)	3000 / Tape & Reel
NL17SZU04XV5T2G	SOT-553 (Pb-Free)	4000 / Tape & Reel

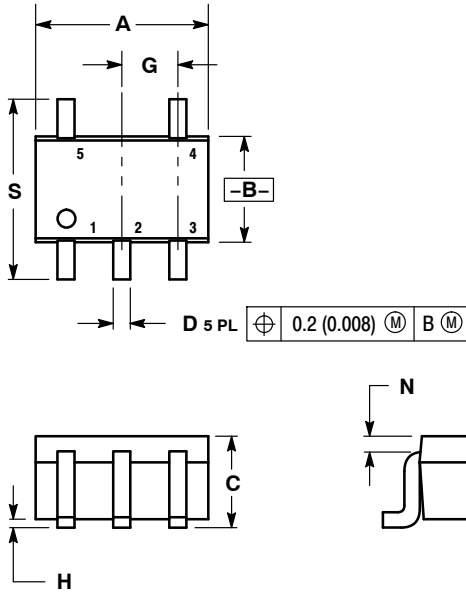
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

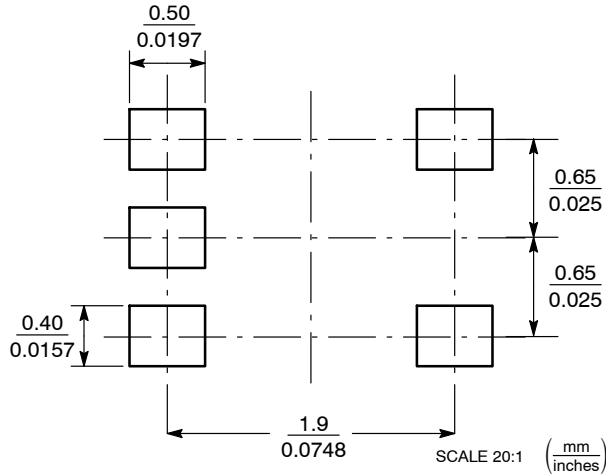


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT*

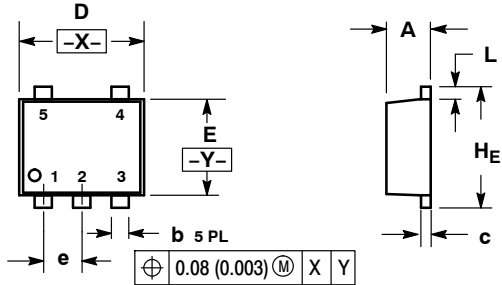


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOT-553
XV5 SUFFIX
CASE 463B
ISSUE B

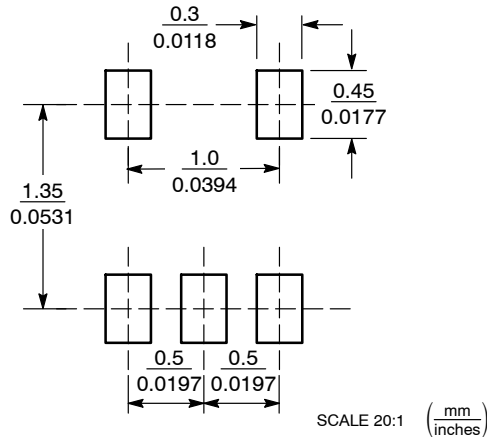


- STYLE 1:
 PIN 1. BASE 1
 2. EMITTER 1/2
 3. BASE 2
 4. COLLECTOR 2
 5. COLLECTOR 1
- STYLE 2:
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. CATHODE
 5. CATHODE


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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