L99PM62GXP



Power management IC with LIN and high speed CAN

Features

- Two 5V voltage regulators for microcontroller and peripheral supply
- No electrolytic capacitor required on regulator outputs
- Ultra low quiescent current in standby modes
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog and fail safe output
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Advanced HS CAN transceiver (ISO 11898-2/-5 and SAE J2284 compliant) with local failure and bus failure diagnosis
- HS CAN transceiver supports partial networking
- Complete 3-channel contact monitoring interface with programmable cyclic sense functionality
- Programmable periodic system wake-up feature
- ST SPI interface for mode control and diagnosis
- 5 fully protected high-side drivers with internal 4-channel PWM generator
- 2 low-side drivers with active Zener clamping
- 4 internal PWM timers
- 2 operational amplifiers with rail-to-rail outputs (V_S) and low voltage inputs
- Temperature warning and thermal shutdown

Applications

 Automotive ECU's such as door zone and body control modules



Description

The L99PM62GXP is a power management system IC that provides electronic control units with enhanced system power supply functionality, including various standby modes, as well as LIN and HS CAN physical communication layers. The device's two low-drop voltage regulators supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability.

In addition, five high-side drivers, two low-side drivers and two operational amplifiers increase the system integration level.

The ST standard SPI interface (3.0) allows control and diagnosis of the device and enables generic software development.

Table 1. Device summary

Package	Order codes	
Package	Tube	Tape and reel
PowerSSO-36	L99PM62GXP	L99PM62GXPTR

Contents L99PM62GXP

Contents

1	Bloc	k diagra	am and pin descriptions	9
2	Deta	iled des	scription	12
	2.1	Voltage	e regulators	12
		2.1.1	Voltage regulator: V ₁	12
		2.1.2	Voltage regulator: V ₂	13
		2.1.3	Increased output current capability for voltage regulator $V_2 \ \dots$	13
		2.1.4	Voltage regulator failure	15
		2.1.5	Voltage regulator behaviour	16
	2.2	Opera	ting modes	16
		2.2.1	Active mode	16
		2.2.2	Flash mode	17
		2.2.3	V1 standby mode	17
		2.2.4	VBAT standby mode	18
		2.2.5	Wake up from standby modes	18
		2.2.6	Wake-up inputs	19
		2.2.7	Cyclic contact supply	19
		2.2.8	Timer interrupt / wake-up of microcontroller by timer	19
	2.3	Function	onal overview (truth table)	20
	2.4	Config	urable window watchdog	21
		2.4.1	Change watchdog timing	23
	2.5	Fail sa	ıfe mode	25
		2.5.1	Single failures	25
		2.5.2	Multiple failures – entering forced V _{BAT} standby mode	27
	2.6	Reset	output (NRESET)	28
	2.7	Opera	tional amplifiers	28
	2.8		is interface	
		2.8.1	Error handling	
		2.8.2	Wake up (from LIN)	
		2.8.3	LIN pull-up	
	2.9		peed CAN bus transceiver	
		2.9.1	CAN error handling	
		2.9.2	Wake up (from CAN)	
		~		

L99PM62GXP Contents

2.9.4 CAN receive only mode 2.9.5 CAN looping mode 2.9.5 CAN looping mode 2.10 Serial peripheral interface (ST SPI standard) 3 Protection and diagnosis 3.1 Power supply fail 3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.1.2 Vs undervoltage 3.3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver					
2.9.5 CAN looping mode 2.10 Serial peripheral interface (ST SPI standard) 3 Protection and diagnosis 3.1 Power supply fail 3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver			2.9.3	CAN sleep mode	33
2.10 Serial peripheral interface (ST SPI standard) 3 Protection and diagnosis 3.1 Power supply fail 3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.1.2 Vs undervoltage 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.4.1 PowerSSO-36 thermal data 5.5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			2.9.4	CAN receive only mode	33
3.1 Power supply fail 3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.1.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.4.1 PowerSSO-36 thermal data 5.5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			2.9.5	CAN looping mode	33
3.1 Power supply fail 3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.1.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		2.10	Serial p	peripheral interface (ST SPI standard)	. 33
3.1.1 V _S overvoltage 3.1.2 Vs undervoltage 3.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver	3	Prote	ection a	nd diagnosis	. 35
3.1.2 Vs undervoltage 3.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.6.6 Reset output 5.7 Watchdog 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		3.1	Power	supply fail	. 35
3.2 Temperature warning and thermal shutdown 3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			3.1.1	V _S overvoltage	35
3.3 High-side driver outputs 3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver			3.1.2	Vs undervoltage	35
3.4 Low-side driver outputs REL1, REL2 3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		3.2	Temper	rature warning and thermal shutdown	. 37
3.5 SPI diagnosis 4 Typical application 5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		3.3	High-si	de driver outputs	. 38
Flectrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		3.4	Low-sic	de driver outputs REL1, REL2	. 39
5 Electrical specifications 5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver		3.5	SPI dia	gnosis	. 40
5.1 Absolute maximum rating 5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver	4	Туріс	al appli	cation	. 41
5.2 ESD protection 5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver	5	Elect	rical sp	ecifications	. 42
5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		5.1	Absolut	te maximum rating	. 42
5.3 Thermal data 5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		5.2	ESD pr	otection	. 43
5.4 Package and PCB thermal data 5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		5.3	•		
5.4.1 PowerSSO-36 thermal data 5.5 Electrical characteristics 5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		5.4			
5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver				PowerSSO-36 thermal data	
5.5.1 Supply and supply monitoring 5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver		5.5	Electric		
5.5.2 Oscillator 5.5.3 Power-on reset (VS) 5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver				Supply and supply monitoring	
5.5.4 Voltage regulator V ₁ 5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			5.5.2	Oscillator	
5.5.5 Voltage regulator V ₂ 5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			5.5.3	Power-on reset (VS)	49
5.5.6 Reset output 5.5.7 Watchdog 5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			5.5.4	Voltage regulator V ₁	49
5.5.7 Watchdog			5.5.5	Voltage regulator V ₂	50
5.5.8 High-side outputs 5.5.9 Relay drivers 5.5.10 Wake up inputs (WU1 WU3) 5.5.11 High speed CAN transceiver 5.5.12 LIN transceiver			5.5.6	Reset output	51
5.5.9 Relay drivers			5.5.7	Watchdog	51
5.5.10 Wake up inputs (WU1 WU3)			5.5.8	High-side outputs	53
5.5.11 High speed CAN transceiver			5.5.9	Relay drivers	54
5.5.12 LIN transceiver			5.5.10	Wake up inputs (WU1 WU3)	55
			5.5.11	High speed CAN transceiver	55
5.5.13 Operational amplifier			5.5.12	LIN transceiver	58
			5.5.13	Operational amplifier	61

Pack 7.1 7.2	6.2.2 6.2.3 age and ECOPA	Control registers Status registers d packing information ACK® SSO-36 package information	93 99
	6.2.2 6.2.3 age and	Status registers	93
Pack	6.2.2 6.2.3	Status registers	93
	6.2.2		
	6.2.1	Overview	79
6.2	SPI reg	gisters	79
	6.1.11	Read device information	77
	6.1.10	Read and clear status operation	
	6.1.9	Format of data shifted out at SDO during read cycle	75
	6.1.8	Read operation	74
	6.1.7	Format of data shifted out at SDO during write cycle	73
	6.1.6	Write operation	72
	6.1.5	Address mapping	72
	6.1.4	Configuration register	70
	6.1.3	Global status register	70
	6.1.2	Operating code definition	69
	6.1.1	General description	69
6.1	SPI co	mmunication flow	69
ST S	PI		69
	5.5.15	Inputs TxD_C and TxD_L for Flash mode	65
	5.5.14	SPI	
	6.1	5.5.15 ST SPI 6.1 SPI co 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8 6.1.9 6.1.10 6.1.11	5.5.15 Inputs TxD_C and TxD_L for Flash mode ST SPI 6.1 SPI communication flow 6.1.1 General description 6.1.2 Operating code definition 6.1.3 Global status register 6.1.4 Configuration register 6.1.5 Address mapping 6.1.6 Write operation 6.1.7 Format of data shifted out at SDO during write cycle 6.1.8 Read operation 6.1.9 Format of data shifted out at SDO during read cycle 6.1.10 Read and clear status operation 6.1.11 Read device information 6.2 SPI registers

L99PM62GXP List of tables

List of tables

Table 1.	Device summary	1
Table 2.	Pin definition	10
Table 3.	Wake up sources	18
Table 4.	Functional overview (truth table)	20
Table 5.	Fail safe conditions and exit modes	
Table 6.	Persisting fail safe conditions and exit modes	
Table 7.	PWM configuration for high-side outputs	
Table 8.	Absolute maximum rating	
Table 9.	ESD protection	
Table 10.	Operating junction temperature	
Table 11.	Temperature warning and thermal shutdown	
Table 12.	Thermal parameter	
Table 13.	Supply and supply monitoring	
Table 14.	Oscillator	
Table 15.	Power-on reset (Vs)	
Table 16.	Voltage regulator V ₁	
Table 17.	Voltage regulator V ₂	
Table 18.	Reset output	
Table 19.	Watchdog	
Table 20.	Output (OUT_HS)	
Table 21.	Outputs (OUT14)	
Table 22.	Relay drivers	
Table 23.	Wake up inputs (WU1 WU3)	
Table 24.	CAN communication operating range	
Table 25.	CAN transmit data input: pin TXDC	
Table 26.	CAN receive data output: pin RXDC	
Table 27.	CAN bus common mode stabilization output termination: pin SPLIT	
Table 28.	CAN transmitter and receiver: pins CANH and CANL	
Table 29.	CAN transceiver timing	
Table 30.	LIN transmit data input: pin TXD	
Table 31.	LIN receive data output: pin RXD	
Table 32.	LIN transmitter and receiver: pin LIN	
Table 33.	LIN transceiver timing	
Table 34.	LIN pull-up: pin LINPÜ	
Table 35.	Operational amplifier	
Table 36.	Input: CSN	
Table 37.	Input CLK, DI	
Table 38.	DI timing	
Table 39.	DO output pin	
Table 40.	DO timing	
Table 41.	CSN timing	
Table 42.	RXDL/NINT timing	
Table 43.	Inputs TxD_C and TxD_L for Flash mode	
Table 44.	Command byte	
Table 45.	Operating code definition	
Table 46.	Global status register	
Table 47.	Configuration register	
Table 48.	Address mapping	

Table 49.	Write command format: command byte	72
Table 50.	Write command format: data byte 1	73
Table 51.	Write command format: data byte 2	73
Table 52.	Format of data shifted out at SDO during write cycle: global status register	73
Table 53.	Format of data shifted out at SDO during write cycle: data byte 1	73
Table 54.	Format of data shifted out at SDO during write cycle: data byte 2	73
Table 55.	Read command format: command byte	74
Table 56.	Read command format: data byte 1	
Table 57.	Read command format: data byte 2	74
Table 58.	Format of data shifted out at SDO during read cycle: global status register	75
Table 59.	Format of data shifted out at SDO during read cycle: data byte 1	75
Table 60.	Format of data shifted out at SDO during read cycle: data byte 2	75
Table 61.	Read and clear status command format: command byte	76
Table 62.	Read and clear status command format: data byte 1	76
Table 63.	Read and clear status command format: data byte 2	76
Table 64.	Format of data shifted out at SDO during read and clear status: global status register	76
Table 65.	Format of data shifted out at SDO during read and clear status: data byte 1	76
Table 66.	Format of data shifted out at SDO during read and clear status: data byte 2	77
Table 67.	Read device information	77
Table 68.	ID-header	78
Table 69.	Family identifier	78
Table 70.	Silicon version identifier	78
Table 71.	SPI-frame-ID	79
Table 72.	SPI register: command byte	79
Table 73.	SPI register: mode selection	79
Table 74.	SPI register: CTRL register selection	
Table 75.	SPI register: STAT register selection	80
Table 76.	Overview of control registers data bytes	
Table 77.	Control register 1: command and data bytes	
Table 78.	Control register 1, data bytes	
Table 79.	Control register 1, bits	
Table 80.	Control register 2: command and data bytes	
Table 81.	Control register 2, data bytes	
Table 82.	Control register 2, bits	
Table 83.	Control register 3: command data bytes	
Table 84.	Control register 3, data bytes	
Table 85.	Control register 3, bits	
Table 86.	Control register 4: command and data bytes	
Table 87.	Control register 4, data bytes	
Table 88.	Control register 4, bits	
Table 89.	Control register 5: command and data bytes	
Table 90.	Control register 5, data bytes	
Table 91.	Control register 5, bits	
Table 92.	Control register 6: command and data bytes	
Table 93.	Control register 6, data bytes	
Table 94.	Control register 6, bits	
Table 95.	Overview of status register data bytes	
Table 96.	Global status register	
Table 97.	Status register 1: command and data bytes	
Table 98.	Status register 1, data bytes	
Table 99.	Status register 1, bits	
Table 100	Status register 2: command and data bytes	96

577

L99PM62GXP List of tables

Table 101.	Status register 2, data bytes	96
Table 102.	Status register 2, bits	96
Table 103.	Status register 3: command and data bytes	97
Table 104.	Status register 3, data bytes	97
Table 105.	Status register 3, bits	97
Table 106.	PowerSSO-36 mechanical data	100
Table 107.	Document revision history	101

List of figures L99PM62GXP

List of figures

Figure 1.	Block diagram	. 9
Figure 2.	Pin connection (top view)	
Figure 3.	Voltage source with external PNP	
Figure 4.	Voltage source with external PNP and current limitation	13
Figure 5.	Voltage source with external NPN	14
Figure 6.	Voltage source with external NPN and current limitation	14
Figure 7.	Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down	
	conditions	16
Figure 8.	Operating modes	21
Figure 9.	Watchdog in normal operating mode (no errors)	22
Figure 10.	Watchdog with error conditions	
Figure 11.	Watchdog in Flash mode	
Figure 12.	Change watchdog timing within long open window	24
Figure 13.	Change watchdog timing within window mode	24
Figure 14.	General procedure to change watchdog timing out of fail safe mode	
Figure 15.	Change watchdog timing out of fail safe mode (watchdog failure)	
Figure 16.	Example: exit fail safe mode from watchdog failure	
Figure 17.	LIN master node configuration using LIN_PU (optional)	
Figure 18.	CAN wake up capabilities	32
Figure 19.	Over voltage and under voltage protection and diagnosis	36
Figure 20.	Thermal shutdown protection and diagnosis	
Figure 21.	Phase shifted PWM	
Figure 22.	Typical application diagram	
Figure 23.	Thermal data of PowerSSO-36	
Figure 24.	PowerSSO-36 PC board	
Figure 25.	PowerSSO-36 Thermal Resistance junction to ambient vs PCB copper area (V1 ON)	46
Figure 26.	PowerSSO-36 Thermal Impedance junction to ambient vs PCB copper area (single	
	pulse with V1 ON)	
Figure 27.	PowerSSO-36 thermal fitting model (V1 ON)	
Figure 28.	Watchdog timing (long, early, late and safe window)	
Figure 29.	Watchdog early, late and safe windows	
Figure 30.	LIN transmit, receive timing	
Figure 31.	SPI – transfer timing diagram	
Figure 32.	SPI - input timing	
Figure 33.	SPI output timing (part 1)	
Figure 34.	SPI output timing (part 2)	68
Figure 35.	SPI – CSN low to high transition and global status bit access	68
Figure 36.	Read configuration register ⁽¹⁾	71
Figure 37.		
Figure 38.	Format of data shifted out at SDO during write cycle	
Figure 39.	Format of data shifted out at SDO during read cycle	
Figure 40.	Format of data shifted out at SDO during read and clear status operation	
Figure 41.	PowerSSO-36 package dimensions	99

8/102 Doc ID 17639 Rev 4

Block diagram and pin descriptions 1



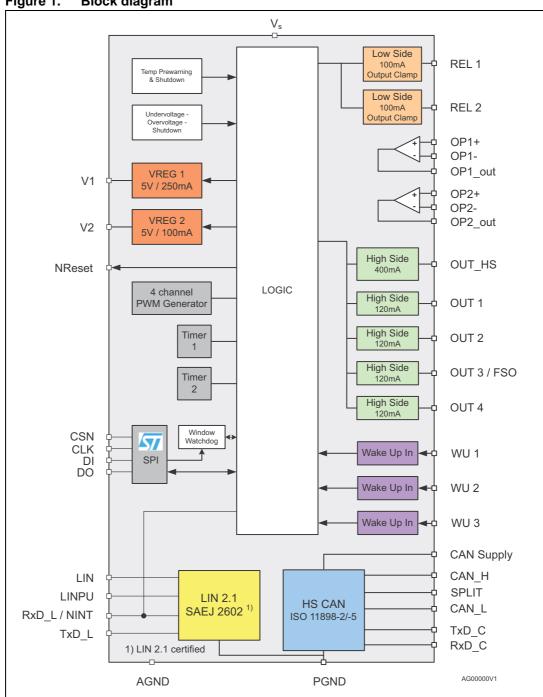


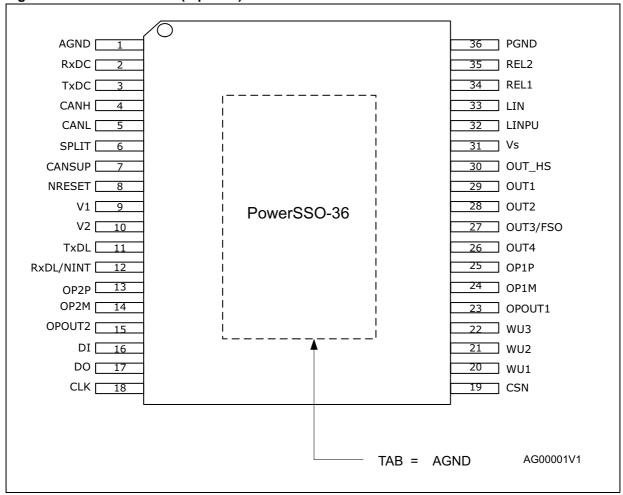
Table 2. Pin definition

Pin	Symbol	Function		
1	AGND	Analog ground		
2	RxDC	CAN receive data output		
3	TxDC	CAN transmit data input		
4	CANH	CAN high level voltage I/O		
5	CANL	CAN low level voltage I/O		
6	SPLIT	CAN reference voltage output, CAN termination		
7	CANSUP	CAN supply input; to allow external CAN supply from V ₁ or V ₂ regulator.		
8	NRESET	NReset output to micro controller; Internal pull-up of typical 100 K Ω (reset state = LOW)		
9	V ₁	Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver		
10	V ₂	Voltage regulator 2 output: 5 V supply for external loads (IR receiver, potentiometer, sensors) or CAN Transceiver. V_2 is protected against reverse supply.		
11	TxDL	LIN Transmit data input		
12	RxDL/NINT	RxDL -> LIN receive data output NINT -> indicates local/remote wake-up events or provides a programmable timer interrupt signal		
13	OP2+	Non inverting input of operational amplifier 2		
14	OP2-	Inverting input of operational amplifier 2		
15	OP2_OUT	Output of operational amplifier 2		
16	DI	SPI: serial data input		
17	DO	SPI: serial data output		
18	CLK	SPI: serial clock input		
19	CSN	SPI: chip select not input		
2022	WU13	Wake-up Inputs 1to 3: Input pins for static or cyclic monitoring of external contacts		
23	OP1_OUT	Output of operational amplifier 1		
24	OP1-	Inverting input of operational amplifier 1		
25	OP1+	Non inverting input of operational amplifier 1		
26	OUT4	High-side driver output (7 Ω , typ)		
27	OUT3/FSO	Configurable as high-side driver output (7 Ω , typ) or fail safe output pin (default)		
28	OUT2	High-side driver output (7 Ω , typ)		
29	OUT1	High-side driver output (7 Ω , typ)		
30	OUT_HS	High-side driver (1 Ω , typ)		
31	V_S	Power supply voltage		
32	LINPU	High-side driver output to switch off LIN master pull up resistor		
33	LIN	LIN bus line		
34	REL1	Low-side driver output (2 Ω typ)		

Table 2. Pin definition (continued)

Pin	Symbol	Function	
35	REL2	Low-side driver output (2 Ω typ)	
36	PGND	Power ground (REL1/2, LIN and CAN GND), to be externally connected to AGND	

Figure 2. Pin connection (top view)



Note: It is recommended to connect the PGND and AGND pins directly to the TAB.

2 Detailed description

2.1 Voltage regulators

The L99PM62GXP contains two independent and fully protected low drop voltage regulators, which are designed for very fast transient response and don't require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors \geq 220 nF.

2.1.1 Voltage regulator: V₁

The V_1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current and is mainly intended for supply of the system microcontroller. The V_1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode.

It can be used to supply the internal HS CAN Transceiver via the CANSUP pin externally. In case of a short circuit condition on the CAN bus, the output current of the transmitter is limited to 100 mA and the transceiver is turned off in order to ensure continued supply of the microcontroller.

In addition the regulator V_1 drives the L99PM62GXP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors \geq 220 nF.

If the device temperature exceeds the TSD1 threshold, all outputs (OUTx, RELx, V_2 , LIN) is deactivated except V_1 . Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2>TSD1), also V_1 is deactivated (see state chart in *Chapter 3: Protection and diagnosis*). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1sec. During this time, all other wake up sources (CAN, LIN, WU1 to3 and wake up of μ C by timer) are disabled. After 1 sec, the voltage regulator tries to restart automatically. If the restart fails 7 times, within one minute, without clearing and thermal shutdown condition still exists, the L99PM62GXP enters the forced V_{BAT} standby Mode.

In case of short to GND at " V_1 " after initial turn on (V_1 < 2V for t > $t_{V1short}$) the L99PM62GXP enters the forced V_{BAT} standby Mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..3 or periodic wake by timer (see Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer).

2.1.2 Voltage regulator: V₂

The voltage regulator V_2 can supply additional 5 V loads (e.g. logic components or the integrated HS CAN transceiver or external loads such as sensors or potentiometers). The maximum continuous load current is 100 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.1.3 Increased output current capability for voltage regulator V₂

For applications which require high output currents, the output current capability of the regulator can be increased my means of the integrated operational amplifiers and an external pass transistor.

Figure 3. Voltage source with external PNP

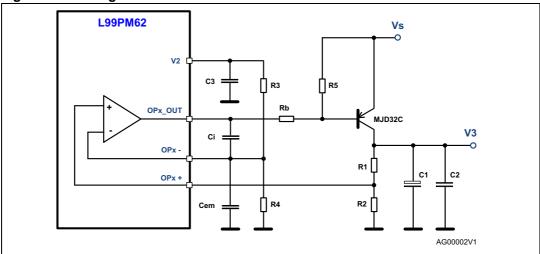


Figure 4. Voltage source with external PNP and current limitation

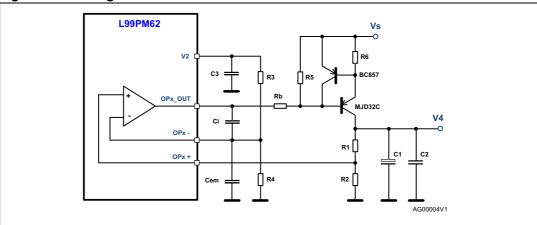


Figure 3 shows a possible configuration with a PNP pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3.

The Vs operating range for this circuit is 5.5 V to 18 V. It is important the respect the input common mode range specified for the operational amplifiers.

The output voltage V3 can be calculated using the following formula:

$$v_3 = \frac{v_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 4* provides additional current limitation using an additional PNP transistor and R6 which allows setting the current limit.

Figure 5. Voltage source with external NPN

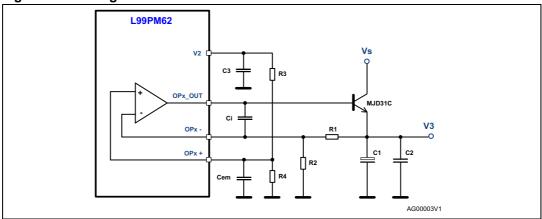


Figure 6. Voltage source with external NPN and current limitation

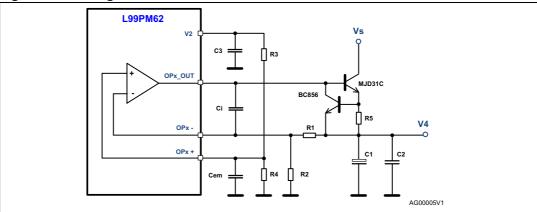


Figure 5 shows a possible configuration with an NPN pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3. This circuit requires fewer components compared to the configuration in Figure 3 but has a limited V_S operating range (6 V to 18 V).

The output voltage V3 can be calculated using the following formula:

$$v_3 = \frac{v_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 6* provides additional current limitation using an additional NPN transistor and R5 which allows setting the current limit.

14/102 Doc ID 17639 Rev 4

Alternatively, voltage regulator 1 can be used to provide the 5 V reference for this topology. However, the additional current consumption through R3 and R4 has to be considered in V_1 standby mode.

2.1.4 Voltage regulator failure

The V₁ and V₂ regulator output voltages are monitored.

In case of a drop below the $V_{1,}$ V_{2} – fail thresholds ($V_{1,2}$ < 2 V, typ for t > 2 μ s), the $V_{1,2}$ -fail bits are latched. The fail bits can be cleared by a dedicated SPI command.

Short to ground detection

If 4 ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for $V_{1,2}$), the L99PM62GXP identifies a short circuit condition at the related regulator output and the regulator is switched off.

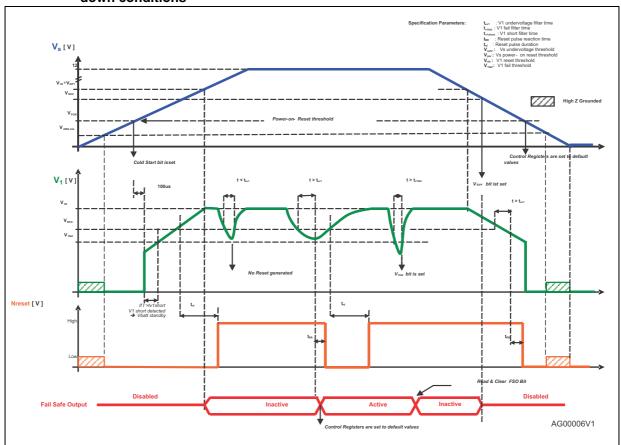
In case of V_1 short to GND failure the device enters V_{BAT} standby mode automatically. Bits Forced V_{BAT} STD2/SHT V_1 and V_1 fail were set.

In case of a V₂ short to GND failure the V₂short and V₂ fail bit is set.

If the output voltage of the corresponding regulator once exceeded the $V_{1,2}$ fail thresholds the short to ground detection is disabled. If a short to ground condition occurs the regulator outputs switches off due to thermal shutdown (V_1 at TSD2; V_2 at TSD1).

2.1.5 Voltage regulator behaviour

Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions



2.2 Operating modes

The L99PM62GXP can be operated in 4 different operating modes:

- Active
- Flash
- V₁ standby
- V_{BAT} standby

A cyclic monitoring of wake-up inputs and a periodic interrupt/wake-up by timer is available in standby modes.

2.2.1 Active mode

All functions are available and the device is controlled by the ST SPI Interface.

2.2.2 Flash mode

To program the system microcontroller, the L99PM62 can be operated in Flash mode where the internal watchdog is disabled. This mode can also be used for software debugging.

Except for the disabled watchdog, the Flash mode is identical to active mode and all device features are available.

A transition from Flash mode to V_{1stby} or V_{batstby} is not possible.

The mode can be entered if one of the following conditions is applied:

- V_{TxDL} ≥ V_{Flash}
- $V_{TxDC} \ge V_{Flash}$

At exit from Flash mode ($V_{TxD} < V_{Flash}$) no NReset pulse is generated and the watchdog starts with a long open window.

Note: Setting both TxDL and TxDC to high voltage levels (> V_{Flash}) is not allowed.

Communication at the respective TxD pin is not possible.

2.2.3 V₁ standby mode

The transition from active mode to V₁ standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 (V_1) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the I_{cmp} current threshold. At this transition, the L99PM62 also deactivates the internal watchdog.

Relay outputs, LIN and CAN transmitters is switched off in V_1 standby mode. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

A cyclic supply of external contacts and a synchronized monitoring of the contact state can be activated and configured by SPI.

In V₁ standby mode various wake up sources can be individually programmed. Each wake up event puts the device into active mode and forces the RxDL/NINT pin to a low level indicating the wake-up condition to the microcontroller.

After power ON reset (POR) all wake up sources are activated by default except the periodic interrupt/wake timer.

With the interrupt timer the micro controller can be forced from 'stop' to 'run' after a programmable period. The RxDL/NINT pin is forced low after the timer is elapsed. The L99PM62GXP enters active mode and is awaiting a valid watchdog trigger.

Both internal timers can be used for this feature.

The interrupt timer (T_{INT}) at pin RxDL/NINT is only available in V₁ standby mode.

Note: Inputs TxDL, TxDC and CSN must be at high level or at high impedance in order to achieve minimum standby current in V₁ standby mode.

Inputs DI and CLK must be at GND or at high impedance to achieve minimum standby current in V_1 standby mode.

Interrupt

The interrupt signal (linked to RxDL/NINT internally) indicates a wake-up event from V_1 standby mode. In case of a wake-up by Wake-up Inputs, activity on LIN or CAN, SPI access or timer-interrupt the NINT pin is pulled low for 56 μ s.

In case of V_1 standby mode and $(I_{V1} > I_{cmp})$, the device remains in standby mode, the V_1 regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

2.2.4 V_{BAT} standby mode

The transition from active mode to V_{BAT} standby mode is initiated by an SPI command.

In V_{BAT} standby mode, the V_1 voltage regulator, relay outputs, LIN and CAN transmitters are switched off. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

In V_{BAT} standby mode the current consumption of the L99PM62GXP is reduced to a minimum level.

Note:

Inputs TXDL, TXDC and CSN must be terminated to GND in V_{BAT} standby to achieve minimum standby current.

This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V_1 is pulled to GND).

2.2.5 Wake up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 3. Wake up sources

Wake up source	Description		
LIN bus activity	Can be disabled by SPI		
CAN bus activity	Can be disabled by SPI		
Level change of WU1 - 3	Can be individually configured or disabled by SPI		
I _{V1} > I _{cmp}	Device remains in V_1 standby mode but watchdog is enabled (If $I_{cmp} = 0$) and the V_1 regulator goes into high current mode (increased current consumption). No interrupt is generated.		
Timer interrupt / wake up of μC by TIMER	Programmable by SPI - V ₁ standby mode: device wakes up and Interrupt signal is generated at RxDL/NINT when programmable time-out has elapsed - V _{BAT} standby mode: device wakes up, V ₁ regulator is turned on and NReset signal is generated when programmable time-out has elapsed		
SPI access	Always active (except in V _{BAT} standby mode) Wake up event: CSN is low and first rising edge on CLK		

To prevent the system from a deadlock condition (no wake up possible) a configuration where the periodic timer interrupt and wake up by LIN and HS CAN are disabled, is not

allowed. The default configuration is entered for all wake-up sources in case of such an invalid setting.

All wake-up events from V_1 standby mode (except $I_{V1} > I_{cmp}$) are indicated to the microcontroller by a low-pulse at RxDL/NINT (duration: 56 µs).

Wake-up from V_1 standby by SPI Access might be used to check the interrupt service handler.

2.2.6 Wake-up inputs

The de-bounced digital inputs WU1 to WU3 can be used to wake up the L99PM62GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of $64 \mu s$ is implemented at WU1-3. The filter is started when the input voltage passes the specified threshold.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic sense functionality is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer1 or Timer2 (see Section 2.2.7: Cyclic contact supply). The input signal is filtered with a filter time of 16 μ s after a programmable delay (80 μ s or 800 μ s) according to the configured timer on-time. A wake-up is processed if the status has changed versus the previous cycle.

The outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode the input filter timing and input filter delay (*WUx_filt* in control register 2) must correspond to the setting of the high-side output which supplies the external contact switches (OUTx in control register 0).

In standby mode, the inputs WU1-3 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external. In active mode the inputs have a pull down resistor.

In active mode, the input status can be read by SPI (Status Register 2). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

2.2.7 Cyclic contact supply

In V_1 standby and V_{BAT} standby modes, any high-side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X s. The on-time is 10 ms resp. 20 ms: With $X \in \{1, 2, 3, 4 s\}$

Timer 2: period is X ms. The on-time is 100 μ s resp. 1ms: With X \in {10, 20, 50, 200 ms}

2.2.8 Timer interrupt / wake-up of microcontroller by timer

During standby modes the cyclic wake up feature, configured via SPI, allows waking up the μ C after a programmable timeout according to timer1 or timer2.

From V_1 standby mode, the L99PM62GXP wakes up (after the selected timer has elapsed) and sends an interrupt signal (via RxDL/NINT pin) to the μ C. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_1 standby after finishing its tasks.

From V_{BAT} standby mode, the L99PM62GXP wakes up (after the selected timer has elapsed), turns on the V_1 regulator and provides an NReset signal to the μ C. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_{BAT} standby after finishing its tasks.

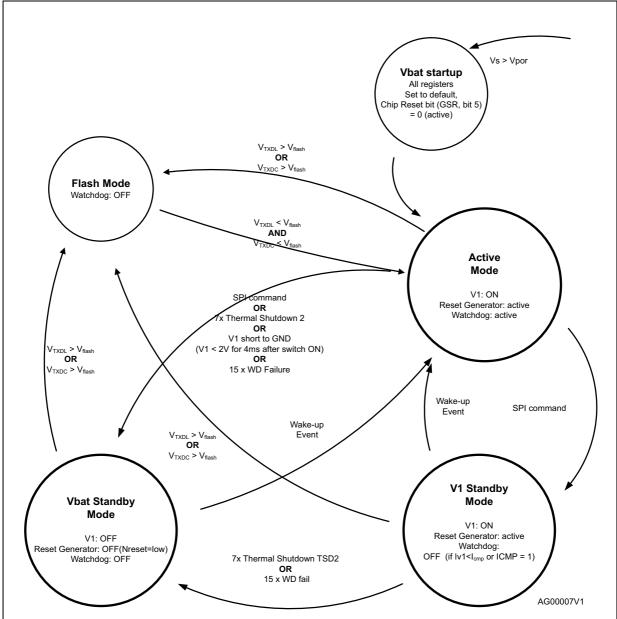
2.3 Functional overview (truth table)

Table 4. Functional overview (truth table)

		Operating modes		
Function	Comments	Active mode	V ₁ -standby static mode (cyclic sense)	V _{BAT} -standby static mode (cyclic sense)
Voltage-regulator, V ₁	V _{OUT} = 5 V	On	On ⁽¹⁾	Off
Voltage-regulator, V ₂	V _{OUT} = 5 V	On/ Off (2)	On ⁽²⁾ / Off	On ⁽²⁾ / Off
Reset-generator		On	On	Off
Window watchdog	V ₁ monitor	On	Off (On: $I_V_1 > I_{cmp}$ - threshold and $I_{cmp} = 0$)	Off
Wake up		Off	Active ⁽³⁾	Active ⁽³⁾
HS-cyclic supply	Oscillator time base	On / Off	On ⁽²⁾ / Off	On ⁽²⁾ / Off
Relay driver		On	Off	Off
Operational amplifiers		On	Off	Off
LIN	LIN 2.1	On	Off ⁽⁴⁾	Off ⁽⁴⁾
HS_CAN		On	Off ⁽⁴⁾	Off ⁽⁴⁾
FSO (if configured by SPI), active by default	Fail safe output	OUT3/FSO Off ⁽⁵⁾	OUT3/FSO Off ⁽⁵⁾	OUT3/FSO Off ⁽⁵⁾
Oscillator		On	(6)	(6)
Vs-monitor		On	(7)	(7)

- 1. Supply the processor in low current mode.
- 2. Only active when selected via SPI.
- 3. Unless disabled by SPI.
- The bus state is internally stored when going to standby mode. A change of bus state leads a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI).
- 5. ON in fail-safe condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
- 6. Activation = ON if cyclic sense is selected.
- 7. cyclic activation = pulsed ON during cyclic sense.

Figure 8. **Operating modes**



2.4 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle: (10 ms, 50 ms, 100 ms, 200 ms)

In V_{BAT} standby and Flash program modes, the watchdog circuit is automatically disabled. In V_1 standby mode a wake up by timer is programmable in order to wake up the μC (see Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer). After wake-up, the watchdog starts with a long open window. After serving the watchdog, the µC may send the device back to V₁ standby mode.

After power-on or standby mode, the watchdog is started with a long open window (65 ms nominal). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is processed when the CSN input becomes HIGH after the transmission of the SPI word.

Writing '1' to the watchdog trigger bit terminates the long open window and start the window watchdog (the timing is programmable by SPI). Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to *Figure 29*). A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the V_1 regulator is switched off for 200ms. If subsequently, 7 additional watchdog failures occur, the V_1 regulator is completely turned off and the device goes into V_{BAT} standby mode until a wakeup occurs.

In case of a watchdog failure, the outputs (RELx, OUTx, V_2) are switched off and the device enters fail-safe mode (i.e. all control registers are set to default values except the 'OUT3 control bit').

The following diagrams illustrate the watchdog behavior of the L99PM62. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of Flash mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

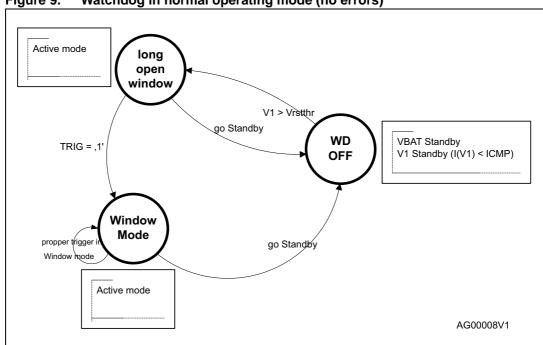


Figure 9. Watchdog in normal operating mode (no errors)

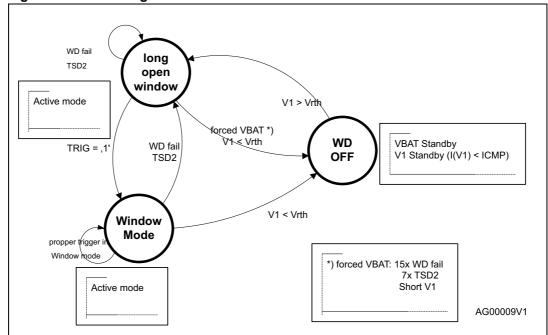
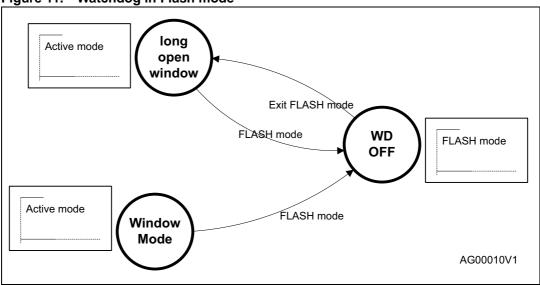


Figure 10. Watchdog with error conditions

Figure 11. Watchdog in Flash mode



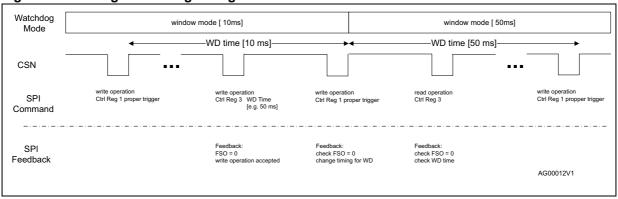
2.4.1 Change watchdog timing

There are 4 programmable watchdog timings available, which represent the nominal trigger time in window mode. To change the watchdog timing, a new timing has to be written by SPI. The new timing gets active with the next valid watchdog trigger. The following figures illustrate the sequence, which is recommended to use, changing the timing within long open window and within window mode.

Watchdog window mode long open window Mode [timing as programmed in previous SPI command; e.g. 50 ms] WD timing [e.g. 50 ms] CSN write operation Ctrl Reg 3 WD Time read operation write operation SPI Ctrl Reg 1 Trig = 0 Ctrl Reg 1 Trig = 1 Ctrl Reg 3 [e.g. 50 ms] Command SPI Feedback: Feedback: Feedback: check FSO = 0 FSO = 0 check FSO = 0 Feedback change timing for WD check WD time write operation accepted AG00011V1

Figure 12. Change watchdog timing within long open window

Figure 13. Change watchdog timing within window mode



If the device is in fail-safe mode, the control registers are locked for writing. To change the watchdog timing out of fail-safe mode, first the fail-safe condition must be solved, respective confirmed from the microcontroller. Afterwards the new watchdog timing can be programmed using the sequence from *Figure 14*. Since the actions to remove, a fail-safe condition can differ from the root cause of the fail safe the following diagram shows the general procedure how to change the watchdog timing out of fail-safe mode. *Figure 15* shows the procedure to change watchdog timing with a previous watchdog failure, since this is a special fail-safe scenario.

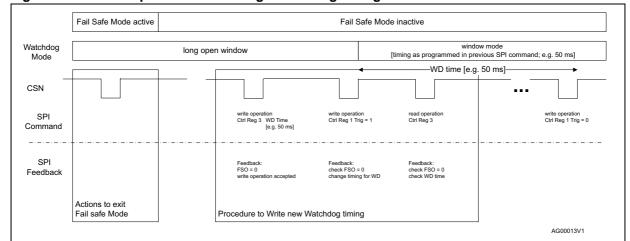
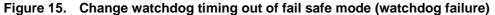
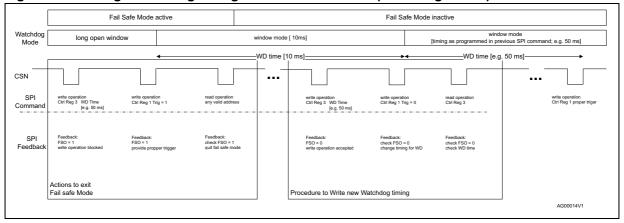


Figure 14. General procedure to change watchdog timing out of fail safe mode





2.5 Fail safe mode

2.5.1 Single failures

L99PM62GXP enters fail safe mode in case of:

- Watchdog failure
- V₁ turn on failure
 - V_1 short ($V_1 < V_{1fail}$ for $t > t_{V1short}$)
- V₁ undervoltage (V₁ < Vrth for t > t_{UV1})
- Thermal shutdown TSD2
- SPI failure
 - DI stuck to GND or V_{CC} (SPI frame = '00 00 00' or 'FF FF FF')

The fail safe functionality is also available in V_1 standby mode. During V_1 standby mode the fails safe mode is entered in the following cases:

- V₁ undervoltage (V₁ < Vrth for t > t_{UV1})
- Watchdog failure (if watchdog still running due to I_{V1} > I_{cmp})
- Thermal shutdown TSD2

In fail safe mode the L99PM62 returns to a default. The fail safe condition is indicated to the remaining system in the global status register. The conditions during fails safe mode are:

- All outputs are turned off
- All control registers are set to default values (except OUT3/FSO configuration)
- Write operations to control registers are blocked until the fail safe condition is cleared (see Table 5)
- LIN and HS CAN transmitter, OpAmps and SPI remain on
- Corresponding failure bits in status registers are set.
- FSO Bit (Bit 0 global status register) is set
- OUT3/FSO is activated if configured as fail safe output

If OUT3 is configured as FSO, the internal fail safe mode can be monitored at OUT3 (high-side driver is turned on in fail-safe mode). Self protection features for OUT3 when configured as FSO are active (see Section 3.3: High-side driver outputs).

OUT3 is configured as fail safe output by default. It can be configured to normal high-side driver operation by SPI. It this case, the configuration remains until Vs power on.

If the fail safe mode was entered it keeps active until the fail safe condition is removed and the fail safe was read by spi. depending on the root cause of the fail safe operation, the actions to exit fail safe mode are as shown in the following table.

Table 5. Fail safe conditions and exit modes

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
μC (oscillator)	Watchdog early write failure or expired window	Fail-safe = 1 WDfail = n+1	TRIG = 1 during LOWi and read fail-safe bit
V ₁	Short at turn-on	Fail-safe = 1 Forced Sleep TSD2/SHTV ₁ = 1	Read&Clear SR3 after wake
	Undervoltage	Fail-safe = 1 $V_{1fail} = 1^{(1)}$	V ₁ > Vrth Read Fail-safe bit
Temperature	T _j > TSD2	Fail-safe = 1 TW = 1 TSD1 = 1 TSD2 = 1	T _j < TSD2 Read&Clear SR3
SPI	DI short to GND or V _{CC}	Fail-safe = 1	Valid SPI command

^{1.} if $V_1 < V_{1fail}$ (for t > t_{V1fail})
The fail-safe bit is located in the global status register (Bit 0).

2.5.2 Multiple failures – entering forced V_{BAT} standby mode

If the fail-safe condition persists and all attempts to return to normal system operation fail, the L99PM62 enters the forced V_{BAT} standby mode in order to prevent damage to the system. The forced V_{BAT} standby mode can be terminated by any regular wake-up event. The root cause of the forced V_{BAT} standby is indicated in the SPI status registers

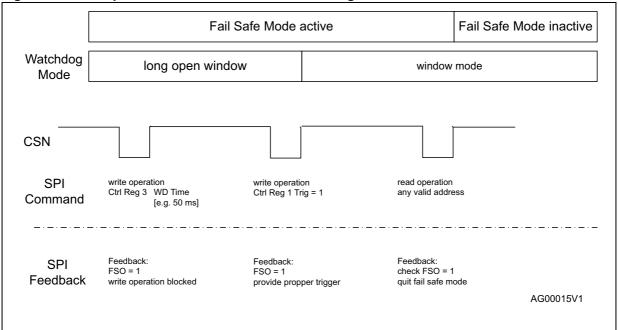
The forced V_{BAT} standby mode is entered in case of:

- Multiple watchdog failures: forced sleep WD = 1 (15x watchdog failure)
- Multiple thermal shutdown 2: forced sleep TSD2/SHTV1 = 1 (7 x TSD2)
- V₁ short at turn-on: forced sleep TSD2/SHTV1 = 1 (V₁ < V_{1fail} for t > t_{V1fail})

Table 6. Persisting fail safe conditions and exit modes

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
μC (oscillator)	15 consecutive watchdog failures	Fail-safe = 1 ForcedSleepWD = 1	Wake-up TRIG = 1 during LOWi read & clear SR3
V ₁	short at turn-on	Fail-safe = 1 ForcedSleepTSD2/SHTV ₁ = 1	Read&clear SR3 after wake-up
Temperature	7 times TSD2	Fail-safe = 1 TW = 1 TSD1 = 1 TSD2 = 1 ForcedSleepTSD2/SHTV ₁ = 1	Read&clear SR3 after wake-up

Figure 16. Example: exit fail safe mode from watchdog failure



2.6 Reset output (NRESET)

If V_1 is turned on and the voltage exceeds the V_1 reset threshold, the reset output "NRESET" is pulled up by internal pull up resistor to V_1 voltage after a reset delay time (t_{rd}) . This is necessary for a defined start of the micro controller when the application is switched on. Since the NRESET output is realized as an open drain output it is also possible to connect an external NRESET open drain NRESET source to the output. It must be considered that as soon the NRESET is released from the L99PM62 the Watchdog timing starts.

A reset pulse is generated in case of:

- V₁ drops below Vrth (configurable by SPI) for t > t_{I IV1}
- Watchdog failure

Note:

An external pull-up resistor (1 $k\Omega$) to V₁ is recommended in order to ensure $I_{LOAD1} > I_{cmp}$ during reset condition

2.7 Operational amplifiers

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes -0.2 V to 3 V.

The operational amplifiers are designed for -0.2 V to +3 V input voltage swing and rail-to-rail output voltage range.

All pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.

The operational amplifiers may also be used to setup an additional high current voltage source with an external pass element. Refer to Section 2.1.3 for a detailed description.

2.8 LIN bus interface

Features

- Speed communication up to 20 kbit/s.
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver.
- Function range from +40 V to -18 V DC at LIN pin.
- GND disconnection fail safe at module level.
- Off mode: does not disturb network.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- Internal pull up resistor.
- Internal high-side switch to disconnect master pull-up resistor in case of short circuit of bus signal.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2.
- Matched output slopes and propagation delay.

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

Note: Use of master pull-up switch is optional.

2.8.1 Error handling

The L99PM62GXP provides the following 3 error handling features which are not described in the LIN Spec. V_{2.1}, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

At V_S > Vpor (i.e. Vs power-on reset threshold), the LIN transceiver is enabled. The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal shutdown 1
- V_S over/undervoltage
- The LIN receiver is not disabled in case of any failure condition.

Dominant TxDL time out

If TXDL is in dominant state (low) for more than 12 ms (typ) the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared. This feature can be disabled via SPI.

Permanent recessive

If TXDL changes to dominant (low) state but RXDL signal does not follow within 40 µs the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

Permanent dominant

If the bus state is dominant (low) for more than 12 ms a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

2.8.2 Wake up (from LIN)

In standby mode the L99PM62GXP can receive a wake up from LIN bus. For the wake up feature the L99PM62GXP logic differentiates two different conditions.

Normal wake up

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t_{linbus} , switches the L99PM62GXP to active mode.

Wake up from short to GND condition

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{linbus} , switches the L99PM62GXP to active mode.

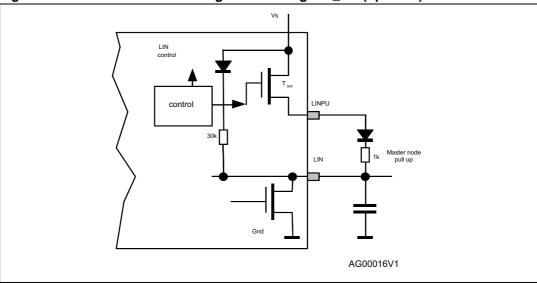
Note: A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

477

2.8.3 LIN pull-up

The master node pull-up resistor (1 $k\Omega$) can be connected to V_S using the internal LIN_PU high-side switch. This high-side switch can be controlled by SPI in order to allow disconnection of the pull-up resistor in case of LIN bus short to GND conditions.

Figure 17. LIN master node configuration using LIN_PU (optional)



LIN_PU high-side driver characteristics:

- Activated by default and can be turned off by SPI command (CR4).
- Remains active in standby modes.
- Switch off only in case of over temperature (TSD2 = thermal shutdown #2).
- No over current protection.
- Typical R_{DS}on, 10 Ω .

2.9 High speed CAN bus transceiver

General requirements

- Communication speed up to 1 Mbit/s.
- ISO 11898-2 and ISO 11898-5 compliant
- SAE J2284 compliant
- Function range from -27 V to +40 V DC at CAN pins.
- GND disconnection fail safe at module level.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Split output pin for stabilizing the recessive bus level
- Receive-only mode available

In order to further reduce the current consumption in standby mode, the integrated CAN bus interface offers an ultra low current consumption.

2.9.1 CAN error handling

The L99PM62GXP provides the following 4 error handling features which are not described in the ISO 11898-2/ISO 11898-5, but are realized in different stand alone CAN transceivers/micro controllers to switch the application back to normal operation mode.

At V_S > Vpor (i.e. V_S power-on reset threshold), the CAN transceiver is enabled. It remains enabled also in case of V_S overvoltage and undervoltage conditions.

The CAN transmitter is disabled only in case of the following errors:

- Dominant TxDC time out
- CAN permanent recessive
- RxDC permanent recessive
- Thermal shutdown 1

The CAN receiver is not disabled in case of any failure condition.

Dominant TxDC time out

If TXDC is in dominant state (low) for $t > t_{dom(TxD)}$ the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN permanent recessive

If TXDC changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN permanent dominant

If the bus state is dominant (low) for $t > t_{CAN}$ a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

RXDC permanent recessive

If RXDC pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXDC does not follow TXDC for 4 times the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

2.9.2 Wake up (from CAN)

When the L99PM62GXP is in standby mode with CAN wake up option enabled, the CAN bus traffic is detected. For the wake up feature the L99PM62GXP logic differentiates different conditions. During V_1 Standby mode RXDC output is kept at recessive level. Independent from the wakeup pattern selected and independent from the previous Standby mode, the RXDC reflect immediately the bus state after the wakeup. This feature allows implementation of a 'partial networking' functionality controlled by the system microcontroller.

Normal pattern wake up

Normal pattern wake up can occur when CAN pattern wake up option is enabled and the CAN transceiver was set in standby mode while CAN bus was in recessive (high) state or dominant (low) state. In order to wake up the L99PM62GXP, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than 2 μs
- The distance between 2 pulses must be longer than 2 µs.
- The two pulses must occur within a time frame of 1.0 ms

Wake up from short to GND condition

Even if CAN pattern wake up option is enabled, but the CAN transceiver was set in standby mode after a qualified permanent dominant state, recessive level at CAN, switches the L99PM62GXP to active mode.

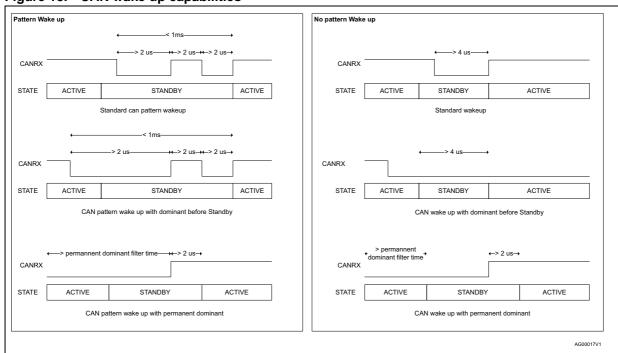
No pattern wake up

If the CAN pattern wake up option is disabled, any transition either dominant (low) state to recessive (high) state or recessive (high) state to dominant (low) state switches the L99PM62GXP to active mode (after a filtering time of 2 µs).

Note:

A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

Figure 18. CAN wake up capabilities



Note: Pictures above illustrate the wake up behaviour from V_1 standby mode. For wake up from V_{BAT} standby mode an NReset pulse is generated instead of the RXDL (Interrupt) signal.

32/102 Doc ID 17639 Rev 4

2.9.3 CAN sleep mode

During active mode it is possible to deactivate the CAN transceiver with a dedicated SPI command (CR4, CAN_act = 0). The CAN transceiver remains deactivated until it is activated again. With a deactivated CAN the receiver input termination network is disconnected from the bus and the CANH, CANL bus lines is driven to GND. The SPLIT output is also deactivated in this case.

2.9.4 CAN receive only mode

With the CAN_rec_only bit in control register 4 it is possible to disable the CAN transmitter in active mode. In this mode it is possible to listen to the bus but not sending to it. The receiver termination network is still activated in this mode.

2.9.5 CAN looping mode

If the CAN_Loop_en bit in control register 4 is set the TXDC input is mapped directly to the RXDC pin. This mode can be used in combination with the CAN receive only mode, to run diagnosis for the CAN protocol handler of the micro controller.

2.10 Serial peripheral interface (ST SPI standard)

A 24 bit SPI is used for bi-directional communication with the micro controller.

During active mode, the SPI

- Triggers the watchdog
- Controls the modes and status of all L99PM62GXP modules (incl. input and output drivers)
- Provides driver output diagnostic
- Provide L99PM62GXP diagnostic (incl. overtemperature warning, L99PM62GXP operation status)

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a built-in SPI. Only three CMOS-compatible output pins and one input pin is needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin reflects the global error flag (fault condition) of the device.

Chip select not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

If CSN = low for $t > t_{CSNfail}$ the DO output is switched to high impedance in order to not block the signal line for other SPI nodes.

Serial data in (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to Data Input Register. The writing to the selected data input register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note:

Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial data out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 1MHz.

3 Protection and diagnosis

3.1 Power supply fail

Over and under-voltage detection on Vs

3.1.1 V_S overvoltage

If the supply voltage Vs reaches the over voltage threshold (V_{SOV}):

- Outputs OUTx, RELx and LIN are switched to high impedance state (load protection).
 CAN is not disabled. Recovery of outputs when the overvoltage condition disappears is depending on the setting of VLOCKOUT_EN bit in Control Register 4.
 - VLOCKOUT EN = 1: Outputs are off until read and clear SR3.
 - VLOCKOUT_EN = 0: Outputs switch automatically on when overvoltage condition disappears.
- The over voltage bit is set and can be cleared with a 'Read and Clear' command. The overvoltage bit is removed automatically if VLOCKOUT_EN = 0 and the overvoltage condition disappears.
- Outputs REL1,2 can be excluded from a shutdown in case of overvoltage by SPI (LSOVUV Shutdown en in CR4)

3.1.2 Vs undervoltage

If the supply voltage Vs drops below the under voltage threshold voltage (V_{SUV})

- Outputs OUTx, RELx and LIN are switched to high impedance state (load protection).
 CAN is not disabled. Recovery of outputs when the undervoltage condition disappears is depending on the setting of VLOCKOUT_EN bit.
 - VLOCKOUT_EN = 1: Outputs are off until read and clear SR3.
 - VLOCKOUT_EN = 0: Outputs switch on automatically when undervoltage condition disappears.
- The undervoltage bit is set and can be cleared with a 'Read and Clear' command. The
 undervoltage bit is removed automatically if VLOCKOUT_EN = 0 and the undervoltage
 condition disappears
- Outputs REL1,2 can be excluded from a shutdown in case of undervoltage by SPI (LSOVUV_shutdown_en in CR4)

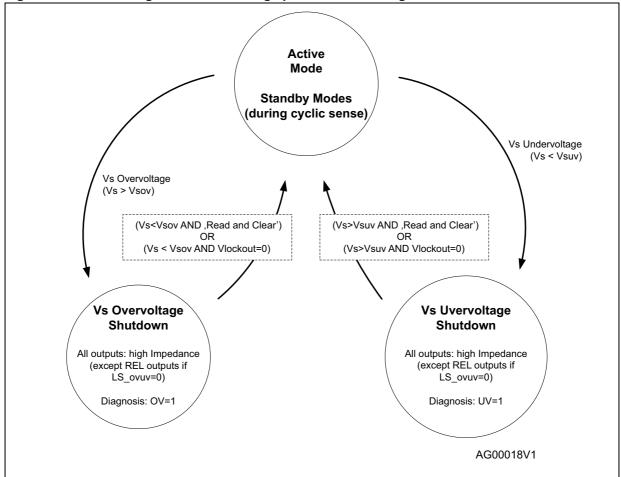
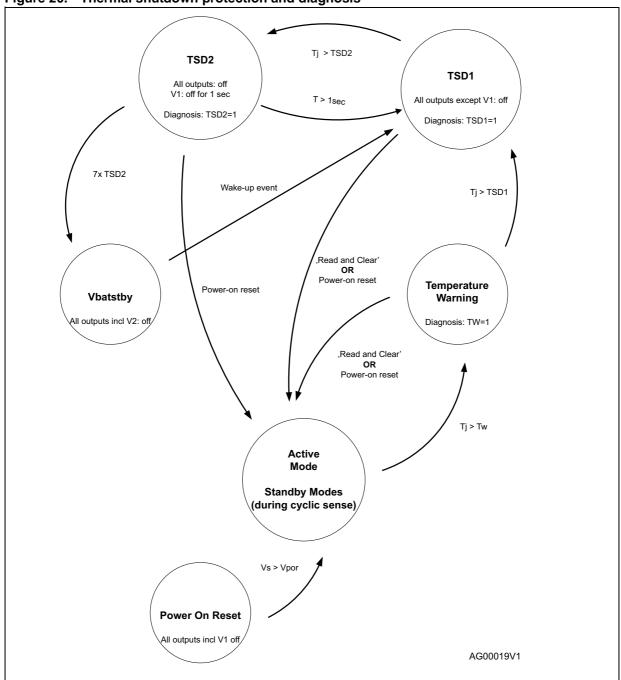


Figure 19. Over voltage and under voltage protection and diagnosis

36/102 Doc ID 17639 Rev 4

3.2 Temperature warning and thermal shutdown

Figure 20. Thermal shutdown protection and diagnosis



Note: The thermal state machine recovers the same state were it was before entering standby mode. In case of a TSD2 it enters TSD1 state.

Note:

3.3 High-side driver outputs

The component provides a total of 4 high-side outputs Out1 to 4, (7 Ω typical at 25°C) to drive e.g. LED's or hall sensors and 1 high-side output OUT_HS with 1 Ω typical at 25 °C).

The high-side outputs switch off in case of:

- V_S over and undervoltage
- Overcurrent
- Overtemperature (TSD1) with pre warning^(a)

In case of overload or over temperature (TSD1) condition, the drivers switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case over/under voltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the Vlockout bit (Control Register 4) is set to '1' the drivers remain off until the status is cleared. If the Vlockout bit is set to '0' the drivers switches on automatically if the error condition disappears.

In case of open-load condition, the according status register is latched. The status can be read and optionally cleared by SPI. The high-sides are not switched off.

For OUT_HS the auto recovery feature (OUTHSREC bit Control Register 4) can be enabled. If this bit is set to '1' the driver is automatically restart from a overload condition. This overload recovery feature is intended for loads which have an initial current higher than the over current limit of the output (e.g. Inrush current of cold light bulbs). During auto recovery mode the over current status bit can not be read from SPI.

The device itself can not distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the micro controller can switch on light bulbs by setting the over current recovery bit for the first 50ms. After clearing the recovery bit, the output is automatically disabled if the overload condition still exists.

In case of a fail safe condition, the high-side drivers are switched off. The control bits are set to default values. (except OUT3/FSO if it is used as a high-side driver output)

The maximum voltage and current applied to the high-side outputs is specified in Section 5.1: Absolute maximum rating. Appropriate external protection may be required in order to respect these limits under application conditions.

Each high-side driver can be driven whether with a PWM signal or with a internal Timer. See *Table 7*.

For more Details please refer to Section 6.2: SPI registers.

Table 7. PWM configuration for high-side outputs

High-side output	PWM channel	Internal timer
OUT1	PWM 1	Timer 1
OUT2	PWM 2	Timer 2
OUT3	PWM 3	-

a. Except OUT3 when configured as FSO.

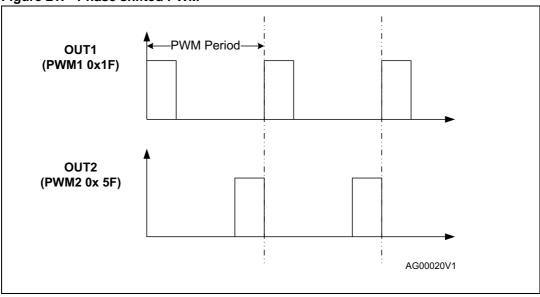
Table 7. PWM configuration for high-side outputs (continued)

High-side output	PWM channel	Internal timer
OUT4	PWM 4	Timer 2
OUTHS	PWM 3 / PWM 4	Timer 1 / Timer 2

The PWM 1 / 3 channels start a PWM period with the ON phase, while the PWM 2 / 4 channels start with the OFF phase. In this way it is possible to use the 4 PWM channels in a phase shifted way.

The *Figure 21* shows this feature with a duty cycle of 25% for both PWM channels.

Figure 21. Phase shifted PWM



3.4 Low-side driver outputs REL1, REL2

The outputs REL1, REL2 (R_{DSon} = 2 Ω typical at 25 °C) are specially designed to drive relay loads.

The outputs provide an active output zener clamping (45 V typical) feature for the demagnetization of the relay coil, even though a load dump condition exists.

For fail-safe reasons the relay drivers are linked with the fail safe operation: in case of entering the fail safe mode, the relay drivers switches off and the SPI control bits are set to default (i.e. driver is off).

The low-side drivers switch off in case of:

- V_S over and undervoltage
- Overcurrent
- Overtemperature with pre warning

In case of overload or overtemperature (TSD1) condition, the drivers switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case V_S over/undervoltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the Vlockout bit (Control Register 4) is set to '1' the drivers remain off until the status is cleared. If the Vlockout bit is set to '0' the drivers is switched on automatically if the error condition disappears.

With the LSOVUV_shutdown_en bit (Control Register 4) the drivers can be excluded from a switch off in case of V_S over/undervoltage. If the bit is set to '1' the driver switches off, otherwise the drivers remain on.

3.5 SPI diagnosis

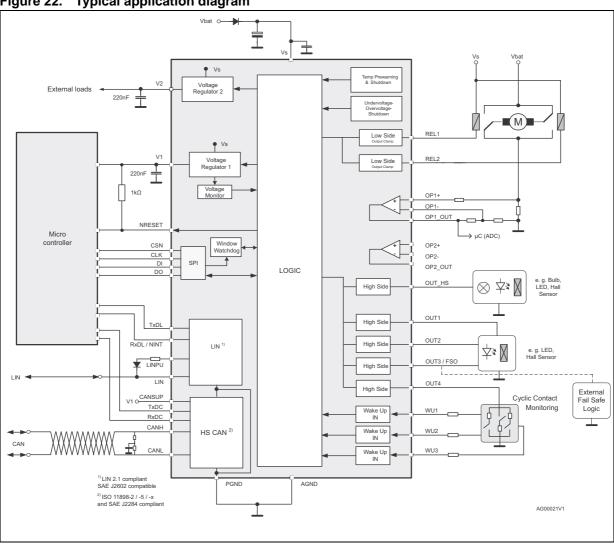
Digital diagnosis features are provided by SPI (for details please refer to Section 6.2: SPI registers.

- V₁ reset threshold programmable
- Overtemperature including, pre warning
- Open-load separately for each output stage except REL1/REL2
- Overload status separately for each output stage
- Vs-supply over/under voltage
- V₁ and V₂ fail bit
- V₂ output short to GND
- Status of the WU1 to 3
- Wake-up sources (CAN, LIN, SPI, Timer, WU1...3)
- chip reset bit (start from power-on reset)
- Number of unsuccessful V₁ restarts after thermal shutdown
- Number of sequential watchdog failures
- LIN diagnosis (permanent recessive/dominant, dominant TxD)
- CAN diagnosis (permanent recessive/dominant, dominant TxD, recessive RXD)
- Device State (wake-up from V1 standby or V_{BAT} standby)
- Forced V_{BAT} standby after WD-fail, forced V_{BAT} standby after overtemperature
- Watchdog timer state (diagnosis of watchdog)
- Fail-safe status
- SPI communication error

L99PM62GXP **Typical application**

Typical application 4

Figure 22. Typical application diagram



5 Electrical specifications

5.1 Absolute maximum rating

Table 8. Absolute maximum rating

Symbol	Parameter/test condition	Value [DC voltage]	Unit
V _S	DC supply voltage / "jump start"	-0.3 to +28	V
	Single pulse / t _{max} < 400 ms "transient load dump"	-0.3 to +40	V
V ₁	Stabilized supply voltage, logic supply	-0.3 to $(V_1 + 0.3) V$ $V_1 < V_S$	V
V ₂	Stabilized supply voltage	-0.3 to +28	V
V _{DI} V _{CLK} V _{DO} V _{RXDL} V _{NRESET} V _{RXDC}	Logic input / output voltage range	-0.3 to V ₁ +0.3	V
V _{TXDC} , V _{TXDL} , V _{CSN}	Multi level inputs	-0.3 to V _S +0.3	V
V _{REL1,} V _{REL2,}	Low-side output voltage range	-0.3 to +40	V
V _{OUT14} , V _{OUT_HS}	High-side output voltage range	-0.3 to V _S +0.3	V
V _{WU13}	Wake up input voltage range	-0.3 to V _S +0.3	V
V _{OP1P,} V _{OP1M,} V _{OP2P,} V _{OP2M,}	Opamp1 input voltage range Opamp2 input voltage range	-0.3 to V ₁ +0.3	V
V _{OPOUT1,} V _{OPOUT2}	Analog Output voltage range	-0.3 to V _S +0.3	V
V _{LIN,} V _{LINPU}	LIN bus I/O voltage range	-20 to +40	V
I _{Input}	Current injection into V _S related input pins	20	mA
lout_inj	Current injection into V _S related outputs	20	mA
V _{CANSUP}	CAN supply	-0.3 to +5.25	V
V _{CANH,} V _{CANL,} V _{SPLIT}	CAN bus I/O voltage range	-27 to +40	V

Note:

All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

5.2 ESD protection

Table 9. ESD protection

Parameter	Value	Unit
All pins ⁽¹⁾	+/-2	kV
All output pins ⁽²⁾	+/-4	kV
LIN	+/-8 ⁽²⁾ +/-10 ⁽³⁾ +/-6 ⁽⁴⁾	kV
CAN_H, CAN_L	+/-8 ⁽²⁾ +/-6 ⁽⁴⁾	kV
All pins ⁽⁵⁾	+/-500	V
Corner pins ⁽⁵⁾	+/-750	V
All pins ⁽⁶⁾	+/-200	V

- 1. HBM (human body model, 100 pF, 1.5 k Ω) according to MIL 883C, method 3015.7 or EIA/JESD22A114-A.
- 2. HBM with all none zapped pins grounded.
- 3. Indirect ESD test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02).
- 4. Direct ESD test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02); $C_{bus,LIN}$ = 220 pF.
- 5. Charged device model.
- 6. Machine model: C = 200 pF; $R = 0 \Omega$.

5.3 Thermal data

Table 10. Operating junction temperature

Symbol	Parameter	Value	Unit
T _j	Operating junction temperature	-40 to 150	°C
R _{thjA}	Thermal resistance junction / ambient	See Figure 25	°K/W

Table 11. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Тур.	Max.	Unit
T _{W ON}	Thermal over temperature warning threshold	T _j ⁽¹⁾	120	130	140	°C
T _{SD1 OFF}	Thermal shutdown junction temperature 1	T _j ⁽¹⁾	130	140	150	°C
T _{SD2 OFF}		$T_j^{(1)}$	150	160	170	°C
T _{SD2 ON}	Thermal shutdown junction temperature 2	Hysteresis		5		°C
T _{SD12hys}		Trysteresis		,		O

1. Non-overlapping

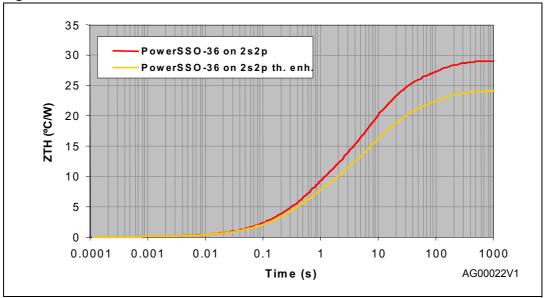


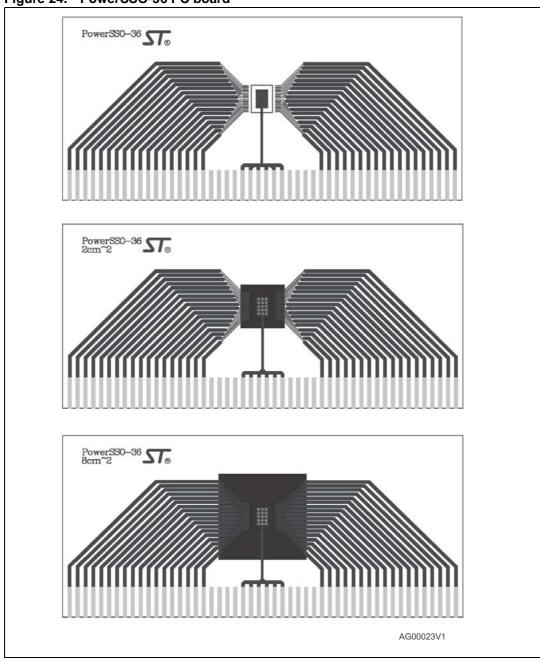
Figure 23. Thermal data of PowerSSO-36

44/102 Doc ID 17639 Rev 4

5.4 Package and PCB thermal data

5.4.1 PowerSSO-36 thermal data

Figure 24. PowerSSO-36 PC board

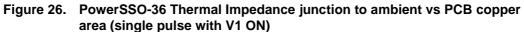


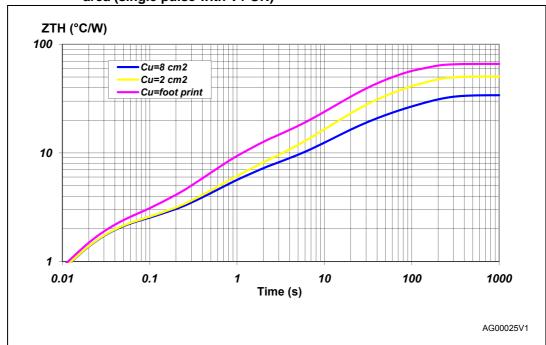
Note:

Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10% board double layer, board dimension 129x60, board Material FR4, Cu thickness 0.070 mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm).

RTHjamb RTHj_amb(C/W) 70 RTHjamb 60 50 40 30 0 2 4 6 8 10 PCB Cu heatsink area (cm^2) AG00024V1

Figure 25. PowerSSO-36 Thermal Resistance junction to ambient vs PCB copper area (V1 ON)





46/102 Doc ID 17639 Rev 4

Tj C1 C2 C3 C4
R1 R2 R3 R4
W Pd AG00026V1

Figure 27. PowerSSO-36 thermal fitting model (V1 ON)

Equation 1: pulse calculation formula

$$\begin{split} & \textbf{Z}_{TH\delta} = \textbf{R}_{TH} \cdot \delta + \textbf{Z}_{THtp} (1 - \delta) \\ & \text{where} \quad \delta = t_p / T \end{split}$$

Table 12. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	2		
R2 (°C/W)	8	4	4
R3 (°C/W)	20	15.5	10
R4 (°C/W)	36	29	18
C1 (W.s/°C)	0.01		
C2 (W.s/°C)	0.1	0.2	0.2
C3 (W.s/°C)	0.8	1	1.5
C4 (W.s/°C)	2	3	6

5.5 **Electrical characteristics**

5.5.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin T_i = -40 °C to 130 °C, unless otherwise specified.

Table 13. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{SUV}	V _S undervoltage threshold	V _S increasing / decreasing	5.11		5.81	V
V _{hyst_UV}	V _S undervoltage hysteresis		0.0	0.1	0.15	V
V _{SOV}	V _S overvoltage threshold	V _S increasing / decreasing	18.5		22	V
V _{hyst_OV}	V _S overvoltage hysteresis	Hysteresis	0.5	1	1.5	V
t _{ovuv_filt}	V _S over/undervoltage filter time			64*T _{osc}		
I _{V(act)}	Current consumption in active mode	$Vs = 12V$ $TxD CAN = high$ $TxD LIN = high$ $V_1 = on, V_2 = on$ $HS/LS driver off$		6	12	mA
I _{V(BAT)}	Current consumption in V _{BAT} standby mode	V _S = 12V Both voltage regulators deactivated, no wake-up request ⁽¹⁾ HS/LS driver off	8	12	28	μΑ
I _{V(BAT)} CS	Current consumption in V _{BAT} standby mode with cyclic sense enabled	$V_S = 12V$ Both voltage regulators deactivated, T = 50 ms, ton = 100 µs no wake-up request ⁽¹⁾	70	110	130	μА
I _{V(BAT)CW}	Current consumption in V _{BAT} standby mode with cyclic wake enabled	V _S = 12V Both voltage regulators deactivated During standby phase no wake-up request ⁽¹⁾	70	110	130	μА
I _(V1)	Current consumption in V ₁ -standby mode	$V_S = 12V$ Voltage Regulator V_1 active, $(I_{v1} < I_{cmp})$ no wake-up request ⁽¹⁾ HS/LS driver off	16	51	76	μА

Conditions for no wake-up request are (all conditions must be met): $2 \ V < LIN < (V_S-2 \ V) \\ 0.4 \ V < (CAN_H - CAN_L) < 1,2 \ V \\ 1 \ V < V_{WUth} < (V_S-2 \ V) \\ \text{The current consumption in standby modes with cyclic sense can be calculated using the following formulas: } \\ \frac{I_{V(BAT)CS}}{I_{V(S-1)}} = \frac{I_{V(BAT)}}{I_{V(S-1)}} + \frac{55}{\mu} \\ \text{A} + \frac{(2 \ \text{mA} * (t_{ON} + 100 \ \mu\text{s}) / T)}{I_{(V(S)CS)}} = \frac{I_{V(S-1)}}{I_{V(S-1)}} + \frac{100}{\mu} \\ \text{A} + \frac{100}{\mu} \\ \text{B} + \frac{100}{\mu} \\ \text{A} + \frac{1$

5.5.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V \leq V_S \leq 28 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 14. Oscillator

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
F _{CLK}	Oscillation frequency		0.80	1.0	1.35	MHz

5.5.3 Power-on reset (V_S)

All outputs open; $T_i = -40$ °C to 130°C, unless otherwise specified.

Table 15. Power-on reset (V_s)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V_{POR}	V _{POR} threshold	Vs increasing		3.45	4.5	V
V _{POR}	V _{POR} threshold	Vs decreasing ⁽¹⁾	2.65		3.5	٧

^{1.} This threshold is valid if Vs had already reached 7V previously

5.5.4 Voltage regulator V₁

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V \leq V_S \leq 28 V; T_i = -40 °C to 130 °C, unless otherwise specified.

Table 16. Voltage regulator V₁

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V ₁	Output voltage			5.0		V
V ₁	Output voltage tolerance Active mode	I _{LOAD1} = 4 mA to 100 mA; V _S = 13.5 V	-2		+2	%
V	Output voltage tolerance	I_{LOAD1} = 100 mA to 250 mA; V _S = 13.5 V	-3		+3	%
V _{hc1}	active mode, high current	I _{LOAD1} = 250 mA; V _S = 13.5 V	-5		+5	%
V _{STB1}	Output voltage tolerance V ₁ -standby mode	$I_{LOAD1} = 0 \mu A \text{ to 4 mA};$ $V_S = 13.5 \text{ V}$	-2		+4	%
		I _{LOAD1} = 50 mA; V _S = 5 V		0.2	0.4	V
		$I_{LOAD1} = 100 \text{ mA}; V_S = 4.5 \text{ V}$		0.2	0.5	٧
V_{DP1}	Drop-out voltage	$I_{LOAD1} = 100 \text{ mA}; V_S = 5 \text{ V}$		0.3	0.5	٧
		$I_{LOAD1} = 150 \text{ mA}; V_S = 4.5 \text{ V}$		0.45	0.6	٧
		I _{LOAD1} = 150 mA; V _S = 5.0 V		0.45	0.6	V
I _{CC1}	Output current in active mode	Max. continuous load current		_	250	mA
I _{CCmax1}	Short circuit output current	Current limitation	340	600	900	mA

Table 16. Voltage regulator V₁ (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
C _{load1}	Load capacitor1	Ceramic (+/- 20%)	0.22 ⁽¹⁾			μF
t _{TSD}	V ₁ deactivation time after thermal shutdown			1		sec
I _{cmp_ris}	Current comp. rising thresh.	Rising current	1.0	2.5	4	mA
I _{cmp_fal}	Current comp. falling threshold	Falling current	0.8	1.95	3.1	mA
I _{cmp_hys}	Current comp. hysteresis			0.5		mA
V _{1fail}	V ₁ fail threshold	V ₁ forced		2		V
tV _{1fail}	V ₁ fail filter time			2		μs
tV _{1short}	V ₁ short filter time			4		ms

Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20 %). Capacitor must be located close to the regulator output pin.

5.5.5 Voltage regulator V₂

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V \leq V_S \leq 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 17. Voltage regulator V₂

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V ₂	Output voltage			5,0		V
V ₂	Output voltage tolerance active mode	I_{LOAD2} = 1 mA to 50 mA; V_S = 13.5 V			+/- 3	%
V _{hc1}	Output voltage tolerance active mode	I_{LOAD2} = 50 mA to 80 mA; V_S = 13,5 V			+/- 4	%
V ₂	Output voltage tolerance active mode, high current	I _{LOAD2} = 100 mA; V _S = 13.5 V			+/- 6	%
V _{STB2}	Output voltage tolerance V ₁ standby mode	I _{LOAD2} = 1 mA; V _S = 13.5 V			+/-6.5	%
V	Dran out valtage	$I_{LOAD2} = 25 \text{ mA}; V_S = 5.25 \text{ V}$		0.3	0.4	V
V _{DP2}	Drop-out voltage	$I_{LOAD2} = 50 \text{ mA}; V_S = 5.25 \text{ V}$		0.4	0.7	V
I _{CC2}	Output current in active mode	Max. continuous load current			100	mA
I _{CCmax2}	Short circuit output current	Current limitation	150	280	450	mA
C _{load}	Load capacitor	Ceramic (+/- 20 %)	0.22 ⁽¹⁾			μF
V _{2fail}	V ₂ fail threshold	V ₂ forced			2	V
t _{V2fail}	V ₂ fail filter time			2		μs
t _{V2short}	V ₂ short filter time			4		ms

^{1.} Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20 %). Capacitor must be located close to the regulator output pin.

50/102 Doc ID 17639 Rev 4

5.5.6 Reset output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 4.0 V < V_S = 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 18. Reset output

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{RT1}	Reset threshold voltage1	V ₁ decreasing	3.7	3.9	4.1	V
V _{RT2}	Reset threshold voltage2	V ₁ decreasing	4.2	4.3	4.45	V
V _{RT3}	Reset threshold voltage3	V ₁ decreasing	4.25	4.4	4.55	V
V _{RT4}	Reset threshold voltage4	V1 decreasing	4.5	4.60	4.75	V
VRT4	Reset threshold voltage4	V ₁ increasing	4.7	4.8	4.9	V
V _{RESET}	Reset pin low output voltage	V ₁ > 1 V; I _{RESET} = 5 mA		0,2	0,4	V
R _{RESET}	Reset pull up int. resistor		80	110	150	kΩ
t _{RR}	Reset reaction time	I _{LOAD1} = 1 mA	6		40	μs
t _{UV1}	V ₁ under-voltage filter time			16		μs
Trd	Reset pulse duration		1.46	2	2.5	ms

5.5.7 Watchdog

4.5 V < V $_S$ < 28 V; 4.8 V < V $_1$ < 5.2 V; T $_j$ = -40 °C to 130 °C, unless otherwise specified, see Figure 28 and Figure 29.

Table 19. Watchdog

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t_{LW}	Long open window		48,75	65	81,25	ms
T _{EFW1}	Early failure window 1				4.5	ms
T _{LFW1}	Late failure window 1		20			ms
T _{SW1}	Safe window 1		7.5		12	ms
T _{EFW2}	Early failure window 2				22.3	ms
T _{LFW2}	Late failure window 2		100			ms
T _{SW2}	Safe window 2		37.5		60	ms
T _{EFW3}	Early failure window 3				45	ms
T _{LFW3}	Late failure window 3		200			ms
T _{SW3}	Safe window 3		75		120	ms
T _{EFW4}	Early failure window 4				90	ms
T _{LFW4}	Late failure window 4		400			ms
T _{SW4}	Safe window 4		150		240	ms

Normal startup operation and timeout failures T_{LW} = long window $T_{\rm cw}$ = closed window = correct trigger timing T_{ow}= open window = early trigger timing T_{WDR}= watchdog reset = missing trigger WDtrigger trigger signa time / ms $T_{\underline{LW}}$ $\mathsf{T}_{_{\mathsf{LW}}}$ NRES-Out 0 missing normal operation early time / ms trigger write Missing uC trigger signal WDtrigger time / ms NRES Out time / ms 0 AG00027V1

Figure 28. Watchdog timing (long, early, late and safe window)

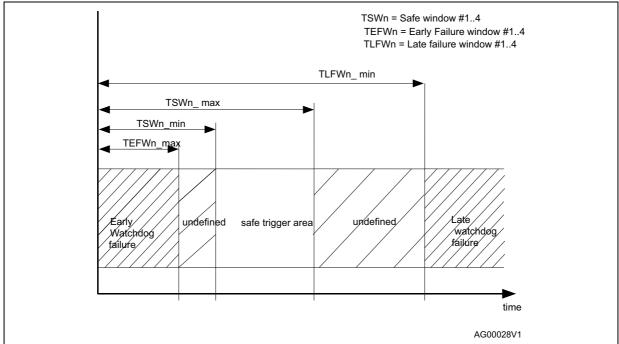


Figure 29. Watchdog early, late and safe windows

5.5.8 High-side outputs

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.8 V \leq V₁ \leq 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 20. Output (OUT_HS)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
R _{DS} ON	Static drain source	T _j = 25 °C		1	2	Ω
NDSON	on-resistance (IOUT_HS = 150 mA)	T _j = 125 °C		1.6	3	Ω
t _d ON	Switch on delay time	0.2 V _S	5	35	60	μs
t _d OFF	Switch off delay time	0.8 V _S	40	95	150	μs
t _{SCF}	Short circuit filter time	Tested by scan chain		64*T _{OSC}		
t _d ARHS	Auto recovery filter time	Tested by scan chain		400*T _{OSC}		
dV _{OUT} /dt	Slew rate		0,18	0,5	0,8	V/µs
l _{out}	Short circuit shutdown current		480	900	1320	mA
I _{OLD}	Open-load detection current		40	80	120	mA
t _{OLDT}	Open-load detection time	Tested by scan chain		64*T _{OSC}		
I _{FW} ⁽¹⁾	Loss of GND current (ESD structure)		100			mA

^{1.} Parameter guaranteed by design

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.8 V \leq V₁ \leq 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 21. Outputs (OUT1...4)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
R _{DS} ON	Static drain source on-resistance (IOUT_HS = 150mA)	I _{LOAD} = 60 mA @ T _j = +25 °C		7	13	Ω
I _{OUT}	Short circuit shutdown current	8 V < V _s < 16 V	140	235	350	mA
I _{OLD}	Open-load detection current 1		0.9	2	4.5	mA
dV _{OUT} /dt	Slew rate		0.2	0.5	0.8	V/µs
t _{dON}	Switch ON delay time	0.2 V _s	5	35	60	μs
t _{dOFF}	Switch OFF delay time	0.8 V _s	30	95	150	μs
t _{SCF}	Short circuit filter time	Tested by scan chain		64*T _{OSC}		
I _{FW} ⁽¹⁾	Loss of GND current (ESD structure)		100			mA
t _{OLDT}	Open-load detection time	Tested by scan chain		64*T _{OSC}		

^{1.} Parameter guaranteed by design

5.5.9 Relay drivers

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.8 V \leq V₁ \leq 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 22. Relay drivers

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
R _{DSON}	DC output resistance	$I_{LOAD} = 100 \text{ mA } @ T_j = +25 \text{ °C}$		2	3	Ω
l _{out}	Short circuit shutdown current	8 V < V _s < 16 V	250	375	500	mA
V _Z	Output clamp voltage ⁽¹⁾	I _{LOAD} = 100 mA	40		48	V
t _{ONHL}	Turn on delay time to 10% V _{OUT}		5	50	100	μs
t _{OFFLH}	Turn off delay time to 90% V _{OUT}		5	50	100	μs
t _{SCF}	Short circuit filter time	Tested by scan chain		64*T _{OSC}		
dV _{OUT} /dt	Slew Rate		0.2	2	4	V/µs

^{1.} The output is capable to switch off relay coils with the impedance of RL = 160Ω; L = 300mH (RL = 220Ω; L = 420mH); at V_S = 40V (load dump condition)

5.5.10 Wake up inputs (WU1... WU3)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; T_i = -40 °C to 130 °C, unless otherwise specified.

Table 23. Wake up inputs (WU1... WU3)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{WUthp}	Wake-up negative edge threshold voltage		0.4*V _s	0.45*V _s	0.5*V _s	V
V _{WUthn}	Wake-up positive edge threshold voltage		0.5*V _s	0.55*V _s	0.6*V _s	V
V _{HYST}	Hysteresis		0.05*V _s	0.1*V _s	0.15*V _s	V
t _{WU_stat}	Static wake filter time			64*T _{OSC}		μs
I _{WU_stdby}	Input current in standby mode	$1 \text{ V} > \text{V}_{in} > (\text{V}_{s} - 2 \text{ V})$	9	15	28	μΑ
R _{WU_act}	Input resistor to Gnd in active mode and in standby mode during wake-up request		80	160	300	kΩ
t _{WU_cyc}	Cyclic wake filter time			16 ⁽¹⁾		μs

^{1.} Blanking time 80 μs or 800 μs .

5.5.11 High speed CAN transceiver(b)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V \leq V_S \leq 18 V; 4.8 V \leq Vcansup. \leq 5.2 V; T_{junction} = -40 °C to 130 °C, unless otherwise specified.

Table 24. CAN communication operating range

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{SCOM}	Supply voltage operating range for CAN communication	Active mode, $V_1 = V_{CANSUP}$	5.5	-	18	V

Table 25. CAN transmit data input: pin TXDC

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{TXDCLOW}	Input voltage dominant level	Active mode, V ₁ = 5 V	1.35	1.8		V
V _{TXDCHIGH}	Input voltage recessive level	Active mode, V ₁ = 5 V		2.7	2.9	V
V _{TXDCHYS}	V _{TXDCHIGH} -V _{TXDCLOW}	Active mode, V ₁ = 5 V	0.7	1		V
R _{TXDCPU}	TXDC pull up resistor	Active mode, V ₁ = 5 V	10	20	35	kΩ

b. ISO 11898-2 and ISO 11898-5 compliant; SAE J2284 compliant.



Table 26. CAN receive data output: pin RXDC

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{RXDCLOW}	Output voltage dominant level	Active mode, V ₁ = 5 V, 2 mA		0.2	0.5	V
V _{RXDCHIGH}	Output voltage recessive level	Active mode, V ₁ = 5 V, 2 mA	4.5			V

Table 27. CAN bus common mode stabilization output termination: pin SPLIT

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
V _{SPLIT,I}	Split output voltage, loaded condition (normal mode)	Active mode; $V_{TXDC} = V_{TXDCHIGH}$; $ Isplit = 500 \mu A$	0.3* V _{CANSUP}	0.5* V _{CANSUP}	0.7* V _{CANSUP}	٧
V _{SPLIT,u}	Split output voltage, unloaded condition (normal mode)	Active mode; V _{TXDC} = V _{TXDCHIGH} ; No Load		0.5* V _{CANSUP}	0.55* V _{CANSUP}	٧
I _{SPLIT}	Split leakage current (low power mode)	V ₁ -standby mode; -12 V < V _{SPLIT} < 12 V			5	μΑ

Table 28. CAN transmitter and receiver: pins CANH and CANL

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
V _{CANHdom}	CANH voltage level in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW};$ $R_L = 60 \Omega; R_L = 50 \Omega$	2.75		4.5	V
V _{CANLdom}	CANL voltage level in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW};$ $R_L = 60 \Omega; R_L = 50 \Omega$	0.5		2.25	V
V _{DIFF,domOUT}	Differential output voltage in dominant state: VCANHdom - VCANLdom	Active mode; $V_{TXDC} = V_{TXDCLOW}$; $R_L = 60 \Omega$; $R_L = 50 \Omega$	1.5		3	V
V _{CM}	Driver symmetry: V _{CANHdom} + 0V _{CANLdom}	Active mode; $V_{TXDC} = V_{TXDCLOW};$ $R_L = 60 \ \Omega;$ $C_{SPLIT} = 4.7 \ pF$	0.9* V _{CANSUP}	V _{CANSUP}	1.1* V _{CANSUP}	V
V _{CANHrec}	CANH voltage level in recessive state (normal mode)	Active mode; V _{TXDC} = V _{TXDCHIGH} ; no load	2	2.5	3	V
V _{CANLrec}	CANL voltage level in recessive state (normal mode)	Active mode; V _{TXDC} = V _{TXDCHiGH} ; no load	2	2.5	3	V
V _{CANHrecLP}	CANH voltage level in recessive state (low power mode)	V ₁ standby mode; V _{TXDC} = V _{TXDCHIGH} ; no load	-0.1	0	0.1	V
V _{CANLrecLP}	CANL voltage level in recessive state (low power mode)	V ₁ standby mode; V _{TXDC} = V _{TXDCHiGH} ; no load	-0.1	0	0.1	V

Table 28. CAN transmitter and receiver: pins CANH and CANL (continued)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
V _{DIFF,recOUT}	Differential output voltage in recessive state (normal mode): VCANHrec - VCANLrec	Active mode; V _{TXDC} = V _{TXDCHIGH} ; no load	-50		50	mV
V _{DIFF,recOUTL}	Differential output voltage in recessive state (low power mode): V _{CANHrec} - V _{CANLrec}	V ₁ standby mode; V _{TXDC} = V _{TXDCHIGH} ; no load	-50		50	mV
V _{CANHL,CM}	Common mode Bus voltage	Measured with respect to the ground of each CAN node	-12		12	V
I _{OCANH,dom}	CANH output current in dominant state	Active mode; V _{TXDC} = V _{TXDCLOW} ; V _{CANH} = 0 V	-160	-75	-45	mA
I _{OCANL,dom}	CANL output current in dominant state	Active mode; V _{TXDC} = V _{TXDCLOW} ; V _{CANL} = 5 V	45	75	160	mA
I _{Leakage}	Input leakage current	Unpowered device; V _{BUS} = 5 V	0		250	μA
R _{in}	Internal resistance	Active mode & V ₁ standby mode; V _{TXDC} = V _{TXDCHIGH} ; no load	20	27.5	38	kΩ
R _{in,matching}	Internal resistor matching CANH, CANL	Active mode & V ₁ standby mode; V _{TXDC} = V _{TXDCHIGH} ; no load R _{in} (CANH) - R _{in} (CANL)			3	%
R _{in,diff}	Differential internal resistance	Active mode & V ₁ standby mode; V _{TXDC} = V _{TXDCHIGH} ; no load	50	60	75	kΩ
C _{in}	Internal capacitance	Guaranteed by design		20		pF
C _{in,diff}	Differential internal capacitance	Guaranteed by design		10		pF
V_{THdom}	Differential receiver threshold voltage recessive to dominant state (normal mode)	Active mode			0.9	V
$V_{THdomLP}$	Differential receiver threshold voltage recessive to dominant state (low power mode)	V ₁ standby mode			1.15	V
V_{THrec}	Differential receiver threshold voltage dominant to recessive state (normal mode)	Active mode	0.5			V
V _{THrecLP}	Differential receiver threshold voltage dominant to recessive state (low power mode)	V ₁ standby mode	0.4			V

Table 29. CAN transceiver timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
tTXpd,hl	Propagation delay TXDC to RXDC (high to low)	Active mode; 50 % V_{TXDC} to 50 % V_{RXDC} ; C_{RXDC} = 100 pF; R_L = 60 Ω	0		255	ns
tTXpd,lh	Propagation delay TXDC to RXDC (low to high)	Active mode; 50 % V_{TXDC} to 50 % V_{RXDC} ; C_{RXDC} = 100 pF; R_L = 60 Ω	0		255	ns
t _{wake}	Wake up filter time		0.5		5	μs
t _{dom(TXDC)}	TXDC dominant time-out			700		μs
t _{CAN}	CAN permanent dominant time-out			700		μs

5.5.12 LIN transceiver^(c)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V \leq V_S \leq 18 V; 4.8 V \leq V₁ \leq 5.2 V; T_{junction} = -40 °C to 130 °C unless otherwise specified.

Table 30. LIN transmit data input: pin TXD

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{TXDLOW}	Input voltage dominant level	Active mode; V ₁ = 5 V	1,35	1.8		V
V _{TXDHIGH}	Input voltage recessive level	Active mode; V ₁ = 5 V		2.7	2.9	V
V _{TXDHYS}	V _{TXDHIGH} -V _{TXDLOW}	Active mode; V ₁ = 5 V	0.7	1		V
R _{TXDPU}	TXD pull up resistor	Active mode; V ₁ = 5 V	10	20	35	kΩ

Table 31. LIN receive data output: pin RXD

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{RXDLOW}	Output voltage dominant level	Active mode; V ₁ = 5 V, I _{LOAD1} = 2 mA		0.2	0.5	V
V _{RXDHIGH}	Output voltage recessive level	Active mode; V ₁ = 5 V, I _{LOAD1} = 2 mA	4.5			V

Table 32. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4*V _S	0.45*V _S	0.5*V _S	V
V _{Busdom}	Receiver dominant state				0.4*V _S	V

58/102 Doc ID 17639 Rev 4

c. LIN 2.1 compliant for Baud rates up to 20 kBit/s SAE J2602 compatible

Table 32. LIN transmitter and receiver: pin LIN (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{THrec}	Receiver threshold voltage dominant to recessive state		0.5*V _S	0.55*V _S	0.6*V _S	٧
V _{Busrec}	Receiver recessive state		0.6*V _S			V
V_{THhys}	Receiver threshold hysteresis: V _{THrec} -V _{THdom}		0.07*V _S	0.1*V _S	0.175*V _S	V
V _{THcnt}	Receiver tolerance center value: (V _{THrec} +V _{THdom})/2		0.475*V _S	0.5*V _S	0.525*V _S	V
V_{THwkup}	Receiver wakeup threshold voltage		1.0	1.5	2	V
$V_{THwkdwn}$	Receiver wakeup threshold voltage		V _S -3.5	V _S -2.5	V _S -1.5	٧
t _{linbus}	Dominant time for wakeup via bus	Sleep mode; edge: rec-dom		64*T _{OSC}		μs
I _{LINDomSC}	Transmitter input current limit in dominant state	$V_{TXD} = V_{TXDLOW};$ $V_{LIN} = V_{BATMAX} = 18 \text{ V}$	40	100	180	mA
I _{bus_PAS_dom}	Input leakage current at the receiver incl. pull-up resistor	$V_{TXD} = V_{TXDHIGH};$ $V_{LIN} = 0 \text{ V}; V_{BAT} = 12 \text{ V}^{(1)}$	-1			mA
I _{bus_PAS_rec}	Transmitter input current in recessive state	$\begin{aligned} &V_{TXD} = V_{TXDHIGH};\\ &8 \ V < V_{LIN};\\ &V_{BAT} < 18 \ V; \ V_{LIN} >= V_{BAT}\\ &\text{in standby modes} \end{aligned}$			20	μA
I _{bus_NO_GND}	Input current if loss of GND at device	GND = V _S ; 0 V < V _{LIN} < 18 V; V _{BAT} = 12 V	-1		1	mA
I _{bus}	Input current if loss of V _{BAT} at device	GND = V _S ; 0 V < V _{LIN} < 18 V			100	μA
V_{LINdom}	LIN voltage level in dominant state	Active mode; V _{TXD} = V _{TXDLOW} ; I _{LIN} = 40 mA			1.2	V
V _{LINrec}	LIN voltage level in recessive state	Active mode; V _{TXD} = V _{TXDHIGH} ; I _{LIN} = 10 μA	0.8*V _S		1	V
R _{LINup}	LIN output pull up resistor	V _{LIN} = 0 V	20	40	60	kΩ

^{1.} Slave mode.

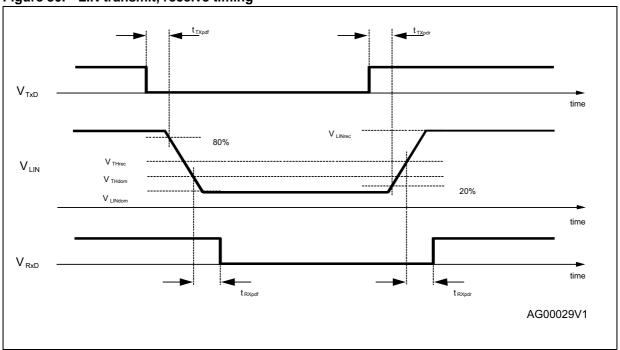
Table 33. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
^t RXpd	Receiver propagation delay time	$\begin{split} t_{RXpd} &= \text{max } (t_{RXpdr}, t_{RXpdf}); \\ t_{RXpdf} &= t(0.5 \ V_{RXD}) - t(0.45 \ V_{LIN}); \\ t_{RXpdr} &= t(0.5 \ V_{RXD}) - t(0.55 \ V_{LIN}); \\ V_{S} &= 12 \ V; \ C_{RXD} = 20 \ \text{pF}; \\ R_{bus}, &= 1 \ \text{k}\Omega, \ C_{bus} = 1 \ \text{nF}; \\ R_{bus} &= 660 \ \Omega, \ C_{bus} = 6.8 \ \text{nF}; \\ R_{bus} &= 500 \ \Omega, \ C_{bus} = 10 \ \text{nF} \end{split}$			6	μs
t _{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	$\begin{aligned} t_{\text{RXpd_sym}} &= t_{\text{RXpdr}} - t_{\text{RXpdf}}; \\ V_{\text{S}} &= 12 \text{ V}; \\ R_{\text{bus}} &= 1 \text{ k}\Omega, C_{\text{bus}} = 1 \text{ nF} \end{aligned}$	-2		2	μs
D1	Duty cycle 1	$\begin{split} TH_{Rec}(\text{max}) &= 0.744^* \text{V}_{\text{S}}; \\ TH_{Dom}(\text{max}) &= 0.581^* \text{V}_{\text{S}}; \\ \text{V}_{\text{S}} &= 7 \text{ V to 18 V, } t_{bit} = 50 \mu\text{s}; \\ \text{D1} &= t_{bus_rec}(\text{min})/(2xt_{bit}); \\ R_{bus} &= 1 \text{ k}\Omega, \text{ C}_{bus} = 1 \text{ nF}; \\ R_{bus} &= 660 \Omega, \text{ C}_{bus} = 6.8 \text{ nF}; \\ R_{bus} &= 500 \Omega, \text{ C}_{bus} = 10 \text{ nF} \end{split}$	0.396			
D2	Duty cycle 2	$\begin{split} & TH_{Rec}(min) = 0.284^*V_S; \\ & TH_{Dom}(min) = 0.422^*V_S; \\ & V_S = 7.6 \text{ to } 18 \text{ V}, t_{bit} = 50 \mu\text{s}; \\ & D2 = t_{bus_rec}(max)/(2xt_{bit}); \\ & R_{bus} = 1 k\Omega, C_{bus} = 1 nF; \\ & R_{bus} = 660 \Omega, C_{bus} = 6.8 nF; \\ & R_{bus} = 500 \Omega, C_{bus} = 10 nF \end{split}$			0.581	
D3	Duty cycle 3	$\begin{split} TH_{Rec}(\text{max}) &= 0.778^*\text{V}_{\text{S}}; \\ TH_{Dom}(\text{max}) &= 0.616^*\text{V}_{\text{S}}; \\ \text{V}_{\text{S}} &= 7 \text{ V to 18 V, } t_{bit} = 96 \mu\text{s}; \\ \text{D3} &= t_{bus_rec}(\text{min})/(2xt_{bit}); \\ R_{bus} &= 1 \text{ k}\Omega, \text{ C}_{bus} = 1 \text{ nF}; \\ R_{bus} &= 660 \Omega, \text{ C}_{bus} = 6.8 \text{ nF}; \\ R_{bus} &= 500 \Omega, \text{ C}_{bus} = 10 \text{ nF} \end{split}$	0.417			
D4	Duty cycle 4	$\begin{split} &TH_{Rec}(min) = 0.251^*V_S; \\ &TH_{Dom}(min) = 0.389^*V_S; \\ &V_S = 7.6 \text{ V to } 18 \text{ V, } t_{bit} = 96 \mu\text{s;} \\ &D4 = t_{bus_rec}(max)/(2xt_{bit}); \\ &R_{bus} = 1 k\Omega, C_{bus} = 1 nF; \\ &R_{bus} = 660 \Omega, C_{bus} = 6.8 nF; \\ &R_{bus} = 500 \Omega, C_{bus} = 10 nF \end{split}$			0.590	
t _{dom(TXDL)}	TXDL dominant time-out			12		ms
t _{LIN}	LIN permanent recessive time-out			40		μs
t _{dom(BUS)}	LIN bus permanent dominant time-out			12		ms

Table 34. LIN pull-up: pin LINPU

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
RDS _{ON}	ON resistance			10.5	16	Ω
I _{leak}	Leakage current				1	μΑ

Figure 30. LIN transmit, receive timing



5.5.13 Operational amplifier

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; T_i = -40 °C to 130 °C, unless otherwise specified.

Table 35. Operational amplifier

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
GBW	GBW product		1	3.5	7.0	MHz
AVOL _{DC}	DC open loop gain		80			dB
PSRR	Power supply rejection	DC, Vin = 150 mV	80			dB
V _{off}	Input offset voltage		-5		+5	mV
V _{ICR}	Common mode input range		-0.2	0	3	V
V _{OH}	Output voltage range high	I _{LOAD} = 1 mA to Gnd	V _S -0.2		Vs	V
V _{OL}	Output voltage range low	$I_{LOAD} = 1 \text{ mA to } V_S$	0		0.2	V
I _{Lim+}	Output current limitation +	DC	10	15	30	mA
I _{lim-}	Output current limitation -	DC	-10	15	-30	mA

Table 35. Operational amplifier (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
SR+	Slew rate positive		1	4	10	V/µs
SR-	Slew rate negative		-1	-4	-10	V/µs

Note:

The operational amplifier is on-chip stabilized for external capacitive loads $C_L \le 25$ pF (all operating conditions)

5.5.14 SPI

Input: CSN

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Input: CSN

Table 36. Input: CSN

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
VCSNLOW	Input voltage low level	Normal mode, V ₁ = 5 V	1.35	1.8		V
VCSNHIGH	Input voltage high level	Normal mode, V ₁ = 5 V		2.7	2.9	V
VCSNHYS	VCSNHIGH - VCSNLOW	Normal mode, V ₁ = 5 V	0.6	1.0	1.5	٧
ICSNPU	CSN pull up resistor	Normal mode, V ₁ = 5 V	10	20	35	kΩ

CLK, DI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 37. Input CLK, DI

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t _{set}	delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	μs
V _{in L}	input low level	V ₁ = 5 V	1.0	2.05	2.5	V
V _{in H}	input high level	V ₁ = 5 V	1.5	2.8	3.5	V
V _{in Hyst}	input hysteresis	V ₁ = 5 V	0.4	0.75	1.5	V
I in	pull down current at input	V _{in} = 1.5 V	5	30	60	μΑ

Table 37. Input CLK, DI (continued)

Symbol	Parameter Test condition		Min.	Тур.	Max.	Unit
C _{in} ⁽¹⁾	input capacitance at input CSN, CLK, DI and PWM _{1,2}	0 V < V ₁ < 5.3 V		10	15	pF
f _{CLK}	SPI input frequency at CLK				1	MHz

^{1.} Value of input capacity is not measured in production test. Parameter guaranteed by design.

DI timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 38. DI timing⁽¹⁾

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t _{CLK}	Clock period	V ₁ = 5 V	1000	-		ns
t _{CLKH}	Clock high time	V ₁ = 5 V	400	-		ns
t _{CLKL}	Clock low time	V ₁ = 5 V	400	-		ns
t _{set CSN}	CSN setup time, CSN low before rising edge of CLK	V ₁ = 5 V	400	-		ns
t _{set CLK}	CLK setup time, CLK high before rising edge of CSN	V ₁ = 5 V	400	-		ns
t _{set DI}	DI setup time	V ₁ = 5 V	200	-		ns
t _{hold DI}	DI hold time	V ₁ = 5 V	200	-		ns
t _{r in}	Rise time of input signal DI, CLK, CSN	V ₁ = 5 V		-	100	ns
t _{f in}	Fall time of input signal DI, CLK, CSN	V ₁ = 5 V		-	100	ns

^{1.} See Figure 32.

DO

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 39. DO output pin

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{DOL}	Output low level	$V_1 = 5 \text{ V}, I_D = -4 \text{ mA}$			0.5	V
V _{DOH}	output high level	V = 5 V, I _D = 4 mA	4.5			V

Table 39. DO output pin (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I _{DOLK}	3-state leakage current	$V_{CSN} = V_1, 0 V < V_{DO} < V_1$	-10		10	μΑ
C _{DO} ²	3-state input capacitance	$V_{CSN} = V_1,$ 0 V < V ₁ < 5.3 V		10	15	pF

DO timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 40. DO timing⁽¹⁾

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t _{r DO}	DO rise time	$C_L = 100 \text{ pF}, I_{LOAD} = -1 \text{ mA}$	-	50	100	ns
t _{f DO}	DO fall time	$C_L = 100 \text{ pF}, I_{LOAD} = 1 \text{ mA}$	-	50	100	ns
t _{en DO tri L}	DO enable time from 3-state to low level	$C_L = 100 \text{ pF}, I_{LOAD} = 1 \text{ mA}$ pull-up load to V_1	-	50	250	ns
t _{dis DO L tri}	DO disable time from low level to 3-state	L TIP LOAD		50	250	ns
t _{en DO tri H}	DO enable time from 3-state to high level	C _L = 100 pF, I _{LOAD} = -1 mA pull-down load to GND	-	50	250	ns
t _{dis DO H tri}	DO disable time from high level to 3-state	E I ZOND		50	250	ns
t _{d DO} DO delay time		$V_{DO} < 0.3 V_1,$ $V_{DO} > 0.7 V_1,$ $C_L = 100 pF$	-	50	250	ns

^{1.} See Figure 33 and Figure 34.

CSN timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V \leq V_S \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 41. CSN timing⁽¹⁾

Symbol	Parameter	Test Condition		Тур.	Max.	Unit
I triski Hi min	Minimum CSN HI time, active mode	Transfer of SPI-command to Input register	6			μs
t _{CSNfail}	CSN low timeout	Tested by scan chain	20	35	50	ms

^{1.} See Figure 35.

RXDL/NINT timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

 $6V \le V_S \le 18~V$; 4.5 $V \le V_1 \le 5.3~V$; all outputs open; $T_j = -40~^{\circ}C$ to 130 $^{\circ}C$, unless otherwise specified.

Table 42. RXDL/NINT timing

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t _{Interupt}	Interrupt pulse duration	Walk-up from V _{1-standby}	_	56	_	μs

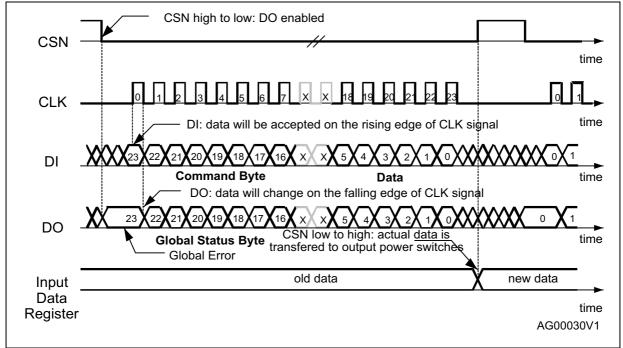
5.5.15 Inputs TxD_C and TxD_L for Flash mode

6 V \leq Vs \leq 18 V; 4.5 V \leq V₁ \leq 5.3 V; T_j = -40 °C to 130 °C, voltages are referred to PGND, all outputs open

Table 43. Inputs TxD_C and TxD_L for Flash mode

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{FlashL}	Input low level (V _{TXDC/L} for transition into Flash mode)	V ₁ = 5 V	6.1	7.25	8.4	V
V _{FlashH}	Input high level (V _{TXDC/L} for exit from Flash mode)	V ₁ = 5 V	7.4	8.4	9.4	V
V _{FlashHYS}	Input Voltage Hysteresis	V ₁ = 5 V	0.6	0.8	1.0	V

Figure 31. SPI – transfer timing diagram



The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 32. SPI - input timing

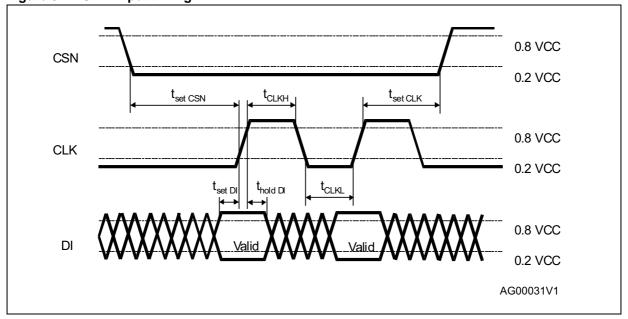


Figure 33. SPI output timing (part 1)

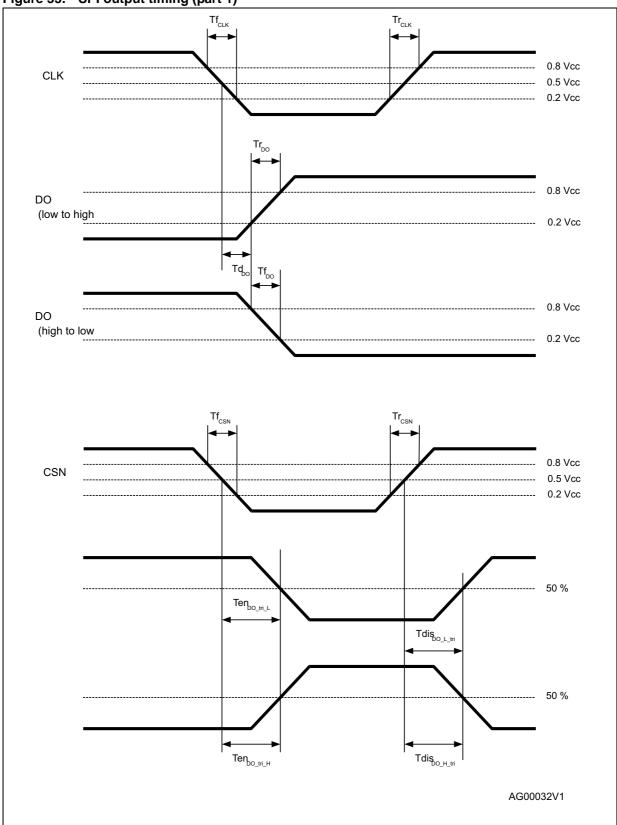


Figure 34. SPI output timing (part 2)

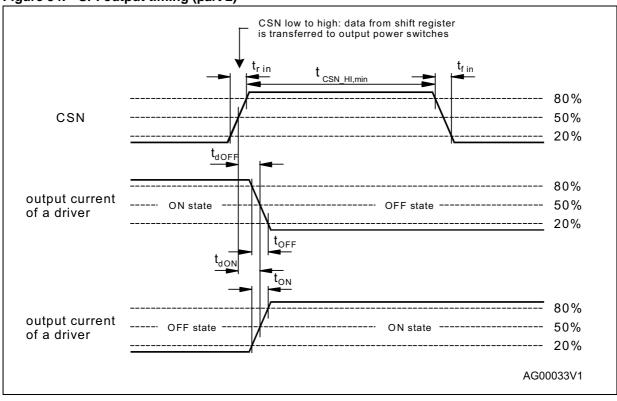
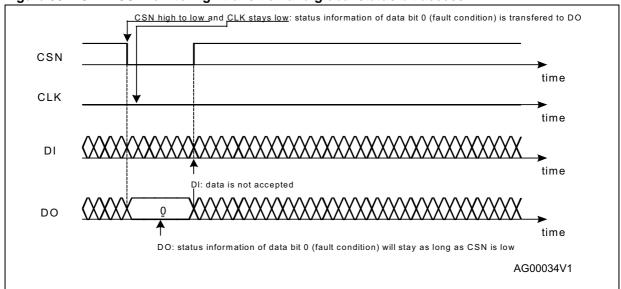


Figure 35. SPI - CSN low to high transition and global status bit access



L99PM62GXP ST SPI

6 ST SPI

6.1 SPI communication flow

6.1.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines.

At device start-up the master reads the *<SPI-frame-ID>* register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (24bit) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by 2 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 2 data bytes (i. e. 'In-frame-response').

For write cycles the *<Global Status>* register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

A write command is only accepted as a valid command by the device if the counted number of clocks is exact 24, otherwise the command is rejected.

Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Write>, <Read>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

Table 44. Command byte

MSB							LSB
Оро	code			Add	ress		
OC1	OC0	A5	A4	А3	A2	A1	A0

OCx: operating code

Ax: address

6.1.2 Operating code definition

Table 45. Operating code definition

OC1	OC0	Meaning
0	0	<write mode=""></write>
0	1	<read mode=""></read>

ST SPI L99PM62GXP

Table 45. Operating code definition (continued)

OC1	OC0	Meaning
1	0	<read and="" clear="" status=""></read>
1	1	<read device="" information=""></read>

The <Write Mode> <Read Mode> and <Read and Clear Status> operations allow access to the RAM of the device, i. e. to write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register.

A <Read and Clear Status> operation with address 3FH clears all status registers (including the Global Status Register). Configuration register is read by this operation.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version, register width and availability of a watchdog.

More detailed descriptions of the device information are available in 'Read Device Information'.

6.1.3 Global status register^(d)

Table 46. Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset OR comm error)	TSD2	TSD1	V ₁ Fail	VS Fail (OV/UV)	Fail safe

6.1.4 Configuration register

The <Configuration> register is accessible at RAM address 3FH.

For the config register, the 8 bits are located in the low byte (LSB).

The configuration register is implemented for compliance purpose to ST SPI standard.

Table 47. Configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	WD trigger

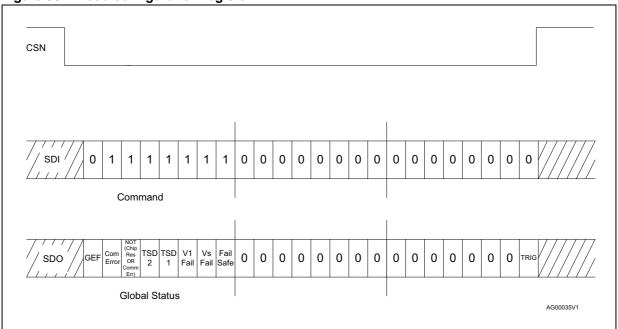
<WD trigger>: this bit is reserved to serve the watchdog.

70/102 Doc ID 17639 Rev 4

d. See Section 6.2 for details.

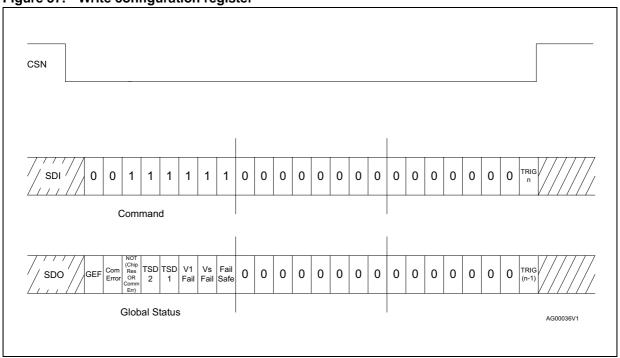
L99PM62GXP ST SPI





The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0

Figure 37. Write configuration register⁽¹⁾



The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0

ST SPI L99PM62GXP

6.1.5 Address mapping

Table 48. Address mapping

	raan ooo mapping		
RAM adress	Description	Access	
3FH	<configuration></configuration>	R/W	
13H	Status register 3	R	
12H	Status register 2	R	
11H	Status register 1	R	
06H	Control register 6	R/W	
05H	Control register 5	R/W	
04H	Control register 4	R/W	
03H	Control register 3	R/W	
02H	Control register 2	R/W	
01H	Control register 1	R/W	
00H	00H Reserved		

ROM adress	Description	Access	
3FH	FH Reserved		
3EH	<spi frame="" id=""></spi>	R	
	Unused	N/A	
03H	<pre><pre><pre><pre><pre><pre><pre><pre></pre></pre></pre></pre></pre></pre></pre></pre>	N/A	
02H	<pre><pre><pre><pre><pre><pre><pre><pre></pre></pre></pre></pre></pre></pre></pre></pre>	R	
01H	<silicon version=""></silicon>	R	
00H	<id header=""></id>	R	

The RAM memory area consists of 16 bit registers.

For the device information (ROM memory area) the eight most significant bits of the memory cell are used. The remaining 8 are zero.

All unused RAM and ROM addresses is read as '0'.

Note:

- 1 The register definition for RAM address 00H is unused. A register value of all 0 must cause the device to enter a fail-safe state (interpreted as 'SDI stuck to GND' failure).
- 2 ROM address 3FH is unused. An attempt to access this address must be recognized as a communication error ('SDI stuck to V_{CC}' failure) and must cause the device to enter a fail-safe state.

6.1.6 Write operation

The write operation starts with a command byte followed by 2, data bytes. The number of data bytes is specified in the *<SPI-frame-ID>*.

Write command format

Table 49. Write command format: command byte

MSB									
Op (Op Code		Address						
0	0	A5	A4	А3	A2	A1	A0		

Table 50. Write command format: data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 51. Write command format: data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

OC0, OC1:operating code (00 for 'write' mode)

A0 to A5:address bits

An attempt to write 00H at RAM address 00H is recognized as a failure (SDI stuck to GND). The device enters a fail-safe state.

6.1.7 Format of data shifted out at SDO during write cycle

Table 52. Format of data shifted out at SDO during write cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V ₁ Fail	V _S Fail (OV/UV)	Fail safe

Table 53. Format of data shifted out at SDO during write cycle: data byte 1

MSB		Previous content of addressed register					
D15	D14	D13	D12	D11	D10	D9	D8

Table 54. Format of data shifted out at SDO during write cycle: data byte 2

MSB		Previous	content of	addressed re	egister		LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the previous content of the accessed register.

CSN A5 A4 A3 A2 A1 A0 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 Command 1st Databyte 2nd Databyte TSD Vs | Fail | D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 2 1st Databyte 2nd Databyte Global Status (previous content of register) (previous content of register) AG00037V1

Format of data shifted out at SDO during write cycle

6.1.8 **Read operation**

The read operation starts with a command byte followed by 2 data bytes. The number of data bytes is specified in the *<SPI-frame-ID>*. The content of the data bytes is 'don't care'. The content of the addressed register is shifted out at SDO within the same frame ('in-frame response').

Read command format

Table 55. Read command format: command byte

MSB							LSB	
Op C	Code		Address					
0	1	A5	A4	A3	A2	A1	A0	

Table 56. Read command format: data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Table 57. Read command format: data byte 2

MSB							LSB
0	0	0	0	0	0	0	0

OC0, OC1:operating code (01 for 'read' mode)

A0 to A5:address bits

6.1.9 Format of data shifted out at SDO during read cycle

Table 58. Format of data shifted out at SDO during read cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V ₁ Fail	V _S Fail (OV/UV)	Fail safe

Table 59. Format of data shifted out at SDO during read cycle: data byte 1

MSB		Previous	content of	addressed re	egister		LSB
D15	D14	D13	D12	D11	D10	D9	D8

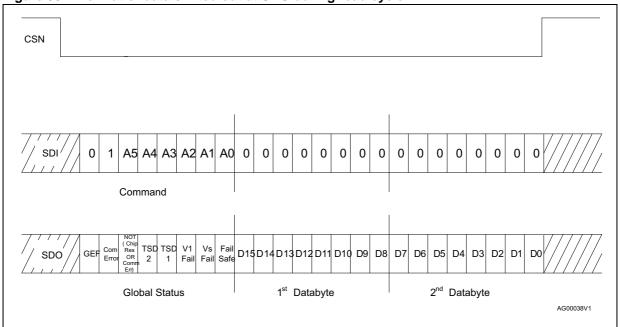
Table 60. Format of data shifted out at SDO during read cycle: data byte 2

MSB		Previous	content of	addressed re	egister		LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 39. Format of data shifted out at SDO during read cycle



6.1.10 Read and clear status operation

The 'Read and Clear Status' operation starts with a command byte followed 2 data bytes. The number of data bytes is specified in the *<SPI-frame-ID>*. The content of the data bytes is 'don't care'. The content of the addressed status register is transferred to SDO within the same frame ('in-frame response') and is subsequently cleared.

A 'Read and Clear Status' operation with address 3FH clears all status registers (incl. the *<Global Status>* register). The configuration register is read by this operation.

Read and clear status command format

Table 61. Read and clear status command format: command byte

MSB							LSB
Op C	Code			Add	ress		
1	01	A5	A4	А3	A2	A1	A0

Table 62. Read and clear status command format: data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Table 63. Read and clear status command format: data byte 2

MSB							LSB
0	0	0	0	0	0	0	0

OC0, OC1:operating code (10 for 'read and clear status' mode)

A0 to A5:address bits

Format of data shifted out at SDO during read and clear status operation

Table 64. Format of data shifted out at SDO during read and clear status: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V ₁ Fail	V _S Fail (OV/UV)	Fail safe

Table 65. Format of data shifted out at SDO during read and clear status: data byte 1

MSB	MSB Previous content of addressed register						
D15	D14	D13	D12	D11	D10	D9	D8

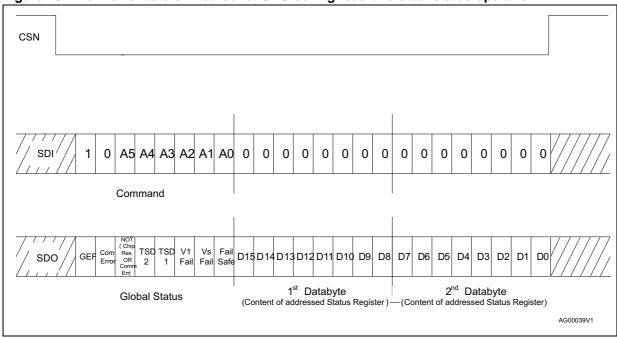
Table 66. Format of data shifted out at SDO during read and clear status: data byte 2

MSB	Previous content of addressed register						
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 40. Format of data shifted out at SDO during read and clear status operation



6.1.11 Read device information

The device information is stored at the ROM addresses defined below and is read using the respective operating code.

Table 67. Read device information

Оро	ode	ROM	Device information	Value	
OC1	OC0	address	Device information	value	
1	1	3FH	Reserved	00	
1	1	3EH	<spi frame="" id=""> includes frame width and availability of watchdog</spi>	42 Hex	
1	1	04H to 3DH	unused	00	
1	1 1 03H ·		<pre><pre><pre><pre><pre><pre><pre><pre></pre></pre></pre></pre></pre></pre></pre></pre>	4B Hex	

Table 67. Read device information (continued)

Оро	code	ROM	Device information	Value	
OC1	OC0	address	Device information		
1	1	02H	<pre><pre><pre><pre><pre><pre><pre><pre></pre></pre></pre></pre></pre></pre></pre></pre>	13 Hex	
1	1	01H	<silicon version=""> indicates Design Version</silicon>	According to silicon version	
1	1 1 00H <id header=""> device family</id>		<id header=""> device family max adress of device information</id>	43 Hex	

The <*ID-Header*> (ROM address 00H) indicates the product family and specifies the highest address which contains product information

Table 68. ID-header

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0	1	0	0	0	0	1	1		
Family Idea	ntifier	Highest address containing device information							

< Family Identifier>:01 Hex (BCD)

Table 69. Family identifier

Bit 7 Bit 6		Meaning			
0	0	VIPower			
0 1		BCD			
1	0	VIPower hybrid			
1	1	Tbd			

The <*Product Code 1>* (ROM address 02H) and <*Product Code 2>* (ROM address 03H) represents a unique code to identify the product name.

The *<Silicon Version>* (ROM address 01H) provides information about the silicon version according to the table below:

Table 70. Silicon version identifier

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Rese	erved			Silicon	version	

<Highest address>:03 Hex

<Pre><Product Code 1> 13 Hex

<Pre><Pre>roduct Code 2> 4B Hex

The *<SPI-frame-ID>* (ROM address 3EH) provides information about the register width (1, 2, 3 bytes) and the availability of 'Burst Mode Read' and watchdog.

Table 71. SPI-frame-ID

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------|--------|--------|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| BR | WD | Х | Х | Х | 32-bit | 24-bit | 16-bit |

BR:burst-mode read (1 = burst-mode read is supported)

WD:watchdog (1 = available, 0 = not available)

32-bit, 24-bit, 16-bit: width of SPI frame (see table below)

<Burst Mode>:not supported

<Watchdog>:available

<Frame Width>:24 bit

6.2 SPI registers

6.2.1 Overview

Overview command byte

Table 72. SPI register: command byte

| Read/write | | Address | | | | | | |
|------------|---|---------|---|---|---|---|---|--|
| Х | х | х | х | х | х | х | х | |

Table 73. SPI register: mode selection

| Read/w | rite | Mode selection | | | | | | |
|--------|------|------------------|--|--|--|--|--|--|
| 0 | 0 | Write | | | | | | |
| 0 | 1 | Read | | | | | | |
| 1 | 0 | Read and clear | | | | | | |
| 1 | 1 | Read device info | | | | | | |

Table 74. SPI register: CTRL register selection

| | | CTRL reg | ister 16 | | | CTRL register selection |
|---|---|----------|----------|---|---|-------------------------|
| 0 | 0 | 0 | 0 | 0 | 1 | CTRL register1 |
| 0 | 0 | 0 | 0 | 1 | 0 | CTRL register2 |
| 0 | 0 | 0 | 0 | 1 | 1 | CTRL register3 |
| 0 | 0 | 0 | 1 | 0 | 0 | CTRL register4 |

Table 74. SPI register: CTRL register selection (continued)

| | | | CTRL register selection | | | |
|---|---|---|-------------------------|---|----------------|----------------|
| 0 | 0 | 0 | 1 | 1 | CTRL register5 | |
| 0 | 0 | 0 | 1 | 1 | 0 | CTRL register6 |

Table 75. SPI register: STAT register selection

| | | STAT regi | | STAT register selection | | |
|---|---|-----------|---|-------------------------|---|----------------|
| 0 | 1 | 0 | 0 | 0 | 1 | STAT register1 |
| 0 | 1 | 0 | 0 | 1 | 0 | STAT register2 |
| 0 | 1 | 0 | 0 | 1 | 1 | STAT register3 |

Overview of control register data bytes

6.2.2 Control registers

Table 76. Overview of control registers data bytes

| | | 1 st data byte <15:8> | | | | | | | | 2 nd data byte <7:0> | | | | | | |
|----------|--------------------------------------|----------------------------------|--------------------|--------------------|--------------------|--------------------------------|----------------------------------|----------------------------------|----------------------|---------------------------------|--------------------------|------------------------|-------------------|----------------------------|---------------------|-------------------------|
| | | | | | | | Cont | rol reg | ister | 1, data | | | | | | |
| Defaults | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |
| Function | OUT
HS | OUT
HS | OUT
4 | OUT
4 | OUT
HS_EXT | OUT
3 | OUT
2 | OUT
1 | REL
2 | REL
1 | V ₂ | V ₂ | Res | Stby
sel | Go
Stby | Trig |
| Group | | | | H | S control | | | | | | LS Out | tput, V ₂ a | nd mode | control | | |
| | Control r | | | | | | | | | 2, data | | | | | | |
| Defaults | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 1 | 1 | 1 |
| Function | Res | Res | Inp.
Filt 3 | Inp.
Filt 3 | Inp.
Filt 2 | Inp.
Filt 2 | Inp.
Filt 1 | Inp.
Filt1 | Res | Input
Pu/Pd 3 | Input
Pu/Pd 2 | Input
Pu/Pd 1 | Res | WU
EN 3 | WU
EN 2 | WU
EN 1 |
| Group | Wake-up control | | | | | | | | | | | Wake-up | control | | | |
| | | | | | | | Cont | rol reg | ister | 3, data | | | | | | |
| Defaults | | 0 | 0 | 0 | | 0 | 0 | 0 | | | 0 | 0 | 1 | 1 | 0 | 0 |
| Function | on Res T1 T1 T1 Res T2 T2 T2 Per Per | | | | | | | | Res | Res | WD
time | WD
time | LIN
WU
En | CAN
WU
En | Wake
timer
En | Wake
Timer
Select |
| Group | | I | I | Tim | er Settings | ; | I | l | | , | Watchdog | and cycl | ic wake ι | up setting | js | |
| | | | | | | | Cont | rol reg | ister | 4, data | | | | | | |
| Defaults | | 0 | 0 | 1 | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| Function | Res | I _{CMP} | OutHS
Rec
En | Vlock
Out
En | Res | LS
OV/UV
shut
down_en | V ₁
Reset
Level | V ₁
Reset
Level | LIN
Pu
En | Res | Lin
TxD
Tout
En | CAN
ACT | CAN
Loop
En | CAN
Patt.
wake
En | CAN
split
On | CAN
Rec
Only |
| Group | | | | Con | trol (other) |) | | | Transceiver settings | | | | | | | |
| | | | | | | | Cont | rol reg | ister | 5, data | | | | | | |
| Defaults | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Res | PWM2
Off-
DC | PWM2
Off-
DC | PWM2
Off-
DC | PWM2
Off-
DC | PWM2
Off-
DC | PWM2
Off-
DC | PWM2
Off-
DC | PWM
Freq | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC |
| Group | p PWM2 setting | | | | | | | | | | | PWM1 | setting | l | l | |
| | Control re | | | | | | | | | 6, data | | | | | | |
| Defaults | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Res | PWM4
Off-DC | PWM4
Off-DC | | PWM4
Off-
DC | PWM4
Off-
DC | PWM4
Off-DC | PWM4
Off-DC | Res | PWM3
ON-
DC | PWM3
ON-
DC | PWM3
ON-
DC | PWM3
ON-
DC | PWM3
ON-
DC | PWM3
ON-
DC | PWM3
ON-
DC |
| Group | | • | • | PW | M4 setting | • | • | • | PWM3 setting | | | | | | | |

Table 77. Control register 1: command and data bytes

| | Com | man | d byt | е | 1 st data byte | 2 nd data byte | | | |
|------|---------------|-----|-------|-----|---------------------------|---------------------------|---|------------|-------------|
| Read | d/write | | | Add | | | | | |
| Х | x 0 0 0 0 0 1 | | | | | 0 | 1 | Data, 8bit | Data, 8 bit |

Table 78. Control register 1, data bytes

| | <u> </u> | | | | | | | | | | | | | | | |
|----------|----------------------------------|-------------|------------|------------|---------------|----------|----------|---------------------------------|--------------------------------------------|----------|------------------|------------------|-----|-------------|------------|------|
| | 1 st data byte <15:8> | | | | | | | 2 nd data byte <7:0> | | | | | | | | |
| Defaults | 0 0 0 0 0 0 0 0 | | | | | | | | | 0 | 0 | 0 | | 0 | 0 | 0 |
| Function | OUT
HS_2 | OUT
HS_1 | OUT
4_2 | OUT
4_1 | OUT
HS_EXT | OUT
3 | OUT
2 | OUT
1 | REL
2 | REL
1 | V _{2_2} | V _{2_1} | Res | Stby
sel | Go
Stby | Trig |
| Group | | HS control | | | | | | | LS Output, V ₂ and mode control | | | | | | | |

Table 79. Control register 1, bits

| Bit | Name | | | Comi | ment | | | | | | | |
|-----|-----------|---------------------------------------------|---------|---------------------------|---------------------------|--------------|--|--|--|--|--|--|
| 15 | OUTHS | Select mode of | OUTHS | | | | | | | | | |
| 14 | | OUTHS_EXT | OUTHS_2 | OUTHS_1 | | Mode | | | | | | |
| | | 0 | 0 | 0 | HS off | | | | | | | |
| | | 0 | 0 | 1 | HS cyclic on with timer 1 | 1 | | | | | | |
| | | 0 | 1 | 0 | HS controlled by PWM4 | Active and | | | | | | |
| | | 0 | 1 | 1 | HS cyclic on with Timer 2 | standby mode | | | | | | |
| | | 1 | 1 | 0 | PWM3 | | | | | | | |
| | | 1 | X | 1 | HS on | | | | | | | |
| | | | | | | | | | | | | |
| 13 | OUT4 | Select mode of | OUT4 | | | | | | | | | |
| 12 | | OUT4_2 | OUT4_1 | | Mode | | | | | | | |
| | | 0 | 0 | HS off | | | | | | | | |
| | | 0 | 1 | HS on | | | | | | | | |
| | | 1 | 0 | HS controlled
by PWM4 | Active and standby mode | | | | | | | |
| | | 1 | 1 | HS cyclic on with Timer 2 | | | | | | | | |
| | | | | | • | - | | | | | | |
| 11 | OUTHS_EXT | Extended function of OUTHS; see table OUTHS | | | | | | | | | | |

Table 79. Control register 1, bits (continued)

| Bit | Name | | | Comr | nent |
|-----|------|---------------|---------------|-------------------------|------|
| 10 | OUT3 | Select mode o | f OUT3 | | |
| | | OUT3 | | Mode | |
| | | 0 | Select FSO | Active and standby mode | |
| | | 1 | Select PWM3 | | |
| | | | | | |
| 9 | OUT2 | Select mode o | f OUT2 | | |
| | | OUT2 | | Mode | |
| | | 0 | Select PWM2 | Active and | |
| | | 1 | Select timer2 | standby mode | |
| | | | | | |
| 8 | OUT1 | Select mode o | f OUT1 | 1 | |
| | | OUT1 | | Mode | |
| | | 0 | Select PWM1 | Active and | |
| | | 1 | Select timer1 | standby mode | |
| | | | | | |
| 7 | REL2 | Select mode o | f REL2 | | |
| | | REL2 | | Mode | |
| | | 0 | REL2 off | Active and standby mode | |
| | | 1 | REL2 on | Active mode | |
| | | | | | |
| 6 | REL1 | Select mode o | f REL1 | 1 | |
| | | REL1 | | Mode | |
| | | 0 | REL1 off | Active and standby mode | |
| | | 1 | REL1 on | Active mode | |
| | | | | | |

Table 79. Control register 1, bits (continued)

| Bit | Name | | | Comment |
|-----|----------|------------------|---------------------------|-----------------------------------------------------------------------------------------------|
| 5 | V_2 | | | |
| 4 | | V _{2_2} | V _{2_1} | |
| | | 0 | 0 | V ₂ OFF in all modes |
| | | 0 | 1 | V ₂ ON in active mode; OFF in V ₁ /V _{BAT} standby mode |
| | | 1 | 0 | V ₂ ON in Active/V ₁ standby mode; OFF in V _{BAT} standby mode |
| | | 1 | 1 | V ₂ ON in all modes |
| | | | | |
| 3 | RES | Reserved | | |
| 2 | STBY_SEL | Select standby | mode | |
| | | 0 | V _{BAT} standby | mode |
| | | 1 | V ₁ standby mo | ode |
| | | | | |
| 1 | GO_STBY | Execute stand | by mode | |
| | | 0 | No action | |
| | | 1 | Execute stand | dby mode |
| | | | | |
| 0 | TRIG | Trigger Bit for | Watchdog | |

Table 80. Control register 2: command and data bytes

| | Com | man | d by | te | | 1 st data byte | 2 nd data byte | | |
|------|--------------------|-------------|------|----|--|---------------------------|---------------------------|------------|-------------|
| Read | Read/write Address | | | | | | | | |
| Х | х | 0 0 0 0 1 0 | | | | 1 | 0 | Data, 8bit | Data, 8 bit |

Table 81. Control register 2, data bytes

| | 1 st data byte <15:8> | | | | | | | | | 2 nd data byte <7:0> | | | | | | |
|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|-----------------|-----|----------------|---------------------------------|--------------|-----|-----------|-----------|-----------|---|
| Defaults | 0 0 0 0 0 | | | | | | | | | 0 | 0 | 0 | | 1 | 1 | 1 |
| Function | Res Res Wu3 Wu3 WU2 WU2 WU1 WU1 Filt_LSB Filt_LSB Filt_LSB Filt_LSB Filt_LSB Filt_LSB | | | | | | WU1
Filt_LSB | Res | WU3
Pu/Pd | WU2
Pu/Pd | WU1
Pu/Pd | Res | WU3
EN | WU2
EN | WU1
EN | |
| Group | Wakeup control | | | | | | | | Wakeup control | | | | | | | |

Table 82. Control register 2, bits

| Bit | Name | | | Comment |
|--------|-----------|--------------------|------------------|------------------------------------|
| 15 | Res | Reserved | | |
| 14 | Res | Reserved | | |
| 13, 12 | WU3_Filt | Wakeup filter cor | nfiguration | |
| 11, 10 | WU2_Filt | MSB | LSB | |
| 9, 8 | WU1_Filt | 0 | 0 | Static, 64 µs |
| | | 0 | 1 | Enabled with timer 2; 80 µs blank |
| | | 1 | 0 | Enabled with timer 2; 800 µs blank |
| | | 1 | 1 | Enabled with timer 1; 800 µs blank |
| | | | • | |
| 7 | Res | Reserved | | |
| 6 | WU3_Pu/Pd | Pull up or pull do | wn configuration | |
| 5 | WU2_Pu/Pd | 0 | Pull down | |
| 4 | WU1_Pu/Pd | 1 | Pull up | |
| | | | | |
| 3 | Res | Reserved | | |
| 2 | WU3_EN | Enable Wake up | source | |
| 1 | WU2_EN | 0 | Disable | |
| 0 | WU1_EN | 1 | Enable | _ |
| | | | | |

Table 83. Control register 3: command data bytes

| | Com | man | d by | te | | | 1 st data byte | 2 nd data byte | |
|------|--------------------|-----|------|----|--|--|---------------------------|---------------------------|-------------|
| Read | Read/write Address | | | | | | | | |
| х | x 0 0 0 0 1 1 | | | | | | 1 | Data, 8bit | Data, 8 bit |

Table 84. Control register 3, data bytes

| | 1 st data byte <15:8> | | | | | | | | | 2 nd data byte <7:0> | | | | | | | |
|----------|----------------------------------|----------|------------------|------------------|-----|----------|------------------|------------------|--------------------------------------|---------------------------------|-------------------|-------------------|-----------------|-----------------|---------------------|-------------------------|--|
| Defaults | 0 0 0 0 0 0 0 | | | | | | | | | | 0 | 0 | 1 | 1 | 0 | 0 | |
| Function | Res | T1
On | T1
Per
MSB | T1
Per
LSB | Res | T2
On | T2
Per
MSB | T2
Per
LSB | Res | Res | WD
time
MSB | WD
time
LSB | LIN
WU
En | CAN
WU
En | Wake
timer
En | Wake
timer
select | |
| Group | Timer Settings | | | | | | | | Watchdog and cyclic wake up settings | | | | | | | | |

Table 85. Control register 3, bits

| Bit | Name | | | | Comment | | | | | | |
|-----|------------|-----------------------------------------------------------------------|----------------|------------------|-------------------------------|--|--|--|--|--|--|
| 15 | RES | Reserved | | | | | | | | | |
| 14 | T1_On | Timer 1 "C | ON" time sele | ections | | | | | | | |
| | | 0 | 10 ms | | | | | | | | |
| | | 1 | 20 ms | | | | | | | | |
| | | | | , | | | | | | | |
| 13 | T1_Per_MSB | Timer 1 p | eriod selectio | n | | | | | | | |
| 12 | T1_Per_LSB | | | | | | | | | | |
| | | MSB | LSB | | | | | | | | |
| | | 0 | 0 | 1 s | | | | | | | |
| | | 0 | 1 | 2 s | | | | | | | |
| | | 1 | 0 | 3 s | | | | | | | |
| | | 1 | 1 | 4 s | | | | | | | |
| | | Timer 1 is | restarted wit | th a valid write | command to control register 3 | | | | | | |
| 11 | Res | | | | | | | | | | |
| 10 | T2_On | Timer 2 "C | ON" time sele | ection | | | | | | | |
| | | 0 | 0.1 ms | | | | | | | | |
| | | 1 | 1 ms | | | | | | | | |
| | | | | | | | | | | | |
| 9 | T2_Per_MSB | Timer 2 p | eriod selectio | n | | | | | | | |
| 8 | T2_Per_LSB | | 1 | T | 1 | | | | | | |
| | | MSB | LSB | | | | | | | | |
| | | 0 | 0 | 10 ms | | | | | | | |
| | | 0 | 1 | 20 ms | | | | | | | |
| | | 1 | 0 | 50 ms | | | | | | | |
| | | 1 | 1 | 200 ms | | | | | | | |
| | | Timer 2 is restarted with a valid write command to control register 3 | | | | | | | | | |
| 7 | Res | Reserved | | | | | | | | | |
| 6 | Res | Reserved | | | | | | | | | |

Table 85. Control register 3, bits (continued)

| Bit | Name | | | (| Comment |
|-----|-------------------|-----------------------|-----------------|-----------------------------|--------------------------------------------------------|
| 5 | WD_time_MSB | Trigger wi | ndow selection | on | |
| 4 | WD_time_LSB | | | | |
| | | MSB | LSB | | |
| | | 0 | 0 | 10 ms | |
| | | 0 | 1 | 50 ms | |
| | | 1 | 0 | 100 ms | |
| | | 1 | 1 | 200 ms | |
| | | | | | |
| 3 | LIN_WU_En | Enable LI | N as wake up | source | |
| | | 0 | Disabled | | |
| | | 1 | Enabled | | |
| | | | | | |
| 2 | CAN_WU_En | Enable C | AN as wake ι | ip source | |
| | | 0 | Disabled | | |
| | | 1 | Enabled | | |
| | | | | | |
| 1 | Wake_timer_En | Enable wa
(Nreset) | ake up by tim | er from V ₁ stan | ndby mode (Interrupt) or V _{BAT} standby Mode |
| | | 0 | Disabled | | |
| | | 1 | Enabled | | |
| | | | | | |
| 0 | Wake_timer_select | Timer sele | ection for time | er interrupt / wa | ake-up of µC by timer |
| | | 0 | Timer 2 | | |
| | | 1 | Timer 1 | | |
| | | | | | |

Table 86. Control register 4: command and data bytes

| | Com | man | d by | te | | | | 1 st data byte | 2 nd data byte |
|-----------------|--------|-----|------|-----|------|--|---|---------------------------|---------------------------|
| Read | /Write | | | Add | ress | | | | |
| x x 0 0 0 1 0 0 | | | | | | | 0 | Data, 8bit | Data, 8 bit |

Table 87. Control register 4, data bytes

| | | | 1 | st data b | yte < | 15:8> | | 2 nd data byte <7:0> | | | | | | | | |
|----------|---------------|------------------|--------------------|----------------------|-------|--------------------------------|----------------------------------|----------------------------------|-----------------|----------------------|--------------------------|------------|-------------------|----------------------------|--------------------|--------------------|
| Defaults | 0 0 1 0 1 0 0 | | | | | | | | | | 1 | 1 | 0 | 1 | 1 | 0 |
| Function | RES | I _{CMP} | OutHS
Rec
En | Vlock
Out_en | RES | LS
OV/UV
shut
down_en | V ₁
Reset
Lev_2 | V ₁
Reset
Lev_1 | LIN
Pu
En | Res | Lin
TxD
Tout
En | CAN
ACT | CAN
Loop
En | CAN
Patt.
wake
En | CAN
split
On | CAN
Rec
only |
| Group | | Control (other) | | | | | | | | Transceiver settings | | | | | | |

Table 88. Control register 4, bits

| Bit | Name | | Comment |
|-----|--------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------|
| 15 | Res | Reserved; must | be set to zero |
| 14 | I _{cmp} | V ₁ load current s | supervision |
| | | 0 | Enabled; Watchdog is disabled in V ₁ Standby when the V _{1loadcurrent} < I _{cmpthreshold} |
| | | 1 | Disabled; Watchdog is automatically disabled when V ₁ standby is entered |
| | | | |
| 13 | OUTHS_rec_en | Overcurrent Auto | o recovery mode for OUTHS |
| | | 0 | Disabled |
| | | 1 | Enabled |
| | | | <u> </u> |
| 12 | Vlock_out_en | Voltage lock out: | : OV/UV status |
| | | 0 | Over/under voltage status recovers automatically when condition disappears |
| | | 1 | Over/under voltage status is latched until a read and clear command is performed |
| | | | |
| 11 | Res | Reserved | |
| 10 | LS_OV/UV
shut_down_en | Shutdown of low | v-side drivers in case of over-/under voltage |
| | | 0 | No shutdown of low-sides in case of over/under voltage |
| | | 1 | Shutdown low-sides in case of over/under voltage |
| | | | |

Table 88. Control register 4, bits (continued)

| Bit | Name | | Co | mment | | | | | | |
|-----|-------------------|-------------------------------------|----------------------|---------------------------------|--------------------|--|--|--|--|--|
| 9 | V1Reset_level_1 | Select reset level | | | | | | | | |
| 8 | V1Reset_level_2 | | | | | | | | | |
| | | V1RSTlev_2 | V1RSTlev_1 | V1 reset level | | | | | | |
| | | 0 | 0 | 4.6 V | | | | | | |
| | | 0 | 1 | 4.35 V | | | | | | |
| | | 1 | 0 | 4.1 V | | | | | | |
| | | 1 | 1 | 3.8 V | | | | | | |
| | | | | | | | | | | |
| 7 | LIN_PU_EN | Enable internal Lin | pull up | | _ | | | | | |
| | | 0 | No LIN master pull | -up | | | | | | |
| | | 1 | LIN master pull-up | | | | | | | |
| | _ | | | | | | | | | |
| 6 | Res | Must be written to ' | | | | | | | | |
| 5 | Lin_TxD_Tout_En | Enable / disable monitoring via TxD | | | | | | | | |
| | | 0 | No TxD monitoring | | | | | | | |
| | | 1 | dominant for t > 12 | N transmitter is switch
! ms | ied off if TXDL is | | | | | |
| | | | 1 | | | | | | | |
| 4 | CAN_ACT | Activate CAN trans | ceiver | | | | | | | |
| | | 0 | CAN transceiver de | eactivated | Active mode | | | | | |
| | | 1 | CAN transceiver a | ctivated | Active mode | | | | | |
| | | | | | | | | | | |
| 3 | CAN_Loop_En | | CANTX to CANRXD | | 1 | | | | | |
| | | 0 | No looping | | | | | | | |
| | | 1 | TXDC is looped to | RXDC | | | | | | |
| 2 | CAN Dett walks Es | Cookle wettern well | o un for CAN | | | | | | | |
| 2 | CAN_Patt_wake_En | - | 1 | | | | | | | |
| | | 1 | No pattern wake up | | | | | | | |
| | | | Fattern wake up | | | | | | | |
| 1 | CAN_split_On | Enable SPLIT term | ination for CAN | | | | | | | |
| | · | 0 | Split termination di | | | | | | | |
| | | 1 | Split termination er | Active mode | | | | | | |
| | | | 1 | | | | | | | |

Table 88. Control register 4, bits (continued)

| Bit | Name | | Comment | | | | | | | | | | |
|-----|--------------|---------------------------------------|----------------------------|-------------|--|--|--|--|--|--|--|--|--|
| 0 | CAN_Rec_only | Enable CAN receive | able CAN receive only mode | | | | | | | | | | |
| | | 0 | CAN in transceiver mode | Active mode | | | | | | | | | |
| | | 1 CAN in receive only mode Active mod | | | | | | | | | | | |
| | | | | | | | | | | | | | |

Table 89. Control register 5: command and data bytes

| | Com | man | d by | te | | | 1 st data byte | 2 nd data byte | |
|------|--------|-------------|------|-----|------|--|---------------------------|---------------------------|-------------|
| Read | /write | | | Add | ress | | | | |
| х | х | 0 0 0 1 0 1 | | | | | 1 | Data, 8bit | Data, 8 bit |

Table 90. Control register 5, data bytes

| | 1 st data byte <15:8> | | | | | | | | | 2 nd data byte <7:0> | | | | | | | |
|----------|----------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------|---------------------------------|---------------|---------------|---------------|---|---------------|---------------|--|
| Defaults | 1 1 1 1 1 1 | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Function | Res | PWM2
Off-
DC | PWM
Freq | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | PWM1
ON-DC | | PWM1
ON-DC | PWM1
ON-DC | |
| Group | PWM2 setting | | | | | | | | | | | PWM′ | 1 setting | | | | |

Table 91. Control register 5, bits

| Bit | Name | | | | | Com | ment | | |
|-----|-------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------|
| 15 | RES | Reserve | d; must be | e set to ze | ero | | | | |
| 14 | PWM2_
Off_DC_6 | | | | | | | | |
| 13 | PWM2_
Off_DC_5 | PWM2
OFF_
DC_6 | PWM2
OFF_
DC_5 | PWM2
OFF_
DC_4 | PWM2
OFF_
DC_3 | PWM2
OFF_
DC_2 | PWM2
OFF_
DC_1 | PWM2
OFF_
DC_0 | PWM duty cycle |
| 12 | PWM2_
Off_DC_4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0%, HS OFF |
| 11 | PWM2_
Off_DC_3 | | | | | | | | |
| 10 | PWM2_
Off_DC_2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 98.5% |
| 9 | PWM2_
Off_DC_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 99.25% |
| 8 | PWM2_
Off_DC_0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100% HS ON |
| | | | | | | | | | |

Table 91. Control register 5, bits (continued)

| Bit | Name | | | | | Com | ment | | |
|-----|------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|----------------|
| 7 | PWM_
FREQ | Select P | WM frequ | ency | | | | | |
| | | 0 | 128 Hz | | | | | | |
| | | 1 | 256 Hz | | | | | | |
| | | | | | | | | | |
| 6 | PWM1_
ON_DC_6 | | | | | | | | |
| 5 | PWM1_
ON_DC_5 | PWM1
ON_
DC_6 | PWM1
ON_
DC_5 | PWM1
ON_
DC_4 | PWM1
ON_
DC_3 | PWM1
ON_
DC_2 | PWM1
ON_
DC_1 | PWM1
ON_
DC_0 | PWM duty cycle |
| 4 | PWM1_
ON_DC_4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 100%, HS ON |
| 3 | PWM1_
ON_DC_3 | | | | | | | | |
| 2 | PWM1_
ON_DC_2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.5% |
| 1 | PWM1_
ON_DC_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.75% |
| 0 | PWM1_
ON_DC_0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0% HS OFF |
| | | | | | | | | | |

Table 92. Control register 6: command and data bytes

| | | C | omma | ınd byt | e | | | 1 st data byte | 2 nd data byte |
|------|--------|---|------|---------|------|---|------------|---------------------------|---------------------------|
| Read | /Write | | | Add | ress | | | | |
| Х | Х | 0 | 0 | 0 | 1 | 0 | Data, 8bit | Data, 8 bit | |

Table 93. Control register 6, data bytes

| | | | 1 st | data k | yte <1 | 5:8> | | | | | 2 | nd data | a byte <7 | :0> | | |
|----------|--------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|-----|---------------------|---------------------|---------------------|-----------------|---------------------|---------------------|---------------------|
| Defaults | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Res | PWM4
Off_
DC_6 | PWM4
Off_
DC_5 | PWM4
Off_
DC_4 | PWM4
Off_
DC_3 | PWM4
Off_
DC_2 | PWM4
Off_
DC_1 | PWM4
Off_
DC_0 | Res | PWM3
ON_
DC_6 | PWM3
ON_
DC_5 | PWM3
ON_
DC_4 | PWM3
ON-DC_3 | PWM3
ON_
DC_2 | PWM3
ON_
DC_1 | PWM3
ON_
DC_0 |
| Group | PWM4 setting | | | | | | | | | | | PWI | M3 setting | | | |

Table 94. Control register 6, bits

| Bit | Name | | | | | Com | ment | | |
|-----|-------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|-----------------|
| 15 | RES | Reserve | d; must b | e set to z | ero | | | | |
| 14 | PWM4_
Off_DC_6 | | | | | | | | |
| 13 | PWM4_
Off_DC_5 | PWM4
OFF_
DC_6 | PWM4
OFF_
DC_5 | PWM4
OFF_
DC_4 | PWM4
OFF_
DC_3 | PWM4
OFF_
DC_2 | PWM4
OFF_
DC_1 | PWM4
OFF_
DC_0 | PWM4 duty cycle |
| 12 | PWM4_
Off_DC_4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0%, HS OFF |
| 11 | PWM4_
Off_DC_3 | | | | | | | | |
| 10 | PWM4_
Off_DC_2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 98.5% |
| 9 | PWM4_
Off_DC_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 99.25% |
| 8 | PWM4_
Off_DC_0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100% HS ON |
| | | _ | | | | | | | |
| 7 | RES | Reserve | d; must b | e set to z | ero | | | | |
| 6 | PWM3_
ON_DC_6 | | | | | | | | |
| 5 | PWM3_
ON_DC_5 | PWM3
ON_
DC_6 | PWM3
ON_
DC_5 | PWM3
ON_
DC_4 | PWM3
ON_
DC_3 | PWM3
ON_
DC_2 | PWM3
ON_
DC_1 | PWM3
ON_
DC_0 | PWM3 duty cycle |
| 4 | PWM3_
ON_DC_4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 100%, HS ON |
| 3 | PWM3_
ON_DC_3 | | | | | | | | |
| 2 | PWM3_
ON_DC_2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.5% |
| 1 | PWM3_
ON_DC_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.75% |
| 0 | PWM3_
ON_DC_0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0% HS OFF |
| | | | | | | | | | |

6.2.3 Status registers

Table 95. Overview of status register data bytes

| | | | 1 st | data b | yte <1 | 5:8> | | | | | 2 ⁿ | ^d data | byte <7 | :0> | | |
|----------|--------------------------------|--------------|-----------------|-----------------|------------------------|---------------------------|---------------------------|---------------------------|----------------------|----------------------|-------------------------|----------------------|-------------------------|----------------------------------|----------------------|------------------------|
| | | | | | | | Statu | ıs regi | ster 1 | , data | a <15:0> | | | | | |
| Function | OL
HS | OL
OUT4 | OL
OUT3 | OL
OUT2 | OL
OUT1 | UV | V ₂
fail | V ₂
short | OV | OC
HS | OC
Out4 | OC
Out3 | OC
OUT2 | OC
Out1 | OC
Rel2 | OC
Rel1 |
| Group | | • | | Diagn | osis 1 | | | • | | | | Dia | gnosis 2 | | | |
| | Status register 2, data <15:0> | | | | | | | | | | | | | | | |
| Function | WU3
state | WU2
state | WU1
state | WU3
wake | WU2
wake | WU1
Wake | Wake
CAN | Wake
LIN | Wake
Timer
int | LIN
perm.
dom. | LIN
TxD
perm dom. | LIN
perm.
rec. | CAN
RxD
perm rec. | CAN
perm.
rec. | CAN
perm.
dom. | CAN
TxD
perm dom |
| Group | | • | | Diagn | osis 3 | | | • | | | | Dia | gnosis 4 | | | |
| | | | | | | | Statu | ıs regi | ster 3 | 3, data | a <15:0> | | | | | |
| Function | TSD1 | TW | Device
state | Device
state | V ₁
fail | V ₁
restart | V ₁
restart | V ₁
restart | WD
fail | WD
fail | WD
fail | WD
fail | Forced
sleep
WD | Forced
sleep
TSD2
SHTV1 | WD
timer
state | WD
timer
state |
| Group | | | | Diagn | osis 5 | | | | | | | Dia | gnosis 6 | | | |

Table 96. Global status register

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|-------------------------------------------------------------------------------------------------------------|-------------------------------------|---------------------------------------|-----------------------------------------------------|---------------------|-------|---------------------|-----------------------------------|--------------------------|--------------|
| | Global error
flag ⁽¹⁾ | Communication
error ⁽²⁾ | NOT (chip reset or comm. error) i.e. cold start (3) | TSD2 ⁽⁴⁾ | TSD1 | V ₁ Fail | Vs fail ⁽⁵⁾
(OV/UV) | Fail safe ⁽⁶⁾ | Hex
value |
| Active high/low | High | High | Low | High | High | High | High | High | |
| Default value in
normal mode -
after correct WD
trigger or after
read & clear on
error flags | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| Power ON | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 |
| Power ON
weak battery ⁽⁷⁾ | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 |
| Communication error | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 |
| Vs over or under-voltage | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2 |
| WD failure | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 |

Table 96. Global status register (continued)

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|-------------------------------------|-------------------------------------|---------------------------------------|-----------------------------------------------------|---------------------|-------|---------------------|-----------------------------------|--------------------------|--------------|
| | Global error
flag ⁽¹⁾ | Communication
error ⁽²⁾ | NOT (chip reset or comm. error) i.e. cold start (3) | TSD2 ⁽⁴⁾ | TSD1 | V ₁ Fail | Vs fail ⁽⁵⁾
(OV/UV) | Fail safe ⁽⁶⁾ | Hex
value |
| SPI error (DI stuck) | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 |
| TSD1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 |
| TSD2 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | В9 |
| V ₁ fail | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A4 |
| Other device failure ⁽⁸⁾ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 |

1. The following status bits are reported in the global error flag:

Global status register: Bits 0 - 6 Status register 1: Bits 0 - 10 Status register 3: Bits 2, 3, 15

- 2. Invalid CLOCK COUNT.
- 3. Cleared with CLR command on SR3.
- 4. Cleared with "READ and CLEAR" on SR3 (-> TSD1).
- 5. Diagnosis bit only, Vs Fail is not a fail-safe event; cleared by read&clear. Bit is automatically cleared at (Vs > VsUV) and. (Vs < VsOV) if Vlock_out_en = 0.
- 6. Cleared with a valid WD trigger (WD fail) or by clearing the corresponding status register related to failure.
- 7. Slow Vs ramp-up (Vs undervoltage is filtered with 64 µs after Power-on reset).
- 8. The global error flag is raised due to a failure condition which is not reported in the global status register. The Failure is reported in the status registers 1 3.

Status register 1

Table 97. Status register 1: command and data bytes

| | Com | man | d byt | te | | | | 1 st data byte | 2 nd data byte |
|------|--------|-------------|-------|-----|------|--|---|---------------------------|---------------------------|
| Read | /write | | | Add | ress | | | Bit <15:8> | Bit<7:0> |
| х | х | 0 1 0 0 0 1 | | | | | 1 | Data, 8bit | Data, 8 bit |

Table 98. Status register 1, data bytes

| | | | 1 st d | ata byte | e <15:8 | > | | | | | 2 | nd data | byte < | 7:0> | | |
|----------|-------------|------------|-------------------|------------|------------|----|------------------------|-------------------------|----|----------|------------|--------------------|------------|------------|------------|------------|
| Function | OL
HS | OL
OUT4 | OL
OUT3 | OL
OUT2 | OL
OUT1 | UV | V ₂
fail | V ₂
short | OV | OC
HS | OC
Out4 | OC
Out3 | OC
OUT2 | OC
Out1 | OC
Rel2 | OC
Rel1 |
| Group | Diagnosis 1 | | | | | | | | | | | Dia | gnosis 2 | | | |

Table 99. Status register 1, bits

| Bit | Name | Comment | | Information storage |
|-----|-----------------------|-----------------------------------------------------------------------------------------------------------------|------------------------|--------------------------------------------------|
| 15 | OL_HS | | | |
| 14 | OL_OUT4 | | | |
| 13 | OL_OUT3 | Open-load event occurred since last read out | Bit is latched until a | "read and clear" access |
| 12 | OL_OUT2 | | | |
| 11 | OL_OUT1 | | | |
| 10 | UV | | | |
| | | | VLOCKOUTEN
(CR4) | Information storage |
| | | Under voltage event on V _S occurred since last read out | 0 | automatically reset when UV condition disappears |
| | | | 1 | Bit is latched until a "read and clear" access |
| | | | | |
| 9 | V ₂ _fail | V_2 fail (V_2 < 2 V for t> 2 µs)
event occurred since last
readout | Bit is latched until a | "Read and clear" access |
| 8 | V ₂ _short | V ₂ short (V ₂ < 2 V for t > 4ms
during start up) event
occurred since last readout | Bit is latched until a | "Read and clear" access |
| 7 | OV | | | |
| | | | VLOCKOUTEN
(CR4) | Information storage |
| | | Over voltage event on V _S occurred since last read out | 0 | automatically reset when OV condition disappears |
| | | | 1 | Bit is latched until a "read and clear" access |
| | | | | |
| 6 | OC_HS | | | |
| 5 | OC_OUT4 | | | |
| 4 | OC_OUT3 | Over current event account | | |
| 3 | OC_OUT2 | Over current event occurred since last read out | Bit is latched until a | "read and clear" access |
| 2 | OC_OUT1 | | | |
| 1 | OC_REL2 | | | |
| 0 | OC_REL1 | | | |

Status register 2

Table 100. Status register 2: command and data bytes

| | Com | man | d by | te | | | | 1 st data byte | 2 nd data byte | | | | |
|------|--------|-------------|------|-----|------|---------------|--|---------------------------|---------------------------|---|---|------------|-------------|
| Read | /write | | | Add | ress | | | Bit <15:8> | Bit<7:0> | | | | |
| х | Х | 0 1 0 0 1 0 | | | | x 0 1 0 0 1 0 | | | | 1 | 0 | Data, 8bit | Data, 8 bit |

Table 101. Status register 2, data bytes

| | 1 st data byte <15:8> | | | | | | 2 nd data byte <7:0> | | | | | | | | | |
|----------|----------------------------------|--------------|--------------|--|-------------|--|---------------------------------|-------------|----------------------|----------------------|-------------------------|----------------------|-------------------------|----------------------|----------------------|------------------------|
| Function | WU3
state | WU2
state | WU1
state | | WU2
wake | | Wake
CAN | Wake
LIN | Wake
Timer
int | LIN
perm.
dom. | LIN
TxD
perm dom. | LIN
perm.
rec. | CAN
RxD
perm rec. | CAN
perm.
rec. | CAN
perm.
dom. | CAN
TxD
perm dom |
| Group | Diagnosis 3 | | | | | | | | Dia | gnosis 4 | | | | | | |

Table 102. Status register 2, bits

| Bit | Name | Comment | Information storage | | |
|-----|------------------|--------------------------------------------------------------------|--------------------------------------------------|--|--|
| 15 | WU3_state | | | | |
| 14 | WU2_state | State of WUx input; | "Live bits" not clearable | | |
| 13 | WU1_state | | | | |
| 12 | WU3_wake | | | | |
| 11 | WU2_wake | | | | |
| 10 | WU1_wake | Shows wake up source ('1' = wake-up) | | | |
| 9 | WAKE_CAN | Shows wake up source (r = wake-up) | | | |
| 8 | WAKE_LIN | | | | |
| 7 | Wake_TIMER_int | | | | |
| 6 | LIN_perm_DOM | LIN bus is dominant for t > 12 ms | | | |
| 5 | LIN_TxD_perm_DOM | TxDL pin is dominant for t > 12 ms;
Transmitter is disabled | Bits are latched until a "Read and clear" access | | |
| 4 | LIN_perm_REC | LIN bus does not follow TxDL within 40 µs; Transmitter is disabled | | | |
| 3 | CAN_RxD_perm_rec | RxDC has not followed TxDC for 4 times;
Transmitter is disabled | | | |
| 2 | CAN_perm_REC | CAN has not followed TxDC for 4 times;
Transmitter is disabled | | | |
| 1 | CAN_perm_DOM | CAN bus is dominant for t > 700 µs | | | |
| 0 | CAN_TxD_perm_DOM | TxDC pin is dominant for t > 700 µs;
Transmitter is disabled | | | |

Status register 3

Table 103. Status register 3: command and data bytes

| | Com | man | d by | te | | | 1 st data byte | 2 nd data byte | |
|------|----------------|-----|------|----|---|---|---------------------------|---------------------------|-------------|
| Read | /write Address | | | | | | | Bit <15:8> | Bit<7:0> |
| х | х | 0 | 1 | 0 | 0 | 1 | 1 | Data, 8bit | Data, 8 bit |

Table 104. Status register 3, data bytes

| | 1 st data byte <15:8> | | | | | | | 2 nd data byte <7:0> | | | | | | |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|-----------------------------|--------------|---------------------------------|--------------|--------------|-----------------------|----------------------------------|------------------------|------------------------|
| Function | TSD1 TW Device state_2 Device state_1 V ₁ V ₁ V ₁ V ₂ V ₃ V ₄ V ₄ V ₄ V ₄ V ₄ V ₄ V ₅ V ₄ V ₄ V ₄ V ₅ V ₄ V ₄ V ₄ V ₅ V ₄ V ₄ V ₅ V ₄ V ₅ V ₆ V ₇ V ₇ V ₇ V ₈ V ₈ | | | | | V ₁
restart_0 | WD
fail_3 | WD
fail_2 | WD
fail_1 | WD
fail_0 | Forced
sleep
WD | Forced
sleep
TSD2
SHTV1 | WD
timer
state_1 | WD
timer
state_0 |
| Group | Diagnosis 5 | | | | | | | | | Di | agnosis 6 | 6 | | |

Table 105. Status register 3, bits

| Bit | Name | | Comment | | Information storage | | | |
|-----|---------------------------|-----------------------------------------|---------------------------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--|--|--|
| 15 | TSD1 | Thermal warning / sk | Bit is latched until a | | | | | |
| 14 | TW | Thermal warning / Si | Thermal warning / shutdown1 occurred since last readout | | | | | |
| 13 | | State from which the | | | | | | |
| 12 | | Device state 2 Device state 1 which the | | State from
which the
device woke
up | Bit is latched until a
"read and clear access"
after a "read and clear
access", the device
state is updated | | | |
| | Device_state | 0 | 0 | Active | after a wake up, device | | | |
| | | 0 | 1 | V ₁ standby | state is
01: V ₁ standby | | | |
| | | 1 | 0 | V _{BAT} standby | or v ₁ standby | | | |
| | | 1 | 1 | Flash | 10: V _{BAT} standby | | | |
| | | | | _ | | | | |
| 11 | V ₁ _fail | V_1 fail ($V_1 < 2$ V for t | > 2 µs) event occurre | d since last read out | Bit is latched until a "read and clear access" | | | |
| 10 | V ₁ _restart_2 | Never have a f TODO and | | | | | | |
| 9 | V ₁ _restart_1 | Number of TSD2 ever
regulator | is cleared automatically if no additional TSD2 | | | | | |
| 8 | V ₁ _restart_0 | (7 TSD2 events force | event occurs within 1 min. | | | | | |
| 7 | WD_fail_3 | | | | | | | |
| 6 | WD_fail_2 | Number of missing w | Bits are not clearable; is cleared with a proper | | | | | |
| 5 | WD_fail_1 | (15 missing watchdo standby) | Watchdog trigger | | | | | |
| 4 | WD_fail_0 | | | | | | | |

Table 105. Status register 3, bits (continued)

| Bit | Name | | Information storage | | |
|-----|-----------------------------------------|-----------------------------------------------------------------------------------|------------------------------------------------|--------------|------------------------|
| 3 | Forced_sleep_WD | Device was forced to watchdog errors | | | |
| 2 | Forced_sleep_TSD
2_SHTV ₁ | Device was forced to
shutdown events
or
a short on V ₁ during | Bits are latched until a read and clear access | | |
| 1 | WD_timer_state_1 | Status of watchdog of | counter of selected wat | chdog timing | |
| 0 | WD_timer_state_0 | | | | |
| | | WD_timer_state_1 | WD_timer_state_0 | Counter | |
| | | 0 | 0 | 0 – 33% | Bits are not clearable |
| | | 0 | 1 | 33 – 66% | |
| | | 1 | 1 | 66 – 100% | |
| | | | | | |

7 Package and packing information

7.1 ECOPACK[®]

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

7.2 PowerSSO-36 package information

Figure 41. PowerSSO-36 package dimensions

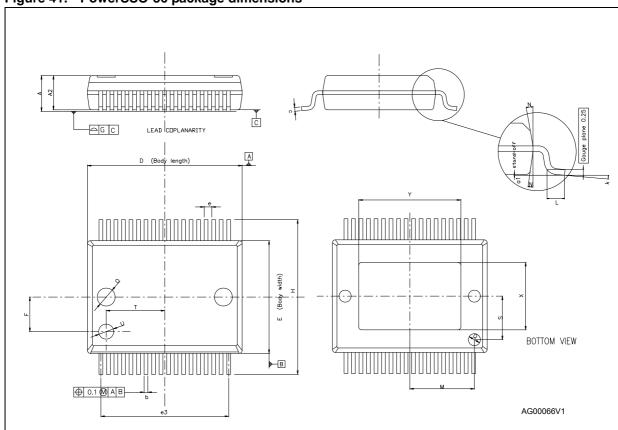


Table 106. PowerSSO-36 mechanical data

| Oh. a.l. | Millimeters | | | | | | | | |
|----------|-------------|------|--------|--|--|--|--|--|--|
| Symbol | Min. | Тур. | Max. | | | | | | |
| А | - | - | 2.45 | | | | | | |
| A2 | 2.15 | - | 2.35 | | | | | | |
| a1 | 0 | - | 0.1 | | | | | | |
| b | 0.18 | - | 0.36 | | | | | | |
| С | 0.23 | - | 0.32 | | | | | | |
| D | 10.10 | - | 10.50 | | | | | | |
| E | 7.4 | - | 7.6 | | | | | | |
| е | - | 0.5 | - | | | | | | |
| e3 | - | 8.5 | - | | | | | | |
| F | - | 2.3 | - | | | | | | |
| G | - | - | 0.1 | | | | | | |
| G1 | - | - | 0.06 | | | | | | |
| Н | 10.1 | - | 10.5 | | | | | | |
| h | - | - | 0.4 | | | | | | |
| k | 0° | - | 8° | | | | | | |
| L | 0.55 | - | 0.85 | | | | | | |
| M | - | 4.3 | - | | | | | | |
| N | - | - | 10 deg | | | | | | |
| 0 | - | 1.2 | - | | | | | | |
| Q | - | 0.8 | - | | | | | | |
| S | - | 2.9 | - | | | | | | |
| Т | - | 3.65 | - | | | | | | |
| U | - | 1.0 | - | | | | | | |
| Х | 4.1 | - | 4.7 | | | | | | |
| Y | 6.5 | - | 7.1 | | | | | | |

L99PM62GXP Revision history

8 Revision history

Table 107. Document revision history

| Date | Revision | Change |
|---------------|----------|------------------------------------------------------------------------------------------------------------------------|
| 24-Jan-2011 | 1 | Initial release. |
| 23-Feb-2011 | 2 | Table 11: Temperature warning and thermal shutdown: - T _{SD2 OFF} : updated minimum and typical values |
| 01-Jun-2011 3 | | Updated following figures: - Figure 3: Voltage source with external PNP - Figure 5: Voltage source with external NPN |
| 19-Sep-2013 | 4 | Updated disclaimer. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries. Information in this document supersedes and replaces all information previously supplied. The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

102/102 Doc ID 17639 Rev 4





Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А