

NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PARTS
ZL8101 and ZL6105

ZL2004-01

Adaptive Digital DC/DC Controller with Current Sharing

FN6847
Rev 2.00
May 23, 2011

The ZL2004-01 is specialized version of the ZL2004 DC/DC controller that has been optimized for high output accuracy within a given set of operating conditions. The ZL2004-01 is otherwise identical to the ZL2004 in features and functionality. The ZL2004-01 has been optimized for use with the ZL1505 MOSFET driver and discrete MOSFETs.

The ZL2004-01 integrates a proprietary Digital-DC communication bus for current sharing and inter device communication. Adaptive algorithms improve light load efficiency. All operating features can be configured by simple pin-strap selection, resistor selection or through the on-board serial port. The PMBus™-compliant ZL2004-01 uses the SMBus™ serial interface for communication with other Digital-DC products or a host controller.

Related Literature

- See [FN6846](#), ZL2004 “Adaptive Digital DC-DC Controller with Current Sharing”

Features

- Power Conversion
- Efficient synchronous buck controller
- $\pm 0.2\%$ VOUT set-point accuracy
- 8.0V to 10.0V input range
- 0.9V to 1.1V output range
- Adaptive performance optimization algorithms
- Fast load transient response
- Active current sharing
- DCR current sensing with digitally adjustable current sense range
- RoHS compliant (5mmx5mm) QFN package
- Power Management
- Digital soft-start/stop
- Precision delay and ramp-up
- Power-good/enable
- Voltage tracking, sequencing and margining
- Voltage/current/temperature monitoring
- SMBus communication (PMBus compliant)
- Output voltage and current protection
- Internal non-volatile memory (NVM)

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

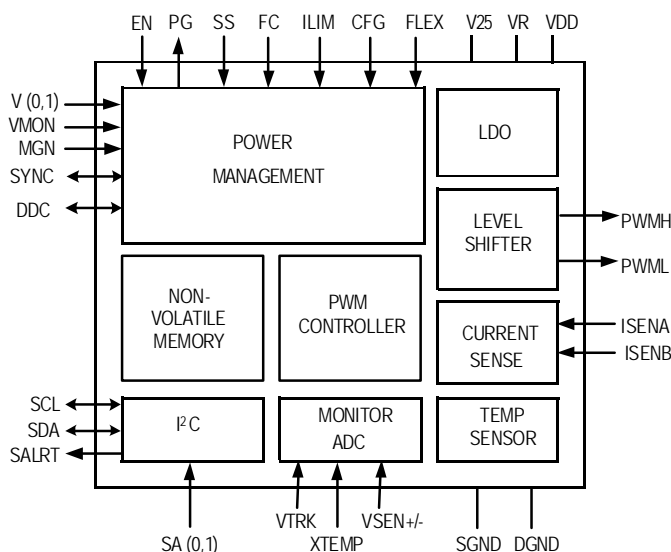


FIGURE 1. BLOCK DIAGRAM

Ordering Information

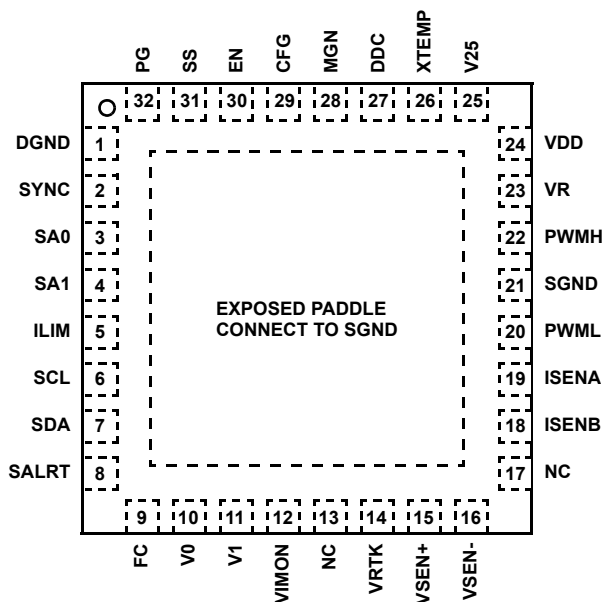
| PART NUMBER (Notes 1, 4) | PART MARKING | TEMP RANGE (°C) | SHIPPING CONTAINER | PACKAGE Tape & Reel (Pb-free) | PKG. DWG. # |
|-----------------------------|--------------|--------------------|--------------------|-------------------------------------|-------------|
| ZL2004ALNN-01 (Note 2) | 2004-01 | 0 to +65 | 490 pieces | 32 Ld QFN | L32.5x5D |
| ZL2004ALNNT-01 (Note 2) | 2004-01 | 0 to +65 | 100 pieces | 32 Ld QFN | L32.5x5D |
| ZL2004ALNNT1-01 (Note 2) | 2004-01 | 0 to +65 | 1000 pieces | 32 Ld QFN | L32.5x5D |
| ZL2004ALNF-01 (Note 3) | 2004-01 | 0 to +65 | 490 pieces | 32 Ld QFN | L32.5x5G |
| ZL2004ALNFT-01 (Note 3) | 2004-01 | 0 to +65 | 100 pieces | 32 Ld QFN | L32.5x5G |
| ZL2004ALNFT1-01 (Note 3) | 2004-01 | 0 to +65 | 1000 pieces | 32 Ld QFN | L32.5x5G |

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for [ZL2004-01](#). For more information on MSL please see techbrief [TB363](#).

Pin Configuration

ZL2004-01
(32 LD QFN)
TOP VIEW



Pin Descriptions

| PIN | SYMBOL | TYPE (Note 5) | DESCRIPTION |
|--------|-----------------|--------------------|--|
| 1 | DGND | PWR | Digital ground. Connect to low impedance ground plane. |
| 2 | SYNC | I/O, M (Note 6) | Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock. |
| 3 | SA0 | I, M | Serial address select pins. Used to assign unique address for each individual device or to enable certain management features. |
| 4 | SA1 | | |
| 5 | ILIM | I, M | Current limit select. Sets the overcurrent threshold voltage for ISENA, ISENB. |
| 6 | SCL | I/O | Serial clock. Connect to external host and/or to other ZL devices. |
| 7 | SDA | I/O | Serial data. Connect to external host and/or to other ZL devices. |
| 8 | SALRT | O | Serial alert. Connect to external host if desired. |
| 9 | FC | I | Loop compensation selection pin. |
| 10 | V0 | I, M | Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max. |
| 11 | V1 | | |
| 12 | VMON | I, M | External voltage monitoring (Can be used for external driver bias monitoring for Power-good). |
| 13, 17 | NC | | No Connect. |
| 14 | VTRK | I | Tracking sense input. Used to track an external voltage source. |
| 15 | VSEN+ | I | Differential Output voltage sense feedback. Connect to positive output regulation point. |
| 16 | VSEN- | I | Differential Output voltage sense feedback. Connect to negative output regulation point. |
| 18 | ISENB | I | Differential voltage input for current sensing. |
| 19 | ISENA | I | Differential voltage input for current sensing. High voltage (DCR). |
| 20 | PWML | O | PWM Gate low signal. |
| 21 | SGND | PWR | Connect to low impedance ground plane. Internal connection to SGND. |
| 22 | PWMH | O | PWM Gate High signal. |
| 23 | VR | PWR | Internal 5V reference used to power internal drivers. |
| 24 | VDD (Note 7) | PWR | Supply voltage. |
| 25 | V25 | PWR | Internal 2.5V reference used to power internal circuitry. |
| 26 | XTEMP | I | External temperature sensor input. Connect to external 2N3904 (Base Emitter junction). |
| 27 | DDC | I | Single wire DDC bus (Current sharing, interdevice communication). |
| 28 | MGN | I | V_{OUT} margin control. |
| 29 | CFG | M | Configuration pin. Used to control the switching phase offset, sequencing and other management features. |
| 30 | EN | I | Enable. Active signal enables PWM switching. |
| 31 | SS | I, M | Soft-start delay and ramp select. Sets the delay from when EN is asserted until the output voltage starts to ramp and the ramp time. |
| 32 | PG | O | Power-good output. |
| EPAD | SGND | PWR | Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND. |

NOTES:

5. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins.
6. The SYNC pin can be used as a logic pin, a clock input or a clock output.
7. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

Absolute Maximum Ratings (Note 8)

| | |
|---|----------------|
| DC Supply Voltage (VDD) | -0.3V to 17V |
| Logic I/O Voltage | |
| CFG, DDC, EN, FC, FLEX, ILIM, MGN, PG, SA (0,1) | |
| SALRT, SCL, SDA, SS, SYNC, VMON, V (0,1) | -0.3V to 6.5V |
| Analog Input Voltages | |
| VSEN+, VSEN-, VTRK, XTEMP | -0.3V to 6.5V |
| ISENA, ISENB | -1.5V to 6.5V |
| MOSFET Drive Reference (VR) | -0.3V to 6.5V |
| Logic reference (V25) | -0.3V to 3V |
| Ground Voltage Differential (VDGND- VSGND) | |
| DGND, SGND | -0.3V to +0.3V |

Thermal Information

| | | |
|---------------------------------|---|---|
| Thermal Resistance (Typical) | θ_{JA} ($^{\circ}\text{C}/\text{W}$) | θ_{JC} ($^{\circ}\text{C}/\text{W}$) |
| 32 Ld QFN Package (Notes 9, 10) | 35 | 5 |
| Junction Temperature | -55 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$ | |
| Storage Temperature Range | -55 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$ | |
| Pb-Free Reflow Profile | see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp | |

Recommended Operating Conditions

| | |
|-----------------------------------|--|
| Input Supply Voltage Range, (VDD) | 8V to 10V |
| Output Voltage Range (VOUT) | 0.9V to 1.1V, 1.0V (Typ) |
| Operating Frequency (FSW) | 400kHz Typ |
| Operating Ambient Temperature | 0 $^{\circ}\text{C}$ to +65 $^{\circ}\text{C}$ |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- All voltages are measured with respect to SGND.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications $V_{DD} = 8.6\text{V}$, $V_{OUT} = 1.0\text{V}$, $T_A = 0^{\circ}\text{C}$ to +65 $^{\circ}\text{C}$ unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$. The following specifications describe the ZL2004-01 electrical specifications that differ from the ZL2004. Please refer to the ZL2004 data sheet for the full operating specification limits for the remaining functions not described herein. **Boldface limits apply over the operating temperature range, 0 $^{\circ}\text{C}$ to +65 $^{\circ}\text{C}$.**

| PARAMETER | CONDITIONS | MIN (Note 11) | TYP | MAX (Note 11) | UNIT |
|--|---|------------------|-----|------------------|------|
| INPUT AND SUPPLY CHARACTERISTICS | | | | | |
| I _{DD} Supply Current at F _{SW} = 400kHz | GH no load, GL no load, MISC_CONFIG[7] = 1 | - | 16 | 30 | mA |
| I _{DDS} Shutdown Current | EN = 0V No I ² C/SMBus activity | - | 2 | 5 | mA |
| VR Reference Output Voltage | V _{DD} > 6V, I _{VR} < 50mA | 4.5 | 5.2 | 5.7 | V |
| V25 Reference Output Voltage | V _R > 3V, I _{V25} < 50mA | 2.25 | 2.5 | 2.75 | V |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Adjustment Range | V _{IN} > V _{OUT} | 0.9 | - | 1.1 | V |
| Output Voltage Setpoint Accuracy (Note 12) | V _{IN} = 8.6V, V _{OUT} = 1V T _A = 0 $^{\circ}\text{C}$ to +65 $^{\circ}\text{C}$, I _{LOAD} = 0A to 40A | -0.2 | - | 0.2 | % |
| PMBus READ_VOUT Accuracy | | -1.0 | - | 1.0 | % |
| OSCILLATOR AND SWITCHING CHARACTERISTICS | | | | | |
| Switching Frequency (Note 13) | SYNC pin floating or NVM configured for 400kHz | - | 400 | - | kHz |
| Switching Frequency Set-point Accuracy | | -5 | - | 5 | % |
| FAULT PROTECTION CHARACTERISTICS | | | | | |
| UVLO Threshold Range | Configurable via I ² C/SMBus | 2.85 | - | 16 | V |

NOTES:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- V_{OUT} set-point measured at the termination of the VSEN+ and VSEN- sense points.
- The ZL2004-01 has been optimized for operation at 400kHz only. Please consult the factory for requirements at other operating frequencies.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---------|----------|---|
| 5/11/11 | FN6847.2 | <p>On page 1: Added "Related Literature"</p> <p>On page 2: Added following parts to "Ordering Information": ZL2004ALNN-01 ZL2004ALNF-01 ZL2004ALNFT-01 ZL2004ALNFT1-01</p> <p>Added lead finish Note 3 for ALNF parts.</p> <p>On page 4: Updated note in Min Max column of "Electrical Specifications" table from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."</p> <p>On page 8: Added "Package Outline Drawing" L32.5x5G for ALNF parts.</p> |
| 4/9/10 | FN6847.1 | On page 4, changed max value from 5.5 to 5.7 for "VR Reference Output Voltage". |
| 3/23/10 | | <p>Converted to New Intersil Template. Added spec to existing parameter on the device in Electrical Specifications Table "Output Characteristics": PMBus READ_VOUT Accuracy -1.0 (MIN), 1.0 (MAX) %. Changed Temp Range in ordering information from "-40°C to +85°C" to "0°C to +65°C" matching information in Thermal Information. Added over-temp note and reference Electrical spec table Min and Max columns. Added ordering information table, Pin Configuration and Pin Description Table, POD, Revision History and Products Information.</p> <p>Updated POD L32.5x5D to latest released version. Change to POD is as follows: Updated POD to new standards by adding land pattern and moving dimensions from table onto drawing.</p> |
| 2/19/09 | FN6847.0 | Assigned file number FN6847 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to datasheet content. |

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ZL2004-01](http://www.intersil.com/products)

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at <http://rel.intersil.com/reports/search.php>

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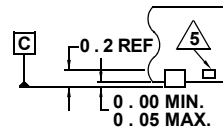
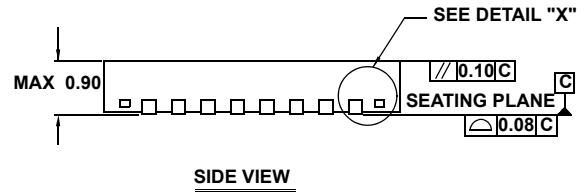
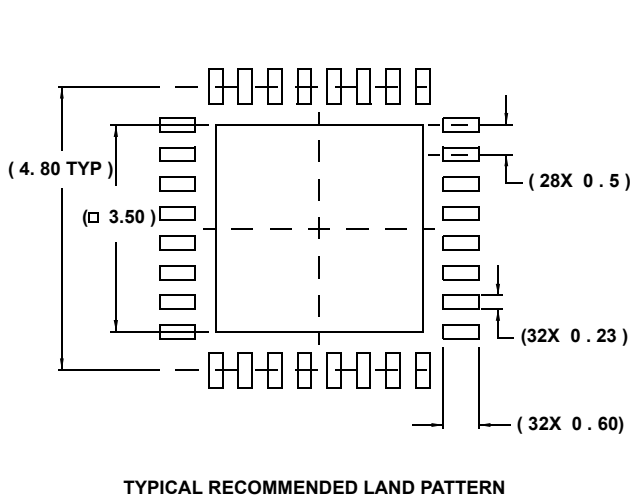
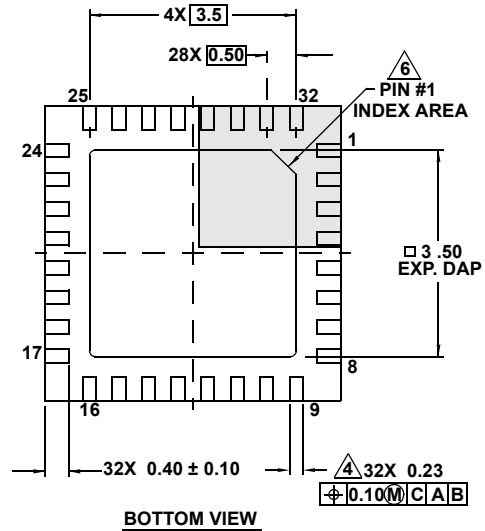
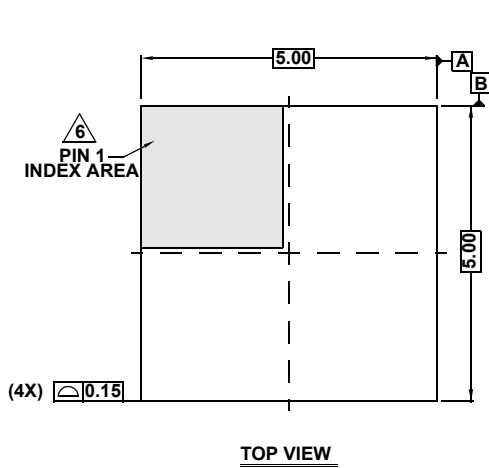
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Package Outline Drawing

L32.5x5D

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 3/10



NOTES:

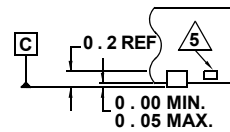
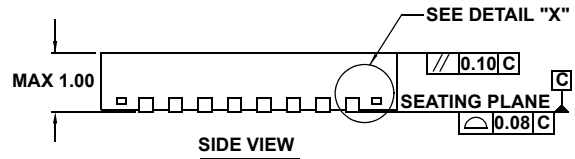
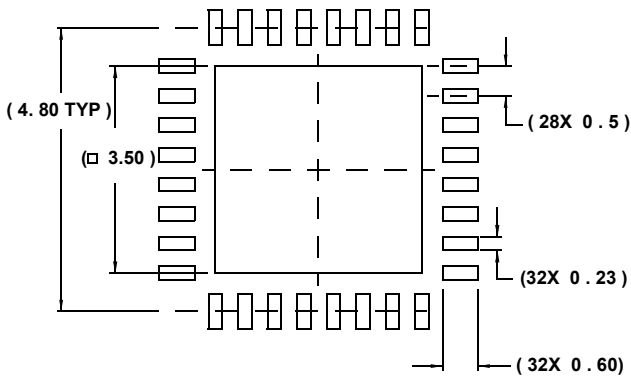
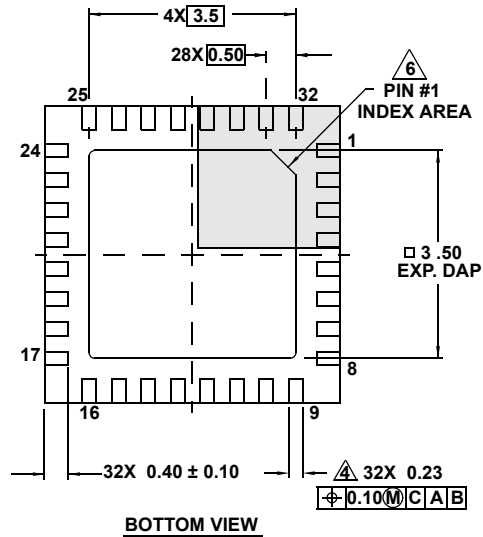
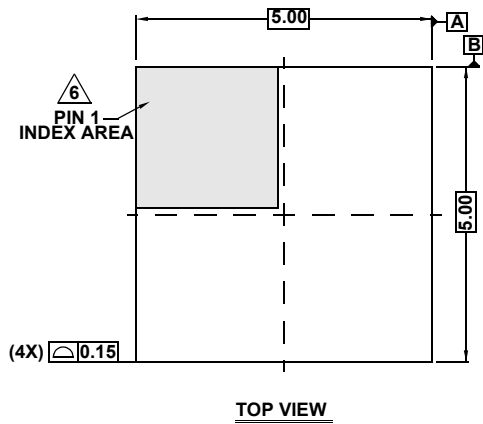
1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
- ④ Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- ⑤ Tiebar shown (if present) is a non-functional feature.
- ⑥ The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

L32.5x5G

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 3/10



NOTES:

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Dimensions in () for Reference Only.
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