

## High Speed Quad MOSFET Driver

### Features

- ▶ 6ns rise and fall time
- ▶ 2 A peak output source/sink current
- ▶ 1.2V to 5V input CMOS compatible
- ▶ 5V to 12V total supply voltage
- ▶ Smart Logic threshold
- ▶ Low jitter design
- ▶ Quad matched channels
- ▶ Drives two P- and two N-channel MOSFETs
- ▶ Outputs can swing below ground
- ▶ Low inductance quad flat no-lead package
- ▶ High-performance thermally-enhanced

### Applications

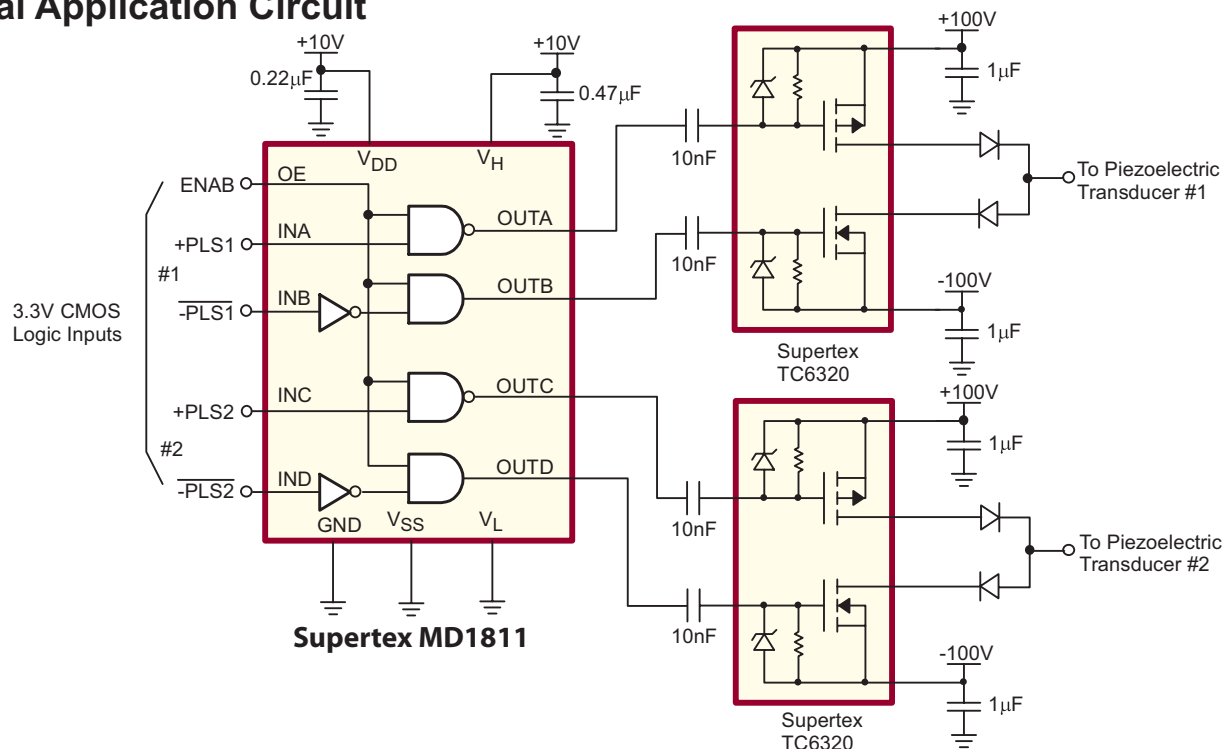
- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Nondestructive evaluation
- ▶ PIN diode driver
- ▶ Clock driver/buffer
- ▶ High speed level translator

### General Description

The Supertex MD1811 is a high speed, quad MOSFET driver designed to drive high voltage P and N-channel MOSFETs for medical ultrasound applications and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1811 can operate from a 1.2 to 5.0 volt logic interface with an optimum operating input signal range of 1.8 to 3.3 volts. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic 0 and logic 1 levels. The input logic levels may be ground referenced, even though the driver is putting out bipolar signals. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1811 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0 and 1.8 volts, the control logic may be powered by +5 and -5 volts, and the output L and H levels may be varied anywhere over the range of -5 to +5 volts. The output stage is capable of peak currents of up to  $\pm 2$  amps, depending on the supply voltages used and load capacitance present. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Secondly, when OE is low, the outputs are disabled, with the A & C output high and the B & D output low. This assists in properly pre-charging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair.

### Typical Application Circuit



## Ordering Information

DEVICE	Package Options
	16-Lead QFN 4x4mm body, 1.0mm height (max), 0.65mm pitch
MD1811	MD1811K6-G
$\theta_{JA}$	45°C/W (1oz. 4-layer 3x4inch PCB)

-G indicates package is RoHS compliant ("Green")

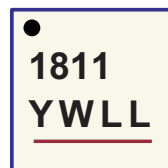


## Absolute Maximum Ratings

Parameter	Value
$V_{DD}-V_{SS}$ , Logic supply voltage	-0.5V to +13.5V
$V_H$ , Output high supply voltage	$V_L$ -0.5V to $V_{DD}$ +0.5V
$V_L$ , Output low supply voltage	$V_{SS}$ -0.5V to $V_H$ +0.5V
$V_{SS}$ , Low side supply voltage	-7V to +0.5V
Logic Input levels	$V_{SS}$ -0.5V to $V_{SS}$ +7V
Maximum junction temperature	+125°C
Storage temperature	-65°C to 150°C
Soldering temperature	235°C
Package power dissipation	2.2W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Product Marking



Y = Last Digit of Year Sealed  
W = Code for Week Sealed  
L = Lot Number  
— = "Green" Packaging

### 16-Lead QFN Package

## DC Electrical Characteristics ( $V_H = V_{DD} = 12V$ , $V_L = V_{SS} = GND = 0V$ , $V_{OE} = 3.3V$ , $T_J = 25^\circ C$ )

Sym.	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{DD}-V_{SS}$	Logic supply voltage	4.5	-	13	V	--
$V_{SS}$	Low side supply voltage	-5.5	-	0	V	--
$V_H$	Output high supply voltage	$V_{SS}+2$	-	$V_{DD}$	V	--
$V_L$	Output low supply voltage	$V_{SS}$	-	$V_{DD}-2$	V	--
$I_{DDQ}$	$V_{DD}$ quiescent current	-	0.8		mA	No input transitions, OE = 1
$I_{HQ}$	$V_H$ quiescent current	-		10	$\mu A$	
$I_{DD}$	$V_{DD}$ average current	-	8.0	-	mA	One channel on at 5.0Mhz, No load
$I_H$	$V_H$ average current	-	26	-	mA	
$V_{IH}$	Input logic voltage high	$V_{OE}-0.3$	-	5.0	V	For logic inputs INA, INB, INC, and IND
$V_{IL}$	Input logic voltage low	0	-	0.3	V	
$I_{IH}$	Input logic current high	-	-	1.0	$\mu A$	
$I_{IL}$	Input logic current low	-	-	1.0	$\mu A$	
$V_{IH}$	OE Input logic voltage high	1.2	-	5	V	For logic input OE
$V_{IL}$	OE Input logic voltage low	0	-	0.3	V	
$R_{IN}$	Input logic impedance to GND	12	20	30	K $\Omega$	
$C_{IN}$	Logic input capacitance	-	5.0	10	pF	--

## Outputs $(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{OE} = 3.3V, T_J = 25^\circ C)$

Sym.	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_{SINK}$	Output sink resistance	-	-	12.5	$\Omega$	$I_{SINK} = 50mA$
$R_{SOURCE}$	Output source resistance	-	-	12.5	$\Omega$	$I_{SOURCE} = 50mA$
$I_{SINK}$	Peak output sink current	-	2.0	-	A	--
$I_{SOURCE}$	Peak output source current	-	2.0	-	A	--

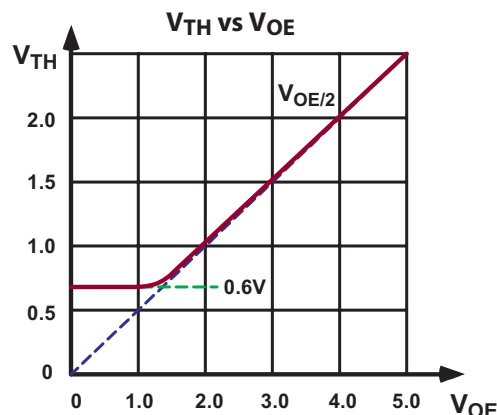
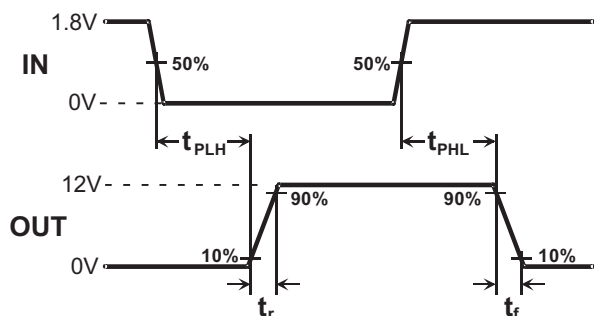
## AC Electrical Characteristics $(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{OE} = 3.3V, T_J = 25^\circ C)$

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{irf}$	Input or OE rise & fall time	-	-	10	ns	Logic input edge speed requirement
$t_{PLH}$	Propagation delay when output is from low to high	-	7.0	-	ns	$C_{LOAD} = 1000pF$ , see timing diagram Input signal rise/fall time 2ns
$t_{PHL}$	Propagation delay when output is from high to low	-	7.0	-	ns	
$t_{POE}$	Propagation delay OE to output	-	9.0	-	ns	
$t_r$	Output rise time	-	6.0	-	ns	
$t_f$	Output fall time	-	6.0	-	ns	
$ t_r - t_f $	Rise and fall time matching	-	1.0	-	ns	
$ t_{PLH} - t_{PHL} $	Propagation low to high and high to low matching	-	1.0	-	ns	for each channel
$\Delta t_{dm}$	Propagation delay matching	-	$\pm 2.0$	-	ns	Device to device delay match

## Logic Truth Table

Logic Inputs			Output	
OE	INA	INB	OUTA	OUTB
H	L	L	$V_H$	$V_H$
H	L	H	$V_H$	$V_L$
H	H	L	$V_L$	$V_H$
H	H	H	$V_L$	$V_L$
L	X	X	$V_H$	$V_L$
OE	INC	IND	OUTC	OUTD
H	L	L	$V_H$	$V_H$
H	L	H	$V_H$	$V_L$
H	H	L	$V_L$	$V_H$
H	H	H	$V_L$	$V_L$
L	X	X	$V_H$	$V_L$

## Timing Diagram and $V_{TH} / V_{OE}$ Curve



## Application Information

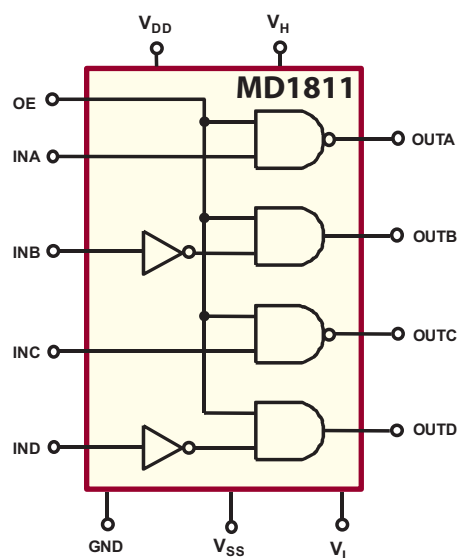
For proper operation of the MD1811, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND, and OE pins should be connected to a logic source with a swing of GND to  $V_{LL}$ , where  $V_{LL}$  is 1.2 to 5.0 volts. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1811 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the  $V_{SS}$  and  $V_L$  pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection  $V_{DD}$  should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

The voltages of  $V_H$  and  $V_L$  decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor

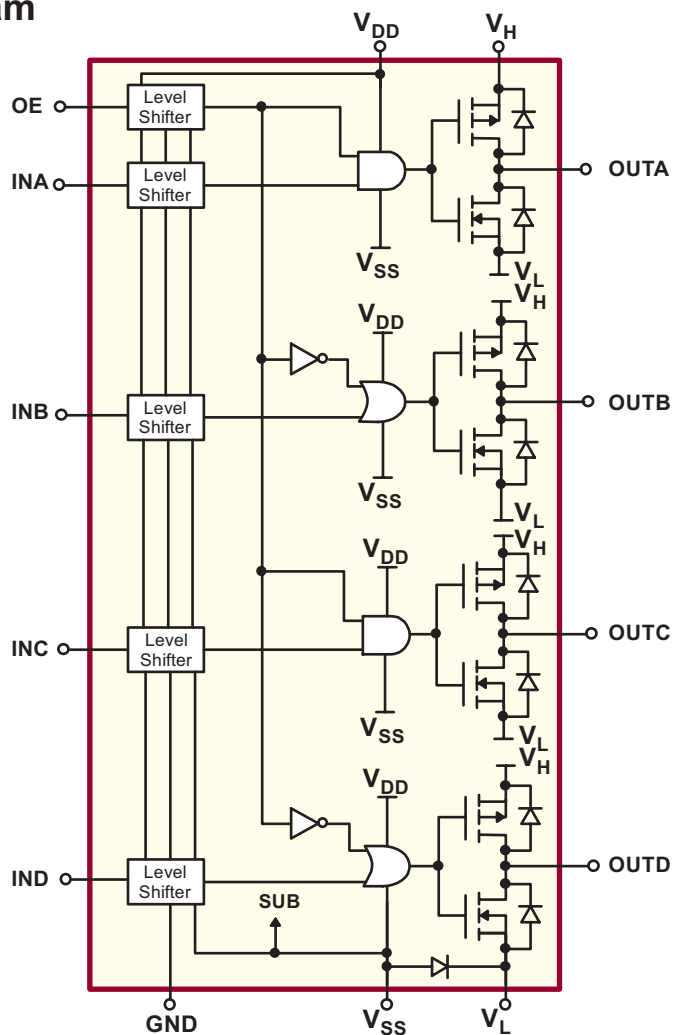
of up to 1.0 $\mu$ F may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will of course reduce the output voltage slew rate at the terminals of a capacitive load.

Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

## Simplified Block Diagram



## Detailed Block Diagram

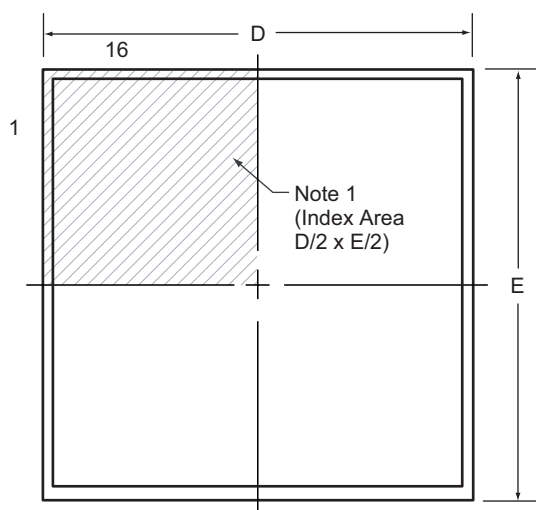


## Pin Description

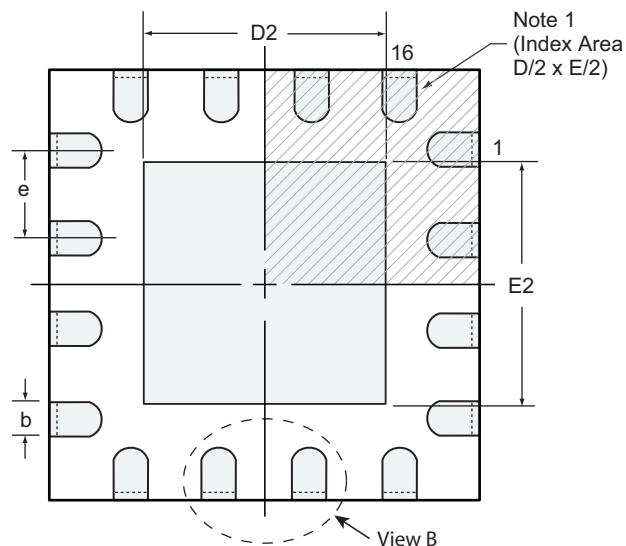
Pin #	Function	Description
1	INB	Logic input. Input logic high will cause the output to swing to $V_H$ . Input logic low will cause the output to swing to $V_L$ . Keep all logic inputs low until IC powered up.
5	INC	
6	IND	
15	INA	
2	$V_L$	Supply voltage for N-channel output stage.
4		
3	GND	Logic input ground reference.
7	$V_{SS}$	Low side supply voltage. $V_{SS}$ is also connected to the IC substrate. It is required to connect to the most negative potential of voltage supplies and powered-up first.
8	OUTD	Output driver. Swings from $V_H$ to $V_L$ . Intended to drive the gate of an external N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTD will swing to $V_L$ turning off the external N-channel MOSFET.
9	OUTC	Output driver. Swings from $V_H$ to $V_L$ . Intended to drive the gate of an external P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTC will swing to $V_H$ turning off the external P-channel MOSFET.
12	OUTB	Output driver. Swings from $V_H$ to $V_L$ . Intended to drive the gate of an external N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTB will swing to $V_L$ turning off the external N-channel MOSFET.
13	OUTA	Output driver. Swings from $V_H$ to $V_L$ . Intended to drive the gate of an external P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTA will swing to $V_H$ turning off the external P-channel MOSFET.
10	$V_H$	Supply voltage for P-channel output stage.
11		
14	$V_{DD}$	High side supply voltage.
16	OE	Output enable logic input. When OE is high, $(V_{OE}+V_{GND})/2$ sets the threshold transition between logic level high and low. When OE is low, all outputs are at high impedance. Keep OE low until IC powered up.
Substrate		The IC substrate is internally connected to the thermal pad. Thermal Pad and $V_{SS}$ must be connected externally.

# 16-Lead QFN Package Outline (K6)

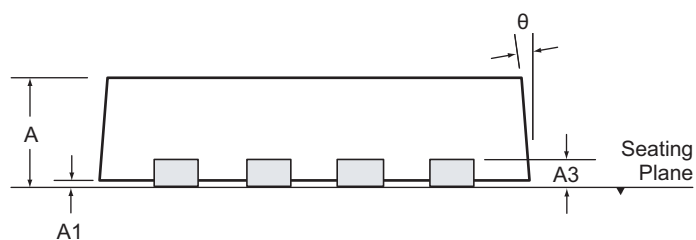
4x4mm body, 1.00mm height (max), 0.65mm pitch



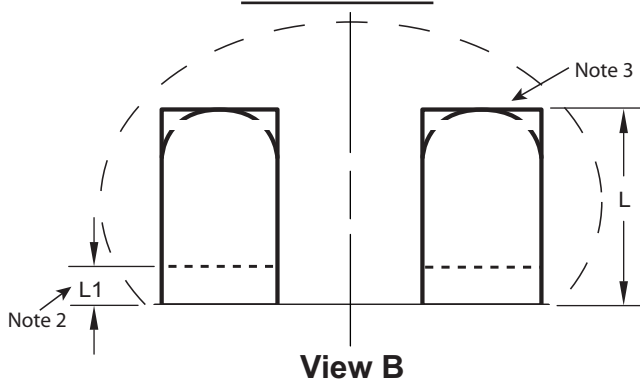
**Top View**



**Bottom View**



**Side View**



**View B**

## Notes:

- Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
- Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
- The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85	2.40	3.85	2.40	0.65 BSC	0.30	-	0°
	NOM	0.90	0.02		0.30	4.00	-	4.00	-		0.40	-	-
	MAX	1.00	0.05		0.35	4.15	2.80	4.15	2.80		0.50	0.15	14°

JEDEC Registration MO-220, Variation VGGC-3, Issue K, June 2006.

Drawings not to scale.

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