

74HC4060; 74HCT4060

14-stage binary ripple counter with oscillator

Rev. 5 — 8 May 2020

Product data sheet

1. General description

The 74HC4060; 74HCT4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, RTC and CTC), ten buffered parallel outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (RTC and CTC) floating. The counter advances on the HIGH-to-LOW transition of RS. A HIGH level on MR clears all counter stages and forces all outputs LOW, independent of the other input conditions. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- All active components on chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7 A
- Input levels:
 - For 74HC4060: CMOS level
 - For 74HCT4060: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4060D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4060D				
74HC4060DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4060PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4060BQ	-40 °C to +125 °C	DHWQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4060BQ				

5. Functional diagram

001aai467

(a) (b)

001aai468

001aai113

Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Functional diagram

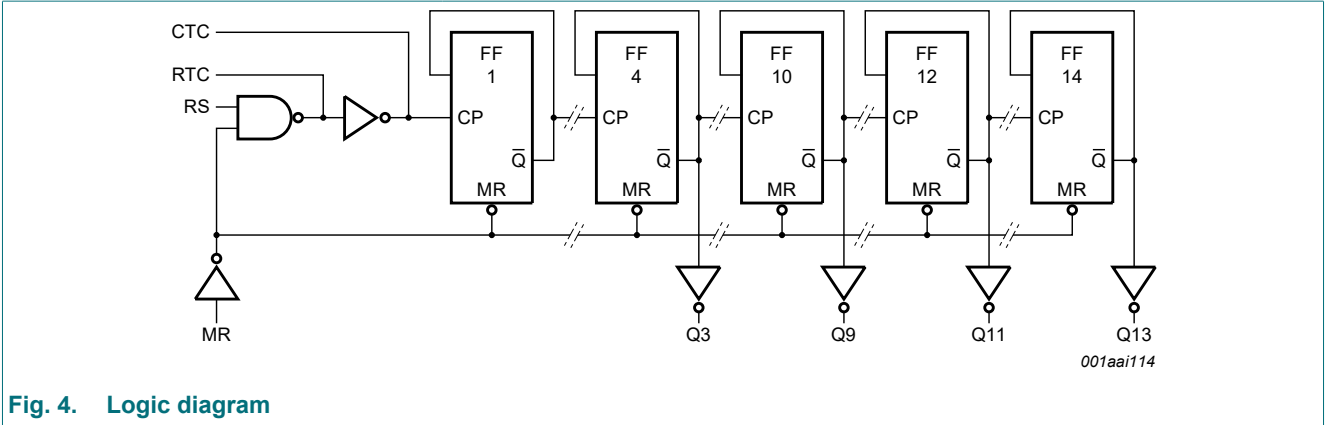


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning

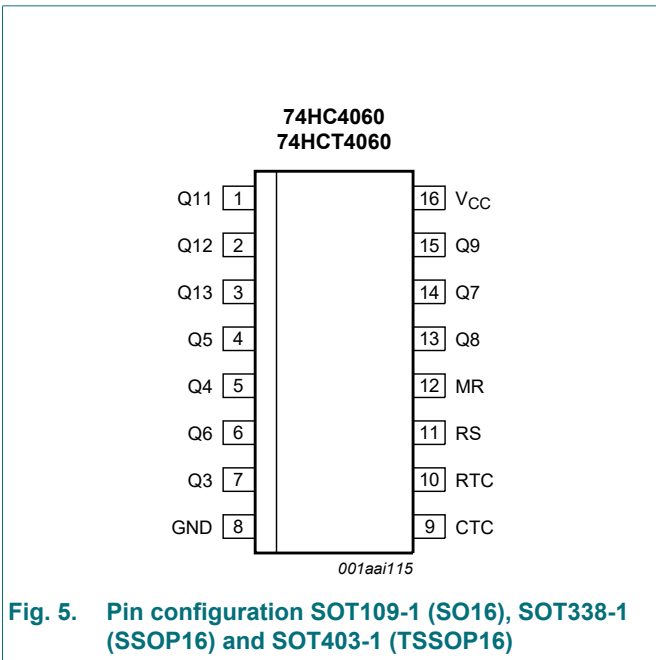


Fig. 5. Pin configuration SOT109-1 (SO16), SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)

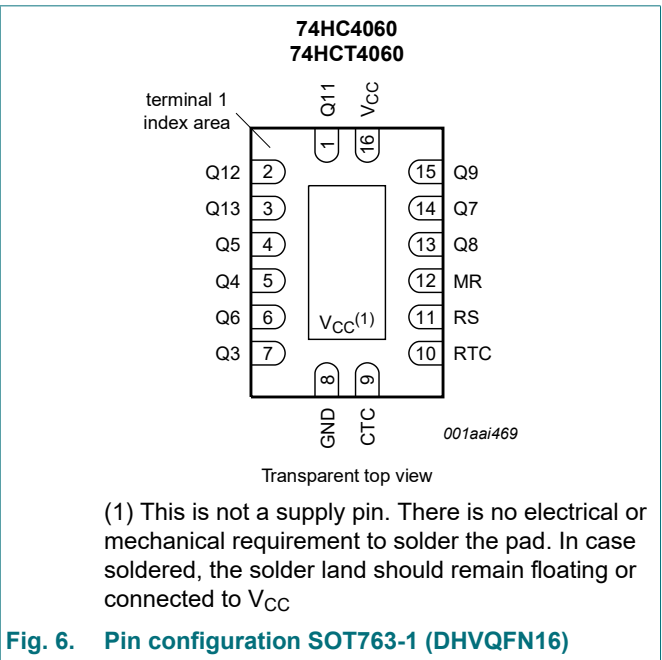


Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11, Q12, Q13	1, 2, 3	counter output
Q3, Q4, Q5, Q6, Q7, Q8, Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input /oscillator pin
MR	12	master reset input (active HIGH)
V _{CC}	16	supply voltage

7. Functional description

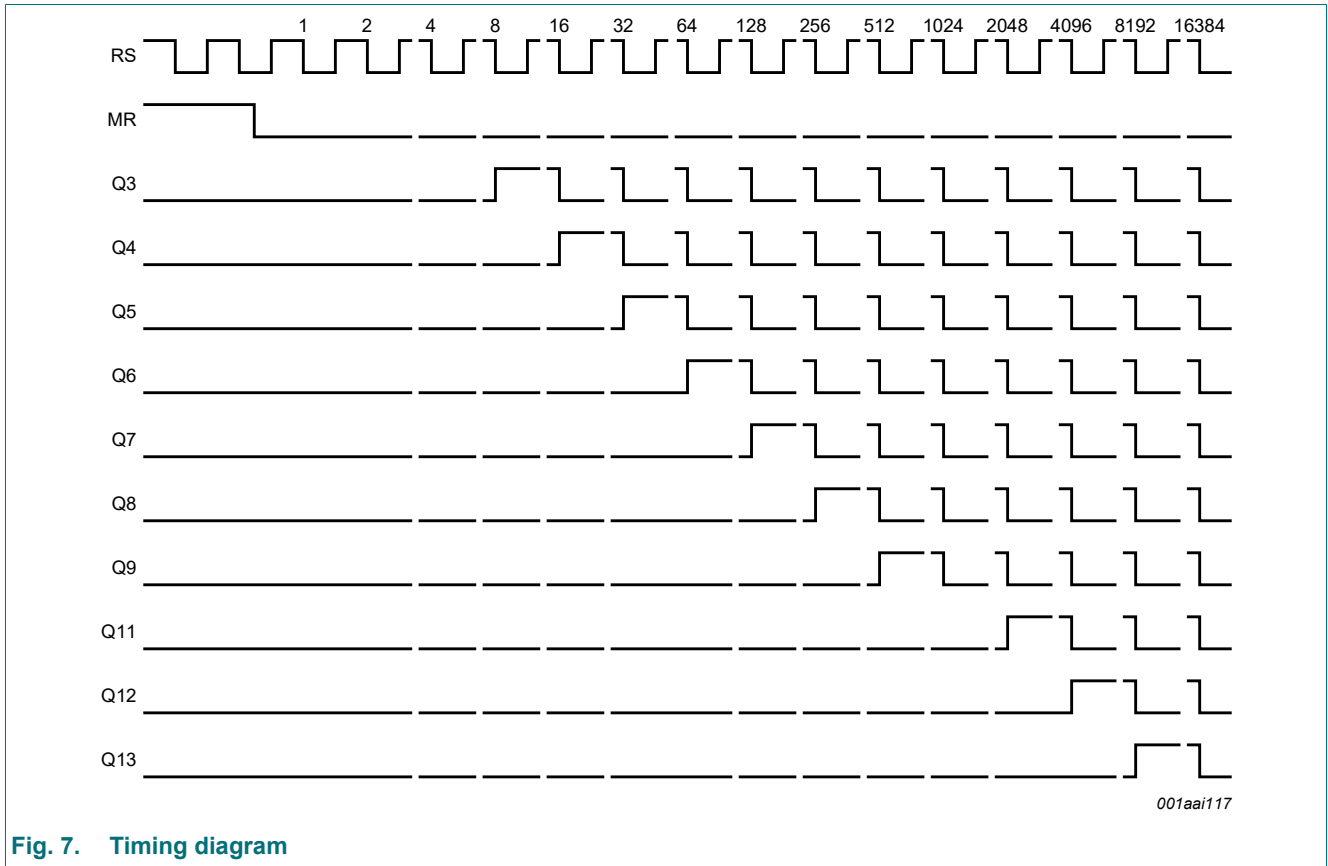


Fig. 7. Timing diagram

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4060			74HCT4060			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4060										
V_{IH}	HIGH-level input voltage	MR input								
		$V_{CC} = 2.0\text{ V}$	1.5	1.3	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.1	-	4.2	-	4.2	-	V
		RS input								
		$V_{CC} = 2.0\text{ V}$	1.7	-	-	1.7	-	1.7	-	V
		$V_{CC} = 4.5\text{ V}$	3.6	-	-	3.6	-	3.6	-	V
V_{IL}	LOW-level input voltage	MR input								
		$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
		RS input								
		$V_{CC} = 2.0\text{ V}$	-	-	0.3	-	0.3	-	0.3	V
		$V_{CC} = 4.5\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
$V_{CC} = 6.0\text{ V}$	-	-	1.2	-	1.2	-	1.2	V		

14-stage binary ripple counter with oscillator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	RTC output; RS = MR = GND								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -2.6 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = -3.3 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		RTC output; RS = MR = V _{CC}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -0.65 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = -0.85 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		CTC output; RS = V _{IH} ; MR = V _{IL}								
		I _O = -3.2 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = -4.2 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		V _I = V _{IH} or V _{IL} ; except RTC output								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		V _I = V _{IH} or V _{IL} ; except RTC and CTC outputs								
I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V		
I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V		
V _{OL}	LOW-level output voltage	RTC output; RS = V _{CC} ; MR = GND								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 2.6 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I _O = 3.3 mA; V _{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V
		CTC output; RS = V _{IL} ; MR = V _{IH}								
		I _O = 3.2 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I _O = 4.2 mA; V _{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V
		V _I = V _{IH} or V _{IL} ; except RTC output								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		V _I = V _{IH} or V _{IL} ; except RTC and CTC outputs								
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V

14-stage binary ripple counter with oscillator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4060										
V_{IH}	HIGH-level input voltage	MR input; $V_{CC} = 4.5$ V to 5.5 V [1]	2.0	-	-	2.0	-	2.0	-	V
		RS input; $V_{CC} = 4.5$ V	3.6	-	-	3.6	-	3.6	-	V
V_{IL}	LOW-level input voltage	MR input; $V_{CC} = 4.5$ V to 5.5 V [1]	-	-	0.8	-	0.8	-	0.8	V
		RS input; $V_{CC} = 4.5$ V	-	-	0.9	-	0.9	-	0.9	V
V_{OH}	HIGH-level output voltage	RTC output; RS = MR = V_{CC}								
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -0.65$ mA; $V_{CC} = 4.5$ V	3.98	-	-	3.84	-	3.7	-	V
		RTC output; RS = MR = GND								
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -2.6$ mA; $V_{CC} = 4.5$ V	3.98	-	-	3.84	-	3.7	-	V
		CTC output; RS = V_{IH} ; MR = V_{IL}								
		$I_O = -3.2$ mA; $V_{CC} = 4.5$ V	3.98	-	-	3.84	-	3.7	-	V
		$V_I = V_{IH}$ or V_{IL} ; except RTC output								
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; except RTC and CTC outputs								
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.98	-	-	3.84	-	3.7	-	V
		RTC output; RS = V_{CC} ; MR = GND								
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 2.6$ mA; $V_{CC} = 4.5$ V	-	-	0.26	-	0.33	-	0.4	V
		CTC output; RS = V_{IL} ; MR = V_{IH}								
		$I_O = 3.2$ mA; $V_{CC} = 4.5$ V	-	-	0.26	-	0.33	-	0.4	V
		$V_I = V_{IH}$ or V_{IL} ; except RTC output								
$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V		
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
		$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_O = 0$ A	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A	-	40	144	-	180	-	196	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

[1] For HCT4060, only input MR (pin 12) has TTL input switching levels.

11. Dynamic characteristics

Table 6. Dynamic characteristics

$GND = 0\text{ V}$; $C_L = 50\text{ pF}$ unless otherwise specified; for test circuit see [Fig. 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4060										
t_{pd}	propagation delay	RS to Q3; see Fig. 8 [1]								
		$V_{CC} = 2.0\text{ V}$	-	99	300	-	375	-	450	ns
		$V_{CC} = 4.5\text{ V}$	-	36	60	-	75	-	90	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	31	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	29	51	-	64	-	77	ns
		Qn to Qn+1; see Fig. 9 [2]								
		$V_{CC} = 2.0\text{ V}$	-	22	80	-	100	-	120	ns
		$V_{CC} = 4.5\text{ V}$	-	8	16	-	20	-	24	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	6	-	-	-	-	-	ns
$V_{CC} = 6.0\text{ V}$	-	6	14	-	17	-	20	ns		
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 10								
		$V_{CC} = 2.0\text{ V}$	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5\text{ V}$	-	20	35	-	44	-	53	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	16	30	-	37	-	45	ns
t_t	transition time	Qn; see Fig. 8 [3]								
		$V_{CC} = 2.0\text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0\text{ V}$	-	6	13	-	16	-	19	ns
t_w	pulse width	RS (HIGH or LOW); see Fig. 8								
		$V_{CC} = 2.0\text{ V}$	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	5	-	17	-	20	-	ns
		MR (HIGH); see Fig. 10								
		$V_{CC} = 2.0\text{ V}$	80	25	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	9	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	7	-	17	-	20	-	ns
t_{rec}	recovery time	MR to RS; see Fig. 10								
		$V_{CC} = 2.0\text{ V}$	100	28	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	10	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	8	-	21	-	26	-	ns

14-stage binary ripple counter with oscillator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	RS; see Fig. 8								
		V _{CC} = 2.0 V	6	26	-	4.8	-	4	-	MHz
		V _{CC} = 4.5 V	30	80	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	87	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	95	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 5 V; f _i = 1 MHz [4]	-	40	-	-	-	-	-	pF
74HCT4060										
t _{pd}	propagation delay	RS to Q3; see Fig. 8 [1]								
		V _{CC} = 4.5 V	-	33	66	-	83	-	99	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	31	-	-	-	-	-	ns
		Qn to Qn+1; see Fig. 9 [2]								
		V _{CC} = 4.5 V	-	8	16	-	20	-	24	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	6	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 10								
		V _{CC} = 4.5 V	-	21	44	-	55	-	66	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	18	-	-	-	-	-	ns
t _t	transition time	Qn; see Fig. 8 [3]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	RS (HIGH or LOW); see Fig. 8								
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		MR (HIGH); see Fig. 10								
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
t _{rec}	recovery time	MR to RS; see Fig. 10								
		V _{CC} = 4.5 V	26	13	-	33	-	39	-	ns
f _{max}	maximum frequency	RS; see Fig. 8								
		V _{CC} = 4.5 V	30	80	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	88	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} - 1.5 V; V _{CC} = 5 V; f _i = 1 MHz [4]	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] Qn+1 is the next Qn output.

[3] t_t is the same as t_{THL} and t_{TLH}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

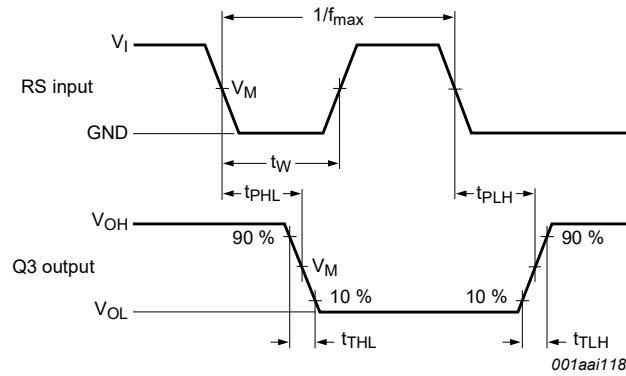
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

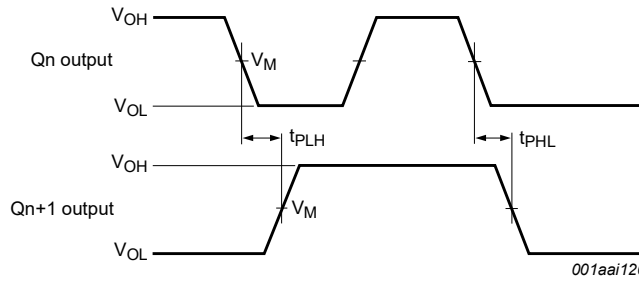
11.1. Waveforms and test circuit



Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

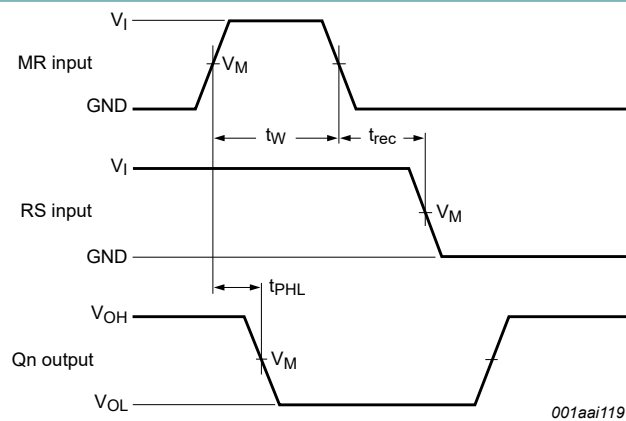
Fig. 8. Waveforms showing the clock (RS) to output (Q3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. Waveforms showing the output Qn to output Qn+1 propagation delays



Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (RS) recovery time

Table 7. Measurement points

Type	Input	Output
	V_M	V_M
74HC4060	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4060	1.3 V	1.3 V

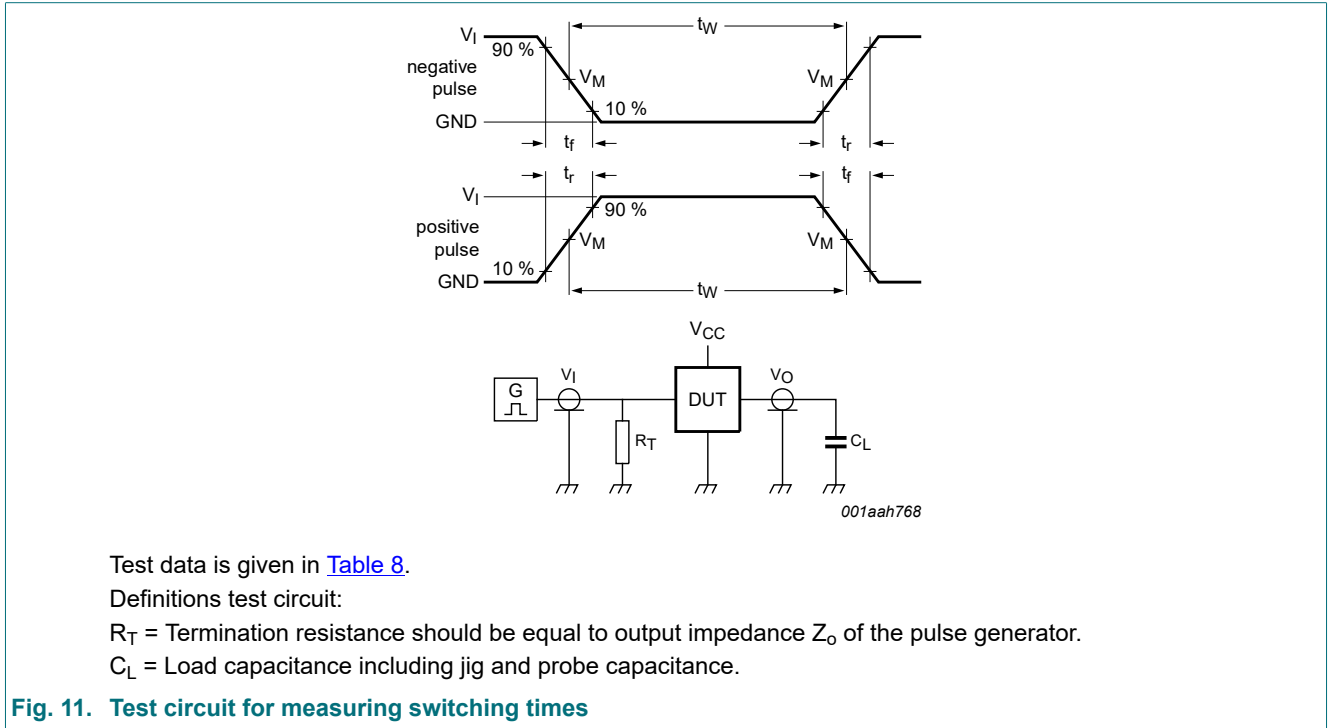


Fig. 11. Test circuit for measuring switching times

Table 8. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4060	V_{CC}	6 ns	15 pF, 50 pF
74HCT4060	3 V	6 ns	15 pF, 50 pF

12. RC oscillator

12.1. Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_2 \approx 2R_t$ and $R_2 C_2 \ll R_t C_t$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the ON resistance in series with it, which typically is 280 Ω at $V_{CC} = 2.0$ V, 130 Ω at $V_{CC} = 4.5$ V and 100 Ω at $V_{CC} = 6.0$ V.

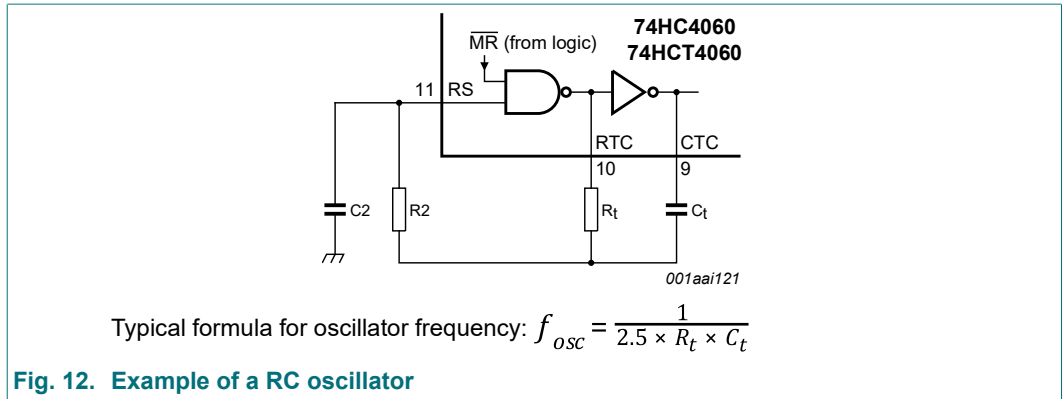


Fig. 12. Example of a RC oscillator

The recommended values for these components to maintain agreement with the typical oscillation formula are:

- $C_t > 50 \text{ pF}$, up to any practical value and $10 \text{ k}\Omega < R_t < 1 \text{ M}\Omega$.
- In order to avoid start-up problems, $R_t \geq 1 \text{ k}\Omega$.

12.2. Typical crystal oscillator circuit

In Fig. 13, R₂ is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R₂ should not be too large. A practical value for R₂ is 2.2 kΩ.

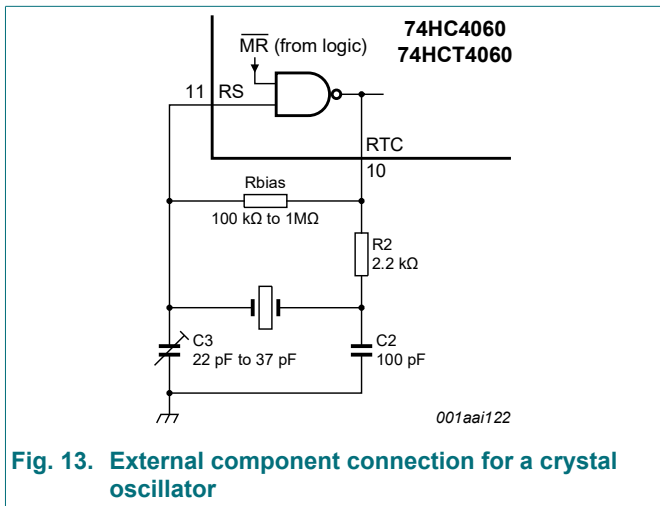


Fig. 13. External component connection for a crystal oscillator

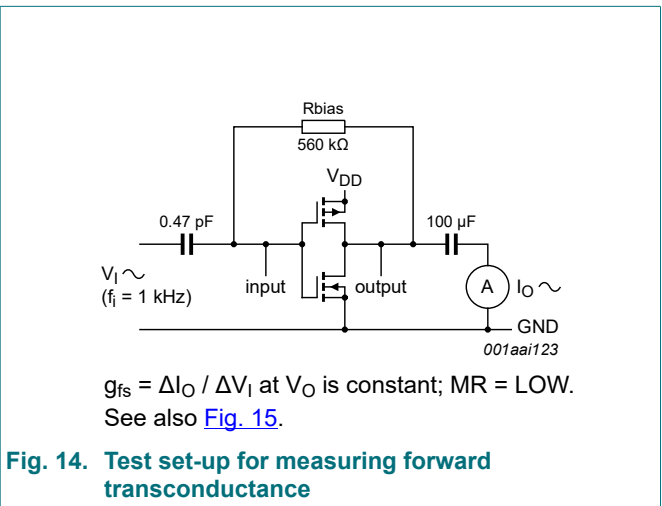
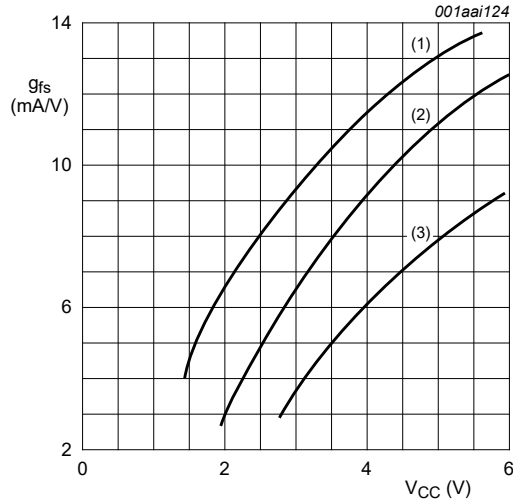
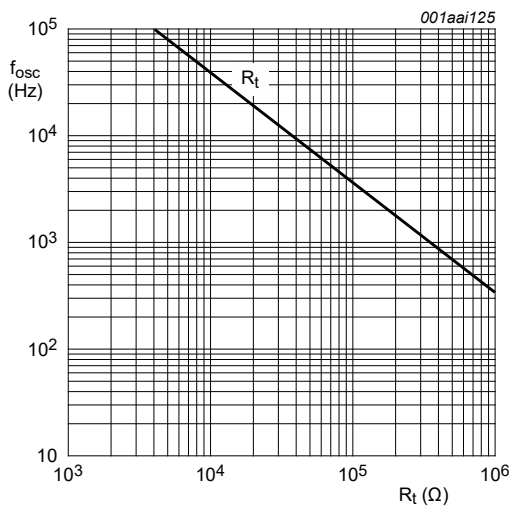


Fig. 14. Test set-up for measuring forward transconductance



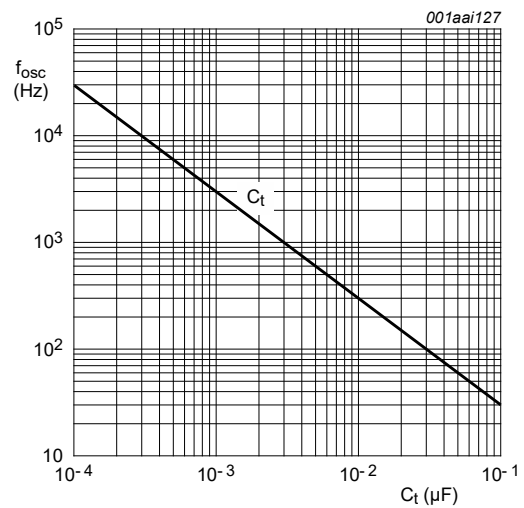
(1) Maximum.
 (2) Typical.
 (3) Minimum.
 $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig. 15. Typical forward transconductance as function of the supply voltage



$V_{CC} = 2.0\text{ V to }6.0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.
 For R_t curve: $C_t = 1\text{ nF}$; $R_2 = 2 \times R_t$.

Fig. 16. RC oscillator frequency as a function of R_t



$V_{CC} = 2.0\text{ V to }6.0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.
 For C_t curve: $R_t = 100\text{ k}\Omega$; $R_2 = 200\text{ k}\Omega$.

Fig. 17. RC oscillator frequency as a function of C_t

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

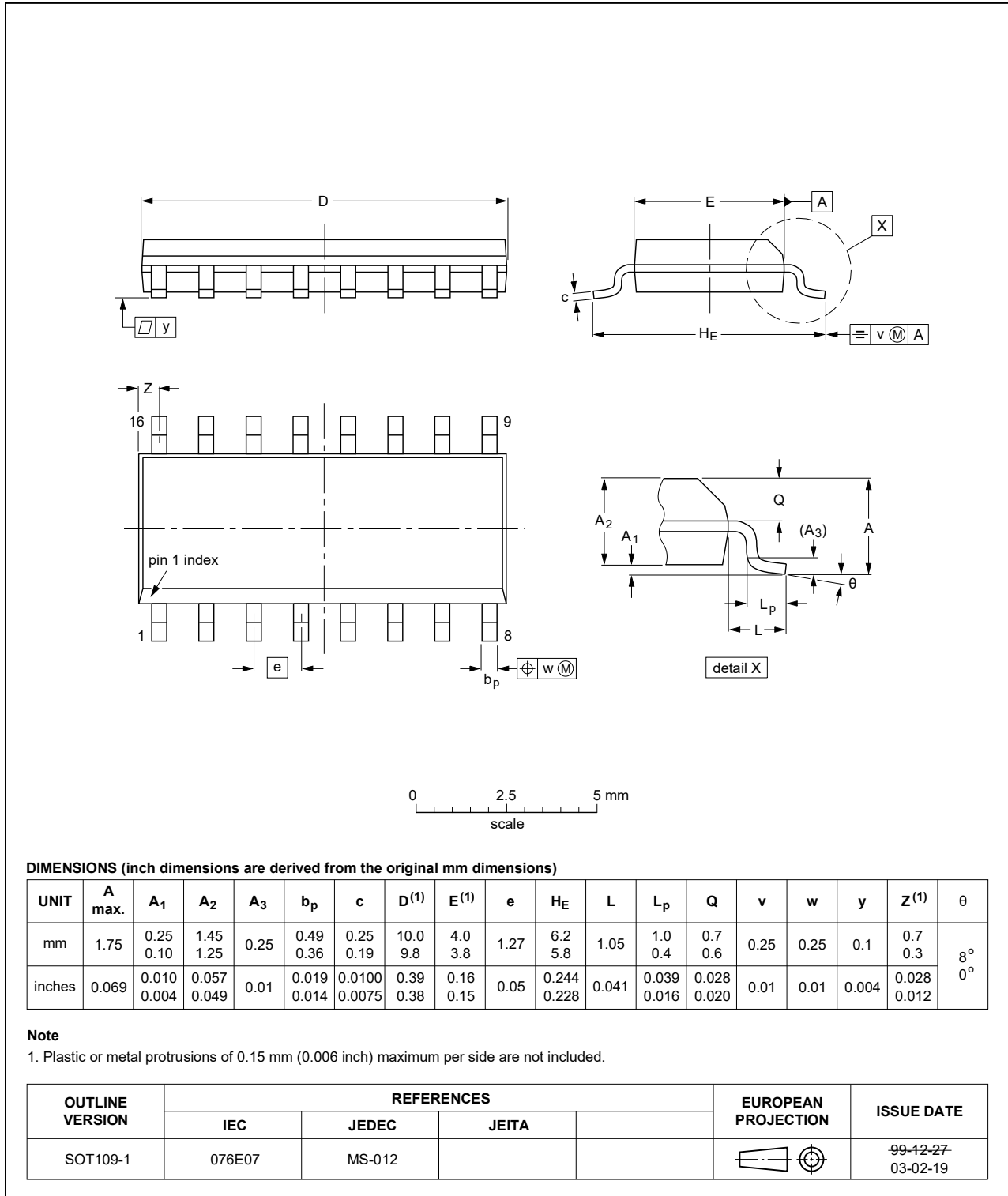


Fig. 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

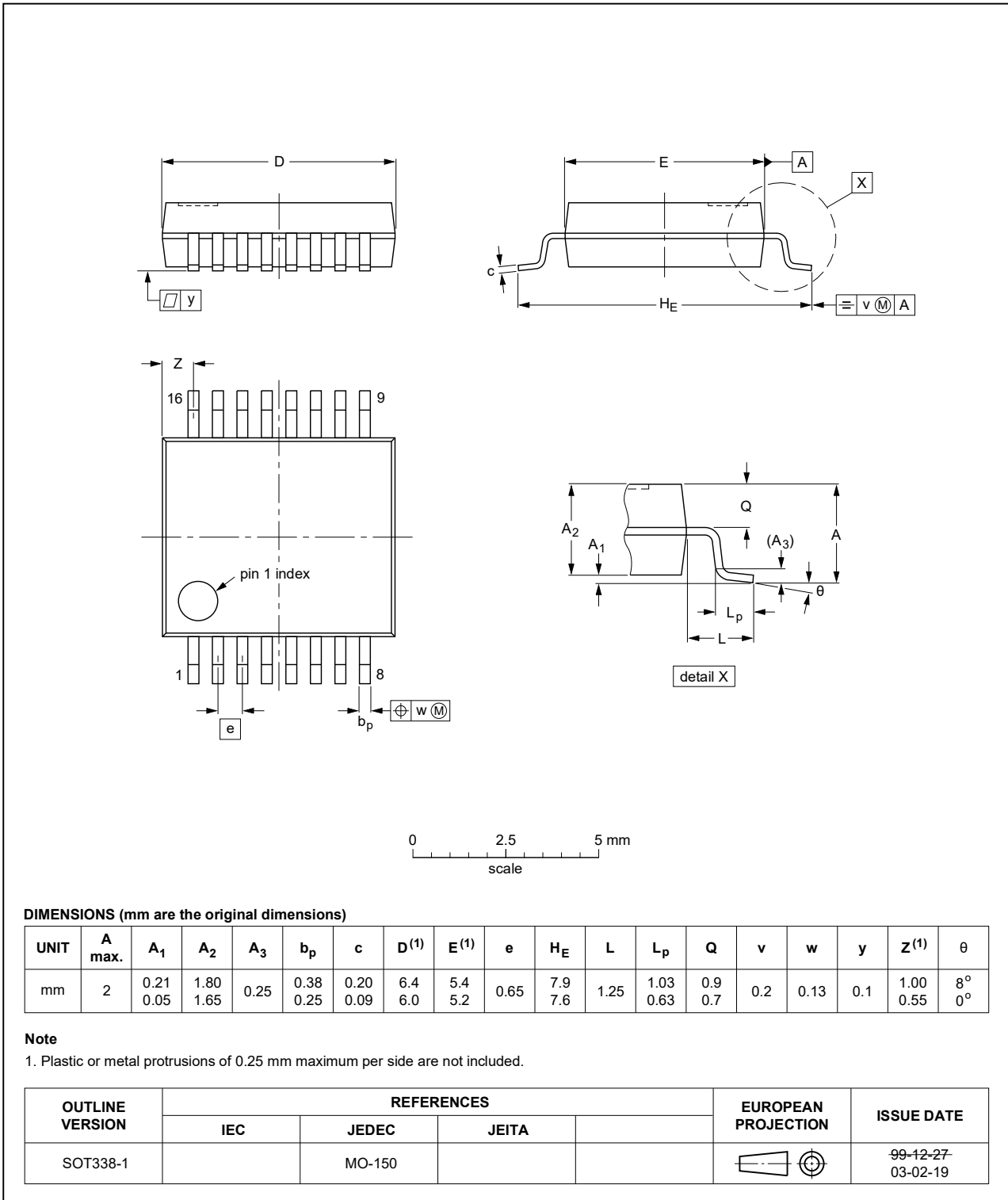


Fig. 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

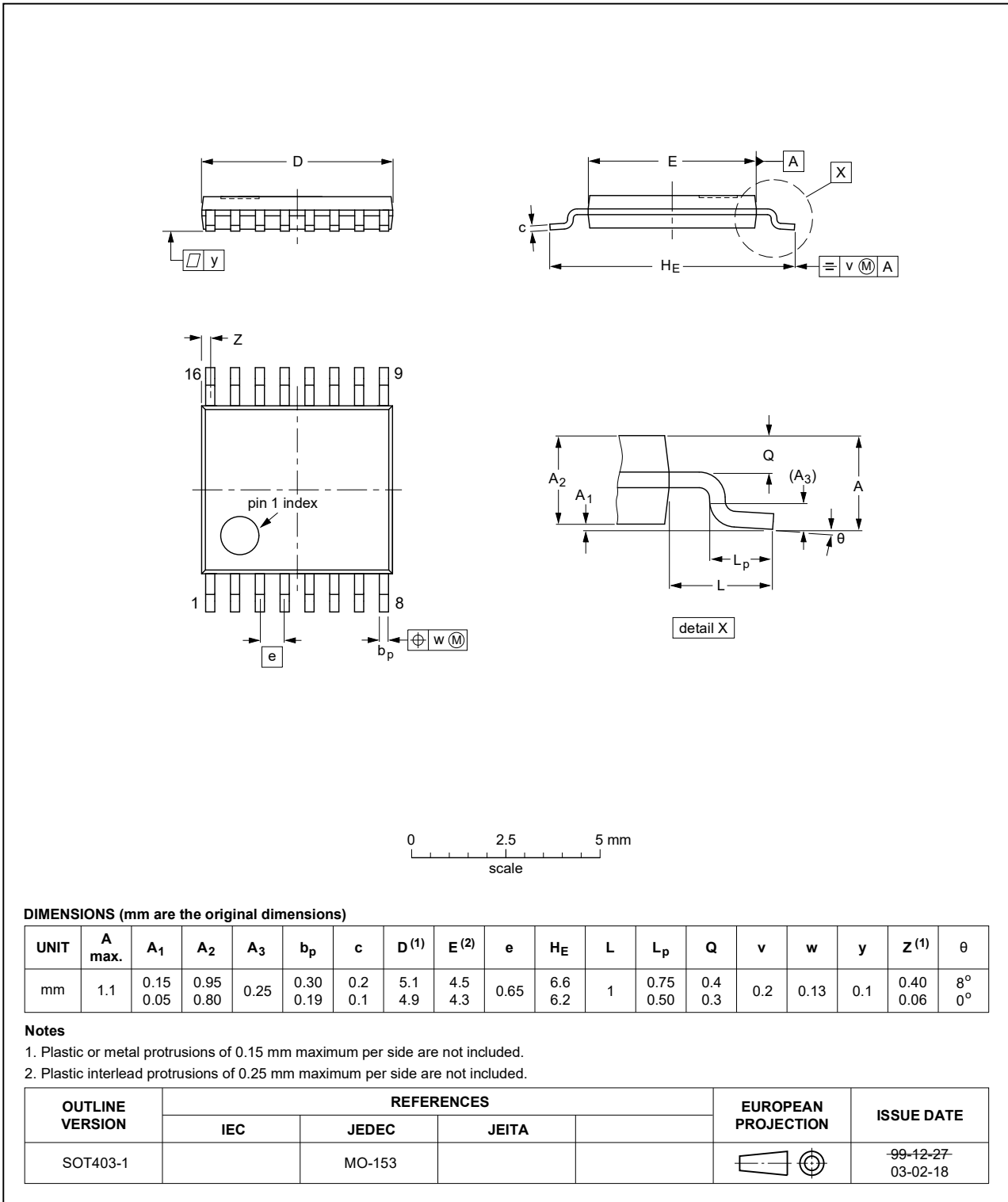


Fig. 20. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

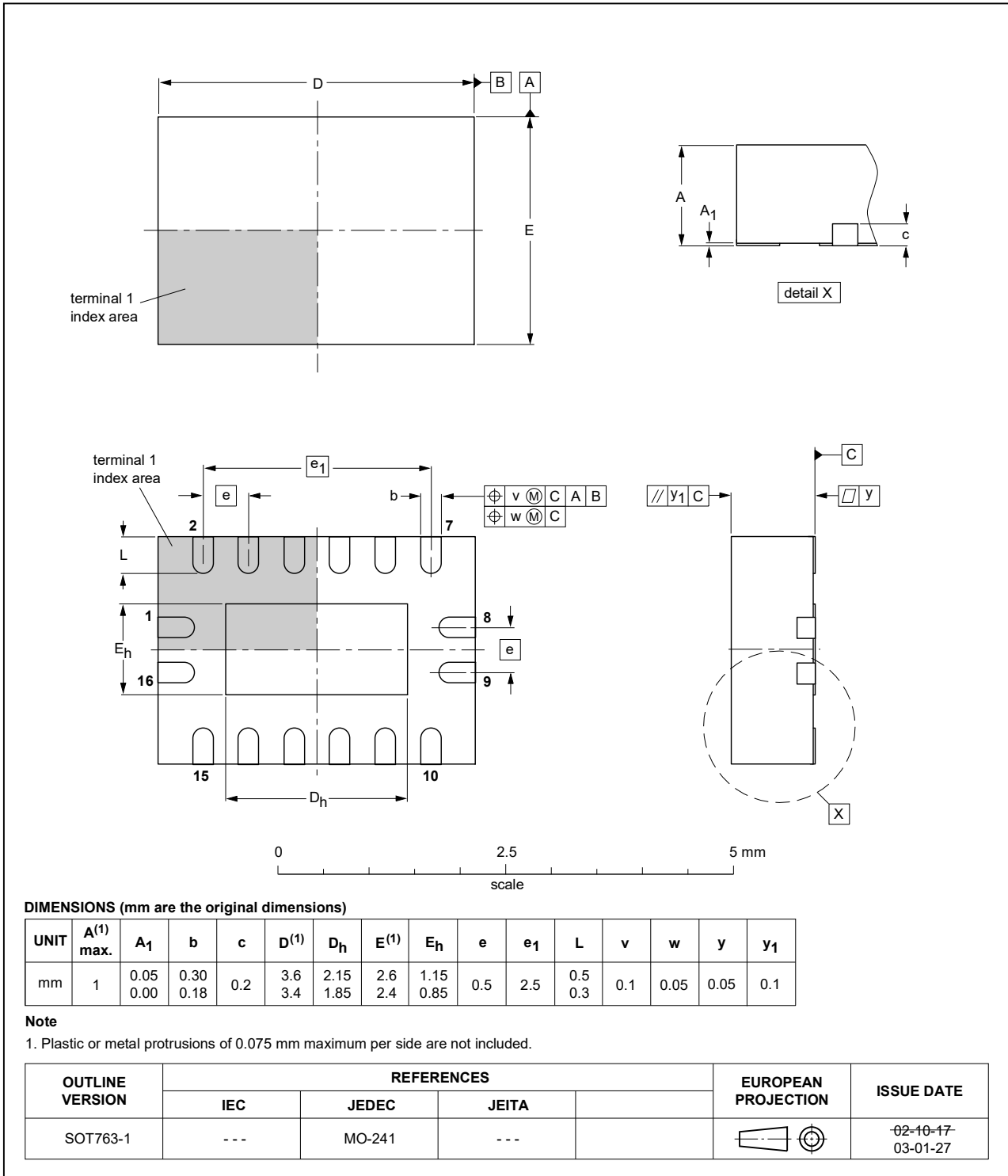


Fig. 21. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4060 v.5	20200508	Product data sheet	-	74HC_HCT4060 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HCT4060DB (SSOP16/SOT338-1) removed. Table 3: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT4060 v.4	20160210	Product data sheet	-	74HC_HCT4060 v.3
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC4060N and 74HCT4060N (SOT38-4) removed. Table 5: HIGH and LOW input levels added for 74HCT4060. (errata) 			
74HC_HCT4060 v.3	20080714	Product data sheet	-	74HC_HCT4060_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Section 4: DHVQFN16 package added. Section 8: derating values added for DHVQFN16 package. Section 13: outline drawing added for DHVQFN16 package. 			
74HC_HCT4060_CNV v.2	19970901	Product specification	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Телефон: 8 (812) 309-75-97 (многоканальный)

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А