14-Bit, 160 MSPS TxDAC+ with 2× Interpolation Filter

AD9772A

FEATURES

Single 3.1 V to 3.5 V supply
14-bit DAC resolution and input data width
160 MSPS input data rate
67.5 MHz reconstruction pass band @ 160 MSPS
74 dBc SFDR @ 25 MHz
2× interpolation filter with high- or low-pass response
73 dB image rejection with 0.005 dB pass-band ripple
Zero-stuffing option for enhanced direct IF performance
Internal 2×/4× clock multiplier
250 mW power dissipation; 13 mW with power-down mode
48-lead LQFP package

APPLICATIONS

Communication transmit channel
W-CDMA base stations, multicarrier base stations, direct IF synthesis, wideband cable systems
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

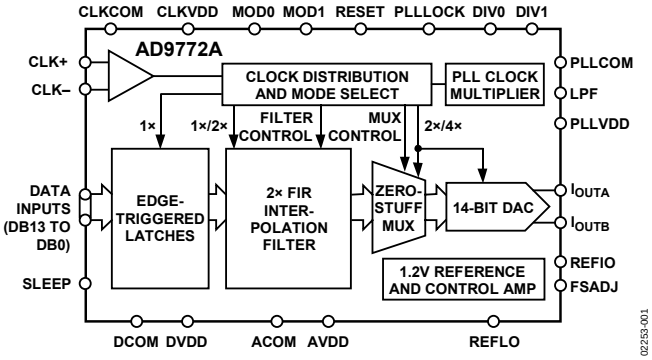

Figure 1.

GENERAL DESCRIPTION

The AD9772A is a single-supply, oversampling, 14-bit digital-to-analog converter (DAC) optimized for baseband or IF waveform reconstruction applications requiring exceptional dynamic range. Manufactured on an advanced CMOS process, it integrates a complete, low distortion 14-bit DAC with a 2× digital interpolation filter and clock multiplier. The on-chip PLL clock multiplier provides all the necessary clocks for the digital filter and the 14-bit DAC. A flexible differential clock input allows for a single-ended or differential clock driver for optimum jitter performance.

For baseband applications, the 2× digital interpolation filter provides a low-pass response, thus providing as much as a threefold reduction in the complexity of the analog reconstruction filter. It does so by multiplying the input data rate by a factor of 2 while suppressing the original upper in-band image by more than 73 dB. For direct IF applications, the 2× digital interpolation filter response can be reconfigured to select the upper in-band image (that is, the high-pass response) while suppressing the original baseband image. To increase the signal level of the higher IF images and their pass-band flatness in direct IF applications, the AD9772A also features a zero-stuffing option in which the data following the 2× interpolation filter is upsampled by a factor of 2 by inserting midscale data samples.

The AD9772A can reconstruct full-scale waveforms with bandwidths of up to 67.5 MHz while operating at an input data rate of 160 MSPS. The 14-bit DAC provides differential current outputs to support differential or single-ended applications.

A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The differential current outputs can be fed into a transformer or a differential op amp topology to obtain a single-ended output voltage using an appropriate resistive load.

The on-chip band gap reference and control amplifier are configured for maximum accuracy and flexibility. The AD9772A can be driven by the on-chip reference or by a variety of external reference voltages. The full-scale current of the AD9772A can be adjusted over a 2 mA to 20 mA range, thus providing additional gain-ranging capabilities.

The AD9772A is available in a 48-lead LQFP package and is specified for operation over the industrial temperature range of –40°C to +85°C.

Rev. C
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PRODUCT HIGHLIGHTS

1. A flexible, low power 2× interpolation filter supporting reconstruction bandwidths of up to 67.5 MHz can be configured for a low- or high-pass response with 73 dB of image rejection for traditional baseband or direct IF applications.
2. A zero-stuffing option enhances direct IF applications.
3. A low glitch, fast settling 14-bit DAC provides exceptional dynamic range for both baseband and direct IF waveform reconstruction applications.
4. The AD9772A digital interface, consisting of edge-triggered latches and a flexible differential or single-ended clock input, can support input data rates up to 160 MSPS.
5. An on-chip PLL clock multiplier generates all of the internal high speed clocks required by the interpolation filter and DAC.
6. The current output(s) of the AD9772A can easily be configured for various single-ended or differential circuit topologies.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)		±3.5		LSB
Differential Nonlinearity (DNL)		±2.0		LSB
Monotonicity (12-Bit)		Guaranteed over specified temperature range		
ANALOG OUTPUT				
Offset Error	−0.025		+0.025	% of FSR
Gain Error				
Without Internal Reference	−2	±0.5	+2	% of FSR
With Internal Reference	−5	±1.5	+5	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	−1.0		+1.25	V
Output Resistance		200		kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		1		µA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (REFLO = 3 V)		10		MΩ
Small-Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift		0		ppm of FSR/°C
Gain Drift				
Without Internal Reference		±50		ppm of FSR/°C
With Internal Reference		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
AVDD				
Voltage Range	3.1	3.3	3.5	V
Analog Supply Current (I_{AVDD})		34	37	mA
Analog Supply Current in Sleep Mode (I_{AVDD})		4.3	6	mA
DVDD				
Voltage Range	3.1	3.3	3.5	V
Digital Supply Current (I_{DVDD})		37	40	mA
CLKVDD, PLLVDD[4] (PLLVDD = 3.3 V)				
Voltage Range	3.1	3.3	3.5	V
Clock Supply Current (I_{CLKVDD} + I_{PLLVDD})		25	30	mA

Parameter	Min	Typ	Max	Unit
CLKVDD (PLLVDD = 0 V)				
Voltage Range	3.1	3.3	3.5	V
Clock Supply Current (I_{CLKVDD})		6.0		mA
Nominal Power Dissipation[5]		253	272	mW
Power Supply Rejection Ratio (PSRR)[6]				
PSRR – AVDD	−0.6		+0.6	% of FSR/V
PSRR – DVDD	−0.025		+0.025	% of FSR/V
OPERATING RANGE	−40		+85	°C

[1] Measured at I_{OUTA} driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3] Use an external amplifier to drive any external load.
[4] Measured at f_{DATA} = 100 MSPS and f_{OUT} = 1 MHz with DIV1 and DIV0 = 0 V.
[5] Measured with PLL enabled at f_{DATA} = 50 MSPS and f_{OUT} = 1 MHz.
[6] Measured over a 3.0 V to 3.6 V range.

DYNAMIC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 3.3 V, I_{OUTFS} = 20 mA, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum DAC Output Update Rate (f_{DAC})	400			MSPS
Output Settling Time (t_{ST}) (to 0.025%)		11		ns
Output Propagation Delay[1] (t_{PD})		17		ns
Output Rise Time (10% to 90%)[2]		0.8		ns
Output Fall Time (10% to 90%)		0.8		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA√Hz
AC LINEARITY—BASEBAND MODE				
Spurious-Free Dynamic Range (SFDR) to Nyquist (f_{OUT} = 0 dBFS)				
f_{DATA} = 65 MSPS; f_{OUT} = 1.01 MHz		82		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 10.01 MHz		75		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 25.01 MHz		73		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 5.02 MHz		82		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 20.02 MHz		75		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 50.02 MHz		65		dBc
Two-Tone Intermodulation (IMD) to Nyquist (f_{OUT1} = f_{OUT2} = −6 dBFS)				
f_{DATA} = 65 MSPS; f_{OUT1} = 5.01 MHz; f_{OUT2} = 6.01 MHz		85		dBc
f_{DATA} = 65 MSPS; f_{OUT1} = 15.01 MHz; f_{OUT2} = 17.51 MHz		75		dBc
f_{DATA} = 65 MSPS; f_{OUT1} = 24.1 MHz; f_{OUT2} = 26.2 MHz		68		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 10.02 MHz; f_{OUT2} = 12.02 MHz		85		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 30.02 MHz; f_{OUT2} = 35.02 MHz		70		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 48.2 MHz; f_{OUT2} = 52.4 MHz		65		dBc
Total Harmonic Distortion (THD)				
f_{DATA} = 65 MSPS; f_{OUT} = 1.0 MHz; 0 dBFS		−80		dB
f_{DATA} = 78 MSPS; f_{OUT} = 10.01 MHz; 0 dBFS		−74		dB
Signal-to-Noise Ratio (SNR)				
f_{DATA} = 65 MSPS; f_{OUT} = 16.26 MHz; 0 dBFS		71		dB
f_{DATA} = 100 MSPS; f_{OUT} = 25.1 MHz; 0 dBFS		71		dB
Adjacent Channel Power Ratio (ACPR)				
WCDMA with 4.1 MHz BW, 5 MHz Channel Spacing				
IF = 16 MHz, f_{DATA} = 65.536 MSPS		78		dBc
IF = 32 MHz, f_{DATA} = 131.072 MSPS		68		dBc
Four-Tone Intermodulation				
15.6 MHz, 15.8 MHz, 16.2 MHz, and 16.4 MHz at −12 dBFS		88		dBFS
f_{DATA} = 65 MSPS, Missing Center				
AC LINEARITY—IF MODE				
Four-Tone Intermodulation at IF = 70 MHz				
68.1 MHz, 69.3 MHz, 71.2 MHz, and 72.0 MHz at −20 dBFS		77		dBFS
f_{DATA} = 52 MSPS, f_{DAC} = 208 MHz				

[1] Propagation delay is delay from the CLK+/CLK− input to the DAC update.
[2] Measured single-ended into 50 Ω load.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current[1]	−10		+10	µA
Logic 0 Current	−10		+10	µA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
PLL CLOCK ENABLED (SEE Figure 2)				
Input Setup Time (t_S)				
T_A = 25°C	1.5			ns
T_A = −40 to +85°C	2.1			ns
Input Hold Time (t_H)				
T_A = 25°C	1.3			ns
T_A = −40 to +85°C	1.6			ns
Latch Pulse Width (t_{LPW}), T_A = 25°C	1.5			ns
PLL CLOCK DISABLED (SEE Figure 3)				
Input Setup Time (t_S)				
T_A = 25°C	−0.7			ns
T_A = −40 to +85°C	−0.4			ns
Input Hold Time (t_H)				
T_A = 25°C	3.3			ns
T_A = −40 to +85°C	3.7			ns
Latch Pulse Width (t_{LPW}), T_A = 25°C	1.5			ns
CLK+/CLK− to PLLLOCK Delay (t_{OD})				
T_A = 25°C	1.9		2.8	ns
T_A = −40 to +85°C	1.8		3.3	ns
PLLLOCK (V_{OH}), T_A = 25°C	3.0			V
PLLLOCK (V_{OL}), T_A = 25°C			0.3	V

[1] MOD0, MOD1, DIV0, DIV1, SLEEP, RESET have typical input currents of 15 µA.

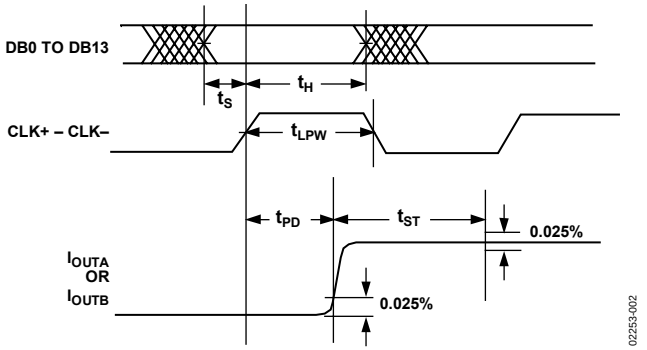


Figure 2. Timing Diagram—PLL Clock Multiplier Enabled

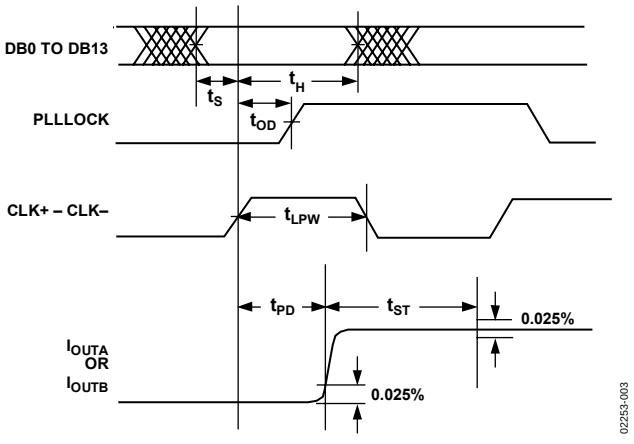


Figure 3. Timing Diagram—PLL Clock Multiplier Disabled

DIGITAL FILTER SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
MAXIMUM INPUT DATA RATE (f_{DATA})	150			MSPS
DIGITAL FILTER CHARACTERISTICS				
Pass-Bandwidth[1]: 0.005 dB		0.401		f_{OUT}/f_{DATA}
Pass-Bandwidth: 0.01 dB		0.404		f_{OUT}/f_{DATA}
Pass-Bandwidth: 0.1 dB		0.422		f_{OUT}/f_{DATA}
Pass-Bandwidth: −3 dB		0.479		f_{OUT}/f_{DATA}
LINEAR PHASE (FIR IMPLEMENTATION)				
STOP BAND REJECTION		73		dB
0.606 f_{CLOCK} to 1.394 f_{CLOCK}		11		Input clocks
GROUP DELAY[2]				
IMPULSE RESPONSE DURATION				
−40 dB		36		Input clocks
−60 dB		42		Input clocks

[1] Excludes sin(x)/x characteristic of DAC.
[2] Defined as the number of data clock cycles between impulse input and peak of output response.

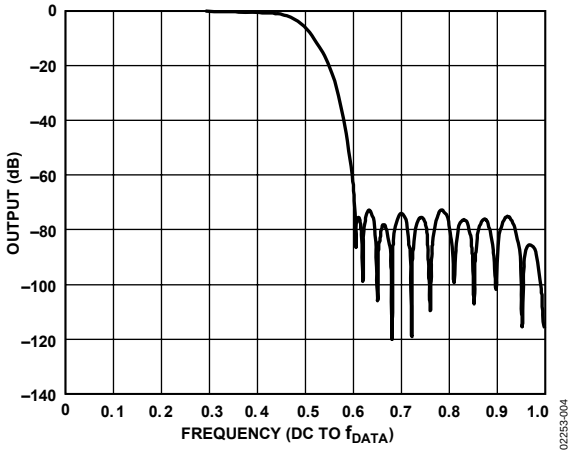


Figure 4. FIR Filter Frequency Response—Baseband Mode

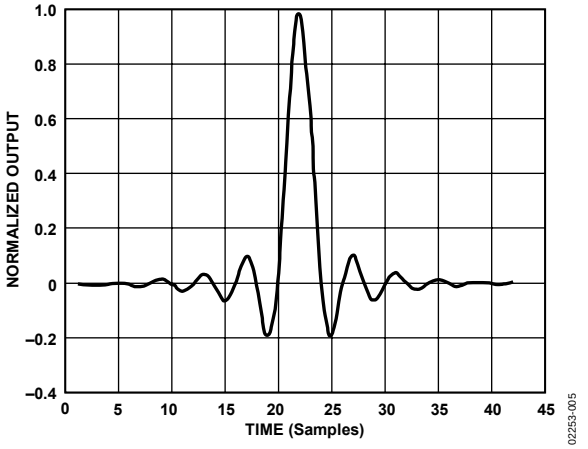


Figure 5. FIR Filter Impulse Response—Baseband Mode

Table 5. Integer Filter Coefficients for Interpolation Filter (43-Tap Half-Band FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(43)	10
H(2)	H(42)	0
H(3)	H(41)	−31
H(4)	H(40)	0
H(5)	H(39)	69
H(6)	H(38)	0
H(7)	H(37)	−138
H(8)	H(36)	0
H(9)	H(35)	248
H(10)	H(34)	0
H(11)	H(33)	−419
H(12)	H(32)	0
H(13)	H(31)	678
H(14)	H(30)	0
H(15)	H(29)	−1083
H(16)	H(28)	0
H(17)	H(27)	1776
H(18)	H(26)	0
H(19)	H(25)	−3282
H(20)	H(24)	0
H(21)	H(23)	10,364
H(22)		16,384

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect to	Rating
AVDD, DVDD, CLKVDD, PLLVDD	ACOM, DCOM, CLKCOM, PLLCOM	−0.3 V to +4.0 V
AVDD, DVDD, CLKVDD, PLLVDD	AVDD, DVDD, CLKVDD, PLLVDD	−4.0 V to +4.0 V
ACOM, DCOM, CLKCOM, PLLCOM	ACOM, DCOM, CLKCOM, PLLCOM	−0.3 V to +0.3 V
REFIO, REFLO, FSADJ, SLEEP	ACOM	−0.3 V to AVDD + 0.3 V
I_{OUTA}, I_{OUTB}	ACOM	−1.0 V to AVDD + 0.3 V
DB0 to DB13, MOD0, MOD1, PLLLOCK	DCOM	−0.3 V to DVDD + 0.3 V
CLK+, CLK−	CLKCOM	−0.3 V to CLKVDD + 0.3 V
DIV0, DIV1, RESET	CLKCOM	−0.3 V to CLKVDD + 0.3 V
LPF	PLLCOM	−0.3 V to PLLVDD + 0.3 V
Junction Temperature		125°C
Storage Temperature		−65°C to +150°C
Lead Temperature (10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP	91	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

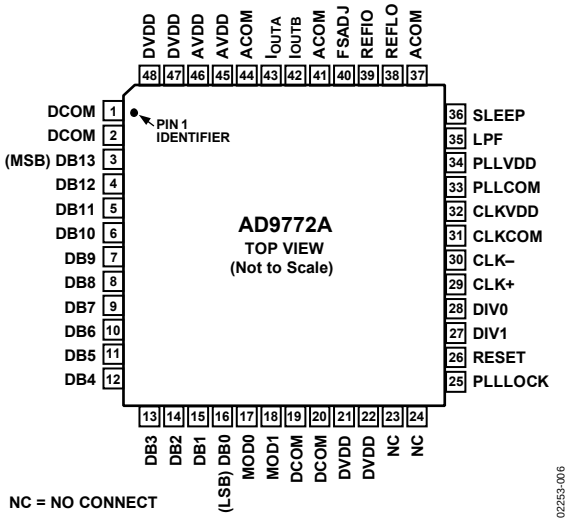


Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 19, 20	DCOM	Digital Common.
3	DB13	Most Significant Data Bit (MSB).
4 to 15	DB12 to DB1	Data Bit 1 to Data Bit 12.
16	DB0	Least Significant Data Bit (LSB).
17	MOD0	Digital High-Pass Filter Response. Active high. This pin invokes the digital high-pass filter response (that is, half-wave digital mixing mode). Note that quarter-wave digital mixing occurs if this pin and the MOD1 pin are set high.
18	MOD1	Zero-Stuffing Mode. Active high. This pin invokes zero-stuffing mode. Note that quarter-wave digital mixing occurs if this pin and the MOD0 pin are set high.
23, 24	NC	No Connect. Leave open.
21, 22, 47, 48	DVDD	Digital Supply Voltage (3.1 V to 3.5 V).
25	PLLLOCK	Lock Signal of the Phase-Lock Loop. This pin provides the lock signal of the phase-lock loop when the PLL clock multiplier is enabled, and provides the 1× clock output when the PLL clock multiplier is disabled. High indicates that PLL is locked to the input clock. The maximum fanout is 1 (that is, <10 pF).
26	RESET	Internal Divider Reset. This pin can reset the internal driver to synchronize the internal 1× clock to the input data and/or multiple AD9772A devices. The reset is initiated if this pin is momentarily brought high when PLL is disabled.
27, 28	DIV1, DIV0	PLL Prescaler Divide Ratio. DIV1 and DIV0 set the prescaler divide ratio of the PLL (refer to Table 10).
29	CLK+	Noninverting Input to Differential Clock. Bias this pin to the midsupply (that is, CLKVDD/2).
30	CLK–	Inverting Input to Differential Clock. Bias this pin to the midsupply (that is, CLKVDD/2).
31	CLKCOM	Clock Input Common.
32	CLKVDD	Clock Input Supply Voltage (3.1 V to 3.5 V).
33	PLLCOM	Phase-Lock Loop Common.
34	PLLVDD	Phase-Lock Loop (PLL) Supply Voltage (3.1 V to 3.5 V). To disable the PLL clock multiplier, connect PLLVDD to PLLCOM.
35	LPF	PLL Loop Filter Node. This pin should be left as a no connect (open) unless the DAC update rate is less than 10 MSPS, in which case a series RC should be connected from LPF to PLLVDD as indicated in Figure 61.
36	SLEEP	Power-Down Control Input. Active high. When this pin is not used, connect it to ACOM.
37, 41, 44	ACOM	Analog Common.
38	REFLO	Reference Ground When Internal 1.2 V Reference Is Used. Connect this pin to AVDD to disable the internal reference.

Pin No.	Mnemonic	Description
39	REFIO	Reference Input/Output. This pin serves as the reference input when the internal reference is disabled (that is, when REFLO is tied to AVDD), or it serves as the 1.2 V reference output when the internal reference is activated (that is, when REFLO is tied to ACOM). If the internal reference is activated, a 0.1 µ F capacitor to ACOM is required.
40	FSADJ	Full-Scale Current Output Adjust.
42	I_{OUTB}	Complementary DAC Current Output. Full-scale current is selected when all data bits are 0s.
43	I_{OUTA}	DAC Current Output. Full-scale current is selected when all data bits are 1s.
45, 46	AVDD	Analog Supply Voltage (3.1 V to 3.5 V).

TERMINOLOGY

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output and is determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale that is associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value. It is measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
Spurious-free dynamic range is the difference, in decibels, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Pass Band
Pass band is the frequency band in which any input applied therein passes unattenuated to the DAC output.

Stop-Band Rejection
Stop-band rejection is the amount of attenuation of a frequency outside the pass band applied to the DAC relative to a full-scale signal applied at the DAC input within the pass band.

Group Delay
Group delay is the number of input clocks between an impulse applied at the device input and the peak DAC output current.

Impulse Response
Impulse response is the response of the device to an impulse applied to the input.

Adjacent-Channel Power Ratio (ACPR)
ACPR is a ratio, in dBc, between the measured power within a channel relative to its adjacent channel.

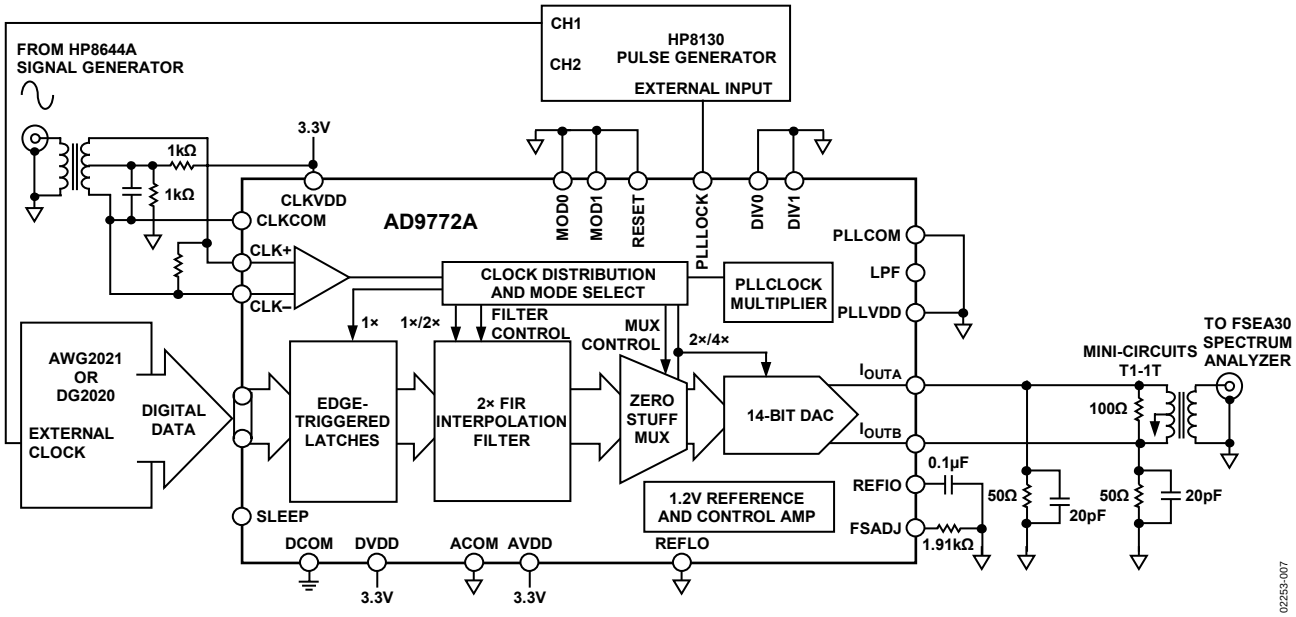


Figure 7. Basic AC Characterization Test Setup

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V, CLKDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA. PLL disabled.

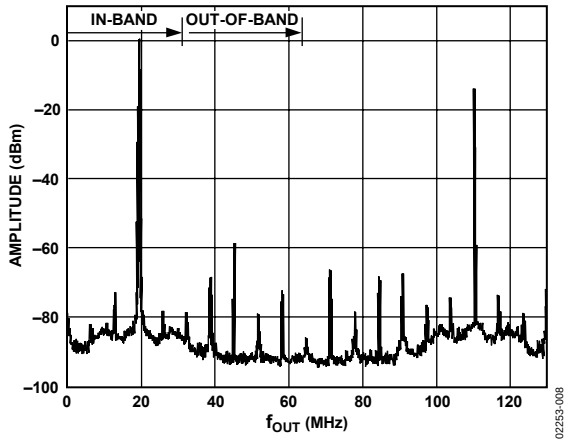


Figure 8. Single-Tone Spectral Characteristics @ f_{DATA} = 65 MSPS with f_{OUT} = f_{DATA}/3

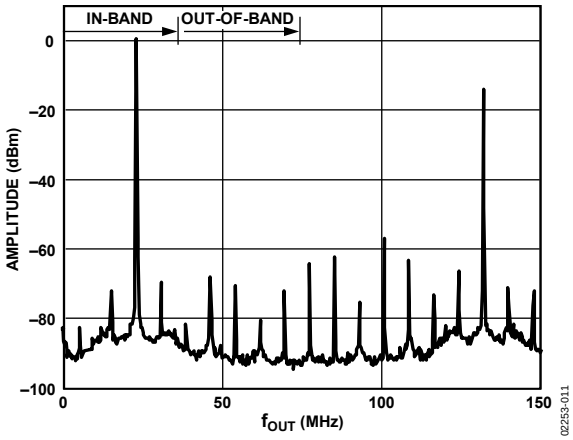


Figure 11. Single-Tone Spectral Characteristics @ f_{DATA} = 78 MSPS with f_{OUT} = f_{DATA}/3

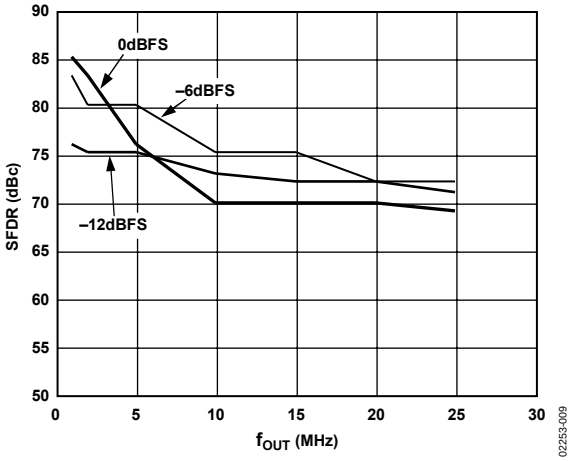


Figure 9. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS

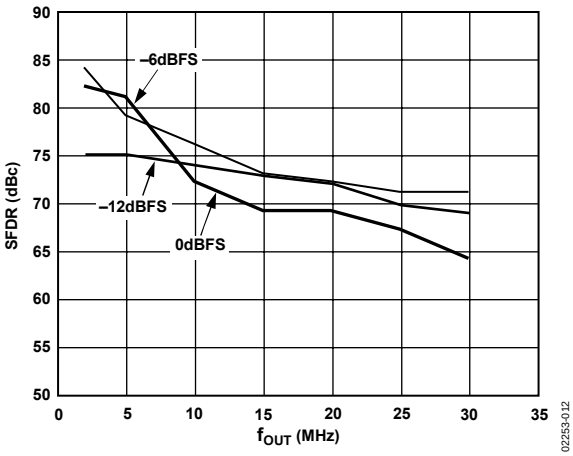


Figure 12. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS

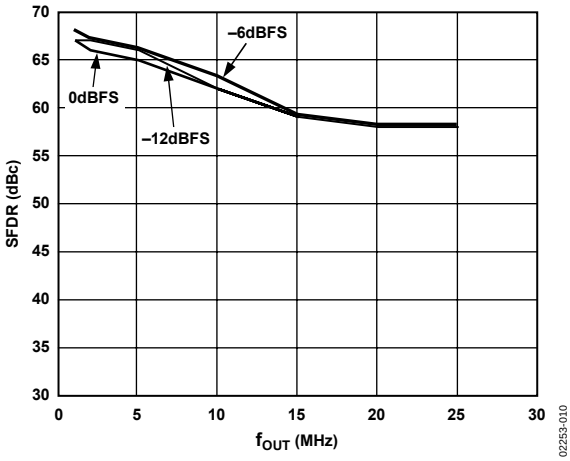


Figure 10. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS

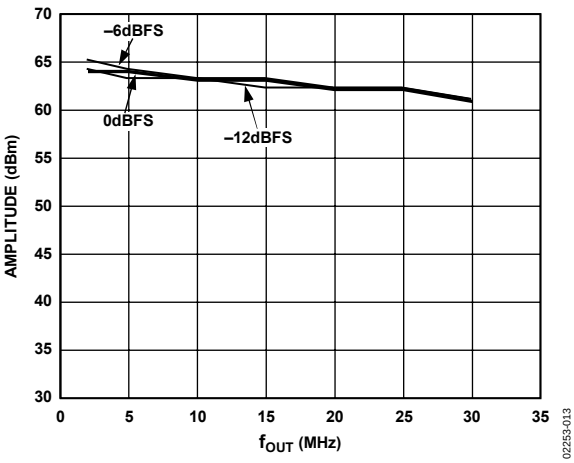


Figure 13. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS

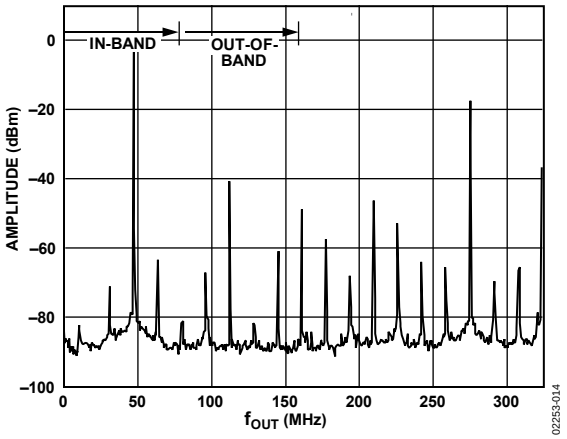


Figure 14. Single-Tone Spectral Characteristics @ f_{DATA} = 160 MSPS with $f_{OUT} = f_{DATA}/3$

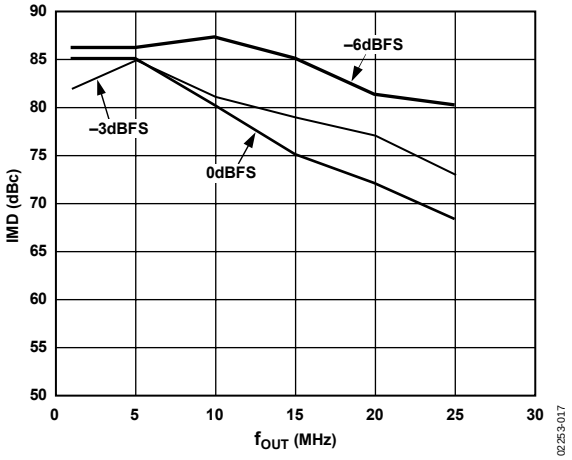


Figure 17. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 65 MSPS

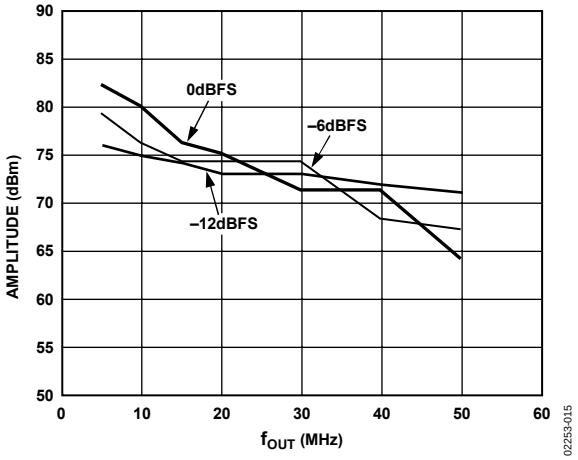


Figure 15. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS

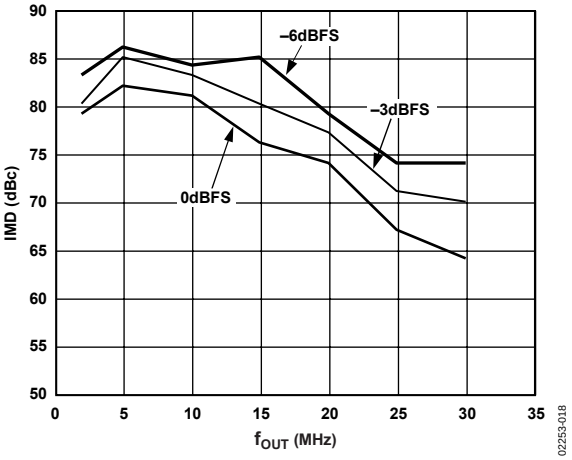


Figure 18. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 78 MSPS

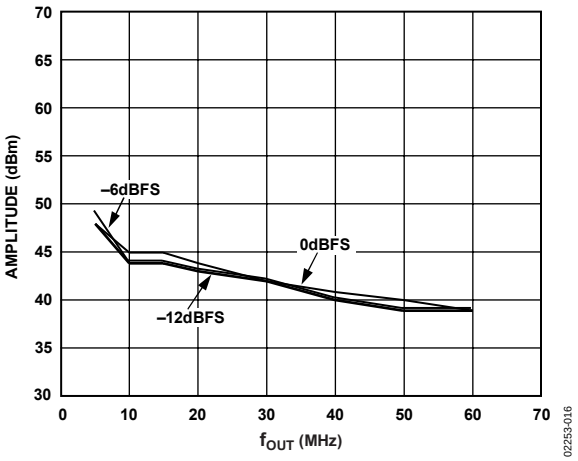


Figure 16. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS

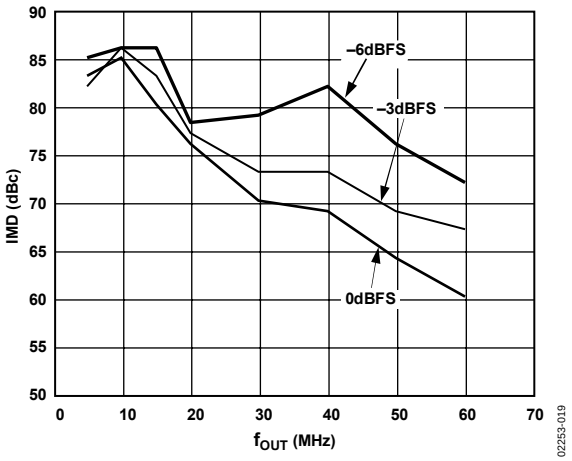


Figure 19. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 160 MSPS

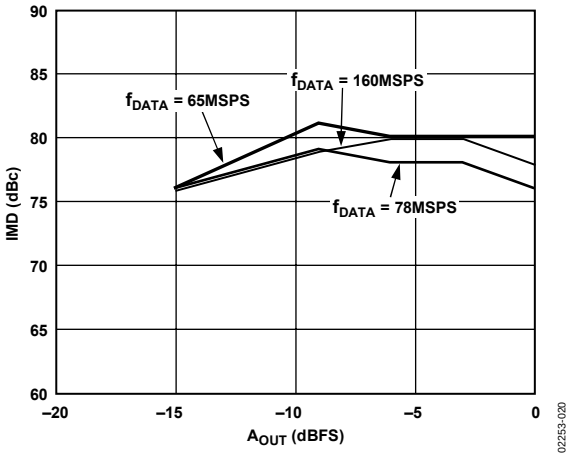


Figure 20. Third-Order IMD Products vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$

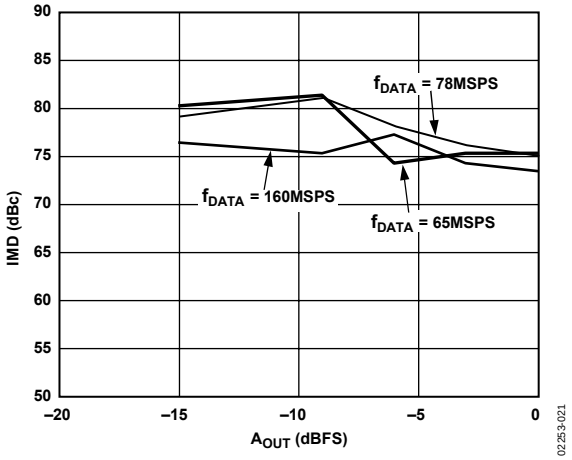


Figure 21. Third-Order IMD Products vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$

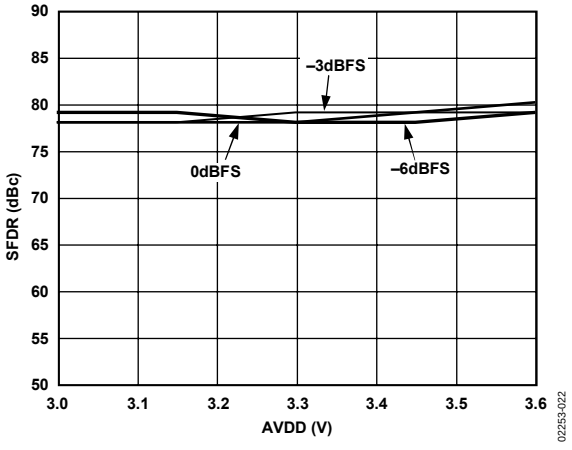


Figure 22. SFDR vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS

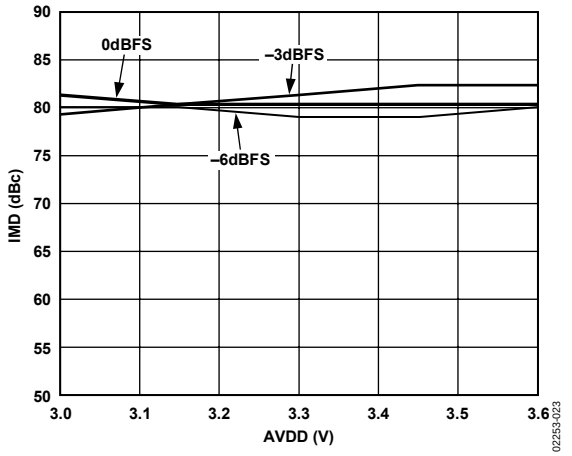


Figure 23. Third-Order IMD Products vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS

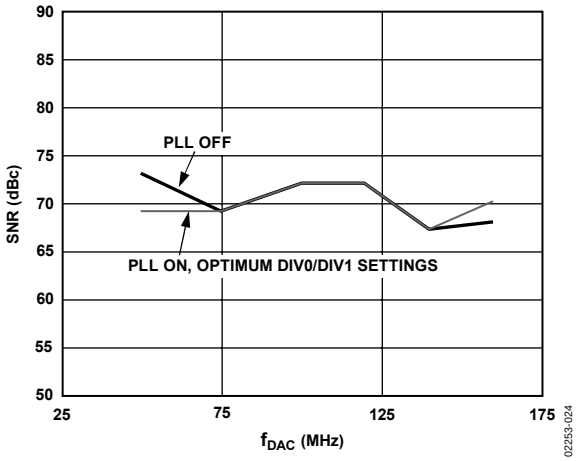


Figure 24. SNR vs. f_{DAC} @ f_{OUT} = 10 MHz

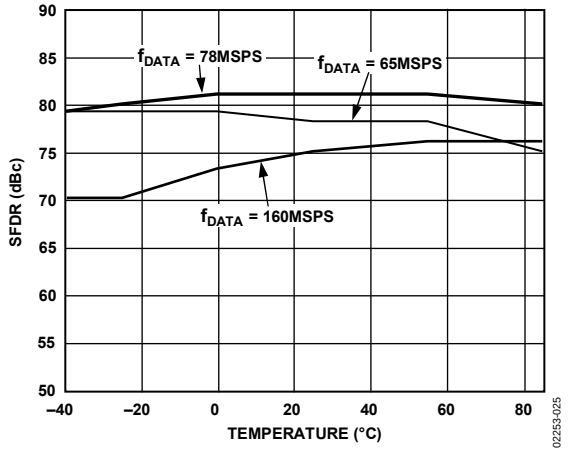


Figure 25. In-Band SFDR vs. Temperature @ $f_{OUT} = f_{DATA}/11$

THEORY OF OPERATION

FUNCTIONAL DESCRIPTION

Figure 26 shows a simplified block diagram of the AD9772A. The AD9772A is a complete 2× oversampling, 14-bit DAC that includes a 2× interpolation filter, a phase-locked loop (PLL) clock multiplier, and a 1.20 V band gap voltage reference. Although the AD9772A digital interface can support input data rates as high as 160 MSPS, its internal DAC can operate up to 400 MSPS, thus providing direct IF conversion capabilities. The 14-bit DAC provides two complementary current outputs whose full-scale current is determined by an external resistor. The AD9772A features a flexible, low jitter differential clock input, providing excellent noise rejection while accepting a sine wave input. An on-chip PLL clock multiplier produces all of the necessary synchronized clocks from an external reference clock source. Separate supply inputs are provided for each functional block to ensure optimum noise and distortion performance. A sleep mode is also included for power savings.

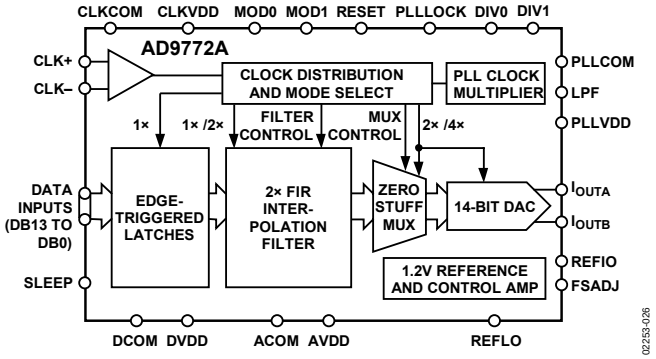


Figure 26. Simplified Functional Block Diagram

Preceding the 14-bit DAC is a 2× digital interpolation filter that can be configured for a low-pass (that is, baseband mode) or high-pass (that is, direct IF mode) response. The input data is latched into the edge-triggered input latches on the rising edge of the differential input clock, as shown in Figure 2, and then interpolated by a factor of 2 by the digital filter. For traditional baseband applications, the 2× interpolation filter has a low-pass response. For direct IF applications, the filter response can be converted into a high-pass response to extract the higher image. The output data of the 2× interpolation filter can update the 14-bit DAC directly or undergo a zero-stuffing process to increase the DAC update rate by another factor of 2. This action enhances the relative signal level and pass-band flatness of the higher frequency images.

DIGITAL MODES OF OPERATION

The AD9772A features four modes of operation controlled by the digital inputs, MOD0 and MOD1. MOD0 controls the 2× digital filter response (that is, low-pass or high-pass), and MOD1 controls the zero-stuffing option. The appropriate mode to select (see Table 9) depends on whether the application requires the reconstruction of a baseband or IF signal.

Table 9. Digital Modes

Digital Mode	MOD0	MOD1	Digital Filter	Zero-Stuffing
Baseband	0	0	Low	No
Baseband	0	1	Low	Yes
Direct IF	1	0	High	No
Direct IF	1	1	High	Yes

For applications requiring the highest dynamic range over a wide bandwidth, users should consider operating the AD9772A in a baseband mode. Although the zero-stuffing option can be used in this mode, the ratio of the signal to the image power will be reduced.

For applications requiring the synthesis of IF signals, users should consider operating the AD9772A in a direct IF mode. In this case, the zero-stuffing option should be considered when synthesizing and selecting IFs beyond the input data rate, f_{DATA}. If the reconstructed IF falls below f_{DATA}, the zero-stuffing option may or may not be beneficial. Note that the dynamic range (that is, SNR/SFDR) can be optimized by disabling the PLL clock multiplier (that is, by connecting PLLVDD to PLLCOM) and by using an external low-jitter clock source operating at the DAC update rate, f_{DAC}.

2× Interpolation Filter Description

The 2× interpolation filter is based on a 43-tap, half-band, symmetric FIR topology that can be configured for a low- or high-pass response, depending on the state of the MOD0 control input. The low-pass response is selected with MOD0 low, and the high-pass response is selected with MOD0 high. The low-pass frequency and the impulse response of the half-band interpolation filter are shown in Figure 4 and Figure 5, and the idealized filter coefficients are listed in Table 5. Note that the impulse response of a FIR filter is also represented by its idealized filter coefficients.

The 2× interpolation filter essentially multiplies the input data rate to the DAC by a factor of 2, relative to its original input data rate, while reducing the magnitude of the first image associated with the original input data rate occurring at $f_{DATA} - f_{FUNDAMENTAL}$. As a result of the 2× interpolation, the digital filter frequency response is uniquely defined over its Nyquist zone of dc to f_{DATA}, with mirror images occurring in adjacent Nyquist zones.

The benefits of an interpolation filter are clearly seen in Figure 27, which shows an example of the frequency and time domain representation of a discrete time sine wave signal before and after it is applied to the 2× digital interpolation filter in a low-pass configuration. Images of the sine wave signal appear around multiples of the input data rate (that is, f_{DATA}) of the DAC, as predicted by sampling theory. These undesirable images also appear at the output of a reconstruction DAC, although they are attenuated by the sin(x)/x roll-off response of the DAC.

In many band-limited applications, the images from the reconstruction process must be suppressed by an analog filter following the DAC. The complexity of this analog filter is typically determined by the proximity of the desired fundamental to the first image and the required amount of image suppression. Adding to the complexity of this analog filter is the requirement of compensating for the sin(x)/x response of the DAC.

Referring to Figure 27, the new first image associated with the higher data rate of the DAC after interpolation is pushed out further relative to the input signal, because it now occurs at 2× $f_{DATA} - f_{FUNDAMENTAL}$. The old first image associated with the lower DAC data rate before interpolation is suppressed by the digital filter. As a result, the transition band for the analog reconstruction filter is increased, thus reducing the complexity of the analog filter. Furthermore, the value of the sin(x)/x roll-off divided by the original input data pass band (that is, dc to $f_{DATA}/2$) is significantly reduced.

As previously mentioned, the 2× interpolation filter can be converted into a high-pass response, thus suppressing the fundamental while passing the original first image occurring at $f_{DATA} - f_{FUNDAMENTAL}$. Figure 28 shows the time and frequency representation for a high-pass response of a discrete time sine wave. This action can also be modeled as a half-wave digital mixing process in which the impulse response of the low-pass filter is digitally mixed with a square wave having a frequency of exactly $f_{DATA}/2$. Because the even coefficients have an integer value of 0 (see Table 5), this process simplifies into inverting the center coefficient of the low-pass filter (that is, inverting H(18)). Note that this also corresponds to inverting the peak of the impulse response shown in Figure 4. The resulting high-pass frequency response becomes the frequency inverted mirror image of the low-pass filter response shown in Figure 5.

Note that the new first image occurs at $f_{DATA} + f_{FUNDAMENTAL}$. A reduced transition region of $2 \times f_{FUNDAMENTAL}$ exists for image selection, thus mandating that the $f_{FUNDAMENTAL}$ be placed sufficiently high for practical filtering purposes in direct IF applications. In addition, the lower sideband images occurring at $f_{DATA} - f_{FUNDAMENTAL}$ and its multiples (that is, $N \times f_{DATA} - f_{FUNDAMENTAL}$) experience a frequency inversion while the upper sideband images occurring at $f_{DATA} + f_{FUNDAMENTAL}$ and its multiples (that is, $N \times f_{DATA} + f_{FUNDAMENTAL}$) do not.

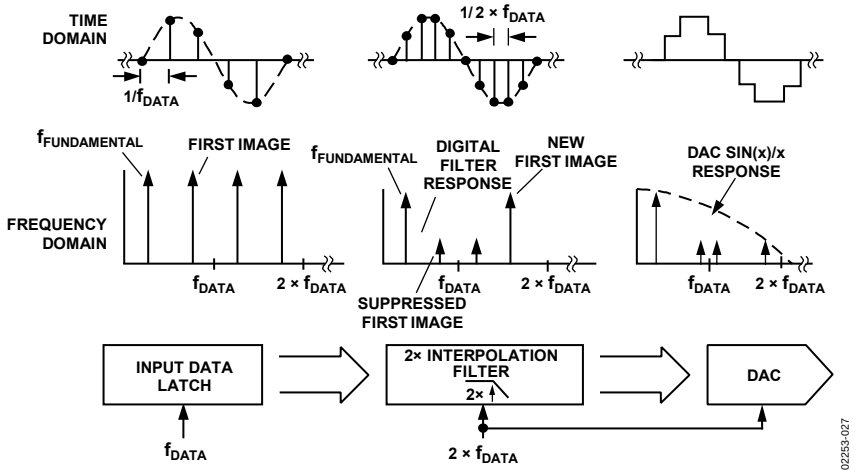


Figure 27. Time and Frequency Domain Example of Low-Pass 2× Digital Interpolation Filter

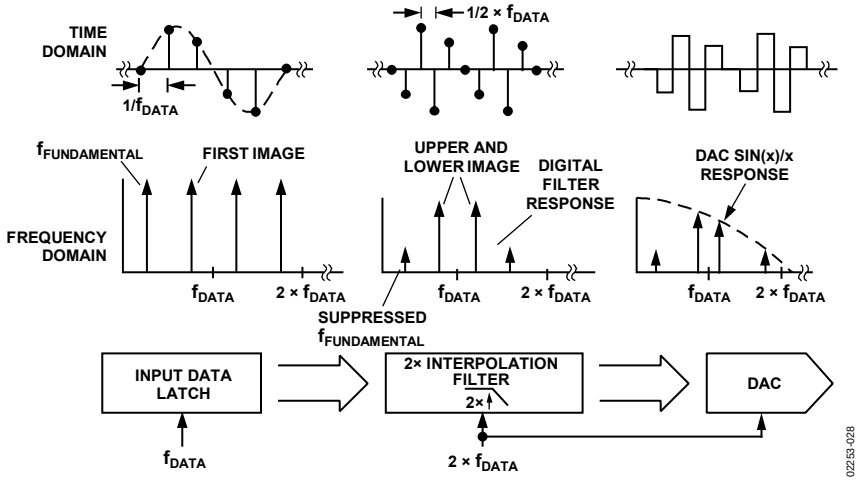


Figure 28. Time and Frequency Domain Example of High-Pass 2× Digital Interpolation Filter

Zero-Stuffing Option Description

As shown in Figure 29, a zero or null in the frequency response (after interpolation and DAC reconstruction) occurs at the final DAC update rate (that is, 2× f_{DATA}) due to the inherent sin(x)/x roll-off response of the DAC. In baseband applications, this roll-off in the frequency response may not be as problematic because much of the desired signal energy remains below $f_{DATA}/2$ and the amplitude variation is not as severe. However, in direct IF applications interested in extracting an image above $f_{DATA}/2$, this roll-off may be problematic due to the increased pass-band amplitude variation as well as the reduced signal level of the higher images.

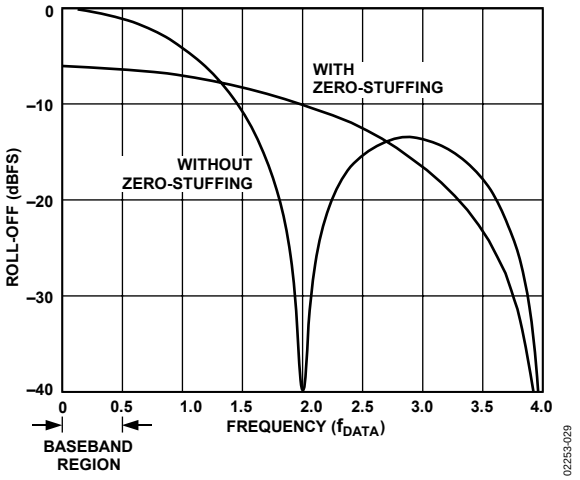


Figure 29. Effects of Zero-Stuffing on the Sin(x)/x Response of the DAC

For instance, if the digital data into the AD9772A represents a baseband signal centered around $f_{DATA}/4$ with a pass band of $f_{DATA}/10$, the reconstructed baseband signal output from the AD9772A experiences only a 0.18 dB amplitude variation over its pass band, with the first image occurring at $7/4 \times f_{DATA}$ and exhibiting 17 dB of attenuation relative to the fundamental. However, if the high-pass filter response is selected, the AD9772A produces pairs of images at $[(2N + 1) \times f_{DATA}] \pm f_{DATA}/4$, where N = 0, 1, and so on. Note that due to the sin(x)/x response of the DAC, only the lower or upper sideband images centered around f_{DATA} may be useful, although they are attenuated by −2.1 dB and −6.54 dB and have a pass-band amplitude roll-off of 0.6 dB and 1.3 dB, respectively.

To improve on the pass-band flatness of the desired image and/or to extract higher images (that is, $3 \times f_{DATA} \pm f_{FUNDAMENTAL}$), the zero-stuffing option should be employed by bringing the MOD1 pin high. This option increases the effective DAC update rate by another factor of 2 because a midscale sample (that is, 10 0000 0000 0000) is inserted after every data sample originating from the 2× interpolation filter. A digital multiplexer switching at a rate of $4 \times f_{DATA}$ between the interpolation filter output and a data register containing the midscale data sample is used as shown in Figure 28 to implement this option. Therefore, the DAC output is now forced to return to its differential midscale current value (that is, $I_{OUTA} - I_{OUTB}$ at 0 mA) after reconstructing each data sample from the digital filter.

The net effect is to increase the DAC update rate such that the zero in the sin(x)/x frequency response occurs at $4 \times f_{DATA}$ accompanied by a corresponding reduction in output power as shown in Figure 29. Note that if the high-pass response of the 2× interpolation filter is also selected, this action can be modeled as a quarter-wave digital mixing process, because this is equivalent to digitally mixing the impulse response of the low-pass filter with a square wave having a frequency of exactly f_{DATA} (that is, $f_{DAC}/4$).

It is important to realize that the zero-stuffing option by itself does not change the location of the images, but rather changes their signal level, amplitude flatness, and relative weighting. For instance, in the previous example, the pass-band amplitude flatness of the lower and upper sideband images centered around f_{DATA} are improved to 0.14 dB and 0.24 dB, respectively, while the signal level changes to −6.5 dBFS and −7.5 dBFS. The lower or upper sideband image centered around $3 \times f_{DATA}$ exhibit an amplitude flatness of 0.77 dB and 1.29 dB with signal levels of approximately −14.3 dBFS and −19.2 dBFS.

PLL CLOCK MULTIPLIER OPERATION

The phase-lock loop (PLL) clock multiplier circuitry, along with the clock distribution circuitry, can produce the necessary internally synchronized 1×, 2×, and 4× clocks for the edge-triggered latches, 2× interpolation filter, zero-stuffing multiplier, and DAC. Figure 30 shows a functional block diagram of the PLL clock multiplier, which consists of a phase detector, a charge pump, a voltage controlled oscillator (VCO), a prescaler, and digital control input/output. The clock distribution circuitry generates all the internal clocks for a given mode of operation. The charge pump and VCO are powered from PLLVDD, and the differential clock input buffer, phase detector, prescaler, and clock distribution circuitry are powered from CLKVDD. To ensure optimum phase noise performance from the PLL clock multiplier and clock distribution circuitry, PLLVDD and CLKVDD must originate from the same clean analog supply.

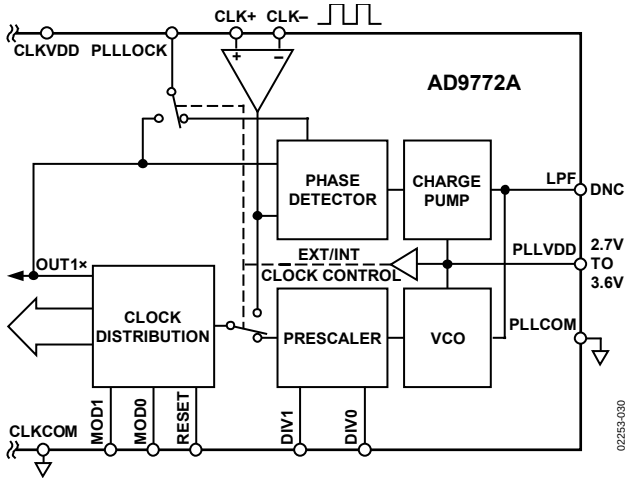


Figure 30. Clock Multiplier with PLL Clock Multiplier Enabled

The PLL clock multiplier has two modes of operation. It can be enabled for less demanding applications, providing a reference clock meeting the minimum specified input data rate of 6 MSPS. Alternatively, it can be disabled for applications below this data rate or for applications requiring higher phase noise performance. In this case, a reference clock must be provided at twice the input data rate (that is, $2 \times f_{DATA}$) without the zero-stuffing option selected or at four times the input data rate (that is, $4 \times f_{DATA}$) with the zero-stuffing option selected. Note that multiple AD9772A devices can be synchronized in either mode if driven by the same reference clock because the PLL clock multiplier, when enabled, ensures synchronization. RESET can be used for synchronization if the PLL clock multiplier is disabled.

Figure 30 shows the proper configuration used to enable the PLL clock multiplier. In this case, the external clock source is applied to CLK+ (and/or CLK−) and the PLL clock multiplier is fully enabled by connecting PLLVDD to CLKVDD.

The settling/acquisition time characteristics of the PLL are also dependent on the divide-by-N ratio as well as the input data rate. In general, the acquisition time increases with increasing data rate (for fixed divide-by-N ratio) or with an increasing divide-by-N ratio (for fixed input data rate).

Because the VCO can operate over a 96 MHz to 400 MHz range, the prescaler divide-by-ratio following the VCO must be set according to Table 10 for a given input data rate (that is, f_{DATA}) to ensure optimum phase noise and successful locking. In general, the best phase noise performance for any prescaler setting is achieved with the VCO operating near its maximum output frequency of 400 MHz. Note that the divide-by-N ratio also depends on whether the zero-stuffing option is enabled because this option requires the DAC to operate at 4× the input data rate. The divide-by-N ratio is set by DIV1 and DIV0.

With the PLL clock multiplier enabled, PLLLOCK serves as an active high control output that can be monitored upon system power-up to indicate that the PLL is successfully locked to the input clock. Note that when the PLL clock multiplier is not locked, PLLLOCK toggles between logic high and low in an asynchronous manner until locking is finally achieved. As a result, it is recommended that PLLLOCK, if monitored, be sampled several times to detect proper locking 100 ms after power-up.

Table 10. Recommended Prescaler Divide-by-N Ratio Settings

f_{DATA} (MSPS)	MOD1	DIV1	DIV0	Divide-by-N Ratio
48 to 160	0	0	0	1
24 to 100	0	0	1	2
12 to 50	0	1	0	4
6 to 25	0	1	1	8
24 to 100	1	0	0	1
12 to 50	1	0	1	2
6 to 25	1	1	0	4
3 to 12.5	1	1	1	8

As previously stated, applications requiring input data rates below 6 MSPS must disable the PLL clock multiplier and provide an external reference clock. However, for applications already containing a low phase noise (that is, low jitter) reference clock that is twice (or four times) the input data rate, users should consider disabling the PLL clock multiplier to achieve the best SNR performance from the AD9772A. Note that the SFDR performance and wideband noise performance of the AD9772A remain unaffected with or without the PLL clock multiplier enabled.

The effects of phase noise on the AD9772A SNR performance become more noticeable at higher reconstructed output frequencies and signal levels. Figure 31 compares the phase noise of a full-scale sine wave at exactly $f_{DATA}/4$ for different data rates (and therefore carrier frequencies) with the optimum DIV1 and DIV0 settings. The effects of phase noise, and its effect on a signal's CNR performance, become even more evident at higher IF frequencies, as shown in Figure 32. In both instances, it is the narrow-band phase noise that limits the CNR performance.

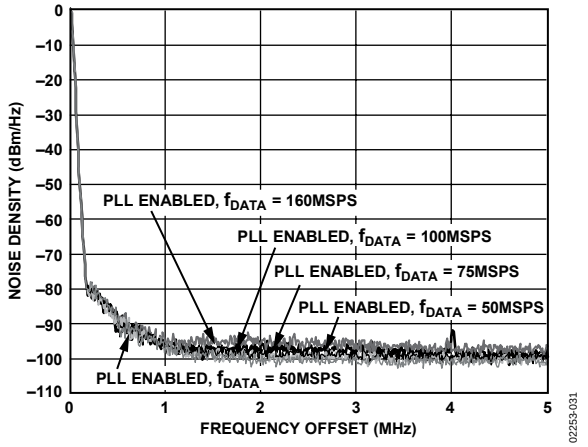


Figure 31. Phase Noise of PLL Clock Multiplier with a Full-Scale Sine Wave at Exactly $f_{OUT} = f_{DATA}/4$ for Different f_{DATA} Settings with Optimum DIV0/DIV1 Settings Using the Rohde & Schwarz FSEA30, RBW = 30 kHz

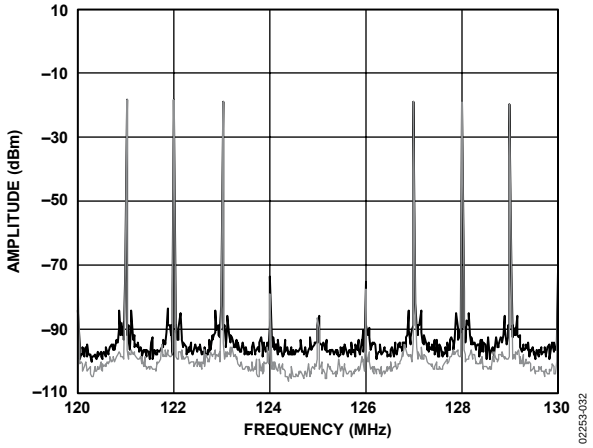


Figure 32. Direct IF Mode Reveals Phase Noise Degradation with and Without PLL Clock Multiplier (IF = 125 MHz and f_{DATA} = 100 MSPS)

To disable the PLL clock multiplier, connect PLLVDD to PLLCOM as shown in Figure 33. LPF can then remain open because this portion of the PLL circuitry is disabled. The

differential clock input should be driven with a reference clock that is twice the data input rate in baseband applications, or that is four times the data input rate in direct IF applications in which the quarter-wave mixing option is employed (that is, MOD1 and MOD0 active high). The clock distribution circuitry remains enabled, providing a 1× internal clock at PLLLOCK. Digital input data is latched into the AD9772A on every other rising edge of the differential clock input. The rising edge that corresponds to the input latch immediately precedes the rising edge of the 1× clock at PLLLOCK. Adequate setup and hold times for the input data, as shown in Figure 3, should be allowed. Note that enough delay is present between CLK+/CLK– and the data input latch to cause the minimum setup time for input data to be negative. This is noted in the Digital Filter Specifications section. PLLLOCK contains a relatively weak driver output, with its output delay (t_{OD}) sensitive to output capacitance loading. Therefore, PLLLOCK should be buffered for fanouts greater than 1 and/or for load capacitance greater than 10 pF. If a data timing issue exists between the AD9772A and its external driver device, the 1× clock appearing at PLLLOCK can be inverted via an external gate to ensure proper setup and hold time.

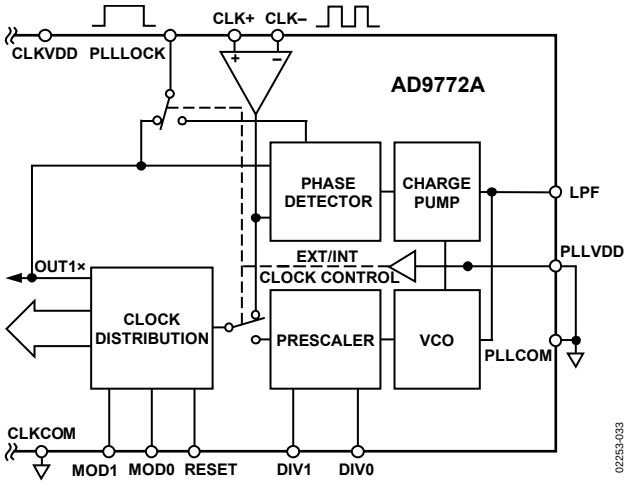


Figure 33. Clock Multiplier with PLL Clock Multiplier Disabled

SYNCHRONIZATION OF CLOCK/DATA USING RESET WITH PLL DISABLED

The relationship between the internal and external clocks in this mode is shown in Figure 34. A clock at the output update data rate (2× the input data rate) must be applied to the CLK+ and CLK– inputs. Internal dividers create the internal 1× clock necessary for the input latches. With the PLL disabled, a delayed version of the 1× clock is present at the PLLLOCK pin. The DAC latch is updated on the rising edge of the external 2× clock that corresponds to the rising edge of the 1× clock. Updates to the input data should be synchronized to this rising edge as shown in Figure 34. To ensure this synchronization, a Logic 1 should be momentarily applied to the RESET pin on power-up before CLK+/CLK– is applied. Momentarily applying a Logic 1 to the RESET pin brings the 1× clock at PLLLOCK to a Logic 1. On the next rising edge of the 2× clock, the 1× clock goes to Logic 0. The following rising edge of the 2× clock causes the 1× clock to go to Logic 1 again and updates the data in both of the input latches.

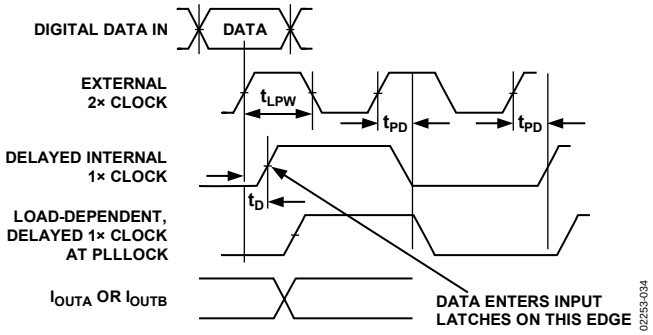


Figure 34. Internal Timing of AD9772A with PLL Disabled

Figure 35 and Figure 36 illustrate the details of the RESET function timing. The RESET pin going from a high to a low logic level enables the 1× clock output generated by the PLLLOCK pin. If RESET goes low before the rising edge of the 2× clock as shown in Figure 35, PLLLOCK goes high on the following edge of the 2× clock. If RESET goes from a high to a low logic level 600 ps or later following the rising edge of the 2× clock, as shown in Figure 36, there is a delay of one 2× clock cycle before PLLLOCK goes high. In either case, as long as RESET remains low, PLLLOCK changes state on every rising edge of the 2× clock. As previously stated, the rising edge of the 2× clock immediately preceding the rising edge of PLLLOCK latches data into the AD9772A input latches.

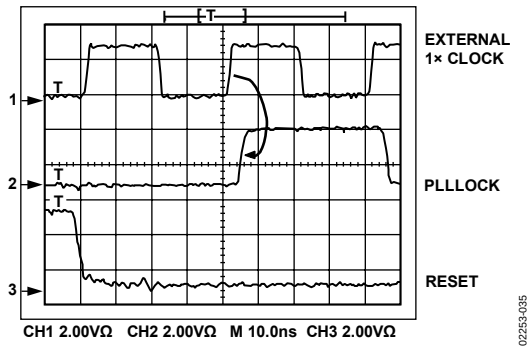


Figure 35. RESET Timing with PLL Disabled

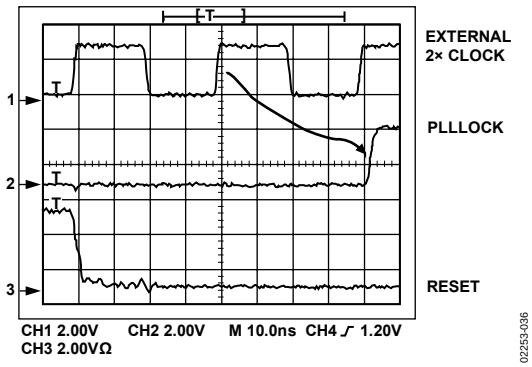


Figure 36. RESET Timing with PLL Disabled and Insufficient Setup Time

DAC OPERATION

The 14-bit DAC, along with the 1.2 V reference and reference control amplifier, is shown in Figure 37. The DAC consists of a large PMOS current source array capable of providing up to 20 mA of full-scale current, I_{OUTFS}. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose values are 1/16th of an MSB current source. The remaining LSBs are binary-weighted fractions of the middle bits' current sources. All of these current sources are switched to one of the two output nodes (that is, I_{OUTA} or I_{OUTB}) via the PMOS differential current switches. Implementing the middle and lower bits with current sources instead of an R-2R ladder enhances its dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of the DAC.

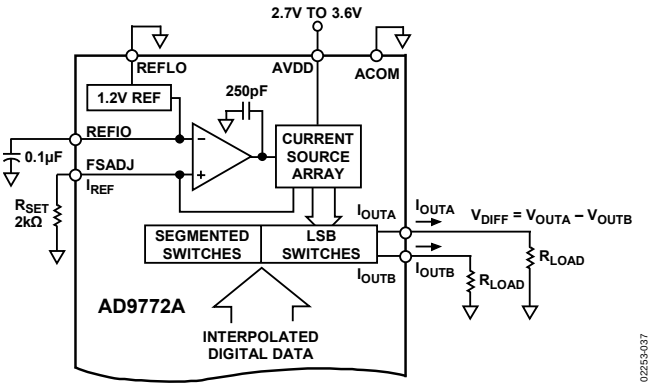


Figure 37. Block Diagram of Internal DAC, 1.2 V Reference, and Reference Control Circuits

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, as shown in Figure 37. R_{SET}, in combination with both the reference control amplifier and voltage reference, REFIO, sets the reference current, I_{REF}, which is mirrored to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is exactly 32 times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9772A provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} provides a near full-scale current output, I_{OUTFS}, when all bits are high (that is, DAC CODE = 16,383), whereas I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as

$$I_{OUTA} = (DAC\ CODE/16{,}384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16{,}383 - DAC\ CODE)/16{,}384 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16,383 (that is, decimal representation).

As previously mentioned, I_{OUTFS} is a function of the reference current (I_{REF}), which is nominally set by a reference voltage (V_{REFIO}) and an external resistor (R_{SET}). It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where:

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note that R_{LOAD} can represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB}, as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range of 1.25 V to prevent signal compression. To maintain optimum distortion and linearity performance, the maximum voltages at V_{OUTA} and V_{OUTB} should not exceed ±500 mV p-p.

The differential voltage, V_{DIFF}, appearing across I_{OUTA} and I_{OUTB} is

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB}, and I_{REF}, V_{DIFF} can be expressed as

$$V_{DIFF} = [(2\ DAC\ CODE - 16{,}383)/16{,}384] \times (32 \times R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

The last two equations highlight some of the advantages of operating the AD9772A differentially. First, the differential operation helps cancel common-mode error sources, such as noise, distortion, and dc offsets, associated with I_{OUTA} and I_{OUTB}. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single- ended voltage output (that is, V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9772A can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship, as shown in Equation 8.

REFERENCE OPERATION

The AD9772A contains an internal 1.20 V band gap reference that can easily be disabled and overridden by an external reference. REFIO serves as either an output or input, depending on whether the internal or external reference is selected. If REFLO is tied to ACOM, as shown in Figure 38, the internal reference is activated, and REFIO provides a 1.20 V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. If any additional loading is required, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA.

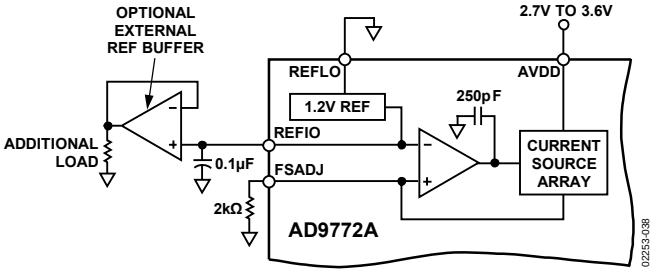


Figure 38. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external 1.2 V reference, such as the AD1580, can be applied to REFIO as shown in Figure 39. The external reference can provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage to improve gain control. Note that the 0.1 µF compensation capacitor is not required because the internal reference is disabled and the high input impedance of REFIO minimizes any loading of the external reference.

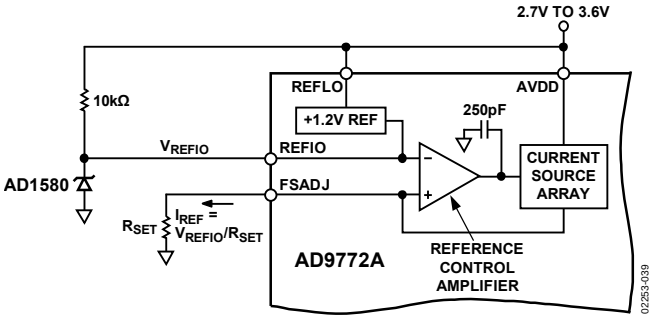


Figure 39. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9772A also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 39, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9772A DAC, which is proportional to I_{OUTFS} (see the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

I_{REF} can be controlled using the single-supply circuit shown in Figure 40 for a fixed R_{SET}. In this example, the internal reference is disabled, and the voltage of REFIO is varied over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply DAC or digital potentiometer, thus allowing I_{REF} to be digitally controlled for a fixed R_{SET}. This particular example shows the AD5220, an 8-bit serial input digital potentiometer, along with the AD1580 voltage reference. Note that because the input impedance of REFIO does interact with and load the digital potentiometer wiper to create a slight nonlinearity in the programmable voltage divider ratio, a digital potentiometer with 10 kΩ or less resistance is recommended.

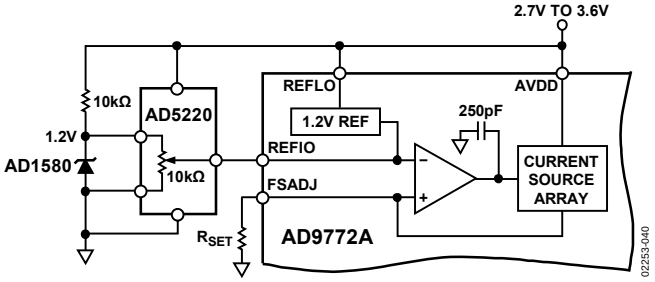


Figure 40. Single-Supply Gain Control Circuit

ANALOG OUTPUTS

The AD9772A produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which can be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section, by using Equation 5 through Equation 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 41 shows the equivalent analog output circuit of the AD9772A, which consists of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches and is typically 200 kΩ in parallel with 3 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (that is, V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, AVDD, and full-scale current, I_{OUTFS}. Although the signal dependency of the output impedance can be a source of dc nonlinearity and ac linearity (that is, distortion), its effects can be limited if certain precautions are taken.

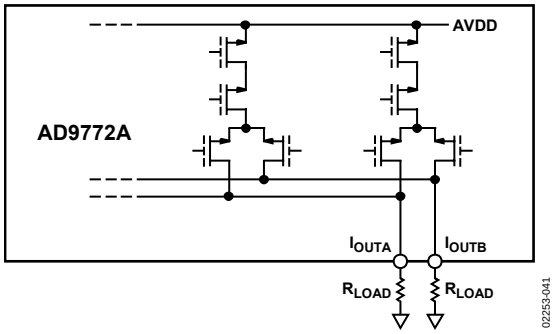


Figure 41. Equivalent Analog Output Circuit

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range. The negative output compliance threshold of −1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown

of the output stage and affect the reliability of the AD9772A. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. Operation beyond the positive compliance range induces clipping of the output signal, which severely degrades the AD9772A linearity and distortion performance.

Operating the AD9772A with reduced voltage output swings at I_{OUTA} and I_{OUTB} in a differential or single-ended output configuration reduces the signal dependency of its output impedance, thus enhancing distortion performance. Although the voltage compliance range of I_{OUTA} and I_{OUTB} extends from −1.0 V to +1.25 V, optimum distortion performance is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed approximately 0.5 V. Using a properly selected transformer with a grounded center tap allows the AD9772A to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at I_{OUTA} and I_{OUTB}. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to the Output Configurations section for examples of various output configurations.

The most significant improvement in the AD9772A distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed waveform's frequency content increases and/or its amplitude decreases. The distortion and noise performance of the AD9772A is also dependent on the full-scale current setting, I_{OUTFS}. Although I_{OUTFS} can be set between 2 mA and 20 mA, selecting an I_{OUTFS} of 20 mA provides the best distortion and noise performance.

In summary, the AD9772A achieves the optimum distortion and noise performance under the following conditions:

- Positive voltage swing at I_{OUTA} and I_{OUTB} limited to 0.5 V
- Differential operation
- I_{OUTFS} set to 20 mA
- PLL clock multiplier disabled

Note that the majority of the ac characterization curves for the AD9772A are performed with these operating conditions.

DIGITAL INPUTS/OUTPUTS

The AD9772A consists of several digital input pins used for data, clock, and control purposes. It also contains a single digital output pin, PLLLOCK, which is used to monitor the status of the internal PLL clock multiplier or provide a 1× clock output. The 14-bit parallel data inputs follow standard positive binary coding, where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch and is designed to support an input data rate as high as 160 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width, as shown in Figure 2 and Figure 3. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met. The digital inputs (excluding CLK+ and CLK–) are CMOS compatible with its logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (that is, DVDD or CLKVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9772A is capable of operating over a digital supply range of 3.1 V to 3.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers $V_{OH(MAX)}$. Although a DVDD of 3.3 V typically ensures proper compatibility with most TTL logic families, series 200 Ω resistors are recommended between the TTL logic driver and digital inputs to limit the peak current through the ESD protection diodes if $V_{OH(MAX)}$ exceeds DVDD by more than 300 mV. Figure 42 shows the equivalent digital input circuit for the data and control inputs.

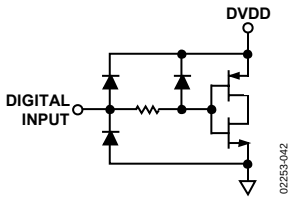


Figure 42. Equivalent Digital Input

The AD9772A features a flexible differential clock input operating from separate supplies (that is, CLKVDD, CLKCOM) to achieve optimum jitter performance. The two clock inputs, CLK+ and CLK–, can be driven from a single-ended or differential clock source. For single-ended operation, CLK+ should be driven by a single-ended logic source, and CLK– should be set to the logic source's threshold voltage via a resistor divider/capacitor network referenced to CLKVDD as shown in Figure 43. For differential operation, both CLK+ and CLK– should be biased to CLKVDD/2 via a resistor divider network as shown in Figure 44. An RF transformer as shown in Figure 7 can also be used to convert a single-ended clock input to a differential clock input.

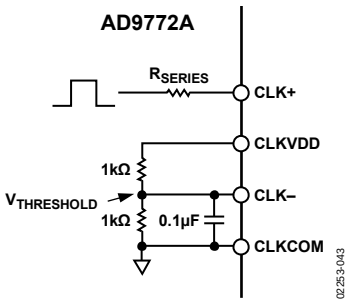


Figure 43. Single-Ended Clock Interface

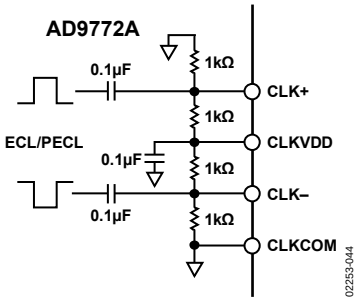


Figure 44. Differential Clock Interface

The quality of the clock and data input signals is important in achieving the optimum performance. The external clock driver circuitry should provide the AD9772A with a low jitter clock input, which meets the minimum/maximum logic levels while providing fast edges. Although fast clock edges help minimize jitter manifesting as phase noise on a reconstructed waveform, the high gain-bandwidth product of the AD9772A differential comparator can tolerate sine wave inputs as low as 0.5 V p-p, with minimal degradation in its output noise floor.

Digital signal paths should be kept short, and run lengths should match to avoid propagation delay mismatch. The insertion of a low value resistor network (that is, 50 Ω to 200 Ω) between the AD9772A digital inputs and driver outputs may be helpful in reducing overshooting and ringing at the digital inputs that contribute to data feedthrough.

SLEEP MODE OPERATION

The AD9772A has a sleep function that turns off the output current and reduces the analog supply current to less than 6 mA over the specified supply range of 3.1 V to 3.5 V. This mode can be activated by applying a Logic Level 1 to the SLEEP pin. The AD9772A takes less than 50 ns to power down and then approximately 15 µs to power up.

POWER DISSIPATION

The power dissipation, P_D, of the AD9772A is dependent on several factors, including

- The power supply voltages (AVDD, PLLVDD, CLKVDD, and DVDD)
- The full-scale current output (I_{OUTFS})
- The update rate (f_{DATA})
- The reconstructed digital input waveform

The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} and is not sensitive to f_{DATA}.

Conversely, I_{DVDD} is dependent on both the digital input waveform and f_{DATA}. Figure 45 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{DATA}) for various update rates with DVDD = 3.3 V. The supply current from CLKVDD and PLLVDD is relatively insensitive to the digital input waveform but directly proportional to the update rate, as shown in Figure 46.

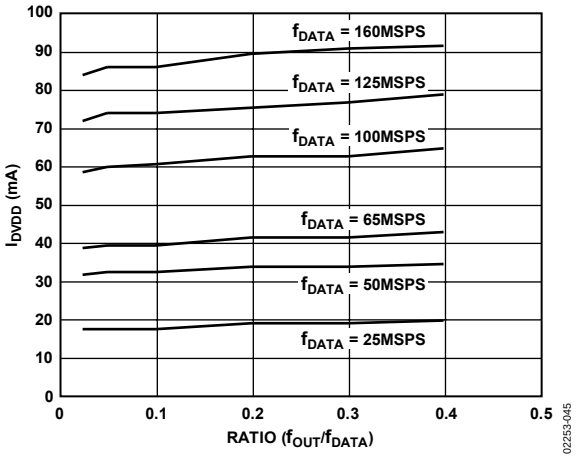


Figure 45. I_{DVDD} vs. Ratio @ DVDD = 3.3 V

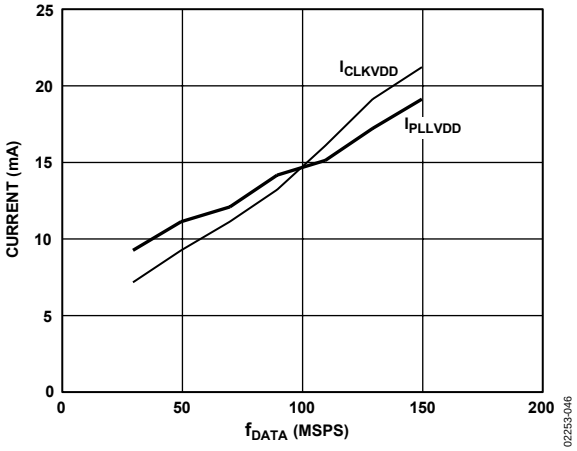


Figure 46. I_{PLLVDD} and I_{CLKVDD} vs. f_{DATA}

APPLYING THE AD9772A

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9772A. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA for optimum performance. For applications requiring the optimum dynamic performance, a differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage results if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground-referred output voltage. Alternatively, an amplifier can be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity because I_{OUTA} or I_{OUTB} is maintained at a virtual ground.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used as shown in Figure 47 to perform a differential-to-single-ended signal conversion. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the pass band of the transformer. An RF transformer such as the Mini-Circuits® T1-1T provides excellent rejection of common-mode distortion (that is, even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios can also be used for impedance matching purposes. Note that the transformer provides ac coupling only, and its linearity performance degrades at the low end of its frequency range due to core saturation.

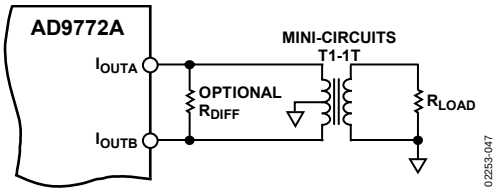


Figure 47. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (that is, V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9772A. A differential resistor, R_{DIFF}, can be inserted into applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination, resulting in a low voltage standing wave ratio (VSWR). Note that approximately half the signal power is dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 48. The AD9772A is configured with two equal load resistors, R_{LOAD}, each of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the distortion performance of the op amp by preventing the DAC's high slewing output from overloading the op amp input.

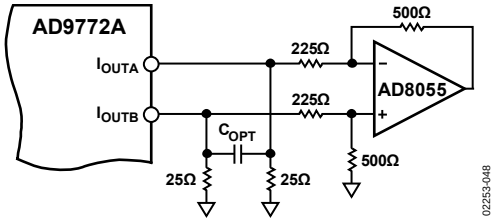


Figure 48. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8055 is configured to provide some additional signal gain. The op amp must operate from a dual supply because its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9772A while meeting other system-level objectives (such as cost and power) should be selected. The op amp's differential gain, gain-setting resistor values, and full-scale output swing capabilities should be considered when optimizing this circuit.

The differential circuit shown in Figure 49 provides the necessary level shifting required in a single-supply system. In this case, AVDD, the positive analog supply for both the AD9772A and the op amp, is also used to level-shift the differential output of the AD9772A to midsupply (that is, AVDD/2). The AD8057 is a suitable op amp for this application.

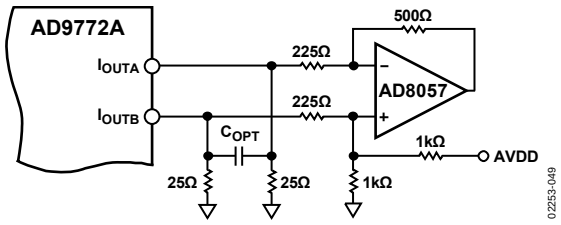


Figure 49. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED, UNBUFFERED VOLTAGE OUTPUT

Figure 50 shows the AD9772A configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable because the nominal full-scale current, I_{OUTFS},

of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA}. The unused output (I_{OUTB}) should be connected directly to ACOM. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL), as discussed in the Analog Outputs section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

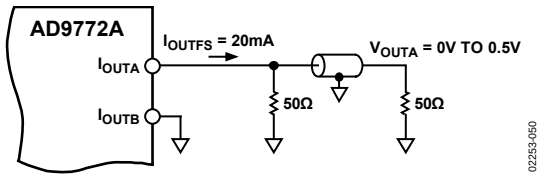


Figure 50. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT

Figure 51 shows a single-ended, buffered output configuration in which the op amp U1 performs an I-V conversion on the AD9772A output current. U1 maintains I_{OUTA} (or I_{OUTB}) at virtual ground, thus minimizing the nonlinear output impedance effect on the INL performance of the DAC, as discussed in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates is often limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage, and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result in a reduced I_{OUTFS} because the signal current that U1 will be required to sink is subsequently reduced.

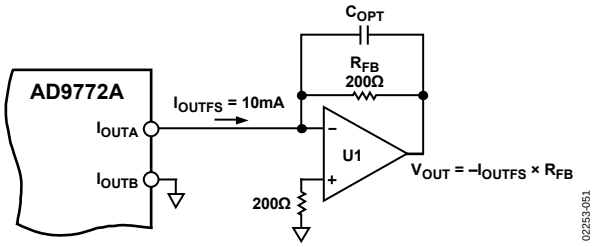


Figure 51. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

The AD9772A contains the following power supply inputs: AVDD, DVDD, CLKVDD, and PLLVDD. The AD9772A is specified to operate over a 3.1 V to 3.5 V supply range, thus accommodating a 3.3 V power supply with up to ±6% regulation. However, the following two conditions must be adhered to when selecting power supply sources for AVDD, DVDD, CLKVDD, and PLLVDD:

- PLLVDD = CLKVDD = 3.1 V to 3.5 V when the PLL clock multiplier is enabled (otherwise, PLLVDD = PLLCOM)
- DVDD = CLKVDD ± 0.30 V

To meet the first condition, PLLVDD must be driven by the same power source as CLKVDD, with each supply input independently decoupled using a 0.1 µF capacitor connected to its respective ground. To meet the second condition, CLKVDD can share the same power supply source as DVDD by using the decoupling network shown in Figure 52 to isolate digital noise from the sensitive CLKVDD (and PLLVDD) supply. Alternatively, separate precision voltage regulators can be used to ensure that the second condition is met.

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing, and supply bypassing and grounding. Figure 60 to Figure 67 illustrate the recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9772A evaluation board.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9772A features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. AVDD, CLKVDD, and PLLVDD must be powered from a clean analog supply and decoupled to their respective analog common (that is, ACOM, CLKCOM, and PLLCOM) as close to the chip as physically possible. Similarly, the digital supplies (DVDD) should be decoupled to DCOM.

For applications requiring a single 3.3 V supply for the analog, digital, and phase-lock loop supplies, a clean AVDD and/or CLKVDD can be generated using the circuit shown in Figure 52. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR-type electrolytic and tantalum capacitors.

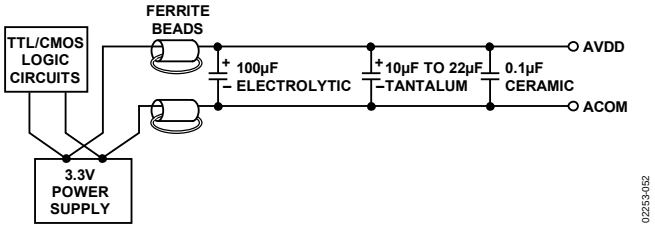


Figure 52. Differential LC Filter for 3.3 V

Maintaining low noise on power supplies and ground is critical for achieving optimum results from the AD9772A. If properly implemented, ground planes can perform a host of functions on high speed circuit boards, such as bypassing and shielding current transport. In mixed-signal designs, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference, and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path ⅛ to ¼ inch wide underneath or within ½ inch of the DAC to maintain

optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC. On the analog side, this includes the DAC output signal, the reference signal, and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part and allowing some capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnections to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct, and as physically close to the package as possible to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, use of strip line techniques with proper termination resistors should be considered. The necessity and value of these resistors depends on the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed-signal printed circuit boards, refer to the AN-333 Application Note.

APPLICATIONS INFORMATION

MULTICARRIER

The AD9772A's wide dynamic range performance makes it well suited for next-generation base station applications in which it reconstructs multiple modulated carriers over a designated frequency band. Cellular multicarrier and multimode radios are often referred to as software radios because the carrier tuning and modulation scheme is software programmable and performed digitally. The AD9772A is the recommended TxDAC® in the Analog Devices, Inc., SoftCell® chipset, which comprises the AD6622 (a quadrature digital upconverter IC), the AD6624 (an Rx digital downconverter IC that acts as a companion to the AD6622), and the AD6644 (a 14-bit, 65 MSPS ADC). Figure 53 shows a generic software radio Tx signal chain using the AD9772A and AD6622.

Figure 54 shows a spectral plot of the AD9772A operating at 64.54 MSPS, reconstructing eight IS-136-modulated carriers spread over a 25 MHz band. In this example, the AD9772A exhibits an SFDR performance of 74 dBc and a carrier-to-noise ratio (CNR) of 73 dB. Figure 55 shows a spectral plot of the AD9772A operating at 52 MSPS, reconstructing four equal GSM-modulated carriers spread over a 15 MHz band. The SFDR and CNR (in 100 kHz BW) are measured to be 76 dBc and 83.4 dB, respectively, and have a channel power of −13.5 dBFS. The test vectors were generated using the Rohde & Schwarz WinIQSIM software.

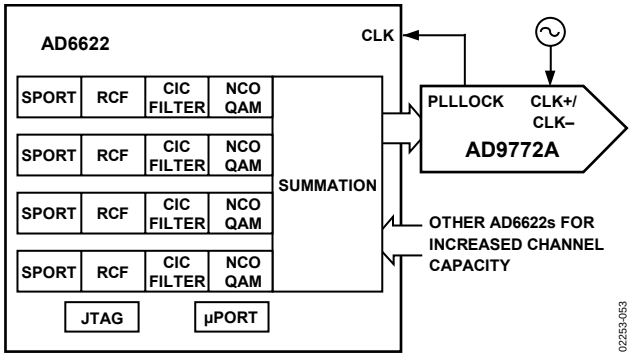


Figure 53. Generic Multicarrier Signal Chain Using the AD6622 and AD9772A

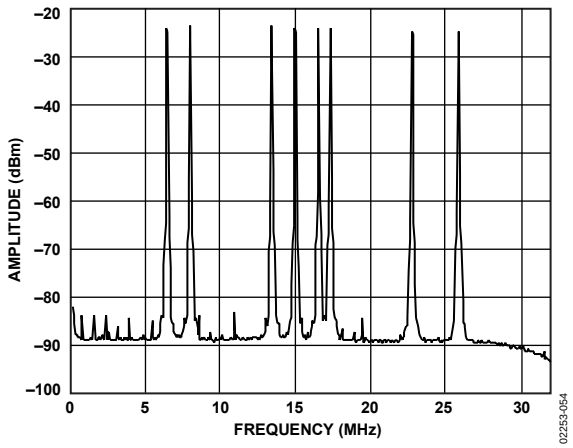


Figure 54. Spectral Plot of AD9772A Reconstructing Eight IS-136-Modulated Carriers @ f_{DATA} = 64.54 MSPS, PLLVDD = 0

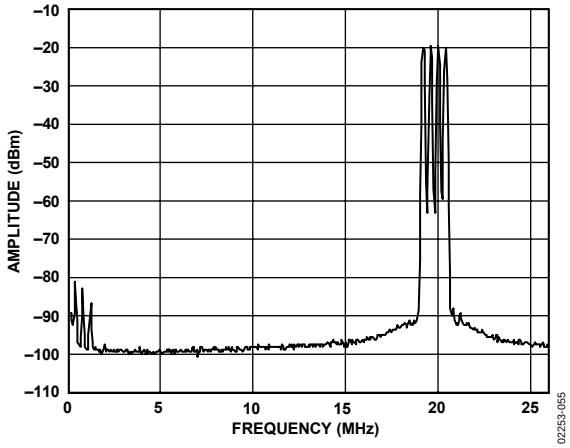


Figure 55. Spectral Plot of AD9772A Reconstructing Four GSM-Modulated Carriers @ f_{DATA} = 52 MSPS, PLLVDD = 0

Although the above IS-136 and GSM spectral plots are representative of the AD9772A's performance for a set of test conditions, the following recommendations are offered to maximize the performance and system integration of the AD9772A into multicarrier applications:

1. To achieve the highest possible CNR, the PLL clock multiplier should be disabled (that is, PLLVDD to PLLCOM) and the AD9772A clock input should be driven with a low jitter, low phase noise clock source at twice the input data rate. In this case, the divide-by-2 clock appearing at PLLLOCK should serve as the master clock for the digital upconverter IC(s), such as the AD6622. PLLLOCK should be limited to a fanout of 1.
2. The AD9772A achieves its optimum noise and distortion performance when the device is configured for baseband operation and the differential output and full-scale current, I_{OUTFS}, are set to approximately 20 mA.
3. Although the frequency roll-off of the 2× interpolation filter provides a maximum reconstruction bandwidth of 0.422 × f_{DATA}, the optimum adjacent image rejection (due to the interpolation process) can be achieved (that is, > 73 dBc) if the maximum channel assignment is kept below 0.400 × f_{DATA}.
4. To simplify the filter requirements (that is, mixer image and LO rejection) of the subsequent IF stages, it is often advantageous to offset the frequency band from dc to relax the transition band requirements of the IF filter.
5. Oversampling the frequency band often results in improved SFDR and CNR performance. This implies that the data input rate to the AD9772A is greater than $f_{PASSBAND}$/0.4 Hz, where $f_{PASSBAND}$ is the maximum bandwidth that the AD9772A is required to reconstruct and place carriers. The improved noise performance results in a reduction in the TxDAC's noise spectral density due to the added process gain realized with oversampling, and higher oversampling ratios provide greater flexibility in the frequency planning.

BASEBAND SINGLE-CARRIER APPLICATIONS

The AD9772A is also well suited for wideband single-carrier applications, such as WCDMA and multilevel quadrature amplitude modulation (QAM), whose modulation scheme requires wide dynamic range from the reconstruction DAC to achieve the out-of-band spectral mask as well as the in-band CNR performance. Many of these applications strategically place the carrier frequency at one quarter of the DAC's input data rate (that is, $f_{DATA}/4$) to simplify the digital modulator design. Because this constitutes the first fixed IF frequency, the frequency tuning is accomplished at a later IF stage. To enhance the modulation accuracy and reduce the shape factor of the second IF SAW filter, many applications specify that the pass band of the IF SAW filter be greater than the channel bandwidth; however, the trade-off is that this requires that the TxDAC meet the spectral mask requirements of the application within the extended pass band of the second IF, which may include two or more adjacent channels.

Figure 56 shows a spectral plot of the AD9772A reconstructing a test vector similar to those encountered in WCDMA applications. However, WCDMA applications prescribe a root raised cosine filter with an alpha = 0.22, which limits the theoretical ACPR of the TxDAC to about 70 dB, whereas the test vector represents white noise that has been band-limited by a brick wall band-pass filter with a pass band for which the maximum ACPR performance is theoretically 83 dB and the peak-to-rms ratio is 12.4 dB. As Figure 56 reveals, the AD9772A is capable of approximately 78 dB ACPR performance when one accounts for the additive noise/distortion contributed by the Rohde & Schwarz FSEA30 spectrum analyzer.

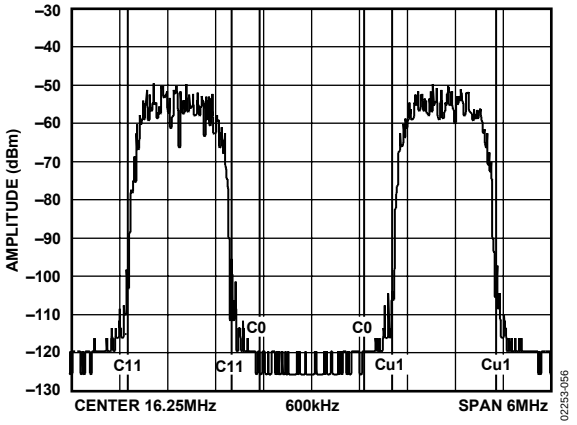


Figure 56. AD9772A Achieves 78 dB ACPR Performance Reconstructing a WCDMA-Like Test Vector with f_{DATA} = 65.536 MSPS and PLLVDD = 0

DIRECT IF

As discussed in the Digital Modes of Operation section, the AD9772A can be configured to transform digital data representing baseband signals into IF signals appearing at odd multiples of the input data rate (that is, $N \times f_{DATA}$, where N = 1, 3, and so on). This is accomplished by configuring the MOD1 and MOD0 digital inputs high. Note that the maximum DAC update rate of 400 MSPS limits the data input rate in this mode to 100 MSPS when the zero-stuffing operation is enabled (that is, when MOD1 is high). Applications requiring higher IFs (that is, 140 MHz) using higher data rates should disable the zero-stuffing operation. In addition, to minimize the effects of the PLL clock multipliers phase noise as shown in Figure 31, an external low jitter/phase noise clock source equal to $4 \times f_{DATA}$ is recommended.

Figure 57 shows the actual output spectrum of the AD9772A reconstructing a 16-QAM test vector with a symbol rate of 5 MSPS. The particular test vector was centered at $f_{DATA}/4$ with f_{DATA} = 100 MSPS and f_{DAC} = 400 MHz. For many applications, the pair of images appearing around f_{DATA} will be more attractive because this pair has the flattest pass band and highest signal power. Higher frequency images can also be used, but such images will have reduced pass-band flatness, dynamic range, and signal power, thus reducing the CNR and ACP performance. Figure 58 shows a dual-tone SFDR amplitude sweep at the various IF images with f_{DATA} = 100 MSPS, f_{DAC} = 400 MHz, and the two tones centered around $f_{DATA}/4$. Note that because an IF filter is assumed to precede the AD9772A, the SFDR was measured over a 25 MHz window around the images occurring at 75 MHz, 125 MHz, 275 MHz, and 325 MHz.

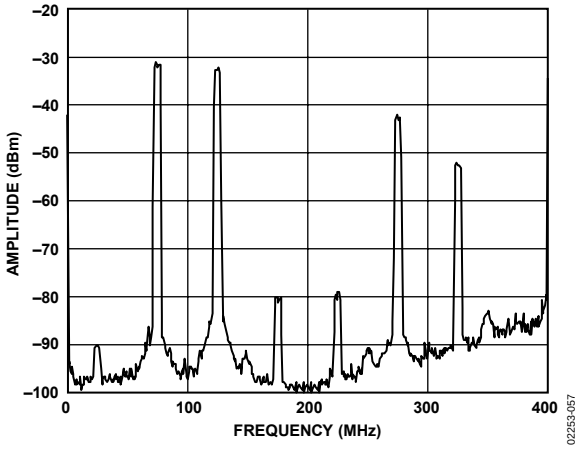


Figure 57. Spectral Plot of 16-QAM Signal in Direct IF Mode at f_{DATA} = 100 MSPS

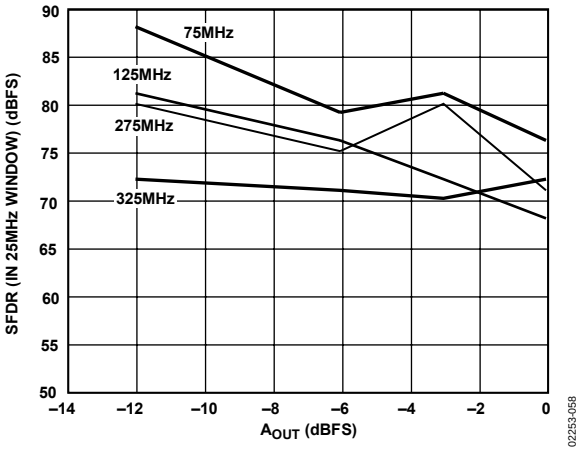


Figure 58. Dual-Tone Windowed SFDR vs. A_{OUT} @ f_{DATA} = 100 MSPS

Regardless of which image is selected for a given application, the adjacent images must be sufficiently filtered. In most cases, a SAW filter providing differential inputs represents the optimum device for this purpose. For single-ended SAW filters, a balanced-to-unbalanced RF transformer is recommended. The high output impedance of the AD9772A provides a certain amount of flexibility in selecting the optimum resistive load, R_{LOAD}, as well as any matching network.

For many applications, the data update rate for the DAC (that is, f_{DATA}) must be a fixed integer multiple of a system reference clock (for example, GSM − 13 MHz). Furthermore, these applications prefer to use standard IF frequencies, which offer a large selection of SAW filter choices with various pass bands (for example, 70 MHz). In addition, these applications may benefit from the AD9772A's direct IF mode capabilities when used in conjunction with a digital upconverter, such as the AD6622. Because the AD6622 can digitally synthesize and tune up to four modulated carriers, it is possible to judiciously tune these carriers in a region falling within the pass band an IF filter while the AD9772A is reconstructing a waveform. Figure 59 shows an example in which four carriers are tuned around 18 MHz with a digital upconverter operating at 52 MSPS such that when reconstructed by the AD9772A in the IF mode, these carriers fall around a 70 MHz IF.

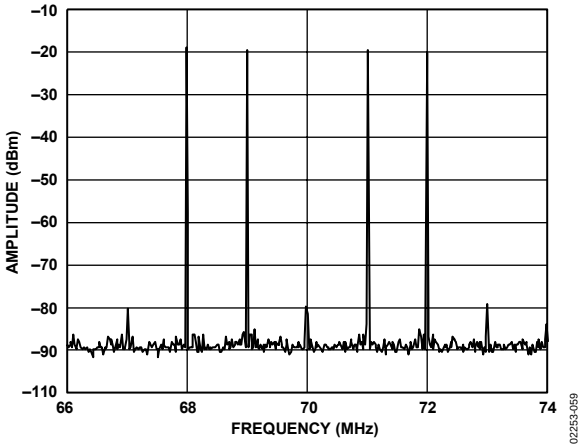


Figure 59. Spectral Plot of Four Carriers at 60 MHz IF with f_{DATA} = 52 MSPS, PLLVDD = 0

AD9772A EVALUATION BOARD

The AD9772A-EB is an evaluation board for the AD9772A TxDAC. Careful attention to the layout and circuit design, along with the prototyping area, allows the user to easily and effectively evaluate the AD9772A in different modes of operation.

Referring to Figure 60 and Figure 61, the performance of AD9772A can be evaluated differentially or in a single-ended fashion using a transformer, differential amplifier, or directly coupled output. To evaluate the output differentially using the transformer, remove Jumper JP12 and Jumper JP13 and monitor the output at J6 (IOUT). To evaluate the output differentially, remove the transformer (T2) and install jumpers JP12 and JP13. The output of the amplifier can be evaluated at J13 (AMPOUT). To evaluate the AD9772A in a single-ended fashion with a directly coupled output, remove the transformer and Jumper JP12 and Jumper JP13, and install Resistor R16 or Resistor R17 with 0 Ω.

The digital data to the AD9772A comes across a ribbon cable that interfaces to a 40-pin IDC connector. Proper termination or voltage scaling can be accomplished by installing the RN2 and/or RN3 SIP resistor networks. The 22 Ω DIP resistor network, RN1, must be installed and helps reduce the digital data edge rates. A single-ended clock input can be supplied via the ribbon cable by installing JP8, or, more preferably, via the SMA connector, J3 (CLOCK). If the clock is supplied by J3, the AD9772A can be configured for a differential clock interface by installing Jumper JP1 and configuring JP2, JP3, and JP9 in the DF position. To configure the AD9772A clock input for a single-ended clock interface, remove JP1 and configure JP2, JP3, and JP9 in the SE position.

The AD9772A PLL clock multiplier can be disabled by configuring Jumper JP5 in the L position. In this case, the user must supply a clock input at twice (2×) the data rate via J3 (CLOCK). The 1× clock is available on the SMA connector J1 (PLLLOCK), and should be used to trigger a pattern generator directly or via a programmable pulse generator. Note that PLLLOCK is capable of providing a 0 V to 0.85 V output into a 50 Ω load. To enable the PLL clock multiplier, JP5 must be configured for the H position. In this case, the clock can be supplied via the ribbon cable (that is, JP8 installed) or J3 (CLOCK). The divide-by-N ratio can be set by configuring JP6 (DIV0) and JP7 (DIV1).

The AD9772A can be configured for baseband or direct IF mode operation by configuring Jumper JP11 (MOD0) and Jumper JP10 (MOD1). For baseband operation, JP10 and JP11 should be configured in the L position. For direct IF operation, JP10 and JP11 should be configured in the H position. For direct IF operation without zero-stuffing, JP11 should be configured in the H position while JP10 should be configured in the low position.

The AD9772A voltage reference can be enabled or disabled via JP4. To enable the reference, configure JP4 in the internal position. A voltage of approximately 1.2 V will appear at the TP6 (REFIO) test point. To disable the internal reference, configure JP4 in the external position and drive TP6 with an external voltage reference. Lastly, the AD9772A can be placed in the sleep mode by driving the TP11 test point with a logic level high input signal.

SCHEMATICS

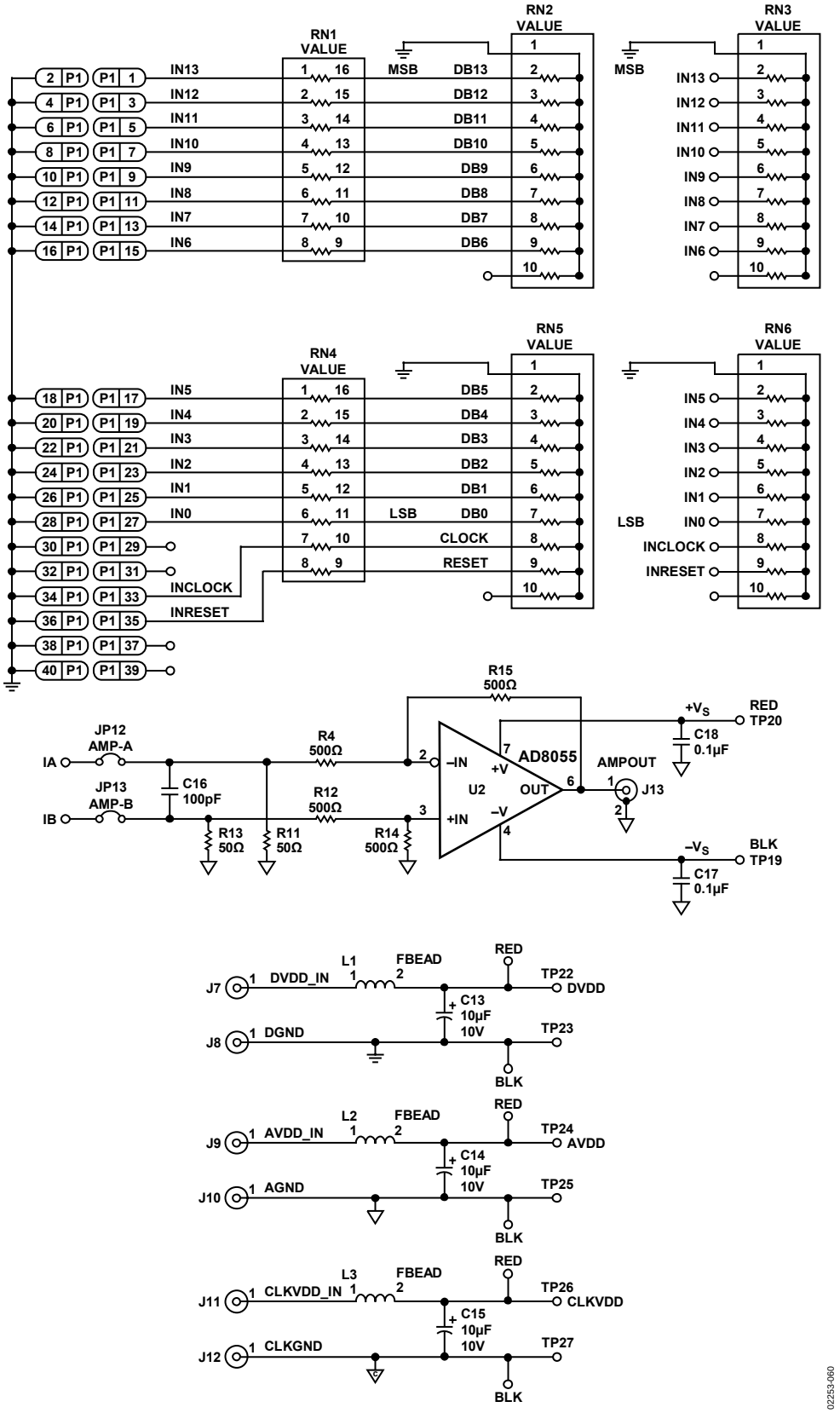
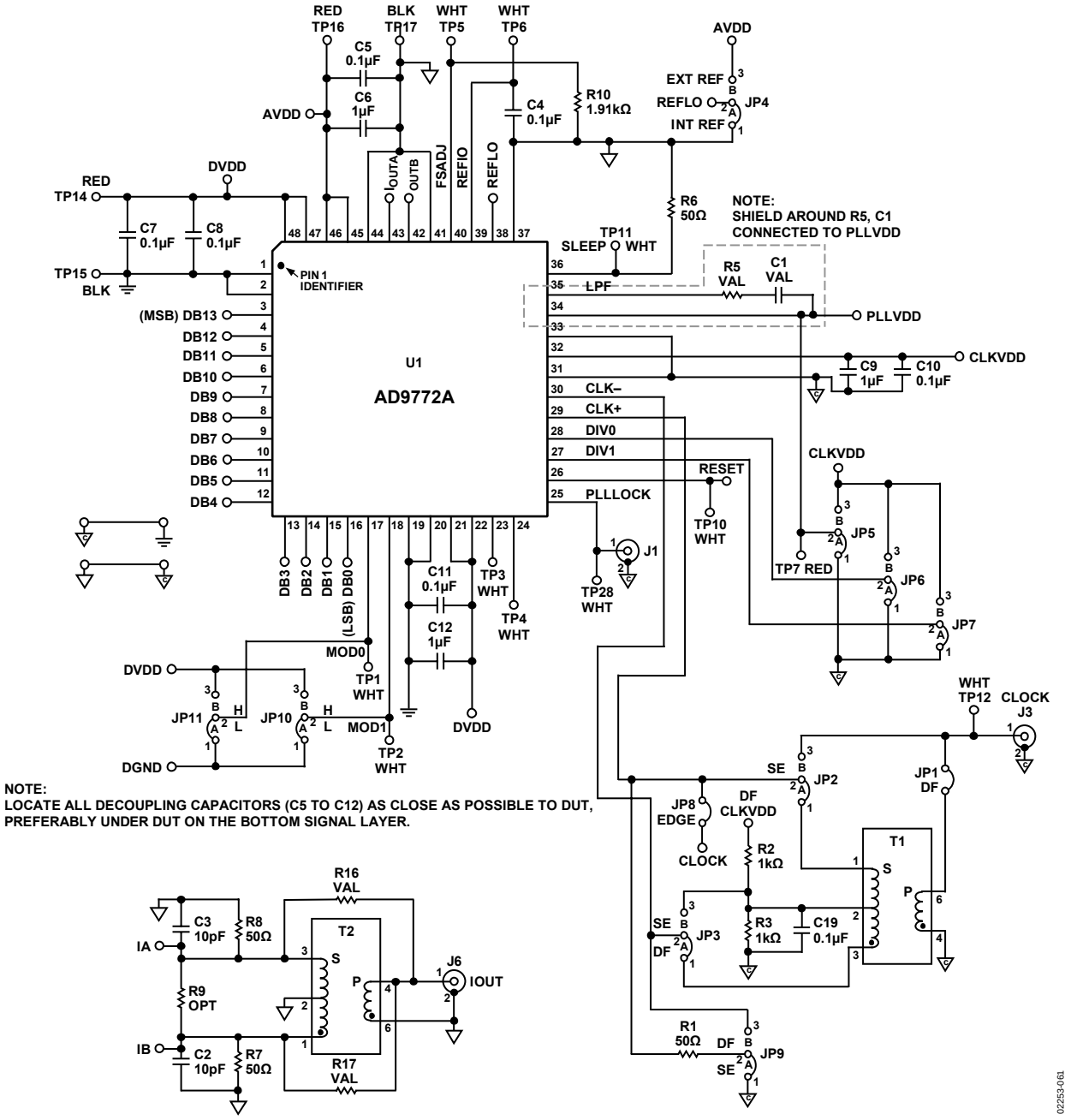


Figure 60. Drafting Schematic of Evaluation Board



NOTE:
LOCATE ALL DECOUPLING CAPACITORS (C5 TO C12) AS CLOSE AS POSSIBLE TO DUT, PREFERABLY UNDER DUT ON THE BOTTOM SIGNAL LAYER.

Figure 61. Drafting Schematic of Evaluation Board (Continued)

EVALUATION BOARD LAYOUT

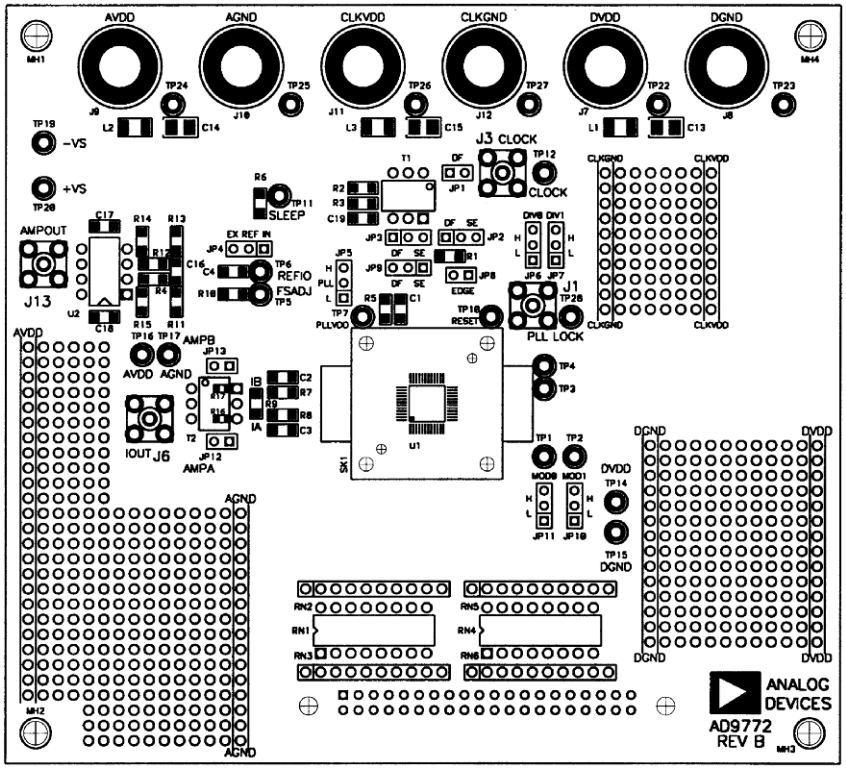


Figure 62. Silkscreen Layer—Top

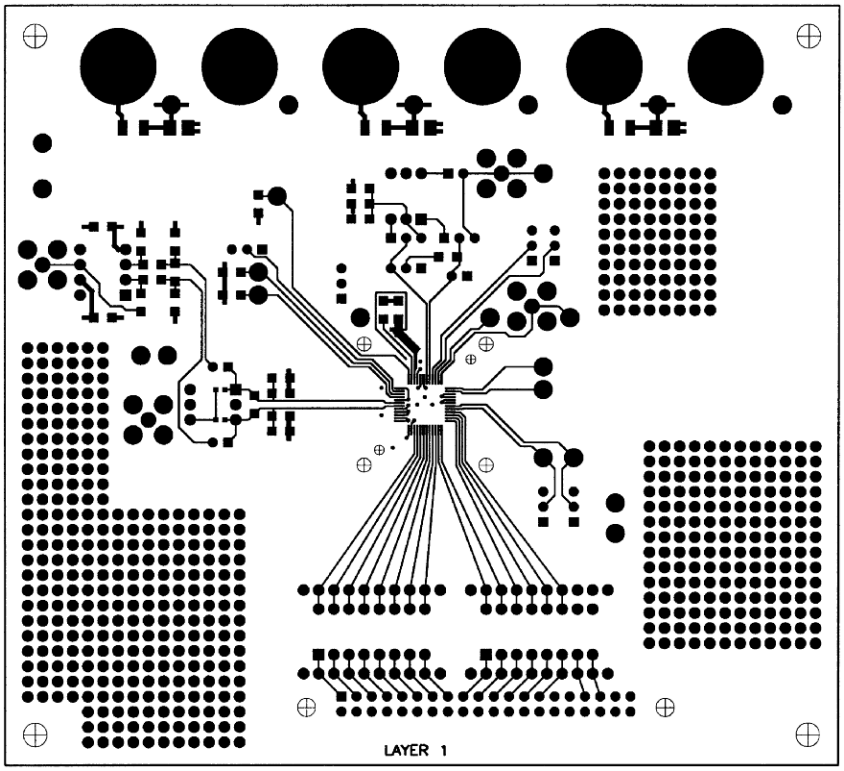


Figure 63. Component-Side PCB Layout (Layer 1)

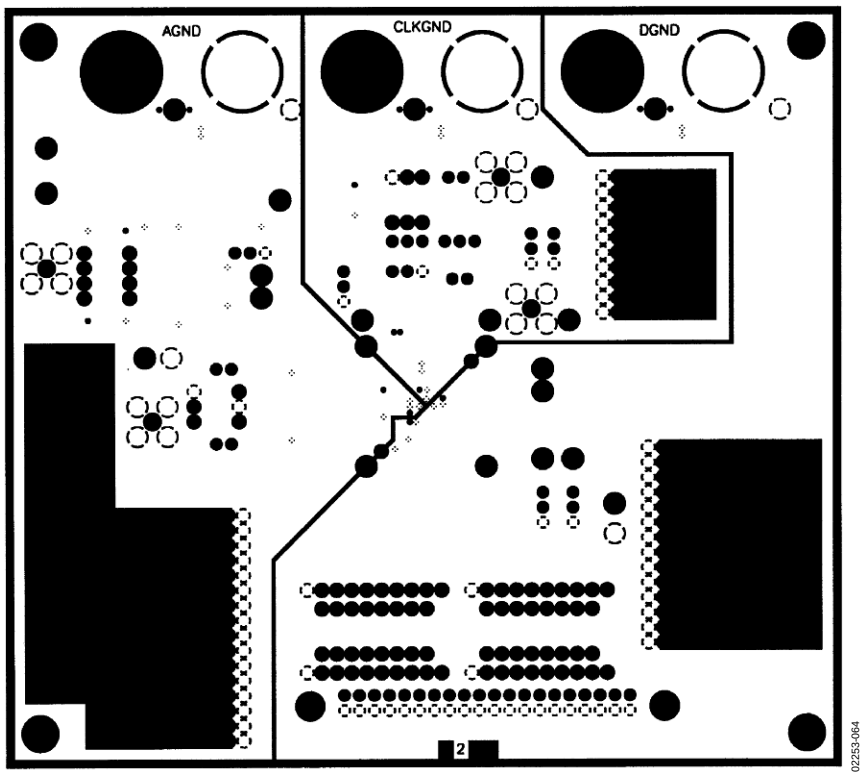


Figure 64. Ground Plane PCB Layout (Layer 2)

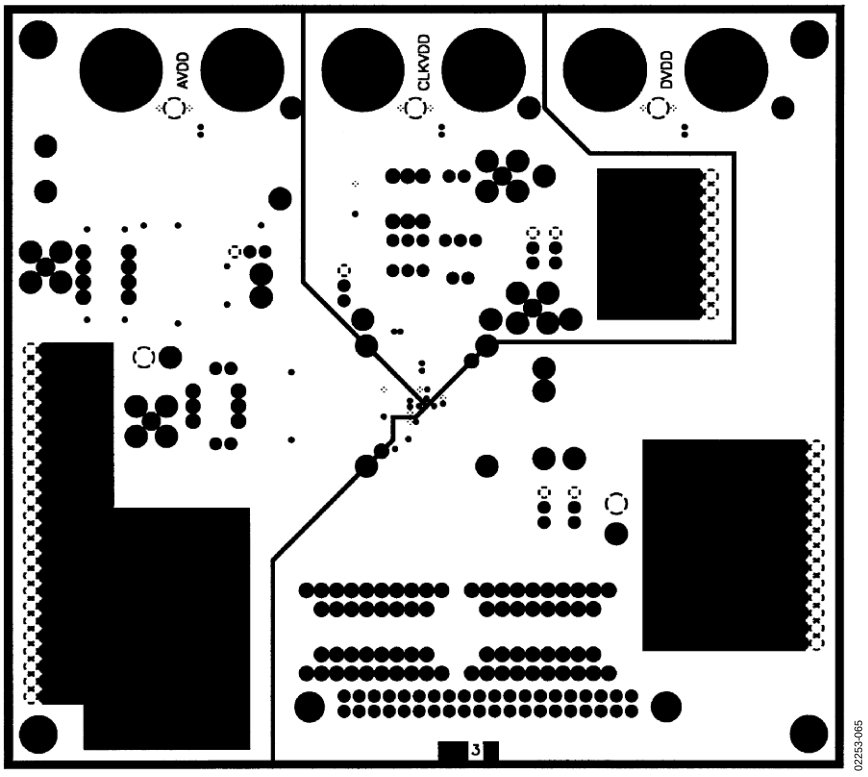


Figure 65. Power Plane PCB Layout (Layer 3)

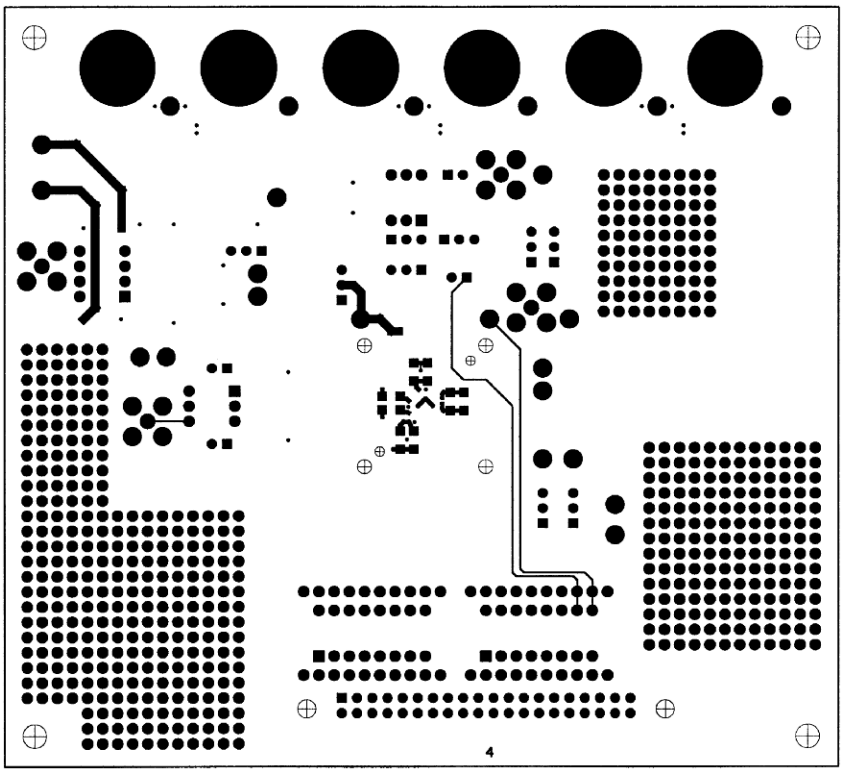


Figure 66. Solder-Side PCB Layout (Layer 4)

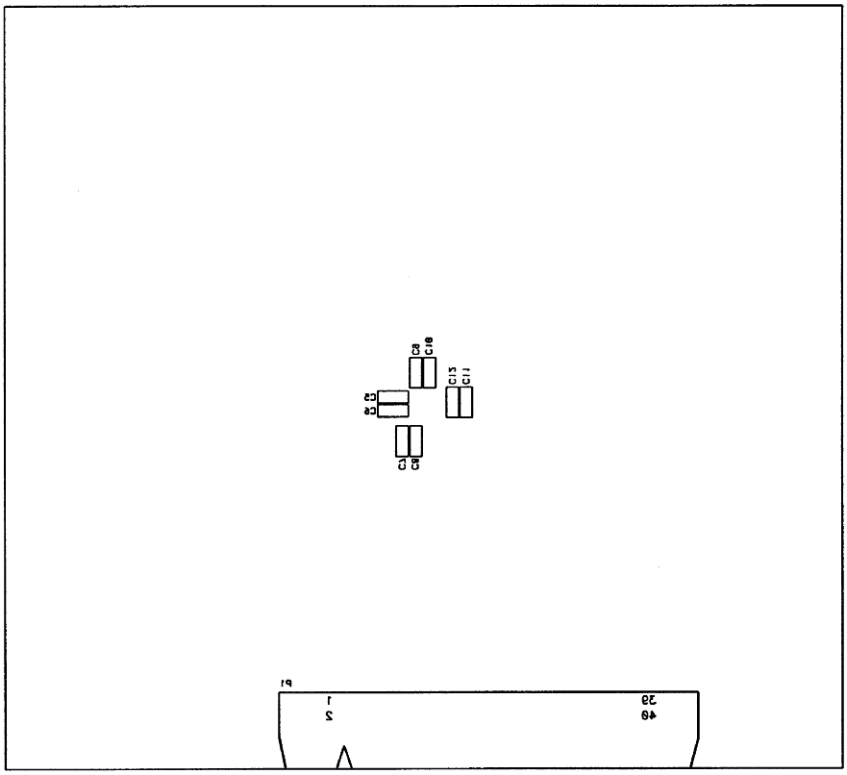


Figure 67. Silkscreen Layer—Bottom

OUTLINE DIMENSIONS

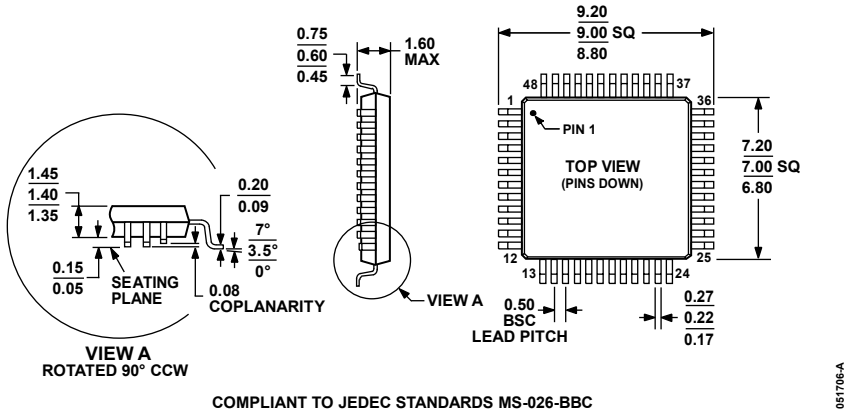


Figure 68. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9772AAST	−40°C to +85°C	48-Lead LQFP	ST-48
AD9772AASTZ[1]	−40°C to +85°C	48-Lead LQFP	ST-48
AD9772AASTRL	−40°C to +85°C	48-Lead LQFP	ST-48
AD9772AASTZRL[1]	−40°C to +85°C	48-Lead LQFP	ST-48
AD9772A-EB		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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D02253-0-2/08(C)

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