# MAX77801

# High-Efficiency Buck-Boost Regulator

## General Description

The MAX77801 is a high-current, high-efficiency buck-boost targeted to mobile applications that use a Li-ion battery or similar chemistries. The MAX77801 utilizes a four-switch H-bridge configuration to support buck and boost operating modes. Buck-boost provides 2.60V to 4.1875V of output voltage range and up to 2A output current.

A unique control algorithm allows high efficiency, outstanding performances in line/load transient response, and seamless transition between buck and boost modes.

DVS (dynamic voltage scaling) input allows the host processor to switch between two preprogrammed output voltages. This feature minimizes power loss for given load conditions. The ramp-up and ramp-down slew rates are programmable through I²C.

The MAX77801 features I²C-compatible, 2-wire serial interface consisting of a bidirectional serial-data line (SDA) and a serial-clock line (SCL). It supports SCL clock rates up to 3.4MHz.

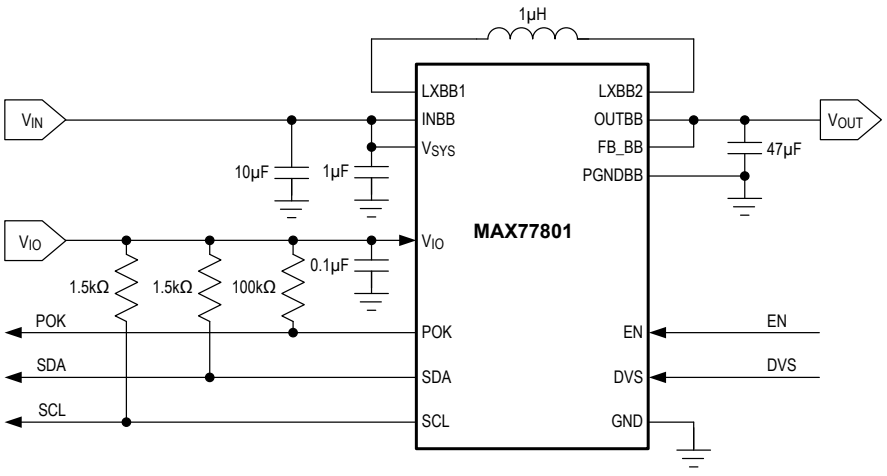
## Applications

- Smartphones and Tablets
- Battery-Powered Applications

## Benefits and Features

- 2A High-Efficiency Buck and Boost Operation Including Seamless Transition Between Buck and Boost Mode
- Flexibility Supports Various Designs
  - $V_{OUT}$ Range from 2.60V to 4.1875V with 12.5mV Step
  - High-Speed (Up to 3.4MHz) I²C Serial Interface
- Low Quiescent Current, High Efficiency, and Dynamic Voltage Scaling Enable System to Be More Efficient
  - DVS Input
  - Up to 97% of Peak Efficiency
  - 55µA Quiescent Current
- High Switching Frequency and Small Package Reduce Solution Size
  - 2.5MHz Switching Frequency
  - 20-Bump WLP (0.4mm Pitch)
- Safety Features Enhance Device and System Reliability
  - POK Output
  - Soft-Start
  - True Shutdown™
  - Thermal Shutdown and Short-Circuit Protection

## Typical Application Circuit




*Ordering Information* ***appears at end of data sheet.***

*True Shutdown is a trademark of Maxim Integrated Products, Inc.*

*19-7515; Rev 0; 2/15*

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## Absolute Maximum Ratings

SYS, $V_{IO}$ to GND .....-0.3V to +6.0V
INBB, OUTBB to PGNDBB .....-0.3V to +6.0V
PGNDBB to GND .....-0.3V to +0.3V
SCL, SDA to GND .....-0.3V to ($V_{IO}$ + 0.3V)
EN, DVS, POK to GND .....-0.3V to ($V_{SYS}$ + 0.3V)
FB_BB to GND ..... -0.3V to ($V_{OUTBB}$ + 0.3V)
LXBB1 to PGNDBB ..... -0.3V to ($V_{INBB}$ + 0.3V)
LXBB2 to PGNDBB ..... -0.3V to ($V_{OUTBB}$ + 0.3V)
LXBB1/LXBB2 Continuous RMS Current (Note 1) .....3.3A
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

**Note 1:** LXBB1/LXBB2 node has internal clamp diodes to PGNDBB and INBB. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed the power dissipation limit of IC package.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 2)

Junction-to Ambient Thermal Resistance ($\theta_{JA}$).....55.49°C/W

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Buck-Boost Electrical Characteristics

($V_{SYS}$ = $V_{INBB}$ = +3.8V, $V_{FB\_BB}$ = $V_{OUTBB}$ = +3.3V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| Input Voltage Range | $V_{INBB}$ | | 2.3 | | 5.5 | V |
| Shutdown Supply Current | $I_{SHDN\_25C}$ | EN = low, $T_A$ = +25°C | | 0.1 | | µA |
| | $I_{SHDN\_85C}$ | EN = low, $T_A$ = +85°C | | 1 | | µA |
| Input Supply Current | $I_{Q\_SKIP}$ | SKIP mode, no switching | | 55 | 70 | µA |
| | $I_{Q\_PWM}$ | FPWM mode, no load | | 6 | | mA |
| Active Discharge Resistance | $R_{DISCHG}$ | | | 100 | | Ω |
| Thermal Shutdown | $T_{SHDN}$ | Rising, 20°C hysteresis | | +165 | | °C |
| **H-BRIDGE** | | | | | | |
| Output Voltage Range | $V_{OUT}$ | I²C programmable (12.5mV step) | 2.60 | | 4.1875 | V |
| Default Output Voltage | | VOUT_DVS_L[6:0] = 0x38 | | 3.3 | | V |
| | | VOUT_DVS_H[6:0] = 0x40 | | 3.4 | | V |
| Output Voltage Accuracy | $V_{OUT\_ACC1}$ | PWM mode, BB_VOUT_DVS_x[6:0 ] = 0x40, no load | -1.0 | | +1.0 | % |
| | $V_{OUT\_ACC2}$ | SKIP mode, BB_VOUT_DVS_x[6:0] = 0x40, no load, $T_A$ = +25°C | -1.0 | | +4.5 | % |

## Buck-Boost Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INBB}$ = +3.8V, $V_{FB\_BB}$ = $V_{OUTBB}$ = +3.3V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Line Regulation | | $V_{INBB}$ = 2.3V to 5.5V | | 0.200 | | %/V |
| Load Regulation | | (Note 4) | | 0.125 | | %/A |
| Line Transient Response | $V_{OS1}$<br>$V_{US1}$ | $I_{OUT}$ = 1.5A,<br>$V_{INB}$ changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, $C_{OUT\_NOM}$ = 47µF<br>(Note 4) | | 50 | | mV |
| Load Transient Response | $V_{OS2}$<br>$V_{US2}$ | $V_{INBB}$ = 3.4V,<br>$I_{OUT}$ changes from 10mA to 1.5A in 15µs, L = 1µH, $C_{OUT\_NOM}$ = 47µF<br>(Note 4) | | 50 | | mV |
| Output Voltage Ramp-Up Slew Rate | | BB_RU_SR = 0 | | 12.5 | | mV/µs |
| | | BB_RU_SR = 1 | | 25 | | mV/µs |
| Output Voltage Ramp-down Slew Rate | | BB_RD_SR = 0 | | 3.125 | | mV/µs |
| | | BB_RD_SR = 1 | | 6.25 | | mV/µs |
| Typical Load Efficiency | ηIOUT_TYP | $I_{OUT}$ = 100mA, $V_{INBB}$ = 3.6V<br>(Note 4) | | 95 | | % |
| Peak Efficiency | ηPK | (Note 4) | | 97 | | % |
| Maximum Output Current | $I_{OUT(MAX)}$ | 2.8V ≤ $V_{INBB}$ ≤ 5.5V | 2000 | | | mA |
| | $I_{OUT(MAX)}$ | 2.3V ≤ $V_{INBB}$ < 2.8V | 1000 | | | mA |
| LXBB1/2 Current Limit | $I_{LIM\_LXBB}$ | | 3.70 | 4.70 | 5.70 | A |
| High-Side PMOS ON Resistance | $R_{DSON}$ (PMOS) | $I_{LXBB}$ = 100mA per switch | | 40 | | mΩ |
| Low-Side NMOS ON Resistance | $R_{DSON}$ (NMOS) | $I_{LXBB}$ = 100mA per switch | | 55 | | mΩ |
| Switching Frequency | $f_{SW}$ | PWM mode, $T_A$ = +25°C | 2.25 | 2.50 | 2.75 | MHz |
| Turn-On Delay Time | $t_{ON\_DLY}$ | From EN asserting to LXBB switching with bias ON | | 100 | | µs |
| Soft-Start Time | $t_{SS}$ | $I_{OUT}$ = 10mA | | 120 | | µs |
| Minimum Effective Output Capacitance | $C_{EFF(MIN)}$ | 0A < $I_{OUT}$ < 2000mA | | 16 | | µF |
| LXBB1, LXBB2 Leakage Current | $I_{LK\_25}$ | $V_{LXBB1/2}$ = 0V or 5.5V, $V_{OUTBB}$ = 5.5V, $V_{SYS}$ = $V_{INBB}$ = 5.5V, $T_A$ = +25°C | | 0.1 | 1 | µA |
| | $I_{LK\_85}$ | $V_{LXBB1/2}$ = 0V or 5.5V, $V_{OUTBB}$ = 5.5V, $V_{SYS}$ = $V_{INBB}$ = 5.5V, $T_A$ = +85°C | | 0.2 | | µA |
| **POWER-OK COMPARATOR** | | | | | | |
| Output POK Trip Level | | Rising threshold | | 80 | | % |
| | | Falling threshold | | 75 | | % |

## Buck-Boost Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INBB}$ = +3.8V, $V_{FB\_BB}$ = $V_{OUTBB}$ = +3.3V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **$V_{SYS}$ UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{SYS}$ Undervoltage Lockout Threshold | $V_{UVLO\_R}$ | $V_{SYS}$ rising | 2.375 | 2.50 | 2.625 | V |
| | $V_{UVLO\_F}$ | $V_{SYS}$ falling (default) | | 2.05 | | V |
| **LOGIC AND CONTROL INPUTS** | | | | | | |
| Input Low Level | $V_{IL}$ | EN, DVS, $V_{SYS}$ ≤ 4.5V, $T_A$ = +25°C | | | 0.4 | V |
| Input High Level | $V_{IH}$ | EN, DVS, $V_{SYS}$ ≤ 4.5V, $T_A$ = +25°C | 1.2 | | | V |
| POK Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 1mA | | | 0.4 | V |
| POK Output High Leakage | $I_{OZH\_25C}$ | $T_A$ = +25°C | -1 | | +1 | µA |
| | $I_{OZH\_85C}$ | $T_A$ = +85°C | | 0.1 | | µA |
| **INTERNAL PULLDOWN RESISTANCE** | | | | | | |
| EN, DVS | RPD | Pulldown resistor to GND | 400 | 800 | 1600 | kΩ |

## I²C Electrical Characteristics

($V_{SYS}$ = 3.8V, $V_{IO}$ = 1.8V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IO}$ Voltage Range | $V_{IO}$ | | 1.7 | | 3.6 | V |
| **SDA AND SCL I/O STAGES** | | | | | | |
| SCL, SDA Input High Voltage | $V_{IH}$ | | 0.7 x $V_{IO}$ | | | V |
| SCL, SDA Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{IO}$ | V |
| SCL, SDA Input Hysteresis | $V_{HYS}$ | | | 0.05 x $V_{IO}$ | | V |
| SCL, SDA Input Current | $I_I$ | $V_{IO}$ = 3.8V | -10 | | +10 | µA |
| SDA Output low Voltage | $V_{OL}$ | $I_{SINK}$ = 20mA | | | 0.4 | V |
| SCL, SDA Input Capacitance | $C_I$ | | | 10 | | pF |
| Output Fall Time from $V_{IO}$ to 0.3 x $V_{IO}$ | $t_{OF}$ | | | | 120 | ns |
| **I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 4)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | | | 1000 | kHz |
| Hold Time (REPEATED) START Condition | $t_{HD;STA}$ | | 0.26 | | | µs |
| SCL low Period | $t_{low}$ | | 0.5 | | | µs |
| SCL high Period | $t_{high}$ | | 0.26 | | | µs |
| Setup Time REPEATED START Condition | $t_{SU\_STA}$ | | 0.26 | | | µs |

## I²C Electrical Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{IO}$ = 1.8V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DATA Hold Time | $t_{HD\_DAT}$ | | 0 | | | µs |
| DATA Setup Time | $t_{SU\_DAT}$ | | 50 | | | ns |
| Setup Time for STOP Condition | $t_{SU\_STO}$ | | 0.26 | | | µs |
| Bus-Free Time Between STOP and START | $t_{BUF}$ | | 0.5 | | | µs |
| Capacitive Load for Each Bus Line | $C_B$ | | | | 550 | pF |
| Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter | | | | 50 | | ns |
| **I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B$ = 100pF) (Note 4)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | | | 3.4 | MHz |
| Set-Up Time REPEATED START Condition | $t_{SU\_STA}$ | | 160 | | | ns |
| Hold Time (REPEATED) START Condition | $t_{HD\_STA}$ | | 160 | | | ns |
| CLK Low Period | $t_{low}$ | | 160 | | | ns |
| CLK High Period | $t_{high}$ | | 60 | | | ns |
| DATA Setup Time | $t_{SU\_DAT}$ | | 10 | | | ns |
| DATA Hold Time | $t_{HD\_DAT}$ | | | 35 | | ns |
| SCL Rise Time (Note 4) | $t_{RCL}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit | $t_{RCL1}$ | $T_A$ = +25°C | 10 | | 80 | ns |
| SCL Fall Time | $t_{FCL}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| SDA Rise Time | $t_{RDA}$ | $T_A$ = +25°C | | | 80 | ns |
| SDA Fall Time | $t_{FDA}$ | $T_A$ = +25°C | | | 80 | ns |
| Setup Time for STOP Condition | $t_{SU\_STO}$ | | 160 | | | ns |
| Bus Capacitance | $C_B$ | | | | 100 | pF |
| Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter | | | | 10 | | ns |

## I²C Electrical Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{IO}$ = 1.8V, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

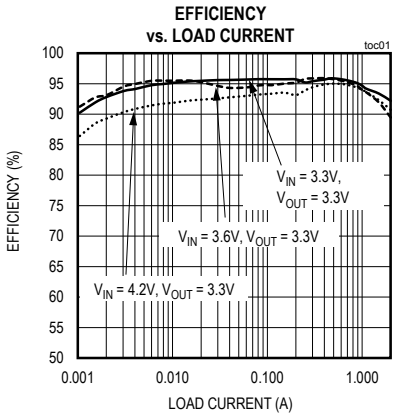
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B$ = 400pF) (Note 4)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | | | 1.7 | MHz |
| Setup Time REPEATED START Condition | $t_{SU\_STA}$ | | 160 | | | ns |
| Hold Time (REPEATED) START Condition | $t_{HD\_STA}$ | | 160 | | | ns |
| SCL Low Period | $t_{low}$ | | 320 | | | ns |
| SCL High Period | $t_{high}$ | | 120 | | | ns |
| DATA Setup Time | $t_{SU\_DAT}$ | | 10 | | | ns |
| DATA Hold Time | $t_{HD\_DAT}$ | | | 75 | | ns |
| SCL Rise Time | $t_{RCL}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit | $t_{RCL1}$ | $T_A$ = +25°C | 20 | | 160 | ns |
| SCL Fall Time | $t_{FCL}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| SDA Rise Time | $t_{RDA}$ | $T_A$ = +25°C | | | 160 | ns |
| SDA Fall Time | $t_{FDA}$ | $T_A$ = +25°C | | | 160 | ns |
| Setup Time for STOP Condition | $t_{SU\_STO}$ | | 160 | | | ns |
| Bus Capacitance | $C_B$ | | | | 400 | pF |
| Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter | $t_{SP}$ | | | 10 | | ns |

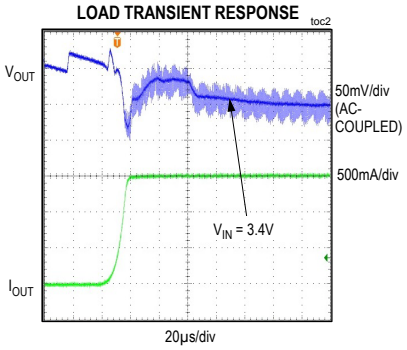
**Note 3:** Limits are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

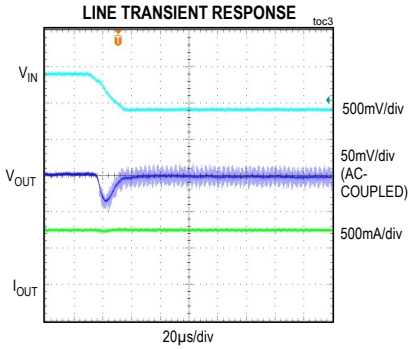
**Note 4:** Guaranteed by design. Not production tested.

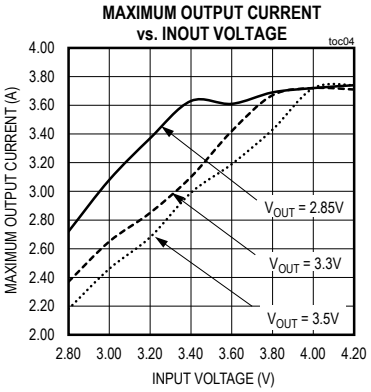
## Typical Operating Characteristics

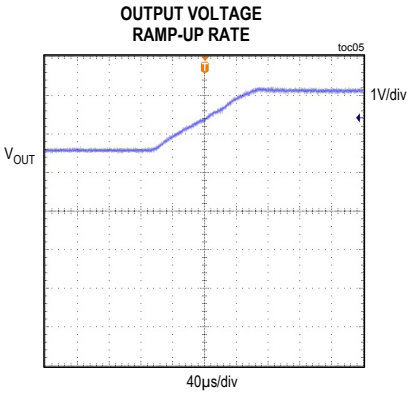
($V_{SYS}$ = $V_{INBB}$ = +3.8V , $V_{FB\_BB}$ = $V_{OUTBB}$ = +3.3V, $T_A$ = +25°C.)

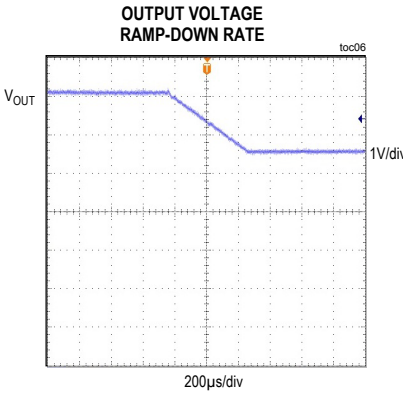


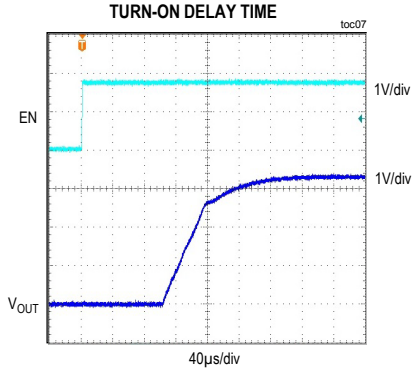



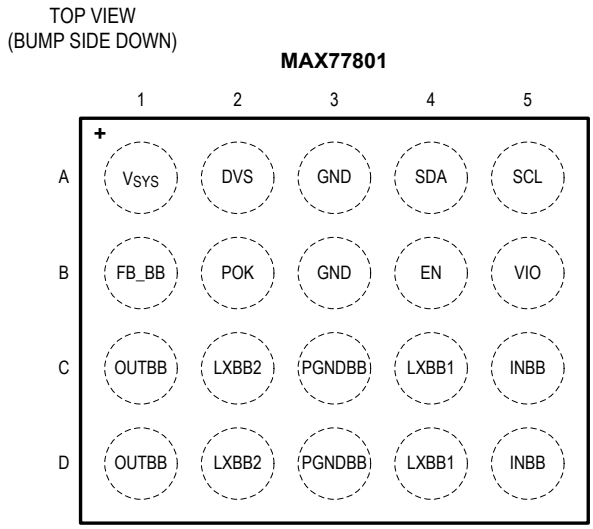



## Pin Configuration




**20-BUMP WLP (5 x 4), 0.4mm Pitch**

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| A1 | $V_{SYS}$ | System (Battery) Voltage Input. Bypass to GND with a 1µF capacitor. |
| A2 | DVS | Dynamic Voltage Scaling Logic Input. If not in use, then it must be connected to GND. |
| A3, B3 | GND | Ground. Star-Ground Connection to System GND |
| A4 | SDA | $I^2C$ Data I/O (High Impedance in Off State). A 1.5kΩ~2.2kΩ of pullup resistor to $V_{IO}$ is required. |
| A5 | SCL | $I^2C$ Clock Input (High Impedance in Off State). A 1.5kΩ~2.2kΩ of pullup resistor to $V_{IO}$ is required. |
| B1 | FB_BB | Buck-Boost Output Voltage Feedback |
| B2 | POK | Power OK. Open-drain output asserted after buck-boost output reaches to 90% of output voltage. Polarity is factory selectable option. Active high by default. |
| B4 | EN | Active-High, Buck-Boost External Enable Input. An 800kΩ internal pulldown resistance to the GND. If this pin is not used, leave it floating. |
| B5 | $V_{IO}$ | $I^2C$ Supply Voltage Input. Bypass to GND with a 0.1µF capacitor. If not in use, connect to GND. |
| C1, D1 | OUTBB | Buck-Boost Output |
| C2, D2 | LXBB2 | Buck-Boost Switching Node 2 |
| C3, D3 | PGNDBB | Buck-Boost Power Ground. Star-ground connection to system GND. |
| C4, D4 | LXBB1 | Buck-Boost Switching Node 1 |
| C5, D5 | INBB | Buck-Boost Input. Bypass to PGNDBB with a 10µF capacitor. |

## Detailed Description

### Chip Enable (EN)

When EN pin goes high, the MAX77801 turns on the internal bias circuitry, which typically takes 85µs to settle. As soon as the bias is ready, buck-boost regulator is enabled. Once $V_{IO}$ is supplied, then all user registers are accessible through I²C. When EN pin is pulled low, the MAX77801 goes into shutdown mode. This event also resets all type-O registers to their POR default values.

### Immediate Turn-Off Events

The following events initiate immediate turn-off:

- Thermal protection ($T_J$ > +165°C)
- $V_{SYS}$ < $V_{SYS\ UVLO}$ falling threshold ($V_{UVLO\_F}$)
- Overcurrent protection

The events in this category disable buck-boost until the hazardous condition come back to normal conditions.

### Regulator Enable Control

Buck-boost has GPIO enable pin EN as well as I²C enable bit. As shown in the Table 1, the regulator should be enabled by EN and then it can be enabled or disabled by I²C control bit (AND logic) until EN remains in high.

### Dynamic Voltage Scaling (DVS)

Buck-boost includes DVS feature that allows output voltage to change dynamically. The buck-boost output voltages are selected by DVS. When EN pin is asserted, the status of DVS pin is latched until completing soft-start so that changes on DVS are ignored. After soft-start is done, internal logic sets $V_{OUT}$ based on DVS input.

Buck-boost regulator supports a programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew rate can be set to 12.5mV/µs or 25mV/µs through BB_RU_SR bit. Also, the ramp-down slew rate can be set to 3.125mV/µs or 6.25mV/µs through BB_RD_SR bit.

### Power-OK (POK) Indicator

Buck-boost has an open-drain output that is asserted after the output voltage reaches 90%. The polarity of POK output is factory programmable option. It is active high by default.

**Table 1. Enable Control Logic Truth Table**

| EN | BB_EN BIT | OPERATING MODE |
|---|---|---|
| low | x | Device off |
| high | 0 | Disable output |
| high | 1 (default) | Enable output |

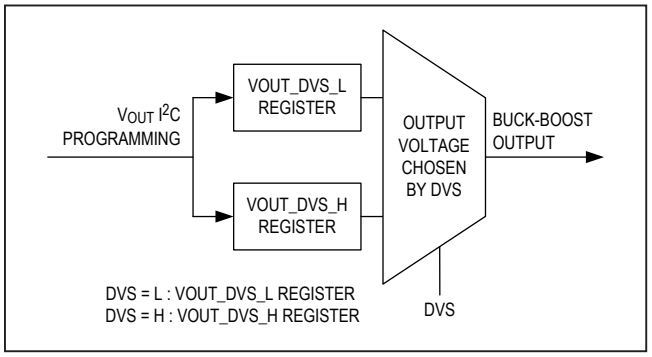



*Figure 1. DVS Functional Block Diagram*

## Buck-Boost Regulator

When EN pin goes high, the MAX77801 turns on the internal bias circuitry, which typically takes 85µs to settle. As soon as the bias is ready, buck-boost regulator is enabled. Once $V_{IO}$ is supplied, then all user registers are accessible through I²C. When EN pin is pulled low, the MAX77801 goes into shutdown mode. This event also resets all type-O registers to their POR default values.

### H-Bridge Controller

H-bridge architecture operates at 2.5MHz fixed frequency with a pulse width modulated (PWM), current-mode control scheme. This topology is in a cascade of a boost regulator and a buck regulator using a single inductor and output capacitor. Buck, buck-boost, and boost stages are 100% synchronous for highest efficiency in portable applications.

There are three phases implemented with the H-bridge switch topology, as shown in Figure 3:

- Φ1 switch period (Phase 1: HS1 = ON, LS2 = ON) stores energy in the inductor, ramping up the inductor current at a rate proportional to the input voltage divided by inductance, $V_{INBB/L}$.
- Φ2 switch period (Phase 2: HS1 = ON, HS2 = ON) ramps the inductor current up or down, depending on the differential voltage across the inductor, divided by inductance; $\pm(V_{INBB} - V_{OUTBB})/L$.
- Φ3 switch period (Phase 3: LS1 = ON, HS2 = ON) ramps down the inductor current at a rate proportional to the output voltage divided by inductance, $-V_{OUTBB/L}$.

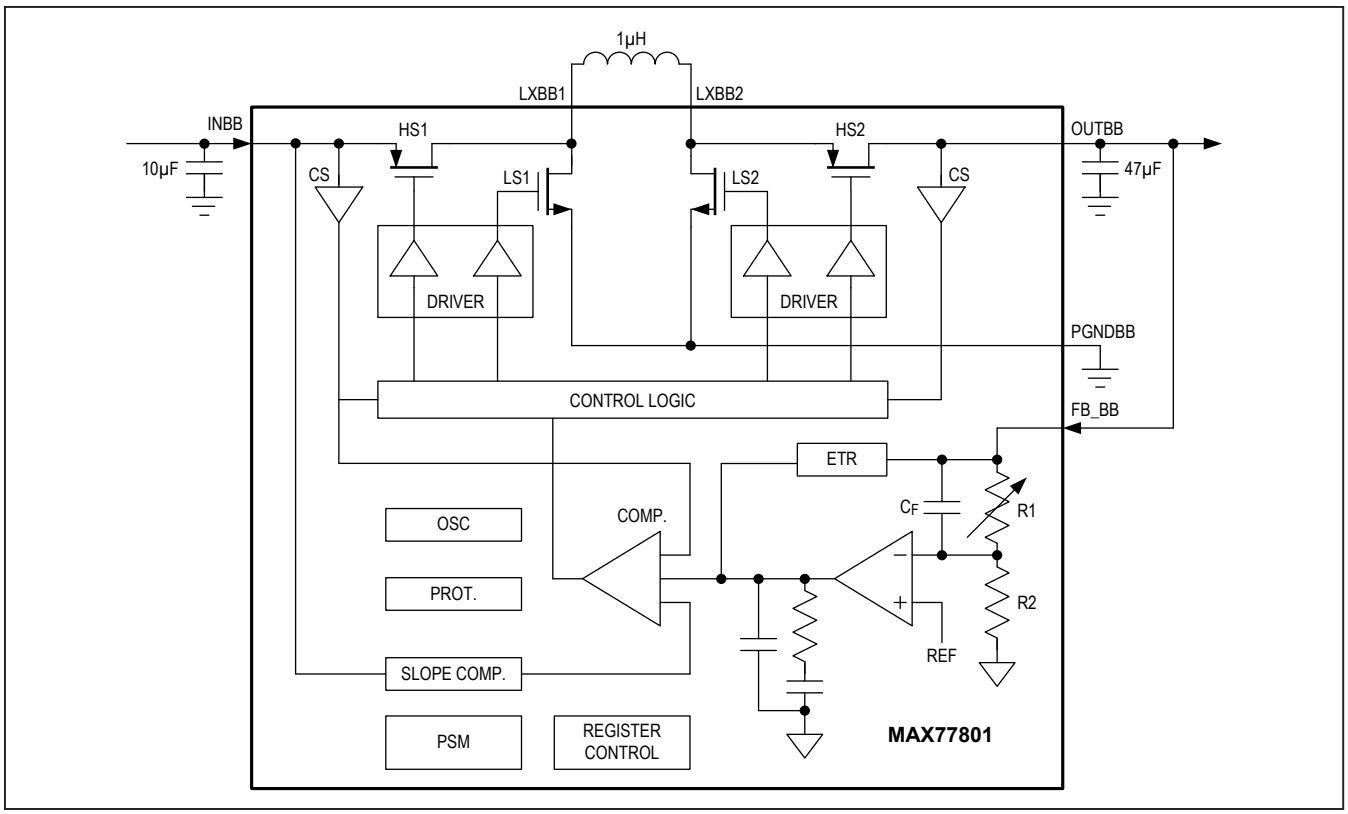



*Figure 2. Buck-Boost Block Diagram*

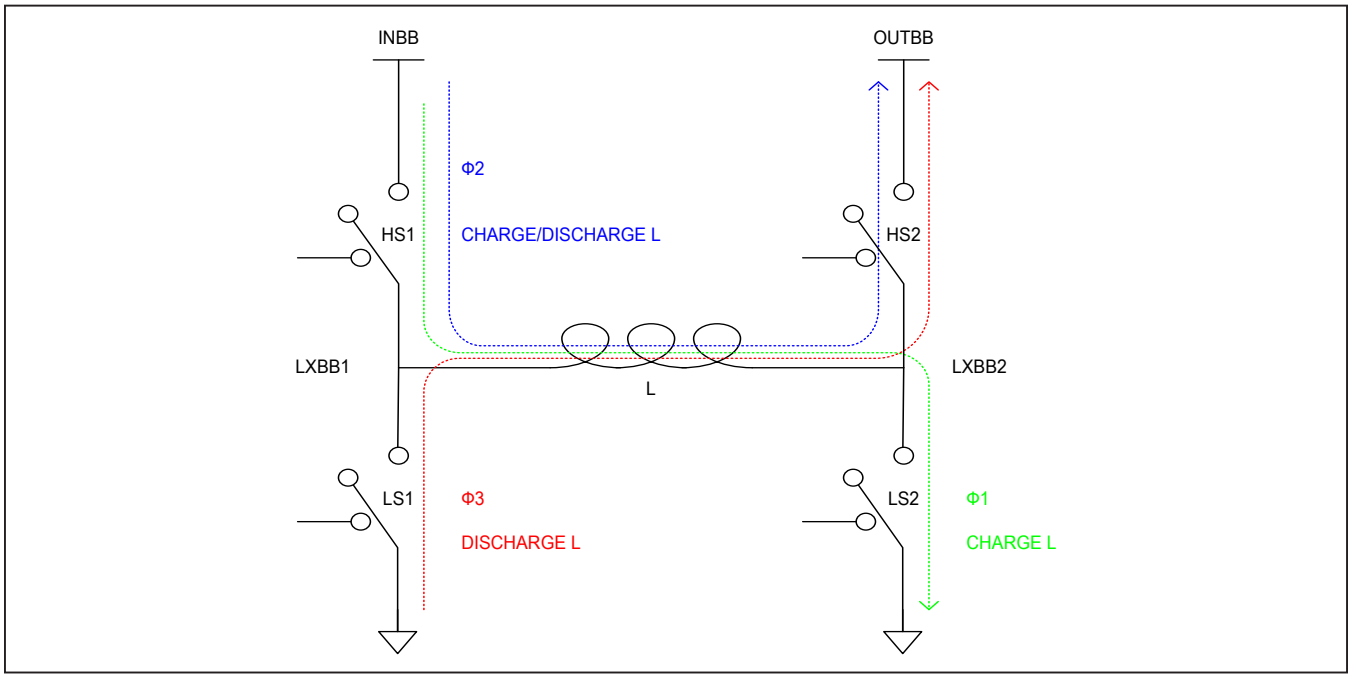



*Figure 3. Buck-Boost Switching Intervals*

2-phase buck topology is utilized when $V_{INBB} > V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ2 is followed by switch period Φ3, resulting in an inductor current waveform similar to Figure 4.

2-phase boost topology is utilized when $V_{INBB} < V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ1 is followed by switch period Φ2, resulting in an inductor current waveform similar to Figure 5.

### Output Voltage Slew-rate Control

Buck-boost regulator supports programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew-rate can be set to 12.5mV/µs or 25mV/µs through BB_RU_SR bit, while the ramp-down slew-rate is programmable to 3.125mV/µs or 6.25mV/µs through BB_RD_SR bit.

### Output Active Discharge

Buck-boost provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (BB_AD = 1), the internal resistor discharges the energy stored in the output capacitor to PGNDBB whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (BB_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

### Inductor Selection

Buck-boost is optimized for a 1µH inductor. The lower the inductor DCR, the higher buck-boost efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for buck-boost.

### Input Capacitor Selection

The input capacitor, $C_{IN}$, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of $C_{IN}$ at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

### Output Capacitor Selection

The output capacitor, $C_{OUT}$, is required to keep the output voltage ripple small and to ensure regulation loop stability. $C_{OUT}$ must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 16µF of minimum effective output capacitance. Considering DC bias characteristic of ceramic capacitors, a 47µF 6.3V capacitor is recommended for most of applications.

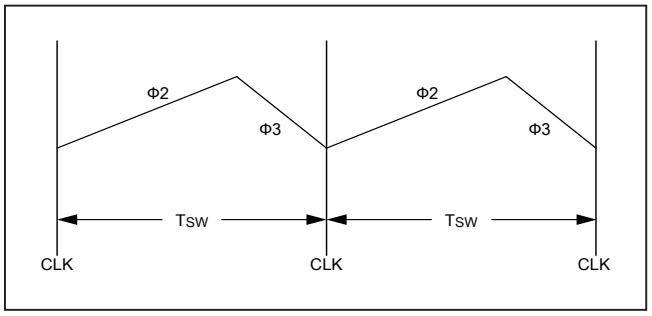



*Figure 4. 2-Phase Buck Mode Switching Current Waveforms*

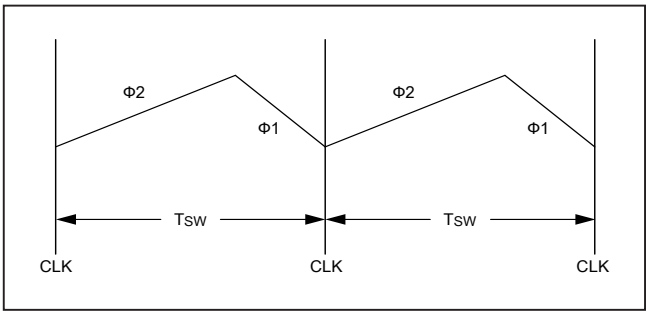



*Figure 5. 2-Phase Boost Mode Switching Current Waveforms*

## Table 2. Suggested Inductors for Buck-Boost

| MANUFACTURER | SERIES | NOMINAL INDUCTANCE (µH) | DC RESISTANCE (typ) (mΩ) | CURRENT RATING (A) -30% (ΔL/L) | CURRENT RATING (A) ΔT = -40°C RISE | DIMENSIONS L x W x H (mm) |
|---|---|---|---|---|---|---|
| TDK | TFM201610GHM-1R0MTAA | 1.0 | 50 | 3.8 | 3.0 | 2.0 x 1.6 x 1.0 |
| Coilcraft | XAL4020-102MEB | 1.0 | 13 | 8.7 | 9.6 | 4.0 x 4.0 x 2.1 |

## Serial Interface

I²C compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the *Register Map* section for details.

I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

### System Configuration

I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

The figure above shows an example of a typical I²C system. A device on I²C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is the master. Any device that is being addressed by the master is considered a slave. When the MAX77801 I²C-compatible interface is operating, it is a slave on I²C bus, and it can be both a transmitter and a receiver, too.

### Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

### START and STOP Conditions

When I²C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the MAX77801. The master terminates transmission by issuing a NOT ACKNOWLEDGE (nA) followed by a STOP condition.

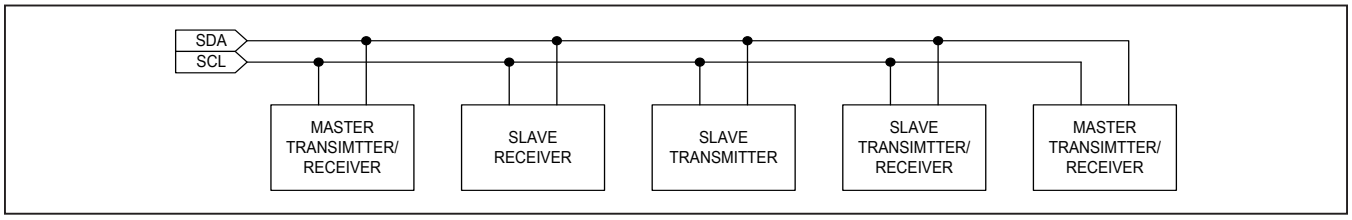



*Figure 6. Functional Logic Diagram for Communications Controller*

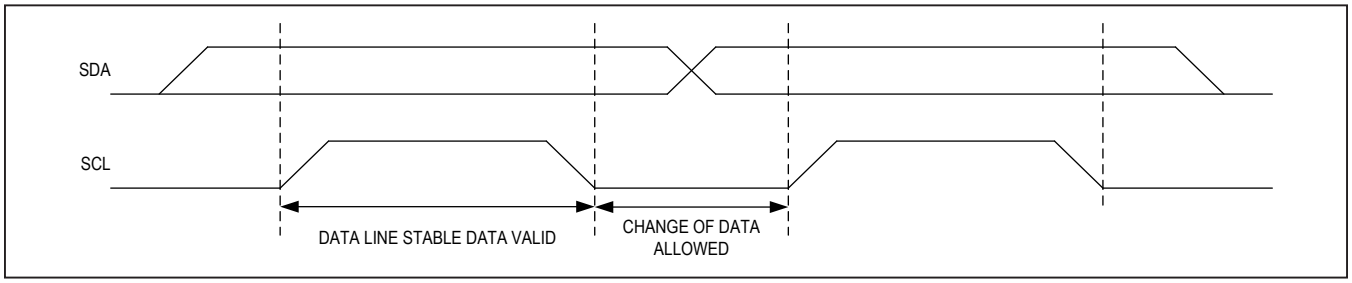



*Figure 7. I²C Bit Transfer*

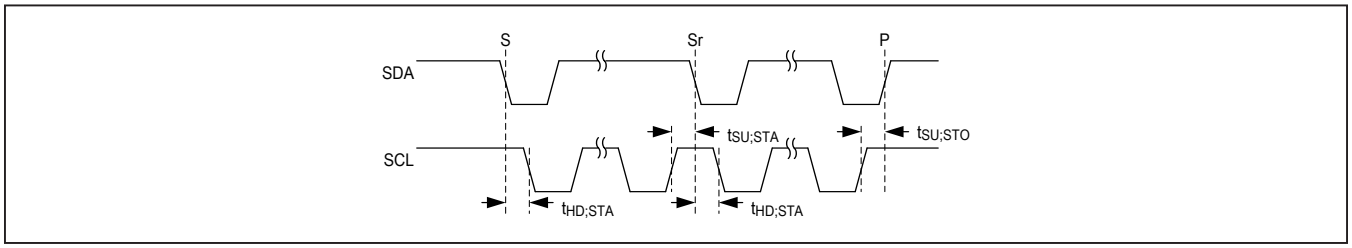



*Figure 8. START and STOP Conditions*

STOP condition frees the bus. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX77801 internally disconnects SCL from I2C serial interface until the next START condition, minimizing digital noise and feedthrough.

### Acknowledge

Both I2C bus master and MAX77801 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT ACKNOWLEDGE, the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

### Slave Address

The I2C slave address of the MAX77801 is shown in Table 3.

### Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77801 does not use any form of clock stretching to hold down the clock line.

### General Call Address

The MAX77801 does not implement the I2C specification called general call address. If the MAX77801 sees a general call address (00000000b), it does not issue an ACKNOWLEDGE.

### Communication Speed

The MAX77801 provides I2C 3.0-compatible (3.4MHz) serial interface.

- I2C revision 3-compatible serial communications channel
  - 0Hz to 100kHz (standard mode)
  - 0Hz to 400kHz (fast mode)
  - 0Hz to 1MHz (fast mode plus)
  - 0Hz to 3.4MHz (high-speed mode)
- Does not utilize I2C clock stretching

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V2/R).

## Table 3. I2C Slave Address

| SLAVE ADDRESS (7 bit) | SLAVE ADDRESS (Write) | SLAVE ADDRESS (Read) |
|---|---|---|
| 001 1000 | 0x30 (0011 0000) | 0x31 (0011 0001) |

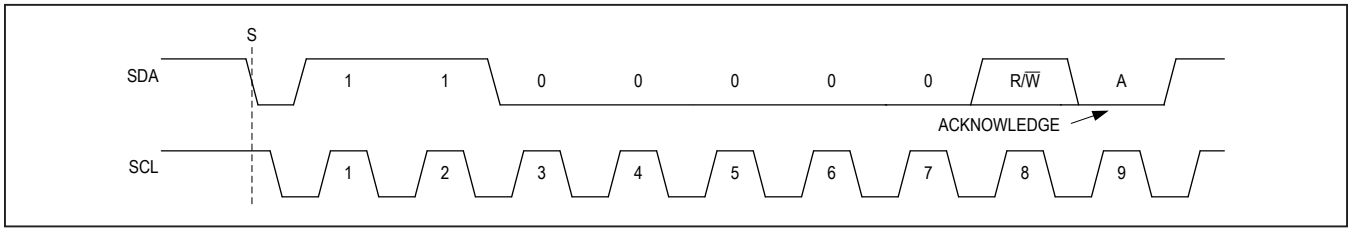



*Figure 9. Slave Address Byte Example*

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I2C 3.0 specification. The major considerations with respect to the MAX77801 are:

- I2C bus master uses current source pullups to shorten the signal rise times.
- I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the MAX77801 inputs filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in *Communication Protocols* section.

## Communication Protocols

The MAX77801 supports both writing and reading from its registers. The following sections show the I2C communication protocols for each functional block. The power block uses the same communications protocols.

### Writing to a Single Register

The figure below shows the protocol for I2C master device to write one byte of data to the MAX77801. This protocol is the same as SMBus specification's write byte protocol.

The write byte protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ 0).
3) The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges or does not acknowledge the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
9) The master sends a STOP condition or a REPEATED START condition. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START leaves the bus input filters in their current state.

### Writing to a Sequential Register

The figure below shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START. The writing to sequential registers protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires. During the last acknowledge related clock pulse, the master can issue an ACKNOWLEDGE or a NOT ACKNOWLEDGE.

The master sends a STOP condition or a REPEATED START condition. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START leaves the bus input filters in their current state.

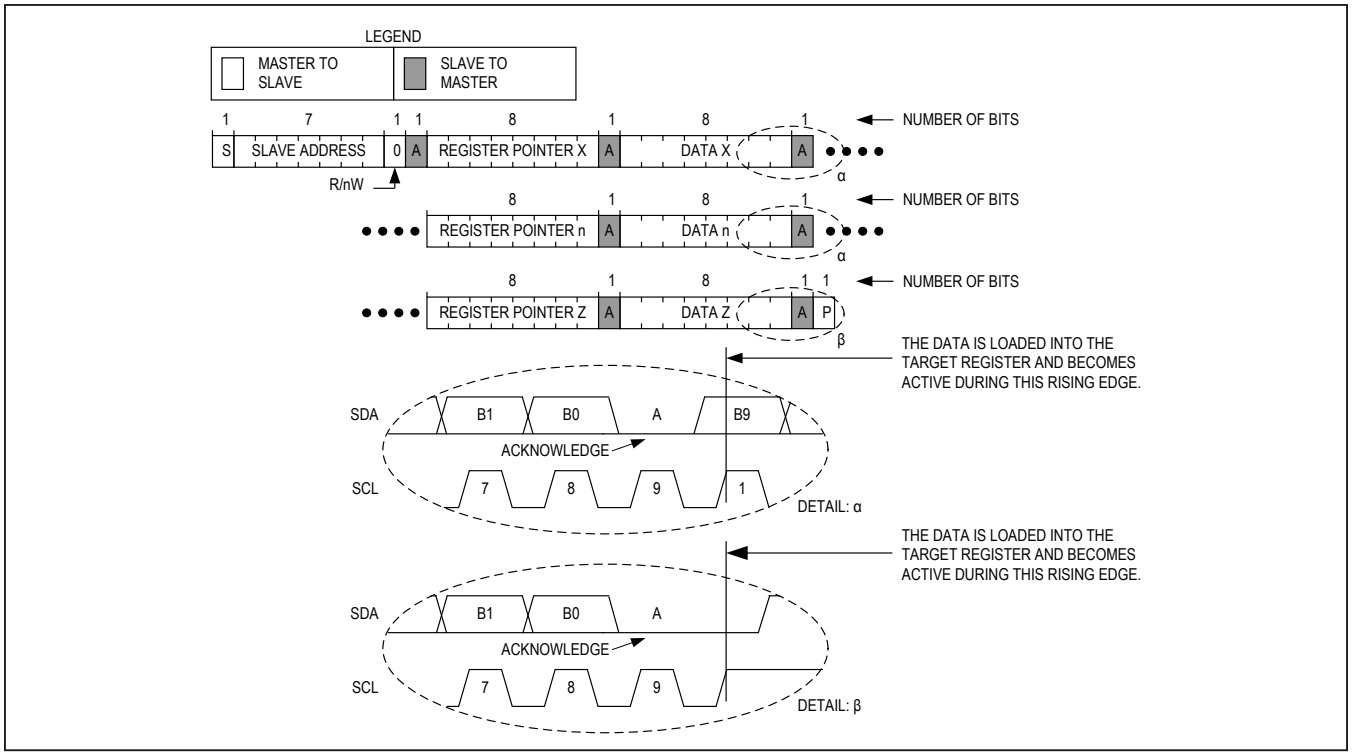



*Figure 10. Writing to a Single Register with Write Byte Protocol*

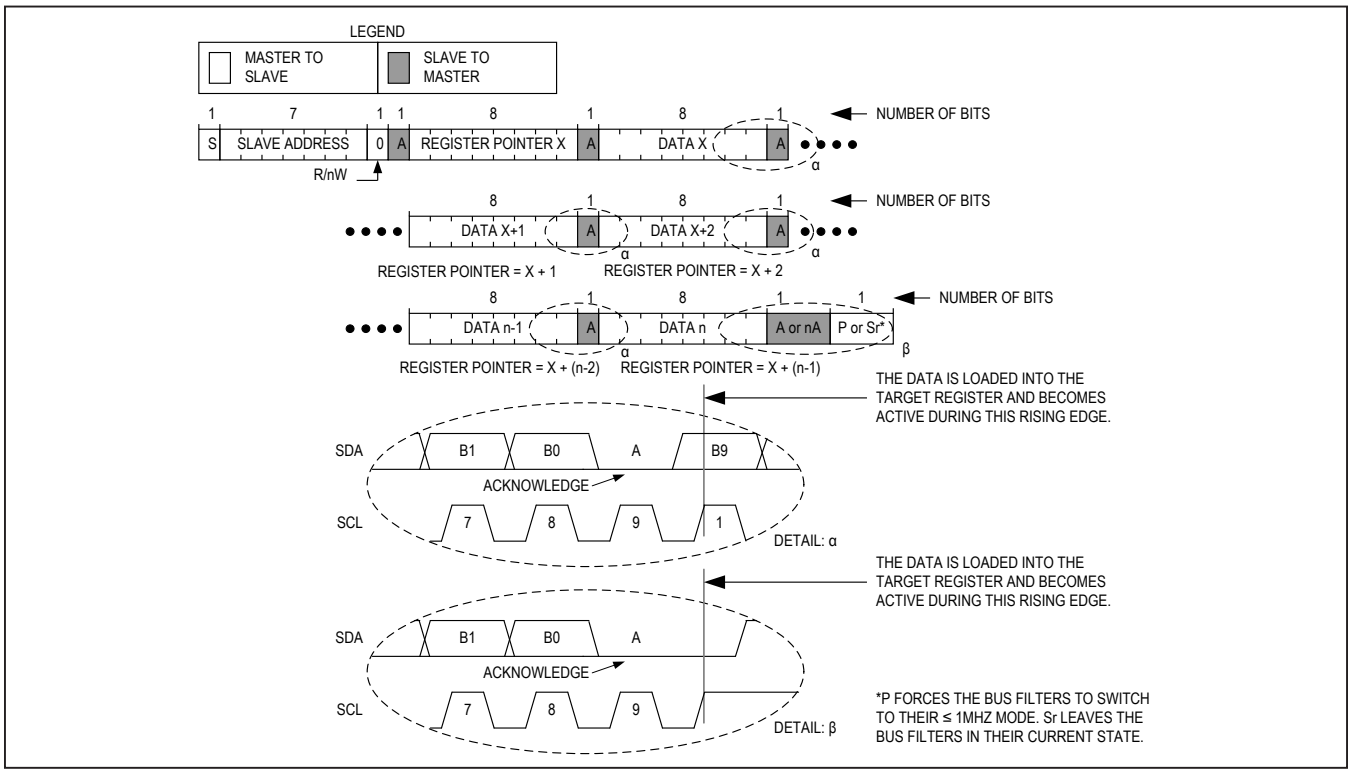



*Figure 11. Writing to Sequential Registers X to N*

### Writing Multiple Bytes Using Register-Data Pairs

The figure below shows the protocol for I2C master device to write multiple bytes to the MAX77801 using register-data pairs. This protocol allows I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition.

The multiple byte register-data pair protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 5 to 7 are repeated as many times as the master requires.

The master sends a STOP condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

### Reading from a Single Register

I2C master device reads one byte of data to the MAX77801. This protocol is the same as SMBus specification's read byte protocol.

The read byte protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command.
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE.
11. The master sends a STOP condition or a REPEATED START condition. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START leaves the bus input filters in their current state.

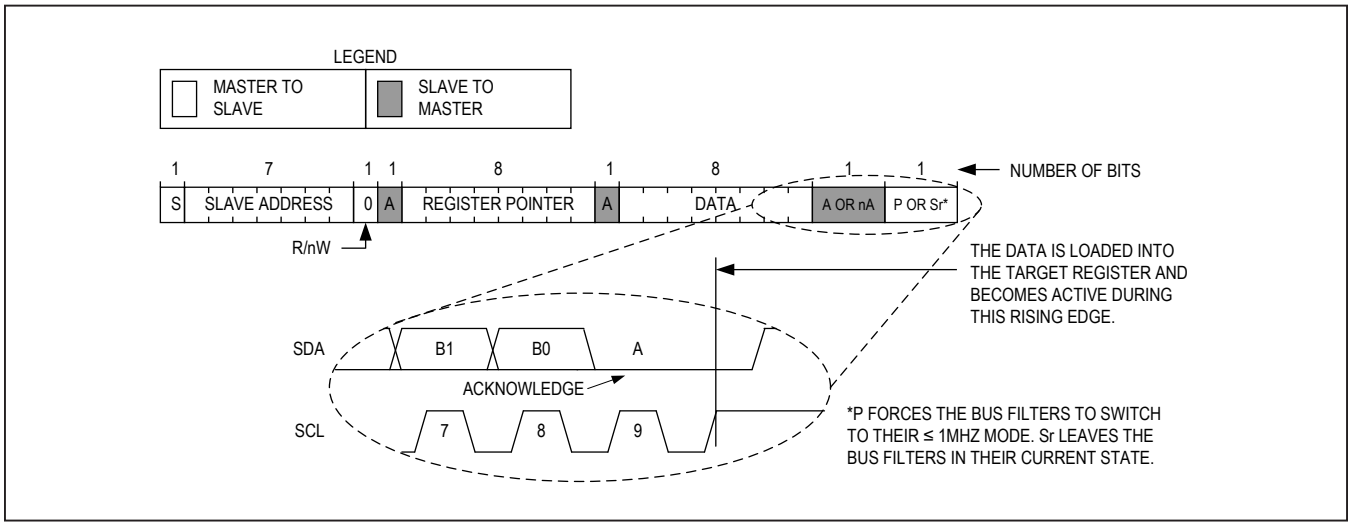



*Figure 12. Writing to Multiple Registers with Multiple Byte Register-Data Pairs Protocol*

Every time the MAX77801 receives a STOP, its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

### Reading from a Sequential Register

Figure 13 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE to signal the slave that it wants more data. When the master has all the data it requires, it issues a NOT ACKNOWLEDGE and a STOP to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command.
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT ACKNOWLEDGE to signal that it wishes to stop receiving data.
12. The master sends a STOP condition or a REPEATED START condition. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START leaves the bus input filters in their current state.

Every time the MAX77801 receives a STOP, its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

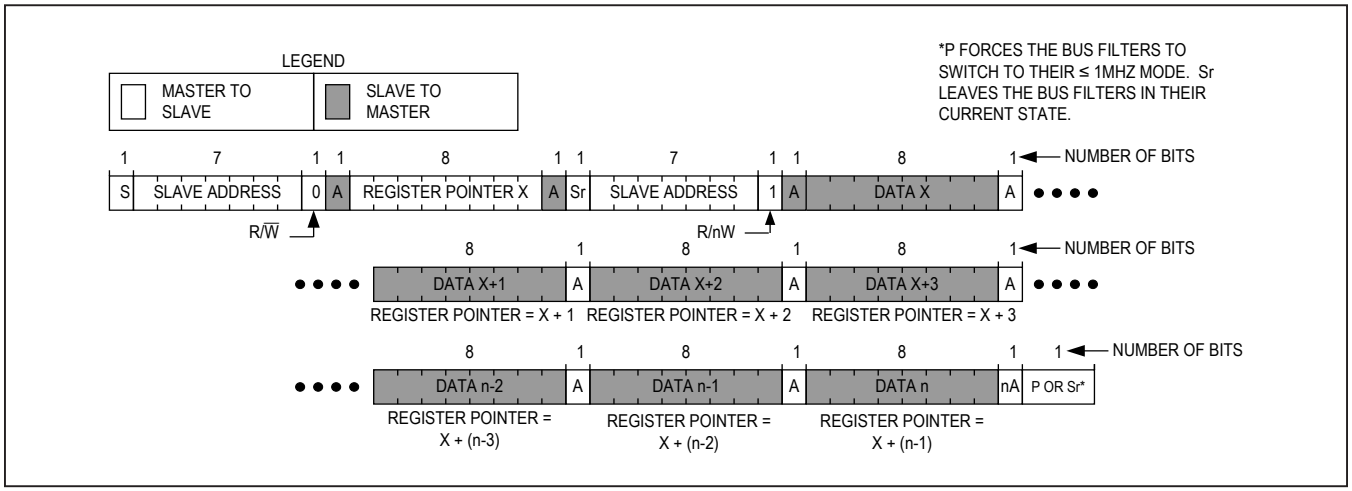



*Figure 13. Reading Continuously from Sequential Registers X to N*

### Engaging HS Mode for Operation Up to 3.4MHz

The figure below shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower
2. The master sends a START command.
3. The master sends the 8-bit master code of 00001xxxb where xxxb are don't care bits.
4. The addressed slave issues a NOT ACKNOWLEDGE.
5. The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a STOP is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. After a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

## Registers

### Register Reset Conditions

- Type O: Registers are reset when $V_{SYS}$ < V = low

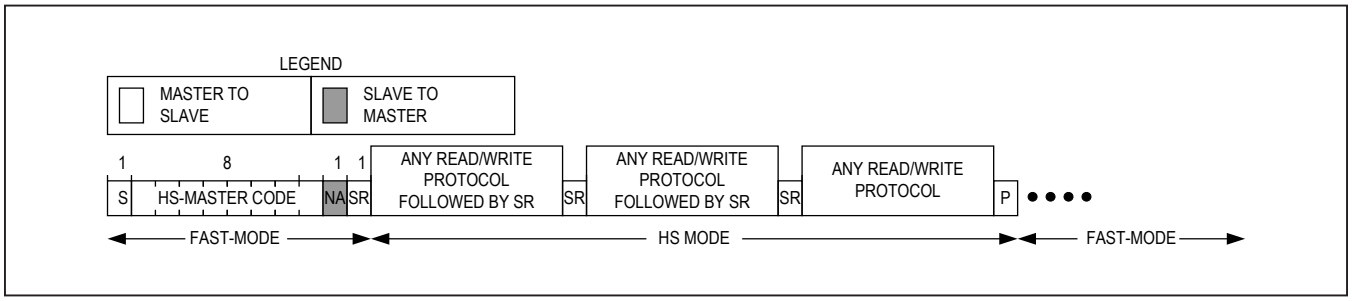



*Figure 14. Engaging HS Mode*

## Register Map

I2C Slave Address (W/R): 0x30/0x31 (default)

| ADDRESS | REGISTER NAME | RESET TYPE | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | DEVICE_ID | TypeO | R | RESERVED | VERSION[3:0] | | | | CHIP_REV[2:0] | | | — |
| 0x01 | STATUS | TypeO | R | RESERVED | RESERVED | RESERVED | RESERVED | TSHDN | BB_POKn | BB_OVP | BB_OCP | — |
| 0x02 | CONFIG1 | TypeO | R/W | RESERVED | RESERVED | BB_RU_SR | BB_RD_SR | BB_OVP_TH[1:0] | | BB_AD | BB_FPWM | 0x0E |
| 0x03 | CONFIG2 | TypeO | R/W | RESERVED | BB_EN | EN_PD | POK_POL | RESERVED | RESERVED | RESERVED | RESERVED | 0x70 |
| 0x04 | VOUT_DVS_L | TypeO | R/W | RESERVED | VOUT_DVS_L[6:0] | | | | | | | 0x38 |
| 0x05 | VOUT_DVS_H | TypeO | R/W | RESERVED | VOUT_DVS_H[6:0] | | | | | | | 0x40 |
| 0x09–0xFF | RESERVED | | | | | | | | | | | |

## DEVICE_ID

Device ID Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: N/A |
|---|---|---|---|---|
| 0x00 | R | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | RESERVED | 0 | | |
| 6:3 | VERSION[3:0] | — | Version<br>0000b: Plain<br>0001b: -1Z<br>0010b: -2Z | |
| 2:0 | CHIP_REV[2:0] | — | Chip revision history<br>001b: PASS1<br>010b: PASS2<br>011b: PASS3<br>and so on | |

## STATUS

Status Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: N/A |
|---|---|---|---|---|
| 0x01 | R | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:4 | RESERVED | — | | |
| 3 | TSHDN | — | 0: Junction Temperature (TJCT) ≤ 165°C<br>1: Junction Temperature (TJCT) > 165°C | |
| 2 | BB_POKn | — | Buck-boost $\overline{\text{POK}}$ Status | |
| 1 | BB_OVP | — | Buck-boost OVP Status | |
| 0 | BB_OCP | — | Buck-boost OCP Status | |

## CONFIG1

Configuration Register1

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x0E |
|---|---|---|---|---|
| 0x02 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:6 | RESERVED | 00 | | |
| 5 | BB_RU_SR | 0 | **Rising Ramp-Rate Control**<br>0: 12.5mV/µs<br>1: 25mV/µs | |
| 4 | BB_RD_SR | 0 | **Ramp-Down Slew Rate Control**<br>0: 3.125mV/µs<br>1: 6.25mV/µs | |
| 3:2 | BB_OVP_TH[1:0] | 11 | **Output OVP Threshold**<br>00b: No OVP<br>01b: 110% of VOUT<br>10b: 115% of VOUT<br>11b: 120% of VOUT | |
| 1 | BB_AD | 1 | **Output Active Discharge**<br>0: Disable Active Discharge<br>1: Enable Active Discharge | |
| 0 | BB_FPWM | 0 | **Forced PWM Enable**<br>0: SKIP Mode<br>1: Forced PWM | |

## CONFIG2

Configuration Register2

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x70 |
|---|---|---|---|---|
| 0x03 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | RESERVED | 0 | | |
| 6 | BB_EN | 1 | 0: Disable buck-boost output<br>1: Enable buck-boost output | |
| 5 | EN_PD | 1 | **EN Input Pulldown Resistor Enable Setting**<br>0: Disable<br>1: Enable | |
| 4 | POK_POL | 1 | 0: Active low<br>1: Active high | |
| 3:0 | RESERVED | 0000 | | |

## VOUT_DVS_L

Output Voltage Setting Register when DVS = low

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x38 | | |
|---|---|---|---|---|---|---|
| 0x04 | R/W | | | | | |
| BIT | NAME | POR | DESCRIPTION | | | |
| 7 | RESERVED | 0 | | | | |
| 6:0 | VOUT_DVS_L[6:0] | 011 1000 | **Buck-Boost Output Voltage** | | | |
| | | | 0x00 = 2.6000V | 0x20 = 3.0000V | 0x40 = 3.4000V | 0x60 = 3.8000V |
| | | | 0x01 = 2.6125V | 0x21 = 3.0125V | 0x41 = 3.4125V | 0x61 = 3.8125V |
| | | | 0x02 = 2.6250V | 0x22 = 3.0250V | 0x42 = 3.4250V | 0x62 = 3.8250V |
| | | | 0x03 = 2.6375V | 0x23 = 3.0375V | 0x43 = 3.4375V | 0x63 = 3.8375V |
| | | | 0x04 = 2.6500V | 0x24 = 3.0500V | 0x44 = 3.4500V | 0x64 = 3.8500V |
| | | | 0x05 = 2.6625V | 0x25 = 3.0625V | 0x45 = 3.4625V | 0x65 = 3.8625V |
| | | | 0x06 = 2.6750V | 0x26 = 3.0750V | 0x46 = 3.4750V | 0x66 = 3.8750V |
| | | | 0x07 = 2.6875V | 0x27 = 3.0875V | 0x47 = 3.4875V | 0x67 = 3.8875V |
| | | | 0x08 = 2.7000V | 0x28 = 3.1000V | 0x48 = 3.5000V | 0x68 = 3.9000V |
| | | | 0x09 = 2.7125V | 0x29 = 3.1125V | 0x49 = 3.5125V | 0x69 = 3.9125V |
| | | | 0x0A = 2.7250V | 0x2A = 3.1250V | 0x4A = 3.5250V | 0x6A = 3.9250V |
| | | | 0x0B = 2.7375V | 0x2B = 3.1375V | 0x4B = 3.5375V | 0x6B = 3.9375V |
| | | | 0x0C = 2.7500V | 0x2C = 3.1500V | 0x4C = 3.5500V | 0x6C = 3.9500V |
| | | | 0x0D = 2.7625V | 0x2D = 3.1625V | 0x4D = 3.5625V | 0x6D = 3.9625V |
| | | | 0x0E = 2.7750V | 0x2E = 3.1750V | 0x4E = 3.5750V | 0x6E = 3.9750V |
| | | | 0x0F = 2.7875V | 0x2F = 3.1875V | 0x4F = 3.5875V | 0x6F = 3.9875V |
| | | | 0x10 = 2.8000V | 0x30 = 3.2000V | 0x50 = 3.6000V | 0x70 = 4.0000V |
| | | | 0x11 = 2.8125V | 0x31 = 3.2125V | 0x51 = 3.6125V | 0x71 = 4.0125V |
| | | | 0x12 = 2.8250V | 0x32 = 3.2250V | 0x52 = 3.6250V | 0x72 = 4.0250V |
| | | | 0x13 = 2.8375V | 0x33 = 3.2375V | 0x53 = 3.6375V | 0x73 = 4.0375V |
| | | | 0x14 = 2.8500V | 0x34 = 3.2500V | 0x54 = 3.6500V | 0x74 = 4.0500V |
| | | | 0x15 = 2.8625V | 0x35 = 3.2625V | 0x55 = 3.6625V | 0x75 = 4.0625V |
| | | | 0x16 = 2.8750V | 0x36 = 3.2750V | 0x56 = 3.6750V | 0x76 = 4.0750V |
| | | | 0x17 = 2.8875V | 0x37 = 3.2875V | 0x57 = 3.6875V | 0x77 = 4.0875V |
| | | | 0x18 = 2.9000V | **0x38 = 3.3000V** | 0x58 = 3.7000V | 0x78 = 4.1000V |
| | | | 0x19 = 2.9125V | 0x39 = 3.3125V | 0x59 = 3.7125V | 0x79 = 4.1125V |
| | | | 0x1A = 2.9250V | 0x3A = 3.3250V | 0x5A = 3.7250V | 0x7A = 4.1250V |
| | | | 0x1B = 2.9375V | 0x3B= 3.3375V | 0x5B = 3.7375V | 0x7B = 4.1375V |
| | | | 0x1C = 2.9500V | 0x3C = 3.3500V | 0x5C = 3.7500V | 0x7C = 4.1500V |
| | | | 0x1D = 2.9625V | 0x3D = 3.3625V | 0x5D = 3.7625V | 0x7D = 4.1625V |
| | | | 0x1E = 2.9750V | 0x3E = 3.3750V | 0x5E = 3.7750V | 0x7E = 4.1750V |
| | | | 0x1F = 2.9875V | 0x3F = 3.3875V | 0x5F = 3.7875V | 0x7F = 4.1875V |

## VOUT_DVS_H

Output Voltage Setting Register when DVS = high

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x40 | | |
|---|---|---|---|---|---|---|
| 0x05 | R/W | | | | | |
| BIT | NAME | POR | DESCRIPTION | | | |
| 7 | RESERVED | 0 | | | | |
| 6:0 | VOUT_DVS_H[6:0] | 011 1000 | **Buck-Boost Output Voltage** | | | |
| | | | 0x00 = 2.6000V | 0x20 = 3.0000V | **0x40 = 3.4000V** | 0x60 = 3.8000V |
| | | | 0x01 = 2.6125V | 0x21 = 3.0125V | 0x41 = 3.4125V | 0x61 = 3.8125V |
| | | | 0x02 = 2.6250V | 0x22 = 3.0250V | 0x42 = 3.4250V | 0x62 = 3.8250V |
| | | | 0x03 = 2.6375V | 0x23 = 3.0375V | 0x43 = 3.4375V | 0x63 = 3.8375V |
| | | | 0x04 = 2.6500V | 0x24 = 3.0500V | 0x44 = 3.4500V | 0x64 = 3.8500V |
| | | | 0x05 = 2.6625V | 0x25 = 3.0625V | 0x45 = 3.4625V | 0x65 = 3.8625V |
| | | | 0x06 = 2.6750V | 0x26 = 3.0750V | 0x46 = 3.4750V | 0x66 = 3.8750V |
| | | | 0x07 = 2.6875V | 0x27 = 3.0875V | 0x47 = 3.4875V | 0x67 = 3.8875V |
| | | | 0x08 = 2.7000V | 0x28 = 3.1000V | 0x48 = 3.5000V | 0x68 = 3.9000V |
| | | | 0x09 = 2.7125V | 0x29 = 3.1125V | 0x49 = 3.5125V | 0x69 = 3.9125V |
| | | | 0x0A = 2.7250V | 0x2A = 3.1250V | 0x4A = 3.5250V | 0x6A = 3.9250V |
| | | | 0x0B = 2.7375V | 0x2B = 3.1375V | 0x4B = 3.5375V | 0x6B = 3.9375V |
| | | | 0x0C = 2.7500V | 0x2C = 3.1500V | 0x4C = 3.5500V | 0x6C = 3.9500V |
| | | | 0x0D = 2.7625V | 0x2D = 3.1625V | 0x4D = 3.5625V | 0x6D = 3.9625V |
| | | | 0x0E = 2.7750V | 0x2E = 3.1750V | 0x4E = 3.5750V | 0x6E= 3.9750V |
| | | | 0x0F = 2.7875V | 0x2F = 3.1875V | 0x4F = 3.5875V | 0x6F = 3.9875V |
| | | | 0x10 = 2.8000V | 0x30 = 3.2000V | 0x50 = 3.6000V | 0x70 = 4.0000V |
| | | | 0x11 = 2.8125V | 0x31 = 3.2125V | 0x51 = 3.6125V | 0x71 = 4.0125V |
| | | | 0x12 = 2.8250V | 0x32 = 3.2250V | 0x52 = 3.6250V | 0x72 = 4.0250V |
| | | | 0x13 = 2.8375V | 0x33 = 3.2375V | 0x53 = 3.6375V | 0x73 = 4.0375V |
| | | | 0x14 = 2.8500V | 0x34 = 3.2500V | 0x54 = 3.6500V | 0x74 = 4.0500V |
| | | | 0x15 = 2.8625V | 0x35 = 3.2625V | 0x55 = 3.6625V | 0x75 = 4.0625V |
| | | | 0x16 = 2.8750V | 0x36 = 3.2750V | 0x56 = 3.6750V | 0x76 = 4.0750V |
| | | | 0x17 = 2.8875V | 0x37 = 3.2875V | 0x57 = 3.6875V | 0x77 = 4.0875V |
| | | | 0x18 = 2.9000V | 0x38 = 3.3000V | 0x58 = 3.7000V | 0x78 = 4.1000V |
| | | | 0x19 = 2.9125V | 0x39 = 3.3125V | 0x59 = 3.7125V | 0x79 = 4.1125V |
| | | | 0x1A = 2.9250V | 0x3A = 3.3250V | 0x5A = 3.7250V | 0x7A = 4.1250V |
| | | | 0x1B = 2.9375V | 0x3B = 3.3375V | 0x5B = 3.7375V | 0x7B = 4.1375V |
| | | | 0x1C = 2.9500V | 0x3C = 3.3500V | 0x5C = 3.7500V | 0x7C = 4.1500V |
| | | | 0x1D = 2.9625V | 0x3D = 3.3625V | 0x5D = 3.7625V | 0x7D = 4.1625V |
| | | | 0x1E = 2.9750V | 0x3E = 3.3750V | 0x5E = 3.7750V | 0x7E = 4.1750V |
| | | | 0x1F = 2.9875V | 0x3F = 3.3875V | 0x5F = 3.7875V | 0x7F = 4.1875V |

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX77801EWP+T | -40°C to 85°C | 20 WLP<br>(5 x 4) 0.4mm Pitch |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

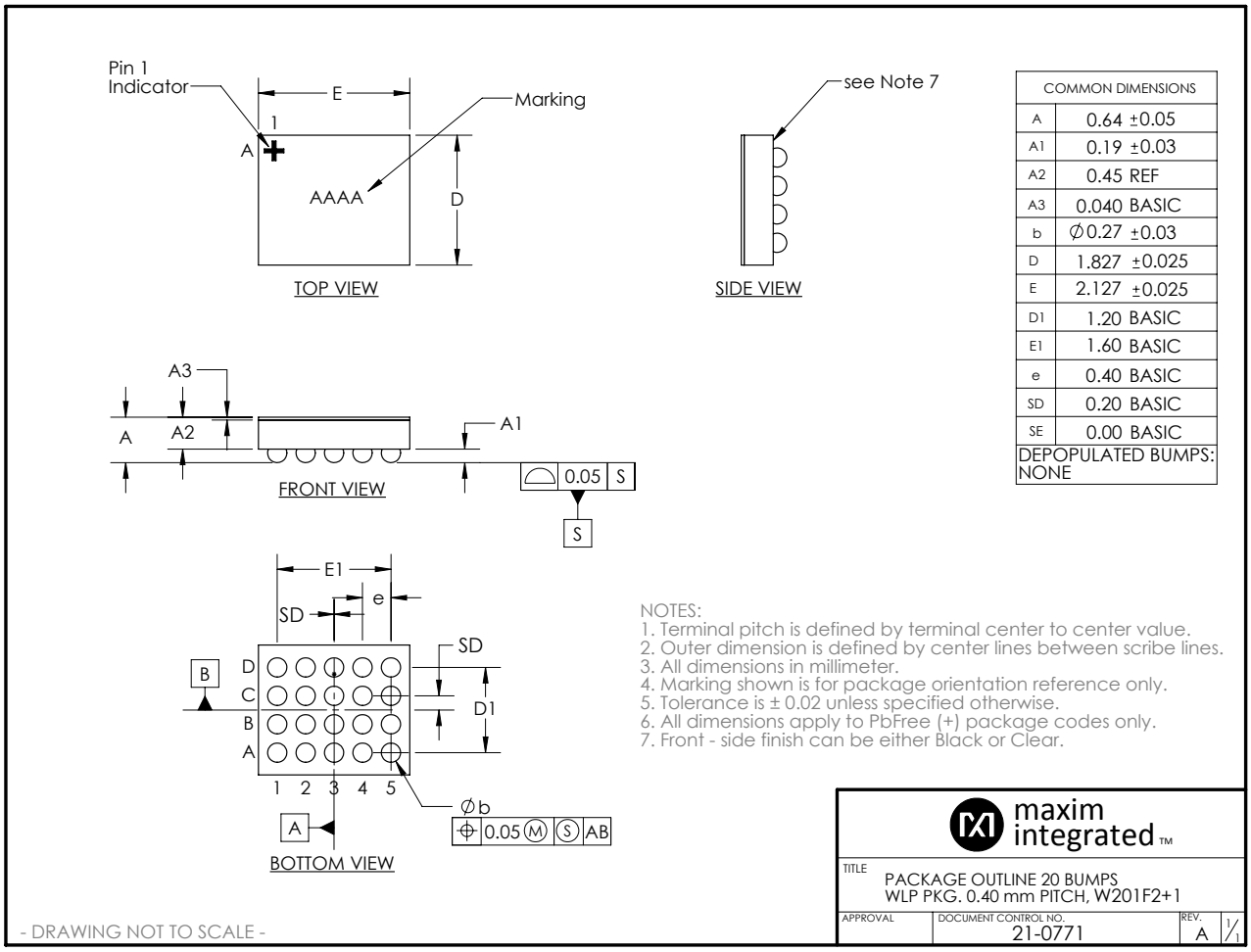
## Chip Information

PROCESS: S18B

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 20 WLP | W201F2+1 | 21-0771 | Refer to Application Note 1891 |



## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 2/15 | Initial release | — |

# OCEAN CHIPS
## Океан Электроники
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Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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