

### Description

The 5P35021 is the latest VersaClock programmable clock generator and is designed for low-power, consumer, and high-performance PCI Express applications. The 5P35021 device is a 3 PLLs architecture design; each PLL is individually programmable and allows up to 3 unique frequency outputs.

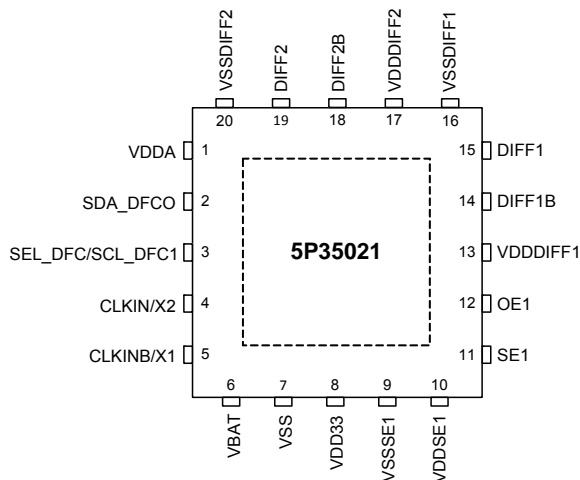
The 5P35021 has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT) and extreme low power DCO. An internal OTP memory allows the user to store the configuration in the device. After power up, the user can change the device register settings through the I<sup>2</sup>C interface when I<sup>2</sup>C mode is selected. It also has programmable VCO and PLL source selection to allow the user to do power-performance optimization based on the application requirements.

The device provides one single-ended output and two pairs of differential outputs that support LVCMOS, LVPECL, LVDS and LPHCSL. The low power 32.768kHz clock is supported with only less than 2μA current consumption for system RTC reference clock.

### Typical Applications

- PCIe Gen1/2/3 clock generator
- Consumer application crystal replacements
- SmartDevice, Handheld, Computing and Consumer applications

### Pin Assignment



### Features

- Configurable OE pin function as OE, PD#, PPS or DFC control function
- Configurable PLL bandwidth/minimizes jitter peaking
- PPS: Proactive Power Saving features save power during the end device power down mode
- PPB: Performance- Power Balancing feature allow user to minimum power consumption base on required performance
- DFC: Dynamic Frequency Control feature allows user to program up to 4 difference frequencies and switch dynamically
- Spread spectrum clock support to lower system EMI
- Store user configuration into OTP memory
- I<sup>2</sup>C interface

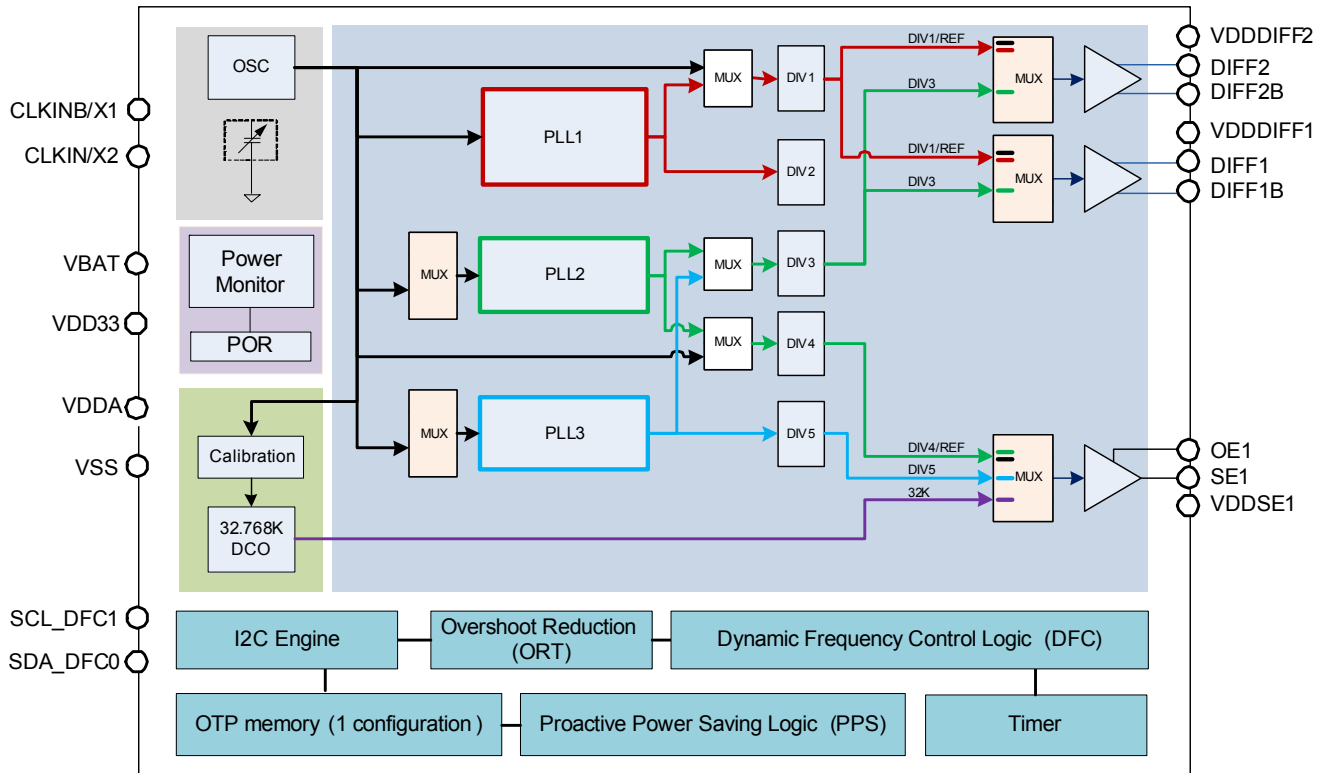
### Key Specifications

- PCIe clocks phase jitter: PCIe Gen3
- Differential clocks < 3 ps rms jitter integer range 12kHz–20MHz
- < 2μA DCO to generate 32.768kHz clock

### Output Features

- 2 DIFF outputs with configurable LPHSCL, LVDS, LVPECL, LVCMOS output pairs. 1MHz–500MHz (160MHz/ with LVCMOS mode)
- 1 LVCMOS output: 1MHz–160MHz
- Maximum 5 LVCMOS outputs as 1 × SE + 2 × DIFF\_T/C as LVCMOS
- Low Power 32.768kHz clock supported on SE1

## Functional Block Diagram



## Power Group

| Power supply table | SE     | DIFF  | DIV    | MUX     | PLL  | DCO | REF | Xtal |
|--------------------|--------|-------|--------|---------|------|-----|-----|------|
|                    | VDDSE1 | SE1   |        |         |      |     |     |      |
| VDDDIFF1           |        | DIFF1 | DIV3/4 | MUXPLL2 | PLL2 |     |     |      |
| VDDDIFF2           |        | DIFF2 | DIV1   | MUXPLL1 |      |     |     |      |
| VDD33              |        |       | DIV5   |         | PLL3 | DCO | REF | Xtal |
| VBAT               |        |       |        |         |      | DCO |     | Xtal |
| VDDA               |        |       | DIV2   |         | PLL1 |     |     |      |

\* VDDSEx for non-32kHz outputs should be OFF when VDDA/VDD3 turn OFF, VBAT mode only support 32.768kHz outputs from SE1-3.

\* VBAT power ramp up should be same or earlier than other VDD power rail.

## Output Source Table

| Source:   | Outputs:  |          |          |
|-----------|-----------|----------|----------|
|           | SE1       | DIFF1    | DIFF2    |
| Xtal REF  | Xtal REF  | Xtal REF | Xtal REF |
| 32.768kHz | 32.768kHz |          |          |
| PLL1      |           | PLL1     | PLL1     |
| PLL2      |           | PLL2     | PLL2     |
| PLL3      |           | PLL3     | PLL3     |

## Output Source Selection Register Setting Table

| SE1                   | B36<4> | B36<3> | B31<1> | B29<3> |
|-----------------------|--------|--------|--------|--------|
| From 32K              | 0      | 1      | 0      | 0      |
| From PLL3 + Divider 5 | 1      | 0      | 0      | 0      |
| From PLL2 + Divider 4 | 1      | 1      | 1      | 0      |
| From REF + Divider 4  | 1      | 1      | 0      | 1      |

| DIFF1                 | B34<7> | B0<3> |
|-----------------------|--------|-------|
| From PLL1 + Divider 1 | 0      | 0     |
| From PLL2 + Divider 3 | 1      | 0     |
| From REF + Divider 1  | 0      | 1     |

| DIFF2                 | B35<7> | B0<3> |
|-----------------------|--------|-------|
| From PLL1 + Divider 1 | 0      | 0     |
| From PLL2 + Divider 3 | 1      | 0     |
| From REF + Divider 1  | 0      | 1     |

## Glossary of Features

| Term      | Function Description   | Apply to  |
|-----------|--|-----------|
| DFC       | Dynamic Frequency Control, from selected PLL to support four VCO frequencies, means two different output frequencies by assign H/W pin state changes.  | PLL2      |
| ORT       | Overshoot Reduction, when the DFC dynamic frequency change is functional, the VCO change frequency smoothly to target frequency without overshoot or under shoot.  | PLL2      |
| OE        | Output Enable function, each output can be controlled by assigned OE pin, the dedicated OE pin can be OTP programmable as Global Power Down function (PD#) or Output enable (OE) or proactive power saving function (PPS) or RESET pin function. | OE1       |
| SS        | Spread spectrum clock.   | PLL1/PLL2 |
| Slew Rate | LVC MOS outputs with slew rate control - slow and fast.  | LVC MOS   |
| PPS       | Proactive Power Saving, utilize OE pin as monitor pin for end device X2 clock status, details see PPS function .description  | SE1       |

## Pin Descriptions

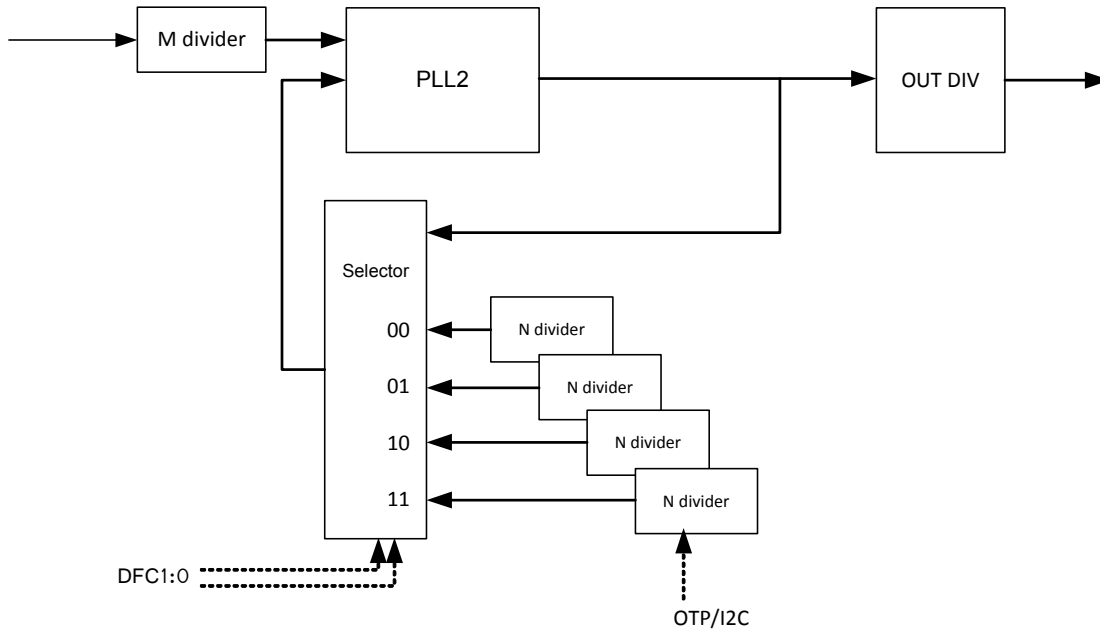
| Number | Name             | Type   | Description  |
|--------|------------------|--------|--|
| 1      | VDDA             | Power  | VDD 3.3V.  |
| 2      | SDA_DFC0         | I/O    | I2C DATA pin, can be setup become DFC0 by OTP programming.   |
| 3      | SEL_DFC/SCL_DFC1 | Input  | I2C CLK pin,<br>SEL_DFC is a latch input pin during the power up<br>High on power on: I2C mode as SCLK function,<br>Low on power on: SCL and SDA as DFC function pins. |
| 4      | CLKIN/X2         | I/O    | Crystal oscillator interface output or differential clock input pin (CLKIN).   |
| 5      | CLKINB/X1        | Input  | Crystal oscillator interface input or differential clock input pin (CLKINB).   |
| 6      | VBAT             | Power  | Power supply pin for 32.768kHz DCO, usually connect to coin cell battery, 2.5-3.3V.  |
| 7      | VSS              | Power  | Connect to ground.   |
| 8      | VDD33            | Power  | VDD 3.3V.  |
| 9      | VSSSE1           | Power  | Connect to ground.   |
| 10     | VDDSE1           | Power  | Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for SE1.   |
| 11     | SE1              | Output | Output Clock SE1.  |
| 12     | OE1              | Input  | OE1's function selected from OTP preprogram register bits.<br>OE1 pull-up to 6.5V when burn OTP registers.<br>Refer to OE function table for details.                  |
| 13     | VDDDIFF1         | Power  | Output power supply. Connect to 2.5 to 3.3V. Sets output voltage levels for DIFF1.   |
| 14     | DIFF1B           | Output | Differential clock output 1_Complement, can be OTP pre-program to LVCMOS/LPHCSL/LVDS/LVPECL output type.   |
| 15     | DIFF1            | Output | Differential clock output 1_True, can be OTP pre-program to LVCMOS/LPHCSL/LVDS/LVPECL output type.   |
| 16     | VSSDIFF1         | Power  | Connect to ground.   |
| 17     | VDDDIFF2         | Power  | Output power supply. Connect to 2.5 to 3.3V. Sets output voltage levels for DIFF2.   |
| 18     | DIFF2B           | Output | Differential clock output 2_Complement, can be OTP pre-program to LVCMOS/LPHCSL/LVDS/LVPECL output type.   |
| 19     | DIFF2            | Output | Differential clock output 2_True, can be OTP pre-program to LVCMOS/LPHCSL/LVDS/LVPECL output type.   |
| 20     | VSSDIFF2         | Power  | Connect to ground.   |
| 21     | EPAD             | Power  | Connect to ground.   |

## Device Feature and Function

### DFC–Dynamic Frequency Control

- OTP program (Only) setup 4 different feedback fractional divider (4 VCO frequencies) that apply to PLL2
- ORT (overshoot reduction) function will be applied automatically during the VCO frequency change
- Smooth frequency incremental or decremental from current VCO to targeted VCO base on DFC hardware pins selection

### DFC Block Diagram



### DFC Function Priority Table

| DFC_EN bit(W32[4]) | OE1_fun_sel (W30[6:5]) | *OE3_fun_sel (W30[3:2]) | SCL_DFC1 | DFC[1:0]             | Notes                            |
|--------------------|------------------------|-------------------------|----------|----------------------|----------------------------------|
| 0                  | x                      | x                       | x        | 0                    | DFC disable                      |
| 1                  | 11 (DFC)               | 00-10 (DFC)             | x        | [0,OE1]              | One pin DFC - OE1                |
| 1                  | 11 (DFC)               | 11 (DFC)                | x        | [OE3,OE1]            | Two pin DFC - OE3,OE1            |
| 1                  | 00-10                  | 11                      | x        | Not permit           | Not supported                    |
| 1                  | 00-10                  | 00-10                   | 0        | [SCL_DFC1, SDA_DFC0] | I2C pin as DFC control pins mode |
| 1                  | 00-10                  | 00-10                   | 1        | W30[1:0]             | I2C control DFC mode             |

\* 5P35021 has only OE1 pin for DFC function hardware pin selection. For OE1/OE3 two pins DFC control, use 5P35023 24-QFN package device.

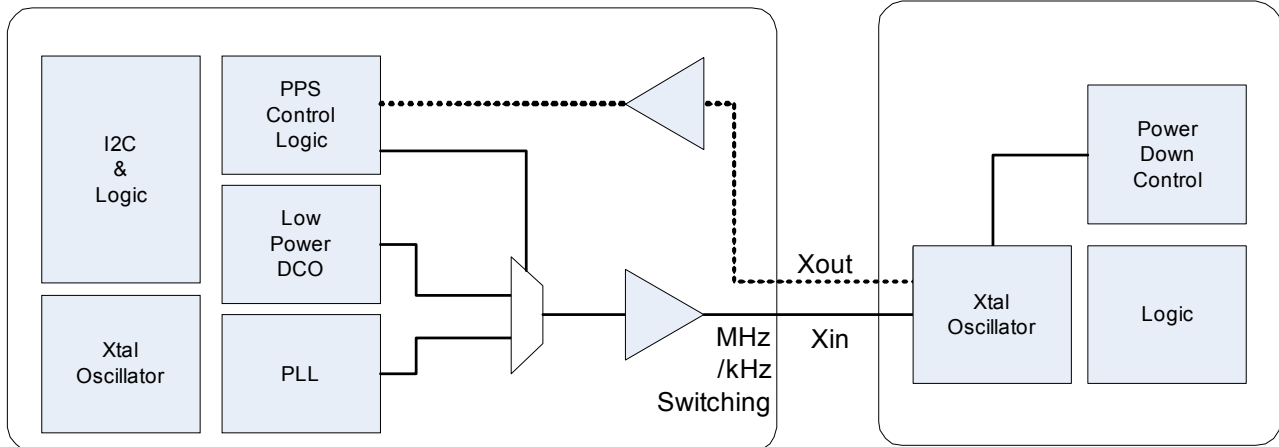
### DFC Function Programming

- Register B63b3:2 select DFC00–DFC11 configuration.
- Byte16–19 are the register for PLL2 VCO setting, base on B63b3:2 configuration selection, the data write to B16–19 will be store in selected configuration OTP memory.
- Refer to DFC function priority table, select proper control pin(s) to activate DFC function.
- Note the DFC function can also be controlled by I<sup>2</sup>C access.

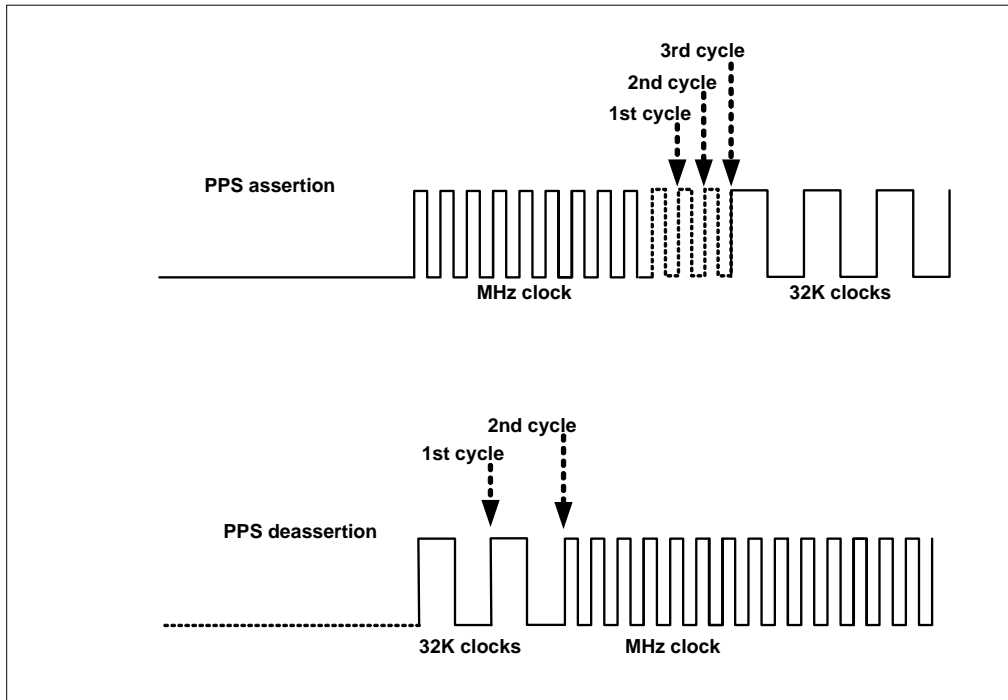
## PPS—Proactive Power Saving Function

PPS Proactive Power Saving is an IDT patented unique design for the clock generator that proactively detects end device power down state and then switches output clocks between the normal operation clock frequency and the low power mode 32kHz clock that only consume  $< 2\mu\text{A}$  current. The system could save power when the device goes into power down or sleep mode. The PPS function diagram is shown below.

### PPS Function Block Diagram



### PPS Assertion/Deassertion Timing Chart

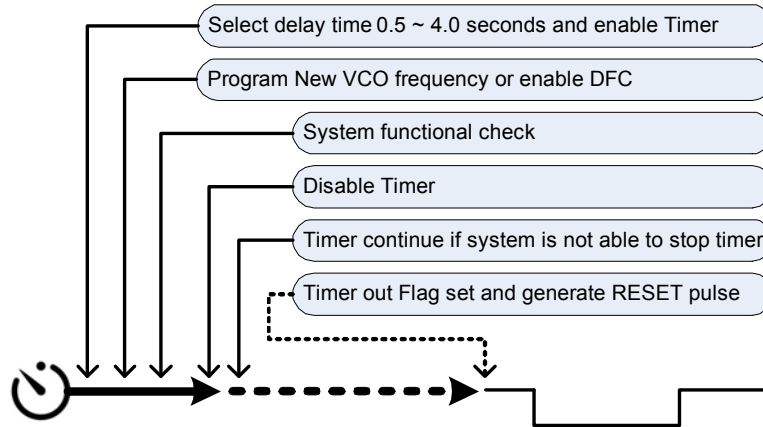


### PPS Function Programming

- Refer to OE\_pin\_function\_table to have proper PPS function selected for OE pin(s), please note that register default is set to Output enable (OE).
- Have proper setup to Byte 30 and 32 for OE1~OE3 function selection, for PPS function, select 10 to control register bits.

## Timer Function Description

1. The timer function can be used together with the DFC (Dynamic Frequency Control) function or with another PLL frequency programming.
2. The timer provides 4 different delay times by two bits selection: 0.5 seconds, 1 seconds, 2 seconds, 4 seconds.
3. The timeout flag will be set when timer times out, and the flag can be cleared by writing 0 to timer enable bit.
4. When timer times out, RESET pin (available in 5P35023) can generate a 250ms pulse signal if RESET control bit is enabled.
5. When timer times out, DFC stage will switch back to DFC00 setting if DFC function is enabled and DFC function will be disabled after RESET.



## OE Pin Function

OE pins in the 5P35021 have multiple functions. The OE pins can be configured as output enable control (OE) or chip power down control (PD#) or Proactive Power Saving function (PPS). Furthermore, the OE pins can be configured as single or two pin dynamic Frequency control (DFC), or the RESET out function that is associated with the Timer function.

### OE Pin Function Table

| Function                     | Pin           |                                |                                |
|------------------------------|---------------|--------------------------------|--------------------------------|
|                              | OE1           | OE2 (Not available in 5P35021) | OE3 (Not available in 5P35021) |
| SE Output Enable/Disable     | SE1 (Default) | SE2 (Default)                  | SE3 (Default)                  |
| DIFF Output Enable/Disable   | -             | DIFF1/DIFF2                    | -                              |
| Global Power Down (PD#)      | PD#           | -                              | -                              |
| Proactive Power Saving Input | SE1_PPS       | SE2_PPS                        | SE3_PPS                        |
| DOC Control (Only PLL2)      | DFC0          | -                              | DFC1                           |
| RESET OUT                    | -             | RESET OUT                      | -                              |

## OE Pin Function Summary (\* Note: OE2, OE3 and SE2, SE3 pins are only available in 5P35023)

|                    |   |
|--------------------|---|
| OE1: SE1           | OE1 only control SE1 enable/disable, other outputs are not affected by this pin status              |
| * OE2: SE2         | OE2 only control SE2 enable/disable, other outputs are not affected by this pin status              |
| * OE2: SE3         | OE3 only control SE3 enable/disable, other outputs are not affected by this pin status              |
| * OE2: DIFF1/DIFF2 | OE2 control Differential outputs 1 and 2 only, other SE outputs are not affected by this pin status |
| OE1: PD#           | OE1 control chip global power down (PD#) except 32.768KHz on OE1 (when 32K is enabled),             |
| OE1: SE1_PPS       | Config OE1 as SE1_PPS (Proactive Power Saving) function pin   |
| * OE1: SE2_PPS     | Config OE2 as SE2_PPS (Proactive Power Saving) function pin   |
| * OE1: SE3_PPS     | Config OE3 as SE3_PPS (Proactive Power Saving) function pin   |
| OE1:DFC0           | Config OE1 as DFC0 control pin0   |
| * OE3/DFC1         | Config OE3 as DFC1 control pin1   |

## PD# Priority Table

| PD# | I2C_OE_EN_bit | SE1, DIFF1/DIFF2<br>SE1_PPS | Output  | Notes          |
|-----|---------------|-----------------------------|---------|----------------|
| 0   | x             | x                           | stop    | 32kHz free run |
| 1   | 0             | x                           | stop    |                |
| 1   | 1             | 0                           | stop    |                |
| 1   | 1             | 1                           | running |                |

## Reference Input and Selection

The 5P35021 accepts crystal input or LVCMOS/Differential clocks input by external AC coupling. See below reference circuit for details.

### Crystal Input (X1/X2)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 40MHz maximum.

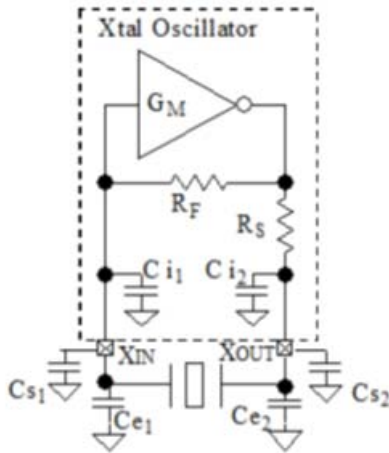
A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate as 0 PPM. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal. In order to get an accurate oscillation frequency, the matching the oscillator load capacitance with the crystal load capacitance is required.

To set the oscillator load capacitance, 5P35021 has built-in two programmable tuning capacitors inside the chip, one at XIN and one at XOUT. They can be adjusted independently. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[7:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.



## Programmable Tuning Caps Table

| Parameter  | Bits | Range          | Min (pF) | Max (pF) |
|------------|------|----------------|----------|----------|
| Xtal [7:0] | 4*2  | +1/+2/+4/+8 pF | 0        | 15pF     |



$$XTAL[4:0] = (XTAL CL - 7pF) \times 2 \quad (\text{Eq.1})$$

Equation 1 and the table of XTAL[7:0] tuning capacitor characteristics show that the parallel tuning capacitance can be set between 4.5pF to 12.5pF with a resolution of 0.25pF.

For a crystal  $C_L = 8pF$ , where  $C_L$  is the parallel capacity specified by the crystal vendor that sets the crystal frequency to the nominal value. Under the assumptions that the stray capacity between the crystal leads on the circuit board is zero and that no external tuning caps are placed on the crystal leads, then the internal parallel tuning capacity is equal to the load capacity presented to the crystal by the device.

The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements.

## Spread Spectrum

The 5P35021 supports spread spectrum clocks from PLL1 and PLL2; the PLL1 built-in with analog spread spectrum and PLL2 has digital spread spectrum.

### Analog Spread Spectrum

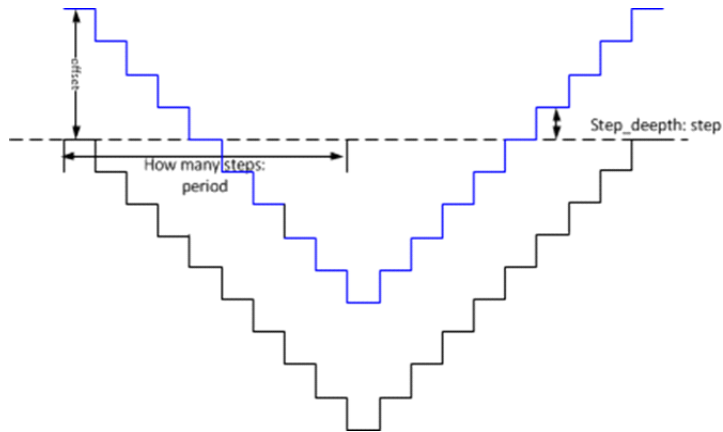
Please refer to programming guide.

## Digital Spread Spectrum

$$N = \frac{F_{vco}}{2 * F_{out}}$$

$$period = \frac{F_{pfd}}{2 * F_{ss}}$$

$$step = \frac{N * SS_{amount}}{period}$$



### Down spread or Spread off

$$N = F_{vco}/F_{pfd}$$

### Center Spread

$$N = N_{soff} + N * SS_{amount}/2$$

N: include integer and fraction

F<sub>vco</sub>: vco's frequency

F<sub>pfd</sub>: PLL's pfd frequency

F<sub>ss</sub>: spread modulation rate

SS<sub>amount</sub>: spread percentage

The black line is for the down spread, N will decrease to make the center frequency is lower than spread off.

The blue line is for the center spread, there is a offset put on divider ratio to make the center frequency keep same as spread off.

Example: 0.5% down spread at 32kHz modulation rate.

## VBAT

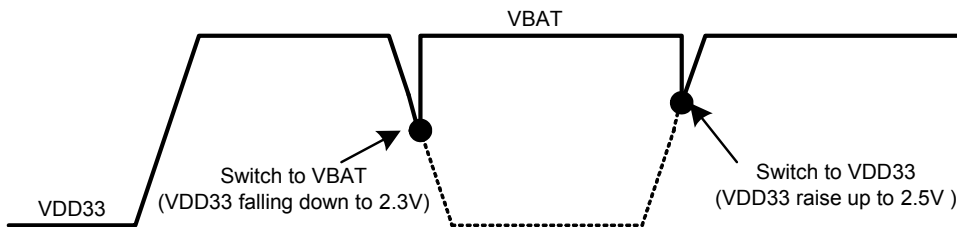
The 5P35021 supports low-power operation 32.768kHz RTC clock with only coin cell battery supply. The coin cell battery power capacitance is usually 170mAh or higher, with less than 2 $\mu$ A\* low-power DCO operation mode will support application up to few years clock source for date/time keeping circuit (RTC).

When there is main power exist like  $V_{DD33}$  and  $V_{DDA}$ , the 5P35021 will switch DCO power source to main power to save battery power.  $V_{BAT}$  should be powered earlier or at same time with other  $V_{DD}$  power up.

### VBAT Switching Threshold

| VDD33 | VBAT | DCO power source |
|-------|------|------------------|
| >2.5V | --   | VDD33            |
| <2.3V | --   | VBAT             |

\*VBAT needs to be 3.0V~3.3V



## ORT-VCO Overshoot Reduction Technology

The 5P35021 supports innovate the VCO overshoot reduction technology (ORT) to prevent an output clock frequency spike when the device is changing frequency on the fly or doing DFC (Dynamic Frequency Control) function. The VCO frequency changes are under control instead of free-run to targeted frequency.

## PLL Features and Descriptions

Output divider 1 table

Output Divider bits<3:2>

| Output Divider bits<1:0> | 00 | 01 | 10 | 11 |
|--------------------------|----|----|----|----|
| 00                       | 1  | 2  | 4  | 8  |
| 01                       | 4  | 8  | 16 | 32 |
| 10                       | 5  | 10 | 20 | 40 |
| 11                       | 6  | 12 | 24 | 48 |

Output 2,4,5 divider table

Output Divider bits<3:2>

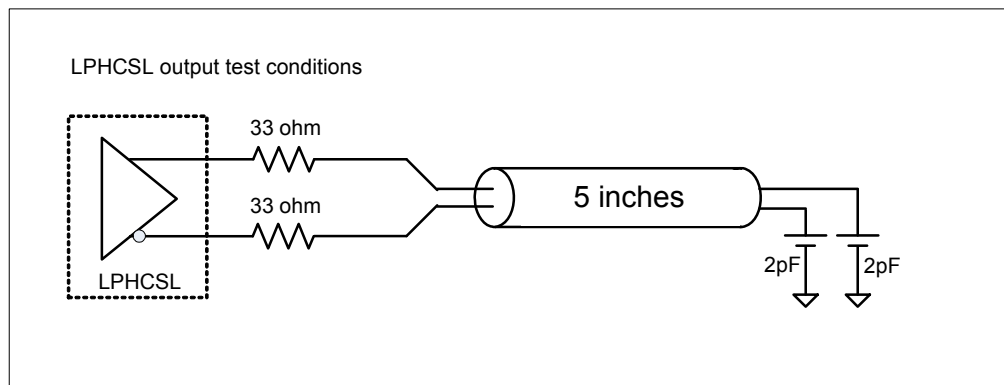
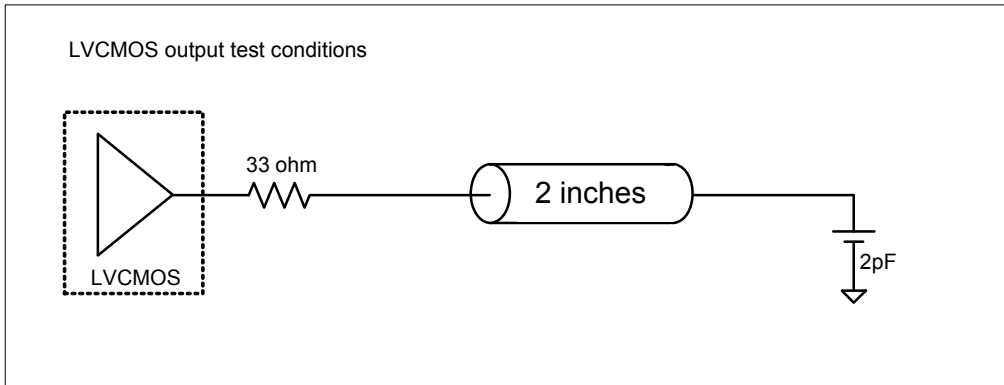
| Output Divider bits<1:0> | 00 | 01 | 10 | 11 |
|--------------------------|----|----|----|----|
| 00                       | 1  | 2  | 4  | 5  |
| 01                       | 3  | 6  | 12 | 15 |
| 10                       | 5  | 10 | 20 | 25 |
| 11                       | 10 | 20 | 40 | 50 |

Output 3 divider table

Output Divider bits<3:2>

| Output Divider bits<1:0> | 00 | 01 | 10 | 11 |
|--------------------------|----|----|----|----|
| 00                       | 1  | 2  | 4  | 8  |
| 01                       | 3  | 6  | 12 | 24 |
| 10                       | 5  | 10 | 20 | 40 |
| 11                       | 10 | 20 | 40 | 80 |

## Output Clock Test Conditions



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P35021. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item  | Rating   |
|---|--|
| Supply Voltage, VDDA, VDD33, VDDSE, VDDDIFF | 3.465V   |
| Supply Voltage, VBAT                        | 3.465V   |
| <b>Inputs</b>                               |  |
| XIN/CLKIN                                   | 0V to 3.3V voltage swing for both LVCMOS or DIFF CLK |
| Other inputs                                | -0.5V to VDD33/VDDSEx                                |
| Outputs, VDDSEx (LVCMOS)                    | -0.5V to VDDSEx/VDDDIFF+ 0.5V                        |
| Outputs, IO (SDA)                           | 10mA   |
| Package Thermal Impedance, $\Theta_{JA}$    | 42°C/W (0 mps)                                       |
| Package Thermal Impedance, $\Theta_{JC}$    | 41.8°C/W (0 mps)                                     |
| Storage Temperature, TSTG                   | -65°C to 150°C                                       |
| ESD Human Body Model,                       | 2500V  |
| ESD Charge Device Model,                    | 1000V  |
| Junction Temperature                        | 125°C  |

## Recommended Operating Conditions

| Symbol    | Parameter  | Min   | Typ  | Max   | Unit |
|-----------|--|-------|------|-------|------|
| VDDSEx    | Power supply voltage for supporting 1.8V outputs   | 1.71  | 1.8  | 1.89  | V    |
|           | Power supply voltage for supporting 2.5V outputs   | 2.375 | 2.5  | 2.625 | V    |
|           | Power supply voltage for supporting 3.3V outputs   | 3.135 | 3.3  | 3.465 | V    |
| VDD33     | Power supply voltage for core logic functions.   | 3.135 | 3.3* | 3.465 | V    |
| VDDA      | Analog power supply voltage. Use filtered analog power supply if available.                    | 2.375 |      | 3.465 | V    |
| VBAT      | Battery power supply voltage.  | 2.8*  | 3*   | 3.465 | V    |
|           | Operating temperature, ambient   | -40   |      | 85    | °C   |
| CLOAD_OUT | Maximum load capacitance (3.3V LVCMOS only)  |       | 5    |       | pF   |
| FIN       | External reference crystal   | 8     |      | 40    | MHz  |
|           | External reference crystal with DCO used   | 12    |      | 38    |      |
|           | External single-ended reference clock CLKINB   | 1     |      | 125   |      |
|           | External differential reference clock CLKIN, CLKINB  | 8     |      | 125   |      |
| tPU       | Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic), | 0.05  |      | 3     | ms   |

\* Power-up sequence conditions.

\* VDDSEx for non-32kHz outputs should be OFF when VDDA/VDD33 turn OFF, VBAT mode only support 32.768kHz outputs from SE1-3.

\* **VBAT power ramp up should be same or earlier than other VDD power rail.**

\* When use single-ended clock to CLKINB pin within differential clocking mode, CLKIN pin needs to be grounded and minimum input frequency should be higher than 8MHz.

## Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance

(TA = +25 °C)

| Symbol             | Parameter   | Min | Typ | Max | Unit |
|--------------------|---|-----|-----|-----|------|
| CIN                | Input Capacitance (CLKIN, CLKINB, OE, SDA, SCL, DFC1:0) |     | 3   | 7   | pF   |
| Pull-down Resistor | OE  |     | 200 |     | kΩ   |
| ROUT               | LVCMOS Output Driver Impedance (VDDSE = 1.8V)           |     | 22  |     |      |
|                    | LVCMOS Output Driver Impedance (VDDSE = 2.5V)           |     | 22  |     |      |
|                    | LVCMOS Output Driver Impedance (VDDSE = 3.3V)           |     | 22  |     | Ω    |
| X1, X2             | Programmable input capacitance at X1 or X2              | 0   |     | 15  | pF   |

## Crystal Characteristics

| Parameter                            | Test Conditions | Min         | Typ | Max | Units |
|--------------------------------------|-----------------|-------------|-----|-----|-------|
| Mode of Oscillation                  |                 | Fundamental |     |     |       |
| Frequency                            |                 | 8           |     | 40  | MHz   |
| Frequency when 32.768K DCO is used   |                 | 12          |     | 38  | MHz   |
| Equivalent Series Resistance (ESR)   |                 |             | 10  | 100 | Ω     |
| Shunt Capacitance                    |                 |             | 2   | 7   | pF    |
| Load Capacitance (CL)                |                 | 6           | 8   | 10  | pF    |
| Maximum Crystal Drive Level (CL=8pF) |                 |             |     | 100 | μW    |

## DC Electrical Characteristics

| Symbol                                | Parameter                    | Test Conditions   | Min | Typ | Max | Unit |
|---------------------------------------|------------------------------|---|-----|-----|-----|------|
| Iddcore                               | Core Supply Current          | VDD=VDDSE=VDD33=3.3V, Xtal=25MHz, PLL2/3 OFF, No Output - PLLs disabled |     | 5   |     | mA   |
| Idd_PLL1 <sup>3</sup>                 | PLL1 Supply Current          | VDD=VDDSE=VDD33=3.3V, Xtal=25MHz, PLL2/3 OFF, No Output - PLL1= 600MHz  |     | 13  |     | mA   |
|                                       |                              | VDD=VDDSE=VDD33=2.5V, Xtal=25MHz, PLL2/3 OFF, No Output - PLL1= 600MHz  |     | 13  |     | mA   |
| Idd_PLL2 <sup>3</sup>                 | PLL2 Supply Current          | VDD=VDDSE=VDD33=3.3V, Xtal=25MHz, PLL1/3 OFF, No Output - PLL2=1GHz     |     | 11  |     | mA   |
|                                       |                              | VDD=VDDSE=VDD33=2.5V, Xtal=25MHz, PLL1/3 OFF, No Output - PLL2=1GHz     |     | 11  |     | mA   |
| Idd_PLL3 <sup>3</sup>                 | PLL3 Supply Current          | VDD=VDDSE=VDD33=3.3V, Xtal=25MHz, PLL1/2 OFF, No Output - PLL3=480MHz   |     | 4   |     | mA   |
| Iddox                                 | Output Buffer Supply Current | LVPECL, 500MHz, 3.3V VDDDIFF (DIFF1,2)                                  |     | 39  |     | mA   |
|                                       |                              | LVPECL, 156.25MHz, 2.5V VDDDIFF (DIFF1,2)                               |     | 33  |     | mA   |
|                                       |                              | LVDS, 500MHz, 3.3V VDDDIFF (DIFF1,2)                                    |     | 13  |     | mA   |
|                                       |                              | LVDS, 250MHz, 2.5V VDDDIFF (DIFF1,2)                                    |     | 8   |     | mA   |
|                                       |                              | LPHCSL, 125MHz, 3.3V VDDDIFF, 2 pF load (DIFF1,2)                       |     | 7   |     | mA   |
|                                       |                              | LPHCSL, 100MHz, 2.5V VDDDIFF, 2 pF load (DIFF1,2)                       |     | 8   |     | mA   |
|                                       |                              | LVC MOS, 8MHz, 3.3V, VDDSE <sup>1,2</sup> (SE1)                         |     | 1   |     | mA   |
|                                       |                              | LVC MOS, 8MHz, 2.5V, VDDSE <sup>1,2</sup> (SE1)                         |     | 1   |     | mA   |
|                                       |                              | LVC MOS, 8MHz, 1.8V, VDDSE <sup>1,2</sup> (SE1)                         |     | 1   |     | mA   |
|                                       |                              | LVC MOS, 160MHz, 3.3V VDDSEx1 (SE1)                                     |     | 9.5 |     | mA   |
|                                       |                              | LVC MOS, 160MHz, 2.5V VDDSEx1,2 (SE1)                                   |     | 5.0 |     | mA   |
| LVC MOS, 160MHz, 1.8V VDDSEx1,2 (SE1) |                              | 6.0   |     | mA  |     |      |
| Iddpd                                 | Power Down Current           | PD asserted with VDDA, VDD33 and VDDSE ON, I2C programming, 32K running |     | 3.5 |     | mA   |
| Iddsuspend - VDD33                    | Iddsuspend-VBAT              | Only VBAT=3.3V and VDDSEn is powered                                    |     | 1.1 |     | μA   |
| Iddsuspend - SE n 3.3V                | Iddsuspend - VDDSE n 3.3V    | Only VBAT=3.3V and VDDSE n is powered with 3.3V                         |     | 3.4 |     | μA   |
| Iddsuspend - SE n 2.5V                | Iddsuspend - VDDSE n 2.5V    | Only VBAT =3.3V and VDDSE n is powered with 2.5V                        |     | 2.5 |     | μA   |
| Iddsuspend - SE n 1.8V                | Iddsuspend - VDDSE n 1.8V    | Only VBAT=3.3V and VDDSE n is powered with 1.8V                         |     | 1.8 |     | μA   |

1. Single CMOS driver active.

2. SE1-3 current measured with 2 inches transmission line and 2 pF load, DIFF clock current measured with 5 inches transmission line with 2 pF loads.

3. Iddcore = IddA+ IddD, no loads.

## Power Consumption of 32.768kHz Output Only Operation

Unless stated otherwise, supply voltage VDDSE = 1.8V–3.3V  $\pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Symbol   | Parameter                     | Test Conditions               | Min | Typ | Max | Unit          |
|----------|-------------------------------|-------------------------------|-----|-----|-----|---------------|
| I_VBAT   | Vbat=3.3V power input current |                               |     | 1.1 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=1.8V current           | 0.5 inch, no load, one output |     | 0.4 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=1.8V current           | 2.0 inch, no load, one output |     | 1.0 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=1.8V current           | 5.0 inch, no load, one output |     | 2.3 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=2.5V current           | 0.5 inch, no load, one output |     | 0.6 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=2.5V current           | 2.0 inch, no load, one output |     | 1.5 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=2.5V current           | 5.0 inch, no load, one output |     | 3.1 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=3.3V current           | 0.5 inch, no load, one output |     | 0.8 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=3.3V current           | 2.0 inch, no load, one output |     | 1.9 |     | $\mu\text{A}$ |
| I_VDDSEx | VDDSEx=3.3V current           | 5.0 inch, no load, one output |     | 4.2 |     | $\mu\text{A}$ |

## Electrical Characteristics – Input Parameters <sup>1,2</sup>

Unless stated otherwise, supply voltage VDDD33 = 3.3V  $\pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Symbol             | Parameter                              | Test Conditions                        | Min       | Typ | Max   | Unit          |
|--------------------|--|--|-----------|-----|-------|---------------|
| V <sub>IH</sub>    | Input High Voltage - CLKIN             | Single-ended input                     | 2.4       |     | 3.345 | V             |
| V <sub>IL</sub>    | Input Low Voltage - CLKIN              | Single-ended input                     | GND - 0.3 |     | 0.8   | V             |
| V <sub>SWING</sub> | Input Amplitude - CLKIN                | Differential Input                     | 325       |     | 3300  | mV            |
| d <sub>w</sub> /dt | Input Slew Rate - CLKIN                | Differential Input                     | 0.4       |     | 8     | V/ns          |
| V <sub>CM</sub>    | Input Common Mode Voltage              | Differential Input                     | 200mV     |     | 2500  | mV            |
| I <sub>IL</sub>    | Input Leakage Low Current for OE1      | V <sub>IN</sub> = GND @ OE1 pin        | -150      |     | 5     | $\mu\text{A}$ |
| I <sub>IL</sub>    | Input Leakage Low Current for OE2/3    | V <sub>IN</sub> = GND                  |           |     | 5     | $\mu\text{A}$ |
| I <sub>IH</sub>    | Input Leakage High Current for OE1/2/3 | V <sub>IN</sub> = 3.465                |           |     | 20    | $\mu\text{A}$ |
| d <sub>TIN</sub>   | Input Duty Cycle                       | Measurement from differential waveform | 45        |     | 55    | %             |

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through  $\pm 75\text{mV}$  window centered around differential zero.

## DC Electrical Characteristics for 3.3V LVC MOS

Unless stated otherwise, VDDSE = 3.3V  $\pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Symbol            | Parameter              | Test Conditions                            | Min       | Typ | Max         | Unit          |
|-------------------|------------------------|--|-----------|-----|-------------|---------------|
| V <sub>OH</sub>   | Output HIGH Voltage    | I <sub>OH</sub> = -15mA                    | 2.4       |     | VDDSE       | V             |
| V <sub>OL</sub>   | Output LOW Voltage     | I <sub>OL</sub> = 15mA                     |           |     | 0.4         | V             |
| I <sub>OZDD</sub> | Output Leakage Current | Tri-state outputs, VDDSE = 3.465V          |           |     | 3           | $\mu\text{A}$ |
| V <sub>IH</sub>   | Input HIGH Voltage     | Single-ended inputs - CLKSEL, OE, SDA, SCL | 2         |     | VDDSE + 0.3 | V             |
| V <sub>IL</sub>   | Input LOW Voltage      | Single-ended inputs - CLKSEL, OE, SDA, SCL | GND - 0.3 |     | 0.8         | V             |
| V <sub>IH</sub>   | Input HIGH Voltage     | Single-ended input - XIN/CLKIN             | 2.4       |     | VDD33       | V             |
| V <sub>IL</sub>   | Input LOW Voltage      | Single-ended input - XIN/CLKIN             | GND - 0.3 |     | 0.8         | V             |

## DC Electrical Characteristics for 2.5V LVC MOS

Unless stated otherwise, VDDSE = 2.5V  $\pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Symbol            | Parameter              | Test Conditions                            | Min       | Typ | Max         | Unit          |
|-------------------|------------------------|--|-----------|-----|-------------|---------------|
| V <sub>OH</sub>   | Output HIGH Voltage    | I <sub>OH</sub> = -12mA                    | 0.7xVDDSE |     | VDDSE       | V             |
| V <sub>OL</sub>   | Output LOW Voltage     | I <sub>OL</sub> = 12mA                     |           |     | 0.4         | V             |
| I <sub>OZDD</sub> | Output Leakage Current | Tri-state outputs, VDDSE = 2.625V          |           |     | 3           | $\mu\text{A}$ |
| V <sub>IH</sub>   | Input HIGH Voltage     | Single-ended inputs - CLKSEL, OE, SDA, SCL | 1.7       |     | VDDSE + 0.3 | V             |
| V <sub>IL</sub>   | Input LOW Voltage      | Single-ended inputs - CLKSEL, OE, SDA, SCL | GND - 0.3 |     | 0.8         | V             |



## DC Electrical Characteristics for 1.8V LVCMOS

Unless stated otherwise, VDDSE = 1.8V ±5%, T<sub>A</sub> = -40°C to +85°C

| Symbol | Parameter              | Test Conditions                    | Min          | Typ | Max          | Unit |
|--------|------------------------|------------------------------------|--------------|-----|--------------|------|
| VOH    | Output HIGH Voltage    | IOH = -8mA                         | 0.7 x VDDSE  |     | VDDSE        | V    |
| VOL    | Output LOW Voltage     | IOL = 8mA                          |              |     | 0.25 x VDDSE | V    |
| IOZDD  | Output Leakage Current | Tri-state outputs, VDDSE = 1.89V   |              |     | 3            | µA   |
| VIH    | Input HIGH Voltage     | Single-ended inputs - OE, SDA, SCL | 0.65 * VDDSE |     | VDDSE + 0.3  | V    |
| VIL    | Input LOW Voltage      | Single-ended inputs - OE, SDA, SCL | GND - 0.3    |     | 0.35 * VDDSE | V    |

## Electrical Characteristics–DIF 0.7V LPHCSL Differential Outputs

Unless stated otherwise, VDDDIFF = 3.3 V ±5% or 2.5V ±5%, T<sub>A</sub> = -40° to +85°C

| Symbol             | Parameter                     | Notes                 | Min  | Typ | Max  | Units |
|--------------------|-------------------------------|-----------------------|------|-----|------|-------|
| dV/dt              | Slew Rate                     | 1,2,3,8               | 1    | 2.5 | 4    | V/ns  |
| ΔdV/dt             | Slew Rate Mismatch            | 1,2,3,8, at <= 200MHz |      |     | 20   | %     |
| VHIGH              | Voltage High                  | 1,6,7,8               | 660  | 800 | 1150 | mV    |
| VLOW               | Voltage Low                   | 1,6                   | -150 | 0   | 150  | mV    |
| VMAX               | Maximum Voltage               | 1                     |      |     | 1150 | mV    |
| VMIN               | Minimum Voltage               | 1                     | -300 |     |      | mV    |
| VSWING             | Voltage Swing                 | 1,2,6                 | 300  |     |      | mV    |
| VCROSS             | Crossing Voltage Value        | 1,4,6                 | 250  | 360 | 550  | mV    |
| ΔVCROSS            | Crossing Voltage variation    | 1,5                   |      |     | 140  | mV    |
| Jitter-Cy/Cy       | Cycle to Cycle Jitter         | 1,2                   |      | 10  |      | ps    |
| Jitter-STJ         | Jitter - Period Jitter        | 1,2                   |      | 70  |      | ps    |
| Duty Cycle         | Duty Cycle                    | 1,2                   | 45   |     | 55   | %     |
| Measured Frequency | LVHCSL at Differential Output | 1,2                   |      |     | 500  | MHz   |

\* differential clock amplitude setting 00.

Note 1: Guaranteed by design and characterization. Not 100% tested in production.

Note 2: Measured from differential waveform.

Note 3: Slew rate is measured through the VSWING voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

Note 4: VCROSS is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

Note 5: the total variation of all VCROSS measurements in any particular system. Note that this is a subset of VCROSS min/max (VCROSS absolute) allowed. The intent is to limit VCROSS induced modulation by setting ΔVCROSS to be smaller than VCROSS absolute.

Note 6: Measured from single-ended waveform.

Note 7: Measured with scope averaging off, using statistics function. Variation is difference between min. and max.

Note 8: Scope average ON.

## DC Electrical Characteristics for LVDS

Unless stated otherwise,  $V_{DDIFF} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ$  to  $+85^\circ\text{C}$

| Symbol             | Parameter  | Notes | Min   | Typ  | Max   | Unit |
|--------------------|--|-------|-------|------|-------|------|
| VOT (+)            | Differential Output Voltage for the TRUE binary state                              |       | 247   |      | 454   | mV   |
| VOT (-)            | Differential Output Voltage for the FALSE binary state                             |       | -247  |      | -454  | mV   |
| $\Delta$ VOT       | Change in VOT between Complimentary Output States                                  |       |       |      | 50    | mV   |
| VOS                | Output Common Mode Voltage (Offset Voltage)  |       | 1.125 | 1.25 | 1.375 | V    |
| $\Delta$ VOS       | Change in VOS between Complimentary Output States                                  |       |       |      | 50    | mV   |
| IOS                | Outputs Short Circuit Current, $V_{OUT+}$ or $V_{OUT-} = 0\text{V}$ or $V_{DDIFF}$ |       |       | 9    | 24    | mA   |
| IOSD               | Differential Outputs Short Circuit Current, $V_{OUT+} = V_{OUT-}$                  |       |       | 6    | 12    | mA   |
| Jitter-Cy/Cy       | Cycle to Cycle Jitter  | 1,2   |       | 20   |       | ps   |
| Jitter-STJ         | Jitter - ST  | 1,2   |       | 100  |       | ps   |
| Duty Cycle         | Duty Cycle   | 1,2   | 45    |      | 55    | %    |
| Measured Frequency | LVDS at Differential Output  | 1,2   |       |      | 500   | MHz  |

\* differential clock amplitude setting 01.

## DC Electrical Characteristics for LVPECL

Unless stated otherwise,  $V_{DDIFF} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ$  to  $+85^\circ\text{C}$

| Symbol             | Parameter   | Notes | Min                | Typ | Max                | Unit |
|--------------------|---|-------|--------------------|-----|--------------------|------|
| VOH                | Output Voltage HIGH, terminated through $50\Omega$ tied to $V_{DDIFF}-2\text{ V}$ |       | $V_{DDIFF} - 1.19$ |     | $V_{DDIFF} - 0.69$ | V    |
| VOL                | Output Voltage LOW, terminated through $50\Omega$ tied to $V_{DDIFF}-2\text{ V}$  |       | $V_{DDIFF} - 1.94$ |     | $V_{DDIFF} - 1.4$  | V    |
| VSWING             | Peak-to-Peak Output Voltage Swing   |       | 0.55               |     | 0.993              | V    |
| Jitter-Cy/Cy       | Cycle to Cycle Litter   | 1,2   |                    | 20  |                    | ps   |
| Jitter-STJ         | Jitter - ST   | 1,2   |                    | 100 |                    | ps   |
| Duty Cycle         | Duty Cycle  | 1,2   | 45                 |     | 55                 | %    |
| Measured Frequency | LVPECL at Differential Output   | 1,2   |                    |     | 500                | MHz  |

\* differential clock amplitude setting 01.

## AC Electrical Characteristics

Unless stated otherwise,  $V_{DDSE} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$  or  $1.8\text{ V} \pm 5\%$ ,  $T_A = -40^\circ$  to  $+85^\circ\text{C}$  (spread spectrum OFF)

| Symbol            | Parameter                   | Test Conditions  | Min. | Typ.  | Max. | Units |
|-------------------|-----------------------------|--|------|-------|------|-------|
| f <sub>IN</sub> 1 | Input Frequency             | Input frequency limit (XIN)  | 8    |       | 40   | MHz   |
|                   |                             | Input frequency limit (XIN) when enable DCO  | 12   |       | 38   | MHz   |
|                   |                             | Input frequency limit (Differential CLKIN)   | 8    |       | 125  | MHz   |
|                   |                             | Input frequency limit (LVCMOS to X1)   | 1    |       | 125  | MHz   |
| f <sub>OUT</sub>  | Output Frequency            | Single ended clock output limit (LVCMOS)   | 1    | < 125 | 160  | MHz   |
|                   |                             | Differential clock output limit (LPHCSL)   | 1    | < 333 | 500  | MHz   |
|                   |                             | Differential clock output limit (LVDS)   | 1    | < 333 | 500  | MHz   |
|                   |                             | Differential clock output limit (LVPECL)   | 1    |       | 500  | MHz   |
| f <sub>VCO1</sub> | VCO frequency range of PLL1 | VCO operating frequency range  | 300  |       | 600  | MHz   |
| f <sub>VCO2</sub> | VCO frequency range of PLL2 | VCO operating frequency range  | 400  |       | 1200 | MHz   |
| f <sub>VCO3</sub> | VCO frequency range of PLL3 | VCO operating frequency range  | 300  |       | 800  | MHz   |
| t <sub>2</sub>    | Input Duty Cycle            | Duty Cycle   | 45   |       | 55   | %     |
| t <sub>3</sub>    | Output Duty Cycle           | LVCMOS and Differential clock < 333MHz ,<br>Crossing point measurements  | 45   |       | 55   | %     |
| t <sub>3</sub>    | Output Duty Cycle           | LVCMOS and Differential clock > 333MHz ,<br>Crossing point measurements  | 40   |       | 60   | %     |
| t <sub>3</sub>    | Output Duty Cycle_REF       | Reference clock output or SE1-3 fan out clock  | 40   |       | 60   | %     |
| t <sub>4</sub>    | Rise/Fall, SLEW[0] = 1      | Single-ended LVCMOS output clock rise and fall time, 20% to 80% of VDDSE 1.8V-3.3V   |      | 1.0   |      | ns    |
|                   | Rise/Fall, SLEW[0] = 0      | Single-ended LVCMOS output clock rise and fall time, 20% to 80% of VDDSE 1.8V-3.3V   |      | 1.1   |      |       |
| t <sub>5</sub>    | Rise Times                  | LVDS, 20% to 80%   |      | 300   |      | ps    |
|                   | Fall Times                  | LVDS, 80% to 20%   |      | 300   |      |       |
|                   | Rise Times                  | LVPECL, 20% to 80%   |      | 300   |      |       |
|                   | Fall Times                  | LVPECL, 80% to 20%   |      | 300   |      |       |
| t <sub>6</sub>    | Clock Jitter                | Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs (1.8V to 3.3V nominal output voltage)<br>SE1 = 25MHz<br>*SE2 = 100MHz<br>*SE3 = 100MHz<br>DIFF1/2 = 100MHz |      | 50    |      | ps    |
|                   |                             | RMS Phase Jitter (12kHz to 20MHz integration range) differential output, VDDSE = 3.465V, 25MHz crystal,<br>SE1 = 25MHz<br>*SE2 = 100MHz<br>*SE3 = 100MHz<br>DIFF1/2 = 100MHz                                 |      | 1.1   |      | ps    |
| t <sub>7</sub>    | Output Skew                 | Skew between the same frequencies, with outputs using the same driver format   |      | 75    |      | ps    |
| t <sub>8</sub> 2  | Lock Time                   | PLL lock time from power-up  |      |       | 20   | ms    |
| t <sub>9</sub>    | Lock Time                   | 32.768kHz clock low power power-up time  |      | 10    | 100  | ms    |
| t <sub>9</sub> 3  | Lock Time                   | PLL lock time from shutdown mode   |      | 0.1   | 2    | ms    |

1. Practical lower frequency is determined by loop filter settings.

2. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

3. Actual PLL lock time depends on the loop configuration.

4. \* SE2/SE3 are not available in 5P35021, only available in 5P35023 QFN24 device.

5. t<sub>4</sub> Rise/Fall time measurements are based on 5pF load.

6. t<sub>5</sub> Rise/Fall time measurements are based on 2pF load.

## PCI Express Jitter Specifications

Unless stated otherwise,  $V_{DDIFF} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ$  to  $+85^\circ\text{C}$

| Symbol                     | Parameter                    | Conditions  | Min | Typ  | Max | PCIe Industry Specification | Units | Notes |
|----------------------------|------------------------------|---|-----|------|-----|-----------------------------|-------|-------|
| tJ (PCIe Gen1)             | Phase Jitter<br>Peak-to-Peak | $f = 100\text{MHz}/125\text{MHz}$ , 25MHz Crystal Input<br>Evaluation Band: 0Hz - Nyquist (clock frequency/2) |     | 30   |     | 86                          | ps    | 1,4   |
| tREFCLK_HF_RMS (PCIe Gen2) | Phase Jitter<br>RMS          | $f = 100\text{MHz}/125\text{MHz}$ , 25MHz Crystal Input<br>High Band: 1.5MHz - Nyquist (clock frequency/2)    |     | 2.56 |     | 3.10                        | ps    | 2,4   |
| tREFCLK_LF_RMS (PCIe Gen2) | Phase Jitter<br>RMS          | $f = 100\text{MHz}/125\text{MHz}$ , 25MHz Crystal Input<br>Low Band: 10kHz - 1.5MHz                           |     | 0.27 |     | 3.0                         | ps    | 2,4   |
| tREFCLK_RMS (PCIe Gen3)    | Phase Jitter<br>RMS          | $f = 100\text{MHz}/125\text{MHz}$ , 25MHz Crystal Input<br>Evaluation Band: 0Hz - Nyquist (clock frequency/2) |     | 0.8  |     | 1.0                         | ps    | 3,4   |

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

1. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1.
2. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for tREFCLK\_HF\_RMS (High Band) and 3.0ps RMS for tREFCLK\_LF\_RMS (Low Band).
3. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI\_Express\_Base\_r3.0 10 Nov, 2010 specification, and is subject to change pending the final release version of the specification.
4. This parameter is guaranteed by characterization. Not tested in production.

## Spread Spectrum Generation Specifications

| Symbol       | Parameter        | Description   | Min | Typ          | Max | Unit  |
|--------------|------------------|---|-----|--------------|-----|-------|
| fOUT         | Output Frequency | Output Frequency Range                              | 1   |              | 350 | MHz   |
| fMOD*        | Mod Frequency    | Modulation Frequency                                |     | 30 to 63     |     | kHz   |
| fSPREAD      | Spread Value     | Amount of Spread Value (programmable) - Down Spread |     | -0.5% to -2% |     | %fOUT |
| %tolerance*1 | Spread % value   | Variation of spread range                           |     | +/-15%       |     | %     |

\* input frequency dependent, see programming guide

\*1 design target

## I2C Bus DC Characteristics

| Symbol | Parameter             | Conditions | Min        | Typ | Max       | Unit |
|--------|-----------------------|------------|------------|-----|-----------|------|
| VIH    | Input HIGH Level      |            | 0.7xVDD33  |     |           | V    |
| VIL    | Input LOW Level       |            |            |     | 0.3xVDD33 | V    |
| VHYS   | Hysteresis of Inputs  |            | 0.05xVDD33 |     |           | V    |
| IIN    | Input Leakage Current |            |            |     | ±1        | µA   |
| VOL    | Output LOW Voltage    | IOL = 3 mA |            |     | 0.4       | V    |

## I2C Bus AC Characteristics

| Symbol    | Parameter                            | Min         | Typ | Max | Unit |
|-----------|--------------------------------------|-------------|-----|-----|------|
| FSCLK     | Serial Clock Frequency (SCL)         |             | 100 | 400 | kHz  |
| tBUF      | Bus free time between STOP and START | 1.3         |     |     | µs   |
| tSU:START | Setup Time, START                    | 0.6         |     |     | µs   |
| tHD:START | Hold Time, START                     | 0.6         |     |     | µs   |
| tSU:DATA  | Setup Time, data input (SDA)         | 100         |     |     | ns   |
| tHD:DATA  | Hold Time, data input (SDA) 1        | 0           |     |     | µs   |
| tOVD      | Output data valid from clock         |             |     | 0.9 | µs   |
| CB        | Capacitive Load for Each Bus Line    |             |     | 400 | pF   |
| tR        | Rise Time, data and clock (SDA, SCL) | 20 + 0.1xCB |     | 300 | ns   |
| tF        | Fall Time, data and clock (SDA, SCL) | 20 + 0.1xCB |     | 300 | ns   |
| tHIGH     | HIGH Time, clock (SCL)               | 0.6         |     |     | µs   |
| tLOW      | LOW Time, clock (SCL)                | 1.3         |     |     | µs   |
| tSU:STOP  | Setup Time, STOP                     | 0.6         |     |     | µs   |

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

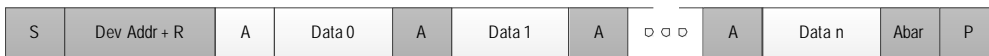
## General I<sup>2</sup>C Mode Operations

The device acts as a slave device on the I<sup>2</sup>C bus using one of the four I<sup>2</sup>C addresses (0xD0, 0xD2, 0xD4, or 0xD6) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I<sup>2</sup>C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.

## I<sup>2</sup>C Slave Read and Write Cycle Sequencing

Current Read



Sequential Read



Sequential Write



- from master to slave
- from slave to master

S = start  
 Sr = repeated start  
 A = acknowledge  
 Abar = none acknowledge  
 P = stop

**Byte0: General Control**

| Byte 00h | Name           | Control Function                  | Type | 0                         | 1                     | PWD |
|----------|----------------|-----------------------------------|------|---------------------------|-----------------------|-----|
| Bit 7    | OTP_Burned     | OTP memory programming indication | R/W  | OTP memory non-programmed | OTP memory programmed | 0   |
| Bit 6    | I2C_addr[1]    | I2C address select bit 1          | R/W  | 00: D0 / 01: D2           |                       | 0   |
| Bit 5    | I2C_addr[0]    | I2C address select bit 0          | R/W  | 10: D4 / 11: D6           |                       | 0   |
| Bit 4    | PLL1_SSEN      | PLL1 Spread Spectrum enable       | R/W  | disable                   | enable                | 0   |
| Bit 3    | DIV1_src_sel   | Divider 1 source clock select     | R/W  | PLL1                      | Xtal                  | 0   |
| Bit 2    | PLL3_refin_sel | PLL3 source selection             | R/W  | Xtal                      | Seed (DIV2)           | 0   |
| Bit 1    | EN_CLKIN       | enable CLKIN                      | R/W  | disable                   | enable                | 0   |
| Bit 0    | OTP_protect    | OTP memory protection             | R/W  | read/write                | write locked          | 0   |

**Byte1: Dash Code ID (optional)**

| Byte 01h | Name           | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|------------------|------|---|---|-----|
| Bit 7    | DashCode ID[7] | Dash code ID     | R/W  | - | - | 0   |
| Bit 6    | DashCode ID[6] | Dash code ID     | R/W  | - | - | 0   |
| Bit 5    | DashCode ID[5] | Dash code ID     | R/W  | - | - | 0   |
| Bit 4    | DashCode ID[4] | Dash code ID     | R/W  | - | - | 0   |
| Bit 3    | DashCode ID[3] | Dash code ID     | R/W  | - | - | 0   |
| Bit 2    | DashCode ID[2] | Dash code ID     | R/W  | - | - | 0   |
| Bit 1    | DashCode ID[1] | Dash code ID     | R/W  | - | - | 0   |
| Bit 0    | DashCode ID[0] | Dash code ID     | R/W  | - | - | 0   |

**Byte2: Crystal Cap setting**

| Byte 02h | Name        | Control Function            | Type | 0                            | 1 | PWD |
|----------|-------------|-----------------------------|------|------------------------------|---|-----|
| Bit 7    | Xtal_Cap[7] | Xtal cap load trimming bits | R/W  | x1 x2<br>x4 x8<br>total 15pf |   | 0   |
| Bit 6    | Xtal_Cap[6] | Xtal cap load trimming bits | R/W  |                              |   | 0   |
| Bit 5    | Xtal_Cap[5] | Xtal cap load trimming bits | R/W  |                              |   | 0   |
| Bit 4    | Xtal_Cap[4] | Xtal cap load trimming bits | R/W  |                              |   | 1   |
| Bit 3    | Xtal_Cap[3] | Xtal cap load trimming bits | R/W  |                              |   | 0   |
| Bit 2    | Xtal_Cap[2] | Xtal cap load trimming bits | R/W  |                              |   | 0   |
| Bit 1    | Xtal_Cap[1] | Xtal cap load trimming bits | R/W  |                              |   | 0   |
| Bit 0    | Xtal_Cap[0] | Xtal cap load trimming bits | R/W  |                              |   | 1   |

**Byte3: PLL3 M Divider**

| Byte 03h | Name          | Control Function               | Type | 0              | 1                   | PWD |
|----------|---------------|--------------------------------|------|----------------|---------------------|-----|
| Bit 7    | PLL3_MDIV1    | PLL3 source clock divider      | R/W  | disable M DIV1 | bypadd divider (/1) | 0   |
| Bit 6    | PLL3_MDIV2    | PLL3 source clock divider      | R/W  | disable M DIV2 | bypadd divider (/2) | 0   |
| Bit 5    | PLL3_M_DIV[5] | PLL3 reference integer divider | R/W  | 3~64           | default 25          | 0   |
| Bit 4    | PLL3_M_DIV[4] | PLL3 reference integer divider | R/W  | -              | -                   | 1   |
| Bit 3    | PLL3_M_DIV[3] | PLL3 reference integer divider | R/W  | -              | -                   | 1   |
| Bit 2    | PLL3_M_DIV[2] | PLL3 reference integer divider | R/W  | -              | -                   | 0   |
| Bit 1    | PLL3_M_DIV[1] | PLL3 reference integer divider | R/W  | -              | -                   | 0   |
| Bit 0    | PLL3_M_DIV[0] | PLL3 reference integer divider | R/W  | -              | -                   | 1   |

**Byte4: PLL3 N Divider**

| Byte 04h | Name          | Control Function                       | Type | 0                                      | 1 | PWD |
|----------|---------------|--|------|--|---|-----|
| Bit 7    | PLL3_N_DIV[7] | PLL3 VCO feedback integer divider bit7 | R/W  | 12~2048, default VCO setting is 480MHz |   | 1   |
| Bit 6    | PLL3_N_DIV[6] | PLL3 VCO feedback integer divider bit6 | R/W  |  |   | 1   |
| Bit 5    | PLL3_N_DIV[5] | PLL3 VCO feedback integer divider bit5 | R/W  |  |   | 1   |
| Bit 4    | PLL3_N_DIV[4] | PLL3 VCO feedback integer divider bit4 | R/W  |  |   | 0   |
| Bit 3    | PLL3_N_DIV[3] | PLL3 VCO feedback integer divider bit3 | R/W  |  |   | 0   |
| Bit 2    | PLL3_N_DIV[2] | PLL3 VCO feedback integer divider bit2 | R/W  |  |   | 0   |
| Bit 1    | PLL3_N_DIV[1] | PLL3 VCO feedback integer divider bit1 | R/W  |  |   | 0   |
| Bit 0    | PLL3_N_DIV[0] | PLL3 VCO feedback integer divider bit0 | R/W  |  |   | 0   |

**Byte5: PLL3 Loop filter setting and N Divider10:8**

| Byte 05h | Name          | Control Function                        | Type | 0                                      | 1                  | PWD |
|----------|---------------|---|------|--|--------------------|-----|
| Bit 7    | PLL3_R100K    | PLL3 Loop filter resistor 100Kohm       | R/W  | bypass                                 | plus 100Kohm       | 0   |
| Bit 6    | PLL3_R50K     | PLL3 Loop filter resistor 50Kohm        | R/W  | bypass                                 | plus 50Kohm        | 0   |
| Bit 5    | PLL3_R25K     | PLL3 Loop filter resistor 25Kohm        | R/W  | bypass                                 | plus 25Kohm        | 0   |
| Bit 4    | PLL3_R12.5K   | PLL3 Loop filter resistor 12.5Kohm      | R/W  | bypass                                 | plus 12.5Kohm      | 1   |
| Bit 3    | PLL3_R6K      | PLL3 Loop filter resistor 6Kohm         | R/W  | bypass                                 | only 6Kohm applied | 0   |
| Bit 2    | PLL3_N_DM[10] | PLL3 VCO feedback integer divider bit10 | R/W  | 12~2048, default VCO setting is 480MHz |                    | 0   |
| Bit 1    | PLL3_N_DM[9]  | PLL3 VCO feedback integer divider bit9  | R/W  |  |                    | 0   |
| Bit 0    | PLL3_N_DM[8]  | PLL3 VCO feedback integer divider bit8  | R/W  |  |                    | 1   |

**Byte6: PLL3 charge pump control**

| Byte 06h | Name           | Control Function                        | Type | 0    | 1    | PWD |
|----------|----------------|---|------|------|------|-----|
| Bit 7    | OUTDIV3 Source | Output divider 3 source clock selection | R/W  | PLL2 | PLL3 | 0   |
| Bit 6    | PLL3_CP_8X     | PLL3 charge pump control                | R/W  | -    | x8   | 1   |
| Bit 5    | PLL3_CP_4X     | PLL3 charge pump control                | R/W  | -    | x4   | 1   |
| Bit 4    | PLL3_CP_2X     | PLL3 charge pump control                | R/W  | -    | x2   | 0   |
| Bit 3    | PLL3_CP_1X     | PLL3 charge pump control                | R/W  | -    | x1   | 1   |
| Bit 2    | PLL3_CP_/24    | PLL3 charge pump control                | R/W  | -    | /24  | 1   |
| Bit 1    | PLL3_CP_/3     | PLL3 charge pump control                | R/W  | -    | /3   | 0   |
| Bit 0    | PLL3_SIREF     | PLL3 SiRef current selection            | R/W  | 10uA | 20uA | 0   |

Notes: Formula :  $(iRef (10uA) * (1+SIREF) * (1*1X+2*2X+4*4X+8*8X+16*16X)) / ((24*/24)+(3*/3))$

**Byte7: PLL1 Control and OUTDIV5 divider**

| Byte 07h | Name              | Control Function              | Type | 0       | 1      | PWD |
|----------|-------------------|-------------------------------|------|---------|--------|-----|
| Bit 7    | PLL1_MDIV_Doubler | PLL1 reference clock doubler  | R/W  | disable | enable | 0   |
| Bit 6    | PLL1_SIREF        | PLL1 SiRef current selection  | R/W  | 10.8uA  | 21.6uA | 0   |
| Bit 5    | PLL1_EN_CH2       | PLL1 output Channel 2 control | R/W  | disable | enable | 1   |
| Bit 4    | PLL1_EN_3rdpole   | PLL1 3rd Pole control         | R/W  | disable | enable | 0   |
| Bit 3    | OUTDIV5[3]        | Output divider5 control bit 3 | R/W  | -       | -      | 0   |
| Bit 2    | OUTDIV5[2]        | Output divider5 control bit 2 | R/W  | -       | -      | 0   |
| Bit 1    | OUTDIV5[1]        | Output divider5 control bit 1 | R/W  | -       | -      | 1   |
| Bit 0    | OUTDIV5[0]        | Output divider5 control bit 0 | R/W  | -       | -      | 1   |

**Byte8: PLL1 M Divider**

| Byte 08h | Name         | Control Function                           | Type | 0                   | 1                   | PWD |
|----------|--------------|--|------|---------------------|---------------------|-----|
| Bit 7    | PLL1_MDIV1   | PLL3 VCO referenceclock divider 1          | R/W  | disable MDIV1       | bypass divider (/1) | 0   |
| Bit 6    | PLL1_MDIV2   | PLL3 VCO referenceclock divider 2          | R/W  | disable MDIV2       | bypass divider (/2) | 0   |
| Bit 5    | PLL1_M_DM[5] | PLL1 reference clock divider control bit 5 | R/W  | 3~64, default is 25 |                     | 0   |
| Bit 4    | PLL1_M_DM[4] | PLL1 reference clock divider control bit 4 | R/W  |                     |                     | 1   |
| Bit 3    | PLL1_M_DM[3] | PLL1 reference clock divider control bit 3 | R/W  |                     |                     | 1   |
| Bit 2    | PLL1_M_DM[2] | PLL1 reference clock divider control bit 2 | R/W  |                     |                     | 0   |
| Bit 1    | PLL1_M_DM[1] | PLL1 reference clock divider control bit 1 | R/W  |                     |                     | 0   |
| Bit 0    | PLL1_M_DM[0] | PLL1 reference clock divider control bit 0 | R/W  |                     |                     | 1   |

**Byte9: PLL1 VCO N divider**

| Byte 09h | Name         | Control Function                        | Type | 0                       | 1 | PWD |
|----------|--------------|---|------|-------------------------|---|-----|
| Bit 7    | PLL1_N_DM[7] | PLL1 VCO feedback divider control bit 7 | R/W  | 12~2048, default is 600 |   | 0   |
| Bit 6    | PLL1_N_DM[6] | PLL1 VCO feedback divider control bit 6 | R/W  |                         |   | 1   |
| Bit 5    | PLL1_N_DM[5] | PLL1 VCO feedback divider control bit 5 | R/W  |                         |   | 0   |
| Bit 4    | PLL1_N_DM[4] | PLL1 VCO feedback divider control bit 4 | R/W  |                         |   | 1   |
| Bit 3    | PLL1_N_DM[3] | PLL1 VCO feedback divider control bit 3 | R/W  |                         |   | 1   |
| Bit 2    | PLL1_N_DM[2] | PLL1 VCO feedback divider control bit 2 | R/W  |                         |   | 0   |
| Bit 1    | PLL1_N_DM[1] | PLL1 VCO feedback divider control bit 1 | R/W  |                         |   | 0   |
| Bit 0    | PLL1_N_DM[0] | PLL1 VCO feedback divider control bit 0 | R/W  |                         |   | 0   |



**Byte10: PLL loop filter and N divider**

| Byte 0Ah | Name           | Control Function                        | Type | 0                        | 1                    | PWD |
|----------|----------------|---|------|--------------------------|----------------------|-----|
| Bit 7    | PLL1_R100K     | PLL1 Loop filter resistor 100Kohm       | R/W  | bypass                   | plus 100Kohm         | 1   |
| Bit 6    | PLL1_R50K      | PLL1 Loop filter resistor 50Kohm        | R/W  | bypass                   | plus 50Kohm          | 0   |
| Bit 5    | PLL1_R25K      | PLL1 Loop filter resistor 25Kohm        | R/W  | bypass                   | plus 25Kohm          | 1   |
| Bit 4    | PLL1_R12.5K    | PLL1 Loop filter resistor 12.5Kohm      | R/W  | bypass                   | plus 12.5Kohm        | 1   |
| Bit 3    | PLL1_R1.0K     | PLL1 Loop filter resistor 1Kohm         | R/W  | bypass                   | only 1.0Kohm applied | 0   |
| Bit 2    | PLL1_N_DIV[10] | PLL1 VCO feedback integer divider bit10 | R/W  | '12~2048, default is 600 |                      | 0   |
| Bit 1    | PLL1_N_DIV[9]  | PLL1 VCO feedback integer divider bit9  | R/W  |                          |                      | 1   |
| Bit 0    | PLL1_N_DIV[8]  | PLL1 VCO feedback integer divider bit8  | R/W  |                          |                      | 0   |

**Byte11: PLL1 charge pump**

| Byte 0Bh | Name        | Control Function         | Type | 0 | 1   | PWD |
|----------|-------------|--------------------------|------|---|-----|-----|
| Bit 7    | PLL1_CP_32X | PLL1 charge pump control | R/W  | - | x32 | 0   |
| Bit 6    | PLL1_CP_16X | PLL1 charge pump control | R/W  | - | x16 | 0   |
| Bit 5    | PLL1_CP_8X  | PLL1 charge pump control | R/W  | - | x8  | 0   |
| Bit 4    | PLL1_CP_4X  | PLL1 charge pump control | R/W  | - | x4  | 0   |
| Bit 3    | PLL1_CP_2X  | PLL1 charge pump control | R/W  | - | x2  | 0   |
| Bit 2    | PLL1_CP_1X  | PLL1 charge pump control | R/W  | - | x1  | 1   |
| Bit 1    | PLL1_CP_/24 | PLL1 charge pump control | R/W  | - | /24 | 1   |
| Bit 0    | PLL1_CP_/3  | PLL1 charge pump control | R/W  | - | /3  | 0   |

**Byte12: PLL1 spread spectrum control**

| Byte 0Ch | Name             | Control Function                             | Type | 0 | 1 | PWD |
|----------|------------------|--|------|---|---|-----|
| Bit 7    | PLL1_SS_REFDIV23 | PLL1 Spread Spectrum control- Ref divider 23 | R/W  | - | - | 0   |
| Bit 6    | PLL1_SS_REFDM[6] | PLL1 Spread Spectrum control- Ref divider 6  | R/W  | - | - | 0   |
| Bit 5    | PLL1_SS_REFDM[5] | PLL1 Spread Spectrum control- Ref divider 5  | R/W  | - | - | 0   |
| Bit 4    | PLL1_SS_REFDM[4] | PLL1 Spread Spectrum control- Ref divider 4  | R/W  | - | - | 0   |
| Bit 3    | PLL1_SS_REFDM[3] | PLL1 Spread Spectrum control- Ref divider 3  | R/W  | - | - | 0   |
| Bit 2    | PLL1_SS_REFDM[2] | PLL1 Spread Spectrum control- Ref divider 2  | R/W  | - | - | 0   |
| Bit 1    | PLL1_SS_REFDM[1] | PLL1 Spread Spectrum control- Ref divider 1  | R/W  | - | - | 0   |
| Bit 0    | PLL1_SS_REFDM[0] | PLL1 Spread Spectrum control- Ref divider 0  | R/W  | - | - | 0   |

**Byte13: PLL1 spread spectrum control**

| Byte 0Dh | Name            | Control Function                          | Type | 0 | 1 | PWD |
|----------|-----------------|---|------|---|---|-----|
| Bit 7    | PLL1_SS_FBDM[7] | PLL1 Spread Spectrum - feedback divider 7 | R/W  | - | - | 0   |
| Bit 6    | PLL1_SS_FBDM[6] | PLL1 Spread Spectrum - feedback divider 6 | R/W  | - | - | 0   |
| Bit 5    | PLL1_SS_FBDM[5] | PLL1 Spread Spectrum - feedback divider 5 | R/W  | - | - | 0   |
| Bit 4    | PLL1_SS_FBDM[4] | PLL1 Spread Spectrum - feedback divider 4 | R/W  | - | - | 0   |
| Bit 3    | PLL1_SS_FBDM[3] | PLL1 Spread Spectrum - feedback divider 3 | R/W  | - | - | 0   |
| Bit 2    | PLL1_SS_FBDM[2] | PLL1 Spread Spectrum - feedback divider 2 | R/W  | - | - | 0   |
| Bit 1    | PLL1_SS_FBDM[1] | PLL1 Spread Spectrum - feedback divider 1 | R/W  | - | - | 0   |
| Bit 0    | PLL1_SS_FBDM[0] | PLL1 Spread Spectrum - feedback divider 0 | R/W  | - | - | 0   |

**Byte14: PLL1 Spread spectrum control**

| Byte 0Eh | Name             | Control Function                           | Type | 0 | 1 | PWD |
|----------|------------------|--|------|---|---|-----|
| Bit 7    | PLL1_SS_FBDM[15] | PLL1 Spread Spectrum - feedback divider 15 | R/W  | - | - | 0   |
| Bit 6    | PLL1_SS_FBDM[14] | PLL1 Spread Spectrum - feedback divider 14 | R/W  | - | - | 0   |
| Bit 5    | PLL1_SS_FBDM[13] | PLL1 Spread Spectrum - feedback divider 13 | R/W  | - | - | 0   |
| Bit 4    | PLL1_SS_FBDM[12] | PLL1 Spread Spectrum - feedback divider 12 | R/W  | - | - | 0   |
| Bit 3    | PLL1_SS_FBDM[11] | PLL1 Spread Spectrum - feedback divider 11 | R/W  | - | - | 0   |
| Bit 2    | PLL1_SS_FBDM[10] | PLL1 Spread Spectrum - feedback divider 10 | R/W  | - | - | 0   |
| Bit 1    | PLL1_SS_FBDM[09] | PLL1 Spread Spectrum - feedback divider 9  | R/W  | - | - | 0   |
| Bit 0    | PLL1_SS_FBDM[08] | PLL1 Spread Spectrum - feedback divider 8  | R/W  | - | - | 0   |

**Byte15: Output divider1 control**

| Byte 0Fh | Name       | Control Function              | Type | 0 | 1 | PWD |
|----------|------------|-------------------------------|------|---|---|-----|
| Bit 7    | OUTDIV1[3] | Output divider1 control bit 3 | R/W  | - | - | 0   |
| Bit 6    | OUTDIV1[2] | Output divider1 control bit 2 | R/W  | - | - | 0   |
| Bit 5    | OUTDIV1[1] | Output divider1 control bit 1 | R/W  | - | - | 1   |
| Bit 4    | OUTDIV1[0] | Output divider1 control bit 0 | R/W  | - | - | 1   |
| Bit 3    | OUTDIV2[3] | Output divider2 control bit 3 | R/W  | - | - | 0   |
| Bit 2    | OUTDIV2[2] | Output divider2 control bit 2 | R/W  | - | - | 0   |
| Bit 1    | OUTDIV2[1] | Output divider2 control bit 1 | R/W  | - | - | 1   |
| Bit 0    | OUTDIV2[0] | Output divider2 control bit 0 | R/W  | - | - | 1   |

**Byte16: PLL2 integer feedback divider**

| Byte 10h | Name            | Control Function                 | Type | 0 | 1 | PWD |
|----------|-----------------|----------------------------------|------|---|---|-----|
| Bit 7    | reserved        | -                                | R/W  | - | - | 0   |
| Bit 6    | reserved        | -                                | R/W  | - | - | 0   |
| Bit 5    | reserved        | -                                | R/W  | - | - | 0   |
| Bit 4    | reserved        | -                                | R/W  | - | - | 0   |
| Bit 3    | reserved        | -                                | R/W  | - | - | 0   |
| Bit 2    | PLL2_FB_INT[10] | PLL2 feedback integer divider 10 | R/W  | - | - | 0   |
| Bit 1    | PLL2_FB_INT[9]  | PLL2 feedback integer divider 9  | R/W  | - | - | 0   |
| Bit 0    | PLL2_FB_INT[8]  | PLL2 feedback integer divider 8  | R/W  | - | - | 0   |

**Byte17: PLL2 integer feedback divider**

| Byte 11h | Name              | Control Function                | Type | 0 | 1 | PWD |
|----------|-------------------|---------------------------------|------|---|---|-----|
| Bit 7    | PLL2_FB_INT_DM[7] | PLL2 feedback integer divider 7 | R/W  | - | - | 0   |
| Bit 6    | PLL2_FB_INT_DM[6] | PLL2 feedback integer divider 6 | R/W  | - | - | 0   |
| Bit 5    | PLL2_FB_INT_DM[5] | PLL2 feedback integer divider 5 | R/W  | - | - | 1   |
| Bit 4    | PLL2_FB_INT_DM[4] | PLL2 feedback integer divider 4 | R/W  | - | - | 0   |
| Bit 3    | PLL2_FB_INT_DM[3] | PLL2 feedback integer divider 3 | R/W  | - | - | 1   |
| Bit 2    | PLL2_FB_INT_DM[2] | PLL2 feedback integer divider 2 | R/W  | - | - | 0   |
| Bit 1    | PLL2_FB_INT_DM[1] | PLL2 feedback integer divider 1 | R/W  | - | - | 0   |
| Bit 0    | PLL2_FB_INT_DM[0] | PLL2 feedback integer divider 0 | R/W  | - | - | 0   |

**Byte18: PLL2 fractional feedback divider**

| Byte 12h | Name              | Control Function                   | Type | 0 | 1 | PWD |
|----------|-------------------|------------------------------------|------|---|---|-----|
| Bit 7    | PLL2_FB_FRC_DM[7] | PLL2 feedback fractional divider 7 | R/W  | - | - | 0   |
| Bit 6    | PLL2_FB_FRC_DM[6] | PLL2 feedback fractional divider 6 | R/W  | - | - | 0   |
| Bit 5    | PLL2_FB_FRC_DM[5] | PLL2 feedback fractional divider 5 | R/W  | - | - | 0   |
| Bit 4    | PLL2_FB_FRC_DM[4] | PLL2 feedback fractional divider 4 | R/W  | - | - | 0   |
| Bit 3    | PLL2_FB_FRC_DM[3] | PLL2 feedback fractional divider 3 | R/W  | - | - | 0   |
| Bit 2    | PLL2_FB_FRC_DM[2] | PLL2 feedback fractional divider 2 | R/W  | - | - | 0   |
| Bit 1    | PLL2_FB_FRC_DM[1] | PLL2 feedback fractional divider 1 | R/W  | - | - | 0   |
| Bit 0    | PLL2_FB_FRC_DM[0] | PLL2 feedback fractional divider 0 | R/W  | - | - | 0   |

**Byte19: PLL2 fractional feedback divider**

| Byte 13h | Name               | Control Function                    | Type | 0 | 1 | PWD |
|----------|--------------------|-------------------------------------|------|---|---|-----|
| Bit 7    | PLL2_FB_FRC_DM[15] | PLL2 feedback fractional divider 15 | R/W  | - | - | 0   |
| Bit 6    | PLL2_FB_FRC_DM[14] | PLL2 feedback fractional divider 14 | R/W  | - | - | 0   |
| Bit 5    | PLL2_FB_FRC_DM[13] | PLL2 feedback fractional divider 13 | R/W  | - | - | 0   |
| Bit 4    | PLL2_FB_FRC_DM[12] | PLL2 feedback fractional divider 12 | R/W  | - | - | 0   |
| Bit 3    | PLL2_FB_FRC_DM[11] | PLL2 feedback fractional divider 11 | R/W  | - | - | 0   |
| Bit 2    | PLL2_FB_FRC_DM[10] | PLL2 feedback fractional divider 10 | R/W  | - | - | 0   |
| Bit 1    | PLL2_FB_FRC_DM[9]  | PLL2 feedback fractional divider 9  | R/W  | - | - | 0   |
| Bit 0    | PLL2_FB_FRC_DM[8]  | PLL2 feedback fractional divider 8  | R/W  | - | - | 0   |

**Byte20: PLL2 spread spectrum control**

| Byte 14h | Name         | Control Function                    | Type | 0 | 1 | PWD |
|----------|--------------|-------------------------------------|------|---|---|-----|
| Bit 7    | PLL2_STEP[7] | PLL2 spread step size control bit 7 | R/W  | - | - | 0   |
| Bit 6    | PLL2_STEP[6] | PLL2 spread step size control bit 6 | R/W  | - | - | 0   |
| Bit 5    | PLL2_STEP[5] | PLL2 spread step size control bit 5 | R/W  | - | - | 0   |
| Bit 4    | PLL2_STEP[4] | PLL2 spread step size control bit 4 | R/W  | - | - | 0   |
| Bit 3    | PLL2_STEP[3] | PLL2 spread step size control bit 3 | R/W  | - | - | 0   |
| Bit 2    | PLL2_STEP[2] | PLL2 spread step size control bit 2 | R/W  | - | - | 0   |
| Bit 1    | PLL2_STEP[1] | PLL2 spread step size control bit 1 | R/W  | - | - | 0   |
| Bit 0    | PLL2_STEP[0] | PLL2 spread step size control bit 0 | R/W  | - | - | 0   |

**Byte21: PLL2 spread spectrum control**

| Byte 15h | Name          | Control Function                     | Type | 0 | 1 | PWD |
|----------|---------------|--------------------------------------|------|---|---|-----|
| Bit 7    | PLL2_STEP[15] | PLL2 spread step size control bit 15 | R/W  | - | - | 0   |
| Bit 6    | PLL2_STEP[14] | PLL2 spread step size control bit 14 | R/W  | - | - | 0   |
| Bit 5    | PLL2_STEP[13] | PLL2 spread step size control bit 13 | R/W  | - | - | 0   |
| Bit 4    | PLL2_STEP[12] | PLL2 spread step size control bit 12 | R/W  | - | - | 0   |
| Bit 3    | PLL2_STEP[11] | PLL2 spread step size control bit 11 | R/W  | - | - | 0   |
| Bit 2    | PLL2_STEP[10] | PLL2 spread step size control bit 10 | R/W  | - | - | 0   |
| Bit 1    | PLL2_STEP[9]  | PLL2 spread step size control bit 9  | R/W  | - | - | 0   |
| Bit 0    | PLL2_STEP[8]  | PLL2 spread step size control bit 8  | R/W  | - | - | 0   |

**Byte22: PLL2 spread spectrum control**

| Byte 16h | Name               | Control Function                          | Type | 0 | 1 | PWD |
|----------|--------------------|---|------|---|---|-----|
| Bit 7    | PLL2_STEP_DELTA[7] | PLL2 spread step size control delta bit 7 | R/W  | - | - | 0   |
| Bit 6    | PLL2_STEP_DELTA[6] | PLL2 spread step size control delta bit 6 | R/W  | - | - | 0   |
| Bit 5    | PLL2_STEP_DELTA[5] | PLL2 spread step size control delta bit 5 | R/W  | - | - | 0   |
| Bit 4    | PLL2_STEP_DELTA[4] | PLL2 spread step size control delta bit 4 | R/W  | - | - | 0   |
| Bit 3    | PLL2_STEP_DELTA[3] | PLL2 spread step size control delta bit 3 | R/W  | - | - | 0   |
| Bit 2    | PLL2_STEP_DELTA[2] | PLL2 spread step size control delta bit 2 | R/W  | - | - | 0   |
| Bit 1    | PLL2_STEP_DELTA[1] | PLL2 spread step size control delta bit 1 | R/W  | - | - | 0   |
| Bit 0    | PLL2_STEP_DELTA[0] | PLL2 spread step size control delta bit 0 | R/W  | - | - | 0   |

**Byte23: PLL2 period control**

| Byte 17h | Name           | Control Function          | Type | 0 | 1 | PWD |
|----------|----------------|---------------------------|------|---|---|-----|
| Bit 7    | PLL2_PERIOD[7] | PLL2 period control bit 7 | R/W  | - | - | 0   |
| Bit 6    | PLL2_PERIOD[6] | PLL2 period control bit 6 | R/W  | - | - | 0   |
| Bit 5    | PLL2_PERIOD[5] | PLL2 period control bit 5 | R/W  | - | - | 0   |
| Bit 4    | PLL2_PERIOD[4] | PLL2 period control bit 4 | R/W  | - | - | 0   |
| Bit 3    | PLL2_PERIOD[3] | PLL2 period control bit 3 | R/W  | - | - | 0   |
| Bit 2    | PLL2_PERIOD[2] | PLL2 period control bit 2 | R/W  | - | - | 0   |
| Bit 1    | PLL2_PERIOD[1] | PLL2 period control bit 1 | R/W  | - | - | 0   |
| Bit 0    | PLL2_PERIOD[0] | PLL2 period control bit 0 | R/W  | - | - | 0   |

**Byte24: PLL2 control register**

| Byte 18h | Name           | Control Function                   | Type | 0       | 1                  | PWD |
|----------|----------------|------------------------------------|------|---------|--------------------|-----|
| Bit 7    | PLL2_PERIOD[9] | PLL2 period control bit 9          | R/W  | -       | -                  | 0   |
| Bit 6    | PLL2_PERIOD[8] | PLL2 period control bit 8          | R/W  | -       | -                  | 0   |
| Bit 5    | PLL2_SSEN      | PLL2 spread spectrum enable        | R/W  | disable | enable             | 0   |
| Bit 4    | PLL2_R100K     | PLL2 Loop filter resistor 100Kohm  |      | bypass  | plus 100Kohm       | 0   |
| Bit 3    | PLL2_R50K      | PLL2 Loop filter resistor 50Kohm   |      | bypass  | plus 50Kohm        | 0   |
| Bit 2    | PLL2_R25K      | PLL2 Loop filter resistor 25Kohm   |      | bypass  | plus 25Kohm        | 0   |
| Bit 1    | PLL2_R12.5K    | PLL2 Loop filter resistor 12.5Kohm |      | bypass  | plus 12.5Kohm      | 0   |
| Bit 0    | PLL2_R6K       | PLL2 Loop filter resistor 6Kohm    |      | bypass  | only 6Kohm applied | 0   |

**Byte25: PLL2 charge pump control**

| Byte 19h | Name        | Control Function             | Type | 0    | 1    | PWD |
|----------|-------------|------------------------------|------|------|------|-----|
| Bit 7    | PLL2_CP_16X | PLL2 charge pump control     | R/W  | -    | x16  | 0   |
| Bit 6    | PLL2_CP_8X  | PLL2 charge pump control     | R/W  | -    | x8   | 0   |
| Bit 5    | PLL2_CP_4X  | PLL2 charge pump control     | R/W  | -    | x4   | 1   |
| Bit 4    | PLL2_CP_2X  | PLL2 charge pump control     | R/W  | -    | x2   | 0   |
| Bit 3    | PLL2_CP_1X  | PLL2 charge pump control     | R/W  | -    | x1   | 0   |
| Bit 2    | PLL2_CP_/24 | PLL2 charge pump control     | R/W  | -    | /24  | 1   |
| Bit 1    | PLL2_CP_/3  | PLL2 charge pump control     | R/W  | -    | /3   | 0   |
| Bit 0    | PLL2_SIREF  | PLL2 SiRef current selection | R/W  | 10uA | 20uA | 0   |

**Byte26: PLL2 M divider setting**

| Byte 1Ah | Name              | Control Function                     | Type | 0                   | 1                   | PWD |
|----------|-------------------|--------------------------------------|------|---------------------|---------------------|-----|
| Bit 7    | PLL2_MDIV_Doubler | PLL2 reference divider - doubler     | R/W  | disable             | enable              | 0   |
| Bit 6    | PLL2_MDIV1        | PLL2 reference divider 1             | R/W  | disable M DIV1      | bypadd divider (/1) | 1   |
| Bit 5    | PLL2_MDIV2        | PLL2 reference divider 2             | R/W  | disable M DIV2      | bypadd divider (/2) | 0   |
| Bit 4    | PLL2_MDIV[4]      | PLL2 reference divider control bit 4 | R/W  | 3~64, default is 25 |                     | 0   |
| Bit 3    | PLL2_MDIV[3]      | PLL2 reference divider control bit 3 | R/W  |                     |                     | 0   |
| Bit 2    | PLL2_MDIV[2]      | PLL2 reference divider control bit 2 | R/W  |                     |                     | 0   |
| Bit 1    | PLL2_MDIV[1]      | PLL2 reference divider control bit 1 | R/W  |                     |                     | 0   |
| Bit 0    | PLL2_MDIV[0]      | PLL2 reference divider control bit 0 | R/W  |                     |                     | 0   |

**Byte27: Output divider 4**

| Byte 1Bh | Name       | Control Function            | Type | 0 | 1 | PWD |
|----------|------------|-----------------------------|------|---|---|-----|
| Bit 7    | OUTDIV3[3] | Out divider 3 control bit 7 | R/W  | - | - | 0   |
| Bit 6    | OUTDIV3[2] | Out divider 3 control bit 6 | R/W  | - | - | 0   |
| Bit 5    | OUTDIV3[1] | Out divider 3 control bit 5 | R/W  | - | - | 1   |
| Bit 4    | OUTDIV3[0] | Out divider 3 control bit 4 | R/W  | - | - | 1   |
| Bit 3    | OUTDIV4[3] | Out divider 4 control bit 3 | R/W  | - | - | 0   |
| Bit 2    | OUTDIV4[2] | Out divider 4 control bit 2 | R/W  | - | - | 0   |
| Bit 1    | OUTDIV4[1] | Out divider 4 control bit 1 | R/W  | - | - | 1   |
| Bit 0    | OUTDIV4[0] | Out divider 4 control bit 0 | R/W  | - | - | 1   |

**Byte28: PLL operation control register**

| Byte 1Ch | Name           | Control Function                             | Type | 0           | 1                     | PWD |
|----------|----------------|--|------|-------------|-----------------------|-----|
| Bit 7    | PLL2_HRS_EN    | PLL2 spread high resolution selection enable | R/W  | normal      | enable (shift 4 bits) | 0   |
| Bit 6    | PLL2_refin_sel | PLL2 reference clock source select           | R/W  | Xtal        | DIV2                  | 0   |
| Bit 5    | PLL3_PDB       | PLL3 Power Down                              | R/W  | Power Down  | running               | 1   |
| Bit 4    | PLL3_LCKBYPSSB | PLL3 lock bypass                             | R/W  | bypass lock | lock                  | 1   |
| Bit 3    | PLL2_PDB       | PLL2 Power Down                              | R/W  | Power Down  | running               | 1   |
| Bit 2    | PLL2_LCKBYPSSB | PLL2 lock bypass                             | R/W  | bypass lock | lock                  | 1   |
| Bit 1    | PLL1_PDB       | PLL1 Power Down                              | R/W  | Power Down  | running               | 1   |
| Bit 0    | PLL1_LCKBYPSSB | PLL1 lock bypass                             | R/W  | bypass lock | lock                  | 1   |

**Byte29: Output control**

| Byte 1Dh | Name           | Control Function                        | Type | 0                            | 1          | PWD |
|----------|----------------|---|------|------------------------------|------------|-----|
| Bit 7    | DIFF1_SEL      | Differential clock 1 output OE2 control |      | not controlled               | controlled | 0   |
| Bit 6    | DIFF2_SEL      | Differential clock 2 output OE2 control |      | not controlled               | controlled | 0   |
| Bit 5    | DIFF1_EN       | Differential clock 1 output enable      | R/W  | disable                      | enable     | 1   |
| Bit 4    | DIFF2_EN       | Differential clock 2 output enable      | R/W  | disable                      | enable     | 1   |
| Bit 3    | OUTDIV4_Source | Output divider 4 source clock selection | R/W  | PLL2                         | Xtal       | 0   |
| Bit 2    | SE1_SLEW       | SE 1 slew rate control                  | R/W  | normal                       | strong     | 0   |
| Bit 1    | VDD1_SEL[1]    | VDD1 level control bit 1                | R/W  | 00/01: 3.3V 10: 2.5V 11: 1.8 |            | 0   |
| Bit 0    | VDD1_SEL[0]    | VDD1 level control bit 0                | R/W  |                              |            | 0   |

**Byte30: OE and DFC control**

| Byte 1Eh | Name             | Control Function                 | Type | 0                         | 1          | PWD |
|----------|------------------|----------------------------------|------|---------------------------|------------|-----|
| Bit 7    | SE1_EN           | SE1 output enable control        | R/W  | disable                   | enable     | 1   |
| Bit 6    | OE1_fun_sel[1]   | OE1 pin function selection bit 1 | R/W  | 11:DFC0 10: SE1_PPS       |            | 0   |
| Bit 5    | OE1_fun_sel[0]   | OE1 pin function selection bit 0 | R/W  | 01: PD#                   | 00: SE1 OE | 0   |
| Bit 4    | * SE3_EN         | SE3 output enable                | R/W  | disable                   | enable     | 1   |
| Bit 3    | * OE3_fun_sel[1] | OE3 pin function selection bit 1 | R/W  | 11: DFC1 10: SE3_PPS      |            | 0   |
| Bit 2    | * OE3_fun_sel[0] | OE3 pin function selection bit 0 | R/W  | 01:xx                     | 00:SE3_OE  | 0   |
| Bit 1    | * DFC_SW_Sel[1]  | DFC frequency select bit 1       | R/W  | 00: N0 01: N1 10:N2 11:N3 |            | 0   |
| Bit 0    | * DFC_SW_Sel[0]  | DFC frequency select bit 0       | R/W  |                           |            | 0   |

**Byte31: Control Register**

| Byte 1Fh | Name              | Control Function              | Type | 0                            | 1                       | PWD |
|----------|-------------------|-------------------------------|------|------------------------------|-------------------------|-----|
| Bit 7    | * SE2_Freerun_32K | SE2 32K free run              |      | freerun 32K                  | B31 bit6 control source | 1   |
| Bit 6    | * SE2_CLKSEL1     | SE2 source clock selection    |      | DIV5                         | DIV4                    | 0   |
| Bit 5    | * VDD2_SEL[1]     | VDD2 level control bit 1      | R/W  | 00/01: 3.3V 10: 2.5V 11: 1.8 |                         | 0   |
| Bit 4    | * VDD2_SEL[0]     | VDD2 level control bit 0      | R/W  |                              |                         | 0   |
| Bit 3    | * SE2_SLEW        | SE 2 slew rate control        | R/W  | normal                       | strong                  | 0   |
| Bit 2    | PLL2_3rd_EN_CFG   | PLL2 3rd order control        |      | 1st order                    | 3rd order               | 1   |
| Bit 1    | PLL2_EN_CH2       | PLL2 channel 2 enable control | R/W  | disable                      | enable                  | 0   |
| Bit 0    | PLL2_EN_3rdpole   | PLL2 3rd Pole control         | R/W  | disable                      | enable                  | 1   |

**Byte32: Control Register**

| Byte 20h | Name             | Control Function                 | Type | 0                     | 1          | PWD |
|----------|------------------|----------------------------------|------|-----------------------|------------|-----|
| Bit 7    | * SE2_EN         | SE2 output enable                | R/W  | disable               | enable     | 1   |
| Bit 6    | * OE2_fun_sel[1] | OE2 pin function selection bit 1 | R/W  | 11: RESET 10: SE2_PPS |            | 0   |
| Bit 5    | * OE2_fun_sel[0] | OE2 pin function selection bit 0 | R/W  | 01: DIFF1/2 OE        | 00: SE2 OE | 0   |
| Bit 4    | DFC_EN           | DFC function control             | R/W  | disable               | enable     | 0   |
| Bit 3    | WD_EN            | WatchDog timer control           | R/W  | disable               | enable     | 0   |
| Bit 2    | Timer_sel<1>     | Watchdog timer select bit 1      | R/W  | 00: 250mS 01: 500ms   |            | 0   |
| Bit 1    | Timer_sel<0>     | Watchdog timer select bit 0      | R/W  | 10: 2S                | 11: 4S     | 0   |
| Bit 0    | Alarm_Flag       | Alarm Status(Read Only)          | R    | No alarm              | Alarmed    | 0   |

**Byte33: SE3 and DIFF1 Control Register**

| Byte 21h | Name              | Control Function                         | Type | 0                 | 1                                | PWD |
|----------|-------------------|--|------|-------------------|----------------------------------|-----|
| Bit 7    | * SE3_Freerun_32K | SE3 32K free run                         | R/W  | freerun 32K       | DIV2 or DIV4 selected by B33bit6 | 1   |
| Bit 6    | * SE3_CLKSEL1     | SE3 source clock selection               | R/W  | DIV2              | DIV4                             | 0   |
| Bit 5    | * VDD3_SEL[1]     | VDD3 level control bit 1                 | R/W  | 11: 1.8V 10: 2.5V |                                  | 0   |
| Bit 4    | * VDD3_SEL[0]     | VDD3 level control bit 0                 | R/W  | 0x: 3.3V          |                                  | 0   |
| Bit 3    | * SE3_SLEW        | SE 3 slew rate control                   | R/W  | normal            | strong                           | 0   |
| Bit 2    | DIFF_PDBHiZEN     | Differential output high-Z at power down | R/W  | TBD               | output tri-state, bias off       | 0   |
| Bit 1    | DIFF1_CMOS2_FLIP  | Differential 1/2 LVCMOS output control   | R/W  | DIFF1_B inverted  | DIFF1_B non-inverted             | 0   |
| Bit 0    | DIFF2_CMOS2_FLIP  | Differential 1/2 LVCMOS output control   | R/W  | DIFF2_B inverted  | DIFF2_B non-inverted             | 0   |

**Byte34: DIFF1 Control Register**

| Byte 22h | Name                 | Control Function                              | Type | 0  | 1      | PWD |
|----------|----------------------|---|------|--|--------|-----|
| Bit 7    | DIFF1_CLK_SEL        | Differential clock 1 source selection         | R/W  | DIV1   | DIV3   | 1   |
| Bit 6    | DIFF1_io_pwr_sel     | Differential clock 1 output power             | R/W  | 2.5V   | 3.3V   | 1   |
| Bit 5    | DIFF1_OUTPUT_TYPE[1] | Differential clock 1 type select bit 1        | R/W  | 00: LVCMOS 01: LVDS<br>10: LVPECL 11: LPHCSL   |        | 1   |
| Bit 4    | DIFF1_OUTPUT_TYPE[0] | Differential clock 1 type select bit 0        | R/W  |  |        | 1   |
| Bit 3    | DIFF1_AMP[1]         | Differential clock 1 amplitude control bit 1  | R/W  | LPHCSL: 00=740mV,01=800mV,10=855mV,11=910mV<br>LPECL:00=710mV,01=810mV,10=875mV,11=920mV<br>LVDS:00=311mV,01=344mV,10=376mV,11=408mV |        | 0   |
| Bit 2    | DIFF1_AMP[0]         | Differential clock 1 amplitude control bit 0  | R/W  |  |        | 1   |
| Bit 1    | DIFF1_CMOS_SLEW      | Differential clock 1 LVCMOS slew rate control | R/W  | normal   | strong | 0   |
| Bit 0    | D1FF1_CMOS2_EN       | Differential clock 1 LVCMOS output_B control  | R/W  | disable  | enable | 0   |

**Byte35: DIFF2 Control Register**

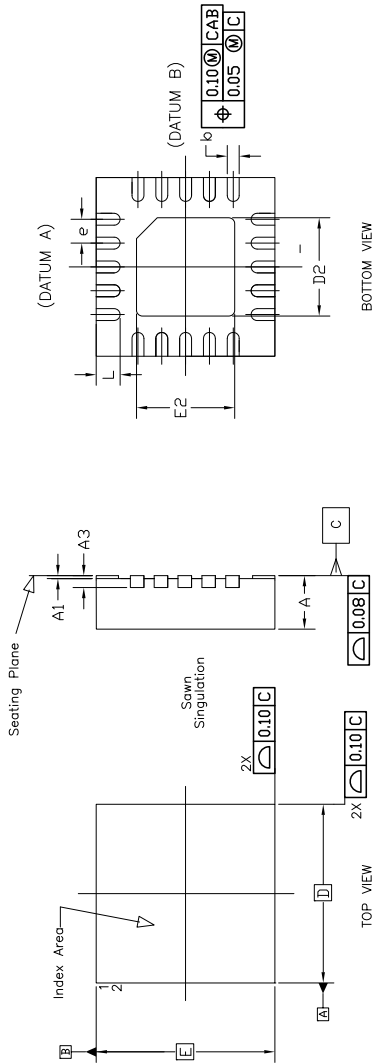
| Byte 23h | Name                 | Control Function                              | Type | 0   | 1      | PWD |
|----------|----------------------|---|------|---|--------|-----|
| Bit 7    | DIFF2_CLK_SEL        | Differential clock 2 source selection         | R/W  | DIV1  | DIV3   | 0   |
| Bit 6    | DIFF2_IO_PWR_SEL     | Differential clock 2 output power             | R/W  | 2.5V  | 3.3V   | 1   |
| Bit 5    | DIFF2_OUTPUT_TYPE[1] | Differential clock 2 type select bit 1        | R/W  | 00: LVCMOS 01: LVDS<br>10: LVPECL 11: LPHCSL  |        | 1   |
| Bit 4    | DIFF2_OUTPUT_TYPE[0] | Differential clock 2 type select bit 0        | R/W  |   |        | 1   |
| Bit 3    | DIFF2_AMP[1]         | Differential clock 2 amplitude control bit 1  | R/W  | LPHCSL: 00=740mV,01=800mV,10=855mV,11=910mV<br>LVPECL:00=710mV,01=810mV,10=875mV,11=920mV<br>LVDS:00=311mV,01=344mV,10=376mV,11=408mV |        | 0   |
| Bit 2    | DIFF2_AMP[0]         | Differential clock 2 amplitude control bit 0  | R/W  |   |        | 1   |
| Bit 1    | DIFF2_CMOS_SLEW      | Differential clock 2 LVCMOS slew rate control | R/W  | normal  | strong | 0   |
| Bit 0    | DIFF2_CMOS2_EN       | Differential clock 2 LVCMOS output_B control  | R/W  | disable   | enable | 0   |

**Byte36: SE1 and DIV4 control**

| Byte 24h | Name                   | Control Function                 | Type | 0            | 1               | PWD |
|----------|------------------------|----------------------------------|------|--------------|-----------------|-----|
| Bit 7    | I2C_PDB                | chip power down control bit      | R/W  | power down   | normal          | 1   |
| Bit 6    | Ref_free_run           | Reference clock output (SE2/SE3) | R/W  | stop         | freerun         | 0   |
| Bit 5    | free_run_output_config | SE clocks free run control       | R/W  | SE2 free run | SE2/3 free run  | 0   |
| Bit 4    | SE1_Freerun_32K        | SE1 clock output default         | R/W  | 32K freerun  | B36bit3 control | 0   |
| Bit 3    | SE1_CLKSEL1            | SEL1 output select               | R/W  | DIV5         | DIV4            | 1   |
| Bit 2    | REF_EN                 | REF output enable                | R/W  | disable      | enable          | 1   |
| Bit 1    | DIV4_CH3_EN            | DIV4 channel 3 output control    | R/W  | disable      | enable          | 0   |
| Bit 0    | DIV4_CH2_EN            | DIV4 channel 2 output control    | R/W  | disable      | enable          | 0   |

# Package Outline Drawings (NDG20)

| REVISIONS |                 |          |
|-----------|-----------------|----------|
| REV       | DESCRIPTION     | DATE     |
| 00        | INITIAL RELEASE | 3/30/16  |
|           |                 | APPROVED |
|           |                 | JH       |



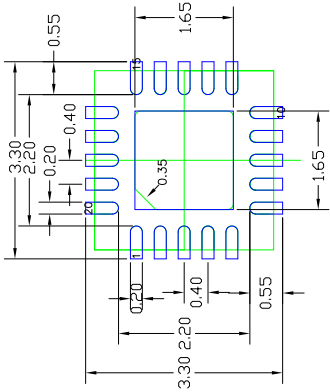
| Symbol | DIMENSION  |      |      |
|--------|------------|------|------|
|        | Min        | Nom  | Max  |
| A      | 0.80       | 0.90 | 1.00 |
| A1     | 0          | 0.02 | 0.05 |
| A3     | 0.20 Ref   |      |      |
| b      | 0.17       | 0.20 | 0.25 |
| e      | 0.40 BASIC |      |      |
| N      | 20         |      |      |
| ND     | 5          |      |      |
| NE     | 5          |      |      |
| D      | 3.00 BASIC |      |      |
| E      | 3.00 BASIC |      |      |
| D2     | 1.55       | 1.65 | 1.75 |
| E2     | 1.55       | 1.65 | 1.75 |
| L      | 0.30       | 0.40 | 0.50 |

- NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
  2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
  3. COPLANARITY SHALL NOT EXCEED 0.05 mm.
  4. WARPAGE SHALL NOT EXCEED 0.05 mm.
  5. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)

|                             |                                    |
|-----------------------------|------------------------------------|
| TOLERANCES UNLESS SPECIFIED | 6024 Silver Creek Valley Road      |
| DECIMAL                     | San Jose CA 95138                  |
| X±                          | PHONE: (408) 284-8200              |
| XX±                         | FAX: (408) 284-8591                |
| XXX±                        | WWW.IDT.COM                        |
| APPROVALS                   | TITLE ND/NDG 20 PACKAGE OUTLINE    |
| DRAWN @AC                   | 3/30/16                            |
| CHECKED                     | 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ |
|                             | 0.40 PITCH QFN                     |
|                             | SIZE DRAWING No.                   |
|                             | C PSC-4179-02                      |
|                             | REV                                |
|                             | 00                                 |
|                             | DO NOT SCALE DRAWING               |
|                             | SHEET 1 OF 2                       |

# Package Outline Drawings (NDG20), cont.

| REVISIONS |                 |          |
|-----------|-----------------|----------|
| REV       | DESCRIPTION     | DATE     |
| 00        | INITIAL RELEASE | 3/30/16  |
|           |                 | APPROVED |
|           |                 | JH       |



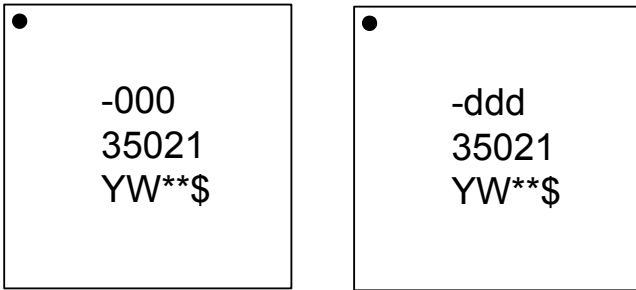
RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
  2. TOP-DOWN VIEW, AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

|                             |                                    |
|-----------------------------|------------------------------------|
| TOLERANCES UNLESS SPECIFIED | 6024 Silver Creek Valley Road      |
| DECIMAL ±1                  | San Jose, CA 95138                 |
| XX±                         | PHONE: (408) 284-8200              |
| XXX±                        | FAX: (408) 284-8591                |
| APPROVALS                   | www.IDT.com                        |
| DRAWN #24C                  | TITLE ND/NDG 20 PACKAGE OUTLINE    |
| CHECKED                     | 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ |
|                             | 0.40 PITCH QFN                     |
|                             | SIZE DRAWING No.                   |
|                             | C PSC-4179-02                      |
|                             | REV                                |
|                             | 00                                 |
|                             | DO NOT SCALE DRAWING               |
|                             | SHEET 2 OF 2                       |



## Marking Diagrams



### Notes:

1. Line 1&2: truncated part number
2. "-000" denotes blank part.
3. "-ddd" denotes dash code.
4. "\*\*\*" is the lot sequence number.
5. "YW" is the last digit of the year and week that the part was assembled.
6. "\$" is the mark code.

## Ordering Information

| Part / Order Number | Shipping Packaging | Package    | Temperature   |
|---------------------|--------------------|------------|---------------|
| 5P35021-000NDGI     | Tubes              | 20-pin QFN | -40° to +85°C |
| 5P35021-000NDGI8    | Tape and Reel      | 20-pin QFN | -40° to +85°C |
| 5P35021-dddNDGI     | Tubes              | 20-pin QFN | -40° to +85°C |
| 5P35021-dddNDGI8    | Tape and Reel      | 20-pin QFN | -40° to +85°C |

## Revision History

| Date     | Description of Change   |
|----------|---|
| 11/30/17 | Updated I <sup>2</sup> C section.                                     |
| 01/25/17 | 1. Corrected typos in Byte 27.<br>2. Updated package outline drawing. |
| 09/20/16 | Changed package outline drawing EPAD reference from 1.10mm to 1.65mm. |
| 05/26/16 | Initial release.  |



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