Enpirion EP5357xUI DC/DC Converter Module Evaluation Board

Introduction

Thank you for choosing Altera® Enpirion power products!

This application note describes how to test the EP5357xUI (EP5357LUI, EP5357HUI) converters using the Altera Enpirion 2.5mmx2.25mm Module EVAL BOARD shown in Fig. 1. In addition to this document you will also need the device datasheet for a thorough evaluation of the power converter module.

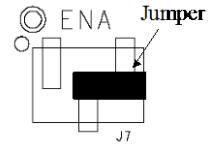
The EP5357xUI converters are part of a new class of DC/DC converter products, a complete power system on silicon:

- These devices are complete modules including magnetics, and require only ceramic input and output capacitors.
- The evaluation board is designed to offer a wide range of engineering evaluation capabilities. This includes the base configuration of an 0603 input capacitor and an 0805 output capacitor.
- Pads are available to add one additional input capacitor and two additional output capacitors for evaluation of performance over a wide range of input/output capacitor combinations.
- Pads are available to populate an external resistor divider to enable output voltage programming of values not available using the VID. The pads are labeled R1 and R2. Pads are also available for placing an optional feed-forward capacitor (labeled C9) across resistor R1.

  NOTE: The External voltage divider option is available only with EP5357LUI.
- Jumpers are provided for easy programming of the following signals:
  - Light load mode (LLM)
  - Enable
  - VS0-VS2 output voltage selection pins
- Test points are provided as well as clip leads for input and output connections
- The board comes with input decoupling, and input reverse polarity protection to safeguard the device from common setup mishaps.

Quick Start Guide

STEP 1: Before applying power to the board, set the "ENABLE" jumper to the Disable Position. Set VS0, VS1 and VS2 pins for the desired output setting. A voltage greater than 1.4V at LLM pin, will enable LLM, while a voltage less than 0.4V will disable it.



Output Disabled

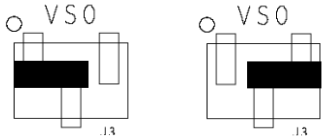
CAUTION: the signal pins LLM, ENA, VS0, VS1 and VS2 must be connected to a logic "high", jumper to the left, or a logic "low", jumper to the right. It may not be left floating as the pin state would then be in an indeterminate state.

STEP 2: Connect a power supply to the input test points, TP8 (VIN) and TP5 (GND) as indicated in Figure 1. The same test points can also be used to measure the input voltage.

CAUTION: be mindful of the polarity and the voltage magnitude. If V_{IN} is greater than 6V, the board may get damaged. If the input voltage polarity is wrong, diode D1 will conduct, and draw excessive input current.

STEP 3: Set the output voltage select pins for the desired output voltage. Refer to Tables 1 and 2 to determine the setting.

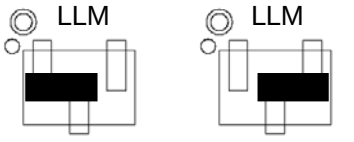
CAUTION: the external resistor divider is not populated in the standard board configuration. Choosing the "EXT" option for the EP5357LUI without the external resistors R1 and R2 will result in unpredictable behavior.



"1" "0"

STEP 4: Connect the load to the output connectors TP7 (VOUT) and TP6 (GND), as indicated in Figure 1.The same test points are also used to measure the DC output voltage.

STEP 5: Connect the LLM (Light Load Mode) jumper as needed. A voltage greater than 1.4V will enable LLM, and less than 0.4V will disable LLM.



LLM Enabled LLM Disabled

STEP 6: Move the ENABLE jumper to the enabled position, and power up the board. The EP5357xUI should now be operational.

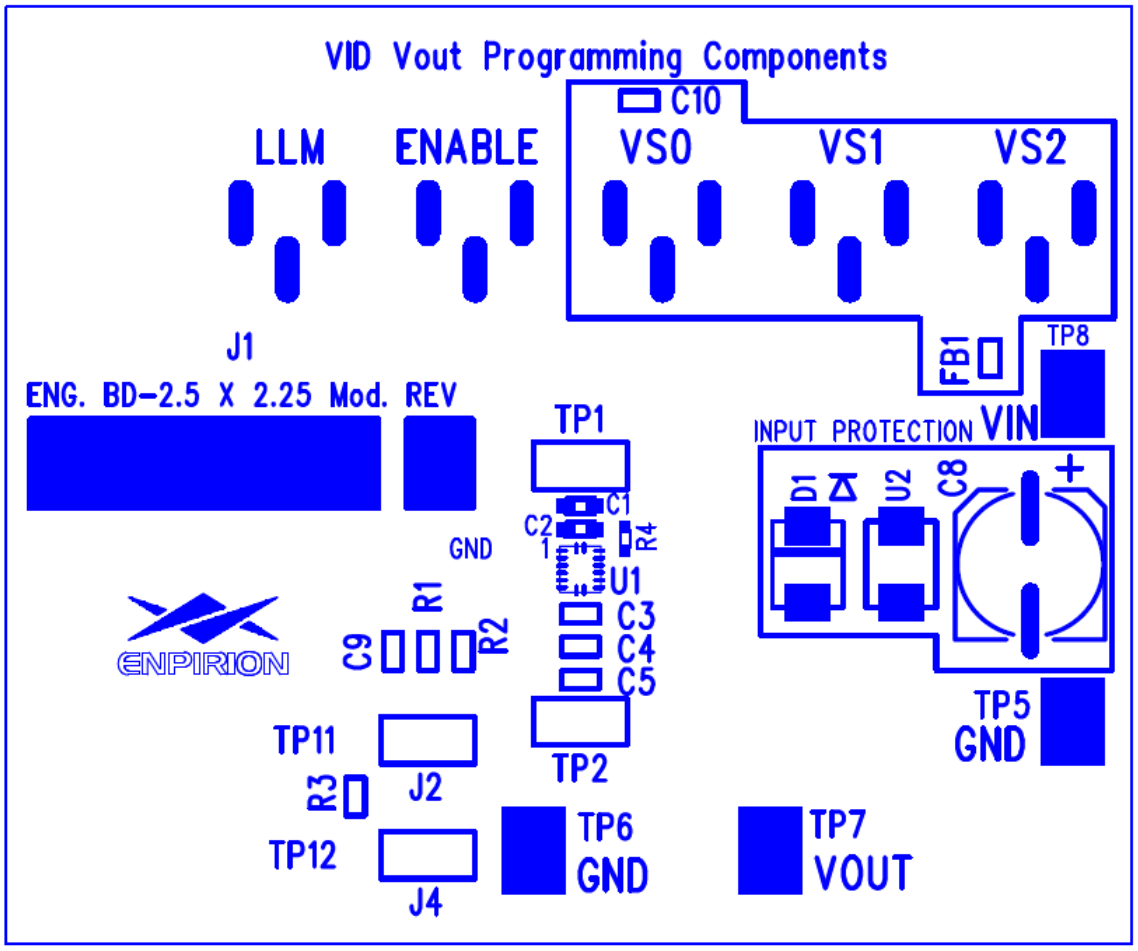


Figure 1. Evaluation Board Layout.

Output Voltage Select

The EP5357xUI utilizes a 3 pin output voltage select scheme. The output voltage is programmed by setting the VSx jumpers to either a logic "1" or a logic "0" as described in the Quick Start section

Tables 1 and 2 show the logic table for V_{OUT} selection. There are seven preset output voltage levels and an externally programmable option for the EP5357LUI. The EP5357HUI has eight preset output voltage levels and no external programming capability.

Table 1: EP5357LUI Output Voltage Select Logic Table

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.8
1	1	1	EXT

Table 2: EP5357HUI Output Voltage Select Logic Table

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	0	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce inaccurate measurements – especially efficiency.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a balanced impedance probe tip as shown in Figure 2, and through-hole test point pair TP2 to measure the output voltage ripple to avoid noise coupling into the probe ground lead and for load transient response measurements.

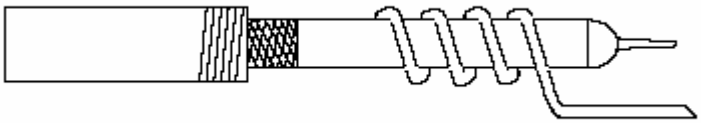


Figure 2: Balanced-impedance oscilloscope probe. Wrap bare wire around the ground shaft and bring the wire close to the probe tip. This minimizes probe loop inductance and stray noise pickup by the probe.

Using The External Voltage Divider

The EP5357xUI evaluation board is designed to provide a great deal of flexibility in evaluating the performance of the Altera Enpirion DC/DC module.

Pre-tinned pads are provided to place 0805 sized 1% resistors on the board to implement an external resistor divider for the EP5357LUI to choose an output voltage other than one of the seven pre-set voltages available on the VID. See Figure 3 for the basic circuit.

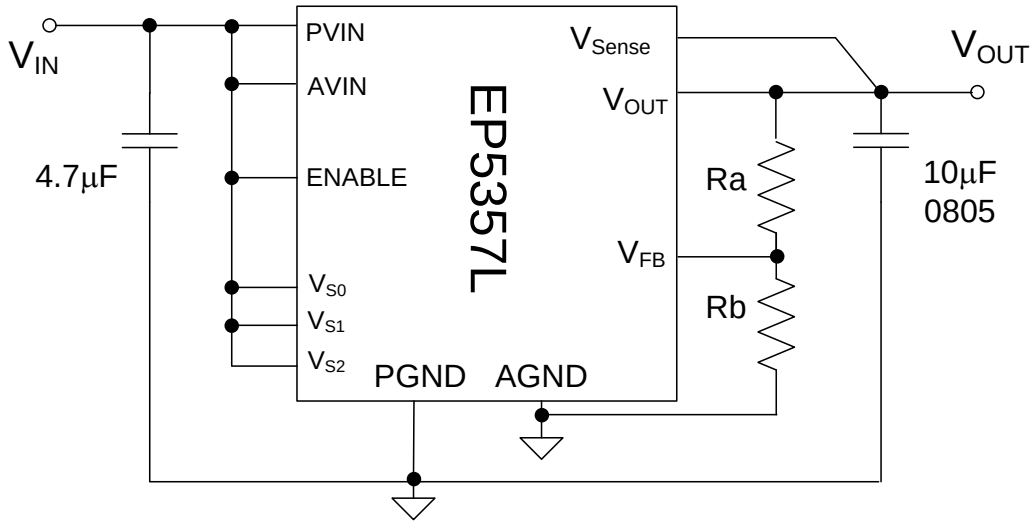


Figure 3. External divider schematic for the EP5357LUI.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{R1}{R2}\right)$$

R_1 must be chosen as 237kΩ to maintain control loop stability. Then R_2 is given as:

$$R_2 = \frac{142.2x10^3}{V_{OUT} - 0.6}\Omega$$

The external voltage divider option is chosen by setting the jumpers VS0 – VS2 to a logic "high". Light-load mode (LLM) is not operational when using external resistor dividers.

Note: The V_{SENSE} pin should be tied to the Output pin even in external feedback mode to access the internal phase lead capacitor that is situated between the V_{SENSE} and V_{FB} pads. This phase lead capacitor is integral to the loop compensation and the power supply stability.

Dynamically Adjustable Output

The EP5357xUI is designed to allow for dynamic switching between the predefined voltage levels by toggling the VID pins. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is defined in the datasheet.

This feature can be tested by connecting the VSx jumper center pins to logic driver to toggle between the various V_{OUT} states.

Note: Dynamic switching between a predefined output and an externally programmed output is not allowed. This could result excess current flow and damage the device.

Input and Output Capacitors

Input Filter Capacitor

For $I_{LOAD} \leq 500mA$, $C_{IN} = 2.2uF$

For $I_{LOAD} > 500mA$ $C_{IN} = 4.7uF$.

0402 capacitor case size is acceptable.

The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

Output Filter Capacitor

For VIN $\leq$ 4.3V, $C_{OUT_MIN} = 10uF$ 0603 MLCC.

For VIN > 4.3V, $C_{OUT_MIN} = 10uF$ 0805 MLCC.

Ripple performance can be improved by using 2x10µF 0603 MLCC capacitors (for any allowed VIN).

The maximum output filter capacitance next to the output pins of the device is 60µF low ESR MLCC capacitance. V_{OUT} has to be sensed at the last output filter capacitor next to the EP5357xUI.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance.

Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Please refer to product datasheet for details on maximum bulk capacitance.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

Board, BOM, Schematic

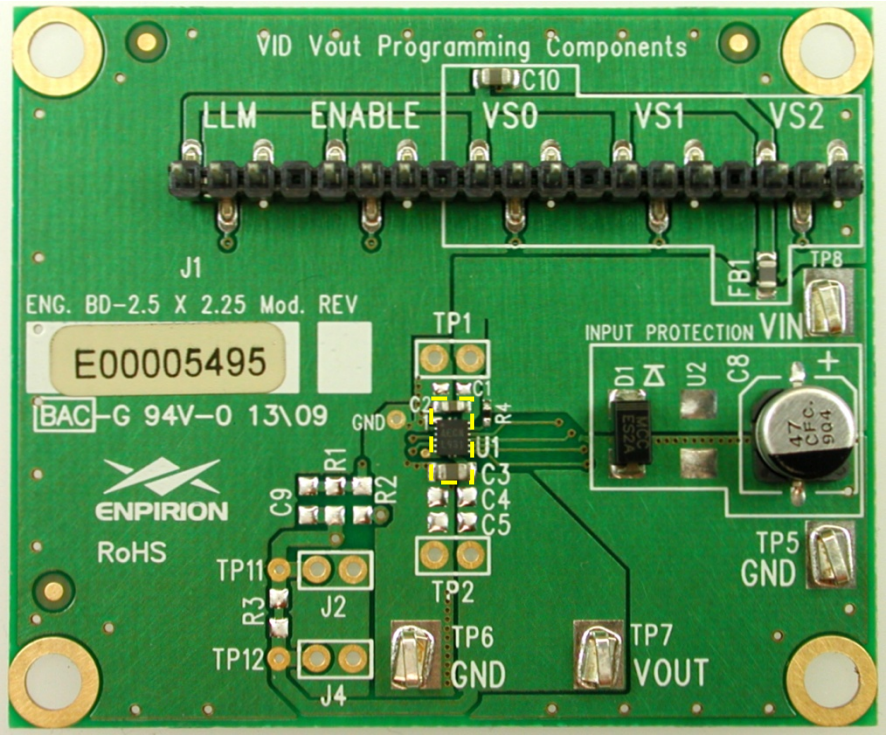


Figure 4. Photo of EVB.

Table 3. EVB Bill of Materials.

Item Description	Qty	Ref Des	Item Type	Function
4.7UF 10V X5R 0603 CAPACITOR CERAMIC	1	C2	Capacitor	Input Capacitor
CAP, 10UF 0805 X7R 10% 10V CERAMIC	2	C3	Capacitor	Output Capacitor
EP5357xUI 2.5MM X 2.25MM	1	U1	Device-GTP	Enpirion EP5357xUI
CAP 47UF 16V ELECT FC SMD	1	C8	Capacitor	Board Input Decoupling Capacitor
S2A DIODE	1	D1	Diode	Reverse Polarity Protection
CAP, 10UF 0805 X7R 10% 10V CERAMIC	1	C10	Capacitor	Connector Decoupling
MULTILAYER SMD FERRITE BEAD 4000MA 0805	1	FB1	Ferrite Bead	Connector Decoupling
CONNECTOR, CUSTOM, VERTICAL HEADER, SMT	1	J1	Connector/Contact	Jumper/Connector Array
COMPONENT NOT USED ** DO NOT INSTALL **	8	C1,C4,C5,C9,R1,R2,R3,U2		Not Used
TEST POINT SURFACE MOUNT	4	TP5,TP6,TP7,TP8	Connector/Contact	Test Point
RESISTOR ZERO OHM 1/10W 5% 0402 SMD	1	R4	Resistor	Zero Ohm Jumper

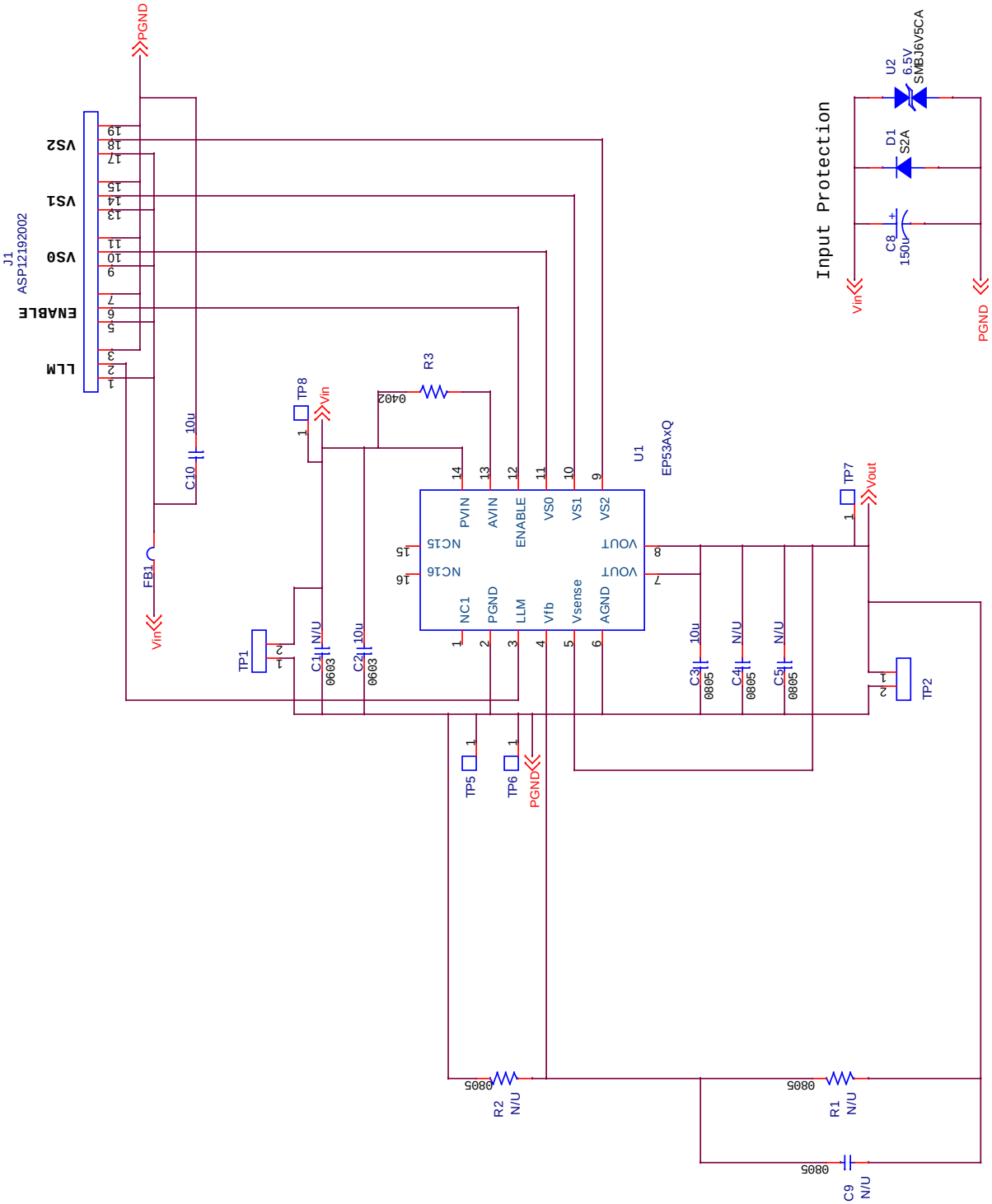

PGND
J1
ASP12192002
VS2
VS1
VS0
ENABLE
LLM
C10
10u
FB1
Vin
TP8
R3
0402
U1
EP53AxQ
PVIN
AVIN
ENABLE
VS0
VS1
VS2
NC15
NC16
VOUT
VOUT
NC1
PGND
LLM
Vfb
Vsense
AGND
TP1
C1
N/U
0603
C2
10u
0603
C3
10u
0805
C4
N/U
0805
C5
N/U
0805
TP7
Vout
TP2
TP5
TP6
PGND
R2
N/U
0805
R1
N/U
0805
C9
N/U
0805
Input Protection
U2
6.5V
SMBJ6V5CA
D1
S2A
C8
150u
Vin
PGND

Figure 4: 2.5mmx2.25mm Module Evaluation Board Schematic

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