

128K x 8 Static RAM

Features

- **High Speed**
— 55ns and 70ns availability
- **Voltage range**
— 2.7V–3.6V
- **Ultra low active power**
— Typical active current: 20 mA @ $f = f_{\max}$ (70ns speed)
- **Low standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The WCMA1008U1X is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$) and three-state drivers. These devices have an automa-

tic power-down feature, reducing the power consumption by over 99% when deselected.

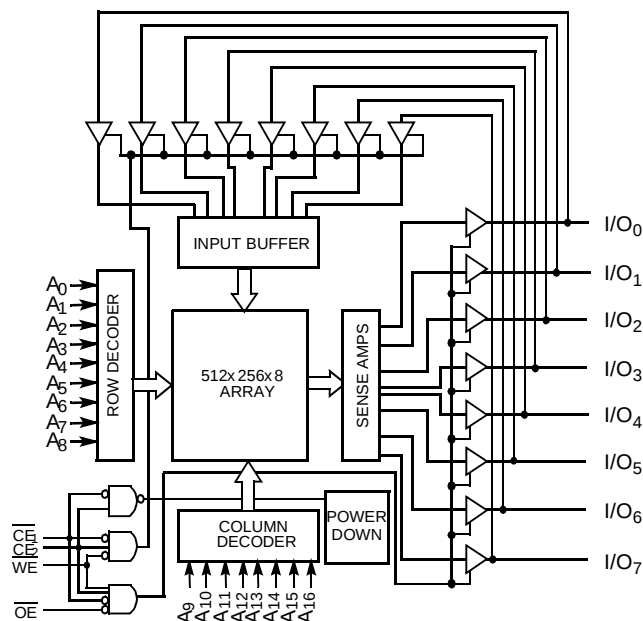
Writing to the device is accomplished by taking Chip Enable one ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and the Chip Enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable one ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

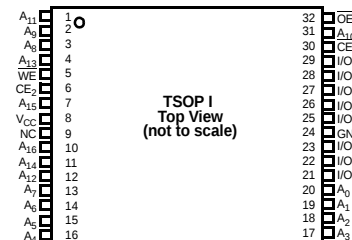
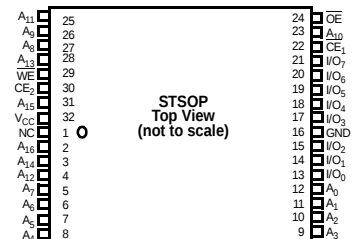
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The WCMA1008U1X is available in a 32 Lead TSOP and STSOP packages.

Logic Block Diagram



Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature-65°C to +150°C

Ambient Temperature with
Power Applied.....55°C to +125°C

Supply Voltage to Ground Potential.....-0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State^[1].....0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1].....-0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage>2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current>200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}
WCMA1008U1X	Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)			
					Operating, I_{CC}		Standby (I_{SB2})	
					$f = f_{max}$		Typ. ^[2]	Max.
	Min.	Typ. ^[2]	Max.		Typ. ^[2]	Max.		
WCMA1008U1X	2.7V	3.0V	3.6V	70 ns	20 mA	40 mA	0.4 μA	30 μA
				55 ns				

Notes:

- $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ C$.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			WCMA1008U1X-70/55			Unit
					Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V		2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V				0.4	V
V _{IH}	Input HIGH Voltage				2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage				−0.5		0.8	V
I _{IX}	Input Leakage Cur- rent	GND ≤ V _I ≤ V _{CC}			−1		+1	μA
I _{OZ}	Output Leakage Cur- rent	GND ≤ V _O ≤ V _{CC} , Output Disabled			−1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6V I _{OUT} = 0 mA CMOS Levels	70ns		20	40	mA
				55ns		23	50	
I _{SB1}	Automatic CE Power-Down Cur- rent— TTL Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, CE ₂ < V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		70ns		15	300	μA
				55ns		17	350	
I _{SB2}	Automatic CE Power-Down Cur- rent— CMOS Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, CE ₂ < 0.3 V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0					0.4	30

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	6	pF
C _{OUT}	Output Capacitance		8	pF

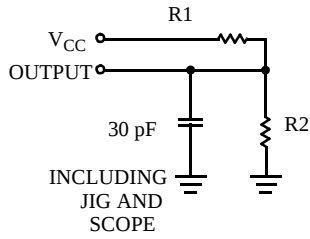
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance ^[3] (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance ^[3] (Junction to Case)		Θ _{JC}	16	°C/W

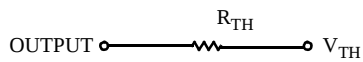
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENINEQUIVALENT

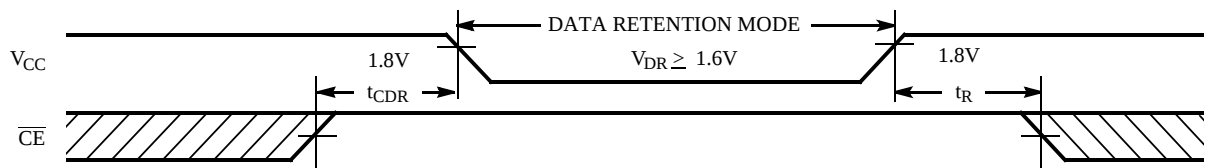


Parameters	3.3V	Unit
R1	1213	Ohms
R2	1378	Ohms
R _{TH}	645	Ohms
V _{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.6			V
I _{CCDR}	Data Retention Current	V _{CC} = 2V, $\overline{CE}_1 \geq V_{CC} - 0.3V$, CE ₂ < 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		0.4	20	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time		0			ns
t _R ^[4]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform



Note:

- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.

Switching Characteristics Over the Operating Range^[5]

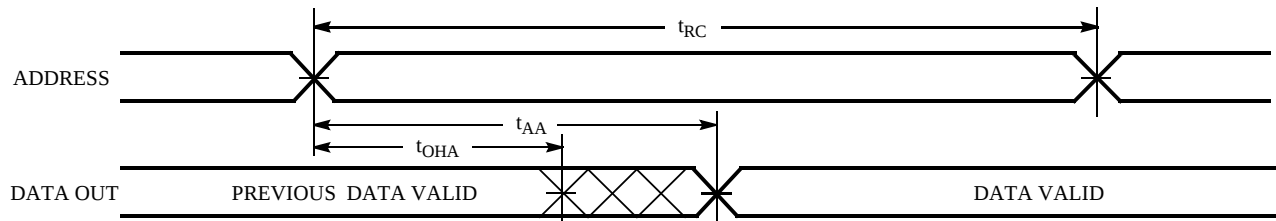
Parameter	Description	WCMA1008U1X-55		WCMA1008U1X-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		10		ns
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[6]	10		10		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6, 7]		20		25	ns
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Low Z ^[6]	10		10		ns
t _{HZCE}	$\overline{CE}_1$ HIGH or CE ₂ LOW to High Z ^[6, 7]		20		25	ns
t _{PU}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Power-Up	0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH or CE ₂ LOW to Power-Down		55		70	ns
WRITE CYCLE ^[8,]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		55		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[6, 7]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	5		5		ns

Notes:

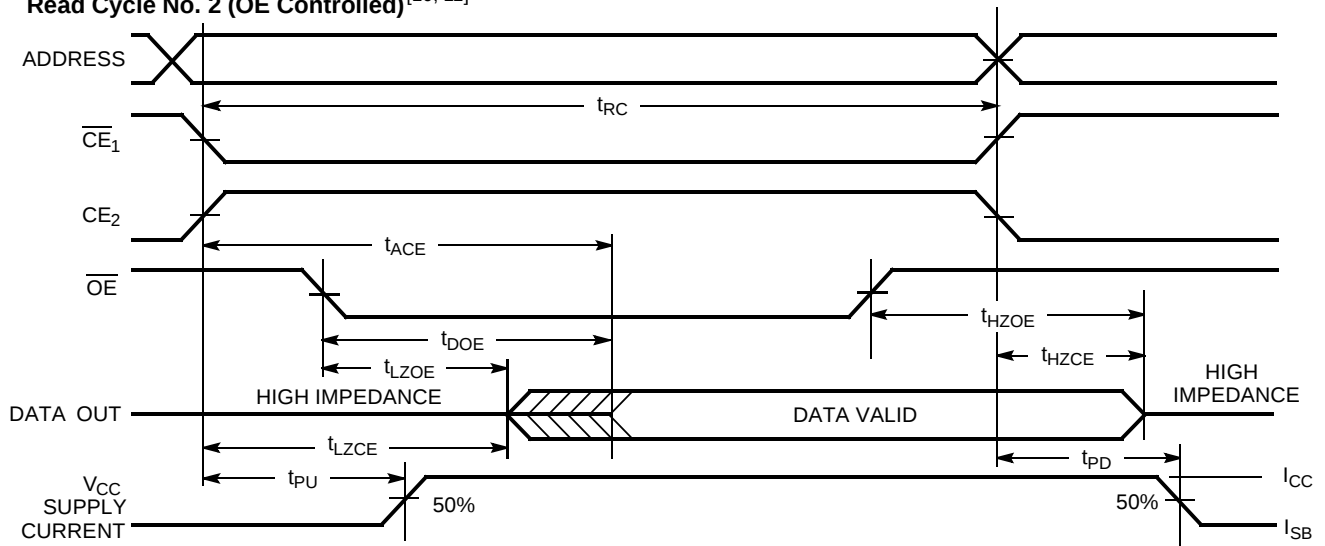
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of $\overline{WE}$, $CE_1 = V_{IL}$ and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [9, 10]

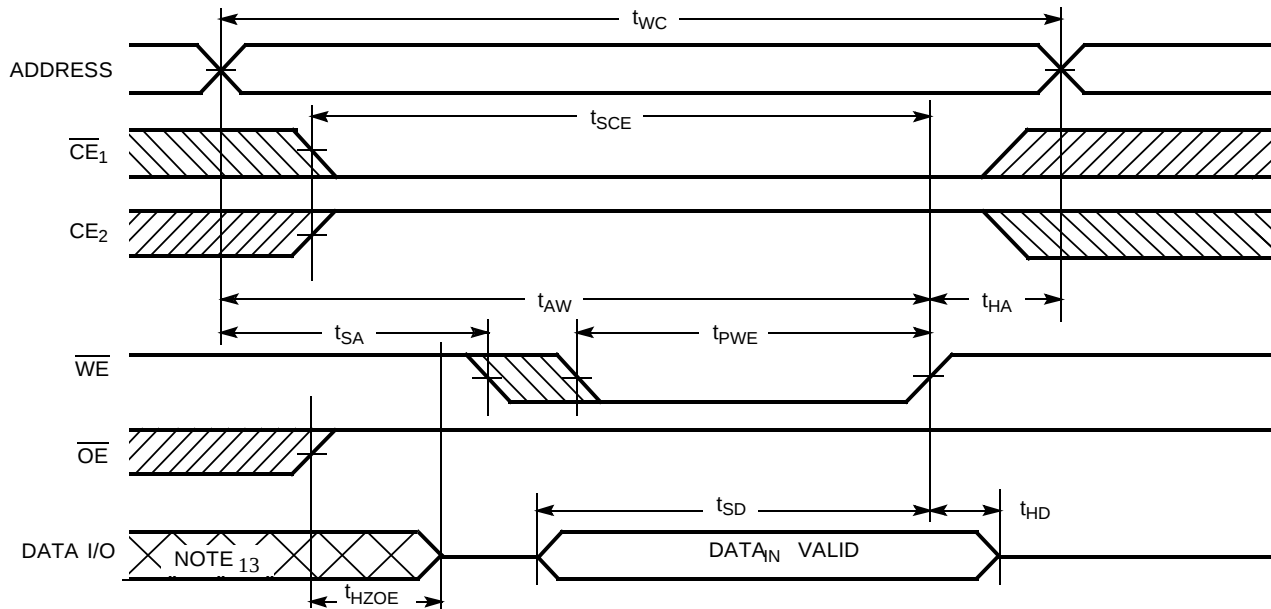
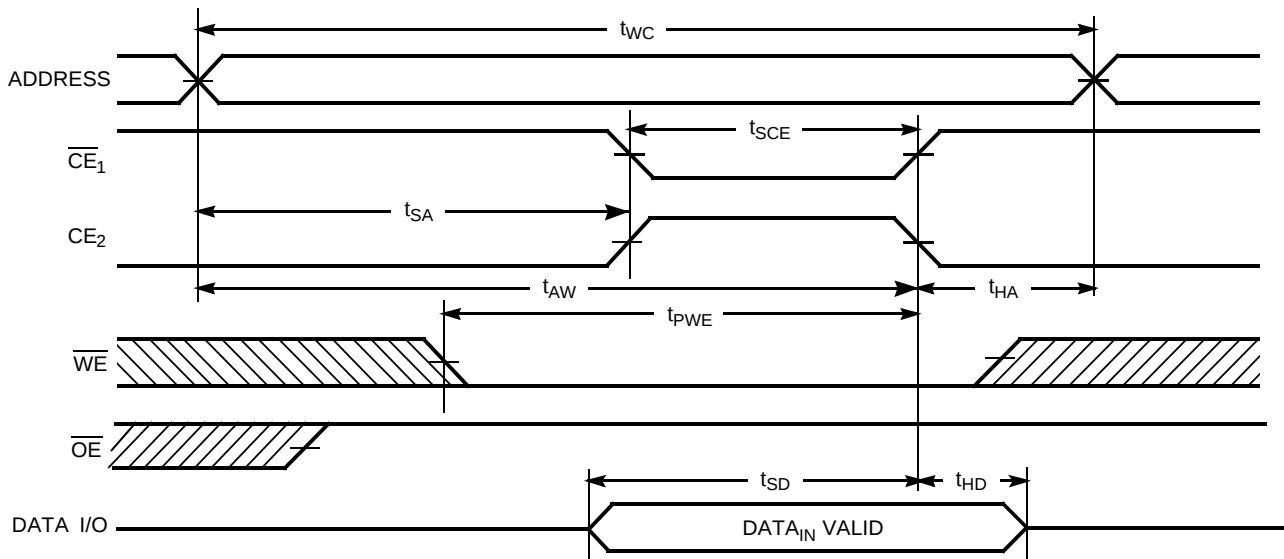


Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [10, 11]



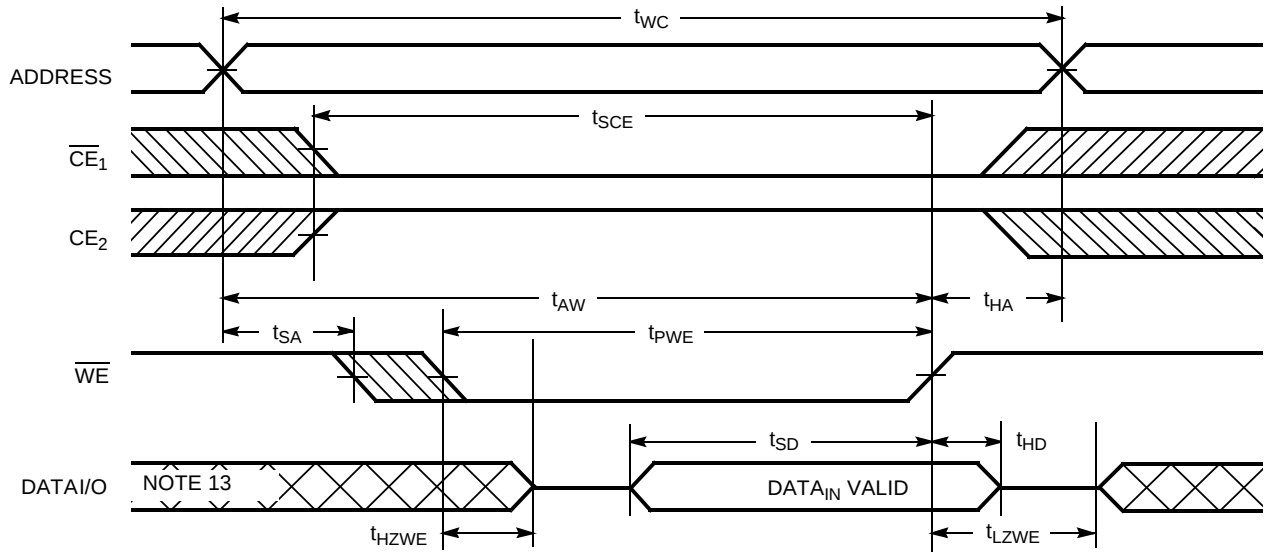
Notes:

9. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}_1 = V_{IL}$, $\text{CE}_2 = V_{IH}$.
10. $\overline{\text{WE}}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{\text{CE}}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) ^[8, 12, 14]

Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE_2 Controlled) ^[8, 12, 14]

Notes:

12. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
13. During this period, the I/Os are in output state and input signals should not be applied.
14. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[14]


Truth Table

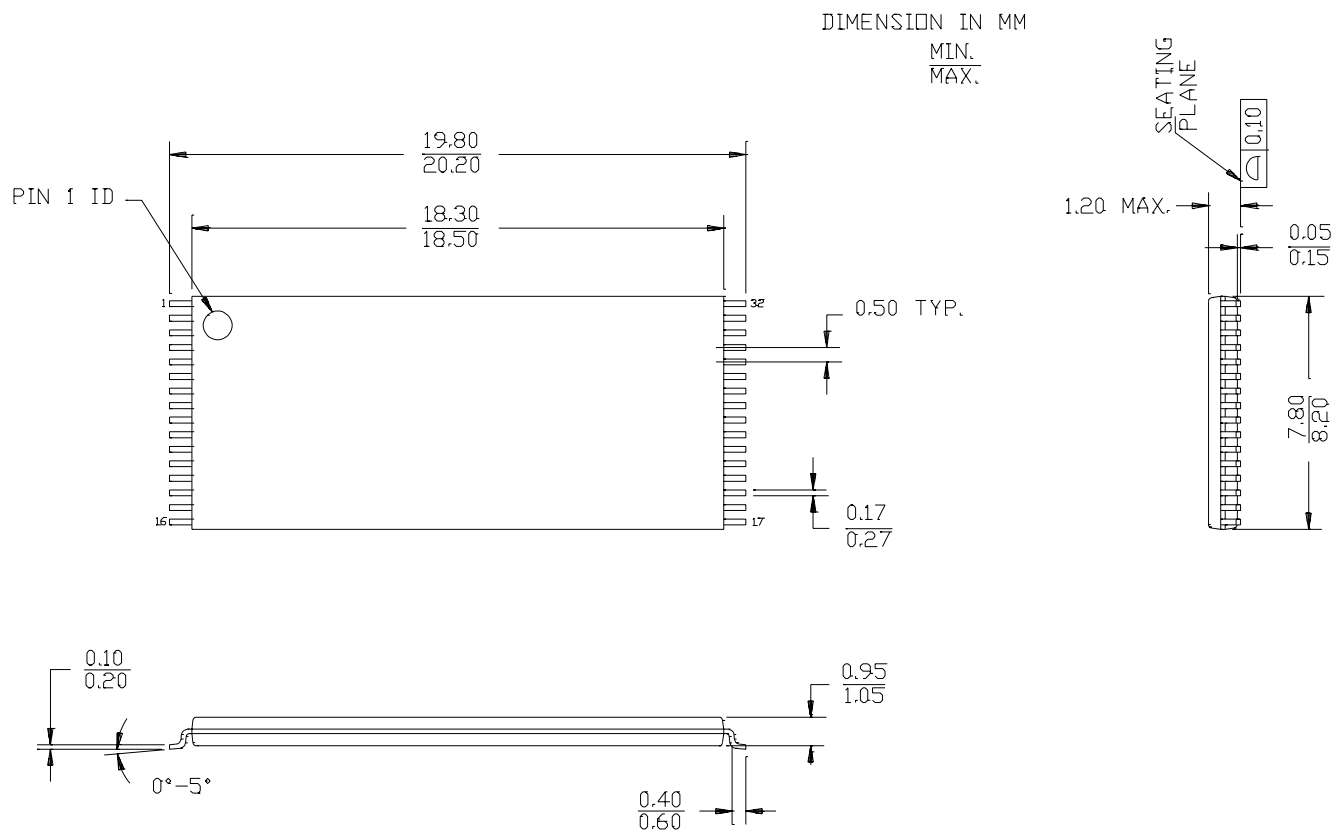
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})

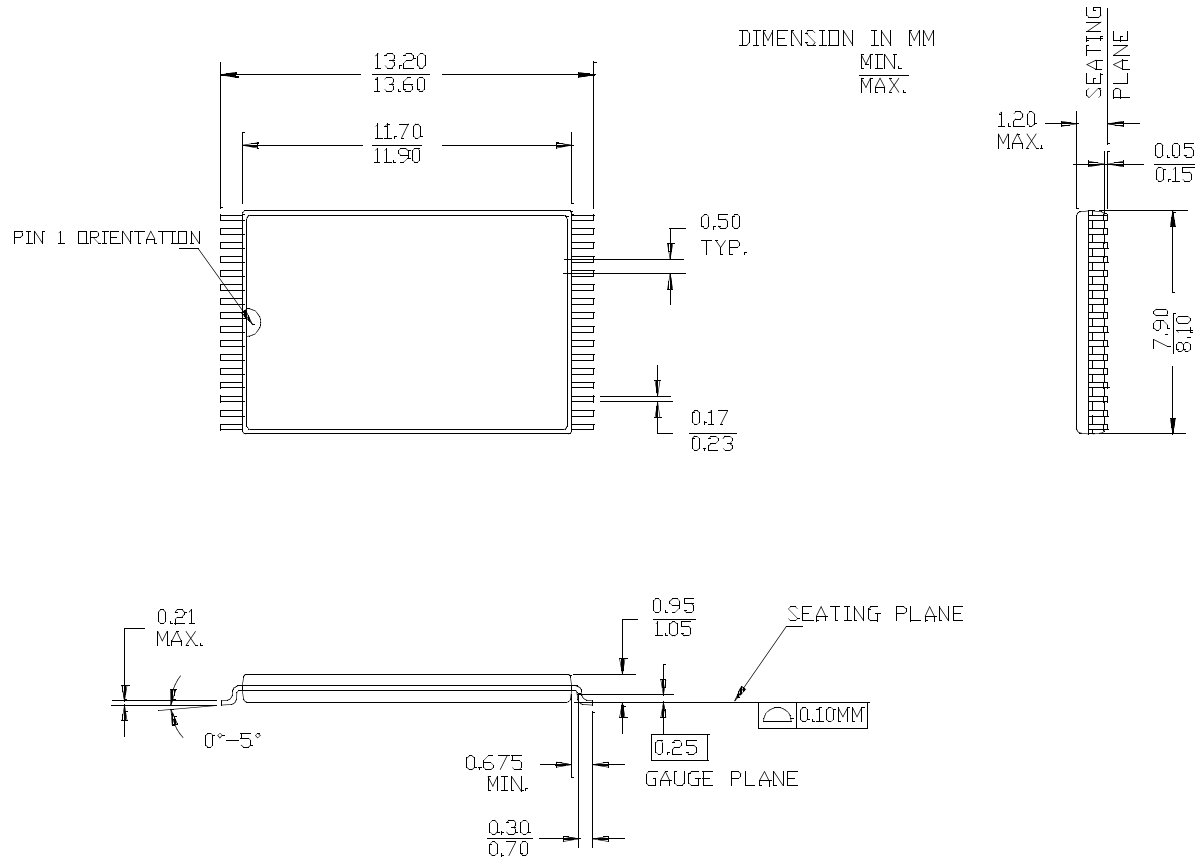
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA1008U1X-TF70	T32	32-Lead TSOP	Industrial
	WCMA1008U1X-SF70	S32	32-Lead STSOP	
55	WCMA1008U1X-TF55	T32	32-Lead TSOP	
	WCMA1008U1X-SF55	S32	32-Lead STSOP	

Package Diagrams

32-Lead Thin Small Outline Package, T32



Package Diagrams (continued)
32-Lead Shrunk Thin Small Outline Package, S32




Document Title: WCMA1008U1X, 128K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14023	115246	4/24/2002	MGN	New Data Sheet

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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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JONHON

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ВЧ соединители, коаксиальные кабели,
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