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FAIRCHILD SEMICONDUCTOR®

May 2009

# FST3257
# Quad 2:1 Multiplexer / Demultiplexer Bus Switch

## Features

- 4Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through the Switch
- Low $I_{CC}$
- Zero Bounce in Flow-Through Node
- Control Inputs Compatible with TTL Level

## Description

The Fairchild Switch FST3257 is a quad 2:1 high-speed CMOS TTL-compatible multiplexer / demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When /OE is LOW, the select pin connects the A port to the selected B port output. When /OE is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

## Ordering Information

| Part Number | Operating Temperature Range | Eco Status | Package | Packing Method |
|---|---|---|---|---|
| FST3257M | -40 to 85°C | RoHS | 16-Lead Small Outline Integrated Circuit (SOIC) JEDEC MS-012,0.150 Narrow | Tubes |
| FST3257MX | -40 to 85°C | | | Tape and Reel |
| FST3257QSC | -40 to 85°C | Green | 16-Lead Quarter Size Outline Package (QSOP) JEDEC MO-137 0.150 Inch Wide | Tubes |
| FST3257QSCX | -40 to 85°C | | | Tape and Reel |
| FST3257MTC | -40 to 85°C | RoHS | 16-Lead Thin Shrink Small Outline Package (TSSOP) JEDEC MO-153, 4mm Wide | Tubes |
| FST3257MTCX | -40 to 85°C | | | Tape and Reel |

*For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

## Pin Assignments

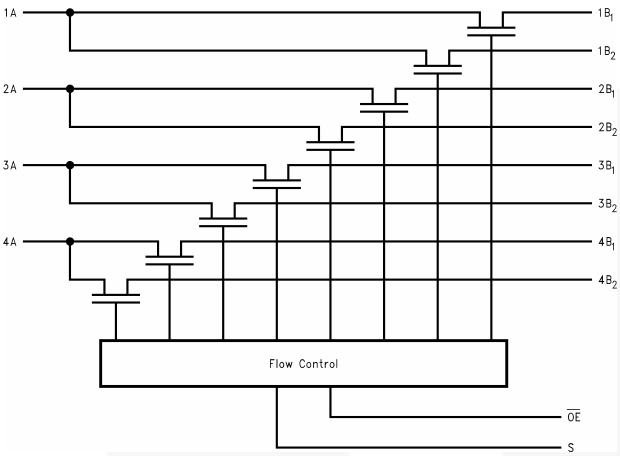



**Figure 1. Logic Diagram**

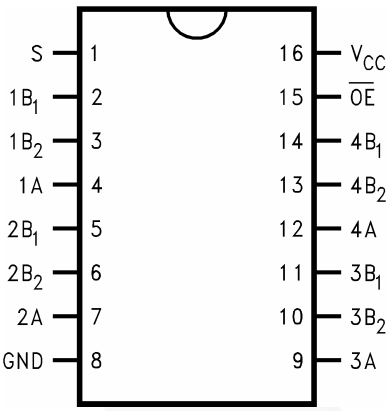



**Figure 2. Connection Diagram**

## Pin Descriptions

| Pin # | Names | Description |
|---|---|---|
| 1 | S | Select Input |
| 2, 3, 5, 6, 10, 11, 13, 14 | $1B_1$, $1B_2$ ,$2B_1$, $2B_2$, $3B_1$, $3B_2$, $4B_1$, $4B_2$ | Bus B |
| 4, 7, 9, 12 | 1A, 2A, 3A, 4A | Bus A |
| 8 | GND | Ground |
| 15 | /OE | Bus Switch Enables |
| 16 | VCC | Supply Voltage |

## Truth Table

| Select Inputs | Bus Switch Enabled | Function |
|---|---|---|
| S | Logic Level HIGH | Disconnected |
| Logic Level LOW | Logic Level LOW | $A=B_1$ |
| Logic Level HIGH | Logic Level LOW | $A=B_2$ |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 | +7.0 | V |
| $V_S$ | DC Switch Voltage | -0.5 | +7.0 | V |
| $V_{IN}$ | DC Input Voltage[1] | -0.5 | +7.0 | V |
| $I_{IK}$ | DC Input Current | | -50 | mA |
| $I_{OUT}$ | DC Output Sink Current | | 128 | mA |
| $I_{CC}/I_{GND}$ | DC $V_{CC}$/GND Current | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | -65 | +150 | °C |

**Note**:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Operating | | 3.0 | 5.5 | V |
| $V_{IN}$ | Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | | 0 | 5.5 | V |
| $t_r, t_f$ | Input Rise and Fall Time | Switch Control Input | 0 | 5 | ns/V |
| | | Switch I/O | 0 | DC | |
| $T_A$ | Free Air Operating Temperature | | -40 | +85 | °C |

**Note**:

2. Unused control inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$=-40 to +85°C | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[3] | Max. | |
| $V_{IK}$ | Clamp Diode Voltage | $I_{IN}$=-18mA | 4.5 | | | -1.2 | V |
| $V_{IH}$ | High-Level Input Voltage | | 3.0 to 3.6[5] | 1.8 | | | V |
| | | | 4.0 to 5.5 | 2.0 | | | |
| $V_{IL}$ | Low-Level Input Voltage | | 3.0 to 3.6[5] | | | 0.7 | V |
| | | | 4.0 to 5.5 | | | 0.8 | |
| $I_{IN}$ | Input Leakage Current | $0 \le V_{IN} \le 5.5$ | 5.5 | | | ±1.0 | µA |
| $I_{OZ}$ | Off-state Leakage Current | $0 \le A, B \le V_{CC}$ | 5.5 | | | ±1.0 | µA |
| $R_{ON}$ | Switch On Resistance[4] | $V_{IN}$=0V, $I_{IN}$=64mA | 3.3[5] | | 13 | 20 | Ω |
| | | $V_{IN}$=0V, $I_{IN}$=30mA | 3.3[5] | | 28 | 40 | |
| | | $V_{IN}$=2.4V, $I_{IN}$=15mA | 3.3[5] | | 200 | 230 | |
| | | $V_{IN}$=2.4V, $I_{IN}$=15mA | 3.0[5] | | 210 | 250 | |
| | | $V_{IN}$=0V, $I_{IN}$=64mA | 4.5 | | 4 | 7 | |
| | | $V_{IN}$=0V, $I_{IN}$=30mA | 4.5 | | 4 | 7 | |
| | | $V_{IN}$=2.4V, $I_{IN}$=15mA | 4.5 | | 8 | 15 | |
| | | $V_{IN}$=2.4V, $I_{IN}$=15mA | 4.0 | | 11 | 20 | |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$=$V_{CC}$ or GND, $I_{OUT}$=0, | 5.5 | | | 3 | µA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per input | One Input at 3.4V, Other inputs at $V_{CC}$ or GND | 5.5 | | | 2.5 | mA |

**Notes**:

3. Typical values are at nominal $V_{CC}$ for the $V_{CC}$ range and $T_A$=25°C.
4. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.
5. This parameter is guaranteed by design, but is not tested.

## AC Electrical Characteristics

| Symbol | Parameter | Conditions | $T_A$=-40 to +85°C, $C_L$= 50pF, RU=RD=500Ω | | | | | | Units | Figure |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$= 4.5 to 5.5V | | $V_{CC}$=4.0V | | $V_{CC}$=3.0 to 3.6V(7) | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{PHL}$,$t_{PLH}$ | Propagation Delay Bus to Bus(6) | $V_{IN}$=Open | | 0.25 | | 0.25 | | 0.25 | ns | Figure 3 Figure 4 |
| | Propagation Delay Select to Bus A(6) | | | | | | 1.0 | 6.8 | | |
| $t_{PZH}$,$t_{PZL}$ | Output Enable Time, Select to Bus B | $V_{IN}$=7V for $t_{PZL}$ $V_{IN}$=Open for $t_{PZH}$ | 1.0 | 5.0 | | 5.5 | 1.0 | 7.9 | ns | Figure 3 Figure 4 |
| | Output Enable Time, Select to Bus /OE | | | | | | 1.0 | 8.5 | | |
| $t_{PHZ}$,$t_{PLZ}$ | Output Disable Time, Select to Bus B | $V_{IN}$=7V for $t_{PLZ}$ $V_{IN}$=Open for $t_{PHZ}$ | 1.5 | 5.3 | | 5.6 | 1.0 | 9.9 | ns | Figure 3 Figure 4 |
| | Output Disable Time, Select to Bus /OE | | | | | | 1.5 | 9.9 | | |

**Notes:**

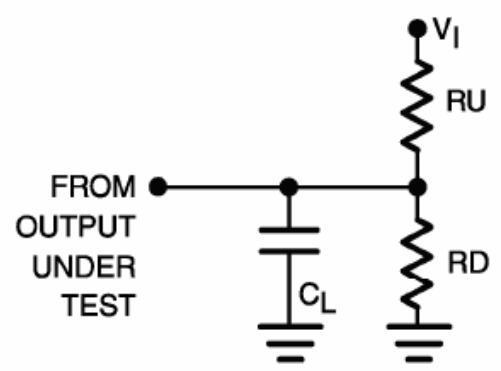
6. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
7. These parameters are guaranteed by design, but not tested.

## Capacitance

$T_A$=+25°C, f=1MHz. Capacitance is characterized by not tested.

| Symbol | Parameter | | Conditions | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Control Pin Input Capacitance | | $V_{CC}$=5.0V | 3.0 | | pF |
| $C_{I/O}$ | Input/Output Capacitance | A Port | $V_{CC}$ /OE=5.0V | 7.0 | | pF |
| | | B Port | | 5.0 | | |
| | | A Port | $V_{CC}$ /OE=3.3V | 3.0 | | pF |
| | | B Port | | 3.5 | | |

## AC Loadings and Waveforms




**Notes:**

8. Input driven by 50Ω source terminated in 50Ω.
9. $C_L$ included load and stray capacitance.
10. Input PRR=1.0MHz, tw=500ns.

**Figure 3. AC Test Circuit**

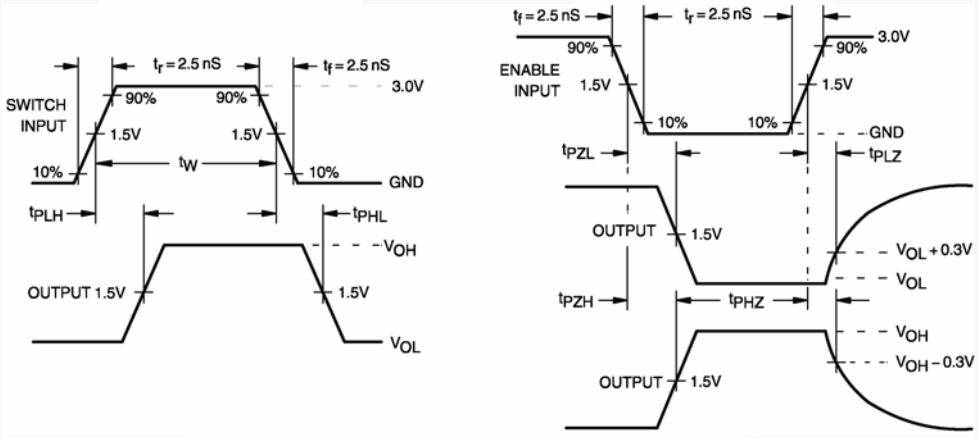



**Figure 4. AC Waveforms**

## Physical Dimensions

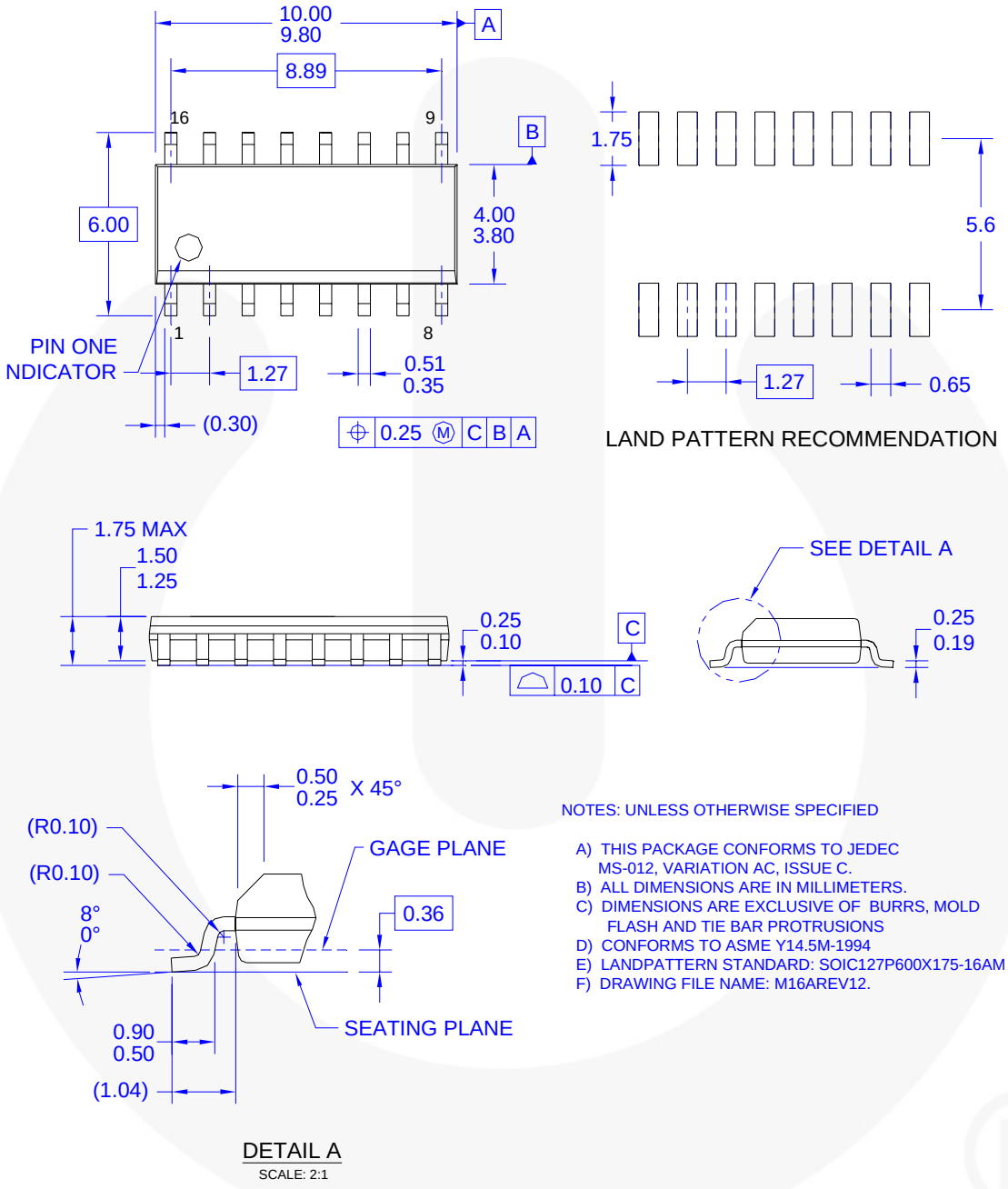



**Figure 5. 16-Lead Small Outline Integrated Circuit (SOIC) JEDEC MS-012,0.150 Narrow**

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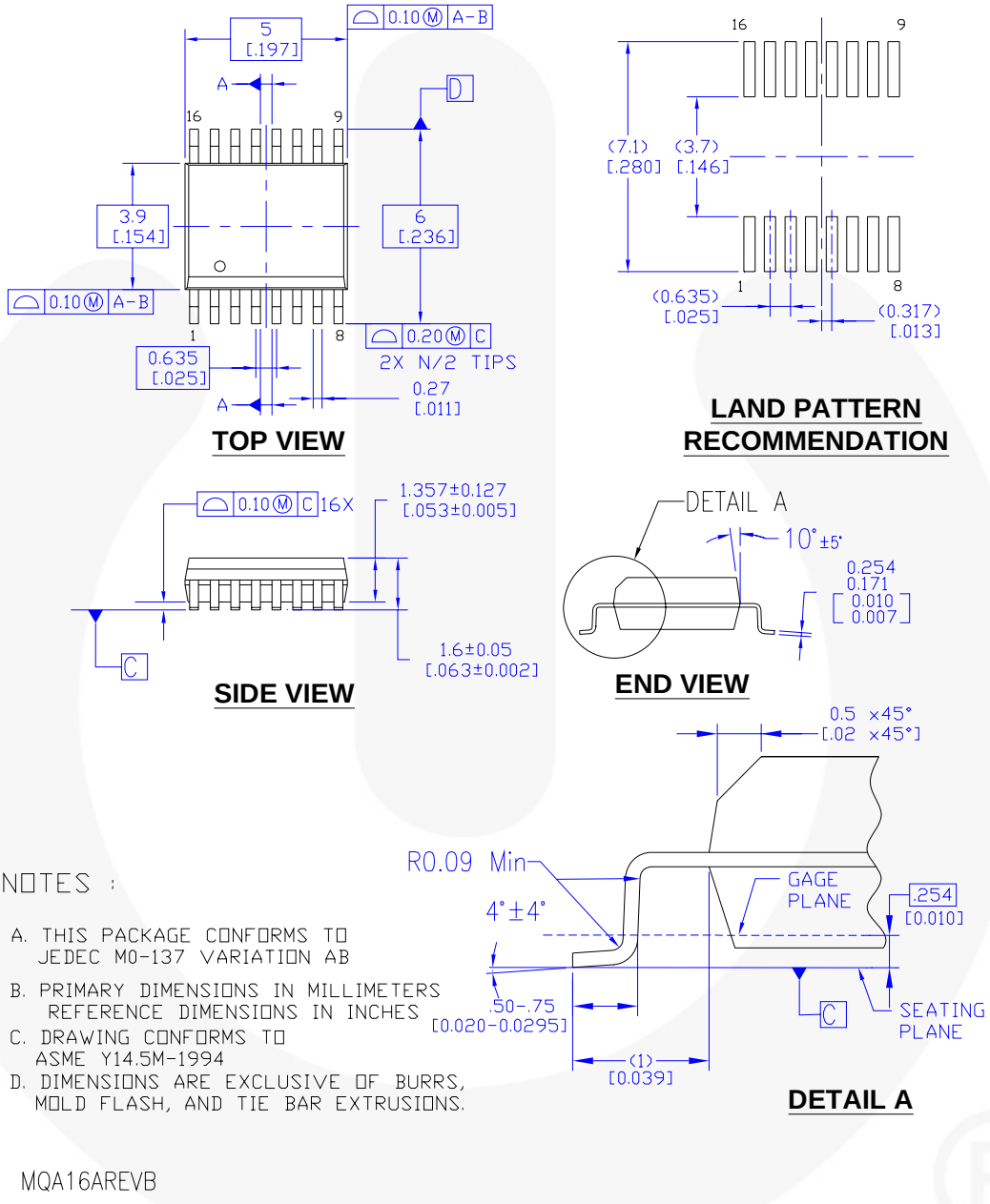


**Figure 6. 16-Lead Quarter Size Outline Package (QSOP) JEDEC MO-137 0.150 Inch Wide**

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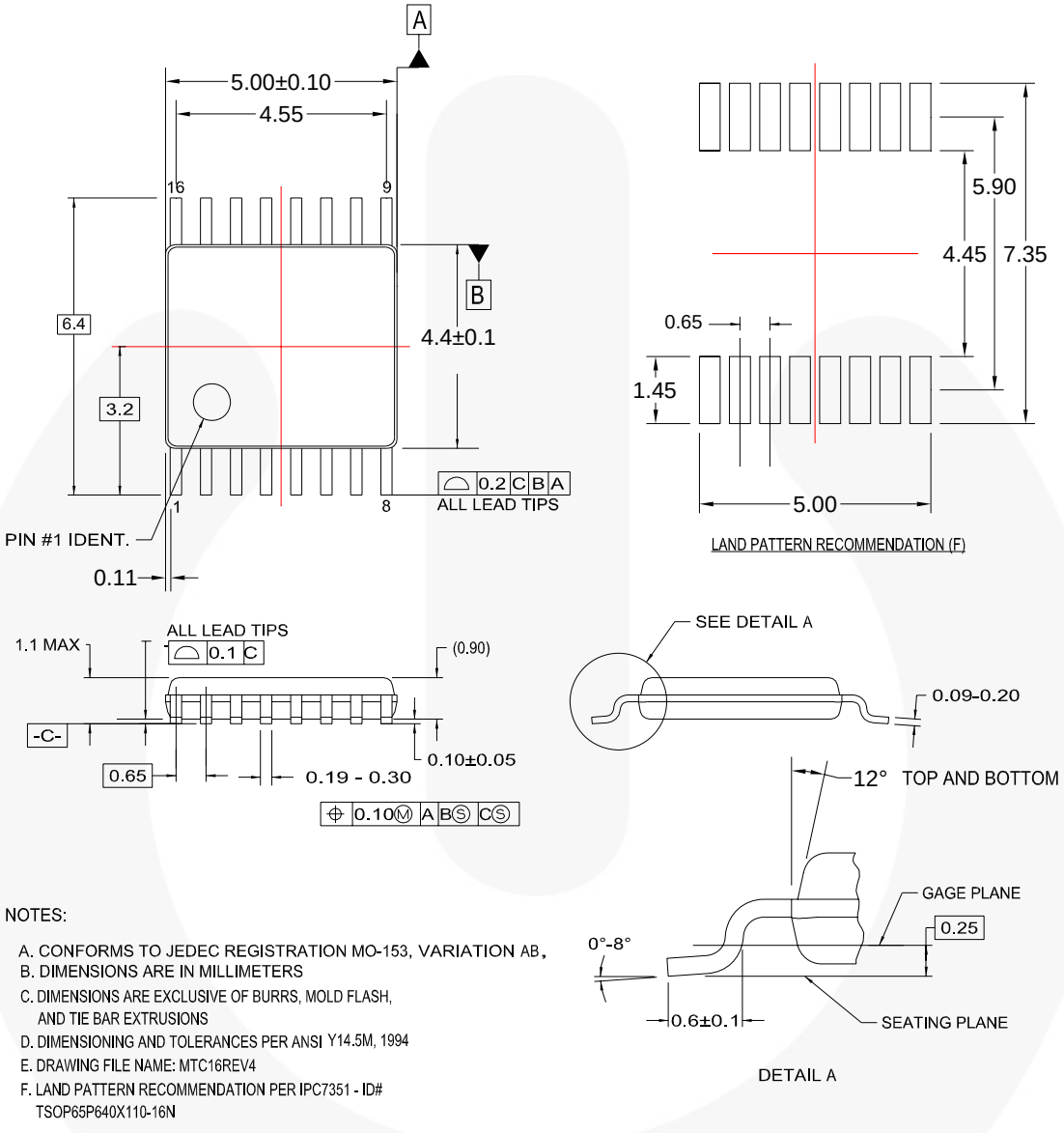


**Figure 7. 16-Lead Thin Shrink Small Outline Package (TSSOP) MO-153, 4.4mm Wide**

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