

NCP6335

Configurable 4.0 A Step Down Converter - Transient Load Helper

The NCP6335 is a synchronous buck converter optimized to supply the different sub systems of portable applications powered by one cell Li-Ion or three cell Alkaline/NiCd/NiMH batteries. The device is able to deliver up to 4.0 A, with programmable output voltage from 0.6 V to 1.4 V. It can share the same output rail with another DC-to-DC converter and works as a transient load helper. Operation at a 3 MHz switching frequency allows the use of small components. Synchronous rectification and automatic PWM/PFM transitions improve overall solution efficiency. The NCP6335 is in a space saving, low profile 2.0 x 1.6 mm CSP-20 package.

Features

- Input Voltage Range from 2.3 V to 5.5 V: Battery and 5 V Rail Powered Applications
- Programmable Output Voltage: 0.6 V to 1.4 V in 6.25 mV Steps
- Modular Output Stage Drive Strength for Increased Efficiency Depending on the Output Current
- 3 MHz Switching Frequency with on Chip Oscillator
- Uses 470 nH Inductor and 2 x 22 μ F Capacitors for Optimized Footprint and Solution Thickness
- PFM/PWM Operation for Optimum Increased Efficiency
- Low 35 μ A Quiescent Current
- I²C Control Interface with Interrupt and Dynamic Voltage Scaling Support
- Enable Pins, Power Good/Fail Signaling
- Thermal protections and Temperature Management
- Transient Load Helper: Share the Same Rail with Another DCDC
- Small 2.0 x 1.6 mm / 0.4 mm pitch CSP Package
- These are Pb-Free Devices

Typical Applications

- Smartphones
- Webtablets

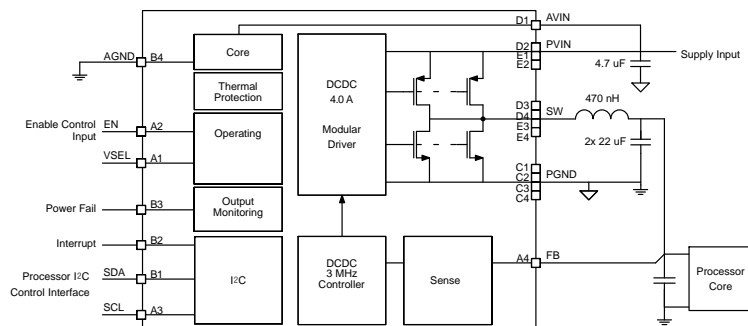


Figure 1. Typical Application Circuit



ON Semiconductor®

<http://onsemi.com>



WLCSP20
CASE 568AG

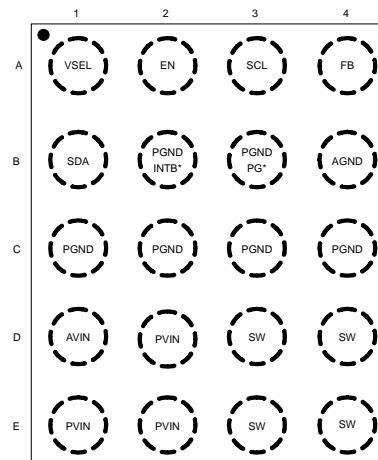
MARKING DIAGRAM



- x = D1: Prototype
- = F: 3.5 A
- = D: 2.5 A (Stand-Alone)
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- = Pb-Free Package

Pb-Free indicator, G or microdot (▪), may or may not be present

PIN OUT



(Top View)

*Optional

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

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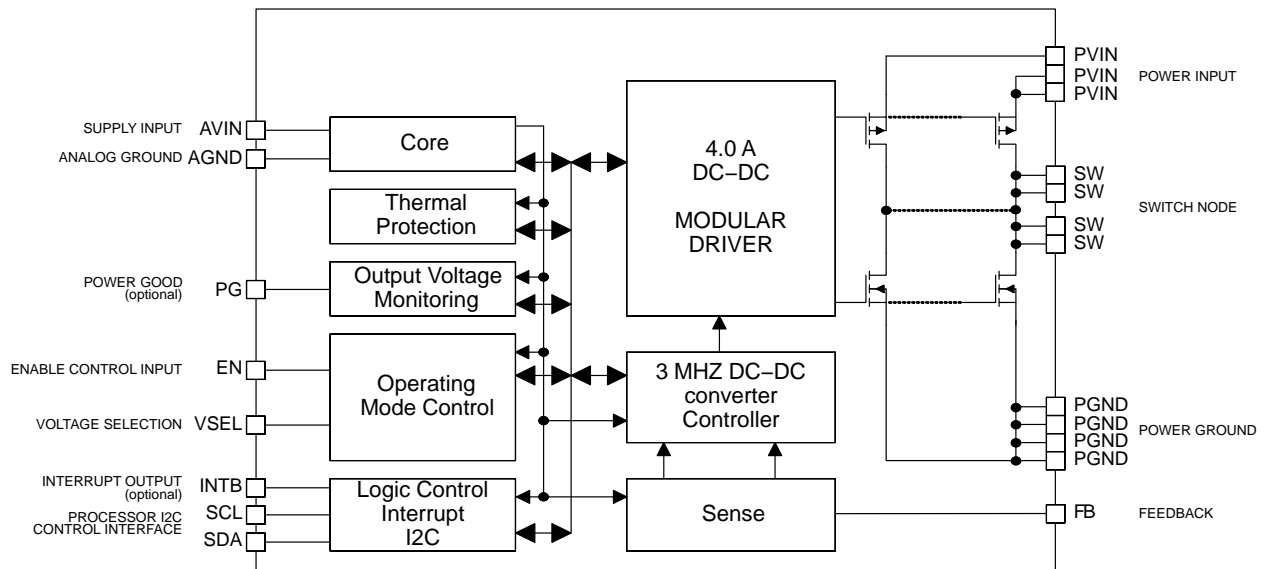


Figure 2. Simplified Block Diagram

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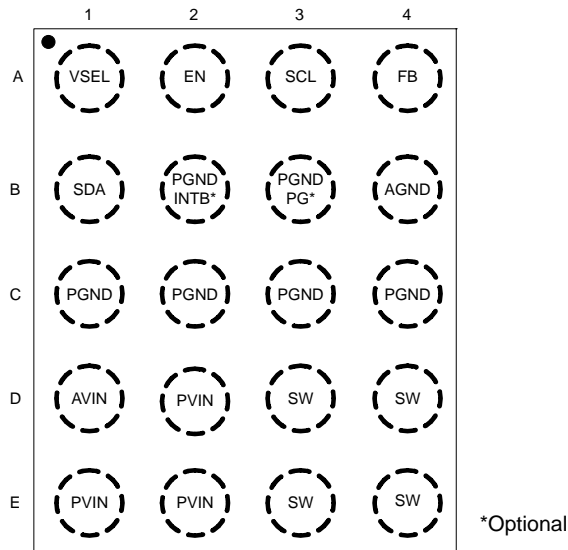


Figure 3. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

| Pin | Name | Type | Description |
|-----|------|------|-------------|
|-----|------|------|-------------|

REFERENCE

| | | | |
|----|------|---------------|--|
| D1 | AVIN | Analog Input | Analog Supply. This pin is the device analog and digital supply. Could be connected directly to the VIN plane just next to the 4.7 μ F PVIN capacitor or to a dedicated 1.0 μ F ceramic capacitor. |
| B4 | AGND | Analog Ground | Analog Ground. Analog and digital modules ground. Must be connected to the system ground. |

CONTROL AND SERIAL INTERFACE

| | | | |
|----|--------------|---------------------------------|---|
| A2 | EN | Digital Input | Enable Control. Active high will enable the part. There is an internal pull down resistor on this pin. |
| A1 | VSEL | Digital Input | Output voltage / Mode Selection. The level determines which of two programmable configurations to utilize (operating mode / output voltage). There is an internal pull down resistor on this pin; could be left open if not used. |
| A3 | SCL | Digital Input | I ² C interface Clock line. There is an internal pull down resistor on this pin; could be left open if not used |
| B1 | SDA | Digital Input/Output | I ² C interface Bi-directional Data line. There is an internal pull down resistor on this pin; could be left open if not used |
| B3 | PGND PG | Digital Output Analog ground | Power Good open drain output. If not used has to be connected to ground plane |
| B2 | PGND INTB | Digital Output Analog Ground | Interrupt open drain output. If not used has to be connected to ground plane |

DCDC CONVERTER

| | | | |
|-------------------|------|--------------|---|
| D2, E1, E2 | PVIN | Power Input | Switch Supply. These pins must be decoupled to ground by a 4.7 μ F ceramic capacitor. It should be placed as close as possible to these pins. All pins must be used with short heavy connections. |
| D3, D4, E3, E4 | SW | Power Output | Switch Node. These pins supply drive power to the inductor. Typical application uses 0.470 μ H inductor; refer to application section for more information. All pins must be used with short heavy connections. |
| C1, C2, C3, C4 | PGND | Power Ground | Switch Ground. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high-density current flow in a limited PCB track, a local ground plane that connects all PGND pins together is recommended. Analog and power grounds should only be connected together in one location with a trace. |
| A4 | FB | Analog Input | Feedback Voltage input. Must be connected to the output capacitor positive terminal with a trace, not to a plane. This is the positive input to the error amplifier. |

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MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------------------------|---|---------|
| Analog and power pins: AVIN, PVIN, SW, PG, INTB, FB | V _A | -0.3 to + 6.0 | V |
| Digital pins: SCL, SDA, EN, VSEL, Pin: Input Voltage Input Current | V _{DG} I _{DG} | -0.3 to V _A +0.3 ≤ 6.0 10 | V mA |
| Human Body Model (HBM) ESD Rating are (Note 1) | ESD HBM | 2500 | V |
| Charged Device Model (CDM) ESD Rating are (Note 1) | ESD CDM | 1250 | V |
| Latch Up Current: (Note 2) Digital Pins All Other Pins | I _{LU} | ±10 ±100 | mA |
| Storage Temperature Range | T _{STG} | -65 to + 150 | °C |
| Maximum Junction Temperature | T _{JMAX} | -40 to +150 | °C |
| Moisture Sensitivity (Note 3) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests: Human Body Model (HBM) ±2.5 kV per JEDEC standard: JESD22-A114, Charged Device Model (CDM) ±1.25 kV per JEDEC standard: JESD22-C101 Class IV.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

OPERATING CONDITIONS (Note 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|-----------------------|-----|------|------|------|
| AV _{IN} , PV _{IN} | Power Supply | | 2.3 | | 5.5 | V |
| T _A | Ambient Temperature Range | | -40 | 25 | +85 | °C |
| T _J | Junction Temperature Range (Note 5) | | -40 | 25 | +125 | °C |
| R _{θJA} | Thermal Resistance Junction to Ambient (Note 6) | CSP-20 on Demo-board | - | 55 | - | °C/W |
| P _D | Power Dissipation Rating (Note 7) | T _A ≤ 85°C | - | 727 | - | mW |
| P _D | Power Dissipation Rating (Note 7) | T _A = 65°C | - | 1090 | - | mW |
| L | Inductor for DCDC converter (Note 4) | | - | 0.47 | - | μH |
| Co | Output Capacitor for DCDC Converter (Note 4) | | 30 | - | 150 | μF |
| Cin | Input Capacitor for DCDC Converter (Note 4) | | 4.7 | - | - | μF |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Including de-ratings (Refer to the Application Information section of this document for further details)
5. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
6. The R_{θJA} is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6335EV board. It is a multilayer board with 1-once internal power and ground planes and 2-once copper traces on top and bottom of the board.
7. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

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ELECTRICAL CHARACTERISTICS (Note 9)

Min and Max Limits apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AVIN = PVIN = 3.6\text{ V}$ and default configuration, unless otherwise specified.

Typical values are referenced to $T_A = +25^\circ\text{C}$, $AVIN = PVIN = 3.6\text{ V}$ and default configuration, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

SUPPLY CURRENT: PINS AVIN – PVINx

| | | | | | | |
|--------------------|---------------------------------|---|---|-----|----|---------------|
| $I_{Q\text{ PWM}}$ | Operating quiescent current PWM | DCDC active in Forced PWM no load | – | 10 | 20 | mA |
| $I_{Q\text{ PFM}}$ | Operating quiescent current PFM | DCDC active in Auto mode no load – minimal switching | – | 35 | 70 | μA |
| I_{SLEEP} | Product sleep mode current | EN high, DCDC off or EN low and (VSEL high or Sleep_Mode high) $V_{IN} = 2.5\text{ V}$ to 5.5 V | – | 7 | 15 | μA |
| I_{OFF} | Product in off mode | EN, VSEL and Sleep_Mode low $V_{IN} = 2.5\text{ V}$ to 5.5 V | – | 0.8 | 5 | μA |

DCDC CONVERTER

| | | | | | | |
|-------------------------|--------------------------------|---|------|----------|------|------------------|
| PV_{IN} | Input Voltage Range | | 2.3 | – | 5.5 | V |
| I_{OUTMAX} | Maximum Output Current | $I_{\text{peak}}[1..0] = 00$ (Note 10) | 2.5 | – | – | A |
| | | $I_{\text{peak}}[1..0] = 01$ (Note 10) | 3.0 | – | – | |
| | | $I_{\text{peak}}[1..0] = 10$ (Note 10) | 3.5 | – | – | |
| | | $I_{\text{peak}}[1..0] = 11$ (Note 10) | 4.0 | – | – | |
| ΔV_{OUT} | Output Voltage DC Error | Forced PWM mode, V_{in} range, I_{OUT} from 0 mA and 300 mA | –1 | – | 1 | % |
| | | Forced PWM mode, V_{in} range, I_{OUT} up to I_{OUTMAX} (Note 10) | –1 | – | 1 | |
| | | Auto mode, V_{in} range, I_{OUT} up to I_{OUTMAX} (Note 10) | –1 | – | 2 | |
| F_{SW} | Switching Frequency | | 2.85 | 3 | 3.15 | MHz |
| R_{ONHS} | P–Channel MOSFET On Resistance | From PV_{IN} to SW $V_{IN} = 5.0\text{ V}$ | – | 45 | 80 | $\text{m}\Omega$ |
| R_{ONLS} | N–Channel MOSFET On Resistance | From SW to PGND $V_{IN} = 5.0\text{ V}$ | – | 22 | 40 | $\text{m}\Omega$ |
| I_{PK} | Peak Inductor Current | Open loop – $I_{\text{peak}}[1..0] = 00$ | 3.0 | 3.4 | 3.8 | A |
| | | Open loop – $I_{\text{peak}}[1..0] = 01$ | 3.6 | 4.0 | 4.4 | |
| | | Open loop – $I_{\text{peak}}[1..0] = 10$ | 4.0 | 4.4 | 4.8 | |
| | | Open loop – $I_{\text{peak}}[1..0] = 11$ | 4.6 | 5.0 | 5.4 | |
| DC_{LOAD} | Load Regulation | I_{OUT} from 300 mA to I_{OUTMAX} | – | –0.2 | – | %/A |
| DC_{LINE} | Line Regulation | $I_{\text{OUT}} = 300\text{ mA}$ $2.3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ | – | 0 | – | % |
| AC_{LOAD} | Transient Load Response | $t_r = t_s = 100\text{ ns}$ Load step 1.2 A (Note 10) | – | ± 40 | – | mV |
| D | Maximum Duty Cycle | | – | 100 | – | % |
| t_{START} | Turn on time | Time from EN transitions from Low to High to 90% of Output Voltage ($\text{DELAY}[2..0] = 000\text{b}$) | – | 80 | 100 | μs |
| | | Time from EN transitions from Low to High to $V_{\text{OUT}} = 1.127\text{ V}$ (Note 10) | | | 150 | |
| R_{DISDCDC} | DCDC Active Output Discharge | $V_{\text{OUT}} = 1.15\text{ V}$ | – | 25 | 35 | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Devices that use non–standard supply voltages which do not conform to the intent I²C bus system levels must relate their input levels to the V_{DD} voltage to which the pull–up resistors R_p are connected.

9. Refer to the Application Information section of this data sheet for more details.

10. Guaranteed by design and characterized.

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ELECTRICAL CHARACTERISTICS (Note 9)

Min and Max Limits apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AVIN = PVIN = 3.6\text{ V}$ and default configuration, unless otherwise specified.

Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $AVIN = PVIN = 3.6\text{ V}$ and default configuration, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

EN, VSEL

| | | | | | | |
|-----------|---|--|------|------|------|---------------|
| V_{IH} | High input voltage | | 1.05 | – | – | V |
| V_{IL} | Low input voltage | | – | – | 0.4 | V |
| T_{FTR} | Digital input X Filter | EN, VSEL rising and falling DBN_Time = 01 (Note 10) | 0.5 | – | 4.5 | μs |
| I_{PD} | Digital input X Pull-Down (input bias current) | | – | 0.05 | 1.00 | μA |

PG (Optional)

| | | | | | | |
|-------------|--------------------------------------|---|----------|----------|---------|---------------|
| V_{PGL} | Power Good Threshold | Falling edge as a percentage of nominal output voltage | 86 | 90 | 94 | % |
| V_{PGHYS} | Power Good Hysteresis | | 0 | 3 | 5 | % |
| T_{RT} | Power Good Reaction Time for DCDC | Falling (Note 10) Rising (Note 10) | – 3.5 | 3.5 – | – 14 | μs |
| V_{PGL} | Power Good low output voltage | $I_{PG} = 5\text{ mA}$ | – | – | 0.2 | V |
| PG_{LK} | Power Good leakage current | 3.6 V at PG pin when power good valid | – | – | 100 | nA |
| V_{PGH} | Power Good high output voltage | Open drain | – | – | 5.5 | V |

INTB (Optional)

| | | | | | | |
|-------------|--------------------------|-----------------------------------|---|---|-----|----|
| V_{INTBL} | INTB low output voltage | $I_{INT} = 5\text{ mA}$ | 0 | – | 0.2 | V |
| V_{INTBH} | INTB high output voltage | Open drain | – | – | 5.5 | V |
| $INTB_{LK}$ | INTB leakage current | 3.6 V at INTB pin when INTB valid | – | – | 100 | nA |

I²C

| | | | | | | |
|--------------|----------------------------------|------------------------------------|-----------------------|---|-----|-----|
| V_{I2CINT} | High level at SCL/SCA line | | 1.7 | – | 5.0 | V |
| V_{I2CIL} | SCL, SDA low input voltage | SCL, SDA pin (Note 8, 10) | – | – | 0.5 | V |
| V_{I2CIH} | SCL, SDA high input voltage | SCL, SDA pin (Note 8, 10) | 0.8 * V_{I2CINT} | – | – | V |
| V_{I2COL} | SDA low output voltage | $I_{SINK} = 3\text{ mA}$ (Note 10) | – | – | 0.4 | V |
| F_{SCL} | I ² C clock frequency | (Note 10) | – | – | 3.4 | MHz |

TOTAL DEVICE

| | | | | | | |
|----------------|-------------------------------------|--------------------------------|----|-----|-----|--------------------|
| V_{UVLO} | Under Voltage Lockout | V_{IN} falling | – | – | 2.3 | V |
| V_{UVLOH} | Under Voltage Lockout Hysteresis | V_{IN} rising | 60 | – | 200 | mV |
| T_{SD} | Thermal Shut Down Protection | | – | 150 | – | $^{\circ}\text{C}$ |
| $T_{WARNING}$ | Warning Rising Edge | | – | 135 | – | $^{\circ}\text{C}$ |
| T_{PWTH} | Pre – Warning Threshold | I ² C default value | – | 105 | – | $^{\circ}\text{C}$ |
| T_{SDH} | Thermal Shut Down Hysteresis | | – | 30 | – | $^{\circ}\text{C}$ |
| $T_{WARNINGH}$ | Thermal warning Hysteresis | | – | 15 | – | $^{\circ}\text{C}$ |
| T_{PWTHH} | Thermal pre-warning Hysteresis | | – | 6 | – | $^{\circ}\text{C}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Devices that use non-standard supply voltages which do not conform to the intent I²C bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_P are connected.

9. Refer to the Application Information section of this data sheet for more details.

10. Guaranteed by design and characterized.

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TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6\text{ V}$, $T_J = +25^\circ\text{C}$, $DCDC = 1.15\text{ V}$ (Unless otherwise noted). $L = 0.47\ \mu\text{H}$ PIFE20161B – $C_{OUT} = 2 \times 22\ \mu\text{F}$ 0603, $C_{IN} = 4.7\ \mu\text{F}$ 0603

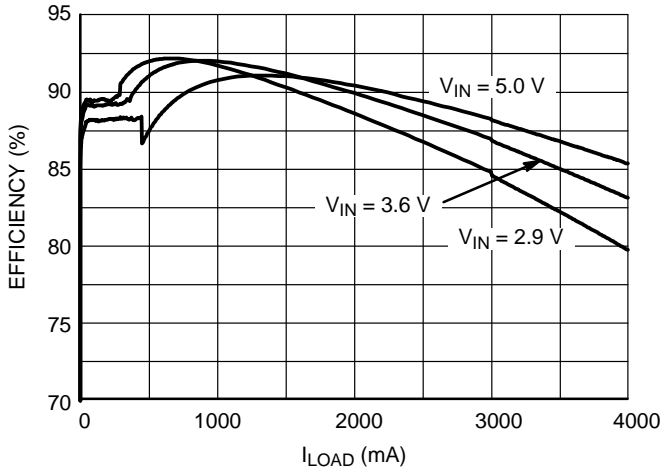


Figure 4. Efficiency vs I_{LOAD} and V_{IN}
 $V_{OUT} = 1.39375\text{ V}$, SPM6530 Inductor

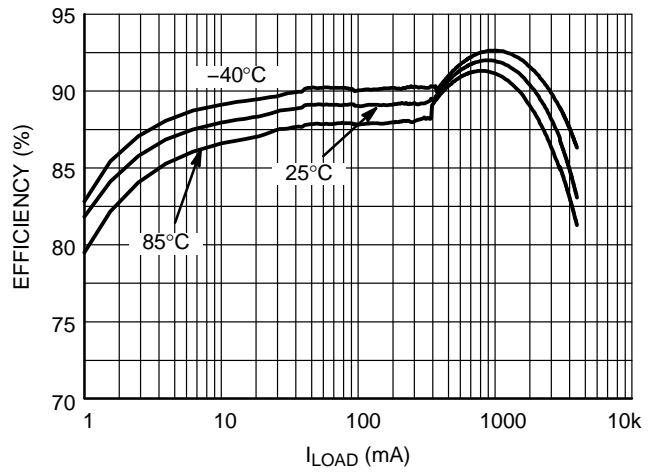


Figure 5. Efficiency vs I_{LOAD} and Temperature
 $V_{OUT} = 1.39375\text{ V}$, SPM6530 Inductor

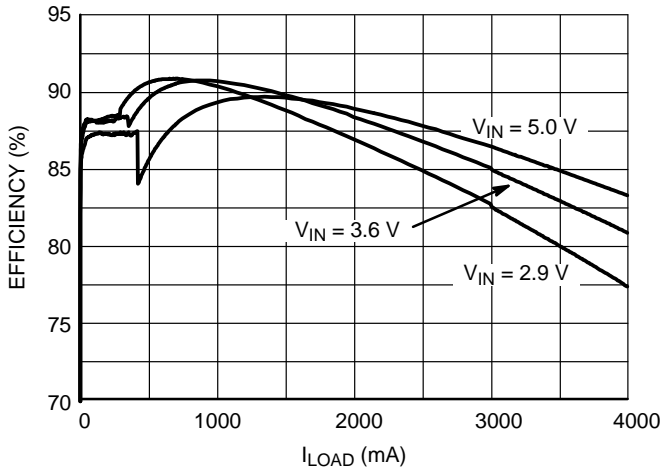


Figure 6. Efficiency vs I_{LOAD} and V_{IN}
 $V_{OUT} = 1.15\text{ V}$, SPM6530 Inductor

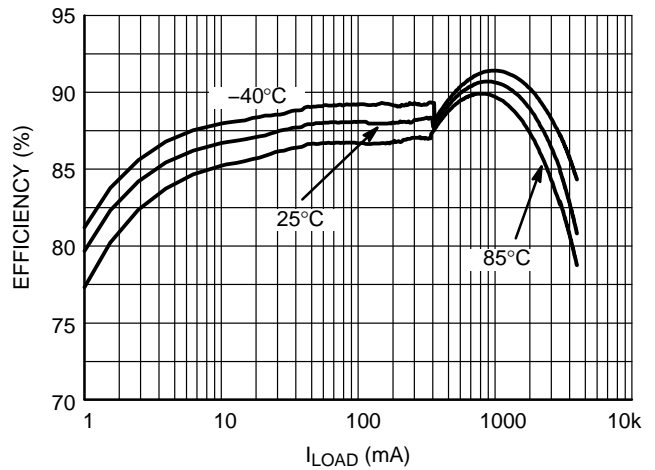


Figure 7. Efficiency vs I_{LOAD} and Temperature
 $V_{OUT} = 1.15\text{ V}$, SPM6530 Inductor

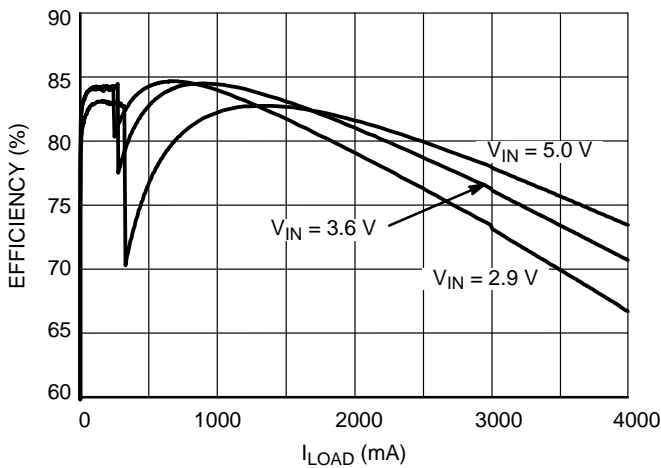


Figure 8. Efficiency vs I_{LOAD} and V_{IN}
 $V_{OUT} = 0.60\text{ V}$, SPM6530 Inductor

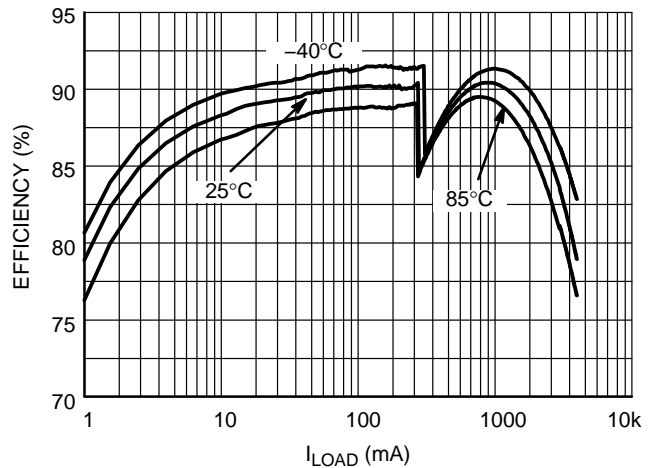


Figure 9. Efficiency vs I_{LOAD} and Temperature
 $V_{OUT} = 0.60\text{ V}$, SPM6530 Inductor

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TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6\text{ V}$, $T_J = +25^\circ\text{C}$, DCDC = 1.15 V (Unless otherwise noted). $L = 0.47\ \mu\text{H}$ PIFE20161B – $C_{OUT} = 2 \times 22\ \mu\text{F}$ 0603, $C_{IN} = 4.7\ \mu\text{F}$ 0603

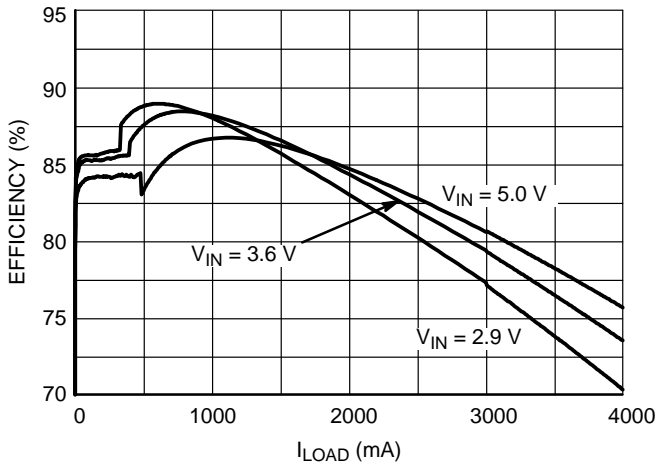


Figure 10. Efficiency vs I_{LOAD} and V_{IN}
 $V_{OUT} = 1.15\text{ V}$, PIFE20161B Inductor

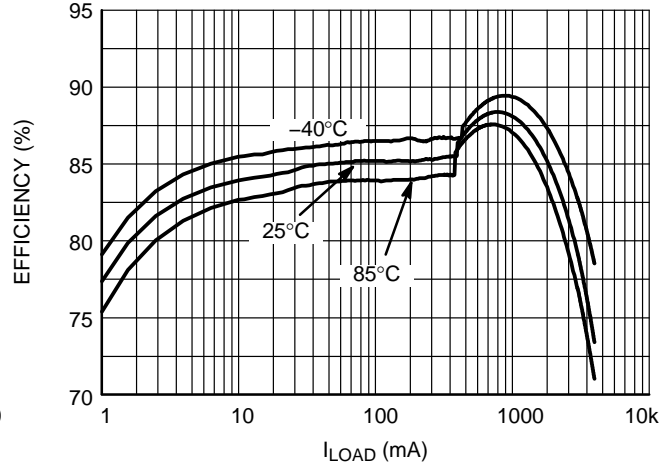


Figure 11. Efficiency vs I_{LOAD} and Temperature
 $V_{OUT} = 1.15\text{ V}$, PIFE20161B Inductor

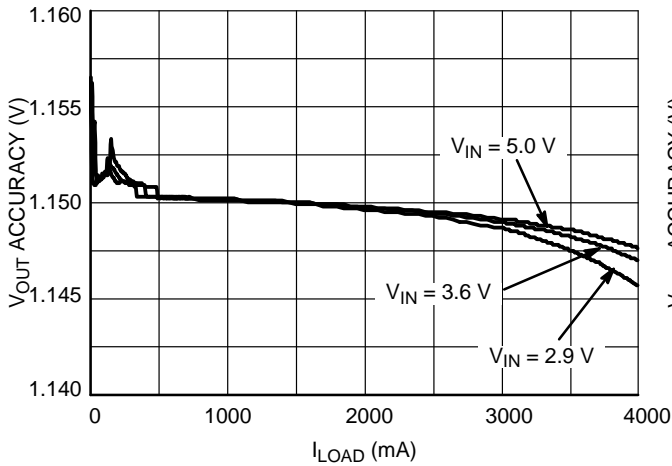


Figure 12. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}
 $V_{OUT} = 1.15\text{ V}$

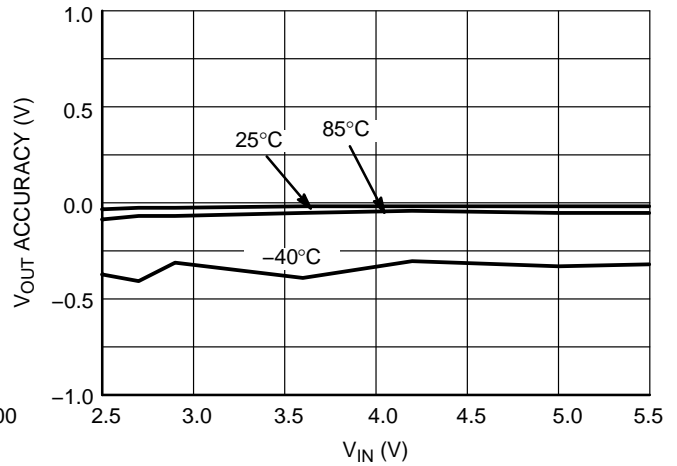


Figure 13. V_{OUT} Accuracy vs V_{IN} and Temperature
 $V_{OUT} = 1.15\text{ V}$, $I_{LOAD} = 2.0\text{ A}$

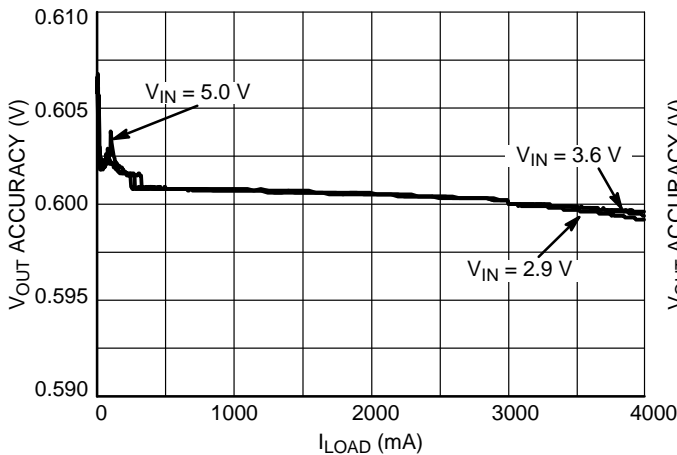


Figure 14. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}
 $V_{OUT} = 0.60\text{ V}$

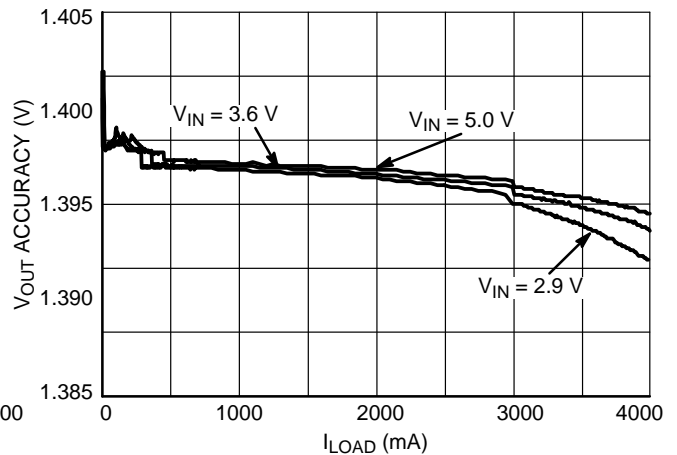


Figure 15. V_{OUT} accuracy vs I_{LOAD} and V_{IN}
 $V_{OUT} = 1.39375\text{ V}$

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TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6\text{ V}$, $T_J = +25^\circ\text{C}$, $DCDC = 1.15\text{ V}$ (Unless otherwise noted). $L = 0.47\ \mu\text{H}$ PIFE20161B – $C_{OUT} = 2 \times 22\ \mu\text{F}$ 0603, $C_{IN} = 4.7\ \mu\text{F}$ 0603

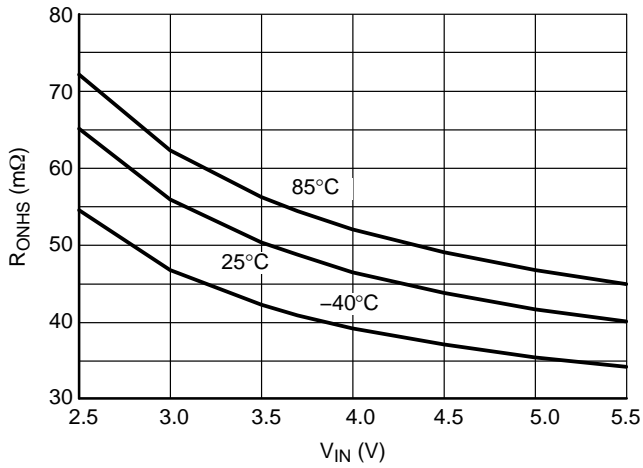


Figure 16. HSS R_{ON} vs V_{IN} and Temperature

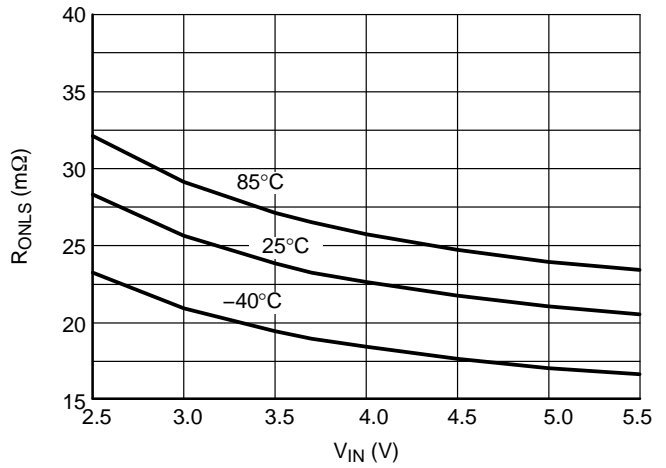


Figure 17. LSS R_{ON} vs V_{IN} and Temperature

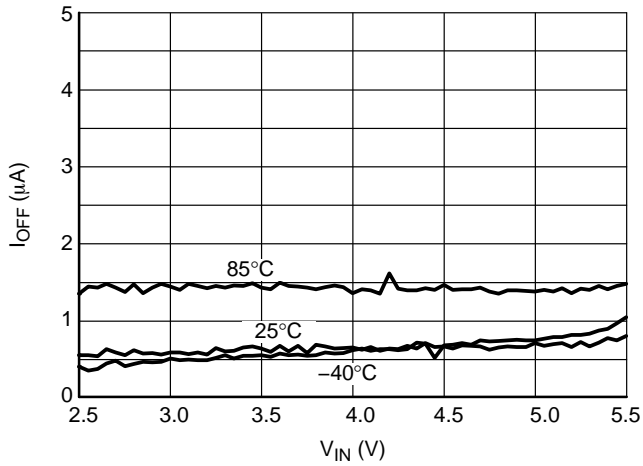


Figure 18. I_{OFF} vs V_{IN} and Temperature

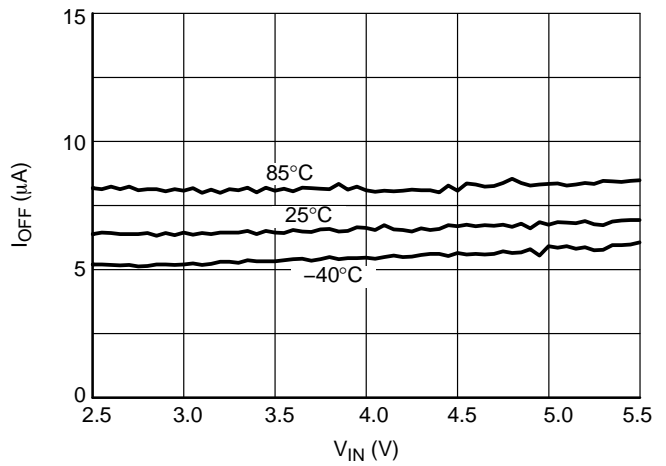


Figure 19. I_{SLEEP} vs V_{IN} and Temperature

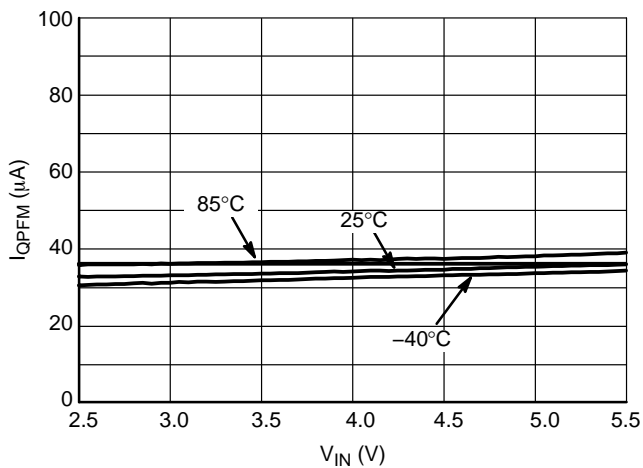


Figure 20. I_{QPFM} vs V_{IN} and Temperature

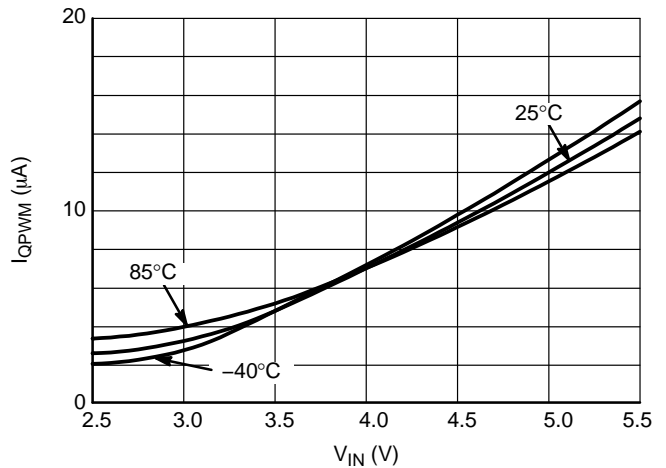


Figure 21. I_{QPWM} vs V_{IN} and Temperature

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TYPICAL OPERATING CHARACTERISTICS

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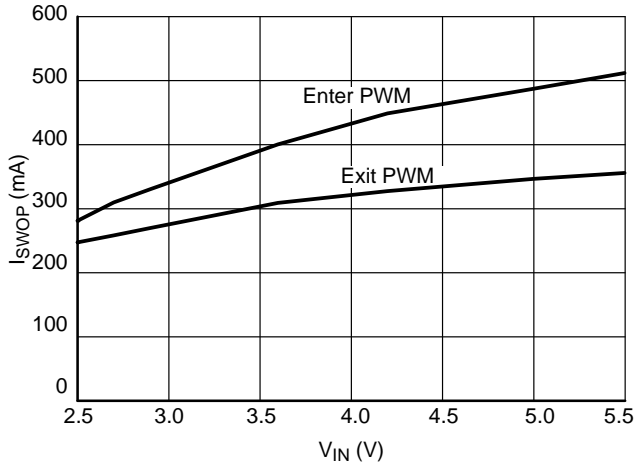


Figure 22. Switchover Point $V_{OUT} = 1.15\text{ V}$

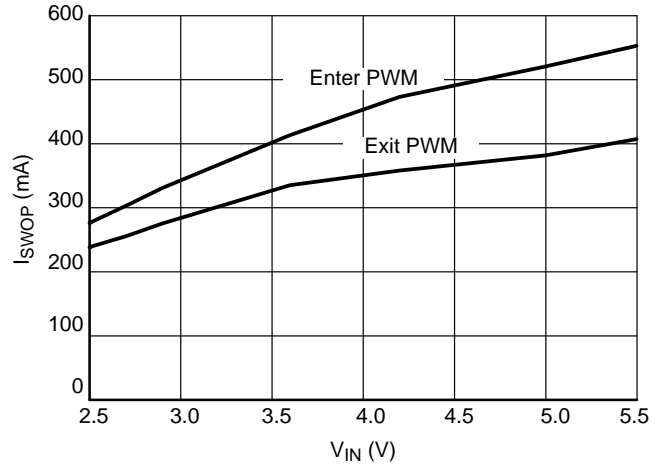


Figure 23. Switchover Point $V_{OUT} = 1.39375\text{ V}$

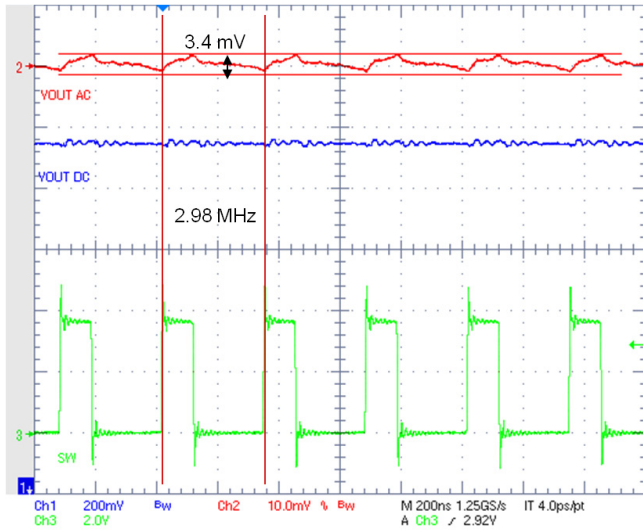


Figure 24. PWM Ripple

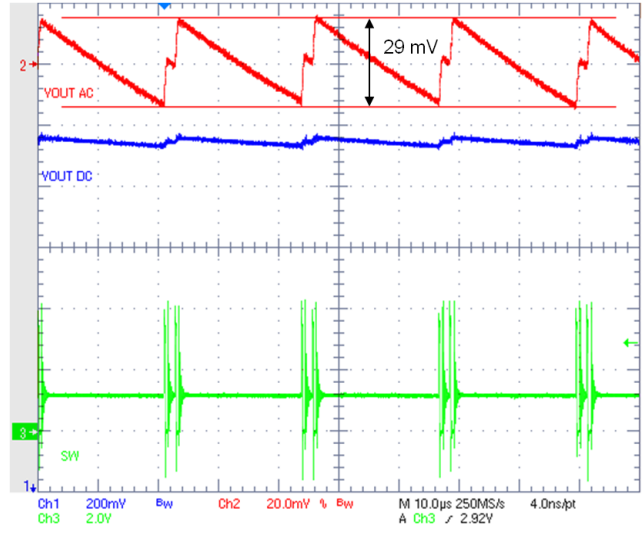


Figure 25. PFM Ripple

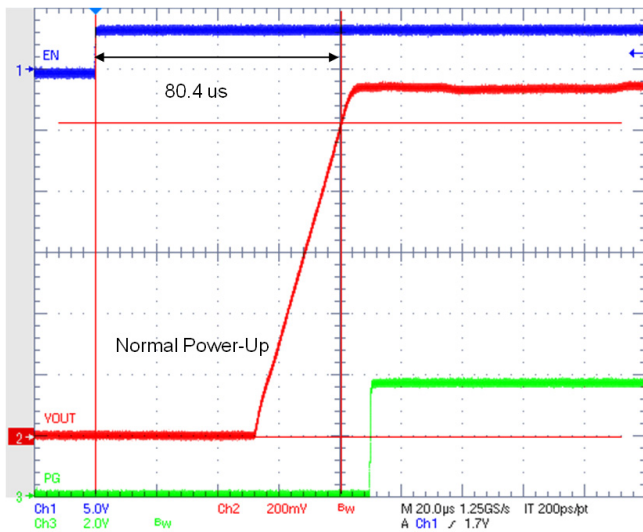


Figure 26. Normal Power Up, $V_{OUT} = 1.15\text{ V}$

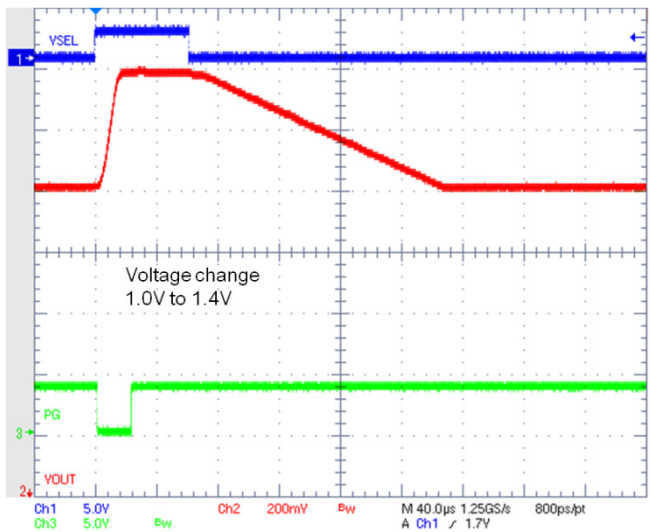


Figure 27. DVS Transition $1.0\text{ V} - 1.39375\text{ V}$

NCP6335

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6\text{ V}$, $T_J = +25^\circ\text{C}$, DCDC = 1.15 V (Unless otherwise noted). $L = 0.47\ \mu\text{H}$ PIFE20161B – $C_{OUT} = 2 \times 22\ \mu\text{F}$ 0603, $C_{IN} = 4.7\ \mu\text{F}$ 0603

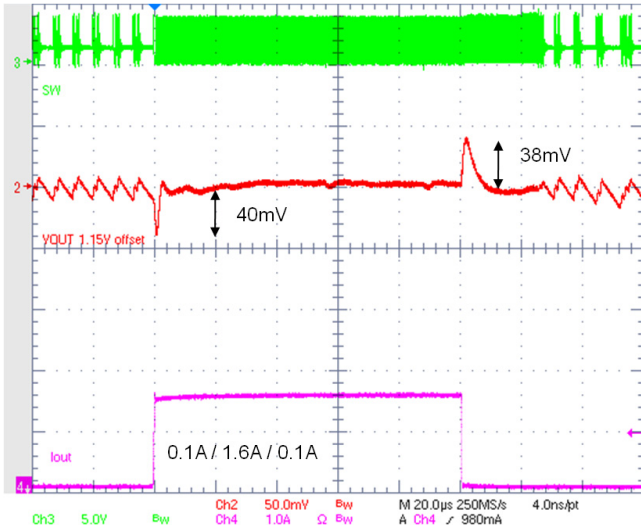


Figure 28. Transient Load 0.1 – 1.6 A Auto Mode

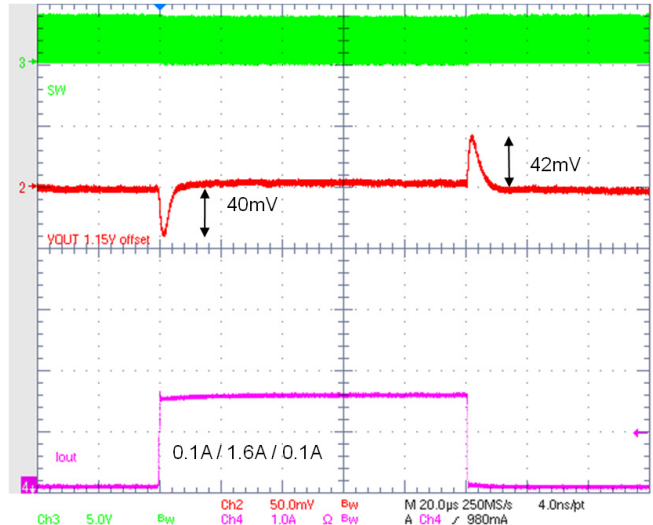


Figure 29. Transient Load 0.1 – 1.6 A Forced PWM Mode

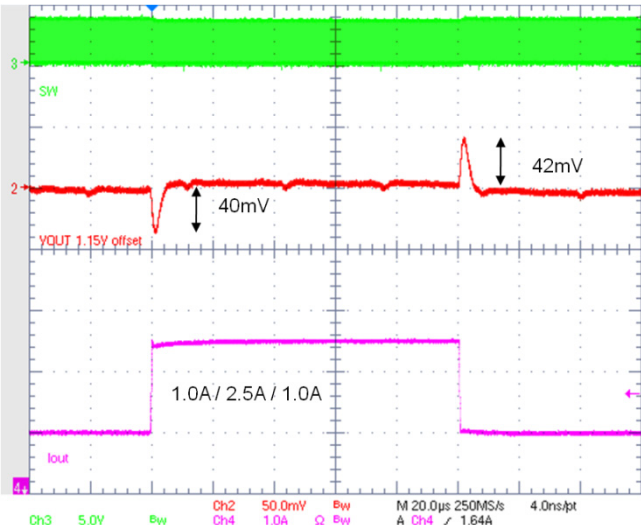


Figure 30. Transient Load 1.0 – 2.5 A Auto Mode

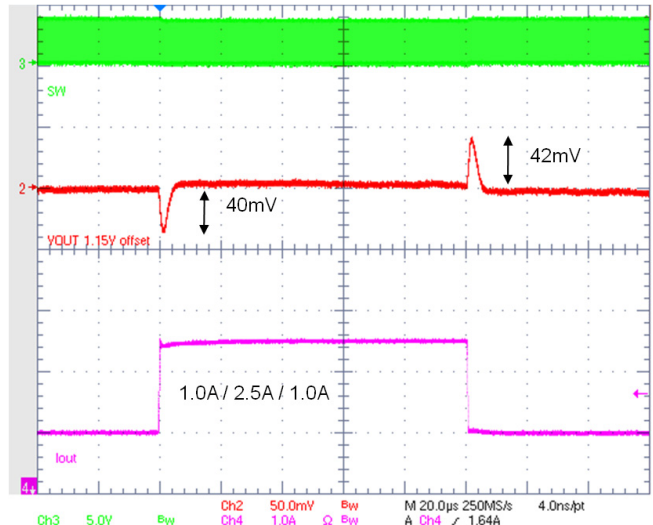


Figure 31. Transient Load 1.0 – 2.5 A Forced PWM Mode



Figure 32. Transient Load 2.0 – 3.5 A Auto Mode



Figure 33. Transient Load 2.0 – 3.5 A Forced PWM Mode

DETAILED OPERATING DESCRIPTION

Detailed Descriptions

The NCP6335 is voltage mode standalone synchronous DC-to-DC converter optimized to supply different sub systems of portable applications powered by one cell Li-Ion or three cells Alkaline/NiCd/NiMH. The IC can deliver up to 4 A at an I²C selectable voltage ranging from 0.6 V to 1.40 V. It can share the same output rail with another DC-to-DC converter and works as a transient load helper without sinking current on shared rail. A 3 MHz switching frequency allows the use of smaller output filter components. Synchronous rectification and automatic PWM/PFM transitions improve overall solution efficiency. Forced PWM is also configurable. Operating modes, configuration, and output power can be easily selected either by using digital I/O pins or by programming a set of registers using an I²C compatible interface capable of operation up to 3.4 MHz. Default I²C settings are factory programmable.

DC to DC Buck Operation

The converter is a synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for NCP6335 operation. Feedback and compensation network are also fully integrated. The converter can operate in two different modes: PWM and PFM. The transition between PWM/PFM modes can occur automatically or the switcher can be placed in forced PWM mode by I²C programming (PWMVSEL0 / PWMVSEL1 bits of COMMAND register).

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, NCP6335 operates in PWM mode from a fixed clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N-MOSFET switch operates as synchronous rectifier and is driven complementary to the P-MOSFET switch. In CCM, the lower switch (N-MOSFET) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the NCP6335 operates in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N-MOSFET operates as synchronous rectifier after each P-MOSFET on-pulse. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM mode.

Forced PWM

The NCP6335 can be programmed to only use PWM and disable the transition to PFM if so desired.

Output Stage

NCP6335 is a 2.5 A to 4 A output current capable integrated DC to DC converter. To supply such a high current, the internal MOSFETs need to be large. The output stage is composed of nine modules that can be individually Enabled / Disabled by setting the MODULE register.

Inductor Peak Current Limitation

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrain inductor power. The user can select peak current to keep inductor within its specifications. The peak current can be set by writing IPEAK[1..0] bits in LIMCONF register.

Table 1. IPEAK VALUES

| IPEAK[1..0] | Inductor Peak Current (A) |
|-------------|------------------------------|
| 00 | 3.4 – for 2.5 output current |
| 01 | 4.0 – for 3.0 output current |
| 10 | 4.4 – for 3.5 output current |
| 11 | 5.0 – for 4.0 output current |

Output Voltage

Output voltage is set internally by integrated resistor bridge and error amplifier that drives the PWM/PFM controller. No extra component is needed to set output voltage. However, writing in the VoutVSEL0[6..0] bits of the PROGSEL0 register or VoutVSEL1[6..0] bits of the PROGSEL1 register will change settings. Output voltage level can be programmed in the 0.6 V to 1.4 V range by 6.25 mV steps.

The VSEL pin and VSELGT bit will determine which register between PROGSEL0 and PROGSEL1 will set the output voltage.

- If VSELGT = 1 AND VSEL=0 → Output voltage is set by VoutVSEL0[6..0] bits (PROGSEL0 register)
- Else → Output voltage is set by VoutVSEL1[6..0] bits (PROGSEL1 register)

Under Voltage Lock Out (UVLO)

NCP6335 core does not operate for voltages below the Under Voltage lock Out (UVLO) level. Below UVLO threshold, all internal circuitry (both analog and digital) is held in reset.

NCP6335 operation is guaranteed down to VUVLO when battery voltage is dropping off. To avoid erratic on / off behavior, a maximum 200 mV hysteresis is implemented.

Restart is guaranteed at 2.5 V when VBAT voltage is recovering or rising.

Thermal Management

Thermal Shutdown (TSD)

The thermal capability of IC can be exceeded due to step down converter output stage power level. A thermal protection circuitry is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, output voltage is turned off.

When NCP6335 returns from thermal shutdown, it can re-start in two different configurations depending on REARM bit in the LIMCONF register (see register description section):

- If REARM = 0 then NCP6335 does not re-start after TSD. To restart, an EN pin toggle is required.
- If REARM = 1, NCP6335 re-starts with register values set prior to thermal shutdown.

A Thermal shut down interrupt is raised upon this event.

Thermal shut down threshold is set at 150°C (typical) when the die temperature increases and, in order to avoid erratic on / off behavior, a 30°C hysteresis is implemented. After a typical 150°C thermal shut down, NCP6335 will return to normal operation when the die temperature cools below 120°C.

Thermal Warnings

In addition to the TSD, the die temperature monitoring will flag potential die over temperature. A thermal warning and thermal pre-warning are implemented which can inform the processor through two different interrupts (if not masked) that NCP6335 is close to its thermal shutdown so that preventive measures to cool down die temperature can be taken by software.

The Warning threshold is set by hardware to 135°C typical when the die temperature increases. The Pre-Warning threshold is set by default to 105°C, but can be changed by user by setting the TPWTH[1..0] bits in the LIMCONF register.

Active Output Discharge

To make sure that no residual voltage remains in the power supply rail, an active discharge path can ground the NCP6335 output voltage.

For maximum flexibility, this feature can be easily disabled or enabled with DISCHG bit in PGOOD register. By default the discharge path is disabled.

However the discharged path is activated during the first 100 μs after battery insertion.

Enabling

The EN pin controls NCP6335 start up. EN pin Low to High transition starts the power up sequencer. If EN is made low, the DC to DC converter is turned off and device enters:

- In Sleep Mode if Sleep_Mode I²C bit is high or VSEL is high,
- In Off Mode if Sleep_Mode I²C bit and VSEL are low.

When EN pin is set to a high level, the DC to DC converter can be enabled / disabled by writing the ENVSEL0 or ENVSEL1 bit of the PROGVSEL0 and PROGVSEL1 registers: If ENx I²C bit is high, DCDC is activated, If ENx I²C is low the DC to DC converter is turned off and device enters in Sleep Mode

A built in pull down resistor disables the device when this pin is left unconnected or not driven.

Power Up Sequence (PUS)

In order to power up the circuit, the input voltage AVIN has to rise above the VUVLO threshold. This triggers the internal core circuitry power up which is the “Wake Up Time” (including “Bias Time”).

This delay is internal and cannot be bypassed. EN pin transition within this delay corresponds to the “Initial power up sequence” (IPUS):

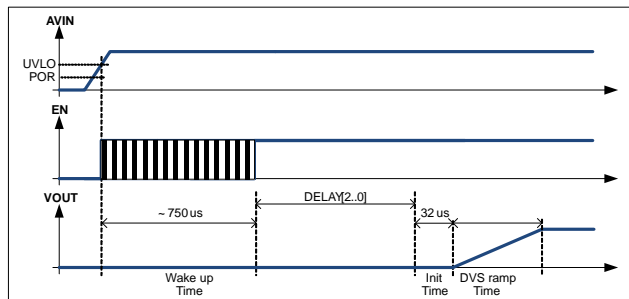


Figure 34. Initial Power Up Sequence

In addition a user programmable delay will also take place between end of Core circuitry turn on (Wake Up Time and Bias Time) and Init time: The DELAY[2..0] bits of TIME register will set this user programmable delay with a 2 ms resolution. With default delay of 0 ms, the NCP6335 IPUS takes roughly 900 μs, means DCDC output voltage will be ready within 1 ms.

The power up output voltage is defined by VSEL state.

NOTE: During the Wake Up time, the I²C interface is not active. Any I²C request to the IC during this time period will result in a NACK reply.

Normal, Quick and Fast Power Up Sequence

The previous description applies only when the EN transitions during the internal core circuitry power up (Wake up and calibration time). Otherwise three different cases are possible:

- Enabling the part by setting EN pin from Off Mode will result in “Normal power up sequence” (NPUS, with DELAY;[2..0]).

- Enabling the part by setting EN pin from Sleep Mode will result in “Quick power up sequence” (QPUS, with DELAY[2..0]). Sleep mode is when VSEL is high and EN low, or when Sleep_Mode I²C bit is set and EN is low, or finally when DCDC is off and EN high.
- Enabling the part either by setting ENVSEL0 or ENVSEL1 bits of the PROGVSEL0 and PROGVSEL1 registers or by VSEL pin transition will (whereas EN is already high) results in “Fast power up sequence” (FPUS, without DELAY[2..0]).

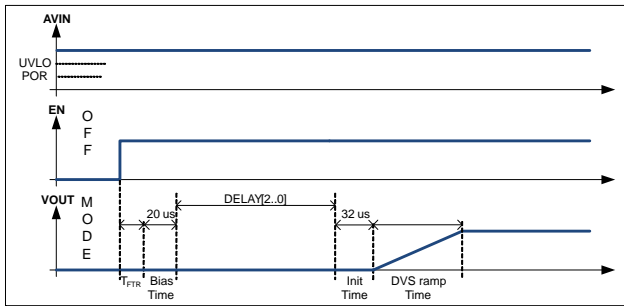


Figure 35. Normal Power Up Sequence

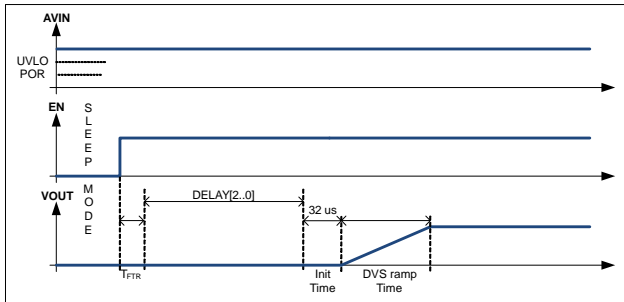


Figure 36. Quick Power Up Sequence

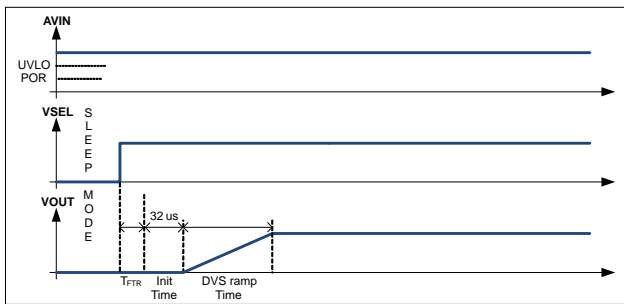


Figure 37. Fast Power Up Sequence

In addition the delay set in DELAY[2..0] bits in TIME register will apply only for the EN pins turn ON sequence (NPUS and QPUS).

The power up output voltage is defined by VSEL state.

Note that the sleep mode needs about 150 μs to be established.

DC to DC Converter Shut Down

When shutting down the device, no shut down sequence is required. Output voltage is disabled and, depending on the DISCHG bit state of PGOOD register, output may be discharged.

DCDC Shutdown is initiated by either grounding the EN pin (Hardware Shutdown) or, depending on the VSEL internal signal level, by clearing the ENVSEL0 or ENVSEL1 bits (Software shutdown) in PROGVSEL0 or PROGVSEL1 registers.

In hardware shutdown (EN = 0), the internal core is still active and I²C accessible.

NCP6335 shuts internal core down when AVIN falls below UVLO.

Dynamic Voltage Scaling (DVS)

This converter supports dynamic voltage scaling (DVS) allowing the output voltage to be reprogrammed via I²C commands and provides the different voltages required by the processor. The change between set points is managed in a smooth fashion without disturbing the operation of the processor.

When programming a higher voltage, output raises in equidistant steps, which are 6.25 mV/0.166 μs, such that the dV/dt is controlled. When programming a lower voltage, output will decrease in equidistant steps per defined time period such that the dV/dt is controlled (default 6.25 mV/2.666 μs) by writing DVS[1..0] bits in TIME register

DVS sequence is automatically initiated by changing output voltage settings. There are two ways to change these settings:

- Directly change the active setting register value (VoutVSEL0[6..0] of PROGVSEL0 register or VoutVSEL1[6..0] of the PROGVSEL1 register) via I²C command
- Change the VSEL internal signal level by toggling VSEL pin.

The second method eliminates the I²C latency and is therefore faster.

The DVS transition mode can be changed with the DVSMODE bit in COMMAND register:

- In forced PWM mode when accurate output voltage control is needed.

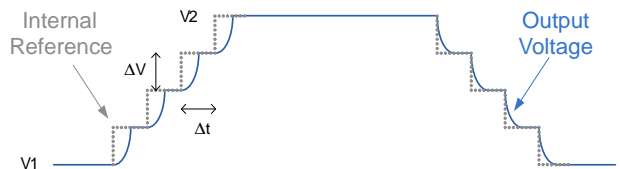


Figure 38. DVS in Forced PWM Mode Diagram

- In Auto mode when output voltage has not to be discharged. Note that approximately 30 μ s is needed to transition from PFM mode to PWM mode.

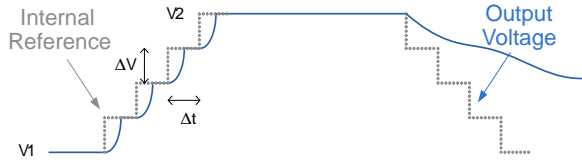


Figure 39. DVS in Auto Mode Diagram

Digital IO Settings

VSEL Pin

By changing VSEL pin levels, the user has a latency free way to change NCP6335 configuration: operating mode (Auto or PWM forced), the output voltage as well as enable.

Table 2. VSEL PIN PARAMETERS

| Parameter VSEL Pin Can Set | REGISTER VSEL = LOW | REGISTER VSEL = HIGH |
|------------------------------------|-------------------------|-------------------------|
| ENABLE | ENVSEL0 PROGVSEL0[7] | ENVSEL1 PROGVSEL1[7] |
| VOUT | VoutVSEL0[6..0] | VoutVSEL1[6..0] |
| OPERATING MODE (Auto / PWM Forced) | PWMVSEL0 COMMAND[7] | PWMVSEL1 COMMAND[6] |

VSEL pin action can be masked by writing 0 to the VSELGT bit in the COMMAND register. In that case I²C bit corresponding to VSEL high will be taken into account.

EN Pin

The EN pin can be gated by writing the ENVSEL0 or ENVSEL1 bits of the PROGVSEL0 and PROGVSEL1 registers, depending on which register is activated by the VSEL internal signal.

Power Good Pin (Optional)

To indicate the output voltage level is established, a power good signal is available.

The power good signal is low when the DC to DC converter is off. Once the output voltage reaches 95% of the expected output level, the power good logic signal becomes high and the open drain output becomes high impedance.

During operation when the output drops below 90% of the programmed level the power good logic signal goes low (and the open drain signal transitions to a low impedance state) which indicates a power failure. When the voltage rises again to above 95% the power good signal goes high again.

During a positive DVS sequence, when target voltage is higher than initial voltage, the Power Good logic signal will be set low during output voltage ramping and transition to high once the output voltage reaches 95% of the target voltage. When the target voltage is lower than the initial

voltage, Power Good pin will remain at high level during transition.

Power Good signal during normal operation can be disabled by clearing the PGDCDC bit in PGOOD register.

Power Good operation during DVS can be controlled by setting / clearing the bit PGDVS in PGOOD register

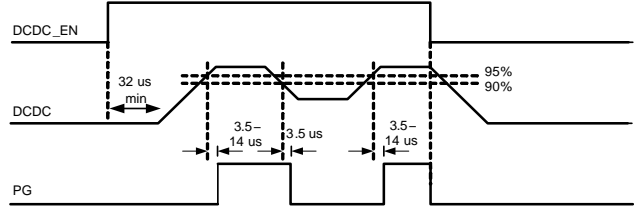


Figure 40. Power Good signal

Power Good Delay

In order to generate a Reset signal, a delay can be programmed between the output voltage gets 95% of its final value and Power Good pin is released to high level.

The delay is set from 0 ms to 64 ms through the TOR[1..0] bits in the TIME register. The default delay is 0 ms.

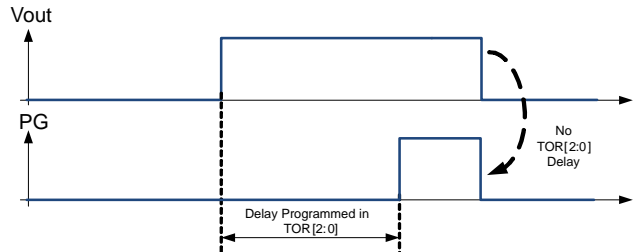


Figure 41. Power Good Operation

Interrupt Pin (Optional)

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring).

Table 3. INTERRUPT SOURCES

| Interrupt Name | Description |
|----------------|---------------------------------|
| TSD | Thermal Shut Down |
| TWARN | Thermal Warning |
| TPREW | Thermal Pre Warning |
| UVLO | Under Voltage Lock Out |
| IDCDC | DCDC current Over / below limit |
| PG | Power Good |

Individual bits generating interrupts will be set to 1 in the INT_ACK register (I²C read only registers), indicating the interrupt source. INT_ACK register is automatically reset by an I²C read. The INT_SEN register (read only register) contains real time indicators of interrupt sources.

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All interrupt sources can be masked by writing in register INT_MSK. Masked sources will never generate an interrupt request on INTB pin.

The INTB pin is an open drain output. A non masked interrupt request will result in INTB pin being driven low.

When the host reads the INT_ACK registers the INTB pin is released to high impedance and the interrupt register INT_ACK is cleared.

Figure 42 is UVLO event example: INTB pin with INT_SEN/INT_MSK/INT_ACK and an I²C read access behavior.

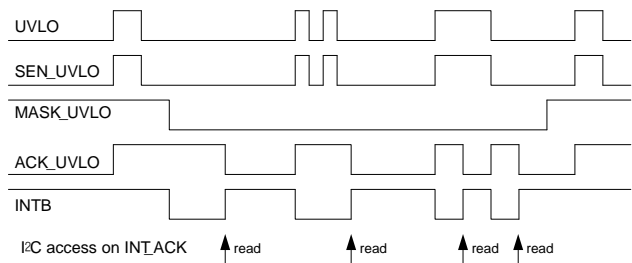


Figure 42. Interrupt Operation Example

INT_MSK register is set to disable INTB feature by default.

Configurations

Default output voltages, enables, DCDC modes, current limit and other parameters can be factory programmed upon request. Two different configurations are pre-defined:

| Configuration | 3.5 A NCP6335F | 2.5 A (Stand-Alone) NCP6335D |
|----------------------------------|-------------------|---------------------------------|
| Default I ² C address | 0x1C | 0x1C |
| PID product identification | 10h | 10h |
| RID revision identification | xxh | xxh |
| FID feature identification | 00h | 01h |
| Default VOUT – VSEL=1 | 1.150 V | 1.100 V |
| Default VOUT – VSEL=0 | 1.025 V | 1.100 V |
| Default MODE – VSEL=1 | Forced PWM | Auto mode |
| Default MODE – VSEL=0 | Auto mode | Auto mode |
| Default IPEAK | 5.0 A | 4.0 A |
| OPN | NCP6335FFCT1G | NCP6335DFCT1G |
| Marking | 6335F | 6335D |

I²C Compatible Interface

NCP6335 can support a subset of I²C protocol Detailed below.

I²C Communication Description

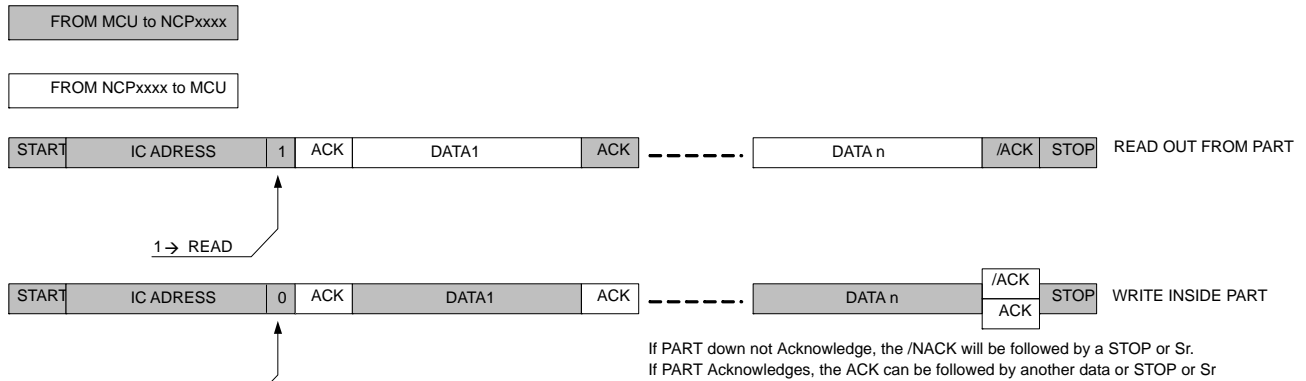


Figure 43. General Protocol Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- In case of a Write operation, the register address (@REG) pointing to the register we want to write in followed by the data we will write in that location. The writing process is auto-incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1, etc.
- In case of read operation, the NCP6335 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto-incremental.

Read Out From Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has pointed to:

In the Drawings Below Change STETS to SETS

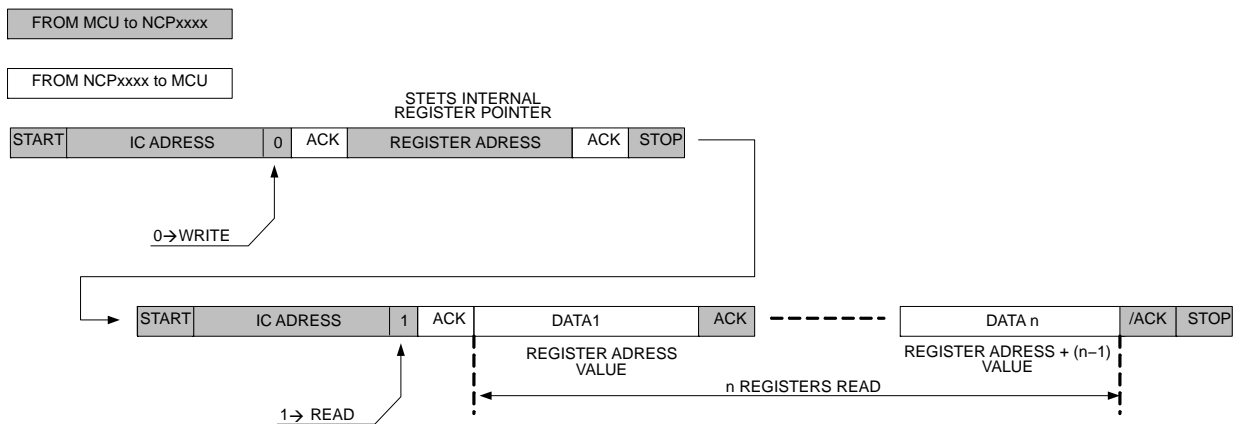


Figure 44. Read Out from Part

The first WRITE sequence will set the internal pointer to the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

With Stop Then Start

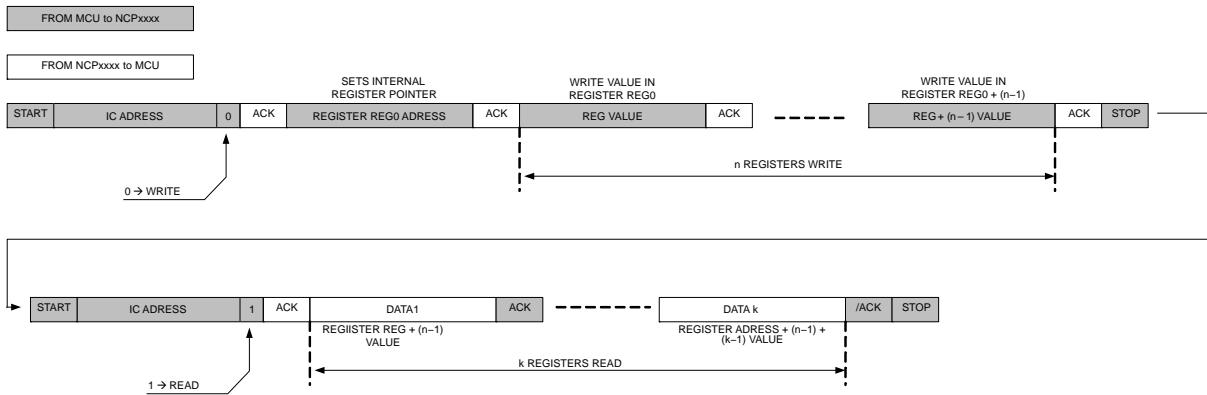


Figure 45. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg + n.

Write n Registers:

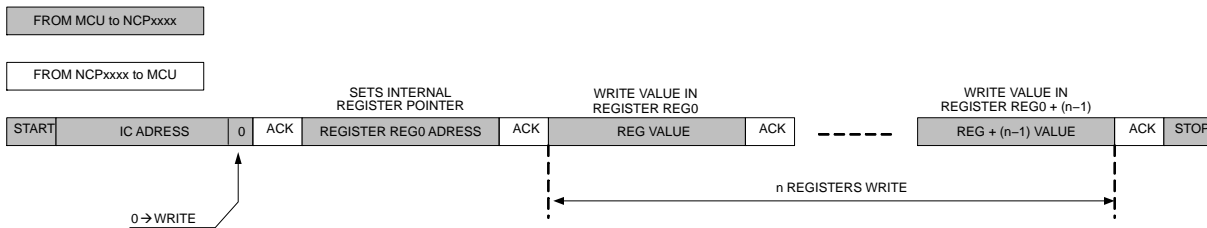


Figure 46. Write in n Registers

I²C Address

NCP6335 has four available I²C address selectable by factory settings (ADD0 to ADD3). Different address settings can be generated upon request to ON Semiconductor. The default address is set to 38h / 39h since the NCP6335 supports 7-bit address only and ignores A0.

Table 4. I²C ADDRESS

| I ² C Address | Hex | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|--------------------------|------------------|------|----|----|----|----|----|----|-----|
| ADD0 | W 0x20 R 0x21 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | R/W |
| | Add | 0x10 | | | | | | | - |
| ADD1 | W 0x28 R 0x29 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | R/W |
| | Add | 0x14 | | | | | | | - |
| ADD2 | W 0x30 R 0x31 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R/W |
| | Add | 0x18 | | | | | | | - |
| ADD3 (default) | W 0x38 R 0x39 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | R/W |
| | Add | 0x1C | | | | | | | - |

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Register Map

Table 5 describes I²C registers.

Registers can be:

| | |
|----------|---|
| R | Read only register |
| RC | Read then Clear |
| RW | Read and Write register |
| Reserved | Address is reserved and register is not physically designed |
| Spare | Address is reserved and register is physically designed |

Table 5. I²C REGISTER MAP 2.5 A (STAND-ALONE) CONFIGURATION (NCP6335D)

| Add. | Register Name | Type | Def. | Function |
|------------|---------------|------|-------|---|
| 00h | INT_ACK | RC | 00h | Interrupt register |
| 01h | INT_SEN | R | 00h | Sense register (real time status) |
| 02h | INT_MSK | RW | FFh | Mask register to enable or disable interrupt sources (trim) |
| 03h | PID | R | 10h | Product Identification |
| 04h | RID | R | Metal | Revision Identification |
| 05h | FID | R | 01h | Features Identification (trim) |
| 06h to 0Fh | - | - | - | Reserved for future use |
| 10h | PROGVSEL1 | RW | D0h | Output voltage settings and EN for VSEL pin = High (trim) |
| 11h | PROGVSEL0 | RW | D0h | Output voltage settings and EN for VSEL pin = Low (trim) |
| 12h | PGOOD | RW | 00h | Power good and active discharge settings (trim) |
| 13h | TIME | RW | 19h | Enabling and DVS timings (trim) |
| 14h | COMMAND | RW | 01h | Enabling and Operating mode Command register (trim) |
| 15h | MODULE | RW | 80h | Active module count settings (trim) |
| 16h | LIMCONF | RW | 63h | Reset and limit configuration register (trim) |
| 17h to 1Fh | - | - | - | Reserved for future use |
| 20h to FFh | - | - | - | Reserved. Test Registers |

Table 6. I²C REGISTER MAP 3.5 A CONFIGURATION (NCP6335F)

| Add. | Register Name | Type | Def. | Function |
|------------|---------------|------|-------|---|
| 00h | INT_ACK | RC | 00h | Interrupt register |
| 01h | INT_SEN | R | 00h | Sense register (real time status) |
| 02h | INT_MSK | RW | FFh | Mask register to enable or disable interrupt sources (trim) |
| 03h | PID | R | 10h | Product Identification |
| 04h | RID | R | Metal | Revision Identification |
| 05h | FID | R | 00h | Features Identification (trim) |
| 06h to 0Fh | - | - | - | Reserved for future use |
| 10h | PROGVSEL1 | RW | D8h | Output voltage settings and EN for VSEL pin = High (trim) |
| 11h | PROGVSEL0 | RW | C4h | Output voltage settings and EN for VSEL pin = Low (trim) |
| 12h | PGOOD | RW | 00h | Power good and active discharge settings (trim) |
| 13h | TIME | RW | 19h | Enabling and DVS timings (trim) |
| 14h | COMMAND | RW | 41h | Enabling and Operating mode Command register (trim) |
| 15h | MODULE | RW | 80h | Active module count settings (trim) |
| 16h | LIMCONF | RW | E3h | Reset and limit configuration register (trim) |
| 17h to 1Fh | - | - | - | Reserved for future use |
| 20h to FFh | - | - | - | Reserved. Test Registers |

Registers Description

Table 7. INTERRUPT ACKNOWLEDGE REGISTER

| | | | | | | | |
|------------------------------------|-----------|--|-----------|--------------------------------|-----------|-----------|-----------|
| Name: INTACK | | | | Address: 0000000b (00h) | | | |
| Type: RC | | | | Default: 00h | | | |
| Trigger: Dual Edge [D7..D0] | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ACK_TSD | ACK_TWARN | ACK_TPREW | Spare = 0 | Spare= 0 | ACK_UVLO | ACK_IDCDC | ACK_PG |
| Bit | | Bit Description | | | | | |
| ACK_PG | | Power Good Sense Acknowledgement 0: Cleared 1: DCDC Power Good Event detected | | | | | |
| ACK_IDCDC | | DCDC Over Current Sense Acknowledgement 0: Cleared 1: DCDC Over Current Event detected | | | | | |
| ACK_UVLO | | Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected | | | | | |
| ACK_TPREW | | Thermal Pre Warning Sense Acknowledgement 0: Cleared 1: Thermal Pre Warning Event detected | | | | | |
| ACK_TWARN | | Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected | | | | | |
| ACK_TSD | | Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected | | | | | |

Table 8. INTERRUPT SENSE REGISTER

| | | | | | | | |
|---------------------|-----------|--|-----------|--------------------------------|-----------|-----------|-----------|
| Name: INTSEN | | | | Address: 01h | | | |
| Type: R | | | | Default: 0000000b (00h) | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SEN_TSD | SEN_TWARN | SEN_TPREW | Spare = 0 | Spare = 0 | SEN_UVLO | SEN_IDCDC | SEN_PG |
| Bit | | Bit Description | | | | | |
| SEN_PG | | Power Good Sense 0: DCDC Output Voltage below target 1: DCDC Output Voltage within nominal range | | | | | |
| SEN_IDCDC | | DCDC over current sense 0: DCDC output current is below limit 1: DCDC output current is over limit | | | | | |
| SEN_UVLO | | Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold | | | | | |
| SEN_TPREW | | Thermal Pre Warning Sense 0: Junction temperature below thermal pre-warning limit 1: Junction temperature over thermal pre-warning limit | | | | | |
| SEN_TWARN | | Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit | | | | | |
| SEN_TSD | | Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit | | | | | |

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Table 9. INTERRUPT MASK REGISTER

| | | | | | | | |
|----------------------|------------|--|-----------|---------------------------------|-----------|------------|-----------|
| Name: INTMASK | | | | Address: 02h | | | |
| Type: RW | | | | Default: 11111111b (FFh) | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MASK_TSD | MASK_TWARN | MASK_TPREW | Spare = 1 | Spare = 1 | MASK_UVLO | MASK_IDCDC | MASK_PG |
| Bit | | Bit Description | | | | | |
| MASK_PG | | Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |
| MASK_IDCDC | | DCDC over current interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |
| MASK_UVLO | | Under Voltage interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |
| MASK_TPREW | | Thermal Pre Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |
| MASK_TWARN | | Thermal Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |
| MASK_TSD | | Thermal Shutdown interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked | | | | | |

Table 10. PRODUCT ID REGISTER

| | | | | | | | |
|---------------------|-----------|-----------|-----------|---------------------------------|-----------|-----------|-----------|
| Name: PID | | | | Address: 03h | | | |
| Type: R | | | | Default: 00010000b (10h) | | | |
| Trigger: N/A | | | | Reset on N/A | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PID_7 | PID_6 | PID_5 | PID_4 | PID_3 | PID_2 | PID_1 | PID_0 |

Table 11. REVISION ID REGISTER

| | | | | | | | |
|---------------------|-----------|---|-----------|-----------------------|-----------|-----------|-----------|
| Name: RID | | | | Address: 04h | | | |
| Type: R | | | | Default: Metal | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RID_7 | RID_6 | RID_5 | RID_4 | RID_3 | RID_2 | RID_1 | RID_0 |
| Bit | | Bit Description | | | | | |
| RID[7..0] | | Revision Identification 00000000: First silicon 00000001: Version Optimized 00010000: Production | | | | | |

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Table 12. FIRMWARE ID REGISTER

| | | | | | | | |
|---------------------|-----------|--|-----------|----------------------------------|-----------|-----------|-----------|
| Name: FID | | | | Address: 05h | | | |
| Type: R | | | | Default: See Register map | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FID_7 | FID_6 | FID_5 | FID_4 | FID_3 | FID_2 | FID_1 | FID_0 |
| Bit | | Bit Description | | | | | |
| FID[7..0] | | Feature Identification 00000000: NCP6335F: 3.5 A configuration 00000001: NCP6335D: 2.5 A configuration | | | | | |

Table 13. DC TO DC VOLTAGE PROG (VSEL = 1) REGISTER

| | | | | | | | |
|------------------------|-----------|---|-----------|----------------------------------|-----------|-----------|-----------|
| Name: PROGVSEL1 | | | | Address: 10h | | | |
| Type: RW | | | | Default: See Register map | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ENVSEL1 | | VoutVSEL1[6..0] | | | | | |
| Bit | | Bit Description | | | | | |
| VoutVSEL1[6..0] | | Sets the DC to DC converter output voltage when VSEL pin = 1 (and VSEL pin function is enabled in register COMMAND.D0) or when VSEL pin function is disabled in register COMMAND.D0 0000000b = 600 mV – 1111111b = 1393.75 mV (steps of 6.25 mV) | | | | | |
| ENVSEL1 | | EN Pin Gating for VSEL internal signal = High 0: Disabled 1: Enabled | | | | | |

Table 14. DC TO DC VOLTAGE PROG (VSEL = 0) REGISTER

| | | | | | | | |
|------------------------|-----------|--|-----------|----------------------------------|-----------|-----------|-----------|
| Name: PROGVSEL0 | | | | Address: 11h | | | |
| Type: RW | | | | Default: See Register map | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ENVSEL0 | | VoutVSEL0[6..0] | | | | | |
| Bit | | Bit Description | | | | | |
| VoutVSEL0[6..0] | | Sets the DC to DC converter output voltage when VSEL pin = 0 (and VSEL pin function is enabled in register COMMAND.D0) 0000000b = 600 mV – 1111111b = 1393.75 mV (steps of 6.25 mV) | | | | | |
| ENVSEL0 | | EN Pin Gating for VSEL internal signal = Low 0: Disabled 1: Enabled | | | | | |

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Table 15. POWER GOOD REGISTER

| | | | | | | | |
|---------------------|--|-----------|-----------|---------------------------------|-----------|-----------|-----------|
| Name: PGOOD | | | | Address: 12h | | | |
| Type: RW | | | | Default: 00000000b (00h) | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Spare = 0 | Spare = 0 | Spare = 0 | DISCHG | TOR[1..0] | | PGDVS | PGDCDC |
| Bit | Bit Description | | | | | | |
| PGDCDC | Power Good Enabling 0 = Disabled 1 = Enabled | | | | | | |
| PGDVS | Power Good Active On DVS 0 = Disabled 1 = Enabled | | | | | | |
| TOR[1..0] | Time out Reset settings for Power Good 00 = 0 ms 01 = 8 ms 10 = 32 ms 11 = 64 ms | | | | | | |
| DISCHG | Active discharge bit Enabling 0 = Discharge path disabled 1 = Discharge path enabled | | | | | | |

Table 16. TIMING REGISTER

| | | | | | | | |
|---------------------|--|-----------|---------------|---------------------------------|-----------|----------------|-----------|
| Name: TIME | | | | Address: 13h | | | |
| Type: RW | | | | Default: 00011001b (19h) | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DELAY[2..0] | | | DVSdown[1..0] | | Spare = 0 | DBN_Time[1..0] | |
| Bit | Bit Description | | | | | | |
| DBN_Time[1..0] | EN and VSEL debounce time 00 = No debounce 01 = 1–2 us 10 = 2–3 us 11 = 3–4 us | | | | | | |
| DVSdown[1..0] | DVS Speed for down DVS 00 = 6.25 mV step / 0.333 us 01 = 6.25 mV step / 0.666 us 10 = 6.25 mV step / 1.333 us 11 = 6.25 mV step / 2.666 us | | | | | | |
| DELAY[2..0] | Delay applied upon enabling (ms) 000b = 0 ms – 111b = 14 ms (Steps of 2 ms) | | | | | | |

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Table 17. COMMAND REGISTER

| | | | | | | | |
|----------------------|-----------|--|------------|----------------------------------|-----------|-----------|-----------|
| Name: COMMAND | | | | Address: 14h | | | |
| Type: RW | | | | Default: See Register map | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PWMVSEL0 | PWMVSEL1 | DVSMODE | Sleep_Mode | Spare = 0 | Spare = 0 | Spare = 0 | VSELGT |
| Bit | | Bit Description | | | | | |
| VSELGT | | VSEL Pin Gating 0 = Disabled 1 = Enabled | | | | | |
| Sleep_Mode | | Sleep mode 0 = Low Iq mode when EN and VSEL low 1 = Force product in sleep mode (when EN and VSEL are low) | | | | | |
| DVSMODE | | DVS transition mode selection 0 = Auto 1 = Forced PWM | | | | | |
| PWMVSEL1 | | Operating mode for VSEL internal signal = High 0 = Auto 1 = Forced PWM | | | | | |
| PWMVSEL0 | | Operating mode for VSEL internal signal = Low 0 = Auto 1 = Forced PWM | | | | | |

Table 18. OUTPUT STAGE MODULE SETTINGS REGISTER

| | | | | | | | |
|---------------------|-----------|---|-----------|---------------------------------|-----------|-----------|-----------|
| Name: MODULE | | | | Address: 15h | | | |
| Type: RW | | | | Default: 10000000b (80h) | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MODUL[3..0] | | | | Spare = 0 | Spare = 0 | Spare = 0 | Spare = 0 |
| Bit | | Bit Description | | | | | |
| MODUL [3..0] | | Number of modules 0000 = 1 Module – 1000 ~ 1111 = 9 Modules (Steps of 1) | | | | | |

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Table 19. LIMITS CONFIGURATION REGISTER

| | | | | | | | |
|----------------------|-----------|---|-----------|----------------------------------|-----------|-----------|-----------|
| Name: LIMCONF | | | | Address: 16h | | | |
| Type: RW | | | | Default: See Register map | | | |
| Trigger: N/A | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| IPEAK[1..0] | | TPWTH[1..0] | | Spare = 0 | FORCERST | RSTSTATUS | REARM |
| Bit | | Bit Description | | | | | |
| REARM | | Rearming of device after TSD 0: No re-arming after TSD 1: Re-arming active after TSD with no reset of I ² C registers: new power-up sequence is initiated with previously programmed I ² C registers values | | | | | |
| RSTSTATUS | | Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset) | | | | | |
| FORCERST | | Force Reset Bit 0 = Default value. Self cleared to 0 1: Force reset of internal registers to default | | | | | |
| TPWTH[1..0] | | Thermal pre-Warning threshold settings 00 = 83°C 01 = 94°C 10 = 105°C 11 = 116°C | | | | | |
| IPEAK | | Inductor peak current settings 00 = 3.4 A 01 = 4.0 A 10 = 4.4 A 11 = 5.0 A | | | | | |

NCP6335

APPLICATION INFORMATION

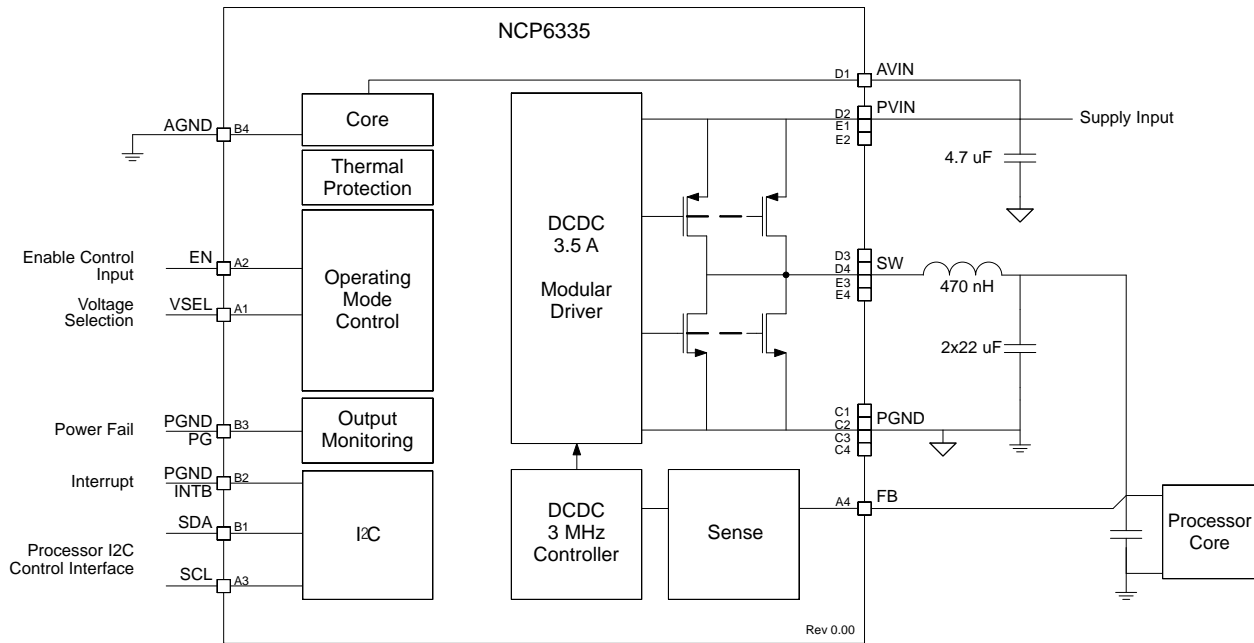


Figure 47. Typical Application Schematic

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \quad (\text{eq. 1})$$

The NCP6335 internal compensation network is optimized for a typical output filter comprising a 470 nH inductor and 2 x 22 uF capacitor as describes in the basic application schematic is described by Figure 47.

Voltage Sensing Considerations

In order to regulate power supply rail, NCP6335 should sense its output voltage. Thanks to the FB pin, the IC can support two sensing methods:

- Normal case: the voltage sensing is achieved close to the output capacitor. In that case, FB is connected to the output capacitor positive terminal (voltage to regulate).
- Remote sensing: In remote sensing, the power supply rail sense is made close to the system powered by the NCP6335. The voltage to system is more accurate, since PCB line impedance voltage drop is within the regulation loop. In that case, we recommend connecting

the FB pin to the system decoupling capacitor positive terminal.

Components Selection

Inductor Selection

The inductance of the inductor is determined by given peak-to-peak ripple current I_{L_PP} of approximately 20% to 50% of the maximum output current I_{OUT_MAX} for a trade-off between transient response and output ripple. The inductance corresponding to the given current ripple is:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L_PP}} \quad (\text{eq. 2})$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L_MAX} = I_{OUT_MAX} + \frac{I_{L_PP}}{2} \quad (\text{eq. 3})$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 20 shows recommended.

Table 20. INDUCTOR SELECTION

| Supplier | Part# | Value (μH) | Size (mm) (L x l x T) | DC Rated Current (A) | DCR Max at 25°C (mΩ) |
|----------|----------------------|------------|-----------------------|----------------------|----------------------|
| Cyntec | PIFE20161B-R33-MS-39 | 0.33 | 2.0 x 1.6 x 1.2 | 4.6 | 33 |
| Cyntec | PIFE20161B-R47-MS-39 | 0.47 | 2.0 x 1.6 x 1.2 | 3.9 | 36 |
| Cyntec | PIFE25201T-R47-MS-39 | 0.47 | 2.5 x 2.0 x 1.0 | 4.5 | 41 |
| TOKO | DFE201610R-H-R47N | 0.47 | 2.0 x 1.6 x 1.0 | 3.3 | 48 |
| TOKO | DFE201612R-H-R47N | 0.47 | 2.0 x 1.6 x 1.2 | 3.8 | 40 |
| TDK | TFM252010A-R47M | 0.47 | 2.5 x 2.0 x 1.0 | 4.5 | 30 |
| TDK | SPM6530T-R47M170 | 0.47 | 7.1 x 6.5 x 3.0 | 20 | 4 |

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be used. For a given peak-to-peak ripple current I_{L_PP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as below.

$$V_{OUT_PP} \approx V_{OUT_PP(C)} + V_{OUT_PP(ESR)} + V_{OUT_PP(ESL)} \quad (eq. 4)$$

Where $V_{OUT_PP(C)}$ is a ripple component from an equivalent total capacitance of the output capacitors, $V_{OUT_PP(ESR)}$ is a ripple component from an equivalent ESR of the output capacitors, and $V_{OUT_PP(ESL)}$ is a ripple component from an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT_PP(C)} = \frac{I_{L_PP}}{8 \cdot C \cdot f_{SW}} \quad (eq. 5)$$

and

$$V_{OUT_PP(ESR)} = I_{L_PP} \cdot ESR \quad (eq. 6)$$

$$V_{OUT_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad (eq. 7)$$

and the peak-to-peak ripple current is

$$I_{L_PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L} \quad (eq. 8)$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT_PP(C)}$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUT_PP} in PWM operation mode.

$$C_{MIN} = \frac{I_{L_PP}}{8 \cdot V_{OUT_PP} \cdot f_{SW}} \quad (eq. 9)$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage

ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding to the input ripple voltage V_{IN_PP} is

$$C_{IN_MIN} = \frac{I_{OUT_MAX} \cdot (D - D^2)}{V_{IN_PP} \cdot f_{SW}} \quad (eq. 10)$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \quad (eq. 11)$$

In addition, the input capacitor needs to be able to absorb the input current, which has a RMS value of

$$I_{IN_RMS} = I_{OUT_MAX} \cdot \sqrt{D - D^2} \quad (eq. 12)$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC. All PGNDs are connected together to the ground terminal of the input cap which then connects to the ground plane. All PVIN are connected together to the Vbat terminal of the input cap which then connects to the Vbat plane.

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper, but compact because it is also a noise source.
- It would be good to have separated ground planes for PGND and AGND and connect the two planes at one point. Try best to avoid overlap of input ground loop

and output ground loop to prevent noise impact on output regulation.

- Arrange a “quiet” path for output voltage sense, and make it surrounded by a ground plane.

Thermal Layout Considerations

Good PCB layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Use two layers for the high current paths (PVIN, PGND, SW) in order to split current in two different paths and limit PCB copper self heating.

(See demo board example Figure 49)

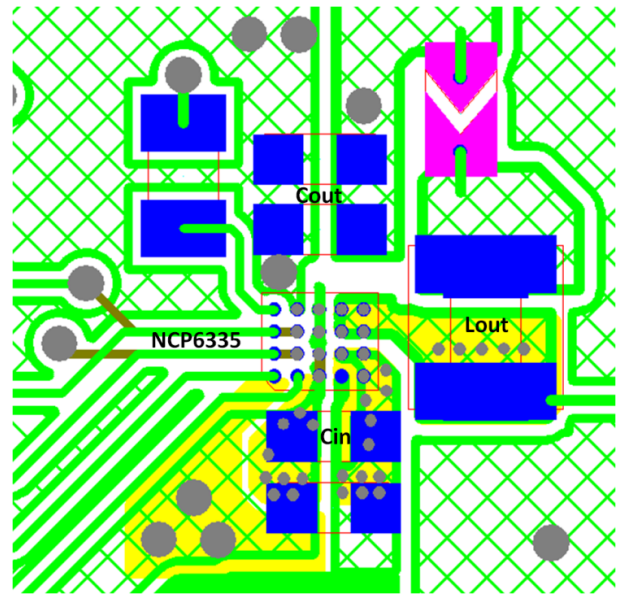


Figure 49. Demo Board Example

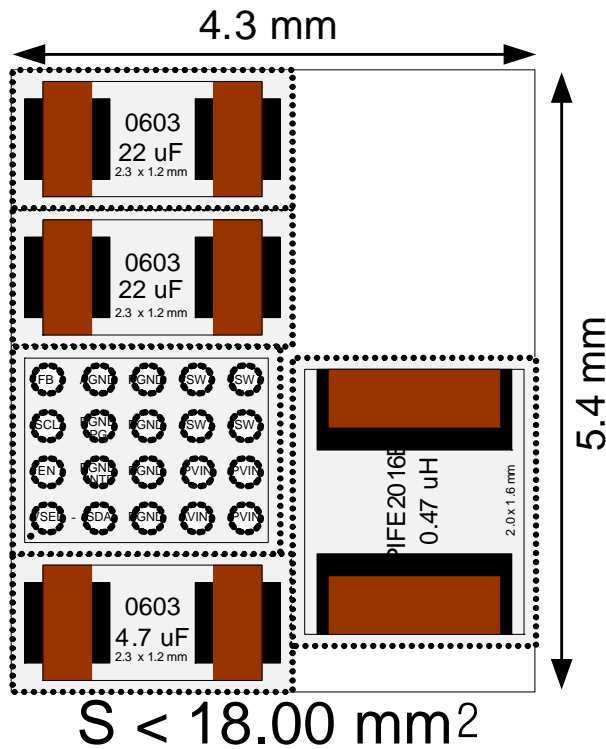


Figure 48. Layout Recommendation

Input capacitor placed as close as possible to the IC.

PVIN directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

AVIN connected to the Vin plane just after the capacitor.

AGND directly connected to the GND plane.

PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

SW connected to the Lout inductor with local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

Legend:

In green are top layer planes and wires

In yellow are layer1 plane and wires (just below top layer)

Big circles gray are normal vias

Small circles gray are top to layer1 vias

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ORDERING INFORMATION

| Device | Marking | Configuration | Package | Shipping† |
|---------------|----------|--------------------------------|-------------------------------------|--------------------|
| NCP6335FFCT1G | NCP6335F | 3.5 A Transient Load Helper | WLCSP20 2.02 x 1.62 mm (Pb-Free) | 3000 / Tape & Reel |
| NCP6335FFCT2G | NCP6335F | 3.5 A Transient Load Helper | WLCSP20 2.02 x 1.62 mm (Pb-Free) | 3000 / Tape & Reel |
| NCP6335DFCT1G | NCP6335D | 2.5 A Stand-Alone | WLCSP20 2.02 x 1.62 mm (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

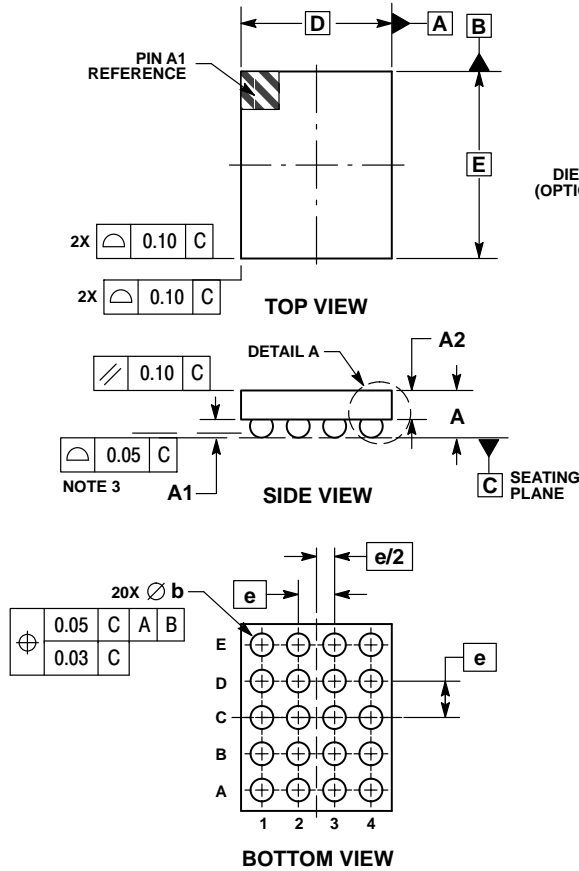
Demo Board Available:

The NCP6335FGEVB/D evaluation board that configures the device in typical application to supply constant voltage.

NCP6335

PACKAGE DIMENSIONS

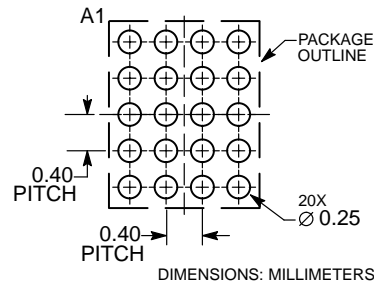
WLCSP20, 1.62x2.02
CASE 568AG
ISSUE D



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | --- | 0.60 |
| A1 | 0.17 | 0.23 |
| A2 | 0.33 | 0.39 |
| A3 | 0.02 | 0.04 |
| b | 0.24 | 0.28 |
| D | 1.62 BSC | |
| E | 2.02 BSC | |
| e | 0.40 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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