



NX3020NAKS

30 V, 180 mA dual N-channel Trench MOSFET

11 November 2013

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection
- Low threshold voltage

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

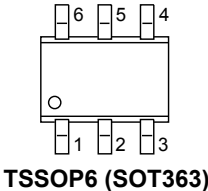
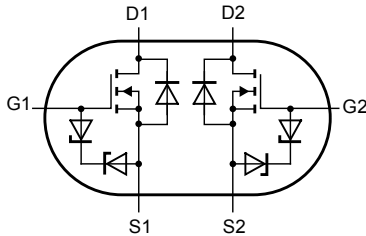
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	180	mA
Static characteristics (per transistor)							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$		-	2.7	4.5	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 TSSOP6 (SOT363)	 017aaa256
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3020NAKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code
	[1]
NX3020NAKS	Ua%

[1] % = placeholder for manufacturing site code

8. Limiting values

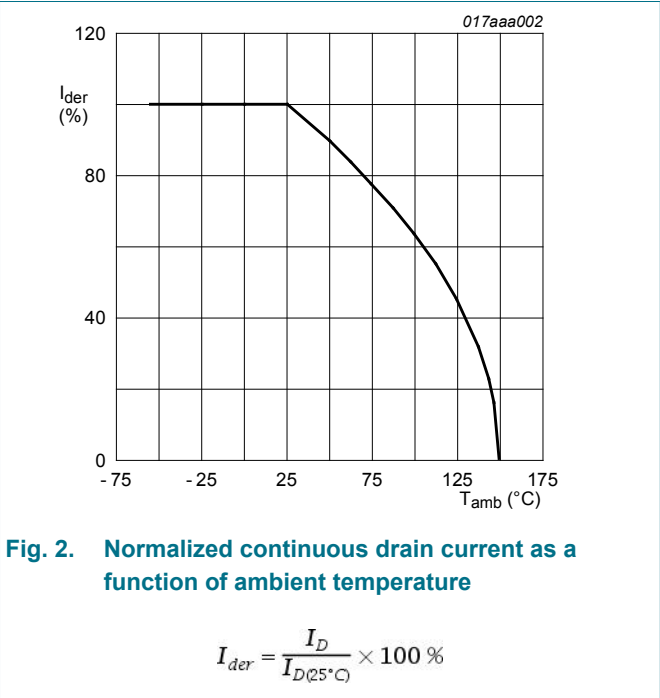
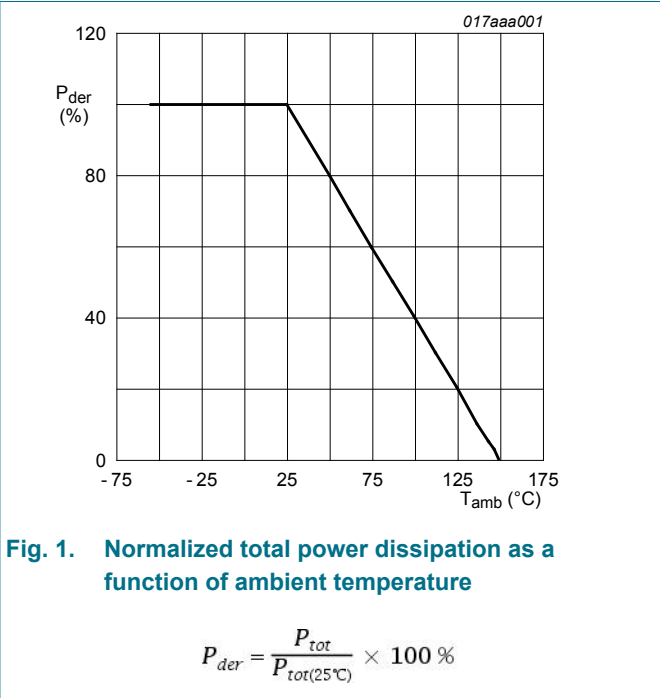
Table 5. Limiting values

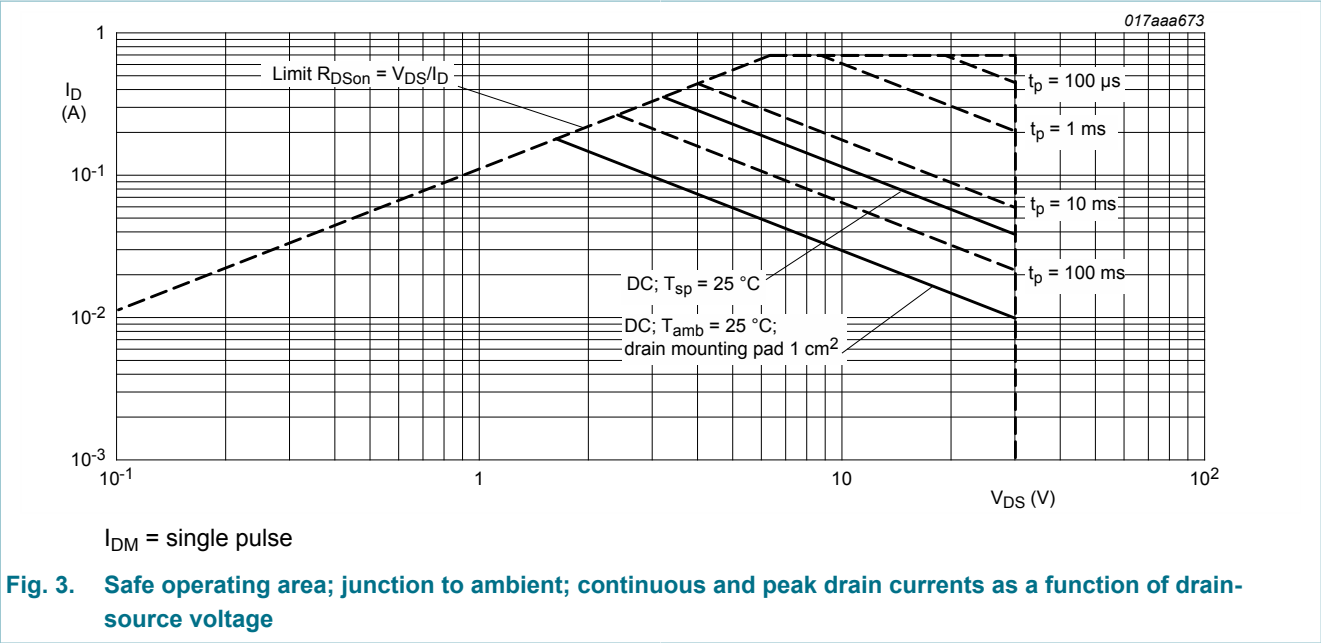
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	180	mA
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	110	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	720	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	260	mW
			[1]	-	280	mW

Symbol	Parameter	Conditions		Min	Max	Unit
		T _{sp} = 25 °C		-	1100	mW
Source-drain diode						
I _S	source current	T _{amb} = 25 °C		-	180	mA
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	375	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





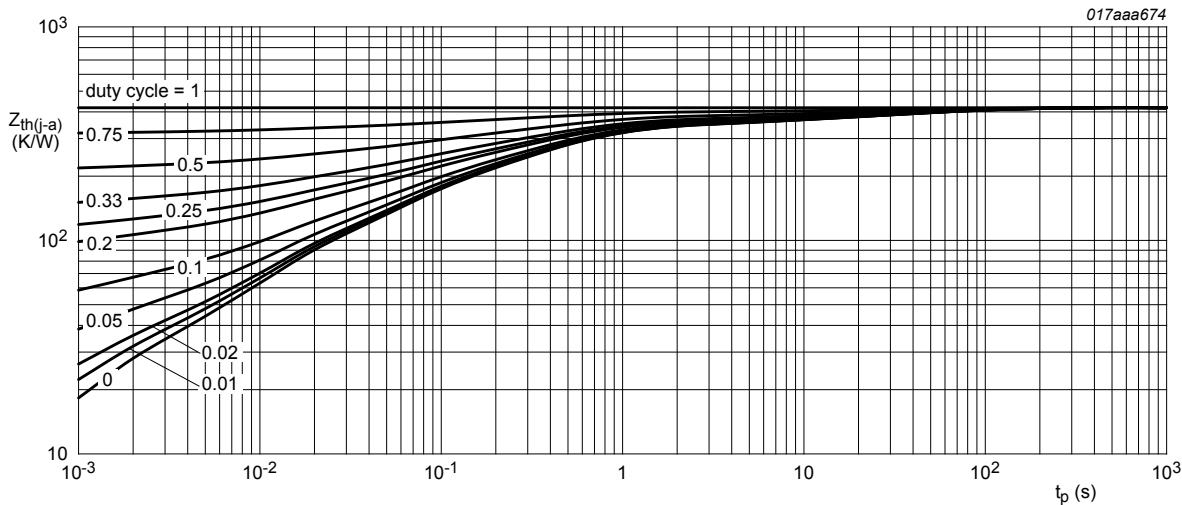
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	480	K/W
			[2]	-	380	430	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	110	K/W

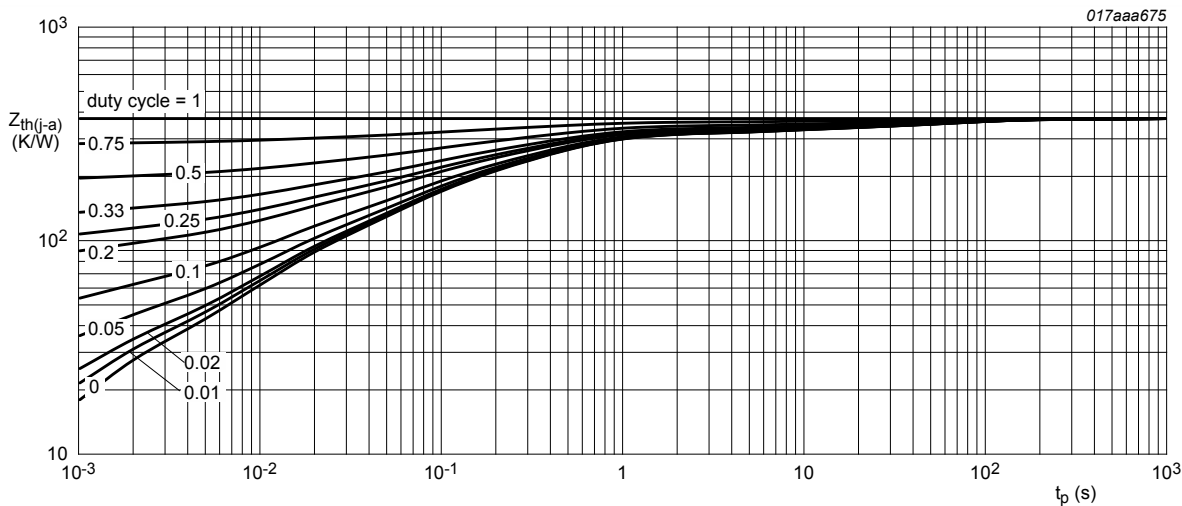
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		0.8	1.2	1.5	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 150 °C		-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	3.5	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	3.5	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	0.5	μA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	0.5	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 100 mA; T _j = 25 °C		-	2.7	4.5	Ω
		V _{GS} = 10 V; I _D = 100 mA; T _j = 150 °C		-	5.5	9.2	Ω
		V _{GS} = 4.5 V; I _D = 100 mA; T _j = 25 °C		-	3	5.2	Ω
		V _{GS} = 2.5 V; I _D = 10 mA; T _j = 25 °C		-	4	13	Ω
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 150 mA; T _j = 25 °C		-	320	-	mS
Dynamic characteristics (per transistor)							
Q _{G(tot)}	total gate charge	V _{DS} = 15 V; I _D = 150 mA; V _{GS} = 4.5 V; T _j = 25 °C		-	0.34	0.44	nC
Q _{GS}	gate-source charge			-	0.11	-	nC
Q _{GD}	gate-drain charge			-	0.06	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	13	20	pF
C _{oss}	output capacitance			-	2.6	-	pF
C _{rss}	reverse transfer capacitance			-	1.1	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 250 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	5	10	ns
t _r	rise time			-	5	-	ns
t _{d(off)}	turn-off delay time			-	34	68	ns
t _f	fall time			-	17	-	ns
Source-drain diode (per transistor)							
V _{SD}	source-drain voltage	I _S = 115 mA; V _{GS} = 0 V; T _j = 25 °C		0.47	0.7	1.2	V

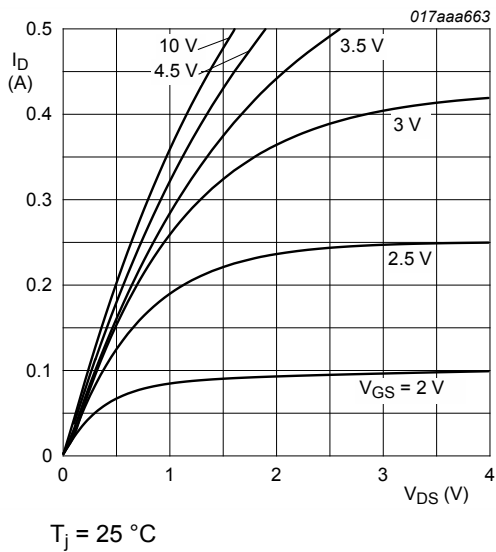


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

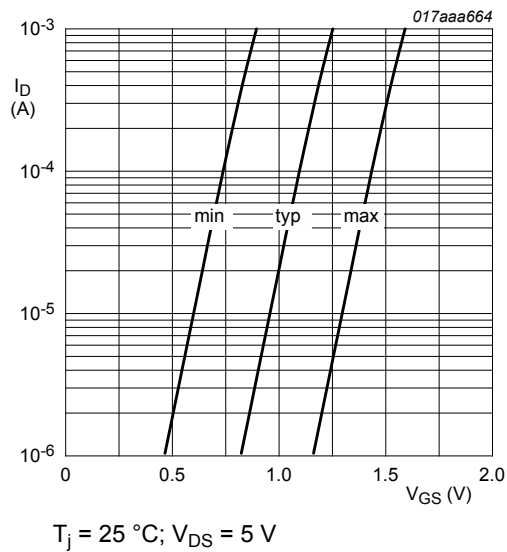


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

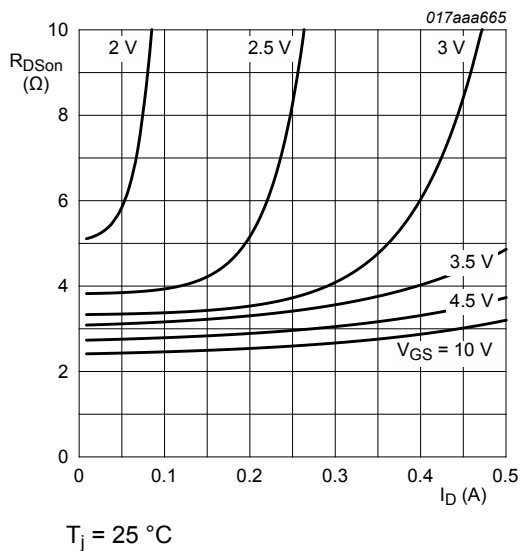


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

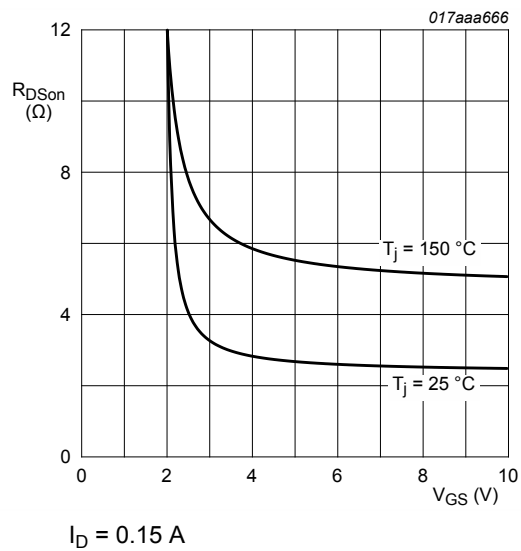


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

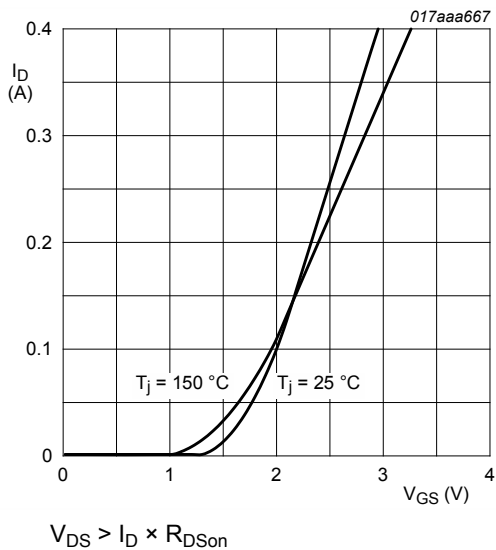


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

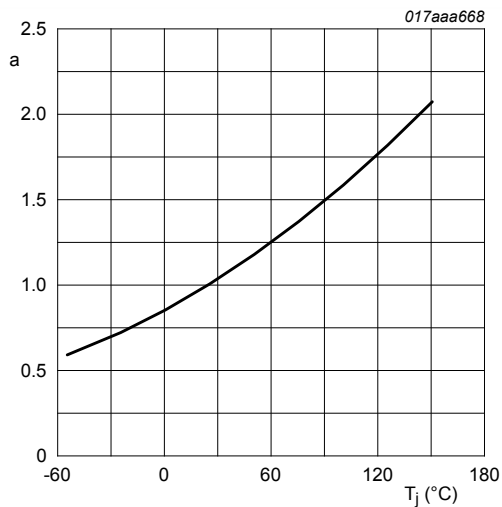


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

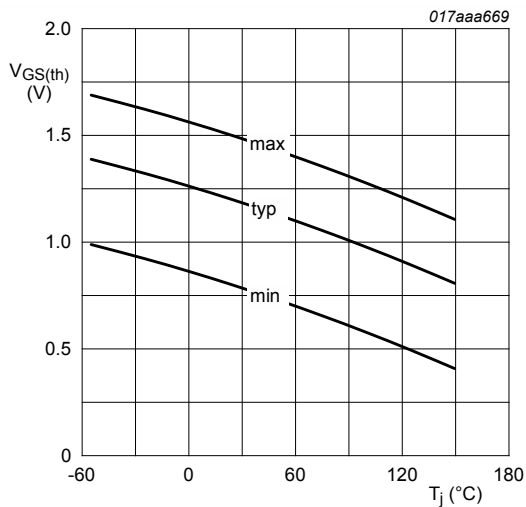


Fig. 12. Gate-source threshold voltage as a function of junction temperature

$I_D = 0.25\text{ mA}$; $V_{DS} = V_{GS}$

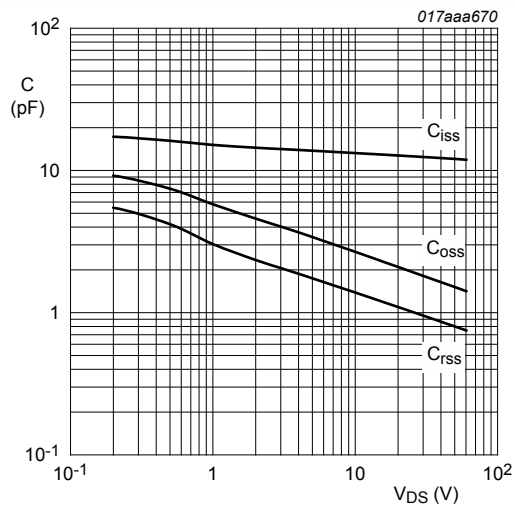


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$f = 1\text{ MHz}$; $V_{GS} = 0\text{ V}$

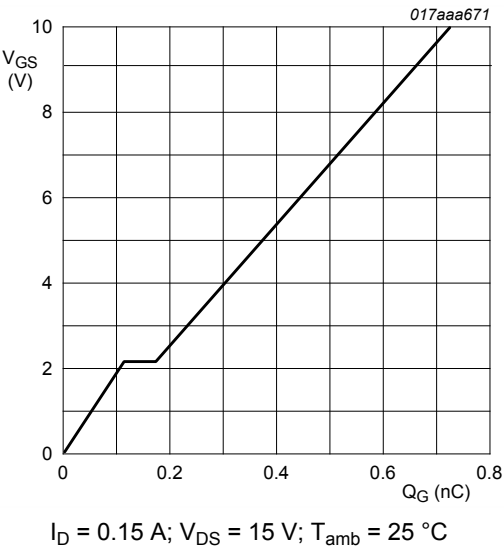


Fig. 14. Gate-source voltage as a function of gate charge; typical values

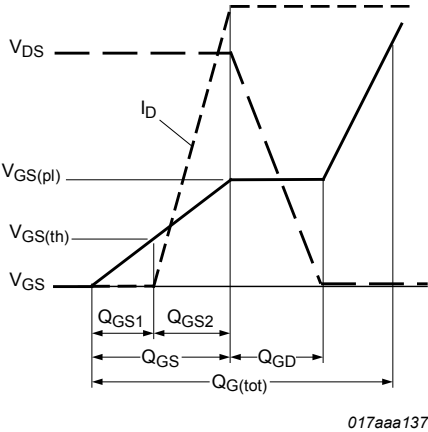


Fig. 15. Gate charge waveform definitions

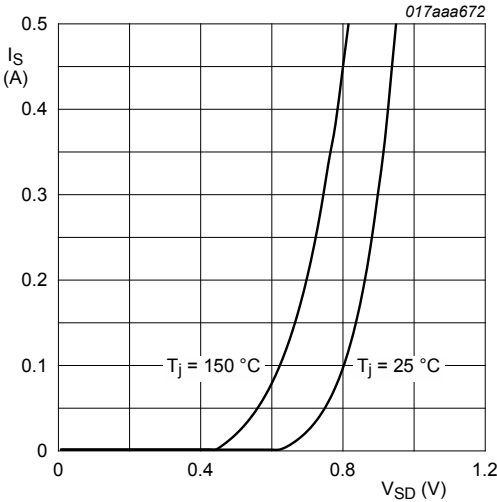


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

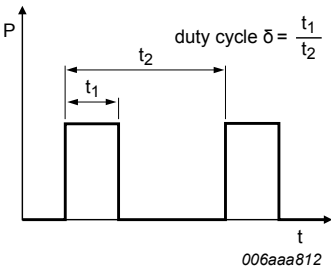


Fig. 17. Duty cycle definition

12. Package outline

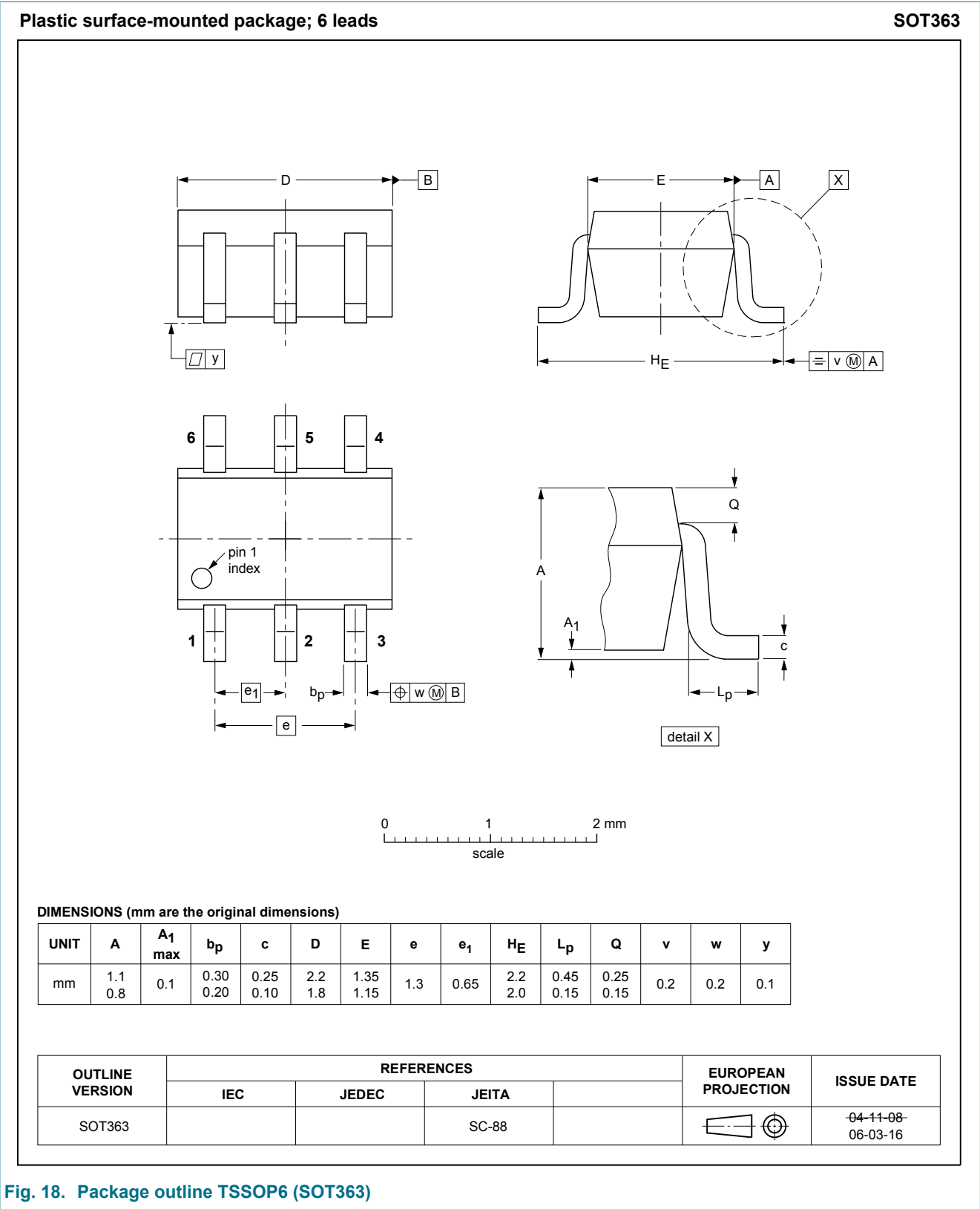


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

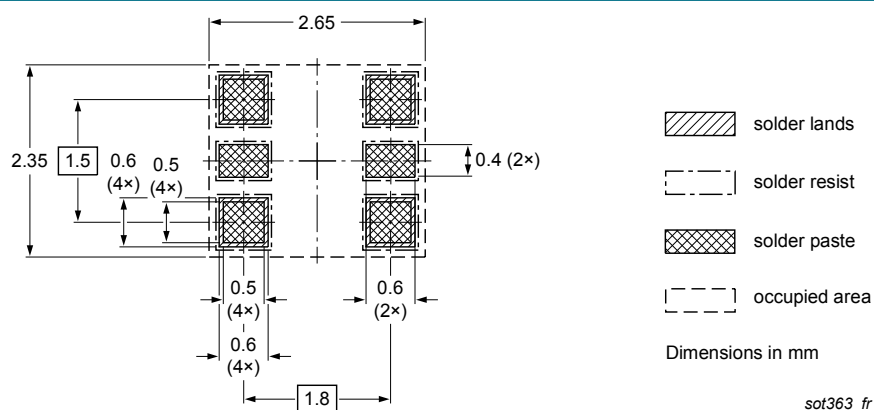


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

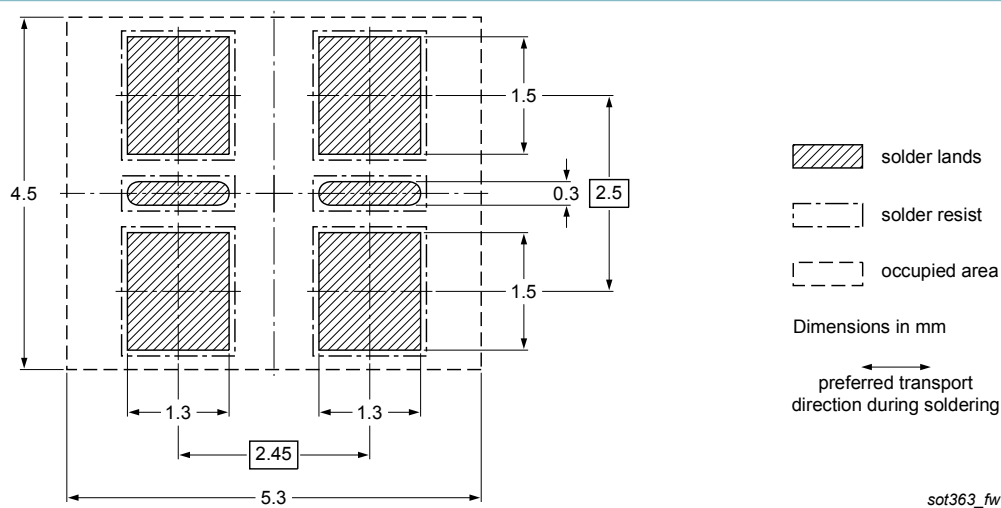


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX3020NAKS v.3	20131111	Product data sheet	-	NX3020NAKS v.2
Modifications:	Marking code corrected			
NX3020NAKS v.2	20131029	Product data sheet	-	NX3020NAKS v.1
NX3020NAKS v.1	20120706	Product data sheet	-	-

15. Legal information

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Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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