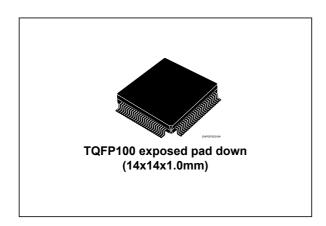


# Automotive advanced airbag IC for mid/high end applications

#### Datasheet - production data



#### **Features**



- AEC-Q100 qualified
- Boost regulator for energy reserve
  - 1.882 MHz operation,  $I_{load}$  = 70 mA max
  - Output voltage user selectable, 23 V/ 33 V ±5%
  - Capacitor value & ESR diagnostics
- Boost regulator for PSI-5 SYNC pulse
  - 1.882 MHz operation,
  - Output voltage, 12 V/14.75 V, user configurable
- Buck regulator for remote sensor
  - 1.882 MHz operation
  - Output voltage, 7.2 V/9 V ±4%, user configurable
- Buck regulator for micro controller unit
  - 1.882 MHz operation
  - Output voltage user selectable, 3.3 V or 5.0 V ±3%
- · Integrated energy reserve crossover switch
  - 3 Ω 912 mA max
  - Switch active output indicator
- Battery voltage monitor & shutdown control with Wake-up control

- System voltage diagnostics with integrated ADC
- · Squib deployment drivers
  - 12 channel HSD/LSD
  - 25 V max deployment voltage
  - Various deployment profiles
  - Current monitoring
  - R<sub>measure</sub>, STB, STG & Leakage diagnostics
  - High & low side driver FET tests
- High side safing switch regulator and enable control
- Four channel remote sensor interface
  - PSI-5 satellite sensors
  - Active wheel speed sensors
- Three channel GPO, HSD or LSD configurable, with PWM 0-100% control
- Nine channel hall-effect, resistive or switch sensor interface
- User customizable safing logic
- · Specific disarm signal for passenger airbag
- Temporal and algorithmic Watchdog timers
- End of life disposal interface
- Temperature sensor
- 32 bit SPI communications
- 5.5 V minimum operating voltage at device battery pin
- Operating temperature, -40 to 95 °C
- Packaging 100 pin

Table 1. Device summary

Order code	Package	Pacing
L9680 TQFP100		Tray
		Tape & Reel

Contents L9680

# **Contents**

1	Desc	ription		13
2	Abso	lute ma	aximum ratings	14
3	Oper	ative m	aximum ratings	18
4	Pin o	ut		22
5	Over	view an	nd block diagram	23
	5.1	Power	supply	24
	5.2	Deploy	ment drivers	24
	5.3	Remote	e sensor interfaces (4)	25
	5.4	DC ser	nsor interfaces (9)	25
	5.5	Genera	al purpose outputs (3)	25
	5.6		logic	
	5.7	_	features	
6	Start-	-up and	l power control	27
	6.1	Power	supply overview	27
	6.2	Power	mode control	29
		6.2.1	POWER OFF mode	30
		6.2.2	SLEEP mode	30
		6.2.3	ACTIVE mode	30
		6.2.4	PASSIVE mode	30
		6.2.5	Power-up and power-down sequences	
		6.2.6	IC operating states	38
	6.3	ERBO	OST switching regulator	39
	6.4		reserve capacitor charging and discharging circuits	41
		Energy		
	6.5	O,	P diagnostic	42
	6.5	O,		
	6.5	ER CA	P diagnostic	42
	6.5	ER CA 6.5.1 6.5.2	P diagnostic	42 44
		ER CA 6.5.1 6.5.2 ER swi	P diagnostic	42 44 45



L9680 Contents

	6.8	SATBU	CK regulator	48
	6.9	VCC bu	ck regulator	48
	6.10	VCORE	MON external core voltage monitor	50
	6.11		julator and control	
	6.12	_	ors	
	6.13		ontrol	
	0.10	1103010		01
7	SPI in	iterface	S	54
	7.1	SPI prot	cocol	54
	7.2	Global S	SPI register map	55
	7.3	Global S	SPI tables	67
		Global S	PI read/write register	. 69
		7.3.1	Fault status register (FLTSR)	. 69
		7.3.2	System configuration register (SYS_CFG)	. 72
		7.3.3	System control register (SYS_CTL)	. 75
		7.3.4	SPI Sleep command register (SPI_SLEEP)	. 77
		7.3.5	System status register (SYS_STATE)	. 77
		7.3.6	Power state register (POWER_STATE)	. 79
		7.3.7	Deployment configuration registers (DCR_x)	. 82
		7.3.8	Deployment command (DEPCOM)	. 84
		7.3.9	Deployment status registers (DSR_x)	. 85
		7.3.10	Deployment current monitor registers (DCMTSxy)	. 87
		7.3.11	Deploy enable register (SPIDEPEN)	. 88
		7.3.12	Deployment ground loss register (LP_GNDLOSS)	. 88
		7.3.13	Device version register (VERSION_ID)	
		7.3.14	Watchdog retry configuration register (WD_RETRY_CONF)	
		7.3.15	Microcontroller fault test register (MCU_FLT_TEST)	
		7.3.16	Watchdog timer configuration register (WDTCR)	
		7.3.17	WD1 timer control register (WD1T)	
		7.3.18	WD state register (WDSTATE)	
		7.3.19	Clock configuration register (CLK_CONF)	
		7.3.20	Scrap seed read command register (SCRAP_SEED)	
		7.3.21	Scrap key write command register (SCRAP_KEY)	
		7.3.22	Scrap state entry command register (SCRAP_STATE)	
		7.3.23	Safing state entry command register (SAFING_STATE)	
		7.3.24	WD2 recover write command register (WD2_RECOVER)	. 97

Contents L9680

	7.3.25	WD2 seed read command register (WD2_SEED)	. 98
	7.3.26	WD2 key write command register (WD2_KEY)	. 98
	7.3.27	WD test command register (WD_TEST)	. 99
	7.3.28	System diagnostic register (SYSDIAGREQ)	100
	7.3.29	Diagnostic result register for deployment loops (LPDIAGSTAT)	101
	7.3.30	Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)	104
	7.3.31	Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)	107
	7.3.32	DC sensor diagnostic configuration command register (SWCTRL) $\dots$	108
	7.3.33	ADC request and data registers (DIAGCTRL_x)	110
	7.3.34	Configuration register for switching regulators (SW_REGS_CONF)	113
	7.3.35	Global configuration register for GPO driver function (GPOCR)	115
	7.3.36	GPOx control register (GPOCTRLx)	116
	7.3.37	GPO fault status register (GPOFLTSR)	117
	7.3.38	Wheel speed sensor test request register (WSS_TEST)	120
	7.3.39	PSI5/WSS configuration register for channel x (RSCRx)	121
	7.3.40	Remote sensor control register (RSCTRL)	125
	7.3.41	WSS Threshold configuration register 1 (RS_AUX_CONF1)	126
	7.3.42	WSS Threshold configuration register 2 (RS_AUX_CONF2)	126
	7.3.43	Safing algorithm configuration register (SAF_ALGO_CONF)	127
	7.3.44	Arming signals register (ARM_STATE)	128
	7.3.45	ARMx assignment registers to specific Loops (LOOP_MATRIX_ARMx)	129
	7.3.46	ARMx enable pulse stretch timer status (AEPSTS_ARMx)	130
	7.3.47	Passenger inhibit upper threshold for DC sensor 0 (PADTHRESH_HI) .	131
	7.3.48	Passenger inhibit lower threshold for DC sensor 0 (PADTHRESH_LO)	131
	7.3.49	Assignment of PSINH signal to specific Loop(s) (LOOP_MATRIX_PSINH)	132
	7.3.50	Safing records enable register (SAF_ENABLE)	132
	7.3.51	Safing records request mask registers (SAF_REQ_MASK_x)	133
	7.3.52	Safing records request target registers (SAF_REQ_TARGET_x)	135
	7.3.53	Safing records response mask registers (SAF_RESP_MASK_x)	137
	7.3.54	Safing records response mask registers (SAF_RESP_TARGET_x)	139
	7.3.55	Safing records data mask registers (SAF_DATA_MASK_x)	141
	7.3.56	Safing record threshold registers (SAF_THRESHOLD_x)	143
	7.3.57	Safing control x registers (SAF_CONTROL_x)	145
	7.3.58	Safing record compare complete register (SAF_CC)	148
7.4	Remote	sensor SPI register map	149
		-	



	7.5	Remot	te sensor SPI tables	150
		7.5.1	Remote sensor SPI global status word	150
	7.6	Remot	te sensor SPI read/write registers	151
		7.6.1	Remote sensor data/fault registers (RSDRx @FLT = 0)	151
		7.6.2	Remote sensor data/fault registers w/o fault (RSDRx @ FLT=1) .	154
		7.6.3	Remote sensor x current registers y (RSTHRx_y)	158
		7.6.4	Arming signals register (ARM_STATE)	159
		7.6.5	Safing record compare complete register (SAF_CC)	160
8	Depl	oyment	t drivers	161
	8.1	Contro	ol logic	161
		8.1.1	Deployment current selection	163
		8.1.2	Deploy command expiration timer	163
		8.1.3	Deployment control flow	164
		8.1.4	Deployment current monitoring	165
		8.1.5	Deployment success	165
	8.2	Energy	y reserve - deployment voltage	165
	8.3	Deploy	yment ground return	165
	8.4	Deploy	yment driver protections	166
		8.4.1	Delayed low-side deactivation	166
		8.4.2	Low-side voltage clamp	166
		8.4.3	Short to battery	166
		8.4.4	Short to ground	166
		8.4.5	Intermittent open squib	166
	8.5	Diagno	ostics	167
		8.5.1	Low level diagnostic approach	168
		8.5.2	High level diagnostic approach	175
9	Rem	ote sen	sor interface	177
	9.1	PSI5 n	node	178
		9.1.1	Functional description	178
		9.1.2	Sensor data integrity: LCID and CRC	
		9.1.3	Detailed description	
	9.2	Active	wheel speed sensor	184
		9.2.1	Wheel speed data register formats	
		9.2.2	Test mode	



	9.3	Remote sensor interface fault protection	36
		9.3.1 Short to ground, current limit	
		9.3.2 Short to battery	37
		9.3.3 Cross link	37
		9.3.4 Leakage to battery, sensor open	37
		9.3.5 Leakage to ground	37
		9.3.6 Thermal shutdown	37
10	Watc	ndog timers18	8
	10.1	Temporal watchdog (WD1)	38
		10.1.1 Watchdog timer configuration	39
		10.1.2 Watchdog timer operation	90
	10.2	Algorithmic watchdog (WD2) 19	1
	10.3	Watchdog reset assertion timer	3
	10.4	Watchdog timer disable input (WDT/TM)	)3
11	DC s	nsor interface	4
	11.1	Passenger inhibit interface	)6
12	Safir	յ logic ․․․․․․․․․․․․․․․․․․․․․	8
	12.1	Safing logic overview	98
	12.2	SPI sensor data decoding	9
	12.3	In-frame and out-of-frame responses	)6
	12.4	Safing state machine operation	
		12.4.1 Simple threshold comparison operation	)7
	12.5	Safing engine output logic (ARMxINT)	8(
		12.5.1 Arming pulse stretch	11
	12.6	Additional communication line	2
13	Gene	ral purpose output (GPO) drivers	5
14	Syst	m voltage diagnostics	8
	14.1	Analog to digital algorithmic converter	23
15	Temp	erature sensor	<u>'</u> 5



16	Elect	rical characteristics	226
	16.1	Configuration and control	226
	16.2	Internal analog reference	231
	16.3	Internal regulators	232
	16.4	Watchdog	233
	16.5	Oscillators	234
	16.6	Reset	235
	16.7	SPI interface	236
	16.8	ERBoost regulator	238
	16.9	ER CAP current generators and diagnostic	241
	16.10	ER switch	242
	16.11	COVRACT	243
	16.12	SYNCBOOST converter	243
	16.13	SATBUCK converter	246
	16.14	VCC regulator	247
	16.15	VSF regulator	249
	16.16	Deployment drivers	250
	16.17	Deployment driver diagnostic	255
		16.17.1 Squib resistance measurement	. 255
		16.17.2 Squib leakage test (VRCM)	. 257
		16.17.3 High/low side FET test	. 258
		16.17.4 Deployment timer test	. 259
	16.18		
		16.18.1 PSI-5 interface	
	40.40	16.18.2 WSS interface	
		Safing engine	
		General purpose output drivers	
		Analog to digital converter	
		Voltage diagnostics (Analog MUX)	
	16.24	Temperature sensor	2/4
17	Quali	ty information	275
	17.1	OTP memory	



Contents		L9680
18	Errata sheet	. 276
19	Package information	. 277
	19.1 TQFP100 (14x14x1.4 mm exp. pad down) package information	. 277
20	Revision history	. 279

L9680 List of tables

# List of tables

Table 1.	Device summary	
Table 2.	Absolute maximum ratings	
Table 3.	Operative maximum ratings	
Table 4.	Functions disabling by state	
Table 5.	SPI MOSI and MISO frames layout	
Table 6.	Global SPI register map	
Table 7.	Global SPI Global Status Word	
Table 8.	Remote sensor SPI register map	
Table 9.	GSW - Remote sensor SPI global status word	
Table 10.	Short between loops diagnostics decoding	
Table 11.	HS FET TEST	
Table 12.	LS FET TEST	
Table 13.	Watchdog timer status description	
Table 14.	WD2 states and signals	
Table 15.	Example of combine function operation	
Table 16.	Short to ground fault in LS mode	
Table 17.	Short to battery fault in HS mode	
Table 18.	Diagnostics control register (DIAGCTRLx)	
Table 19.	Diagnostics divider ratios	
Table 20.	Configuration and control DC specifications	
Table 21.	Configuration and control AC specifications	
Table 22.	Open ground detection DC specifications	
Table 23.	GND_OPEN_AC - Open ground detection DC specifications	
Table 24.	Internal analog reference	
Table 25.	Internal regulator DC specifications	
Table 26.	Internal regulators AC specifications	
Table 27.	Temporal watchdog timer AC specifications (WD1)	
Table 28.	Algorithmic watchdog timer DC specifications (WD2)	
Table 29.	Algorithmic watchdog timer AC specifications (WD2)	
Table 30.	Oscillators specifications	
Table 31.	Reset DC specifications	
Table 32.	Reset AC specifications	
Table 33.	Global and remote sensor SPI DC specifications	
Table 34.	SPI AC specifications	
Table 35.	ERBoost regulator DC specifications	
Table 36.	ERBoost regulator AC specifications	
Table 37.	ERBOOST Converter external components design info	
Table 38.	ER CAP current generators and diagnostic DC specifications	
Table 39.	ER CAP current generators and diagnostic AC specifications	
Table 40.	ER Switch DC specifications	
Table 41.	ER Switch AC specifications	
Table 42.	COVRACT DC specifications	
Table 43.	COVRACT AC specifications	
Table 44.	SYNCBOOST converter DC specifications	
Table 45.	SYNCBOOST converter AC specifications	
Table 46.	SYNCBOOST converter external components design info	
Table 47.	SATBUCK converter DC specifications	
Table 48.	SATBUCK converter AC specifications	247



List of tables L9680

Table 49.	SATBUCK converter external components design info	247
Table 50.	VCC converter DC specifications	247
Table 51.	VCC converter AC specifications	249
Table 52.	VCC converter external components design info	249
Table 53.	VSF regulator DC specifications	
Table 54.	VSF regulator AC specifications	250
Table 55.	Deployment drivers – DC specifications	
Table 56.	Deployment drivers – AC specifications	254
Table 57.	Deployment drivers diagnostics - Squib resistance measurement	255
Table 58.	Squib Leakage Test (VRCM)	
Table 59.	High/low side FET test	
Table 60.	Deployment timer test - AC specifications	259
Table 61.	PSI-5 satellite transceiver - DC specifications	259
Table 62.	PSI-5 satellite transceiver - AC specifications	261
Table 63.	WSS sensor - DC specifications	
Table 64.	WSS sensor - AC specifications	
Table 65.	DC Sensor interface specifications	266
Table 66.	Arming Interface – DC specifications	267
Table 67.	Arming interface – AC specifications	
Table 68.	GPO interface DC specifications	269
Table 69.	GPO driver interface – AC specifications	271
Table 70.	Analog to digital converter	272
Table 71.	Voltage diagnostics (Analog MUX)	274
Table 72.	Temperature sensor specifications	274
Table 73.	Errata sheet	276
Table 74.	TQFP100 (14x14x1.4 mm exp. pad down) package mechanical data	278
Table 75.	Document revision history	

L9680 List of figures

# List of figures

Figure 1.	Pin connection diagram (top view)	22
Figure 2.	Device function block diagram	
Figure 3.	Power supply block diagram	
Figure 4.	Power control state flow diagram	
Figure 5.	Wake-up input signal behaviour	
Figure 6.	Normal power-up sequence with VCOREMON function disabled	
Figure 7.	Normal power-up sequence with VCOREMON function enabled	34
Figure 8.	Normal power down sequence through POWERMODE SHUTDOWN state - no ER cap	
_	active discharge	35
Figure 9.	Normal power down sequence through Powermode Shutdown state - ER cap active	
J	discharge	36
Figure 10.	Normal power down sequence through ER state	
Figure 11.	IC operating state diagram	39
Figure 12.	ERBOOST regulator block diagram	
Figure 13.	ERBOOST regulator state diagram	
Figure 14.	ER charge state diagram	
Figure 15.	ER discharge state diagram	
Figure 16.	ER CAP measurement block diagram	
Figure 17.	ER CAP measurement timing diagram	
Figure 18.	ER ESR measurement block diagram	
Figure 19.	ER ESR measurement timing diagram	
Figure 20.	ER switch state diagram	
Figure 21.	SYNCBOOST regulator block diagram	
Figure 22.	SYNCBOOST regulator state diagram	
Figure 23.	SATBUCK regulator state diagram	
Figure 24.	VCC regulator state diagram	
Figure 25.	VSF control logic	
Figure 26.	Internal voltage monitors	
Figure 27.	Reset control logic	
Figure 28.	Deployment driver control blocks	
Figure 29.	Deployment driver control logic - Enable signal	
Figure 30.	Deployment driver control logic - Turn-on signals	
Figure 31.	Deployment driver block	
Figure 32.	Global SPI deployment enable state diagram	
Figure 33.	Current monitor counter behavior	
Figure 34.	Deployment loop diagnostics	168
Figure 35.	SRx pull-down enable logic	
Figure 36.	Deployment timer diagnostic sequence	
Figure 37.	High level loop diagnostic flow1	
Figure 38.	High level loop diagnostic flow2	
Figure 39.	Remote sensor interface logic blocks	
Figure 40.	PSI-5 remote sensor protocol (10-bit, 1-bit parity	
Figure 41.	Manchester bit encoding	
Figure 42.	Remote sensor synchronization pulses	
Figure 43.	PSI5 slot timing control	
Figure 44.	Manchester decoder state diagram	
Figure 45.	Wheel speed sensor protocols	
Figure 46.	WD1 Temporal watchdog state diagram	



DS11615 Rev 2 11/280

List of figures L9680

Figure 47.	Watchdog timer refresh diagram	190
Figure 48.	Algorithmic watchdog timer flow diagram	
Figure 49.	DC sensor interface block diagram	
Figure 50.	Passenger inhibit logic diagram	196
Figure 51.	Top level safing engine flow chart	198
Figure 52.	Safing engine – 32-bit message decoding flow chart	199
Figure 53.	Safing engine – 16-bit Message decoding flow chart	
Figure 54.	Safing engine - Validate data flow chart	201
Figure 55.	Safing engine - Combine function flow chart	202
Figure 56.	Safing engine threshold comparison	203
Figure 57.	Safing engine - Compare complete	204
Figure 58.	In-frame example	207
Figure 59.	Out-of-frame example	207
Figure 60.	Safing engine arming flow diagram	209
Figure 61.	Safing engine diagnostic logic	210
Figure 62.	ARMx input/output control logic	
Figure 63.	Pulse stretch timer example	212
Figure 64.	Scrap SEED-KEY state diagram	213
Figure 65.	Scrap ACL state diagram	213
Figure 66.	Disposal PWM signal	214
Figure 67.	GPO driver and diagnostic block diagram	215
Figure 68.	GPO Over temperature logic	
Figure 69.	ADC MUX	
Figure 70.	ADC conversion time	224
Figure 71.	SPI timing diagram	237
Figure 72.	Deployment drivers diagram	254
Figure 73.	TQFP100 (14x14x1.4 mm exp. pad down) package outline	277



L9680 Description

### 1 Description

The L9680 is an advanced airbag system chip solution targeted for mature airbag market and integrated safety markets. This device is family compatible with the L9678 and L9679 devices. Safety system integration is enabled through higher power supply currents and integrated active wheel speed sensor interface. The active wheel speed interface is shared with the PSI-5 satellite interface to create a generic remote safety sensor interface compliant to both systems.

High frequency power supply design allows further cost reduction by using smaller and less expensive external components. All switching regulators operate at 1.882 MHz while buck converters have integrated synchronous rectifiers.

Additional attention is given to system integrity and diagnostics. The reserve capacitor is electrically isolated from the boost regulator by a 65 mA nominal fixed current source, controlling in-rush an additional capacitor discharge fixed current source is integrated to diagnose the reserve capacitor value and ESR. The same current sources can be used to discharge the capacitor at shutdown.

Thanks to low quiescent current, the device can be directly connected to battery. In this way, the device start-up and shutdown are controlled through the wake-up input function. The power supply and crossover function are controlled automatically through the internal state machine.

The user can select both ECU logic voltage ( $V_{CC}$  at 3.3 V or 5.0 V) and energy reserve output voltage (at either 23 V or 33 V). Deployment voltage is set to a maximum of 25 V for all profiles and can be controlled through external safing switch circuit using the high side safing switch reference enabled through the system SPI interface or the arming logic.



DS11615 Rev 2 13/280

# 2 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

The operating junction temperature range is -40 °C to +150 °C. The maximum junction temperature must not be exceeded except when in deployment and within the deploy power stages. Deployment is possible starting with a junction temperature of 150 °C. A power dissipation calculation has to be performed for the final application limiting the available functionality to a subset of it in order to respect to the power dissipation capability.

Table 2. Absolute maximum ratings

Pin#	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.3	$VCC+0.3 \leq 6.5$	V
2	SCLK_RS	Remote SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V
3	MOSI_RS	Remote SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
4	MISO_RS	Remote SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
5	RESET	Reset output	-0.3	VCC+0.3 ≤ 6.5	V
6	MISO_G	Global SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
7	MOSI_G	Global SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
8	SCLK_G	Global SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V
9	CS_G	Global SPI interface chip select	-0.3	VCC+0.3 ≤ 6.5	V
10	WDT/TM	Watchdog disable	-0.3	20	V
11	SR4	Squib 4 low-side pin	-0.3	35	V
12	SF4	Squib 4 high-side pin -1.0 40		40	V
13	SS45	Squib 4 & 5 deployment supply pin	Squib 4 & 5 deployment supply pin -0.3		V
14	SF5	Squib 5 high-side pin	-1.0	40	V
15	SR5	Squib 5 low-side pin	-0.3	35	V
16	SR0	Squib 0 low-side pin	-0.3	35	V
17	SF0	Squib 0 high-side pin	-1.0	40	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
19	SF1	Squib 1 high-side pin	-1.0	40	V
20	SR1	Squib 1 low-side pin	-0.3	35	V
21	SR8	Squib 8 low-side pin	-0.3	35	V
22	SF8	Squib 8 high-side pin	-1.0	40	V
23	SS89	Squib 8 & 9 deployment supply pin	-0.3	40	V
24	SF9	Squib 9 high-side pin	-1.0	40	V
25	SR9	Squib 9 low-side pin	-0.3	35	V
26	DCS8	DC Sensor interface channel 8	-2	40	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit	
27	DCS7	DC Sensor interface channel 7	-2	40	V	
28	DCS6	DC Sensor interface channel 6	-2	40	V	
29	DCS5	DC Sensor interface channel 5	-2	40	V	
30	DCS4	DC Sensor interface channel 4	-2	40	V	
31	DCS3	DC Sensor interface channel 3	-2	40	V	
32	DCS2	DC Sensor interface channel 2	-2	40	V	
33	DCS1	DC Sensor interface channel 1	-2	40	V	
34	DCS0	DC Sensor interface channel 0	-2	40	V	
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	40	V	
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	40	V	
37	RSU2	PSI-5/WSS ch. 2 remote sensor output	-1	40	V	
38	RSU3	PSI-5/WSS ch. 3 remote sensor output	-1	40	V	
39	GPOD0	GPO driver 0 drain output pin	-1	40	V	
40	GPOS0	GPO driver 0 source output pin	-1	40	V	
41	GPOS1	GPO driver 1 source output pin	PO driver 1 source output pin -1 40			
42	GPOD1	GPO driver 1 drain output pin	-1 40		V	
43	GPOD2	GPO driver 2 drain output pin	-1	40	V	
44	GPOS2	GPO driver 2 source output pin	-1	40	V	
45	COVRACT	External Crossover Switch Driver	-0.3	40	V	
46	VCOREMON	External Regulator Monitor	-0.3	VCC+0.3 ≤ 6.5	V	
47	MCUFAULTB	Active Low MCU Fault Monitoring Input	-0.3	VCC+0.3 ≤ 6.5	V	
48	SATSYNC	Initiate Satellite Sensor Sync Pulse	-0.3	VCC+0.3 ≤ 6.5	V	
49	PSINHB	Active Low Passenger Airbag Inhibit Control	-0.3	VCC+0.3 ≤ 6.5	V	
50	GNDSUB1	Substrate ground / Squib ground	-0.3	0.3	V	
51	SRB	Squib B low-side pin	-0.3	35	V	
52	SFB	Squib B high-side pin	-1.0	40	V	
53	SSAB	Squib A & B deployment supply pin	-0.3	40	V	
54	SFA	Squib A high-side pin	-1.0	40	V	
55	SRA	Squib A low-side pin	-0.3	35	V	
56	SR3	Squib 3 low-side pin	-0.3	35	V	
57	SF3	Squib 3 high-side pin	40	V		
58	SS23	Squib 2 & 3 deployment supply pin	40	V		
59	SF2	Squib 2 high-side pin	-1.0	40	V	
60	SR2	Squib 2 low-side pin	-0.3	35	V	
61	SR7	Squib 7 low-side pin	-0.3	35	V	



DS11615 Rev 2 15/280

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
62	SF7	Squib 7 high-side pin	-1.0	40	V
63	SS67	Squib 6 & 7 deployment supply pin	-0.3	40	V
64	SF6	Squib 6 high-side pin	-1.0	40	V
65	SR6	Squib 6 low-side pin	-0.3	35	V
66	GNDA	Analog ground	-0.3	0.3	V
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.3	VCC+0.3 ≤ 6.5	V
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.3	$VCC + 0.3 \leq 6.5$	V
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.3	VCC+0.3 ≤ 6.5	V
70	SAF_CS3	SPI interface safing sensor chip select 3	-0.3	VCC+0.3 ≤ 6.5	V
71	WD2_LockOut	WD2 fault output	-0.3	$VCC + 0.3 \leq 6.5$	V
72	WS3	Wheel speed output Ch3	-0.3	$VCC + 0.3 \leq 6.5$	V
73	WS2	Wheel speed output Ch2	-0.3	$VCC + 0.3 \leq 6.5$	V
74	WS1	Wheel speed output Ch1	-0.3	$VCC + 0.3 \leq 6.5$	V
75	WS0	Wheel speed output Ch0	-0.3	$VCC + 0.3 \leq 6.5$	V
76	VCCSEL	VCC select / VCOREMON disable input	-0.3	40	V
77	ACL	EOL disposal control input	control input -0.3 40		V
78	WAKEUP	Wake-up control input -0.3		40	V
79	VBATMON	Battery line voltage monitor	-18 <sup>(1)</sup>	40	V
80	VSF	Safing regulator supply output	-0.3	40	V
81	VIN	Battery connection	-0.3	40	V
82	VER	Reserve voltage	-0.3	40	V
83	ERBOOST	Energy reserve regulator output	-0.3	40	V
84	ERBSTSW	ER Boost switching output	-0.3	40	V
85	BSTGND	Boost regulators ground	-0.3	0.3	V
86	SYNCBSTSW	SYNC Boost switching output	-0.3	40	V
87	SYNCBOOST	SYNC boost output voltage	-0.3	40	V
88	SATBCKSW	SAT Buck switching output	-0.3	40	V
89	SATGND	SAT Buck regulator ground	-0.3	0.3	V
90	SATBUCK	SAT Buck output voltage -0.3 40		40	-
91	VCCBCKSW	VCC Buck switch output	-0.3	40	V
92	VCCGND	VCC Buck Ground -0.3 0.3		0.3	V
93	CVDD	Internal 3.3V regulator output -0.3 4.6		4.6	V
94	GNDD	Digital ground	-0.3	0.3	-
95	VCC	VCC Buck voltage	-0.3	6.5	V
96	ARM1	Arming output 1	-0.3	VCC+0.3 ≤ 6.5	V



Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
97	ARM2	Arming output 2	-0.3	$VCC + 0.3 \leq 6.5$	V
98	ARM3	Arming output 3	-0.3	VCC+0.3 ≤ 6.5	V
99	ARM4	Arming output 4	-0.3	VCC+0.3 ≤ 6.5	V
100	GNDSUB2	Substrate ground / Squib ground	-0.3	0.3	V
-	Exposed pad down	Substrate ground / Squib ground	-0.3	0.3	V

<sup>1.</sup> VBATMON negative AMR is -18 V or -20 mA.



17/280

# 3 Operative maximum ratings

Within the operating ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
2	SCLK_RS	Remote SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V
3	MOSI_RS	Remote SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
4	MISO_RS	Remote SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
5	RESET	Reset output	-0.1	VCC+0.1 ≤ 5.5	V
6	MISO_G	Global SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
7	MOSI_G	Global SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
8	SCLK_G	Global SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V
9	CS_G	Global SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
10	WDT/TM	Watchdog disable	-0.1	15	V
11	SR4	Squib 4 low-side pin	-0.1	SS45	V
12	SF4	Squib 4 high-side pin	-1.0	SS45	V
13	SS45	Squib 4 & 5 deployment supply pin	-0.1	VER	V
14	SF5	Squib 5 high-side pin	-1.0	SS45	\ \
15	SR5	Squib 5 low-side pin	-0.1	SS45	٧
16	SR0	Squib 0 low-side pin	-0.1	SS01	\ \
17	SF0	Squib 0 high-side pin	-1.0	SS01	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.1	VER	\ \
19	SF1	Squib 1 high-side pin	-1.0	SS01	V
20	SR1	Squib 1 low-side pin	-0.1	SS01	V
21	SR8	Squib 8 low-side pin	-0.1	SS89	V
22	SF8	Squib 8 high-side pin	-1.0	SS89	\ \
23	SS89	Squib 8 & 9 deployment supply pin	-0.1	VER	V
24	SF9	Squib 9 high-side pin	-1.0	SS89	V
25	SR9	Squib 9 low-side pin	-0.1	SS89	V
26	DCS8	DC sensor interface channel 8	-1	18	V
27	DCS7	DC sensor interface channel 7	-1	18	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
28	DCS6	DC sensor interface channel 6	-1	18	V
29	DCS5	DC sensor interface channel 5	-1	18	V
30	DCS4	DC sensor interface channel 4	-1	18	V
31	DCS3	DC sensor interface channel 3	-1	18	V
32	DCS2	DC sensor interface channel 2	-1	18	V
33	DCS1	DC sensor interface channel 1	-1	18	V
34	DCS0	DC Sensor interface channel 0	-1	18	V
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	V <sub>RSU_SYNC_MAX</sub>	V
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	V <sub>RSU_SYNC_MAX</sub>	V
37	RSU2	PSI-5/WSS ch. 2 remote sensor output	-1	V <sub>RSU_SYNC_MAX</sub>	V
38	RSU3	PSI-5/WSS ch. 3 remote sensor output	-1	V <sub>RSU_SYNC_MAX</sub>	V
39	GPOD0	GPO driver 0 drain output pin	-0.1	40	V
40	GPOS0	GPO driver 0 source output pin	-1	40	V
41	GPOS1	GPO driver 1 source output pin	-1	40	V
42	GPOD1	GPO driver 1 drain output pin	-0.1	40	V
43	GPOD2	GPO driver 2 drain output pin	-0.1	40	V
44	GPOS2	GPO driver 2 source output pin	-1	40	V
45	COVRACT	External crossover switch driver	-0.1	40	V
46	VCOREMON	External regulator monitor	-0.1	VCC+0.1 ≤ 5.5	V
47	MCUFAULTB	Active low MCU fault monitoring input	-0.1	VCC+0.1 ≤ 5.5	V
48	SATSYNC	Initiate satellite sensor sync pulse	-0.1	VCC+0.1 ≤ 5.5	V
49	PSINHB	Active low passenger airbag inhibit control	-0.1	VCC+0.1 ≤ 5.5	V
50	GNDSUB1	Substrate ground / Squib ground	-0.1	0.1	V
51	SRB	Squib B low-side pin	-0.1	SSAB	V
52	SFB	Squib B high-side pin	-1.0	SSAB	V
53	SSAB	Squib A & B deployment supply pin	-0.1	VER	V
54	SFA	Squib A high-side pin	-1.0	SSAB	V
55	SRA	Squib A low-side pin	-0.1	SSAB	V
56	SR3	Squib 3 low-side pin	-0.1	SS23	V
57	SF3	Squib 3 high-side pin	-1.0	SS23	V
58	SS23	Squib 2 & 3 deployment supply pin	-0.1	VER	V
59	SF2	Squib 2 high-side pin	-1.0	SS23	V
60	SR2	Squib 2 low-side pin	-0.1	SS23	V
61	SR7	Squib 7 low-side pin	-0.1	SS67	V



DS11615 Rev 2 19/280

Table 3. Operative maximum ratings (continued)

Pin	Pin name	Pin function	Min	Max	Unit	
#	Pili lialile	Pili function	IVIIII	IVIAX	Ullit	
62	SF7	Squib 7 high-side pin	-1.0	SS67	V	
63	SS67	Squib 6 & 7 deployment supply pin	-0.1	VER	V	
64	SF6	Squib 6 high-side pin	-1.0	SS67	V	
65	SR6	Squib 6 low-side pin	-0.1	SS67	V	
66	GNDA	Analog ground	-0.1	0.1	V	
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.1	VCC+0.1 <= 5.5	V	
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.1	VCC+0.1 <= 5.5	V	
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.1	VCC+0.1 <= 5.5	V	
70	SAF_CS3	SPI interface safing sensor chip select 3	-0.1	VCC+0.1 <= 5.5	V	
71	WD2_LockOut	WD2 Fault Output	-0.1	VCC+0.1 <= 5.5	V	
72	WS3	Wheel Speed Output Ch3	-0.1	VCC+0.1 <= 5.5	V	
73	WS2	Wheel Speed Output Ch2	-0.1	VCC+0.1 <= 5.5	V	
74	WS1	Wheel Speed Output Ch1	-0.1	VCC+0.1 <= 5.5	V	
75	WS0	Wheel Speed Output Ch0	-0.1	VCC+0.1 <= 5.5	V	
76	VCCSEL	VCC select / VCOREMON disable input	-0.1	35	V	
77	ACL	EOL disposal control input	-0.1	35	V	
78	WAKEUP	Wake-up control input	-0.1	VIN	V	
79	VBATMON	Battery line voltage monitor	-1	18	V	
80	VSF	Safing regulator supply output	-0.1	27	V	
81	VIN	Battery connection	-0.1	35	V	
82	VER	Reserve voltage	-0.1	35	V	
83	ERBOOST	Energy reserve regulator output	-0.1	35	V	
84	ERBSTSW	ER Boost switching output	-0.1	35	V	
85	BSTGND	Boost regulators ground	-0.1	0.1	V	
86	SYNCBSTSW	SYNC Boost switching output	-0.1	35	V	
87	SYNCBOOST	SYNC boost output voltage	-0.1	35	V	
88	SATBCKSW	SAT Buck switching output	-0.1	35	V	
89	SATGND	SAT Buck regulator ground	-0.1	0.1	V	
90	SATBUCK	SAT Buck output voltage	-0.1	10	-	
91	VCCBCKSW	VCC Buck switch Output	-0.1	10	V	
92	VCCGND	VCC Buck Ground	-0.1	0.1	٧	
93	CVDD	Internal 3.3V regulator output	-0.1	3.6	V	
94	GNDD	Digital ground	-0.1	0.1	-	
95	VCC	VCC Buck Voltage	-0.1	5.5	V	

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Мах	Unit
96	ARM1	Arming Output 1	-0.1	VCC+0.1 <= 5.5	V
97	ARM2	Arming Output 2	-0.1	VCC+0.1 <= 5.5	V
98	ARM3	Arming Output 3	-0.1	VCC+0.1 <= 5.5	V
99	ARM4	Arming Output 4	-0.1	VCC+0.1 <= 5.5	V
100	GNDSUB2	Substrate ground / Squib ground	-0.1	0.1	V
-	Exposed Pad Down	Substrate ground / Squib ground	-0.1	0.1	V



21/280

Pin out L9680

### 4 Pin out

The L9680 pin out is shown below. The IC is housed in a 100 pin package (14 x 14 x 1.0mm) with a 7.6 x 7.6 mm exposed pad down.

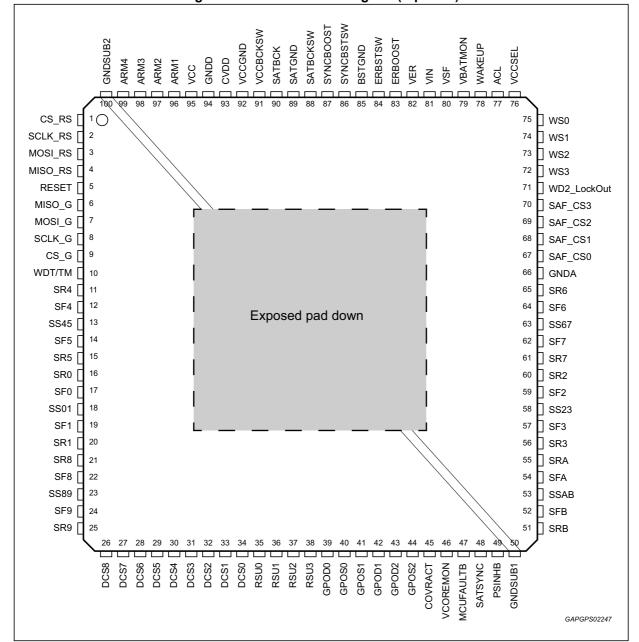


Figure 1. Pin connection diagram (top view)

The exposed pad is electrically shorted to the substrate pins GNDSUB1 and GNDSUB2. These three connection nodes are to be kept shorted on the application.

# 5 Overview and block diagram

The L9680 IC is an application specific standard component air bag system chip. Its main functions include, power management, deployment drivers, remote sensor interfaces (PSI-5 satellite sensors or active wheel speed sensors), diagnostics, deployment arming, hall-effect sensor interface, general purpose output drivers, watchdog timer, microcontroller failsafe input and control and a dedicated passenger airbag disarm signal. A block diagram for this IC is shown in *Figure 2*.

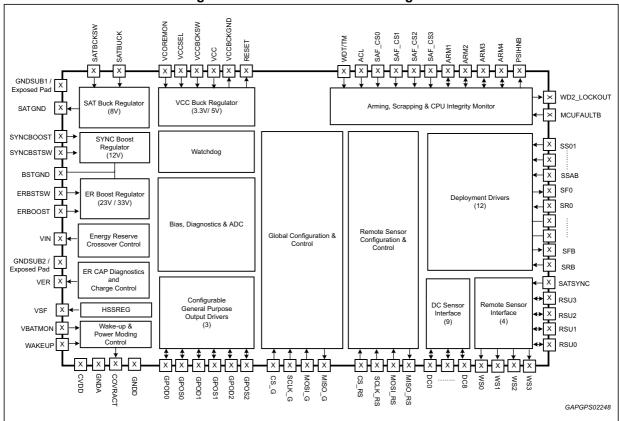


Figure 2. Device function block diagram

57

DS11615 Rev 2 23/280

#### 5.1 Power supply

- Integrated 1.882 MHz boost regulator, 33 V  $\pm$  5% or 23 V  $\pm$  5% nominal output
- Integrated 1.882 MHz boost regulator,12 V/14.75 V nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 7.2 V/9 V ± 4% nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 5 V ± 3% or 3.3 V ± 3% nominal output, user selectable via VCCSEL pin
- Over and under voltage detection and shutdown for all regulators
- Under-voltage lockout to guarantee buck regulator outputs disabled and discharged
- Integrated energy reserve capacitor fixed constant current source (65 mA, nominal) switch for controlled inrush and charge characteristics
- Integrated energy reserve diagnostics, capacitor value and ESR
- Integrated energy reserve crossover switch with current limit and battery input voltage monitoring
- Crossover switch 'active' output signal
- Integrated 25 V/20 V SPI selectable linear regulator for high side safing FET gate supply enabled via SPI or arming logic
- Reset output

#### 5.2 Deployment drivers

- 12 high side deployment drivers, 12 low side deployment drivers
- User programmable deployment options
  - 1.20 A or 1.75 A minimum
  - programmable time in 0.1ms increments
- Capability to deploy a squib with a minimum current of 1.2 / 1.75 A and the SFx shorted to ground up to 25 V on SSxy
- Independently-controlled high-side and low-side FETs
- Squib resistance measurement
- Firing current monitor feature
- High and low side FET tests
- Open & shorts diagnostics, including between loop drivers
- Independent fire enable logic, SPI and discrete digital input

#### 5.3 Remote sensor interfaces (4)

- Quad channel receiver, user selectable
  - standard PSI-5 v1.3 compatible with sync pulse or
  - active wheel speed sensors
- High side drivers for active wheel speed sensor mode (with driver protection)
- Current limit with short circuit protection diagnostics
- PSI-5 satellite sensor mode
  - Auto-adjusting current trip points for each satellite channel
  - Even parity, 8 or 10 bit messages, 125k or 189kbps
  - Satellite message error detection
- Active wheel speed sensor mode
  - Standard active dual level sensors, 7ma/14ma
  - Three level sensors with direction and air gap data, 7ma/14ma/28ma
  - PWM encoded two level sensor, 2 edges/tooth
  - PWM encoded two level sensor, 1 edge/tooth
  - Standard active two and three level sensor data decoding available through SPI

#### 5.4 DC sensor interfaces (9)

- Nine integrated switch interfaces with current sense capability
- Compatible with Hall-effect, resistive and switch sensors
- Current limit protected
- System dedicated path to disable the passenger airbag with input from DC sensor interface

### 5.5 General purpose outputs (3)

- Three configurable high-side or low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit and reverse battery protected

### 5.6 Arming logic

- User configurable safing algorithms with 16 safing records
- Four digital sensor interfaces through SPI
- Independent user programmable thresholds
- Independent user programmable latch timers
- Four discrete and independent arming logic outputs
- Four discrete and independent internal arming signals
- End-of-life interface



DS11615 Rev 2 25/280

#### 5.7 Other features

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control
- Microcontroller 'state of health' input and control function
- Integrated watchdog control with 2 independent structures: windowed WD and algorithmic WD
- Temperature sensor
- Independent thermal shutdown protection on the ER boost switch, the SYNC boost switch, the energy reserve crossover switch, the energy reserve charge paths, the remote sensor interfaces and the general purpose outputs
- All diagnostics are digital and are available through SPI communications
- Configurable logic operation, 5 V or 3.3 V



### 6 Start-up and power control

#### 6.1 Power supply overview

The L9680 IC contains a complete power management system able to provide all necessary voltages for a high feature airbag system or integrated safety system. A general block diagram is shown in *Figure 3*. The power supply block contains the following features:

- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail.
- Energy reserve supply (ERBOOST) achieved through an integrated 1.882 MHz switching boost regulator. The energy reserve capacitor is charged using an internal constant current source controllable through SPI. Besides, a second current source is available to discharge the capacitor. The primary function for the second current source is to diagnose the integrity of the energy reserve capacitor, value and ESR. During system shutdown, the device can enable the discharge current source via SPI command to quickly dissipate the remaining energy stored in the energy reserve capacitor.
- Sync pulse supply (SYNCBOOST) is achieved through an integrated 1.882 MHz switching boost regulator. The SYNCBOOST regulator ensures a minimum voltage is available for operating the satellite sync signal and also provides the input voltage to the remote sensor buck regulator. The sync pulse boost regulator is disabled for battery voltage levels resulting in an output voltage above the set regulation point.
- The integrated current limited ER switch requires no external components. This switch
  is controlled through the integrated power control state machine and is enabled either
  once a loss of battery is detected or a shutdown command is received. Under the same
  conditions also the discrete digital pin COVRACT is activated allowing the control of an
  external optional cross-over switch.
- Two 1.882MHz synchronous buck regulators for remote sensor supply and VCC. The SATBUCK regulator, remote sensor buck supply, is sourced from the SYNCBOOST regulator and can be selected to be either 7.2 V or 9 V nominal. The VCC regulator is sourced from the SATBUCK regulator and is user selectable through the VCCSEL pin to either 5 V or 3.3 V nominal voltage.
- Battery voltage sense input comparator with hysteresis and wake-up input are the primary control signals for the power supply control state machine.
- Based on own mission profile and ECU total current consumption, the user must evaluate if the activation of fast slope option of each ERBoost, SyncBoost and SatBuck regulator (bit 8/9/10, \$3F SW\_REGS\_CONF SPI register) is needed to increase the overall efficiency.



DS11615 Rev 2 27/280

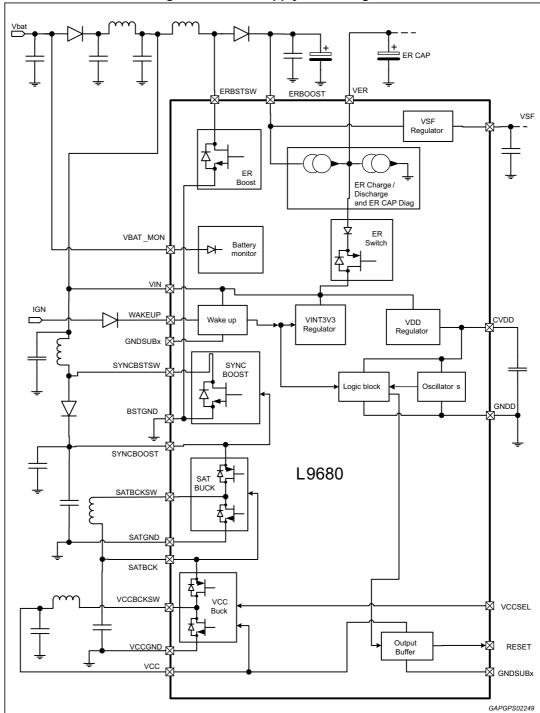


Figure 3. Power supply block diagram



#### 6.2 Power mode control

Start-up and power down of the L9680 are controlled by the WAKEUP pin, VBATMON pin, VIN pin, device status and the SPI interface. There are four main power modes: power-off, sleep, active and passive mode.

Each power mode is described below and represented in the state flow diagram shown in *Figure 4*. The descriptions include references to conditions and sometimes nominal values. The absolute values for each condition are listed in the electrical specifications section.

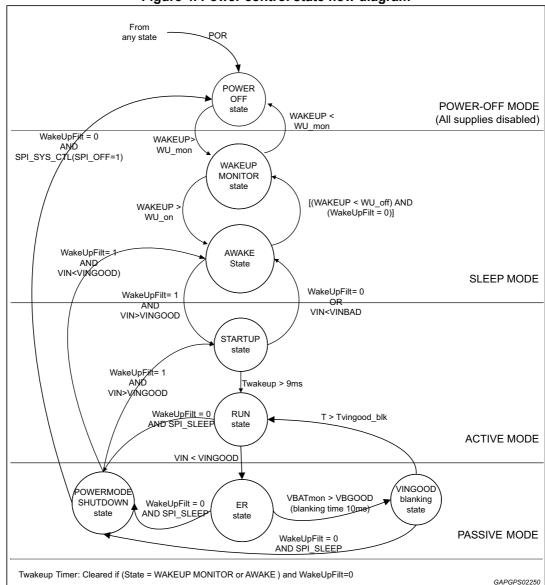


Figure 4. Power control state flow diagram



DS11615 Rev 2

#### 6.2.1 **POWER OFF mode**

During the POWER-OFF Mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as WAKEUP>WU mon the IC will move to SLEEP Mode.

#### **SLEEP mode** 6.2.2

During the Sleep mode the VINT3V3 and CVDD internal regulators are turned on and the IC is ready for full activation of all the other supplies. As soon as VIN voltage is over a minimum threshold, all the other supplies are turned on and the IC enters the ACTIVE mode.

#### 6.2.3 **ACTIVE** mode

This is the normal operating mode for the system.

All power supplies are enabled and the energy reserve boost converter starts to increase the voltage at ERBOOST. Likewise, the SYNCBOOST boost converter continues to charge and regulate to a nominal 12 V (default level at startup). Once the SYNCBOOST has reached a good value, the SATBUCK regulator starts up. In turn, when SATBUCK has ramped up, VCC regulator is enabled. Once the VCC buck regulator is in regulation, RESET is released allowing the system microcontroller and other components to begin their poweron sequence. Among these, also the ER charge current generator can be enabled by the microcontroller via a dedicated SPI command.

The active mode can be left when either WAKEUP pin or VIN voltage drop down. For the very first 9ms after having entered the active mode, the WAKEUP pin low would immediately cause the IC to switch back to sleep mode. After that time, WAKEUP pin low must be first confirmed by a µC SPI SLEEP command prior to cause the system to switch to passive mode. Passive mode is also entered in case of VIN voltage low.

#### 6.2.4 **PASSIVE** mode

In this state, the reserve capacitor charge current and the ERBOOST boost converter are disabled. When in passive mode the device activates both the COVRACT output pin and the integrated ER switch to allow VIN to be connected to the ER capacitor. In this time, VIN is supposed to be increased up to almost VER level and the system operation relies on energy from the ER capacitor. Two scenarios are possible: high or low battery. If VIN < VINGOOD, the device moved from RUN state in ACTIVE mode to the ER state. Here, the ER capacitor is depleted while supplying all the regulators until the POR on internal regulator occurs. The threshold to decide the ER switch activation is based on VIN, because VIN is the supply voltage rail for ERBOOST regulator. If the device has still a good battery level, it entered the POWERMODE SHUTDOWN thanks to a microcontroller command to switch off. In this case, the VER node will be discharged down to approximately VIN level, which then will be supplied out of the battery line. System will continue to run up to a dedicated SPI command to disable the SATBUCK regulator, which will lead the device to enter the POWEROFF state.

The wake-up pin is filtered to suppress undesired state changes resulting from transients or glitches. Typical conditions are shown in the chart below and summarized by state.



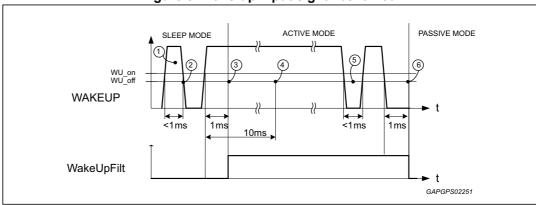


Figure 5. Wake-up input signal behaviour

#### **Condition summary:**

- No change of sleep mode state but current consumption may exceed specification for sleep mode.
- 2. The sleep mode current returns to within specified limits.
- Power supply exits sleep mode. Switchers start operating if applicable voltages exceed under voltage lockouts. As T<sub>wakeup</sub> timeout is not elapsed, a low level at WAKEUP instantaneously sends the system back to sleep.
- 4. Sleep reset is released and the entire system starts operating. An SPI command to enter sleep state would not be executed.
- 5. No change in system status, an SPI command to turn off switchers would be ignored.
- 6. No change in system status, but an SPI command to turn off switchers would be accepted and turn the system off.

With the below table, all the functionalities of the device are shown with respect of the power states. When one function is flagged, the related circuitry cannot be activated on that state.

**Power MODE Power** Sleep **Active Passive** off **Functions** Power VINGOOD Power mode Wakeup ER **Awake** Startup Run monitor off shutdown blanking Wakeup detector Х Χ Internal regulators Χ **ERBOOST** regulator Χ Х Χ Χ Χ Χ Х SYNCBOOST regulator ER CAP charge current Χ Χ Χ Χ Χ Χ ER CAP discharge current Χ Χ Χ Χ Χ ER switch Χ Χ Χ Χ Χ Χ Χ Х Χ Х Х COVRACT

Table 4. Functions disabling by state



DS11615 Rev 2 31/280

Table 4. Functions disabling by state (continued)

	Power MODE							
Functions	Power off	r Sleep		Active		Passive		
	Power off	Wakeup monitor	Awake	Startup	Run	Power mode shutdown	ER	VINGOOD blanking
SATBUCK regulator	Х	Х	Х					
VCC regulator	Х	Х	Х					
Deployment Drivers	Х	Х	Х					
VSF Safing FET regulator	Х	Х	Х					
Remote Sensor Interfaces	Х	Х	Х					
Watchdog	Х	Х	Х					
Diagnostics	Х	Х	Х					
DC Sensor Interface	Х	Х	Х					
GPO drivers	Х	Х	Х					
Safing Logic	Х	Х	Х					

#### 6.2.5 Power-up and power-down sequences

The behaviour of the IC during normal power-up and power-down is shown in *Figure 6* to *Figure 10*. The following sequences represent just a subset of all possible power-up and power-down scenarios. In *Figure 6* a normal IC power-up controlled by the state of the WAKEUP pin is shown assuming the VCOREMON function activated, while in *Figure 7* assuming the VCOREMON function disabled.

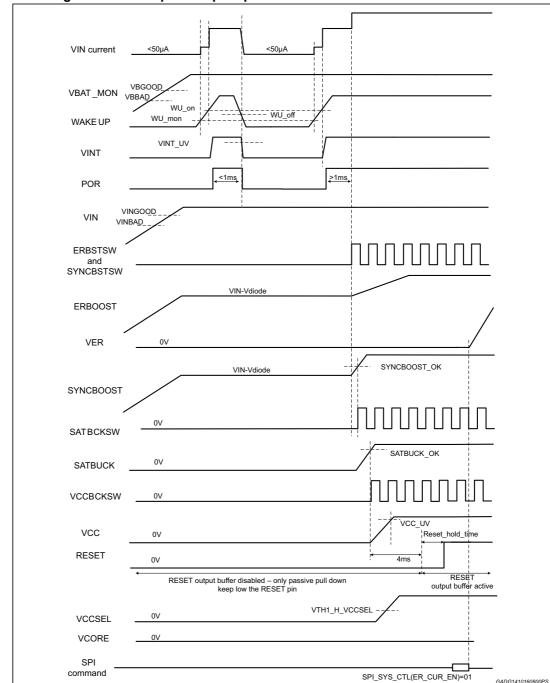


Figure 6. Normal power-up sequence with VCOREMON function disabled

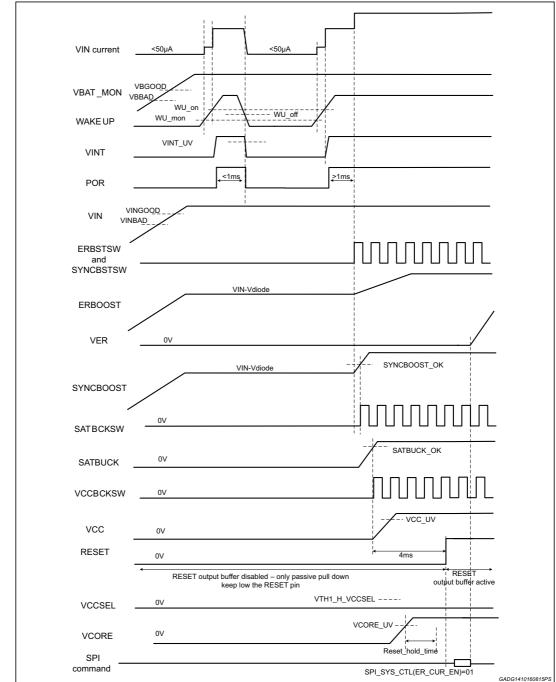


Figure 7. Normal power-up sequence with VCOREMON function enabled



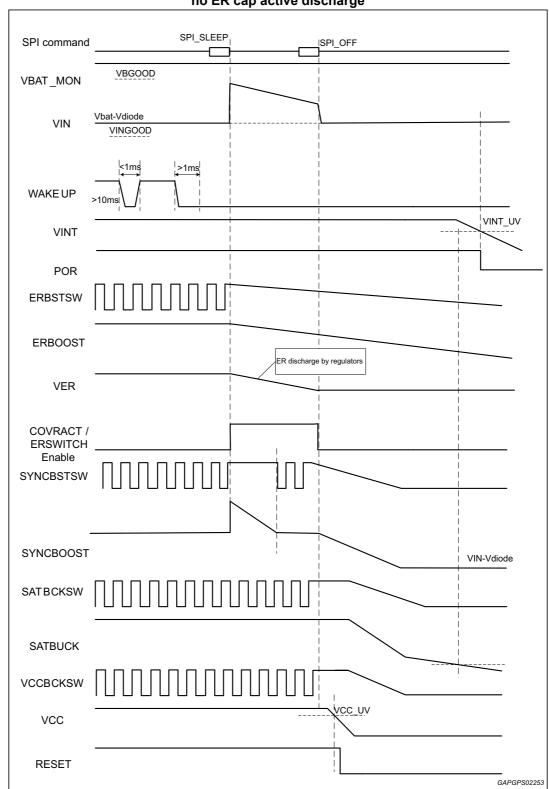


Figure 8. Normal power down sequence through POWERMODE SHUTDOWN state - no ER cap active discharge



SPI\_SYS\_CTL
SPI\_SLEEP| (ER\_CUR\_EN)=10 SPI OFF SPI command VBAT\_MON Vbat-Vdiode VIN VINGOOD <1ms >1ms WAKEUP VINT\_UV VINT POR **ERBSTSW ERBOOST** Vbat-Vdiode --VER\_VBATMON\_VTH ER discharge by regulato VER VIN-0.1V -ER discharge by 70mA Current generator ER\_SWITCH Enable COVRACT SYNCBSTSW VIN-Vdiode SYNCBOOST SATBCKSW SATBUCK VCCBCKSW VCC\_UV VCC RESET GAPG0911151531PS

Figure 9. Normal power down sequence through Powermode Shutdown state - ER cap active discharge



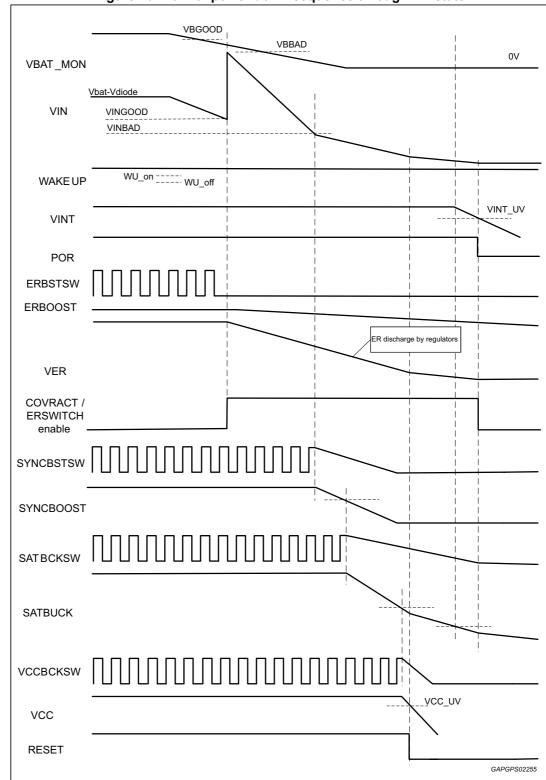


Figure 10. Normal power down sequence through ER state

#### 6.2.6 IC operating states

Different states can be identified while operating the device. These states allow safe and predictable initialization, test, operation and final disposal of the part (scrapping).

As soon as the RESET signal is de-asserted at the beginning of the ACTIVE mode, the microcontroller powers up. At this stage, L9680 is in the Init state: during this state the device must be initialized by the controller. In particular, the watchdog timer window can be programmed during this state.

When the watchdog service begins (upon the first successful watchdog feed), the device switches to Diag state for diagnostics purposes. The remaining configuration of the device is allowed in this state, in particular for safing records and deployment masks. Several tests are also enabled while in this state and all these tests are mutually exclusive to one another. HS and LS switch tests of the squib drivers can only be processed during this Diag state. Also high side safing FET can only be run during this state. When not in Diag state, any commands for squib driver switch tests will be ignored. Other checks are also performed: on the arming outputs to check for non-stuck-at conditions on the pins and on the configured firing time configuration through one of the ARMx pin. The SSM remains in this state until commanded to transition into the Safing state or Scrap state via the dedicated SPI commands.

Upon reception of the SAFING\_STATE command while in Diag state, the device enters Safing state. This is the primary run-time state for normal operation, and the logic performs the safing function, including monitoring of sensor data and setting of the ARMx signals. The only means of exiting Safing state is by the assertion of the SSM\_Reset signal.

The Scrap state is entered upon reception of the SCRAP\_STATE command while in Diag state. While in Scrap state, the part allows the main microcontroller to initiate a transition to Arming state, and monitoring of the Remote Sensor SPI interface and the safing logic is disabled. From Scrap state, the device can transition to Arming state only, and the only means of moving back to Init state is through an SSM Reset.

In order to protect from inadvertent entry into Arming state, and to prevent undesired activation of the safing signals, a handshake mechanism is used to control entry into, and exit from Arming state. This handshake is described further in Section 11.6. While in Arming state, the arming outputs are asserted. Exit from Arming state occurs when the periodic SCRAP\_KEY commands cease (timeout), the key value is incorrect, or when SSM\_Reset is asserted. Upon exit, the device re-enters Scrap state, except for the case of SSM\_Reset, which results in entry into Init state.

The device operating states are shown in *Figure 11*.



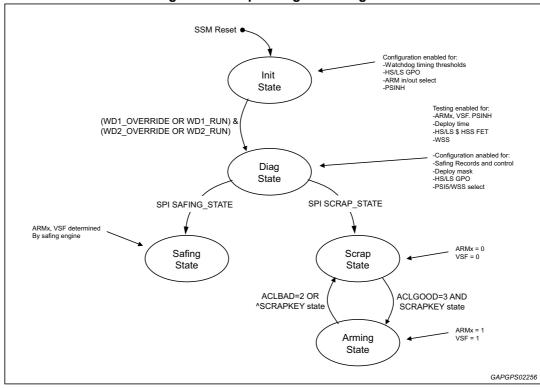


Figure 11. IC operating state diagram

# 6.3 ERBOOST switching regulator

The L9680 IC uses an advanced energy reserve switching regulator operating at 1.882MHz nominal. The higher switching frequency enables the user to select smaller less expensive inductors and moves the operating frequency to permit easier compliance with system emissions.

The ERBoost switching regulator uses a classical peak current mode control loop to properly regulate the output voltage and includes an over-voltage protection that immediately switch off the PowerMOS to protect the device. The regulator includes also a soft start circuit which apply a ramp on the over current threshold from the 40% of IOC\_ERBST value to the maximum one with 16 steps and within 1024 µs. The soft start is restarted every time the regulator has a transition from the ER\_BST\_OFF to the ER\_BST\_ON state.

The energy reserve boost regulator charges the external system tank capacitor through an integrated fixed current source significantly reducing in-rush currents typical of large energy reserve capacitors. The boost circuit provides energy for the reserve capacitor with assumed run time load of less than 20 mA and to the VSF regulator. Once system shutdown is initiated or a loss of battery condition is diagnosed, the boost regulator is by default disabled so that system power can be taken from the energy reserve capacitor. Alternatively, the ER Boost could be kept on even during the ER State by setting the SYS\_CFG(KEEP\_ER\_BOOST\_ON) bit.

The energy reserve boost regulator defaults to 23 V at power-on and can be set to 33 V nominal by the user through an SPI command. The boost converter can also be disabled by the user through an SPI command. Enabling, disabling and setting the boost output voltage



DS11615 Rev 2 39/280

is done through the System Control (SYS\_CTL) register. Boost converter diagnostics include over voltage and under voltage and the circuit is fully protected against shorts. Boost fault status is available through the SPI in Fault Status Register (FLTSR). The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag ERBST\_OT in the FLTSR register is read. In case of loss of BSTGND ground the FET is not turned on. Loss of ground can be detected also when the FET is off thanks to a pull-up current present on the BSTGND pin. The FET will be automatically reactivated as soon as ground connection is restored. Over-voltage protection from load dump and inductive flyback is provided via an active clamp and an ER\_Boost disable circuitry, see *Figure 12*.

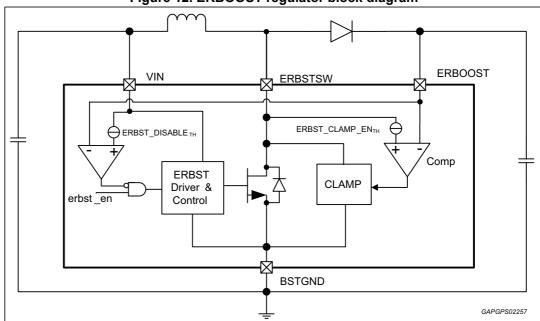


Figure 12. ERBOOST regulator block diagram

Normal run time power for the system is provided directly from the battery input, not from the boost. Boost energy is available to the system through the energy reserve crossover switch once battery is lost or a commanded system shutdown is initiated.



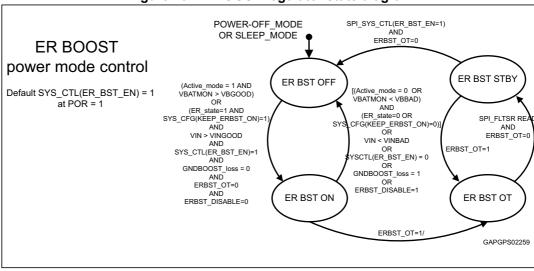


Figure 13. ERBOOST regulator state diagram

# 6.4 Energy reserve capacitor charging and discharging circuits

The energy reserve capacitor connected to VER pin can be charged in an efficient way by means of a current generator. Its capability is 65 mA nominal, so that for example a 10 mF capacitor can be charged in approximately 4 s to 24 V. The current generator is activated or deactivated by SPI command only while in ACTIVE mode. When not in ACTIVE mode, the generator is always switched off in order to decouple ERBOOST node voltage from VER reserve voltage.

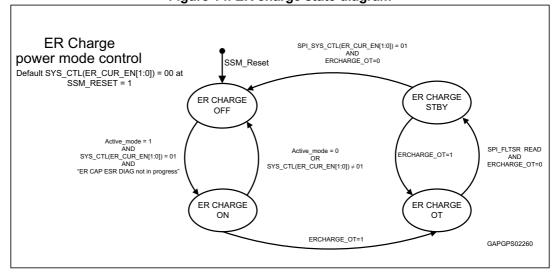


Figure 14. ER charge state diagram

L9680 also offers a safe control to discharge the ER capacitor by means of a fixed current generator. This discharge can be controlled via SPI command while not in SLEEP mode. Furthermore, this discharge circuit is mutually exclusive with the ER charging circuit, to avoid inefficient way of controlling the charge on the VER energy reserve capacitor.



DS11615 Rev 2 41/280

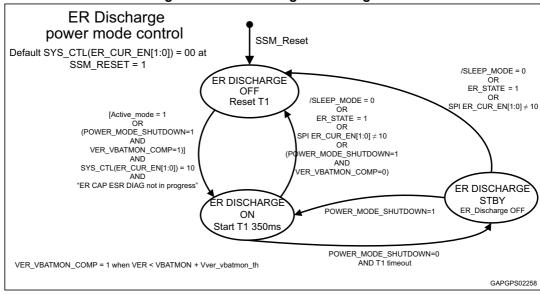


Figure 15. ER discharge state diagram

# 6.5 ER CAP diagnostic

The L9680 IC contains a full integrated solution to check the connection, value and series resistance of energy reserve capacitor independent from ER Cap leakage current and Boost Voltage level.

#### 6.5.1 ER CAP measurement

The IC contains two current generators used to charge and discharge the energy reserve capacitor connected on ER pin. The simplified block diagram is shown in the figure below.

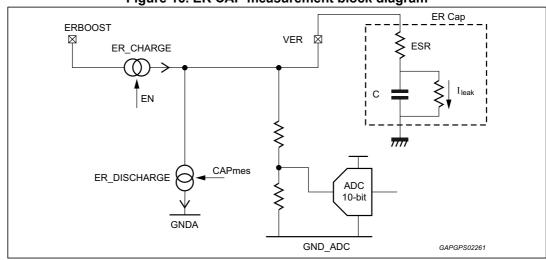


Figure 16. ER CAP measurement block diagram

To obtain an accurate ER CAP measurement, the VER voltage conversion must be required when both current generators are off, namely no current flows through ER cap permits to avoid ESR error contribution.

The user can decide the charge and discharge time based on the ER CAP used in application, in order to maximize the differential voltage and then improve the accuracy.

Anyway, a timeout on ER Discharge current has been implemented to prevent thermal issue, so the discharge time cannot be longer than 350 ms.

VER (t)

ESR > 0

V<sub>start</sub>

V<sub>end</sub>

V<sub>stop</sub>

ER\_CHARGE

ER\_DISCHARGE

T1

T2

GAPGPS02262

Figure 17. ER CAP measurement timing diagram

The following formulas can be used to retrieve the ER CAP value from the voltage and timing measurements.

$$\Delta V_1 + \Delta V_2 = \frac{I_1 + I_{LEAK}}{C} T_1 + \frac{I_2 - I_{LEAK}}{C} T_2$$

$$C = \frac{2 \cdot I \cdot T}{V_{start} + V_{end} - 2 \cdot V_{stop}}$$

T<sub>1</sub> = discharge time

 $T_2$  = charge time, same as discharge time

$$T_1 = T_2 = T$$

$$\Delta V_1 = V_{start} - V_{stop}$$

$$\Delta V_2 = V_{end} - V_{stop}$$

I<sub>1</sub> = discharge current

I<sub>2</sub> = charge current, same as discharge current

$$I_1 = I_2 = I$$

I<sub>LEAK</sub> = leakage current

#### 6.5.2 **ER CAP ESR measurement**

The IC contains the capability to perform a measurement of the equivalent series resistance of energy reserve capacitor. In this case the discharge current is 10 times higher to create a voltage difference proportional to the ER CAP ESR. The voltage measurement and conversion is automatically executed once the user requires the ESR measurement through the LPDIAGREQ register.

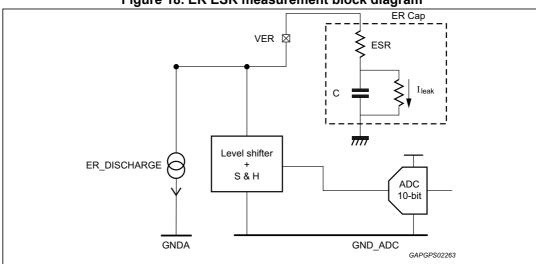


Figure 18. ER ESR measurement block diagram

Upon an ESR measurement is requested, the IC executes an internal automatic sequence to take three voltage measurements at the ER node, toggling the ER discharge current source on and off as shown in *Figure 19*. The test lasts for T<sub>ESR DIAG</sub>. After this time has elapsed, the results can be retrieved by reading the DIAGCTRL\_x registers. The three ER voltage measurements are provided at the same time in DIAGCTRLA, DIAGCTRLB and DIAGCTRLC registers. During the execution of the ESR measurement no other activity on ADC is allowed. The user must ensure no other ADC requests are queued to be executed at the same time of ESR measurement. The ESR diagnostic, once initiated, will continue without interruption even if the device enters in ER State because of a battery loss event.



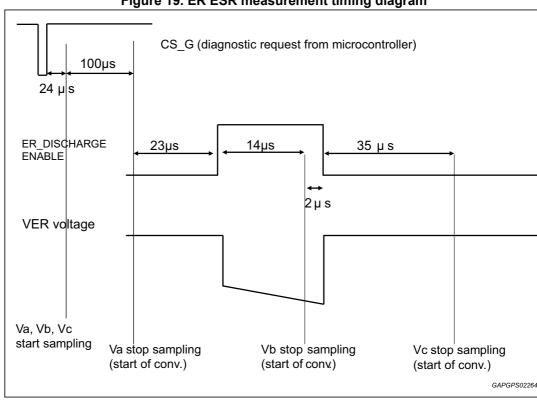


Figure 19. ER ESR measurement timing diagram

The ER CAP ESR can be calculated according to the following formula:

$$\mathsf{ESR}_{\mathsf{ERCAP}} = \frac{\mathsf{V_C} - \mathsf{V_B}}{\mathsf{G}_{\mathsf{ER\_ESR}} \cdot \mathsf{I}_{\mathsf{ER\_DISCHARGE\_HIGH}}} + \mathsf{OFF}_{\mathsf{ER\_ESR}}$$

#### 6.6 ER switch and COVRACT pin

L9680 allows the system to run out of the reserve capacitor energy stored on VER node by means of the charging boost regulator. In this way, an extended operation can take place even in case of battery lost. The ER switch implements a connection from the VER pin to the VIN node, supply input for the SYNCBOOST regulator and for internal power supplies.

The ER switch is automatically activated upon entering the PASSIVE mode. Voltage difference between VIN and VER is monitored in order to prevent VER back-feeding when VIN exceeds VER by V<sub>ER SW OV TH</sub>. The ER switch is automatically deactivated upon the above mentioned overvoltage detection.

During PASSIVE mode the discrete digital output pin COVRACT is activated to allow for external optional cross-over switch control (except during VINGOOD blanking state, where the COVRACT is deactivated).

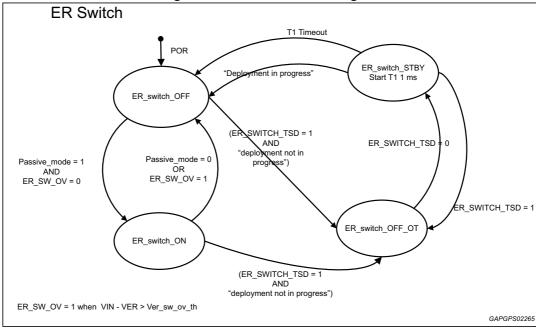


Figure 20. ER switch state diagram

# 6.7 SYNCBOOST boost regulator

The SYNCBOOST boost regulator also operates at 1.882 MHz allowing the user to select smaller less expensive external components. The regulator provides a 12 V/14.75 V nominal for the sync pulse feature used in PSI-5 bussed satellite sensor configuration. The regulator also provides the power for the SATBUCK regulator.

The SyncBoost switching regulator uses a classical peak current mode control loop to properly regulate the output voltage and includes an over-voltage protection that immediately switch off the PowerMOS to protect the device. The regulator includes also a soft start circuit which apply a ramp on the over current threshold from the 40% of  $I_{\text{OC\_SYNCBST}}$  value to the maximum one with 16 steps and within 1024  $\mu s$ . The soft start is restarted every time the regulator is enabled, namely there is a transition from the SYNCBOOST\_OFF state to the SYNCBOOST\_ON state.

In normal operation, the SYNCBOOST regulator operates directly from battery providing a voltage level to operate the sync pulse driver circuit. Should the input voltage be greater than regulation point, the output voltage will track the input voltage less any drops in the external components.

The boost regulator is enabled automatically by the power control state machine, but can be disabled on purpose via SPI command through the SYS\_CTL(SYNCBST\_EN) bit. The regulation point is fixed at a nominal 12 V at startup. User may increase the output regulation voltage to 14.75 V nominal by setting the SATV bit via a dedicated SPI command, should an extended voltage range be needed.

Boost converter diagnostics include over voltage and under voltage, reported by the S\_BST\_NOK bit in the POWER\_STATE register, and the circuit is fully protected against shorts. The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag ERBST\_OT in the FLTSR register is read.



In case of loss of ground the FET is not turned on. Loss of ground can be detected also when the FET is off thanks to a pull-up current present on the BSTGND pin. The FET will be automatically reactivated as soon as ground connection is restored. Over-voltage protection from load dump and inductive flyback is provided via an active clamp and a SYNC\_Boost disable circuitry, see Figure 21.

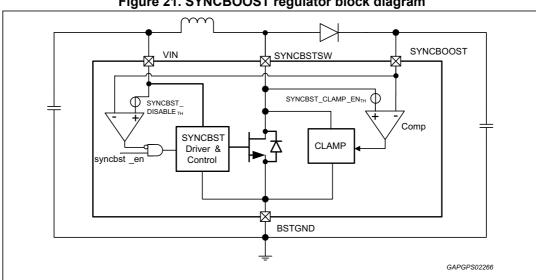
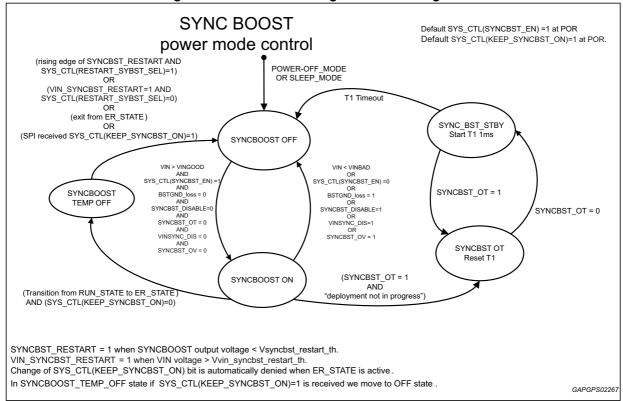


Figure 21. SYNCBOOST regulator block diagram





#### 6.8 SATBUCK regulator

The SATBUCK regulator provides a nominal 7.2 V regulated output voltage at startup for the remote satellite and wheel speed interface circuitry and the VCC buck regulator. The buck regulator is enabled automatically by the power control state machine. This regulator is protected against short circuits. Should the user need a higher voltage range for the remote sensor interface, a specific SPI command allows the output voltage to be increased at 9 V nominal by setting the SAT\_V bit. Fault status is available through SPI in the Fault Status Register (FLTSR). The buck converter operates at 1.882 MHz allowing the user to select smaller less expensive external components. Moreover, the synchronous buck regulator integrates the external recirculation diode.

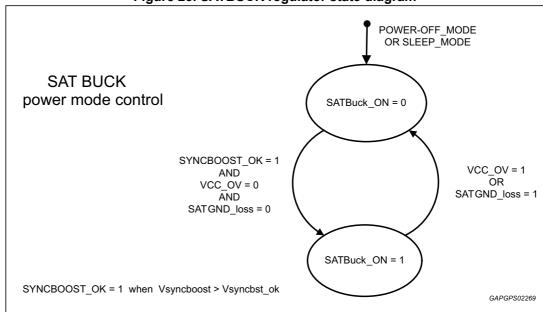


Figure 23. SATBUCK regulator state diagram

#### 6.9 VCC buck regulator

The VCC buck regulator also operates at 1.882 MHz and is user selectable to either 3.3 V or 5 V nominal output voltage. The user can select the output voltage through the VCCSEL pin. To select 5 V operation, the user must bias VCCSEL to a level higher than V<sub>TH2</sub> H V<sub>CCSEL</sub> for instance SyncBoost. For 3.3 V operation, the VCCSEL pin must be biased to a level lower than V<sub>TH2 L VCCSEL</sub>. An internal weak pull down is connected to VCCSEL to ensure the input remains at ground potential in case of open pin. The internal power control state machine will read the VCCSEL input pin and latch the resulting state upon the SATBUCK voltage reaches the good value (SATBUCK\_OK = 1). Upon latching the VCCSEL state, the VCC buck regulator cannot be changed by the user.

The VCC regulator has over and under voltage detections and shutdown capability and it is also protected against short circuits. During start-up an internal pull up current is enabled in order to detect a potential VCC pin open fault trough the over voltage detection. This pull up current is disabled once in VCC\_ON or VCC\_SHUTDOWN states. During normal operation, VCC\_ON state, the VCC pin open fault is quickly detected through the Under Voltage Detection Low to prevent any MCU damage.



An open VCC pin shall lead to an under voltage condition on VCC supply monitor. The SPI related signals (SCLK, MISO, MOSI, CS) or other digital nets shall not power the VCC pin due to back-feeding paths.

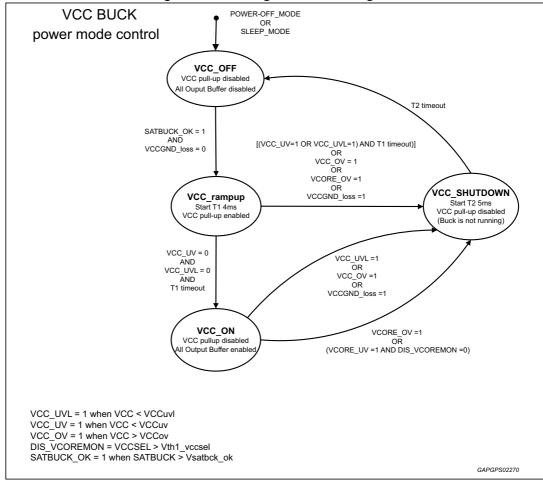


Figure 24. VCC regulator state diagram



### 6.10 VCOREMON external core voltage monitor

The device includes the possibility to monitor the external core voltage of MCU in case an additional external regulator is used to provide the 1.2V rail. The internal power control state machine will read the VCCSEL input pin and latch the resulting state upon the VCCBUCK regulator enters in the VCC\_ON state: if VCCSEL is lower than V<sub>TH1\_L\_VCCSEL</sub> the VCORE monitor will be enabled, otherwise, if VCCSEL is higher than V<sub>TH1\_H\_VCCSEL</sub>, the VCORE monitor will be disabled.

#### In summary:

- VCCSEL < V<sub>TH1</sub> L\_VCCSEL (VCCSEL shorted to ground), to select VCC = 3.3 V and to enable the VCORE monitor
- V<sub>TH1</sub> <sub>VCCSEL</sub> < VCCSEL < V<sub>TH2</sub> <sub>L</sub> <sub>VCCSEL</sub> (VCCSEL shorted to VCC), to select VCC = 3.3 V and to disable the VCORE monitor.
- VCCSEL > V<sub>TH2\_H\_VCCSEL</sub> (VCCSEL shorted to SYNCBOOST), to select VCC = 5 V and to disable the VCORE monitor.

The VCORE monitor is enabled once the VCC regulator is in VCC\_ON state, therefore the external MCU core voltage regulator (1.2 V) must reach the regulation within 4ms after the VCC regulator power-up.

Upon latching the VCCSEL state, the VCOREMON activation cannot be changed by the user

In case of VCCSEL open pin, an internal pull down current would force VCCSEL to ground and then the VCORE monitor will be enabled function.

If the VCORE voltage is low and the VCCSEL pin is higher than  $V_{TH1\_L\_VCCSEL}$ , after the 4ms delay from power-up, a latched VCOREMON fault will cause RESET to drive low, even though VCCSEL pin is high enough to satisfy the disabling of VCOREMON function. This occurs only once at power-up, and is then appropriately disabled. For this reason the RESET is released 500  $\mu s$  (namely the reset\_hold\_time) after the 4 ms delay from power-up as showed in *Figure 6*.



### 6.11 VSF regulator and control

The L9680 provides a low current linear regulator that can be used in the system design to bias the external high side safing switch. The regulator output is 20 V nominal (configurable to 25 V via SPI command). VSF is enabled if any of the ARMxINT signal is asserted, as shown in *Figure 25*. The VSF regulator supply input is ERBOOST.

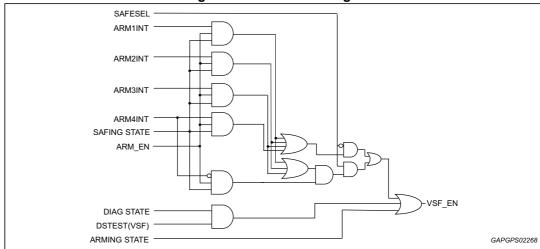


Figure 25. VSF control logic

VSF voltage can be monitored by the user through the internal ADC. Characteristics for this function are shown in the electrical performance tables.

#### 6.12 Oscillators

The device integrates two trimmed oscillators, both of them with spread spectrum capability selectable via the CLK\_CNF register.

The main oscillator runs at 16 MHz typ and is used to provide clock to the internal synchronous logic. Moreover, this frequency is divided down by factor 8.5 to generate clocks for the switching regulators (1.882 MHz typ).

The auxiliary oscillator runs at 7.5 MHz typ and is used to monitor the main oscillator. In case the main oscillator frequency was lower than  $f_{OSC\_LOW\_TH}$  threshold or higher than  $f_{OSC\_HIGH\_TH}$  threshold, the condition is detected by the frequency monitor circuit and then latched into the CLKFRERR flag in the FLTSR register and a POR is issued.

#### 6.13 Reset control

The device provides reset logic to safely control system operation in the event of internal ECU failures. Several internal reset signals are generated depending on the type of failure detected. In *Figure 26* the voltage monitoring diagram is shown.

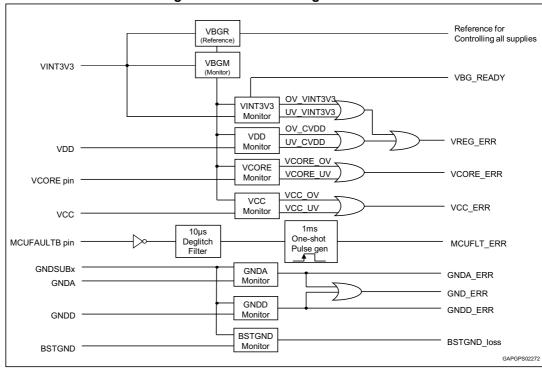


Figure 26. Internal voltage monitors

An active low pin output (RESET pin) is driven from the L9680 to allow resetting of external devices such as the microcontroller, sensors, and other ICs within the ECU.

Three internal reset signals are generated by the device:

POR

Power On Reset - This reset is asserted when a failure is detected in the internal supplies or bandgap circuits. When active, all other resets are asserted.

WSM\_RESET

Watchdog State Machine Reset - This reset is generated when the POR is active or when a failure is detected in the VCC or VCORE supply.

SSM RESET

System State Machine Reset - This reset is asserted when the POR or the WSM\_RESET are active, or when a failure is detected in either Watchdog state machine, or again when the MCUFAULTB pin is active.

The RESET pin is the active-low signal driven on the output pin, and is an inverted form of SSM\_RESET.

The cause of the RESET activation is latched and reported into the Fault Status Register FLTSR and cleared upon SPI reading.

The reset generated by the MCUFLT\_ERR can be masked by the MCU\_FLT\_TEST test mode signal. This allows verification of MCUFLT pin operation and, in turn, microcontroller fault conditions without asserting a reset. The MCURST bit is still set whether in test mode or not.

The reset logic shall be controlled as shown in the diagram below:

47/

CLKFRERR GND\_ERR VBG\_READY SUPPLY\_POR VREG\_ERR VCC\_ERR -- WSM\_Reset VCORE\_ERR DIS\_VCOREMON Reset\_hold\_time MCUFLT\_ERR MCU\_SSMRST MCU\_FLT\_TM SSM\_Reset WD1 RESET state WD2 RESET state RESET (pin) WD2 STOPPING state WD2\_SSMRST WD2\_TM s MCURST -R SPI\_Read -GAPGPS02273

Figure 27. Reset control logic



SPI interfaces L9680

### 7 SPI interfaces

The L9680 system solution device has many user selectable features controlled through serial communications by the integrated microcontroller. The device features two SPI interfaces: one global SPI and one Remote Sensor SPI. The global SPI interface provides general configuration, control and status functions for the device, while the Remote Sensor SPI provides dedicated access to Remote Sensor Data and Status Registers.

# 7.1 SPI protocol

Each SPI interface (Global and Remote Sensor) use their own dedicated set of 4 I/O pins: CS\_G, SCLK\_G, MOSI\_G and MISO\_G for Global SPI; CS\_RS, SCLK\_RS, MOSI\_RS and MISO\_RS for Remote Sensor SPI. Both the SPI interfaces use the same protocol described here below (the suffix '\_X' used in the SPI pin names below is intended to stand for either ' G' or ' RS' depending on the particular SPI interface considered)

The IC SPI interface is composed by an input shift register, an output shift register and four control signals. MOSI\_X is the data input to the input shift register. MISO\_X is the data output from the output shift register. SCLK\_X is the clock input used to shift data into the input shift register or out from the output one while CS X is the active low chip select input.

All SPI communications are executed in exact 32 bit increments. The general format of the 32 bit transmission for the SPI interface is shown in *Table 5*.

Data sent to the IC (i.e. MOSI\_X) consists of a target read register ID (RID), a target write register ID (WID), write data parity (WPAR) and 16 bits of data (WRITE). WRITE data is the data to be written to the target write register indicated by WID. Data returned from the IC (i.e. MISO\_X) consists of a global status word (GSW), read data parity (RPAR) and 20 bits of data (READ). READ data will be the contents of the target read register as indicated by the RID bits. The parity bits WPAR and RPAR cover all the 32 bits of the MOSI and MISO frames, respectively. Odd parity type is used.

Table 5. SPI MOSI and MISO frames layout

						S	PI reg	gister	R/W							
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI_MOSI	GID			F	RID[6:0	)]					,	WID[6:0]				WPAR
SPI_MISO					G	SW[10	):0]					RPAR		REAL	D[19:1	6]
	15	14	13	12	11	10	9	8	7	6	5	4	વ	2	1	0
SPI_MOSI	10	17	10	12	• • • • • • • • • • • • • • • • • • • •	10			ITE[15						'	
SPI_MISO								RE	AD[15	:0]						

The communications is controlled through CS\_X, enabling and disabling communication. When CS\_X is at logic high, all SPI communication I/O is tri-stated and no data is accepted. When CS\_X is low, data is latched on the rising edge of SCLK\_X and data is shifted on the falling edge. The MOSI\_X pin receives serial data from the master with MSB first. Likewise for MISO X, data is read MSB first, LSB last.

The L9680 contains a data validation method through the SCLK\_X input to keep transmissions with not exactly 32 bits from being written to the device. The SCLK\_X input counts the number of received clocks and should the clock counter exceed or count fewer



L9680 SPI interfaces

than 32 clocks, the received message is discarded and a SPI\_FLT bit is flagged in the Global Status Word (GSW). The SPI\_FLT bit is also set in case of parity error detected on the MOSI\_X frame. Any attempt to access to a register with forbidden access mode (read or write) is not leading to changes to the internal registers but the SPI\_FLT bit is not set in this case.

## 7.2 Global SPI register map

The Global SPI interface consists of several 32-bit registers to allow for configuration, control and status of the IC as well as special manufacturing test modes. The register definition is defined by the read register ID (RID) and the write register ID (WID) as shown in *Table 6.* Global ID bit (GID) is used to extend available register addresses, but it is shared between RID and WID; only RID and WID with the same GID value can be addressed within the same SPI word. The operating states here show in which states the SPI command is processed.

The L9680 checks the validity of the received WID and RID fields in the MOSI\_G frame. Should a SPI write command with WID matching a writable register be received in an illegal operating state, the command will be discarded and the ERR\_WID bit will be flagged in the next Global Status Word GSW. The ERR\_WID flag is not set in case WID is addressing a read/only register. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR\_RID bit will be flagged in the current GSW.

DS11615 Rev 2 55/280

able	<i>.</i> 0.				<u> </u>				er ma				On	erating S	etato(1)	
GID			RIC	) / V	VID	)		Hex	R/W	Name	Description	Init	1	Ssafing	1	Arming
0	0	0	0	0	0	0	0	\$00	R	FLTSR	Global fault status register					
0	0	0	0	0	0	0	1	\$01	R/W	SYS_CFG	Power supply configuration <sup>(2)</sup>	Х	Х	Х	Х	Х
0	0	0	0	0	0	1	0	\$02	R/W	SYS_CTL	Register for power management	Х	Х	Х	Х	Х
0	0	0	0	0	0	1	1	\$03	W	SPI_SLEEP	Sleep Mode command	Х	Х	Х	Х	Х
0	0	0	0	0	1	0	0	\$04	R	SYS_STATE	Read register to report in which state the power control state machine is and also in which operating state the device is					
0	0	0	0	0	1	0	1	\$05	R	POWER_STATE	Power state register (feedback on regulators' status and voltage thresholds)					
0	0	0	0	0	1	1	0	\$06	R/W	DCR_0			Х	Х	Х	Х
0	0	0	0	0	1	1	1	\$07	R/W	DCR_1			Х	Х	Х	Х
0	0	0	0	1	0	0	0	\$08	R/W	DCR_2			Х	Х	Х	Х
0	0	0	0	1	0	0	1	\$09	R/W	DCR_3			Х	Х	Х	Х
0	0	0	0	1	0	1	0	\$0A	R/W	DCR_4			Х	Х	Х	Х
0	0	0	0	1	0	1	1	\$0B	R/W	DCR_5	Deployment configuration register		Х	Х	Х	Х
0	0	0	0	1	1	0	0	\$0C	R/W	DCR_6	Deployment configuration register		Х	Х	Х	Х
0	0	0	0	1	1	0	1	\$0D	R/W	DCR_7			Х	Х	Х	Х
0	0	0	0	1	1	1	0	\$0E	R/W	DCR_8			Х	Х	Х	Х
0	0	0	0	1	1	1	1	\$0F	R/W	DCR_9			Х	Х	Х	Х
0	0	0	1	0	0	0	0	\$10	R/W	DCR_A			Х	Х	Х	Х
0	0	0	1	0	0	0	1	\$11	R/W	DCR_B			Х	Х	Х	Х
0	0	0	1	0	0	1	0	\$12	R/W	DEPCOM	Deployment command register			Х		Х
0	0	0	1	0	0	1	1	\$13	R	DSR_0						
0	0	0	1	0	1	0	0	\$14	R	DSR_1	Deployment status register					
0	0	0	1	0	1	0	1	\$15	R	DSR_2						



Table 6. Global SPI register map (continued)

CID			DIE		MID			Have	R/W	Nome	Description		Ор	erating S	State <sup>(1)</sup>	
GID			KIL	) / V	VID	,		нех	K/W	Name	Description	Init	Diag	Ssafing	Scrap	Arming
0	0	0	1	0	1	1	0	\$16	R	DSR_3						
0	0	0	1	0	1	1	1	\$17	R	DSR_4						
0	0	0	1	1	0	0	0	\$18	R	DSR_5						
0	0	0	1	1	0	0	1	\$19	R	DSR_6						
0	0	0	1	1	0	1	0	\$1A	R	DSR_7	Deployment status register					
0	0	0	1	1	0	1	1	\$1B	R	DSR_8						
0	0	0	1	1	1	0	0	\$1C	R	DSR_9						
0	0	0	1	1	1	0	1	\$1D	R	DSR_A						
0	0	0	1	1	1	1	0	\$1E	R	DSR_B						
0	0	0	1	1	1	1	1	\$1F	R	DCMTS01						
0	0	1	0	0	0	0	0	\$20	R	DCMTS23						
0	0	1	0	0	0	0	1	\$21	R	DCMTS45	Deployment current monitor register					
0	0	1	0	0	0	1	0	\$22	R	DCMTS67	Deployment current monitor register					
0	0	1	0	0	0	1	1	\$23	R	DCMTS89						
0	0	1	0	0	1	0	0	\$24	R	DCMTSAB						
0	0	1	0	0	1	0	1	\$25	R/W	SPIDEPEN	Lock/Unlock command			Х		Х
0	0	1	0	0	1	1	0	\$26	R	LP_GNDLOSS	Loss of ground fault for squib loops					
0	0	1	0	0	1	1	1	\$27	R	VERSION_ID	Device version					
0	0	1	0	1	0	0	0	\$28	R/W	WD_RETRY_CONF	Watchdog Retry Configuration	Х				
0	0	1	0	1	0	0	1	\$29	W	MCU_FLT_TEST	Microcontroller Fault test	Х	Х	Х	Х	Х
0	0	1	0	1	0	1	0	\$2A	R/W	WDTCR	Watchdog first level configuration	Х				
0	0	1	0	1	0	1	1	\$2B	R/W	WD1T	Watchdog first level key transmission	Х	Х	Х	Х	Х
0	0	1	0	1	1	0	0	\$2C	R	WD_STATE	Watchdog first and second level state					
0	0	1	0	1	1	0	1	\$2D	R/W	CLK_CONF	Clock configuration	Х	Х	Х	Х	Х
0	0	1	0	1	1	1	0	\$2E	R	SCRAP_SEED	Scrap Seed command					

L9680

Name   Description   First   Diag   Stafing   Stafing							(continued)	er map	egiste	Pl re	SF	oal	ilok	G		le 6	Tab
Init   Diag   Ssafing   S	ə <sup>(1)</sup>	state <sup>(1)</sup>	erating S	Ор		D	Mana a	DAA				·//D	. , ,				OIF.
0         0         1         1         0         0         0         9         330         W         SCRAP_STATE         Scrap State command         X           0         0         1         1         0         0         1         331         W         SAFING_STATE         Safing State command         X         X           0         0         1         1         0         0         1         0         332         W         WD2_RECOVER         Watchdog second level recovery command         X         X         X           0         0         1         1         0         0         1         1         0         0         1         1         0         0         332         W         WD2_RECOVER         Watchdog second level recovery command         X         X         X           0         0         1         1         0         0         334         W         WD2_RECOVER         Watchdog second level recovery command         X         X         X         X           0         0         1         1         0         0         334         W         WD2_RECOVER         Watchdog second level seed transmission         X         X         <	rap Arming	Scrap	Ssafing	Diag	Init	Description	Name	R/W	нех		)	VID	) / V	KIL			GIL
0         0         1         1         0         0         0         1         \$31         W         SAFING_STATE         Safing State command         X         X           0         0         1         1         0         0         1         0         \$32         W         WD2_SEED         Watchdog second level seed transmission         X         X         X           0         0         1         1         0         0         1         1         \$33         R         WD2_SEED         Watchdog second level seed transmission         X         X         X           0         0         1         1         0         1         1         0         1         1         333         R         WD2_SEED         Watchdog second level seed transmission         X	х х	Х				Scrap Key command	SCRAP_KEY	W	\$2F	1	1	1	1	0	1	0	0
0         0         1         1         0         0         1         0         \$32         W         WD2_RECOVER         Watchdog second level recovery command         X         X         X           0         0         1         1         0         0         1         1         \$33         R         WD2_SEED         Watchdog second level seed transmission         X				Х		Scrap State command	SCRAP_STATE	W	\$30	0	0	0	0	1	1	0	0
0         0         1         1         0         0         1         1         \$33\$         R         WD2_SEED         Watchdog second level seed transmission         X <td< td=""><td></td><td></td><td></td><td>Х</td><td></td><td>Safing State command</td><td>SAFING_STATE</td><td>W</td><td>\$31</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></td<>				Х		Safing State command	SAFING_STATE	W	\$31	1	0	0	0	1	1	0	0
0         0         1         1         0         1         0         0         \$34         W         WD2_KEY         Watchdog second level key transmission         X         X         X           0         0         1         1         0         1         \$35         W         WD_TEST         Watchdog first and second level test         X         <	х х	Х	Х	Х	Х	Watchdog second level recovery command	WD2_RECOVER	W	\$32	0	1	0	0	1	1	0	0
0         0         1         1         0         1         \$35\$         W         WD_TEST         Watchdog first and second level test         X         X         X           0         0         1         1         0         1         1         0         \$36\$         R/W         SYSDIAGREQ         Diagnostic command for system safing         X						Watchdog second level seed transmission	WD2_SEED	R	\$33	1	1	0	0	1	1	0	0
0         0         1         1         0         \$36         R/W         SYSDIAGREQ         Diagnostic command for system safing         X           0         0         1         1         0         1         1         1         \$37         R         LPDIAGSTAT         Diagnostic result register for deployment loops         X         X           0         0         1         1         1         0         0         \$38         R/W         LPDIAGREQ         Diagnostic configuration command for deployment loops         X         X         X           0         0         1         1         1         0         0         \$38         R/W         LPDIAGREQ         Diagnostic configuration command for deployment loops         X         X         X           0         0         1         1         1         0         0         \$38         R/W         SWCTRL         DC sensor diagnostic configuration command for deployment loops         X         X         X           0         0         1         1         1         0         \$34         R/W         DIAGCTRL_A         In WID is AtoD converter control register A. In RID is AtoD result B. In WID is AtoD converter control register D. In RID is AtoD result C request.         X         X<	х х	Х	Х	Х	Х	Watchdog second level key transmission	WD2_KEY	W	\$34	0	0	1	0	1	1	0	0
0         0         1         1         0         1	х х	Х	Х	Х	Х	Watchdog first and second level test	WD_TEST	W	\$35	1	0	1	0	1	1	0	0
0         0         1         1         0         1				Х		Diagnostic command for system safing	SYSDIAGREQ	R/W	\$36	0	1	1	0	1	1	0	0
0         0         1         1         1         0         0         \$38 k/W         LPDIAGREQ         deployment loops         X         X           0         0         1         1         1         0         0         1         \$39 k/W         SWCTRL         DC sensor diagnostic configuration         X         X         X           0         0         1         1         1         0         1         0         1         0         1         0         1         0         0         1         0         0         1         0         0         1         0						, ,	LPDIAGSTAT	R	\$37	1	1	1	0	1	1	0	0
0         0         1         1         1         0         1         0         1         1         0         1         1         0         1         1         0         1         1         0         1         1         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0	х х	х	Х	х			LPDIAGREQ	R/W	\$38	0	0	0	1	1	1	0	0
0         0         1         1         1         0         1         0         1         1         0         1         1         0         1         1         0         1         1         0         1         1         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         1         1         1         0         0         \$3C         R/W         DIAGCTRL_B         In WID is AtoD converter control register C. In RID is AtoD result C request.         X         X         X           0         0         1         1         1         0         0         \$3C         R/W         DIAGCTRL_C         In WID is AtoD converter control register C. In RID is AtoD result D request.         X         X         X	х х	Х	Х	Х		DC sensor diagnostic configuration	SWCTRL	R/W	\$39	1	0	0	1	1	1	0	0
0         0         1         1         1         1         1         1         33B         R/W         DIAGCTRL_B         RID is AtoD result B request.         X         X         X           0         0         1         1         1         1         0         0         \$3C         R/W         DIAGCTRL_C         In WID is AtoD converter control register C. In RID is AtoD converter control register D. In RID is AtoD converter control register D. In RID is AtoD result D request.         X         X         X	х х	х	Х	х			DIAGCTRL_A	R/W	\$3A	0	1	0	1	1	1	0	0
0         0         1         1         1         1         0         0         \$3C R/W         DIAGCTRL_C         RID is AtoD result C request.         X         X           0         0         1 <td>х х</td> <td>х</td> <td>Х</td> <td>х</td> <td></td> <td></td> <td>DIAGCTRL_B</td> <td>R/W</td> <td>\$3B</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td>	х х	х	Х	х			DIAGCTRL_B	R/W	\$3B	1	1	0	1	1	1	0	0
RID is AtoD result D request.	х х	х	Х	х			DIAGCTRL_C	R/W	\$3C	0	0	1	1	1	1	0	0
0 0 4 4 4 4 0 000	х х	х	Х	х			DIAGCTRL_D	R/W	\$3D	1	0	1	1	1	1	0	0
0   0   1   1   1   1   0   \$3E									\$3E	0	1	1	1	1	1	0	0
0 0 1 1 1 1 1 1 \$3F R/W SW_REGS_CONF Configuration register for switching regulators X X	х х	Х	Х	Х		Configuration register for switching regulators	SW_REGS_CONF	R/W	\$3F	1	1	1	1	1	1	0	0
0 1 0 0 0 0 0 \$40									\$40	0	0	0	0	0	0	1	0
0 1 0 0 0 0 1 \$41									\$41	1	0	0	0	0	0	1	0
0 1 0 0 0 1 0 \$42 R/W GPOCR General Purpose Output configuration X X				Х	Х	General Purpose Output configuration	GPOCR	R/W	\$42	0	1	0	0	0	0	1	0
0 1 0 0 0 0 1 1 \$43 R/W GPOCTRL0 General Purpose Output 0 control register X X X	х х	Х	Х	Х	Х	General Purpose Output 0 control register	GPOCTRL0	R/W	\$43	1	1	0	0	0	0	1	0





Table	<del>)</del> 6.	Global SPI re	egiste	er ma	р	(continued)

CID			DIE	. / \	A/ID			Have	DAM	News	Description		Ор	erating S	tate <sup>(1)</sup>	
GID			KIL	) / V	VID	,		нех	R/W	Name	Description	Init	Diag	Ssafing	Scrap	Arming
0	1	0	0	0	1	0	0	\$44	R/W	GPOCTRL1	General Purpose Output 1 control register	Х	Х	Х	Х	Х
0	1	0	0	0	1	0	1	\$45	R/W	GPOCTRL2	General Purpose Output 2 control register	Х	Х	Х	Х	Х
0	1	0	0	0	1	1	0	\$46	R	GPOFLTSR	General Purpose Output fault status register					
0	1	0	0	0	1	1	1	\$47								
0	1	0	0	1	0	0	0	\$48	R/W	WSS_TEST	WSS testmode request		Х			
0	1	0	0	1	0	0	1	\$49								
0	1	0	0	1	0	1	0	\$4A	R/W	RSCR0	PSI5/WSS configuration register		Х			
0	1	0	0	1	0	1	1	\$4B	R/W	RSCR1			Х			
0	1	0	0	1	1	0	0	\$4C	R/W	RSCR2			Х			
0	1	0	0	1	1	0	1	\$4D	R/W	RSCR3			Х			
0	1	0	0	1	1	1	0	\$4E	R/W	RSCTRL	Remote sensor control register		Х	Х	Х	Х
0	1	0	0	1	1	1	1	\$4F								
0	1	0	1	0	0	0	0	\$50								
0	1	0	1	0	0	0	1	\$51								
0	1	0	1	0	0	1	0	\$52								
0	1	0	1	0	0	1	1	\$53								
0	1	0	1	0	1	0	0	\$54								
0	1	0	1	0	1	0	1	\$55								
0	1	0	1	0	1	1	0	\$56								
0	1	0	1	0	1	1	1	\$57								
0	1	0	1	1	0	0	0	\$58								
0	1	0	1	1	0	0	1	\$59								
0	1	0	1	1	0	1	0	\$5A								
0	1	0	1	1	0	1	1	\$5B								
0	1	0	1	1	1	0	0	\$5C								

SPI interfaces

CID			DIE	. / \/	V/ID			Have	DAM	Nama	Decembrish		Ор	erating S	state <sup>(1)</sup>	
GID			KIL	) / V	VIL	,		нех	R/W	Name	Description	Init	Diag	Ssafing	Scrap	Arming
0	1	0	1	1	1	0	1	\$5D								
0	1	0	1	1	1	1	0	\$5E								
0	1	0	1	1	1	1	1	\$5F								
0	1	1	0	0	0	0	0	\$60								
0	1	1	0	0	0	0	1	\$61								
0	1	1	0	0	0	1	0	\$62								
0	1	1	0	0	0	1	1	\$63								
0	1	1	0	0	1	0	0	\$64	R/W	RS_AUX_CONF1	WSS Threshold configuration register 1		Х			
0	1	1	0	0	1	0	1	\$65	R/W	RS_AUX_CONF2	WSS Threshold configuration register 2		Х			
0	1	1	0	0	1	1	0	\$66	R/W	SAF_ALGO_CONF	Safing Algorithm configuration register		Х			
0	1	1	0	0	1	1	1	\$67								
0	1	1	0	1	0	0	0	\$68								
0	1	1	0	1	0	0	1	\$69								
0	1	1	0	1	0	1	0	\$6A	R	ARM_STATE	Status of arming signals					
0	1	1	0	1	0	1	1	\$6B								
0	1	1	0	1	1	0	0	\$6C								
0	1	1	0	1	1	0	1	\$6D								
0	1	1	0	1	1	1	0	\$6E	R/W	LOOP_MATRIX_ARM1	Assignment of ARM 1 pin to which LOOPS		Х			
0	1	1	0	1	1	1	1	\$6F	R/W	LOOP_MATRIX_ARM2	Assignment of ARM 2 pin to which LOOPS		Х			
0	1	1	1	0	0	0	0	\$70	R/W	LOOP_MATRIX_ARM3	Assignment of ARM 3 pin to which LOOPS		Х			
0	1	1	1	0	0	0	1	\$71	R/W	LOOP_MATRIX_ARM4	Assignment of ARM 4 pin to which LOOPS		Х			
0	1	1	1	0	0	1	0	\$72								
0	1	1	1	0	0	1	1	\$73	R	AEPSTS_ARM1						
0	1	1	1	0	1	0	0	\$74	R	AEPSTS_ARM2	Arming pulse stretch timer value					
0	1	1	1	0	1	0	1	\$75	R	AEPSTS_ARM3						





Table 6. Global SPI register map (continued)

GID			DIF	) / V	WID.			Цах	R/W	Nome	Description		Ор	erating S	tate <sup>(1)</sup>	
GID			KIL	<i>)  </i> V	VID	,		пех	FC/ VV	Name	Description	Init	Diag	Ssafing	Scrap	Arming
0	1	1	1	0	1	1	0	\$76	R	AEPSTS_ARM4	Arming pulse stretch timer value					
0	1	1	1	0	1	1	1	\$77								
0	1	1	1	1	0	0	0	\$78	R/W	PADTHRESH_HI	Passenger Inhibit Thresholds		Х			
0	1	1	1	1	0	0	1	\$79	R/W	PADTHRESH_LO	rassenger minibit miesnolds		Х			
0	1	1	1	1	0	1	0	\$7A	R/W	LOOP_MATRIX_PSINH	Assignment of PSINH signal to which LOOPS		Х			
0	1	1	1	1	0	1	1	\$7B								
0	1	1	1	1	1	0	0	\$7C								
0	1	1	1	1	1	0	1	\$7D								
0	1	1	1	1	1	1	0	\$7E								
0	1	1	1	1	1	1	1	\$7F	R/W	SAF_ENABLE	Safing record enable		Х	Х	Х	Х
1	0	0	0	0	0	0	0	\$80	R/W	SAF_REQ_MASK_1			Х			
1	0	0	0	0	0	0	1	\$81	R/W	SAF_REQ_MASK_2			Х			
1	0	0	0	0	0	1	0	\$82	R/W	SAF_REQ_MASK_3			Х			
1	0	0	0	0	0	1	1	\$83	R/W	SAF_REQ_MASK_4			Х			
1	0	0	0	0	1	0	0	\$84	R/W	SAF_REQ_MASK_5			Х			
1	0	0	0	0	1	0	1	\$85	R/W	SAF_REQ_MASK_6			Х			
1	0	0	0	0	1	1	0	\$86	R/W	SAF_REQ_MASK_7	Coffine record was a section of		Х			
1	0	0	0	0	1	1	1	\$87	R/W	SAF_REQ_MASK_8	Safing record request mask		Х			
1	0	0	0	1	0	0	0	\$88	R/W	SAF_REQ_MASK_9			Х			
1	0	0	0	1	0	0	1	\$89	R/W	SAF_REQ_MASK_10			Х			
1	0	0	0	1	0	1	0	\$8A	R/W	SAF_REQ_MASK_11			Х			
1	0	0	0	1	0	1	1	\$8B	R/W	SAF_REQ_MASK_12			Х			
1	0	0	0	1	1	0	0	\$8C	R/W	SAF_REQ_MASK_13			Х			
1	0	0	0	1	1	0	1	\$8D	R/W	SAF_REQ_MASK_14_pt1			Х			

SPI interfaces

Table 6. Global SPI register map (continued)

CID			DIE	. / \/	VID.			Have	DAM	Nome	Dog a sinting		Op	erating S	tate <sup>(1)</sup>	
GID			KIL	) / V	VID	,		нех	R/W	Name	Description —	Init C	Diag	Ssafing	Scrap	Arming
1	0	0	0	1	1	1	0	\$8E	R/W	SAF_REQ_MASK_14_pt2			Χ			
1	0	0	0	1	1	1	1	\$8F	R/W	SAF_REQ_MASK_15_pt1			Χ			
1	0	0	1	0	0	0	0	\$90	R/W	SAF_REQ_MASK_15_pt2	Safing record request mask		Χ			
1	0	0	1	0	0	0	1	\$91	R/W	SAF_REQ_MASK_16_pt1			Χ			
1	0	0	1	0	0	1	0	\$92	R/W	SAF_REQ_MASK_16_pt2			Χ			
1	0	0	1	0	0	1	1	\$93	R/W	SAF_REQ_TARGET_1			Χ			
1	0	0	1	0	1	0	0	\$94	R/W	SAF_REQ_TARGET_2			Χ			
1	0	0	1	0	1	0	1	\$95	R/W	SAF_REQ_TARGET_3			Χ			
1	0	0	1	0	1	1	0	\$96	R/W	SAF_REQ_TARGET_4			Χ			
1	0	0	1	0	1	1	1	\$97	R/W	SAF_REQ_TARGET_5			Χ			
1	0	0	1	1	0	0	0	\$98	R/W	SAF_REQ_TARGET_6			Χ			
1	0	0	1	1	0	0	1	\$99	R/W	SAF_REQ_TARGET_7			Χ			
1	0	0	1	1	0	1	0	\$9A	R/W	SAF_REQ_TARGET_8			Χ			
1	0	0	1	1	0	1	1	\$9B	R/W	SAF_REQ_TARGET_9			Χ			
1	0	0	1	1	1	0	0	\$9C	R/W	SAF_REQ_TARGET_10	Safing record request target		Χ			
1	0	0	1	1	1	0	1	\$9D	R/W	SAF_REQ_TARGET_11			Χ			
1	0	0	1	1	1	1	0	\$9E	R/W	SAF_REQ_TARGET_12			Χ			
1	0	0	1	1	1	1	1	\$9F	R/W	SAF_REQ_TARGET_13			Χ			
1	0	1	0	0	0	0	0	\$A0	R/W	SAF_REQ_TARGET_14_pt1			Χ			
1	0	1	0	0	0	0	1	\$A1	R/W	SAF_REQ_TARGET_14_pt2			Χ			
1	0	1	0	0	0	1	0	\$A2	R/W	SAF_REQ_TARGET_15_pt1			Х			
1	0	1	0	0	0	1	1	\$A3	R/W	SAF_REQ_TARGET_15_pt2			Х			
1	0	1	0	0	1	0	0	\$A4	R/W	SAF_REQ_TARGET_16_pt1			Χ			
1	0	1	0	0	1	0	1	\$A5	R/W	SAF_REQ_TARGET_16_pt2			Χ			
1	0	1	0	0	1	1	0	\$A6	R/W	SAF_RESP_MASK_1	Safing record response mask		Х			



GID			DIF	) / V	VID			Цах	R/W	Nome	Description		Ор	erating S	state <sup>(1)</sup>	
GID			KIL	<i>)  </i> V	VID	,		пех	FC/VV	Name	Description	Init	Diag	Ssafing	Scrap	Arming
1	0	1	0	0	1	1	1	\$A7	R/W	SAF_RESP_MASK_2			Х			
1	0	1	0	1	0	0	0	\$A8	R/W	SAF_RESP_MASK_3			Х			
1	0	1	0	1	0	0	1	\$A9	R/W	SAF_RESP_MASK_4			Х			
1	0	1	0	1	0	1	0	\$AA	R/W	SAF_RESP_MASK_5			Х			
1	0	1	0	1	0	1	1	\$AB	R/W	SAF_RESP_MASK_6			Х			
1	0	1	0	1	1	0	0	\$AC	R/W	SAF_RESP_MASK_7			Х			
1	0	1	0	1	1	0	1	\$AD	R/W	SAF_RESP_MASK_8			Х			
1	0	1	0	1	1	1	0	\$AE	R/W	SAF_RESP_MASK_9			Х			
1	0	1	0	1	1	1	1	\$AF	R/W	SAF_RESP_MASK_10	Safing record records many		Х			
1	0	1	1	0	0	0	0	\$B0	R/W	SAF_RESP_MASK_11	Safing record response mask		Х			
1	0	1	1	0	0	0	1	\$B1	R/W	SAF_RESP_MASK_12			Х			
1	0	1	1	0	0	1	0	\$B2	R/W	SAF_RESP_MASK_13			Х			
1	0	1	1	0	0	1	1	\$B3	R/W	SAF_RESP_MASK_14_pt1			Х			
1	0	1	1	0	1	0	0	\$B4	R/W	SAF_RESP_MASK_14_pt2			Х			
1	0	1	1	0	1	0	1	\$B5	R/W	SAF_RESP_MASK_15_pt1			Х			
1	0	1	1	0	1	1	0	\$B6	R/W	SAF_RESP_MASK_15_pt2			Х			
1	0	1	1	0	1	1	1	\$B7	R/W	SAF_RESP_MASK_16_pt1			Х			
1	0	1	1	1	0	0	0	\$B8	R/W	SAF_RESP_MASK_16_pt2			Х			
1	0	1	1	1	0	0	1	\$B9	R/W	SAF_RESP_TARGET_1			Х			
1	0	1	1	1	0	1	0	\$BA	R/W	SAF_RESP_TARGET_2			Х			
1	0	1	1	1	0	1	1	\$BB	R/W	SAF_RESP_TARGET_3			Х			
1	0	1	1	1	1	0	0	\$BC	R/W	SAF_RESP_TARGET_4	Safing record response target		Х			
1	0	1	1	1	1	0	1	\$BD	R/W	SAF_RESP_TARGET_5			Х			
1	0	1	1	1	1	1	0	\$BE	R/W	SAF_RESP_TARGET_6			Х			
1	0	1	1	1	1	1	1	\$BF	R/W	SAF_RESP_TARGET_7			Х			

CID				. / \/	A/ID			Have	DAM	Nama	Description		Ор	erating S	tate <sup>(1)</sup>	
GID			KIL	) / V	VID	,		нех	R/W	Name	Description	Init	Diag	Ssafing	Scrap	Arming
1	1	0	0	0	0	0	0	\$C0	R/W	SAF_RESP_TARGET_8			Х			
1	1	0	0	0	0	0	1	\$C1	R/W	SAF_RESP_TARGET_9			Х			
1	1	0	0	0	0	1	0	\$C2	R/W	SAF_RESP_TARGET_10			Х			
1	1	0	0	0	0	1	1	\$C3	R/W	SAF_RESP_TARGET_11			Х			
1	1	0	0	0	1	0	0	\$C4	R/W	SAF_RESP_TARGET_12			Х			
1	1	0	0	0	1	0	1	\$C5	R/W	SAF_RESP_TARGET_13	Safing record records target		Х			
1	1	0	0	0	1	1	0	\$C6	R/W	SAF_RESP_TARGET_14_pt1	Safing record response target		Х			
1	1	0	0	0	1	1	1	\$C7	R/W	SAF_RESP_TARGET_14_pt2			Х			
1	1	0	0	1	0	0	0	\$C8	R/W	SAF_RESP_TARGET_15_pt1			Х			
1	1	0	0	1	0	0	1	\$C9	R/W	SAF_RESP_TARGET_15_pt2			Х			
1	1	0	0	1	0	1	0	\$CA	R/W	SAF_RESP_TARGET_16_pt1			Х			
1	1	0	0	1	0	1	1	\$CB	R/W	SAF_RESP_TARGET_16_pt2			Х			
1	1	0	0	1	1	0	0	\$CC	R/W	SAF_DATA_MASK_1			Х			
1	1	0	0	1	1	0	1	\$CD	R/W	SAF_DATA_MASK_2			Х			
1	1	0	0	1	1	1	0	\$CE	R/W	SAF_DATA_MASK_3			Х			
1	1	0	0	1	1	1	1	\$CF	R/W	SAF_DATA_MASK_4			Х			
1	1	0	1	0	0	0	0	\$D0	R/W	SAF_DATA_MASK_5			Х			
1	1	0	1	0	0	0	1	\$D1	R/W	SAF_DATA_MASK_6			Х			
1	1	0	1	0	0	1	0	\$D2	R/W	SAF_DATA_MASK_7	Safing record data mask		Х			
1	1	0	1	0	0	1	1	\$D3	R/W	SAF_DATA_MASK_8			Х			
1	1	0	1	0	1	0	0	\$D4	R/W	SAF_DATA_MASK_9			Х			
1	1	0	1	0	1	0	1	\$D5	R/W	SAF_DATA_MASK_10			Х			
1	1	0	1	0	1	1	0	\$D6	R/W	SAF_DATA_MASK_11			Х			
1	1	0	1	0	1	1	1	\$D7	R/W	SAF_DATA_MASK_12			Х			
1	1	0	1	1	0	0	0	\$D8	R/W	SAF_DATA_MASK_13			Х			

SPI interfaces

L9680



Table 6. Global SPI register map (continued)
--

GID			DID	) / <b>V</b>	VID			Цах	R/W	Name	Description	Operating State <sup>(1)</sup>							
GID			KIL	, , <b>v</b>	VID			пех	FC/VV	Name	Description	Init	Diag	Ssafing	Scrap	Arming			
1	1	0	1	1	0	0	1	\$D9	R/W	SAF_DATA_MASK_14_pt1			Х						
1	1	0	1	1	0	1	0	\$DA	R/W	SAF_DATA_MASK_14_pt2			Х						
1	1	0	1	1	0	1	1	\$DB	R/W	SAF_DATA_MASK_15_pt1	Safing record data mask		Х						
1	1	0	1	1	1	0	0	\$DC	R/W	SAF_DATA_MASK_15_pt2	Saling record data mask		Х						
1	1	0	1	1	1	0	1	\$DD	R/W	SAF_DATA_MASK_16_pt1			Х						
1	1	0	1	1	1	1	0	\$DE	R/W	SAF_DATA_MASK_16_pt2			Х						
1	1	0	1	1	1	1	1	\$DF	R/W	SAF_THRESHOLD_1			Х						
1	1	1	0	0	0	0	0	\$E0	R/W	SAF_THRESHOLD_2			Х						
1	1	1	0	0	0	0	1	\$E1	R/W	SAF_THRESHOLD_3			Х						
1	1	1	0	0	0	1	0	\$E2	R/W	SAF_THRESHOLD_4			Х						
1	1	1	0	0	0	1	1	\$E3	R/W	SAF_THRESHOLD_5			Х						
1	1	1	0	0	1	0	0	\$E4	R/W	SAF_THRESHOLD_6			Х						
1	1	1	0	0	1	0	1	\$E5	R/W	SAF_THRESHOLD_7			Х						
1	1	1	0	0	1	1	0	\$E6	R/W	SAF_THRESHOLD_8	Safing record threshold		Х						
1	1	1	0	0	1	1	1	\$E7	R/W	SAF_THRESHOLD_9	- Saling record tilleshold		Х						
1	1	1	0	1	0	0	0	\$E8	R/W	SAF_THRESHOLD_10			Х						
1	1	1	0	1	0	0	1	\$E9	R/W	SAF_THRESHOLD_11			Х						
1	1	1	0	1	0	1	0	\$EA	R/W	SAF_THRESHOLD_12			Х						
1	1	1	0	1	0	1	1	\$EB	R/W	SAF_THRESHOLD_13			Х						
1	1	1	0	1	1	0	0	\$EC	R/W	SAF_THRESHOLD_14			Х						
1	1	1	0	1	1	0	1	\$ED	R/W	SAF_THRESHOLD_15			Х						
1	1	1	0	1	1	1	0	\$EE	R/W	SAF_THRESHOLD_16			Х						
1	1	1	0	1	1	1	1	\$EF	R/W	SAF_CONTROL_1			Х						
1	1	1	1	0	0	0	0	\$F0	R/W	SAF_CONTROL_2	Safing record control		Х						
1	1	1	1	0	0	0	1	\$F1	R/W	SAF_CONTROL_3			Х						



Table 6. Global SPI register map (continued)

GID			DIF	) / V	MID			Цах	R/W	Name	Dogovintion		Ор	erating S	state <sup>(1)</sup>	
GID			KIL	, , v	VID			пех	R/VV	Name	Description	Init	Diag	Ssafing	Scrap	Arming
1	1	1	1	0	0	1	0	\$F2	R/W	SAF_CONTROL_4			Х			
1	1	1	1	0	0	1	1	\$F3	R/W	SAF_CONTROL_5			Х			
1	1	1	1	0	1	0	0	\$F4	R/W	SAF_CONTROL_6			Х			
1	1	1	1	0	1	0	1	\$F5	R/W	SAF_CONTROL_7			Х			
1	1	1	1	0	1	1	0	\$F6	R/W	SAF_CONTROL_8			Х			
1	1	1	1	0	1	1	1	\$F7	R/W	SAF_CONTROL_9			Х			
1	1	1	1	1	0	0	0	\$F8	R/W	SAF_CONTROL_10	Safing record control		Х			
1	1	1	1	1	0	0	1	\$F9	R/W	SAF_CONTROL_11			Х			
1	1	1	1	1	0	1	0	\$FA	R/W	SAF_CONTROL_12			Х			
1	1	1	1	1	0	1	1	\$FB	R/W	SAF_CONTROL_13			Х			
1	1	1	1	1	1	0	0	\$FC	R/W	SAF_CONTROL_14			Х			
1	1	1	1	1	1	0	1	\$FD	R/W	SAF_CONTROL_15			Х			
1	1	1	1	1	1	1	0	\$FE	R/W	SAF_CONTROL_16			Х			
1	1	1	1	1	1	1	1	\$FF	R	SAF_CC	Safing Record Compare Complete					

<sup>1.</sup> A check mark indicates in which operating state a WRITE-command is valid.

DS11615 Rev 2

<sup>2.</sup> KEEP\_ERBOOST\_ON, LOW\_POWER\_MODE, VSF\_V and VINGOOD\_FILT\_SEL bits are writable in all states, the other bits of SYS\_CFG are only writable in INIT state.

L9680 SPI interfaces

#### 7.3 Global SPI tables

A summary of all the registers contained within the global SPI map are shown below and are referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field (the symbol '-' is used to indicate that the register is not affected by the relevant reset signal').

#### Global SPI global status word

The Global SPI of L9680 contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the Global SPI is the most significant 11 bits of MISO\_G data.

Table 7. Global SPI Global Status Word

MISO_G	GSW	Name	POR	WSM	SSM	Description
31	10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read  0 No fault 1 Fault
30	9	DEPOK	0	0	0	General Deployment Successful Flag, logical OR of the corresponding CHxDS bits (bit 15) in DSRx Registers  0 All the DSRx-CHDS bits are 0  1 At least one of the DSRx-CHDS bits is 1
29	8	0	0	0	0	Unused
28	7	WDT/TM_S	0	0	0	State of WDT/TM pin 0 WDT/TM=0 1 WDT/TM=1
27	6	ERSTATE	0	0	0	Set when Powermode state machine is in ER state 0 Powermode state machine is not in ER state 1 Powermode state machine is in ER state
26	5	POWERFLT	0	0	0	Fault present in Power State Register, logical OR between bits from 18 to 9 of POWER_STATE Register  0 All the bits from 18 to 9 in the POWER_STATE Registers are 0s  1 At least one of the bits from 18 to 9 in the POWER_STATE Registers is 1
25	4	FLT	1	1	1	Fault present in Fault Status Register (FLTSR), logical OR between all bits of FLTSR  0 All the bits in the Fault Status Register (FLTSR) are 0s  1 At least one of the bits in the Fault Status Register (FLTSR) is 1
24	3	CONVRDY2	0	0	0	ADC Conversion of request C or D has been completed so new results are available  0 No new data available  1 New data available
23	2	CONVRDY1	0	0	0	ADC Conversion of request A or B has been completed so new results are available  0 No new data available  1 New data available

SPI interfaces L9680

Table 7. Global SPI Global Status Word (continued)

MISO_G	GSW	Name	POR	WSM	SSM	Description
22	1	ERR_WID	0	0	0	Write address of previous SPI frame is not permitted in current operating phase  0 No Error  1 Error
21	0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care  0 No Error 1 Error

L9680 SPI interfaces

#### Global SPI read/write register

### 7.3.1 Fault status register (FLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	ERCHARGE_OT	MCUFLT_TEST	ERBST_OT	CLKFRERR	,	WD2 re	etry cn	t	OTPCRC_ERR	WD2_LO	WD2_TM	WD2_WDR	WD1_LO	WD1_TM	WD1_WDR	MCURST	WSMRST	SSMRST	VCORE_ERR	POR

**ID**: 00

Type: R

**Read:** 0000

Write: -

POR WSM SSM

ERCHARGE\_OT 0 - - ER charge over temperature bit

Set when over-temp condition detected, cleared on SPI read or POR=1

0 No Fault

1 Fault

MCUFLT\_TEST 1 1 1 MCU FAULT test mode - reflects MCU\_FLT\_TM signal state

0 MCU FLT TM=0

1 MCU FLT TM=1

ERBST\_OT 0 - - ER Boost over-temperature bit

Set when over-temp condition detected, cleared on SPI read or POR=1

0 No Fault

1 Fault

CLKFRERR 0 - - Internal oscillator cross-check error bit

Set when osc. error detected, cleared on SPI read or SUPPLY\_POR=1

0 No Fault

1 Fault

WD2\_retry\_cnt[3:0] \$0 \$0 Value of WD2 retry counter

OTPCRC ERR 0 - - OTP CRC error bit

Set when OTP error detected (tested at release of POR), cleared by POR=1

0 No Fault

1 Fault

WD2\_LO 0 0 - WD2 lockout - reflects WD2 lockout state

SPI interfaces L9680

				WD2 Lockout inactive     WD2 Lockout active
WD2_TM	0	0	0	WD2 test mode - reflects WD2TM signal state  0 WD2TM=0
				1 WD2TM=1
WD2_WDR	0	0	-	WD2 reset latch - set when WD2RESET or STOPPING states are entered, cleared upon read
				0 WD2RST signal = 0 1 WD2RST signal = 1
WD1_LO	0	0	-	WD1 lockout - reflects WD1 lockout state Set and cleared per Watchdog Timer Flow Diagram
				0 WD1 Lockout inactive 1 WD1 Lockout active
WD1_TM	0	0	0	WD1 test mode - reflects WD1TM signal state
				Set and cleared per Watchdog Timer Flow Diagram
				0 WD1TM=0 1 WD1TM=1
WD1_WDR	0	0	-	WD1 reset latch
				Set and cleared per Watchdog Timer Flow Diagram
				0 WD1_WDR signal = 0 1 WD1_WDR signal = 1
MCURST	0	0	-	MCU reset latch - set when MCUFLT pin goes low, cleared upon read
				0 MCURST signal = 0 1 MCURST signal = 1
WSMRST	1	1	-	Watchdog state machine reset
				Set when WSM reset goes to '1', cleared upon SPI read
				<ul><li>0 WSM reset has not occurred</li><li>1 WSM reset has occurred</li></ul>
SSMRST	1	1	1	Safing state machine reset
				Set when SSM reset goes to '1', cleared upon SPI read
				<ul><li>0 SSM reset has not occurred</li><li>1 SSM Reset has occurred</li></ul>
VCORE_ERR	0	-	-	VCOREMON pin status - set when VCOREMON pin goes out of range, reset upon read



L9680 SPI interfaces

0 VCORMON in range (VCORE\_UV<VCOREMON<VCORE\_OV)
1 VCOREMON out of range (VCOREMON<VCORE\_UV, or VCOREMON>VCORE\_OV)

POR 1 - - Power on Reset

Set when POR goes to '1', cleared upon SPI read

0 POR reset has not occurred

1 POR Reset has occurred

DS11615 Rev 2 71/280

SPI interfaces L9680

# 7.3.2 System configuration register (SYS\_CFG)

	19	18	17	16	15	14	13	12	11	10	9	8	8 7		5	4	3	2	1	0
MOSI	-			EN_AUTO_SWITCH_OFF	x	LOW_POWER_MODE	KEEP_ERBST_ON	PSINHSEL	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SOME	OCIMEAO	SATIMAN	OKIMIA	DCS_PAD_V	SAFESEL	VSF_V	VINGOOD_FILT_SEL	WD1_TO_DIS	
MISO	0	0	0	0	EN_AUTO_SWITCH_OFF	0	LOW_POWER_MODE	KEEP_ERBST_ON	PSINHSEL	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SOMEAS	SQMEAS		OKIMIA	DCS_PAD_V	SAFESEL	VSF_V	VINGOOD_FILT_SEL	WD1_TO_DIS

 ID:
 01

 Type:
 RW

 Read:
 0100

 Write:
 0002

NSM NSM

EN\_AUTO\_SWITCH\_OFF

0 0 Enable auto switch off ISRC current source and DCS regulator after measurement completion

0 Auto switch off disabled 1 Auto switch off enabled

LOW\_POWER\_MODE

Selection of over current detection for SYNCBOOST, SATBUCK and VCCBUCK

0 High current level1 Low current level

KEEP\_ERBST\_ON 0 0 ER Boost behaviour during ER state

0 ER Boost is disabled

1 ER Boost stay enabled

PSINHSEL 1 1 1 PSINH engine mode select Updated by SSM\_RESET or SPI write

0 Internal 1 External HI\_LEV\_DIAG\_TIME 0 Selection of duration of high level squib diagnostics 0 0 0 Short time (see high level diag diagram) 1 Long time (see high level diag diagram) RSU\_SYNCPULSE\_ 0 0 Selection of sync pulses shift duration SHIFT\_CONF 0 Long time 1 Short time **SQMEAS** 00 00 00 Sample number in DC sensor, squib measurement and temperature conversions Updated by SSM\_RESET or SPI write 00 8 samples 01 16 samples 10 4 samples 11 2 sample **VMEAS** 00 00 00 Sample number in any other voltage measurement conversions Updated by SSM\_RESET or SPI write 00 4 samples 01 16 samples 10 8 samples 11 1 sample DCS\_PAD\_V 0 Passenger inhibit measurement mode 0 Current 1 Voltage SAFESEL 1 1 1 Safing engine mode select Updated by SSM\_RESET or SPI write 0 Internal safing engine 1 external safing engine

DS11615 Rev 2 73/280

VSF\_V 0 0 0 VSF voltage select Updated by SSM\_RESET or SPI write 0 20V 1 25V VINGOOD\_FILT\_SEL Selector of filter time for VINGOOD going low (time is fixed to  $3.5~\mu s$  for VINGOOD going high) 0 1 µs 1 3.5 µs Disable of initial 500ms timeout function of WD1 state machine WD1\_TO\_DIS 0 Updated by WSM\_RESET or SPI write 0 timeout function is enabled 1 timeout function is disabled

DS11615 Rev 2

74/280

#### 7.3.3 System control register (SYS\_CTL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		RESTART_SYBST_SEL	PD&VRCM_SEL	KEEP_SYNCBST_ON	VIN_TH_SEL	IS HI NOWINA	⊑'	ER_BST_V	<u> </u>	را ک	ER_BST_EN	SYNCBST_EN	SPLOFF	x	ERSWITCH_LIM_SEL	V_T28Y2	SAT_V
MISO	0	0	0	0	RESTART_SYBST_SEL	PD&VRCM_SEL	KEEP_SYNCBST_ON	VIN_TH_SEL	VRATMON TH SEI	[	ER_BST_V	<u> </u>		ER_BST_EN	VSUP_EN	SPLOFF	0	ERSWITCH_LIM_SEL	SYBST_V	SAT_V

**ID**: 02

Type: RW

**Read:** 0200

Write: 0004

POR WSM

RESTART\_SYBST\_SEL

- Selection of comparator used to restart sync boost in erstate (don't care in case SYS\_CTL(KEEP\_SYNCBST\_ON) bit is high)
  - 0 VIN comparator is used; syncboost is switched off entering erstate and switched on once VIN goes above VIN\_fastslope threshold.
  - 1 SYNCBST comparator is used; syncboost is switched off entering erstate and switched on when SYNCBST voltage falls down VSYNCBST\_RESTART\_TH threshold (this condition requires that SYNCBST voltage has been pulled up above the same threshold previously).

PD&VRCM\_SEL 0 0 Squib pull down current level and VRCM leakage to GND threshold selection

- 0 1 mA pull down current and 450  $\mu A$  VRCM leakage to GND threshold
- 1 5 mA pull down current and 2 mA VRCM leakage to GND threshold

KEEP\_SYNCBST\_ON 1 - - SYNC Boost behaviour during ER state

- 0 SYNC Boost is disabled entering in ER state
- 1 SYNC Boost stay enabled in ER state. If boost is OFF in ER state and this command is received during that state the boost is switched on.

VIN\_TH\_SEL 0 0 VIN comparators threshold selector

0 VINGOOD= VINgood0

1 VINGOOD= VINgood1

00 VBATMON comparators threshold selector VBATMON\_TH\_SEL 00 00 00 VINGOOD= VINgood0 01 VINGOOD= VINgood1 10 VINGOOD= VINgood2 11 VINGOOD= VINgood3 ER\_BST\_V 0 0 ER Boost voltage select Updated by SSM\_RESET or SPI write 0 set 23V boost 1 set 33V boost ER CUR EN 00 00 00 ER charge / discharge control 00 Current sources off 01 ER charge enabled 10 ER discharge enabled 11 Current sources off 1 Boost enable ER\_BST\_EN Updated by SSM\_RESET or SPI write 0 ER\_BOOST OFF request 1 ER\_BOOST ON request 1 Syncboost enable SYNCBST EN Updated by SSM\_RESET or SPI write 0 SYNC BOOST OFF request 1 SYNC\_BOOST ON request SPI OFF 0 0 Go to POWER OFF state from POWERMODE SHUTDOWN state Updated by SSM\_RESET or SPI write while in POWERMODE SHUTDOWN state 0 no effect 1 transition to POWER OFF state ERSWITCH\_LIM\_SEL ERswitch current limitation select Updated by POR or SPI write 0 Low current limit 1 High current limit is no more available SYBST\_V 0 Sync Boost voltage select Updated by SSM\_RESET or SPI write 0 Low - syncboost=12V 1 High - syncboost=14.75V

76/280 DS11615 Rev 2



SAT\_V 0 0 SatBuck and Satellite Interface voltage select

Updated by SSM\_RESET or SPI write

0 Low - satbuck=7.2V 1 High - satbuck=9V

## 7.3.4 SPI Sleep command register (SPI\_SLEEP)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-									\$3C	95X							
MISO	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ID:** 03

Type: W

Read: -

Write: 0006

POR WSM

SLEEP\_MODE N/A N/A N/A Non-latched command that allows transition into

POWERMODE\_SHUTDOWN state according to the Power Control State Flow Diagram

#### 7.3.5 System status register (SYS\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	0	0	0	0	0	0	0	0	0		OPER_CTL_STATE		0	0	0	0	0		POWER_CTL_STATE	

**ID**: 04

Type: R

**Read:** 0400

Write: -

POR WSM SSM

OPER\_CTL\_STATE[2:0] 000 000 000 Reports Operating Control State

Updated per Power Up Phases diagram

000 = INIT

DS11615 Rev 2

77/280

001 = DIAG

010 = SAFING

011 = SCRAP

100 = ARMING

101 unused

110 unused

111 unused

POWER\_CTL\_STATE[2:0] 000 - - Reports Power Control State

Updated per Power Control State Flow Diagram

000 = AWAKE

001 = STARTUP

010 = RUN

011 = ER

100 = POWER MODE SHUTDOWN

101 unused

110 unused

111 unused

#### 7.3.6 Power state register (POWER\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO	WAKEUP	VBBAD	NOT_VBGOOD	VINBAD	NOT_VINGOOD	S_BST_NOK	SATBUCK_NOK	ER_BST_NOK	vc_uv	vc_0v	0	ER_BST_ON	ER_CHRG_ON	ER_LCDIS_ON	ER_HCDIS_ON	ER_SW_ON	S_BST_ACT	SATBUCK_ACT	VCC_ACT	VSF_ACT

**ID**: 05

Type: R

**Read:** 0500

Write: -

POR WSM SSM

WAKEUP - - - WAKEUP pin status

Set and cleared based on voltage

0 WAKEUP pin < WU\_off

1 WAKEUP pin > WU\_on

VBBAD - - - VBATMON bad pin status

Set and cleared based on voltage

1 VBATMON < VBBAD

0 VBATMON > VBBAD

NOT\_VBGOOD - - - VBATMON good pin status

Set and cleared based on voltage

1 VBATMON < VBGOOD

0 VBATMON > VBGOOD

VINBAD - - - VIN bad pin status

Set and cleared based on voltage

0 VIN > VINBAD

1 VIN < VINBAD

NOT\_VINGOOD - - - VIN good pin status

Set and cleared based on voltage

0 VIN > VINGOOD

1 VIN < VINGOOD

S\_BST\_NOK - - - SYNCBOOST bad pin status

57

DS11615 Rev 2 79/280

Set based on voltage, cleared on SPI read 1 V\_SYNCBOOST < SYNCBOOST\_OK 0 V SYNCBOOST > SYNCBOOST OK SATBUCK\_NOK SATBUCK bad pin status Set based on voltage, cleared on SPI read 1 V SATBUCK < SATBUCK OK 0 V\_SATBUCK > SATBUCK\_OK ER\_BST\_NOK ERBOOST pin status Set and cleared based on voltage 1 V\_ERBOOST < ERBOOST\_OK 0 V\_ERBOOST > ERBOOST\_OK VCC\_UV VCC\_UV status Set based on voltage, cleared on SPI read 0 VCC > VCC\_UV 1 VCC < VCC\_UV VCC\_OV - VCC\_OV status Set based on voltage, cleared on SPI read 0 VCC < VCC OV 1 VCC > VCC\_OV ER\_BST\_ON ERBOOST\_ON state Updated according to ER\_BOOST Control Behavior diagram 0 RBOOST\_OFF or ERBOOST\_OT state or ER\_BST\_STBY state (boost not running) 1 ERBOOST\_ON state (boost running) ER\_CHRG\_ON 0 ERCHARGE\_ON state Updated according to ER\_CHARGE Power Mode Control diagram 0 ERCHARGE\_ON = 0 1 ERCHARGE\_ON = 1 ER\_LCDIS\_ON ER Low Current Discharge State Updated according to ER Low current discharge state diagram 0 ER LCDIS OFF 1 ER\_LCDIS\_ON

ER\_HCDIS\_ON ER High Current Discharge State Updated according to ER High Current discharge state diagram 0 ER\_HCDIS\_OFF 1 ER\_HCDIS\_ON ER\_SW\_ON ER\_SWITCH State Updated according to ER Switch state diagram 0 ER\_SWITCH\_OFF 1 ER\_SWITCH\_ON S BST ACT SYNCBOOST Active state Updated according to SYNCBOOST Power Mode Control state diagram 0 SYNCBOOST supply in SYNCBOOST\_OFF state 1 SYNCBOOST supply in SYNCBOOST\_ON state 0 SATBUCK Active state SATBUCK\_ACT 0 Updated according to SATBUCK Power Mode Control state diagram 0 SATBUCK supply in SATBUCK\_OFF state 1 SATBUCK supply in SATBUCK\_ON state VCC\_ACT **Buck Active state** Updated according to VCC Power Mode Control state diagram 0 VCC supply in VCC\_OFF or VCC\_SHUTDOWN states 1 VCC supply in VCC\_RAMPUP or VCC\_ON states VSF\_ACT 0 VSF Active state Updated according to VSF Control Logic diagram 0 VSF EN = 0 1 VSF\_EN = 1

#### 7.3.7 Deployment configuration registers (DCR\_x)

Deployment Configuration Channel 0 (DCR\_0)

**Deployment Configuration Channel 1 (DCR\_1)** 

**Deployment Configuration Channel 2 (DCR\_2)** 

**Deployment Configuration Channel 3 (DCR\_3)** 

**Deployment Configuration Channel 5 (DCR\_5)** 

Deployment Configuration Channel 6 (DCR\_6)

Deployment Configuration Channel 7 (DCR\_7)

Deployment Configuration Channel 8 (DCR\_8)

**Deployment Configuration Channel 9 (DCR\_9)** 

Deployment Configuration Channel A (DCR\_A)

**Deployment Configuration Channel B (DCR\_B)** 

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	х	х	x			Deploy	/_Time	)				omit original	של של של של	х	PD_CURR_CSR
MISO	0	0	0	0	0	0	0	0			Deploy	/_Time	)				omit oring time	D	0	PD_CURR_CSR

**ID:** 06 (DCR 0)

07 (DCR\_1)

08 (DCR\_2)

09 (DCR\_3)

0A (DCR\_4)

0B (DCR\_5)

0C (DCR\_6)

0D (DCR\_7) 0E (DCR 8)

0F (DCR\_9)

10 (DCR A)

11 (DCR\_B)

Type: RW

**Read:** 0600 (DCR\_0)

0700 (DCR\_1)

0800 (DCR\_2)

0900 (DCR\_3)

0A00 (DCR\_4)

0B00 (DCR\_5)

0C00 (DCR\_6)

0D00 (DCR\_7)

0E00 (DCR 8)

0F00 (DCR\_9)

1000 (DCR A) 1100 (DCR\_B) Write: 000C (DCR\_0) 000E (DCR 1) 0010 (DCR\_2) 0012 (DCR\_3) 0014 (DCR 4) 0016 (DCR\_5) 0018 (DCR\_6) 001A (DCR\_7) 001C (DCR\_8) 001E (DCR\_9) 0020 (DCR\_A) 0022 (DCR B) POR Deploy\_Time[5:0] 0000 0000 0000 Default deployment time = 0 us (no deployment, 8 us pulse output on ARM1 00 00 pin during PULSE TEST) Deployment time: actual deployment time (ms) = Deploy Time\*0.064ms (0.064ms/count up to 4.032ms max) Dep\_Current[1:0] 00 00 00 Deployment Current limit select Updated by SSM RESET or SPI write while in DIAG state 00 Unused (no deploy) 01 1.75A min 10 1.2A min 11 Unused (no deploy) Dep\_expire\_time[1:0] 00 00 00 Deploy command expiration timer select Updated by SSM\_RESET or SPI write while in DIAG state 00 500ms 01 250ms 10 125ms 11 0ms PD CURR CSR Pull down current control for Commmon SR connection 0 Updated by SSM RESET or SPI write 0 PD Current OFF only for channel selected for diagnostic measurement, ON for all other channel 1 PD Current OFF for both channels of the channel pair selected for diagnostic measurement, ON for all other channel

DS11615 Rev 2 83/280

#### 7.3.8 Deployment command (DEPCOM)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	х	х	х	СНВДЕРКЕО	CHADEPREQ	СН9DEPREQ	СН8DEPREQ	CH7DEPREQ	СН6DEPREQ	CH5DEPREQ	CH4DEPREQ	СНЗДЕРКЕО	CH2DEPREQ	CH1DEPREQ	CHODEPREQ
MISO	0	0	0	0	0	0	0	0	CHBDEP	CHADEP	СН9DEP	CH8DEP	CH7DEP	СН6DEP	CH5DEP	CH4DEP	СНЗДЕР	CH2DEP	CH1DEP	СНОБЕР

**ID**: 12

Type: RW

**Read:** 1200

Write:

POR WSM SSM

0024

CHxDEPREQ N/A N/A Channel x Deploy Request - non-latched channel-specific deploy request

0 No change to deployment control for channel x

1 Clear and start Expiration timer if in ARMING or SAFING state and in DEPLOY\_ENABLED state

CHxDEP 0 0 Channel x deployment expiration timer enable

Set when SPI\_DEPCOM(CHxDEPREQ=1) AND in ARMING or SAFING state AND in DEP\_ENABLED state

Cleared on SSM\_RESET OR when in DEP\_DISABLED state OR when Deploy Expiration Timer x reaches timeout threshold

- 1 Expiration timer enabled Deploy command still valid
- 0 Expiration Timer disabled Deploy command no more valid

#### 7.3.9 Deployment status registers (DSR\_x)

Deployment Status Channel 0 (DSR\_0)
Deployment Status Channel 1 (DSR\_1)
Deployment Status Channel 2 (DSR\_2)
Deployment Status Channel 3 (DSR\_3)
Deployment Status Channel 5 (DSR\_5)
Deployment Status Channel 6 (DSR\_6)
Deployment Status Channel 7 (DSR\_7)
Deployment Status Channel 8 (DSR\_8)
Deployment Status Channel 9 (DSR\_9)
Deployment Status Channel A (DSR\_A)
Deployment Status Channel B (DSR\_B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	0	0	0	0	CHXDS	CHXSTAT	0	DCRXERR								DE	EP_CH	x_Exp1	Timer	

13 (DSR\_0)
14 (DSR\_1)
15 (DSR\_2)
16 (DSR\_3)
17 (DSR\_4)
18 (DSR\_5)
19 (DSR\_6)
1A (DSR\_7)
1B (DSR\_8)
1C (DSR\_9)
1D (DSR\_A)
1E (DSR\_B)

Type: R

Read: 1300 (DSR\_0) 1400 (DSR\_1) 1500 (DSR\_2) 1600 (DSR\_3) 1700 (DSR\_4) 1800 (DSR\_5) 1900 (DSR\_6) 1A00 (DSR\_7)

1B00 (DSR\_8) 1C00 (DSR\_9) 1D00 (DSR\_A) 1E00 (DSR\_B)

Write: -

	POR	WSM	SSM	
CHxDS	0	0	0	Channel x deployment successful
				Updated according to Deployment Driver Control Logic
				(set when deployment terminates on ch x due to deploy timer timeout, cleared on SSM_RESET OR when deployment starts on ch x)
				0 Deployment not successful
				1 Deployment successful
CHxSTAT	0	0	0	Channel x deployment status
				Updated according to Deployment Driver Control Logic
				(set when deployment starts on ch x, cleared on SSM_RESET OR when deployment terminates due to deploy timer timeout, LS Over current OR $$
				GND Loss)
				0 Deployment not in progress
				1 Deployment in progress
DCRxERR	0	0	0	Deployment configuration register error
				0 Deploy configuration change accepted and stored in memory
				1 Deploy configuration change rejected because deploy is in progress (or DEP_EXPIRE_TIME changed when in DEP_ENABLED state)
DEP CHx ExpTimer[5:0]	0000	0000	0000	Channel x Deployment Expiration Timer value 8ms/count
o. wwpo.[o.o]				Orialine & Deployment Expiration Time Value on 5/count

00 00 Updated according to Deployment Diver Control Logic
(Cleared on SSM\_RESET OR when Exp Timer times out OR when SPI\_DEPREQx is received while in DEP\_ENABLED state AND in ARMING or SAFING states)

#### 7.3.10 Deployment current monitor registers (DCMTSxy)

Deployment Current Monitor Status Channel 0,1 (DDCMTS01)
Deployment Current Monitor Status Channel 2,3 (DDCMTS23)
Deployment Current Monitor Status Channel 4,5 (DDCMTS45)
Deployment Current Monitor Status Channel 6,7 (DDCMTS67)
Deployment Current Monitor Status Channel 8,9 (DDCMTS89)
Deployment Current Monitor Status Channel A,B (DDCMTSAB)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	0	0	0	0			Curren	t_Mon	_Timer	_y[7:0]					Curren	it_Mon	_Timer	_x[7:0]		

**ID:** 1F (DDCMTS01)

20 (DDCMTS23) 21 (DDCMTS45) 22 (DDCMTS67) 23 (DDCMTS89) 24 (DDCMTSAB)

Type: R

Read: 1F00 (DDCMTS01)

2000 (DDCMTS23) 2100 (DDCMTS45) 2202 (DDCMTS67) 2300 (DDCMTS89) 2400 (DDCMTSAB)

Write: -

POR WSM SSM

Current\_Mon\_Timer\_y[7:0] \$00 \$00 \$00 Channel y current monitor timer value corresponding to SPI command

DCMTSxy.

Set to default (cleared) on SSM\_RESET or when a new deployment starts on channel y. Increments each 16µs while deployment current exceeds

monitor threshold on channel y

Current\_Mon\_Timer\_x[7:0] \$00 \$00 \$00 Channel x current monitor timer value corresponding to SPI command

DCMTSxy.

Set to default (cleared) on SSM\_RESET or when a new deployment starts on channel x. Increments each  $16\mu s$  while deployment current exceeds

monitor threshold on channel y

#### 7.3.11 Deploy enable register (SPIDEPEN)

		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Г	MOSI			-				-	-		-	DE	PEN_	WR[15	:0]						
	MISO	0	0	0	0							DEF	PEN_S	TATE[1	5:0]						

**ID**: 25

 Type:
 RW

 Read:
 2500

 Write:
 004A

POR WSM SSM

DEPEN\_WR[15:0] N/A N/A N/A Non-latched encoded value for LOCK / UNLOCK command

\$0FF0 LOCK - enter DEP\_DISABLED state \$F00F UNLOCK - enter DEP\_ENABLED state.

DEPEN\_STATE[15:0] \$0FF0\$0FF0Deploy Enabled State

Updated according to Global SPI Deployment Enable State Diagram

\$0FF0 In DEP\_DISABLED state \$F00F In DEP\_ENABLED state

## 7.3.12 Deployment ground loss register (LP\_GNDLOSS)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-	-	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	0	0	0	0	0	0	0	0	GNDLOSSB	GNDLOSSA	GNDLOSS9	GNDLOSS8	GNDLOSS7	GNDLOSS6	GNDLOSS5	GNDLOSS4	GNDLOSS3	GNDLOSS2	GNDLOSS1	GNDLOSSO

**ID**: 26

Type: R

**Read:** 2600

Write: -

POR WSM SSM

GNDLOSSx 0 0 Loop x Squib Ground loss

Cleared upon SSM\_RESET or SPI read. Set when GND loss is detected during deployment or loop diag's (HS sw test, LS sw test, squib resistance)

0 Loss of ground not detected

1 Loss of ground detected



# 7.3.13 Device version register (VERSION\_ID)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	0	0	0	0	0	0	0	0	0	DE	VICE	ID	0	0			VE	RSN		

ID: 27Type: RRead: 2700

Write: -

POR WSM SSM

DEVICE ID - - Identification of the device

Static value - never updated

001 Low end010 Medium end011 High end

VERSN - - Identification of the silicon version

Static value - never updated

000000 AA version 000001 AB version 001000 BA version 001001 BB version 010000 CA version 010001 CB version 010010 CC version

## 7.3.14 Watchdog retry configuration register (WD\_RETRY\_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI				-			WD	2_ERR	TH	WD2_	RETR	Y_TH	Х	Х	Х	Х	Х	WD1	_RETR	Y_TH
MISO	0	0	0	0	0	0	WD	2_ERR	TH	WD2	RETR	Y_TH	0	0	0	0	0	WD1	RETR'	Y_TH

 ID:
 28

 Type:
 RW

 Read:
 2800

Write:

POR WSM SSM

0050

WD2\_ERR\_TH 4 4 - WD2 error counter threshold (number of W2 reset permitted before going to

WD2\_STOP state)

WD2\_RETRY\_TH 4 4 - WD2 retry counter threshold (number of W2 errors permitted before asserting

WD2\_Lockout and increment WD2\_ERRcnt)

WD1\_RETRY\_TH 7 7 - WD1 retry counter threshold (number of WD errors permitted before latching

WD1\_LOCKOUT=1)

#### 7.3.15 Microcontroller fault test register (MCU\_FLT\_TEST)

		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MOSI			-		MCU_FLT_TEST Mode															
ſ	MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ID**: 29

Type: W

Read: -

Write: 0052

MCU Fault Test Mode - Allows the masking of the MCUFLT\_ERR and prevents reset

\$0FF0 Mask MCUFLT\_ERR \$F00F Do not mask MCUFLT\_ERR

## 7.3.16 Watchdog timer configuration register (WDTCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	WD1_MODE			WD <sup>-</sup>	TMIN[6	S:0]					WD	TDELT	A[6:0]		•
MISO	0	0	0	0	0	WD1_MODE			WD <sup>-</sup>	TMIN[6	S:0]					WD	TDELT	A[6:0]		

 ID:
 2A

 Type:
 RW

 Read:
 2A00

 Write:
 0054

POR WSM SSM

WD1\_MODE 0 0 - WD1 Mode

Updated by WSM\_RESET or SPI write while in WD1\_INIT state

0 Fast WD1 mode - nominal 8µs timer resolution (2ms max value)

1 Slow WD1 mode - nominal  $64\mu s$  timer resolution (16.3ms max value)

WDTMIN[6:0] \$32 \$32 - WD1 window minimum value - resolution according to WD1\_MODE bit (\$32 =

400µs in WD1 fast mode)

Updated by WSM\_RESET or SPI write while in WD1\_INIT state

 $\label{lem:wdtmin} \mbox{WDTMIN} \mbox{[6:0]} \quad \mbox{\$19} \quad \mbox{$^{-}$ WD1 window delta value - WDTMAX=WDTMIN+WDTDELTA - resolution}$ 

according to WD1\_MODE bit (\$19 = 200µs in WD1 fast mode)

Updated by WSM\_RESET or SPI write while in WD1\_INIT state

## 7.3.17 WD1 timer control register (WD1T)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	Х	Х	Х	х	Х	Х	Х	Х	Χ	WD1C	TL[1:0]
MISO	0	0	0	0				WD1_T	IMER				0	0	0	0	0	0	WD1C	TL[1:0]

 ID:
 2B

 Type:
 RW

 Read:
 2B01

 Write:
 0056

POR WSM SSM

WD1CTL[1:0] 00 00 WD1 Control command

Updated by SSM\_RESET or SPI write

00 NOP

01 Code 'A'

10 Code 'B'

11 NOP

WD1\_TIMER \$00 \$00 WD1 Window timer value

Cleared by SSM\_RESET or by WD1 refresh, incremented every  $8\mu s$  or  $64\mu s$  while in WD1\_RUN or WD1\_TEST states

#### 7.3.18 WD state register (WDSTATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Χ	Х	Х	Χ	Х	Х	Х	Х	Х
MISO	0	0	0	0	0	WE	1_ER	R_CNT	[3:0]	WD_	STATE	[2:0]	WD2	_ERR	_CNT[	3:0]	V	/D2_S	TATE[2:	0]

**ID:** 2C

Type: R

Read: 2C00

Write: -

POR WSM SSM

WD1\_ERR\_CNT[3:0] 0000 0000 - Watchdog 1 error counter

Updated according to Watchdog State Diagram

WD1\_STATE[2:0] 000 000 - Watchdog state

Updated according to Watchdog State Diagram

000 INITIAL
001 RUN
010 TEST
011 RESET
100 OVERRIDE

WD2\_ERR\_CNT[3:0] 0000 0000 - Watchdog 2 error counter

Updated according to Watchdog State Diagram

WD2\_STATE[3:0] 0000 0000 - Watchdog state

Updated according to Watchdog State Diagram

0000 INITIAL
 0001 OVERRIDE
 0010 INITSEED
 0011 RUN
 0100 TEST
 0101 QUAL
 0110 LOCK
 0111 STOPPING
 1000 STOP
 1001 RESET

## 7.3.19 Clock configuration register (CLK\_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		X	x	X	x	X	x	FORD R PER 14-07	-¦	IO-11 IIS I NOBLYS	-	L (	SYBSI_F_SEL[1:0]	AUX_SS_DIS	MAIN_SS_DIS	10.11 E CE114.01	-ı I
MISO	0	0	0	0	0	0	0	0	0	0	NOCECK E SEI		CATECK E SEL	, ,	L 6	SYBSI_F_SEL	AUX_SS_DIS	MAIN_SS_DIS	CDDCT C OCI	-¦

 ID:
 2D

 Type:
 RW

 Read:
 2D00

 Write:
 005A

POR WSM SSM

VCCBCK\_F\_SEL[1:0] 00 - - VCCBuck switching frequency select

Updated by POR or SPI write

00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz

SATBCK\_F\_SEL[1:0] 00 - - SatBuck switching frequency select

Updated by POR or SPI write

00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz

SYBST\_F\_SEL[1:0] 00 - - Sync Boost switching frequency select

Updated by POR or SPI write

00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz

AUX\_SS\_DIS 1 - - Auxiliary oscillator Spread Spectrum disable

Updated by POR or SPI write

0 Spread Spectrum enabled

1 Spread Spectrum disabled

MAIN\_SS\_DIS 0 - - Main oscillator Spread Spectrum disable

Updated by POR or SPI write

0 Spread Spectrum enabled

1 Spread Spectrum disabled

ERBST\_F\_SEL[1:0] 00 - - ER Boost switching frequency select

Updated by POR or SPI write

00 1.88 MHz

01 2.13 MHz

10 2.00 MHz

11 2.00 MHz

## 7.3.20 Scrap seed read command register (SCRAP\_SEED)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO	0	0	0	0	0	0	0	0	0	0	0	0				SEE	D[7:0]			

**ID**: 2E

Type: R

Read: -

Write: 2E00

POR WSM SSM

N/A N/A N/A

SEED[7:0] \$00 \$00 \$00 Random scrap seed value - generated from a free-running 8-bit counter

## 7.3.21 Scrap key write command register (SCRAP\_KEY)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MOSI			-		Х	Х	Х	х	х	Х	Х	Х				KEY[7:0]					
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**ID**: 2F

Type: W Read: -

Write: 005E

POR WSM SSM

N/A N/A N/A

KEY[7:0] \$00 \$00 KEY value submitted to the SCRAP state machine (correct value is derived from the seed value using a simple logical inversion on the even-numbered bits (0, 2, 4, 6))

## 7.3.22 Scrap state entry command register (SCRAP\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-									\$35	535							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ID**: 30

Type: W Read: -

Write: 0060

WS WS SS N/A N/A N/A

Non-latched Scrap State entry command

Enter Scrap state from DIAG state

## 7.3.23 Safing state entry command register (SAFING\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-									\$AC	CAC							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

 ID:
 31

 Type:
 W

 Read:

Write: 0062

MO WS WS N/A N/A

Non-latched Safing State entry command

Enter safing state from DIAG state and clear arming pulse stretch counter (if received in DIAG or SAFING state)

# 7.3.24 WD2 recover write command register (WD2\_RECOVER)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	Х	Х	Χ								
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

 ID:
 32

 Type:
 W

 Read:

Write:

POR WSM SSM

0064

N/A N/A N/A

Non-latched command to clear WD2\_retry counter during WD2 LOCK state

## 7.3.25 WD2 seed read command register (WD2\_SEED)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	х	х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO	0	0	0	0			WD2	_PRE\	KEY[7	7:0]					٧	VD2_S	EED[7	:0]		

**ID:** 33

Type: R

Read: -

Write: 3300

POR WSM SSM

N/A N/A N/A

WD2\_PREV\_KEY[7:0] \$0D \$0D Previous WD2 key value - stored key from previous comparison

WD2 SEED[7:0] \$F0 \$F0 Random WD2 seed value - generated from a free-running 8-bit counter

## 7.3.26 WD2 key write command register (WD2\_KEY)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х				ΚE	/[7:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ID**: 34

Type: W

Read: -

Write: 0068

POR WSM SSM

N/A N/A N/A

KEY[7:0] Previous WD2 key value - stored key from previous comparison

\$0D \$0D (correct value is derived from WD2\_KEY = WD2\_SEED ‡ WD2\_PREV\_KEY + \$01 where ‡ denotes a bit-wise XOR)

98/280 DS11615 Rev 2



# 7.3.27 WD test command register (WD\_TEST)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-				WE	1_TES	ST = \$30	С					W	D2_TE	ST = 9	3C		
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

 ID:
 35

 Type:
 W

 Read:

Write: 006A

MSW N/A N/A

\$0D \$0D \$0D Non-latched WD1 and WD2 Test Commands

 $\ensuremath{\mathsf{WD1\_TEST}}$  and  $\ensuremath{\mathsf{WD2\_TEST}}$  SPI command as described in Watchdog State Diagram

## 7.3.28 System diagnostic register (SYSDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				Х	Х	Х	Х	х	Х	Х	Х	х	Х	Х	Х		DSTE	ST[3:0]	
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTEST[3:0]			

 ID:
 36

 Type:
 RW

 Read:
 3600

 Write:
 006C

POR WSM SSM

DSTEST[3:0] 0000 0000 0000 Diagnostic State Test selection

Updated by SSM\_RESET or SPI write while in DIAG state

0000 = all outputs inactive

0001 = ARM 1 pin active

0010 = ARM 2 pin active

0011 = ARM 3 pin active

0100 = ARM 4 pin active

0101 = PSINHB pin inactive (high)

0110 = VSF regulator active

0111 = HS squib driver FET active

1000 = LS squib driver FET active

1001 = Output deployment timing pulses on ARM1 (separated by 8 ms)

1010 = HS squib driver FET active to test full path (FET switched off by the comparator used in the deployment current timer monitor)

1011 - 1111 = all outputs inactive

## 7.3.29 Diagnostic result register for deployment loops (LPDIAGSTAT)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	Х	Х	Х	Х	х	Х	Х	Х	Х	Х	х	Х
MISO	DIAG_LEVEL	TIP	0	FP	FETON	HS_DRV_OK	HSR_HI	HSR_LO		GES MEAS CHSELLICITED TO SAID SEE			SBL	STG	STB	SQP			LEAK_CHSEL	

ID: 37Type: RRead: 3700Write: -

POR WSM SSM

DIAG\_LEVEL 0 0 Diagnostic mode selector Not present for low level diagnostic

Updated by SSM\_RESET or SPI write to LPDIAGREQ

0 low level mode

1 high level mode

TIP 0 0 High level diagnostic test is running

Updated by SSM\_RESET or Loops diagnostic state machine

0 High level diagnostic test is not running

1 High level diagnostic test is running

FP 0 0 Fault present before requested diagnostic

Updated by SSM\_RESET or Loops diagnostic state machine

0 Fault not present before requested diagnostic

1 Fault present before requested diagnostic

FETON 0 0 FET activation during diagnostic

Updated by SSM\_RESET or Loops diagnostic state machine or when HS or LS FET is activated during DIAG state

0 FET is off during diagnostic

1 FET is on during diagnostic

HS\_DRV\_OK 0 0 FET Test Status

Updated by SSM\_RESET or Loops diagnostic state machine or when driver full path test is run test is run

0 HS squib driver full path test did not complete successfully

1 HS squib driver full path test complete successfully

HSR\_HI 0 0 0 HSR Diagnostic - HIGH Range

Updated by SSM\_RESET or Loops diagnostic state machine or when squib resistance test is run

0 HSR measurement < HSR HIGH value

1 HSR measurement > HSR HIGH value

HSR\_LO 0 0 HSR Diagnostic - Low Range

Updated by SSM\_RESET or Loops diagnostic state machine or when squib resistance test is run

1 HSR measurement< HSR LOW value

0 HSR measurement > HSR LOW value

0100 - 1111 None Selected

RES\_MEAS\_CHSEL[3:0] 0000 0000 0000 Channel selected for resistance measurement

HIGH\_LEV\_DIAG\_SELECTED[3:0]

Updated by SSM\_RESET or Loops diagnostic state machine or as determined by squib resistance channel selected

0000 = Ch 0	0000 No diagnostic selected
0001 = Ch 1	0001 VRCM CHECK
0010 = Ch 2	0010 Leakage CHECK
0011 = Ch 3	0011 Short Between Loops CHECK
0100 = Ch 4	0100 ER cap ESR measure
0101 = Ch 5	0101Squib resistance range CHECK
0110 = Ch 6	0110 Squib resistance measurement
0111 = Ch 7	0111 FET test
1000 = Ch 8	1000 - 1111 Unused
1001 = Ch 9	
1010 = Ch A	
1011 = Ch B	

102/280 DS11615 Rev 2



SBL 0 0 Short between loop state

Updated by SSM\_RESET or Loops diagnostic state machine

0 Short between squib loops is not present

1 Short between squib loops is present

STG 0 0 Short to Ground Test Status

Updated by SSM\_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic

0 STG not detected

1 STG detected

STB 0 0 Short to Battery Test Status

Updated by SSM\_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic

0 STB not detected

1 STB detected

SQP 0 0 Squib PIN where leakage test has been performed

Updated by SSM\_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic

0 SRx

1 SFx

LEAK\_CHSEL[3:0] 0000 0000 0000 Channel selected for leakage measurement

Updated by SSM\_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic

0000 = Ch 0

0001 = Ch 1

0010 = Ch 2

0011 = Ch 3

0100 = Ch 4

0101 = Ch 5

0110 = Ch 6

0111 = Ch 7

1000 = Ch 8

1001 = Ch 9

1010 = Ch A

1011 = Ch B

1100 - 1111 None Selected



# 7.3.30 Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	3	ISRC [1:0]	ISINK	. CONTACT			RES MEAS CHSELT3:01					LEAK_CHSEL[3:0]	
MISO	0 0 0 0		0	DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR		ISRC [1:0]	ISINK	VBCMf4.01			RES MEAS CHSEL[3:0]RES					LEAK_CHSEL[3:0]		

 ID:
 38

 Type:
 RW

 Read:
 3800

 Write:
 0070

POR WSM SSM

DIAG LEVEL 0 0 Diagnostic mode selector

Updated by SSM\_RESET or SPI write

0 low level mode

1 N/A - see description below

ISRC\_CURR\_SEL 0 0 0 Selection of ISRC current value

0 40mA

1 8mA

PD\_CURR 0 0 0 Pull down current control

Updated by SSM\_RESET or SPI write

- 0 Request OFF only for channels connected to VRCM or ISINK or ISRC, ON for all other channels
- 1 Request OFF for all channels

ISRC [1:0] 00 00 High side current source for channel selected in RES\_MEAS\_CHSEL[3:0]

Updated by SSM\_RESET or SPI write

00 = OFF

- 01 = ON 40 mA/8 mA current for channel selected in RES\_MEAS\_CHSEL, OFF on all other channels
- 10 = ON bypass current for channel selected in RES\_MEAS\_CHSEL, OFF ON all other channels
- 11 = ON ISRC 40mA or 8mA current for channel selected in RES\_MEAS\_CHSEL and connect the SRM Differential Amplifier to the other squib channel of the selected channel pair

ISINK 0 0 Low Side current sink control (max 50mA)

Updated by SSM\_RESET or SPI write

- 0 All channels OFF
- 1 ON for channel selected by RES\_MEAS\_CHSEL[3:0], OFF on all other channels

VRCM[1:0] 00 00 Voltage Regulator Current Monitor control

Updated by SSM\_RESET or SPI write

- 00 VRCM not connected
- 01 VRCM connected to SFx of channel selected by LEAK\_CHSEL[3:0]
- 10 VRCM connected to SRx of channel selected by LEAK\_CHSEL[3:0] and pull down current of the same channel disabled
- 11 VRCM connected to SRx of channel selected by LEAK\_CHSEL[3:0] and pull down current of the same channel enabled (ISINK and ISRC must be switched off)

RES\_MEAS\_CHSEL[3:0] 0000 0000 0000 Squib Resistance Measurement Channel select - selects the channel and muxes for the resistance test, and the channel for HS driver test (full path fet test) activation

Updated by SSM RESET or SPI write

0000 Channel 0

0001 Channel 1

0010 Channel 2

0011 Channel 3

0100 Channel 4

0101 Channel 5

0110 Channel 6

0111 Channel 7

1000 Channel 8

1001 Channel 9

1010 Channel A

1011 Channel B

0100 - 1111 None Selected



DS11615 Rev 2 105/280

LEAK\_CHSEL[3:0] 0000 0000 0000 Squib Leakage Measurement Channel select - selects the channel and muxes for the leakage test, and the channel for HS/LS FET test activation.

Updated by SSM\_RESET or SPI write

0000 Channel 0

0001 Channel 1

0010 Channel 2

0011 Channel 3

0100 Channel 4

0101 Channel 5

0110 Channel 6

0111 Channel 7

1000 Channel 8

1001 Channel 9

1010 Channel A

1011 Channel B

0100 - 1111 None Selected

# 7.3.31 Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		DIAG_LEVEL	х	x	x	x	x	Х	х		SELHIGH_LEVEL_DIAG_SEL		SQP			LOOP_DIAG_CHSEL[3:0]	
MISO	0	0	0	0	DIAG_LEVEL	0	0	0	0	0	0	0		HIGH_LEVEL_DIAG_SEL		SQP			LOOP_DIAG_CHSEL[3:0]LOOP	

 ID:
 38

 Type:
 RW

 Read:
 3800

 Write:
 0070

POR WSM SSM

DIAG\_LEVEL 0 0 0 Diagnostic mode selector

0 0 N/A - see description above

1 1 high level mode

HIGH\_LEVEL\_DIAG\_SEL 000 000 Selection of high level squib diagnostic

Updated by SSM\_RESET or SPI write

000 No diagnostic selected

001 VRCM CHECK

010 Leakage CHECK

011 Short Between Loops CHECK

100 ER cap ESR measure

101 Squib resistance range CHECK

110 Squib resistance measurement

111 FET test

SQP 0 0 Squib pin select for all leakage diagnostic

Updated by SSM\_RESET or SPI write

0 SRx

1 SFx

LOOP\_DIAG\_CHSEL[3:0] 0000 0000 0000 Channel select - selects the channel and muxes for all squib diagnostic.

Updated by SSM\_RESET or SPI write

0000 Channel 0

0001 Channel 1

0010 Channel 2

0011 Channel 3

0100 Channel 4

0101 Channel 5

0110 Channel 6

0111 Channel 7

1000 Channel 8

1001 Channel 9

1010 Channel A

1011 Channel B

1100 - 1111 None Selected

#### 7.3.32 DC sensor diagnostic configuration command register (SWCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		x	х	х	х	x	x	х	PSINHPOL	DCS_PDCURR	SWOEN	х	х		СНІІ	D[3:0]	
MISO	0 0 0 0			0	0	0	0	0	0	0	0	PSINHPOL	cs_PDCURR	SWOEN	0	0		СНІІ	D[3:0]	

**ID**: 39

Type: RW

**Read:** 3900

Write: 0072

POR WSM

PSINHPOL 0 0 Selector of in range/ out of range for passenger inhibit function

0 if result is inside thresholds the counter is initialized to start value

1 if result is outside thresholds the counter is initialized to start value

DCS\_PDCURR 0 0 Disable of all pull down current for DC sensor

Updated by SSM\_RESET or SPI write



0 OFF for channel under voltage or current measurement, ON for all other channels

1 OFF for all channels

SWOEN 0 0 Switch Output Enable

Updated by SSM\_RESET or SPI write

0 OFF

1 ON

CHID[3:0] 0000 0000 0000 Channel ID - selects DC sensor channel for output activation

Updated by SSM\_RESET or SPI write

0000 Channel 0

0001 Channel 1

0010 Channel 2

0011 Channel 3

0100 Channel 4

0101 Channel 5

0110 Channel 6

0111 Channel 7

1000 Channel 8

0100 - 1111 None Selected

DS11615 Rev 2 109/280

# 7.3.33 ADC request and data registers (DIAGCTRL\_x)

# ADC A control command (DIAGCTRL\_A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	Х	Х	Х	Х			ADO	CREQ_	A[6:0]		
MISO	NEWDATA_A	0	0			ADC	REQ_	A[6:0]						А	DCRE	:S_A[9	:0]			

 ID:
 3A

 Type:
 RW

 Read:
 3A00

 Write:
 0074

# ADC B control command (DIAGCTRL\_B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	Х	Х	Х	х			ADO	CREQ_	B[6:0]		
MISO	NEWDATA_B	0	0			ADC	REQ_I	B[6:0]						Α	DCRE	:S_B[9	:0]			

 ID:
 3B

 Type:
 RW

 Read:
 3B00

 Write:
 0076

#### ADC C control command (DIAGCTRL\_C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			_		Х	Х	Х	х	Х	Х	Х	Х	Х			ADO	CREQ_	C[6:0]		
MISO	NEWDATA_C	0	0			ADC	REQ_	C[6:0]						А	DCRE	S_C[9	):0]			

 ID:
 3C

 Type:
 RW

 Read:
 3C00

 Write:
 0078

#### ADC D control command (DIAGCTRL\_D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			_		Х	Х	Х	х	х	Х	Х	Х	х			ADO	CREQ_	D[6:0]		
MISO	VEWDATA_D	0	0			ADC	REQ_	D[6:0]						Α	DCRE	S_D[9	):0]			

 ID:
 3D

 Type:
 RW

 Read:
 3D00

 Write:
 007A

POR WSM SSM

NEWDATA\_x 0 0 New data available from convertion

Updated by SSM\_RESET or ADC state machine

0 cleared on read

1 convertion finished

ADCREQ\_x[6:0] \$00 \$00 ADC Request select command

Updated by SSM\_RESET or SPI write to DIAGCTRL\_x

Measurement

\$00 Unused

\$01 Ground Ref

\$02 Full scale Ref

\$03 DCSx voltage

\$04 DCSx current

\$05 DCSx resistance

\$06 Squib x resistance

\$07 Internal BG reference voltage (BGR)

\$08 Internal BG monitor voltage (BGM)

\$09 Vcore

\$0A Temperature

\$0B DCS 0 voltage

\$0C DCS 1 voltage

\$0D DCS 2 voltage

\$0E DCS 3 voltage

\$0F DCS 4 voltage

\$10 DCS 5 voltage

\$11 DCS 6 voltage

\$12 DCS 7 voltage

\$13 DCS 8 voltage

\$14 Vb voltage of ER ESR measure (valid only for ADCREQ\_x field of MISO response when ESR measure results are available)

- \$15 Va voltage of ER ESR measure (valid only for ADCREQ\_x field of MISO response when ESR measure results are available)
- \$16 Vc voltage of ER ESR measure (valid only for ADCREQ\_x field of MISO response when ESR measure results are available)
- \$20 VBATMON pin voltage
- \$21 VIN pin voltage
- \$22 Internal analog supply voltage (VINT)
- \$23 Internal digital supply voltage (VDD)
- \$24 ERBOOST pin voltage
- \$25 SYNCBOOST pin voltage
- \$26 VER pin voltage
- \$27 SATBUCK voltage
- \$28 VCC voltage
- \$29 WAKEUP pin voltage
- \$2A VSF pin voltage
- \$2B WDTDIS pin voltage
- \$2C GPOD0 pin voltage
- \$2D GPOS0 pin voltage
- \$2E GPOD1 pin voltage
- \$2F GPOS1 pin voltage
- \$30 GPOD2 pin voltage
- \$31 GPOS2 pin voltage
- \$32 RSU0 pin Voltage
- \$33 RSU1 pin Voltage
- \$34 RSU2 pin Voltage
- \$35 RSU3 pin Voltage
- \$36 SS0 pin voltage
- \$37 SS1 pin voltage
- \$38 SS2 pin voltage
- \$39 SS3 pin voltage
- \$3A SS4 pin voltage
- \$3B SS5 pin voltage
- \$3C SS6 pin voltage
- \$3D SS7 pin voltage
- \$3E SS8 pin voltage \$3F SS9 pin voltage
- \$40 SSA pin voltage
- \$41 SSB pin voltage
- \$46 SF0
- \$47 SF1
- \$48 SF2
- \$49 SF3
- \$4A SF4
- \$4B SF5
- \$4C SF6
- \$4D SF7

\$4E SF8 \$4F SF9 \$50 SFA \$51 SFB

ADCRES\_x[9:0] \$000 \$000 \$000 10-bit ADC result value corresponding to ADCREQ\_x request Updated by SSM\_RESET or ADC state machine

## 7.3.34 Configuration register for switching regulators (SW\_REGS\_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			<del>-</del>		LOW_ERBST_ILIM_ERON	EN_VCC_GNDLOSS_DET	EN_SAT_GNDLOSS_DET	SATBCK_LS_ON_DELAY	VCCBCK_LS_ON_DELAY	SATBCK_FORCE_F_SLOPE	SYBST_FORCE_F_SLOPE	ERBST_FORCE_F_SLOPE	VCCBCK BH SEL14-01	-		SAIBCK_PH_SEL[1:0]	ā	SYBS1_PH_SEL[1:0]	10.10 Lie Foder	ERBSI_PH_SEL[1:0]
MISO	0	0	0	0	LOW_ERBST_ILIM_ERON	EN_VCC_GNDLOSS_DET	EN_SAT_GNDLOSS_DET	SATBCK_LS_ON_DELAY	VCCBCK_LS_ON_DELAY	SATBCK_FORCE_F_SLOPE	SYBST_FORCE_F_SLOPE	ERBST_FORCE_F_SLOPE	NOCECK BH SE	-! 	i	SAIBCK_PH_SEL	-	SYBSI_PH_SEL	10000	

 ID:
 3F

 Type:
 RW

 Read:
 3F00

 Write:
 007E

POR WSM SSM

LOW\_ERBST\_ILIM\_ERON 0 - - ERBoost current limitation behavior selection Updated by POR or SPI write

ERBoost current limitation is NOT reduced if ER Switch is activated.

1 ERBoost current limitation is reduced if ER Switch is activated

EN\_VCC\_GNDLOSS\_DET 0 - New VCC ground loss detection enable

Updated by POR or SPI write

0 run time ground loss detection disabled1 run time ground loss detection enabled

- New SAT ground loss detection enable

Updated by POR or SPI write

0 run time ground loss detection disabled

EN\_SAT\_GNDLOSS\_DET

				1 run time ground loss detection enabled
SATBCK_LS_ON_DELAY	0	-	-	SATBuck low side activation delay Updated by POR or SPI write
				0 No delay is applied
				1 Delay is applied
VCCBCK_LS_ON_DELAY	0	-	-	SVCCBuck low side activation delay Updated by POR or SPI write
				0 No delay is applied
				1 Delay is applied
SATBCK_FORCE_F_SLOPE	0	-	-	SatBuck fast slope selection Updated by POR or SPI write
				0 Fast slope activation depends on VIN voltage
				1 Fast slope is forced ON
SYBST_FORCE_F_SLOPE	0	-	-	SyncBoost fast slope selection Updated by POR or SPI write
				0 Fast slope activation depends on VIN voltage
				1 Fast slope is forced ON
ERBST_FORCE_F_SLOPE	0	-	-	ER Boost fast slope selection Updated by POR or SPI write
				0 Fast slope activation depends on VIN voltage
				1 Fast slope is forced ON
VCCBCK_PH_SEL[1:0]	11	-	-	VCCBuck phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write
				00 0 ns switching ON shift respect to t0
				01 125 ns switching ON shift respect to t0
				10 250 ns switching ON shift respect to t0
				11 375 ns switching ON shift respect to t0
SATBCK_PH_SEL[1:0]	10	-	-	SatBuck phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write
				00 0 ns switching ON shift respect to t0
				01 125 ns switching ON shift respect to t0
				10 250 ns switching ON shift respect to t0
				11 375 ns switching ON shift respect to t0

114/280 DS11615 Rev 2



SYBST\_PH\_SEL[1:0] 01

 SyncBoost phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed)
 Updated by POR or SPI write

00 0 ns switching ON shift respect to t0

01 125 ns switching ON shift respect to t0

10 250 ns switching ON shift respect to t0

11 375 ns switching ON shift respect to t0

ERBST\_PH\_SEL[1:0] 00

 ER Boost phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed)
 Updated by POR or SPI write

00 0 ns switching ON shift respect to t0

01 125 ns switching ON shift respect to t0

10 250 ns switching ON shift respect to t0

11 375 ns switching ON shift respect to t0

#### 7.3.35 Global configuration register for GPO driver function (GPOCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	х	х	х	х	х	х	х	х	х	Х	х	х	GPO2LS	GP01LS	GPOOLS
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3PO2LS	3PO1LS	SPOOLS

**ID**: 42

Type: RW

**Read:** 4200

Write: 0084

POR WSM SSM

GPOxLS 0 0 GPO driver configuration bit

Updated by SSM RESET or SPI write

- 0 High-side Driver configuration for GPOx (ER\_BOOST\_OK is required to enable GPO as HS)
- 1 Low-side Driver configuration for GPOx (ER\_BOOST\_OK is not required to enable GPO as LS)

# 7.3.36 GPOx control register (GPOCTRLx)

Channel 0 (GPOCTRL0) Channel 1 (GPOCTRL1) Channel 2 (GPOCTRL2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	Х	х	х	х	х	Х	Х	х	Х			GPOxF	WM[5	:0]	
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0		(	GPOxF	WM[5	:0]	

**ID**: 43 (GPOCTRL0)

44 (GPOCTRL1) 45 (GPOCTRL2)

Type: RW

Read: 4300 (GPOCTRL0)

4400 (GPOCTRL1) 4500 (GPOCTRL2)

Write: 0086 (GPOCTRL0)

0088 (GPOCTRL1) 008A (GPOCTRL2)

POR WSM SSM

GPOxPWM 000000 000000 000000 6 bit value for PWM% with scaling of 1.6% per count

Updated by SSM\_RESET or SPI write

#### 7.3.37 GPO fault status register (GPOFLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO	GPO2DISABLE	GP01DISABLE	GPOODISABLE	0	GPOS_NOT_CONF	GPO2TEMP	GPO2LIM	GPOZONOPN	GPO2OFFOPN	GP02SH0RT	GPO1TEMP	GP01LIM	GP010NOPN	GPO10FF0PN	GP01SH0RT	GPOOTEMP	GPOOLIM	GPO0ONOPN	GPO00FFOPN	GP00SHORT

**ID**: 46

Type: R

**Read:** 4600

Write: -

POR NSM SSM

GPO2DISABLE 1 1 1 GPO 2 disable state

0 GPO enable to work

1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)

GPO1DISABLE 1 1 1 GPO 1 disable state

0 GPO enable to work

1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)

GPO0DISABLE 1 1 1 GPO 0 disable state

0 GPO enable to work

1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)

GPOS\_NOT\_CONF 1 1 1 GPOs configuration status

0 GPOs configured (activation is permitted)

1 GPOs not yet configured (activation is denied)

GPO2TEMP 0 0 GPO 2Thermal Fault

Cleared as reported in GPO-Over Temp diagram, set by detection circuit

0 Fault not detected

1 Fault detected

GPO2LIM	0	0	0	GPO 2 Current Limit Flag  Cleared by SSM_RESET or SPI read, set by detection circuit while ON  0 Fault not detected  1 Fault detected
GPO2ONOPN	0	0	0	GPO 2 Open Detection  Cleared by SSM_RESET or SPI read, set by detection circuit while ON  0 Fault not detected  1 Fault detected
GPO2OFFOPN	0	0	0	GPO 2 Open detection in OFF condition  Cleared by SSM_RESET or SPI read, set by detection circuit while OFF  0 Fault not detected  1 Fault detected
GPO2SHORT	0	0	0	GPO 2 Short Detection in OFF condition (short to battery in HS mode, short to ground in LS mode)  Cleared by SSM_RESET or SPI read, set by detection circuit while OFF  0 Fault not detected  1 Fault detected
GPO1TEMP	0	0	0	GPO 1 Thermal Fault  Cleared as reported in GPO-Over Temp diagram, set by detection circuit  0 Fault not detected  1 Fault detected
GPO1LIM	0	0	0	GPO 1 Current Limit Flag  Cleared by SSM_RESET or SPI read, set by detection circuit while ON  0 Fault not detected  1 Fault detected
GPO1ONOPN	0	0	0	GPO 1 Open Detection  Cleared by SSM_RESET or SPI read, set by detection circuit while ON  0 Fault not detected  1 Fault detected
GPO10FFOPN	0	0	0	GPO 1 Open detection in OFF condition  Cleared by SSM_RESET or SPI read, set by detection circuit while OFF  0 Fault not detected  1 Fault detected

118/280 DS11615 Rev 2



**GPO1SHORT** GPO 1 Short Detection in OFF condition (short to battery in HS mode, short to ground in LS mode) Cleared by SSM RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected 0 GPO 0 Thermal Fault **GPOOTEMP** 0 Cleared as reported in GPO-Over Temp diagram, set by detection circuit 0 Fault not detected 1 Fault detected **GPO0LIM** 0 GPO 0 Current Limit Flag 0 Cleared by SSM\_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected **GPO00NOPN** 0 GPO 0 Open Detection OK Cleared by SSM\_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected **GPO00FFOPN** 0 0 GPO 0 Open detection in OFF condition Cleared by SSM\_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected **GPO0SHORT** 0 GPO 0 Short Detection in OFF condition (short to battery in HS mode, short 0 to ground in LS mode) Cleared by SSM\_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected

# 7.3.38 Wheel speed sensor test request register (WSS\_TEST)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	х	х	х	Х	х	х			WSS	SSEL	[6:0]			Х	WSSTP
MISO	0	0	0	0	0	0	0	0	0	0	0			WSS	SSEL	[6:0]			х	NSSTP

 ID:
 48

 Type:
 RW

 Read:
 4800

 Write:
 0090

POR WSM SSM

WSSSEL [6:0] 000000 000000 000000 Wheel Speed Sensor Selection - code below uniquely selects one of the four WSx outputs to place a static output level on

1010011 WSS Test Mode for WS3 Output 1010101 WSS Test Mode for WS2 Output 1011001 WSS Test Mode for WS1 Output 1010110 WSS Test Mode for WS0 Output all other WSS Test Mode disabled

WSSTP 0 0 0 WSx Output Test Value

1 Output for selected WSx set 'high' 0 Output for selected WSx set 'low'

#### 7.3.39 PSI5/WSS configuration register for channel x (RSCRx)

PSI5/WSS configuration register for channel 0 (RSCR0) PSI5/WSS configuration register for channel 1 (RSCR1 PSI5/WSS configuration register for channel 2 (RSCR2) PSI5/WSS configuration register for channel 3 (RSCR3

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		REDUCED_RANGE	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	FIX_THRESH	TSxDIS	BLKTxSEL		WSFI	LT[3:0]		RSPTEN	AVG/SSDIS			STS[3:0]	
MISO	0	0	0	0	REDUCED_RANGE	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	FIX_THRESH	TSxDIS	BLKTxSEL		WSFI	LT[3:0]		RSPTEN	AVG/SSDIS			STS[3:0]	

**ID**: 4A (RSCR0)

4B (RSCR1)

4C (RSCR2)

4D (RSCR3)

Type: RW

Read: 4A00 (RSCR0)

4B00 (RSCR1)

4C00 (RSCR2)

4D00 (RSCR3)

**Write:** 0094 (RSCR0)

0096 (RSCR1) 0098 (RSCR2) 009B (RSCR3)

POR WSM SSM

#### **PSI5** configured channel

REDUCED\_RANGE 0 0 Tracking speed of base and delta current

- 0 Fast tracking of Ibase if rx\_sat\_pre\_filt is low; Slow tracking otherwise. Fast tracking of Idelta if rx\_sat\_pre\_filt is high; Blocked otherwise.
- 1 Fast tracking of Ibase if current is less than (Ibase+(Idelta/4)); Slow tracking otherwise. Fast tracking of Idelta if current is higher than (top current -(Idelta/4)); Slow otherwise.

0 Tracking enable of base and delta current during message transmission BLOCK\_CURR\_IN\_MSG 0 0 0 lbase tracking is enabled during blanking and after start bits recognition. Idelta tracking is disabled during blanking and enabled after start bits recognition. 1 Ibase tracking is enabled during blanking and disabled after start bits recognition. Idelta tracking is disabled during blanking and enabled after start bits recognition PERIOD\_MEAS\_DISABLE 0 0 Disabling of start bits period measure to decode following bits 0 Period is measured 1 Period is not measured (default is used) 0 PSI5 selection of fixed or auto adaptive thresholds FIX\_THRESH 0 0 0 auto adaptive threshold 1 fixed threshold (threshold is latched when this bit is set to high, we recommend to set this bit before enabling of the interface) 0 Time Slot Control Disable **TSxDIS** 0 0 Slot control enabled 1 Slot control disabled **BLKTxSEL** 0 Blanking Time Selection 0 Blanking time = 5ms 1 Blanking time = 10ms WSFILT[3:0] 0010 0010 0010 Wheel speed filter time selection 189k: 125k: (16+x)\*Tosc (24+x)\*Tosc Tosc=1/16MHz **RSPTEN** 0 Pass Through mode Enable 0 0 Off 1 On AVG/SSDIS 0 0 Current average enable during message transmission 0 Off (base and delta work as configured with bits 12, 14, 15) 1 On: base is freezed during data message and during blanking time and delta is averaged during message (fcut of the filter=2500 Hz) while is freezed

122/280 DS11615 Rev 2

during blanking time.



STSx[3:0] 0000 0000 0000 Sensor Type Selection

0000 Synchronous PSI5, parity, 8-bit, 125k (P8P-500/3L) 0001 Synchronous PSI5, parity, 8-bit, 189k (P8P-500/3H) 0010 Synchronous PSI5, parity, 10-bit, 125k (P10P-500/3L) 0011 Synchronous PSI5, parity, 10-bit, 189k (P10P-500/3H) 0100 unused (default automatically selected) 0101 unused (default automatically selected) 0110 unused (default automatically selected) 0111 unused (default automatically selected) 1000 NA 1001 NA 1010 NA 1011 NA 1100 unused (default automatically selected) 1101 unused (default automatically selected) 1110 unused (default automatically selected) 1111 unused (default automatically selected) Wheel speed configured channel REDUCED RANGE 0 Tracking speed of base and delta current X NA BLOCK CURR IN MSG 0 0 Tracking enable of base and delta current during message transmission X NA PERIOD\_MEAS\_DISABLE 0 0 Disabling of start bits period measure to decode following bits X NA FIX\_THRESH 0 0 0 PSI5 selection of fixed or auto adaptive thresholds 0 auto adaptive threshold 1 fixed thresholds (configured through SPI registers) **TSxDIS** 0 Time Slot Control Disable 0 X NA **BLKTxSEL** Blanking Time Selection 0 X NA WSFILT[3:0] 0010 0010 0010 Wheel speed filter time selection (500ns per bit) 0000 8 us --- 500ns/bit 1111 15.5µs:

DS11615 Rev 2 123/280

**RSPTEN** 0 Pass Through mode Enable (only for PWM 2-edges sensors) 0 0 0 Off 1 On AVG/SSDIS 0 WSx output pulses disabled in case of Standstill condition 0 (valid only for PWM Encoded 2 edges sensors) 0 WSx enabled during Standstill 1 WSx disabled during Standstill STSx[3:0] 0000 0000 0000 Sensor Type Selection 0000 NA 0001 NA 0010 NA 0011 NA 0100 unused (default automatically selected) 0101 unused (default automatically selected) 0110 unused (default automatically selected) 0111 unused (default automatically selected) 1000 Two-Level, Standard 1001 Three-Level, VDA 1010 PWM Encoded, 2-Level, 2 edges/tooth 1011 PWM Encoded, 2-Level, 1 edge/tooth 1100 unused (default automatically selected) 1101 unused (default automatically selected) 1110 unused (default automatically selected)

1111 unused (default automatically selected)

# 7.3.40 Remote sensor control register (RSCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	х	х	х	х	х	х	х	CH3EN	SYNC3E	CHZEN	SYNC2E	CH1EN	SYNC1E	CHOEN	SYNCOE
MISO	0	0	0	0	0	0	0	0	0	0	0	0	CH3EN	SYNC3E	CH2EN	SYNC2E	CH1EN	SYNC1E	CHOEN	SYNCOE

 ID:
 4E

 Type:
 R/W

 Read:
 4E00

 Write:
 009C

POR WSM SSM

CHxEN 0 0 Channel x Output enable

Updated by SSM\_RESET or SPI write

0 Off

1 On

SYNCxEN 0 0 Channel x Sync Pulse Enable

0 Off

1 On

# 7.3.41 WSS Threshold configuration register 1 (RS\_AUX\_CONF1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	X													
MISO	0	0	0	0	0	0	0	0	0	0	0	0		١	WSS_	LOW_	THRES	SH [7:0	]	

**ID**: 64

**Type**: R/W **Read**: 6400

Write: 00C8

POR WSM SSM

WSS\_LOW\_THRESH [7:0] \$33 \$33 \$33 Low threshold setting in case of fixed threshold is selected (93,75  $\mu$ A +/-9% each LSB). Low threshold = (\$36+WSS\_LOW\_THRESH)\*93,75  $\mu$ A)

## 7.3.42 WSS Threshold configuration register 2 (RS\_AUX\_CONF2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	X X X X WSS_LOW_THRESH [7:0]											
MISO	0	0	0	0	0	0	0	0	0	0	0	0		١	NSS_	LOW_	THRES	SH [7:0	)]	

**ID**: 65

 Type:
 R/W

 Read:
 6500

 Write:
 00CB

POR WSM SSM

WSS\_LOW\_THRESH [7:0] \$34 \$34 \$34 Delta threshold setting in case of fixed threshold is selected (93,75  $\mu$ A +/-9% each LSB).

High threshold =

(\$6C+WSS\_LOW\_THRESH+WSS\_OFFSET\_THRESH)\*93,75 μA)

#### 7.3.43 Safing algorithm configuration register (SAF\_ALGO\_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		NO_DATA	х		F					ARMP_TH			SUB_VAL			ADD_VAL	
MISO	0	0	0	0	NO_DATA	0		i					ARMP_TH			SUB_VAL			ADD_VAL	

**ID**: 66

Type: R/W

Read: 6600

Write: 00CC

POR WSM SSM

NO\_DATA 0 0 0 Event counter no data select

Updated by SSM\_RESET or SPI write while in DIAG state

- 0 Event counter reset to 0 if CC=0 or (ABS value of response > limit determined by LIM\_SELx) and LIM\_ENx=1 when SPI read of SAF\_CC bit is performed (end of sample cycle)
- 1 Event counter decremented by SUB\_VAL if CC=0 or (ABS value of response > limit determined by LIM\_SELx) and LIM\_ENx=1 when SPI read of SAF\_CC bit is performed (end of sample cycle)

ARMN\_TH 0011 0011 0011 Negative event counter threshold to assert arming

Updated by SSM RESET or SPI write while in DIAG state

0000 Negative event counter disabled

ARMP\_TH 0011 0011 0011 Positive event counter threshold to assert arming

Updated by SSM\_RESET or SPI write while in DIAG state

0000 Positive event counter disabled

SUB\_VAL 011 011 Decremental step size of the event counter

Updated by SSM\_RESET or SPI write while in DIAG state

ADD\_VAL 001 001 lncremental step size of the event counter

Updated by SSM\_RESET or SPI write while in DIAG state

# 7.3.44 Arming signals register (ARM\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO	0	0	0	0	0	0	0	0	0	0	PSINHINT	PSINH_EXP_TIME	ACL_PIN_STATE	ACL_VALID	ARMINT_4	ARMINT_3	ARMINT2	ARMINT_1	0	0

**ID**: 6A

Type: R

Read: 6A00

Write: -

POR WSM SSM

ARMINT\_x - - - State of armint signals

Updated per Safing Engine output logic diagram in case of internal safing engine otherwise is the echo of ARMx pins

ACL\_VALID 0 0 0 Valid ACL detection

0 Cleared when ACL\_BAD=2

1 Set when ACL\_GOOD=3

ACL\_PIN\_STATE - - - Echo of ACL pin

PSINH\_EXP\_TIME 0 0 0 State of PSINH expiration timer

0 If timer is 0

1 If timer is counting

PSINHINT - - State of PSINHINT signal

Updated per PSINH output logic diagram in case of internal engine otherwise is the echo of PSINH pin inverted

#### 7.3.45 ARMx assignment registers to specific Loops (LOOP\_MATRIX\_ARMx)

Assignment of ARM1 to specific loops (LOOP\_MATRIX\_ARM1) Assignment of ARM2 to specific loops (LOOP\_MATRIX\_ARM2) Assignment of ARM3 to specific loops (LOOP\_MATRIX\_ARM3) Assignment of ARM4 to specific loops (LOOP\_MATRIX\_ARM4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		х	х	х	х	ARMx_LB	ARMx_LA	ARMx_L9	ARMx_L8	ARMx_L7	ARMx_L6	ARMx_L5	ARMx_L4	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0
MISO	0	0	0	0	0	0	0	0	ARMx_LB	ARMx_LA	ARMx_L9	ARMx_L8	ARMx_L7	ARMx_L6	ARMx_L5	ARMx_L4	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0

**ID**: 6E (LOOP\_MATRIX\_ARM1)

6F (LOOP\_MATRIX\_ARM2) 70 (LOOP\_MATRIX\_ARM3) 71 (LOOP\_MATRIX\_ARM4)

Type: RW

Read: 6E00 (LOOP\_MATRIX\_ARM1)

6F00 (LOOP\_MATRIX\_ARM2) 7000 (LOOP\_MATRIX\_ARM3) 7100 (LOOP\_MATRIX\_ARM4)

Write: 00DC (LOOP\_MATRIX\_ARM1)

00DE (LOOP\_MATRIX\_ARM2) 00E0 (LOOP\_MATRIX\_ARM3) 00E2 (LOOP\_MATRIX\_ARM4)

POR WSM SSM

ARMx\_Ly 0 0 Configures ARMx for Loop\_y

Updated by SSM\_RESET or SPI write while in DIAG state

- 0 ARMx signal is not associated with Loopy
- 1 ARMx signal is associated with Loopy

## 7.3.46 ARMx enable pulse stretch timer status (AEPSTS\_ARMx)

ARM1 enable pulse stretch timer status (AEPSTS\_ARM1) ARM2 enable pulse stretch timer status (AEPSTS\_ARM2) ARM3 enable pulse stretch timer status (AEPSTS\_ARM3) ARM4 enable pulse stretch timer status (AEPSTS\_ARM4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO	0	0	0	0	0	0	0	0	0	0				Т	mer C	ount[9	:0]			

**ID**: 73 (AEPSTS ARM1)

74 (AEPSTS\_ARM2) 75 (AEPSTS\_ARM3) 76 (AEPSTS\_ARM4)

Type: R

Read: 7300 (AEPSTS\_ARM1)

7400 (AEPSTS\_ARM2) 7500 (AEPSTS\_ARM3) 7600 (AEPSTS\_ARM4)

Write: -

POR VSM SSM

Timer Count \$000 \$000 \$000 10-bit ARMing Enable Pulse Stretcher timer value

Cleared by SSM\_RESET

Loaded with initial value based on ARMx bit and DWELL[1:0] of SAF\_CONTROL\_y while safing is met for record y provided current value is < DWELL[1:0] value

Decremented every 2ms while > 0

Contains remaining pulse stretcher timer value

# 7.3.47 Passenger inhibit upper threshold for DC sensor 0 (PADTHRESH\_HI)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	х	X PADTHRESH_HI										
MISO	0	0	0	0	0	0	0	0	0	0				P	ADTHI	RESH_	HI			

**ID:** 78

Type: RW

**Read:** 7800 **Write:** 00F0

POR WSM

PADTHRESH\_HI \$000 \$000 \$000 Upper threshold - measurements above this upper value will assert the PSINH signal and deactivate loops identified in the PSINH mask

## 7.3.48 Passenger inhibit lower threshold for DC sensor 0 (PADTHRESH\_LO)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	Х	Х				PA	DTHF	RESH_	LO			
MISO	0	0	0	0	0	0	0	0	0	0				PA	DTHF	RESH_	LO			

**ID**: 79

Type: RW

**Read:** 7900

Write: 00F2

POR NSM SSM

PADTHRESH\_LO \$3FF \$3FF Lower threshold - measurements below this lower value will assert the PSINH signal and deactivate loops identified in the PSINH mask

# 7.3.49 Assignment of PSINH signal to specific Loop(s) (LOOP\_MATRIX\_PSINH)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MOSI			-		Х	х	X	х	PSINH_LB	PSINH_LA	PSINH_L9	PSINH_L8	PSINH_L7	PSINH_L6	PSINH_L5	PSINH_L4	ESINH_L3	PSINH_L2	PSINH_L1	PSINH_L0	
MISO	0	0	0	0	0	0	0	0	SINH_LB	SINH_LA	PSINH_L9	PSINH_L8	PSINH_L7	PSINH_L6	PSINH_L5	PSINH_L4	PSINH_L3	PSINH_L2	PSINH_L1	PSINH_L0	

 ID:
 7A

 Type:
 RW

 Read:
 7A00

 Write:
 00F4

POR WSM SSM

PSINH\_Ly 0 0 Configures PSINH for Loop\_y

0 PSINH signal is not associated with Loopy1 PSINH signal is associated with Loopy

# 7.3.50 Safing records enable register (SAF\_ENABLE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		EN_SAF16	EN_SAF15	EN_SAF14	EN_SAF13	EN_SAF12	EN_SAF11	EN_SAF10	EN_SAF9	EN_SAF8	EN_SAF7	EN_SAF6	EN_SAF5	EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1
MISO	0	0	0	0	EN_SAF16	EN_SAF15	EN_SAF14	EN_SAF13	EN_SAF12	EN_SAF11	EN_SAF10	EN_SAF9	EN_SAF8	EN_SAF7	EN_SAF6	EN_SAF5	EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1

**ID**: 7F

Type: RW
Read: 7F00
Write: 00FE

POR WSM

EN\_SAFx Safing Record enable

Updated by SSM\_RESET or SPI write

0 Disable 1 Enable

#### 7.3.51 Safing records request mask registers (SAF\_REQ\_MASK\_x)

Safing record request mask for record 1 (SAF REQ MASK 1) Safing record request mask for record 2 (SAF\_REQ\_MASK\_2) Safing record request mask for record 3 (SAF\_REQ\_MASK\_3) Safing record request mask for record 4 (SAF REQ MASK 4) Safing record request mask for record 5 (SAF\_REQ\_MASK\_5) Safing record request mask for record 6 (SAF\_REQ\_MASK\_6) Safing record request mask for record 7 (SAF\_REQ\_MASK\_7) Safing record request mask for record 8 (SAF\_REQ\_MASK\_8) Safing record request mask for record 9 (SAF\_REQ\_MASK\_9) Safing record request mask for record 10 (SAF REQ MASK 10) Safing record request mask for record 11 (SAF\_REQ\_MASK\_11) Safing record request mask for record 12 (SAF REQ MASK 12) Safing record request mask for record 13 (SAF\_REQ\_MASK\_13) Safing record request mask for record 14\_pt1 (SAF\_REQ\_MASK\_14)\_pt1 Safing record request mask for record 14 pt2 (SAF REQ MASK 14) pt2 Safing record request mask for record 15\_pt1 (SAF\_REQ\_MASK\_15)\_pt1 Safing record request mask for record 15\_pt2 (SAF\_REQ\_MASK\_15)\_pt2 Safing record request mask for record 16\_pt1 (SAF\_REQ\_MASK\_16)\_pt1 Safing record request mask for record 16\_pt2 (SAF\_REQ\_MASK\_16)\_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-								SAF_F	REQ_I	MASKx[	15:0]						
MISO	0	0	0	0							SAF_F	REQ_I	MASKx[	15:0]						

ID: 80 (SAF REQ MASK 1) 81 (SAF REQ MASK 2) 82 (SAF REQ MASK 3) 83 (SAF REQ MASK 4) 84 (SAF REQ MASK 5) 85 (SAF REQ MASK 6) 86 (SAF REQ MASK 7) 87 (SAF\_REQ\_MASK\_8) 88 (SAF\_REQ\_MASK\_9) 89 (SAF REQ MASK 10) 8A (SAF REQ MASK 11) 8B (SAF REQ MASK 12) 8C (SAF REQ MASK 13) 8D (SAF REQ MASK 14 pt1 8E (SAF REQ MASK 14 pt2) 8F (SAF\_REQ\_MASK\_15\_pt1) 90 (SAF REQ MASK 15 pt2) 91 (SAF REQ MASK 16 pt1) 92 (SAF\_REQ\_MASK\_16\_pt2)

Type: RW

**Read:** 8000 (SAF\_REQ\_MASK\_1) 8100 (SAF\_REQ\_MASK\_2)

577

DS11615 Rev 2 133/280

```
8200 (SAF REQ MASK 3)
8300 (SAF_REQ_MASK_4)
8400 (SAF_REQ_MASK_5)
8500 (SAF REQ MASK 6)
8600 (SAF_REQ_MASK_7)
8700 (SAF_REQ_MASK_8)
8800 (SAF_REQ_MASK_9)
8900 (SAF_REQ_MASK_10)
8A00 (SAF_REQ_MASK_11)
8B00 (SAF_REQ_MASK_12)
8C00 (SAF REQ MASK 13)
8D00 (SAF REQ MASK 14 pt1
8E00 (SAF_REQ_MASK_14_pt2)
8F00 (SAF REQ MASK 15 pt1)
9000 (SAF_REQ_MASK_15_pt2)
9100 (SAF_REQ_MASK_16_pt1)
9200 (SAF_REQ_MASK_16_pt2)
8000 (SAF REQ MASK 1)
8002 (SAF_REQ_MASK_2)
8004 (SAF_REQ_MASK_3)
8006 (SAF_REQ_MASK_4)
8008 (SAF_REQ_MASK_5)
800A (SAF_REQ_MASK_6)
800C (SAF REQ MASK 7)
800E (SAF REQ MASK 8)
8010 (SAF REQ MASK 9)
8012 (SAF REQ MASK 10)
8014 (SAF REQ MASK 11)
8016 (SAF_REQ_MASK_12)
8018 (SAF_REQ_MASK_13)
801A (SAF_REQ_MASK_14_pt1
801C (SAF REQ MASK 14 pt2)
801E (SAF_REQ_MASK_15_pt1)
8020 (SAF REQ MASK 15 pt2)
8022 (SAF REQ MASK 16 pt1)
8424 (SAF REQ MASK 16 pt2)
```

Write:

SAF\_REQ\_MASKx[15:0] \$0000\$0000\$0000\$afing Request Mask for safing record x - 16-bit request mask that is bitwise ANDed with MOSI data from SPI monitor

Updated by SSM\_RESET or SPI write while in DIAG state

134/280 DS11615 Rev 2



### 7.3.52 Safing records request target registers (SAF\_REQ\_TARGET\_x)

Safing record request mask for record 1 (SAF REQ TARGET 1) Safing record request mask for record 2 (SAF\_REQ\_TARGET\_2) Safing record request mask for record 3 (SAF\_REQ\_TARGET\_ Safing record request mask for record 4 (SAF REQ TARGET 4) Safing record request mask for record 5 (SAF\_REQ\_TARGET\_5) Safing record request mask for record 6 (SAF\_REQ\_TARGET\_6) Safing record request mask for record 7 (SAF\_REQ\_TARGET\_7) Safing record request mask for record 8 (SAF\_REQ\_TARGET\_8) Safing record request mask for record 9 (SAF\_REQ\_TARGET\_9) Safing record request mask for record 10 (SAF REQ TARGET 10) Safing record request mask for record 11 (SAF\_REQ\_TARGET\_11) Safing record request mask for record 12 (SAF\_REQ\_TARGET\_12) Safing record request mask for record 13 (SAF\_REQ\_TARGET\_13) Safing record request mask for record 14\_pt1 (SAF\_REQ\_TARGET\_14)\_pt1 Safing record request mask for record 14 pt2 (SAF REQ TARGET 14) pt2 Safing record request mask for record 15\_pt1 (SAF\_REQ\_TARGET\_15)\_pt1 Safing record request mask for record 15 pt2 (SAF\_REQ\_TARGET\_15) pt2 Safing record request mask for record 16\_pt1 (SAF\_REQ\_TARGET\_16)\_pt1 Safing record request mask for record 16\_pt2 (SAF\_REQ\_TARGET\_16)\_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	- SAF_REQ_TARGET[15:0]																			
MISO	0	0	0	0		SAF_REQ_TARGET[15:0]														

```
ID:
               93 (SAF REQ TARGET 1)
               94 (SAF REQ TARGET 2)
               95 (SAF REQ TARGET 3)
               96 (SAF REQ TARGET 4)
               97 (SAF REQ TARGET 5)
               98 (SAF REQ TARGET 6)
               99 (SAF REQ TARGET 7)
               9A (SAF_REQ_TARGET_8)
              9B (SAF_REQ_TARGET_9)
               9C (SAF_REQ_TARGET_10)
               9D (SAF REQ TARGET 11)
               9E (SAF REQ TARGET 12)
               9F (SAF REQ TARGET 13)
              A0 (SAF REQ TARGET 14 pt1
              A1 (SAF_REQ_TARGET_14_pt2)
              A2 (SAF_REQ_TARGET_15_pt1)
              A3 (SAF_REQ_TARGET_15_pt2)
              A4 (SAF REQ TARGET 16 pt1)
              A5 (SAF_REQ_TARGET_16_pt2)
```

9300 (SAF\_REQ\_TARGET\_1) 9400 (SAF\_REQ\_TARGET\_2)

RW

57

Type:

Read:

```
9500 (SAF_REQ_TARGET_3)
9600 (SAF_REQ_TARGET_4)
9700 (SAF_REQ_TARGET_5)
9800 (SAF REQ TARGET 6)
9900 (SAF_REQ_TARGET_7)
9A00 (SAF_REQ_TARGET_8)
9B00 (SAF_REQ_TARGET_9)
9C00 (SAF_REQ_TARGET_10)
9D00 (SAF_REQ_TARGET_11)
9E00 (SAF_REQ_TARGET_12)
9F00 (SAF REQ TARGET 13)
A000 (SAF REQ TARGET 14 pt1
A100 (SAF_REQ_TARGET_14_pt2)
A200 (SAF REQ TARGET 15 pt1)
A300 (SAF_REQ_TARGET_15_pt2)
A400 (SAF_REQ_TARGET_16_pt1)
A500 (SAF_REQ_TARGET_16_pt2)
8026 (SAF REQ TARGET 1)
8028 (SAF_REQ_TARGET_2)
802A (SAF_REQ_TARGET_3)
802C (SAF_REQ_TARGET_4)
802E (SAF_REQ_TARGET_5)
8030 (SAF_REQ_TARGET_6)
8032 (SAF_REQ_TARGET_7)
8034 (SAF REQ TARGET 8)
8036 (SAF REQ TARGET 9)
8038 (SAF REQ TARGET 10)
803A (SAF REQ TARGET 11)
803C (SAF_REQ_TARGET_12)
803E (SAF_REQ_TARGET_13)
8040 (SAF_REQ_TARGET_14_pt1
8042 (SAF REQ TARGET 14 pt2)
8044 (SAF_REQ_TARGET_15_pt1)
8246 (SAF REQ TARGET 15 pt2)
8048 (SAF REQ TARGET
                      16 pt1)
804A (SAF REQ TARGET 16 pt2)
```

Write:

SAF\_REQ\_TARGET[15:0 \$0000\$0000\$0000\$Safing Request target for safing record x - 16-bit request target that is compared to the bit-wise AND result of the SAF\_REQ\_MASKx and MOSI data from SPI monitor

Updated by SSM\_RESET or SPI write while in DIAG state

136/280 DS11615 Rev 2

#### 7.3.53 Safing records response mask registers (SAF RESP MASK x)

```
Safing record response mask for record 1 (SAF RESP MASK 1)
Safing record response mask for record 2 (SAF_RESP_MASK_2)
Safing record response mask for record 3 (SAF_RESP_MASK_3)
Safing record response mask for record 4 (SAF RESP MASK 4)
Safing record response mask for record 5 (SAF_RESP_MASK_5)
Safing record response mask for record 6 (SAF RESP MASK 6
Safing record response mask for record 7 (SAF_RESP_MASK_7))
Safing record response mask for record 8 (SAF_RESP_MASK_8)
Safing record response mask for record 9 (SAF_RESP_MASK_9)
Safing record response mask for record 10 (SAF RESP MASK 10)
Safing record response mask for record 11 (SAF_RESP_MASK_11)
Safing record response mask for record 12 (SAF RESP MASK 12)
Safing record response mask for record 13 (SAF_RESP_MASK_13)
Safing record response mask for record 14_pt1 (SAF_RESP_MASK_14_pt1)
Safing record response mask for record 14 pt2 (SAF RESP MASK 14 pt2)
Safing record response mask for record 15_pt1 (SAF_RESP_MASK_15_pt1)
Safing record response mask for record 15_pt2 (SAF_RESP_MASK_14_pt2)
Safing record response mask for record 16_pt1 (SAF_RESP_MASK_16_pt1)
Safing record response mask for record 16_pt2 (SAF_RESP_MASK_16_pt2)
```

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	SAF_RESP_MASKx[15:0]																			
MISO	0	0	0	0		SAF_RESP_MASKx[15:0]														

```
ID:
              A6 (SAF RESP MASK 1)
              A7 (SAF RESP MASK 2
              A8 (SAF RESP MASK 3
              A9 (SAF RESP MASK 4
              AA (SAF RESP MASK 5
              AB (SAF RESP MASK 6
              AC (SAF_RESP_MASK_7
              AD (SAF_RESP_MASK_8
              AE (SAF_RESP_MASK_9
              AF (SAF RESP MASK 10
              B0 (SAF RESP MASK 11
              B1 (SAF RESP MASK 12
              B2 (SAF RESP MASK 13)
              B3 (SAF_RESP_MASK_14_pt1)
              B4 (SAF_RESP_MASK_14_pt2)
              B5 (SAF_RESP_MASK_15_pt1)
              B6 (SAF_RESP_MASK_15_pt2)
```

577

DS11615 Rev 2 137/280

B7 (SAF\_RESP\_MASK\_16\_pt1 B8 (SAF\_RESP\_MASK\_16\_pt2

Type: RW

Read:

Read: A600 (SAF\_RESP\_MASK\_1)

A700 (SAF\_RESP\_MASK\_2 A800 (SAF\_RESP\_MASK\_3 A900 (SAF\_RESP\_MASK\_4 AA00 (SAF\_RESP\_MASK\_5 AB00 (SAF RESP MASK 6 AC00 (SAF\_RESP\_MASK\_7 AD00 (SAF\_RESP\_MASK\_8 AE00 (SAF\_RESP\_MASK\_9 AF00 (SAF\_RESP\_MASK\_10 B000 (SAF RESP MASK 11 B100 (SAF RESP MASK 12 B200 (SAF RESP MASK 13) B300 (SAF\_RESP\_MASK\_14\_pt1) B400 (SAF\_RESP\_MASK\_14\_pt2) B500 (SAF\_RESP\_MASK\_15\_pt1) B600 (SAF\_RESP\_MASK\_15\_pt2) B700 (SAF\_RESP\_MASK\_16\_pt1

B801 (SAF RESP MASK 16 pt1

Write: 804C (SAF\_RESP\_MASK\_1)

804E (SAF\_RESP\_MASK\_2 8050 (SAF\_RESP\_MASK\_3 8052 (SAF\_RESP\_MASK\_4 8054 (SAF\_RESP\_MASK\_5 8056 (SAF\_RESP\_MASK\_6 8058 (SAF\_RESP\_MASK\_7 805A (SAF\_RESP\_MASK\_7 805C (SAF\_RESP\_MASK\_9 805E (SAF\_RESP\_MASK\_10 8060 (SAF\_RESP\_MASK\_11 8062 (SAF\_RESP\_MASK\_11 8064 (SAF\_RESP\_MASK\_12 8064 (SAF\_RESP\_MASK\_13) 8066 (SAF\_RESP\_MASK\_14\_pt1) 8068 (SAF\_RESP\_MASK\_14\_pt2)

806A (SAF\_RESP\_MASK\_15\_pt1) 806C (SAF\_RESP\_MASK\_15\_pt2) 806E (SAF\_RESP\_MASK\_16\_pt1

8070 (SAF\_RESP\_MASK\_16\_pt2

POR WSM

SAF\_RESP\_MASKx[15:0] 0000 0000 0000 Safing Response Mask for safing record x - 16-bit response mask that is bitwise ANDed with MISO data from SPI monitor

16-bit request target that is compared to the bit-wise AND result of the SAF REQ MASKx and MOSI data from SPI

Updated by SSM\_RESET or SPI write while in DIAG state

138/280 DS11615 Rev 2



#### 7.3.54 Safing records response mask registers (SAF\_RESP\_TARGET\_x)

Safing record response target for record 1 (SAF RESP TARGET 1) Safing record response target for record 2 (SAF\_RESP\_TARGET\_2) Safing record response target for record 3 (SAF\_RESP\_TARGET\_3) Safing record response target for record 4 (SAF RESP TARGET 4) Safing record response target for record 5 (SAF\_RESP\_TARGET\_5) Safing record response target for record 6 (SAF\_RESP\_TARGET\_6) Safing record response target for record 7 (SAF\_RESP\_TARGET\_7) Safing record response target for record 8 (SAF\_RESP\_TARGET\_8) Safing record response target for record 9 (SAF\_RESP\_TARGET\_9) Safing record response target for record 10 (SAF RESP TARGET 10) Safing record response target for record 11 (SAF\_RESP\_TARGET\_11) Safing record response target for record 11 (SAF RESP TARGET 12) Safing record response target for record 13 (SAF\_RESP\_TARGET\_13) Safing record response target for record 14\_pt1 (SAF\_RESP\_TARGET\_14)\_pt1 Safing record response target for record 14 pt2 (SAF RESP TARGET 14) pt2 Safing record response target for record 15\_pt1 (SAF\_RESP\_TARGET\_15)\_pt1 Safing record response target for record 15\_pt2 (SAF\_RESP\_TARGET\_15)\_pt2 Safing record response target for record 16\_pt1 (SAF\_RESP\_TARGET\_16)\_pt1 Safing record response target for record 16\_pt2 (SAF\_RESP\_TARGET\_16)\_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	- SAF_RESP_TARGETx[15:0]																			
MISO	0	0	0	0		SAF_RESP_TARGETx[15:0]														

```
ID:
              B9 (SAF RESP TARGET 1)
              BA (SAF RESP TARGET 2
              BB (SAF RESP TARGET 3
              BC (SAF RESP TARGET 4
              BD (SAF_RESP_TARGET_5
              BE (SAF RESP TARGET
              BF (SAF_RESP_TARGET_7
              C0 (SAF_RESP_TARGET_8
              C1 (SAF_RESP_TARGET_9
              C2 (SAF RESP TARGET 10
              C3 (SAF RESP TARGET 11
              C4 (SAF RESP TARGET 12
              C5 (SAF RESP TARGET 13
              C6 (SAF_RESP_TARGET_14_pt1
              C7 (SAF_RESP_TARGET_14_pt2
              C8 (SAF_RESP_TARGET_15_pt1
              C9 (SAF RESP TARGET 15 pt2
              CA (SAF RESP TARGET 16 pt1
              CB (SAF_RESP_TARGET_16_pt2
```

DS11615 Rev 2 139/280

RW

Type:

B900 (SAF RESP TARGET 1) Read: BA00 (SAF\_RESP\_TARGET\_ BB00 (SAF\_RESP\_TARGET\_ BC00 (SAF\_RESP\_TARGET\_4 BD00 (SAF\_RESP\_TARGET\_5 BE00 (SAF\_RESP\_TARGET\_6 BF00 (SAF RESP TARGET 7 C000 (SAF RESP TARGET 8 C100 (SAF\_RESP\_TARGET\_9 C200 (SAF\_RESP\_TARGET\_10 C300 (SAF\_RESP\_TARGET\_ C400 (SAF\_RESP\_TARGET\_12 C500 (SAF\_RESP\_TARGET\_13 C600 (SAF RESP TARGET 14 pt1 C700 (SAF RESP TARGET 14 pt2 C800 (SAF RESP TARGET 15 pt1 C900 (SAF\_RESP\_TARGET\_15\_pt2 CA00 (SAF\_RESP\_TARGET\_16\_pt1 CB00 (SAF\_RESP\_TARGET\_16\_pt2) 8072 (SAF RESP TARGET 1) Write: 8074 (SAF RESP TARGET 2 8076 (SAF RESP TARGET 3 8078 (SAF RESP TARGET 807A (SAF\_RESP\_TARGET] 807C (SAF\_RESP\_TARGET\_6 807E (SAF\_RESP\_TARGET\_ 7 8080 (SAF\_RESP\_TARGET\_8 8082 (SAF RESP TARGET 9 8084 (SAF\_RESP\_TARGET\_10 8086 (SAF RESP TARGET 11 8088 (SAF RESP TARGET 808A (SAF\_RESP\_TARGET\_ 808C (SAF\_RESP\_TARGET\_14\_pt1 808E (SAF\_RESP\_TARGET\_14\_pt2 8090 (SAF RESP TARGET 15 pt1 8092 (SAF RESP TARGET 15 pt2 8094 (SAF\_RESP\_TARGET\_16\_pt1 CB00 (SAF\_RESP\_TARGET\_16\_pt2) SAF\_RESP\_TARGETX[15:0] 0000 0000 0000 Safing Response target for safing record x - 16-bit response target that is compared to the bit-wise AND result of the SAF RESP MASKx and MISO data from SPI monitor

140/280 DS11615 Rev 2

Updated by SSM RESET or SPI write while in DIAG state

#### 7.3.55 Safing records data mask registers (SAF\_DATA\_MASK\_x)

Safing record data mask for record 1 (SAF DATA MASK 1) Safing record data mask for record 2 (SAF\_DATA\_MASK\_2) Safing record data mask for record 3 (SAF\_DATA\_MASK\_3) Safing record data mask for record 4 (SAF DATA MASK 4) Safing record data mask for record 5 (SAF\_DATA\_MASK\_5) Safing record data mask for record 6 (SAF\_DATA\_MASK\_6) Safing record data mask for record 7 (SAF\_DATA\_MASK\_7) Safing record data mask for record 8 (SAF\_DATA\_MASK\_8) Safing record data mask for record 9 (SAF\_DATA\_MASK\_9) Safing record data mask for record 10 (SAF DATA MASK 10) Safing record data mask for record 11 (SAF\_DATA\_MASK\_11) Safing record data mask for record 12 (SAF DATA MASK 12) Safing record data mask for record 13 (SAF\_DATA\_MASK\_13) Safing record data mask for record 14 (SAF\_DATA\_MASK\_14\_pt1) Safing record data mask for record 14 (SAF DATA MASK 14 pt2) Safing record data mask for record 15 (SAF\_DATA\_MASK\_15\_pt1) Safing record data mask for record 15 (SAF\_DATA\_MASK\_15\_pt2) Safing record data mask for record 16 (SAF DATA MASK 16 pt1) Safing record data mask for record 16 (SAF\_DATA\_MASK\_16\_pt2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	- SAF_DATA_MASKx[15:0]																			
MISO	0	0	0	0		SAF_DATA_MASKx[15:0]														

```
ID:
               CC (SAF DATA MASK 1)
               CD (SAF DATA MASK 2)
               CE (SAF_DATA_MASK_3)
               CF (SAF_DATA_MASK_4)
               D0 (SAF_DATA_MASK_5)
               D1 (SAF_DATA_MASK_6)
               D2 (SAF_DATA_MASK_7)
               D3 (SAF_DATA_MASK_8)
               D4 (SAF DATA MASK 9)
               D5 (SAF DATA MASK 10)
               D6 (SAF_DATA_MASK_11)
               D7 (SAF_DATA_MASK_12)
               D8 (SAF_DATA_MASK_13)
               D9 (SAF_DATA_MASK_14_pt1)
               DA (SAF_DATA_MASK_14_pt2)
               DB (SAF DATA MASK 15 pt1)
               DC (SAF_DATA_MASK_15_pt2)
```

DD (SAF\_DATA\_MASK\_16\_pt1) DE (SAF\_DATA\_MASK\_16\_pt2)

Type: RW

Read: CC00 (SAF\_DATA\_MASK\_1)

CD00 (SAF\_DATA\_MASK\_2)
CE00 (SAF\_DATA\_MASK\_3)
CF00 (SAF\_DATA\_MASK\_4)
D000 (SAF\_DATA\_MASK\_5)
D100 (SAF\_DATA\_MASK\_6)
D200 (SAF\_DATA\_MASK\_7)
D300 (SAF\_DATA\_MASK\_8)
D400 (SAF\_DATA\_MASK\_9)
D500 (SAF\_DATA\_MASK\_10)

D600 (SAF\_DATA\_MASK\_11) D700 (SAF\_DATA\_MASK\_12) D800 (SAF\_DATA\_MASK\_13) D900 (SAF\_DATA\_MASK\_14\_pt1) DA00 (SAF\_DATA\_MASK\_14\_pt2) DB00 (SAF\_DATA\_MASK\_15\_pt1)

DC00 (SAF\_DATA\_MASK\_15\_pt2) DD00 (SAF\_DATA\_MASK\_16\_pt1) DE00 (SAF\_DATA\_MASK\_16\_pt2)

Write: 8099 (SAF\_DATA\_MASK\_1)

809A (SAF\_DATA\_MASK\_2)

809C (SAF\_DATA\_MASK\_3)

809E (SAF\_DATA\_MASK\_4)

80A0 (SAF\_DATA\_MASK\_5)

80A2 (SAF\_DATA\_MASK\_6)

80A4 (SAF\_DATA\_MASK\_7)

80A6 (SAF\_DATA\_MASK\_8)

80A8 (SAF\_DATA\_MASK\_9)

80AA (SAF\_DATA\_MASK\_10)

80AC (SAF\_DATA\_MASK\_11)

80AE (SAF\_DATA\_MASK\_12)

80B0 (SAF\_DATA\_MASK\_13)

80B2 (SAF\_DATA\_MASK\_14\_pt1)

80B4 (SAF\_DATA\_MASK\_14\_pt2)

80B6 (SAF\_DATA\_MASK\_15\_pt1)

80B8 (SAF\_DATA\_MASK\_15\_pt2)

80BA (SAF\_DATA\_MASK\_16\_pt1) 80BC (SAF\_DATA\_MASK\_16\_pt2)

\_ \_ \_ \_

POR WSM

SAF\_DATA\_MASKx[15:0] 0000 0000 0000 Safing Data Mask for safing record x - 16-bit data mask that is bit-wise ANDed with MISO data from SPI monitor

Updated by SSM\_RESET or SPI write while in DIAG state

142/280 DS11615 Rev 2



#### 7.3.56 Safing record threshold registers (SAF\_THRESHOLD\_x)

Safing record threshold for record 1 (SAF\_THRESHOLD\_1)
Safing record threshold for record 2 (SAF\_THRESHOLD\_2)
Safing record threshold for record 3 (SAF\_THRESHOLD\_3)
Safing record threshold for record 4 (SAF\_THRESHOLD\_4)
Safing record threshold for record 5 (SAF\_THRESHOLD\_5)
Safing record threshold for record 6 (SAF\_THRESHOLD\_6)
Safing record threshold for record 7 (SAF\_THRESHOLD\_7)
Safing record threshold for record 8 (SAF\_THRESHOLD\_8)
Safing record threshold for record 9 (SAF\_THRESHOLD\_9)
Safing record threshold for record 10 (SAF\_THRESHOLD\_11)
Safing record threshold for record 12 (SAF\_THRESHOLD\_12)
Safing record threshold for record 13 (SAF\_THRESHOLD\_13)
Safing record threshold for record 14 (SAF\_THRESHOLD\_14)
Safing record threshold for record 15 (SAF\_THRESHOLD\_15)
Safing record threshold for record 16 (SAF\_THRESHOLD\_15)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	- SAF_TH										HRES	HOLDx	[15:0]							
MISO	0	0	0	0		SAF_THRESHOLDx[15:0]														

```
ID:
               DF (SAF_THRESHOLD_1)
               E0 (SAF_THRESHOLD_2)
               E1 (SAF THRESHOLD 3)
               E2 (SAF_THRESHOLD_4)
               E3 (SAF_THRESHOLD_5)
               E4 (SAF_THRESHOLD_6)
E5 (SAF_THRESHOLD_7)
               E6 (SAF_THRESHOLD_8)
               E7 (SAF THRESHOLD 9)
               E8 (SAF THRESHOLD 10)
               E9 (SAF THRESHOLD 11)
               EA (SAF_THRESHOLD_12)
               EB (SAF_THRESHOLD_13)
               EC (SAF_THRESHOLD_14)
               ED (SAF_THRESHOLD_15)
               EE (SAF_THRESHOLD_16)
```

Type: RW

Read: DF00 (SAF\_THRESHOLD\_1)
E000 (SAF\_THRESHOLD\_2)
E100 (SAF\_THRESHOLD\_3)
E200 (SAF\_THRESHOLD\_4)
E300 (SAF\_THRESHOLD\_5)
E400 (SAF\_THRESHOLD\_6)
E500 (SAF\_THRESHOLD\_7)

E600 (SAF\_THRESHOLD\_7)

```
E700 (SAF_THRESHOLD_9)
               E800 (SAF_THRESHOLD_10)
               E900 (SAF_THRESHOLD_11)
                EA00 (SAF_THRESHOLD_12)
                EB00 (SAF_THRESHOLD_13)
               EC00 (SAF_THRESHOLD_14)
               ED00 (SAF_THRESHOLD_15)
               EE00 (SAF_THRESHOLD_16)
Write:
                80BE (SAF_THRESHOLD_1)
               80C0 (SAF_THRESHOLD_2)
                80C2 (SAF_THRESHOLD_3)
               80C4 (SAF_THRESHOLD_4)
               80C6 (SAF_THRESHOLD_5)
80C8 (SAF_THRESHOLD_6)
                80CA (SAF_THRESHOLD_7)
                80CC (SAF_THRESHOLD_8)
                80CE (SAF THRESHOLD 9)
                80D0 (SAF THRESHOLD 10)
                80D2 (SAF_THRESHOLD_11)
               80D4 (SAF_THRESHOLD_12)
80D6 (SAF_THRESHOLD_13)
                80D8 (SAF_THRESHOLD_14)
                80DA (SAF_THRESHOLD_15)
                80DB (SAF THRESHOLD 16)
```

SAF\_THRESHOLD\_x \$FFFF \$FFFF \$FFFF Safing threshold for safing record x - 16-bit threshold used for safing data comparison

Updated by SSM\_RESET or SPI write while in DIAG state

144/280 DS11615 Rev 2

## 7.3.57 Safing control x registers (SAF\_CONTROL\_x)

Safing control registers for record 1 (SAF CONTROL 1) Safing control registers for record 2 (SAF\_CONTROL\_2) Safing control registers for record 3 (SAF\_CONTROL\_3) Safing control registers for record 4 (SAF CONTROL 4) Safing control registers for record 5 (SAF\_CONTROL\_5) Safing control registers for record 6 (SAF CONTROL 6) Safing control registers for record 7 (SAF\_CONTROL\_7) Safing control registers for record 8 (SAF\_CONTROL\_8) Safing control registers for record 9 (SAF\_CONTROL\_9) Safing control registers for record 10 (SAF CONTROL 10) Safing control registers for record 11 (SAF\_CONTROL\_11) Safing control registers for record 12 (SAF CONTROL 12) Safing control registers for record 13 (SAF\_CONTROL\_13) Safing control registers for record 14 (SAF\_CONTROL\_14) Safing control registers for record 15 (SAF CONTROL 15) Safing control registers for record 16 (SAF\_CONTROL\_16)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		ARMS	SELx	SPIFLDSELx	LIM SELx	LIM Enx	COMBx	1 12/4	>	ARM4x	ARM3x	ARM2x	ARM1x	(	CSx[2:0	0]	IFx
MISO	0	0	0	0	ARMS	SELx	SPIFLDSELx	LIM SELx	LIM Enx	COMBx	נט. 17. ו		ARM4x	ARM3x	ARM2x	ARM1x	(	CSx[2:0	0]	IFx

**ID:** EF (SAF\_CONTROL\_1) F0 (SAF\_CONTROL\_2)

F0 (SAF\_CONTROL\_2)
F1 (SAF\_CONTROL\_3)
F2 (SAF\_CONTROL\_4)
F3 (SAF\_CONTROL\_5)
F4 (SAF\_CONTROL\_6)
F5 (SAF\_CONTROL\_7
F6 (SAF\_CONTROL\_8)
F7 (SAF\_CONTROL\_9)
F8 (SAF\_CONTROL\_10)
F9 (SAF\_CONTROL\_11)
FA (SAF\_CONTROL\_12)

FB (SAF\_CONTROL\_13) FC (SAF\_CONTROL\_14) FD (SAF\_CONTROL\_15) FE (SAF\_CONTROL\_16)

Type: RW

Read: EF00 (SAF CONTROL 1)

F000 (SAF\_CONTROL\_2) F100 (SAF\_CONTROL\_3) **SPI** interfaces L9680

F200 (SAF\_CONTROL\_4) F300 (SAF\_CONTROL\_5) F400 (SAF\_CONTROL\_6) F500 (SAF CONTROL 7 F600 (SAF\_CONTROL\_8) F700 (SAF\_CONTROL\_9) F800 (SAF\_CONTROL\_10) F900 (SAF\_CONTROL\_11) FA00 (SAF\_CONTROL\_12) FB00 (SAF\_CONTROL\_13) FC00 (SAF CONTROL 14) FD00 (SAF CONTROL 15) FE00 (SAF\_CONTROL\_16) Write: 80DE (SAF\_CONTROL\_1) 80E0 (SAF\_CONTROL\_2) 80E2 (SAF\_CONTROL\_3) 80E4 (SAF CONTROL 4) 80E6 (SAF CONTROL 5) 80E8 (SAF\_CONTROL\_6) 80EA (SAF\_CONTROL\_7 80EC (SAF\_CONTROL\_8) 80EE (SAF\_CONTROL\_9) 80F0 (SAF\_CONTROL\_10) 80F2 (SAF CONTROL 11) 80F4 (SAF CONTROL 12) 80F6 (SAF CONTROL 13) 80F8 (SAF\_CONTROL\_14) 80FA (SAF CONTROL 15) 80FC (SAF\_CONTROL\_16) POR WSM SSM ARMSFI x 00 00 00 ARMINT select for safing recode x - correlates A Updated by SSM\_RESET or SPI write while in DIAG state 00 ARMP OR ARMN 01 ARMP 10 ARMN 11 ARMP OR ARMN **SPIFLDSELx** 0 0 SPI field select for safing record x - determines which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. In case of messages less than 32 bits this bit is don't care. Updated by SSM\_RESET or SPI write while in DIAG state. Updated by SSM RESET or SPI write while in DIAG state

Mask bit-wise AND

- 0 First 16 bits of SPI MISO frame used for Response Mask and Data
- 1 Last 16 bits of SPI MISO frame used for Response Mask and Data Mask bit-wise AND



LIM SELx	0	0	0	Data range limit select for safing record x - When enabled, determines the range limit used for incoming sensor data  Updated by SSM_RESET or SPI write while in DIAG state
				0 8-bit data range limit - incoming  data  >120d is not recognized as valid data
				1 10-bit data range limit - incoming  data  > 480d is not recognized as valid data
LIM Enx	0	0	0	Data range limit enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state
				Data range limit disabled     Data range limit enabled
COMBx	0	0	0	Combine function enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state
				0 Combine function disabled
				1 Combine function enabled
				For record pairs = x,x+1, the comparison for record x uses  data(x) + data(x+1)  and the comparison for record x+1 uses  data(x) - data(x+1)  Record pairs are 1,2; 3,4; 5,6; 7,8; 9,10; 11,12
DWELLx[1:0]	00	00	00	Safing dwell extension time select for safing record x Updated by SSM_RESET or SPI write while in DIAG state
				00 2048 ms 01 256 ms 10 32 ms 11 0 ms
ARM4x	0	0	0	ARM4INT select for safing record x - correlates safing result to ARM4INT Updated by SSM_RESET or SPI write while in DIAG state
				0 Safing record x not assigned to ARM4INT 1 Safing record x assigned to ARM4INT
ARM3x	0	0	0	ARM3INT select for safing record x - correlates safing result to ARM3INT Updated by SSM_RESET or SPI write while in DIAG state
				0 Safing record x not assigned to ARM3INT 1 Safing record x assigned to ARM3INT
ARM2x	0	0	0	ARM2INT select for safing record x - correlates safing result to ARM2INT Updated by SSM_RESET or SPI write while in DIAG state
				0 Safing record x not assigned to ARM2INT 1 Safing record x assigned to ARM2INT
ARM1x	0	0	0	ARM1INT select for safing record x - correlates safing result to ARM1INT Updated by SSM_RESET or SPI write while in DIAG state

147/280

SPI interfaces L9680

0 Safing record x not assigned to ARM1INT

1 Safing record x assigned to ARM1INT

CSx[2:0] 000 000 SPI Monitor CS select for safing record x

Updated by SSM\_RESET or SPI write while in DIAG state

000 None selected for record x

001 SAF\_CS0 selected for record x

010 SAF\_CS1 selected for record x

011 SAF CS2 selected for record x

100 SAF\_CS3 selected for record x

101 CS RS selected for record x

110 None selected for record x

111 None selected for record x

IFx 0 0 SPI format select for safing record x - selects response protocol for SPI monitor

Updated by SSM RESET or SPI write while in DIAG state

0 Out of frame response for record x

1 In Frame response for record x

# 7.3.58 Safing record compare complete register (SAF\_CC)

		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	MOSI			-		х	Х	х	х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
	MISO	0	0	0	0	CC_16	CC_15	CC_14	CC_13	CC_12	CC_11	CC_10	6_000	8_ ) )	0CC_7	9_၁၁0	0CC_5	CC_4	c3	CC_2	CC_1

ID: FF

Type: R

Read: FF00

Write: -

POR WSM

CC\_xx 0 0 0 Indicates compare complete status of each of the 16 safing records, and defines the end of the sample cycle for safing

Cleared by SSM\_RESET or upon SPI read, set by safing engine when request, response mask and target registers match the incoming SPI frame

0 Compare not completed for record x

1 Compare completed for record x



# 7.4 Remote sensor SPI register map

The Remote Sensor SPI interface consists of twelve 32-bit read registers (one for each logical channel) to allow for access to decoded sensor data and fault registers. The registers are addressed by the read register ID and the Global ID bit.

The L9680 checks the validity of the received RID field in the MOSI\_RS frame. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR\_RID bit will be flagged in the current GSW.

Table 8. Remote sensor SPI register map

GID			DIF	) / V	/ID			Hex	R/W	Name	Description		C	perating	State	
GID			KIL	<i>, ,</i> v	טוע			пех	IK/VV	Name	Description	Init	Diag	Safing	Scrap	Arming
0	1	0	1	0	0	0	0	\$50	R	RSDR0						
0	1	0	1	0	0	0	1	\$51	R	RSDR1						
0	1	0	1	0	0	1	0	\$52	R	RSDR2						
0	1	0	1	0	0	1	1	\$53	R	RSDR3						
0	1	0	1	0	1	0	0	\$54	R	RSDR4	Remote sensor					
0	1	0	1	0	1	0	1	\$55	R	RSDR5	data/status					
0	1	0	1	0	1	1	0	\$56	R	RSDR6	registers					
0	1	0	1	0	1	1	1	\$57	R	RSDR7	(PSI-5 or WSS)					
0	1	0	1	1	0	0	0	\$58	R	RSDR8	, ,					
0	1	0	1	1	0	0	1	\$59	R	RSDR9						
0	1	0	1	1	0	1	0	\$5A	R	RSDR10						
0	1	0	1	1	0	1	1	\$5B	R	RSDR11						
0	1	0	1	1	1	0	0	\$5C	R	RSTHR0_L	Remote					
0	1	0	1	1	1	0	1	\$5D	R	RSTHR1_L	sensor					
0	1	0	1	1	1	1	0	\$5E	R	RSTHR2_L	(PSI-5 or					
0	1	0	1	1	1	1	1	\$5F	R	RSTHR3_L	WSS)					
0	1	1	0	0	0	0	0	\$60	R	RSTHR0_H	Remote					
0	1	1	0	0	0	0	1	\$61	R	RSTHR1_H	sensor current					
0	1	1	0	0	0	1	0	\$62	R	RSTHR2_H	2 registers					
0	1	1	0	0	0	1	1	\$63	R	RSTHR3_H	(WSS only)					
0	1	1	0	1	0	1	0	\$6A	R	ARM_STATE	Arming signals status register					
1	1	1	1	1	1	1	1	\$FF	R	SAF_CC	Safing record compare complete register					

SPI interfaces L9680

# 7.5 Remote sensor SPI tables

A summary of all the registers contained within the remote sensor SPI map are shown below and are referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field (the symbol '-'is used to indicate that the register is not affected by the relevant reset signal').

# 7.5.1 Remote sensor SPI global status word

The Remote Sensor SPI of L9680 contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the Remote Sensor SPI is the most significant 11 bits of MISO\_RS data.

Table 9. GSW - Remote sensor SPI global status word

MISO_RS	GSW	Name	POR	WSM	SSM	Description
						SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read '
31	10	SPIFLT	0	0	0	0 No fault
						1 Fault
30	9	0	0	0	0	Unused
						Remote Sensor Interface Fault Present, logical OR of the corresponding FLTBIT bits (bit 15) for all faults but NODATA
29	8	RSFLT	0	0	0	0 All the RSDRx-FLTBIT bits are 0
						1 At least one of the RSDRx-FLTBIT bits is 1 and the associated fault code is different from NODATA
28	7	0	0	0	0	Unused
27	6	0	0	0	0	Unused
26	5	0	0	0	0	Unused
25	4	0	0	0	0	Unused
24	3	0	0	0	0	Unused
23	2	0	0	0	0	Unused
22	1	0	0	0	0	Unused
	_	ERR RI		_	_	Read address received in the actual SPI frame is unused so data in the response is don't care
21	0	D D	0	0	0	0 No Error
						1 Error

# 7.6 Remote sensor SPI read/write registers

# 7.6.1 Remote sensor data/fault registers (RSDRx @FLT = 0)

PSI5/WSS Remote Sensor 0 Data and Fault Flag Register ch 0, slot 1 / ch 0 (RSDR0) PSI5/WSS Remote Sensor 1 Data and Fault Flag Register ch 1, slot 1 / ch 1 (RSDR1) PSI5/WSS Remote Sensor 2 Data and Fault Flag Register ch 2, slot 1 / ch 2 (RSDR2) PSI5/WSS Remote Sensor 3 Data and Fault Flag Register ch 3, slot 1 / ch 3 (RSDR3) PSI5 configuration register for channel 0, slot 2 (RSDR4) PSI5 configuration register for channel 1, slot 2 (RSDR5) PSI5 configuration register for channel 2, slot 2 (RSDR6) PSI5 configuration register for channel 3, slot 2 (RSDR7) PSI5 configuration register for channel 0, slot 2 (RSDR8) PSI5 configuration register for channel 1, slot 2 (RSDR9) PSI5 configuration register for channel 2, slot 2 (RSDR10) PSI5 configuration register for channel 3, slot 2 (RSDR11)

### Bit 15 = 0 NO FAULT Condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS					х	x	x	х	х	х	x	x	x	x	х	х	х	x	х	x
MISO_RS		CRC		0	FLT=0	JJO/UO		LCID	[3:0]						DATA	A [9:0]				
MISO_RS		CRC		STDSTL	FLT=0	-atch_D0	LCID	[1:0]						DATA	[11:0]					

ID: 50 (RSDR0) 51 (RSDR1) 52 (RSDR2) 53 (RSDR3) 54 (RSDR4) 55 (RSDR5) 56 (RSDR6) 57 (RSDR7) 58 (RSDR8) 59 (RSDR9) 5A (RSDR10) 5B (RSDR11)

Type: R

Read: 5000 (RSDR0) 5100 (RSDR1) 5200 (RSDR2) 5300 (RSDR3) 5400 (RSDR4) 5500 (RSDR5) 5600 (RSDR6) SPI interfaces L9680

5700 (RSDR7) 5800 (RSDR8) 5900 (RSDR9) 5A00 (RSDR10) 5B00 (RSDR11)

Write:

POR WSM SSM

### **PSI5** configured channel

CRC[2:0] - - - CRC based on bits [16:0]

Updated based on bits [16:0]

FLT 1 1 Fault Status - Depending on Fault Status, the DATA bits are defined differently

Cleared when all of the following bits are '0': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, INVALID, SLOT ERROR, NODATA

Set when any of the following bits are '1': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, INVALID, SLOT\_ERROR, NODATA

### 0 No fault

1 Fault

On/Off 0 0 Channel On/Off Status

Cleared by SSM\_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set

Set when channel is commanded ON by SPI RSCTRL

0 Off

1 On

LCID[3:0] - - Logical Channel ID

Updated based on SPI read request

0000 RSU0 SLOT1

0001 RSU0 SLOT2

0010 RSU0 SLOT3

0100 RSU1 SLOT1

0101 RSU1 SLOT2

0110 RSU1 SLOT3

1000 RSU2 SLOT1

1001 RSU2 SLOT2

1010 RSU2 SLOT3

1100 RSU3 SLOT1

1010 RSU3 SLOT2

1110 RSU3 SLOT3

DATA[9:0] \$000 \$000 \$000 10-bit data from Manchester decoder

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL

updated when a valid PSI5 frame is received

### Wheel speed configured channel (RSDR0, RSDR1, RSDR2, RSDR3)

CRC[2:0] - - - CRC based on bits [16:0]

Updated based on bits [16:0]

STDSTL 0 0 Standstill indication (valid only for VDA sensor or PWM 2 edges)

1 Standstill

0 Valid Sensor Signal

FLT 1 1 Fault Status - Depending on Fault Status, the DATA bits are defined differently

Cleared when all of the following bits are '0': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, INVALID, PULSE OVERFLOW ERROR, NODATA

Set when any of the following bits are '1': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, INVALID, PULSE OVERFLOW ERROR, NODATA

0 No Fault

1 Fault

Latch\_D0 0 0 Logical Channel ID

0 no prior bit0 faults

1 prior message(s) contained bit0 fault

LCID[1:0] Logical Channel ID

00 RSU0

01 RSU1

10 RSU2

11 RSU3

DATA[11:0] \$000 \$000 \$000 12-bit data from wheel speed decoder

**VDA Data Format** 

DATA [7:0] Counter bits DATA [11:8] Counter bits

**PWM Data Format** 

DATA [8:0] Pulse Data bits

DS11615 Rev 2 153/280

SPI interfaces L9680

# 7.6.2 Remote sensor data/fault registers w/o fault (RSDRx @ FLT=1)

PSI5/WSS Remote Sensor 0 Data and Fault Flag Register ch 0, slot 1 / ch 0 (RSDR0)
PSI5/WSS Remote Sensor 1 Data and Fault Flag Register ch 1, slot 1 / ch 1 (RSDR1)
PSI5/WSS Remote Sensor 2 Data and Fault Flag Register ch 2, slot 1 / ch 2 (RSDR2)
PSI5/WSS Remote Sensor 3 Data and Fault Flag Register ch 3, slot 1 / ch 3 (RSDR3)
PSI5 configuration register for channel 0, slot 2 (RSDR4)
PSI5 configuration register for channel 1, slot 2 (RSDR5)
PSI5 configuration register for channel 2, slot 2 (RSDR6)
PSI5 configuration register for channel 3, slot 2 (RSDR7)
PSI5 configuration register for channel 0, slot 2 (RSDR8)

PSI5 configuration register for channel 1, slot 2 (RSDR9)

PSI5 configuration register for channel 2, slot 2 (RSDR10)

PSI5 configuration register for channel 3, slot 2 (RSDR11)

### Bit 15 = 1 FAULTED condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOS_RS	ı		-			Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
MISO_RS (PSI5)	3	CRC		x	FLT=1	JJO/uO		LCID	[3:0]		STG	STB	CURRENT_HI	OPENDET	RSTEMP	INVALID	NODATA	SLOT_ERROR	×	х
MISO_RS (WSS)	<b>i</b>	CRC		x	FLT=1	JJO/uO	LCIE	[1:0]			STG	STB	CURRENT_HI	OPENDET	RSTEMP	INVALID	NODATA	SLOT_ERROR	x	х

ID: 50 (RSDR0) 51 (RSDR1) 52 (RSDR2) 53 (RSDR3) 54 (RSDR4) 55 (RSDR5) 56 (RSDR6) 57 (RSDR7) 58 (RSDR8) 59 (RSDR9) 5A (RSDR10) 5B (RSDR11)

Type: R

Read: 5000 (RSDR0) 5100 (RSDR1) 5200 (RSDR2) 5300 (RSDR3) 5400 (RSDR4) 5500 (RSDR5) 5600 (RSDR6)

5700 (RSDR7) 5800 (RSDR8) 5900 (RSDR9) 5A00 (RSDR10) 5B00 (RSDR11)

Write:

POR WSM SSM

CRC[2:0] - - - CRC based on bits [16:0]

Updated based on bits [16:0]

FLT 0 0 0 Fault Status

Cleared when all of the following bits are '0': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR

Set when any of the following bits are '1': STG, STB, CURRENT\_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE

**OVERFLOW ERROR** 

0 No fault

1 Fault

On/Off 0 0 Channel On/Off Status

Cleared by SSM\_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set

Set when channel is commanded ON by SPI RSCTRL

0 Off

1 On

LCID[0:3] 0000 0000 0000 Logical Channel ID

Updated based on SPI read request

0000 RSU0 SLOT1

0001 RSU0 SLOT2

0010 RSU0 SLOT3

0100 RSU1 SLOT1

0101 RSU1 SLOT2 1

0110 RSU1 SLOT3

1000 RSU2 SLOT1

1001 RSU2 SLOT2

1010 RSU2 SLOT3

1100 RSU3 SLOT1

1101 RSU3 SLOT2

1110 RSU3 SLOT3

SPI interfaces L9680

STG 0 0 Short to Ground (in current limit condition)

Cleared by SSM\_RESET or when channel is commanded OFF via SPI RSCTRL

0 No fault

1 Fault

STB 0 0 0 Short to Battery

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL - not cleared by channel OFF caused by STG or RSTEMP Set when channel voltage exceeds VSUP for a time greater than  $T_{STBTH}$ 

0 No fault

1 Fault

CURRENT\_HI 0 0 0 Current High

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL

Set when channel current exceeds ILKGG for a time determined by an up/down counter

0 No fault

1 Fault

OPENDET 0 0 Open Sensor Detected

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL

Set when channel current exceeds ILKGB for a time determined by an up/down counter

0 No fault

1 Fault

RSTEMP 0 0 Over temperature detected

Cleared by SSM\_RESET or when channel is commanded OFF via SPI RSCTRL

Set when over-temp condition is detected

0 No fault

1 Fault

INVALID 0 0 0 Invalid Data

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT\_HI, OPEN\_DET,

RSTEMP, SLOT ERROR (PSI5), PULSE OVERFLOW ERROR (WSS) or if a new valid data is received

Set in PSI5 configuration when two valid start bits are received and a Manchester error (# of bits, bit timing) or parity error is detected

Set in WSS configuration when parity error is detected (when this check is feasible). Valid only for VDA sensor.

0 No fault

1 Fault

### NODATA 1 1 1 No Data in buffer

0

Cleared when a valid PSI5/WSS frame is received or if one of the following is set: STG, STB, CURRENT\_HI, OPEN\_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID

Set upon SPI read of RSDRx and none of the following bits are set: STG, STB, CURRENT\_HI, OPEN\_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID

0 No fault

1 Fault

### PULSE OVERFLOW ERROR

0 Pulse duration counter overflow (valid only for PWM 2 edges sensors)

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL

0 No fault

1 Fault

## SLOT ERROR 0 0 Slot error fault (valid only for PSI5 sensors

Cleared by SSM\_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB,

CURRENT\_HI, OPEN\_DET, RSTEMP or if a new valid data is received Set in case of slot control enabled and frame not completely inside slot or more than one frame inside the slot

0 No fault

1 Fault

DS11615 Rev 2 157/280

SPI interfaces L9680

# 7.6.3 Remote sensor x current registers y (RSTHRx\_y)

Remote sensor 0, base current and delta to calculate 1st top current (RSTHR0\_L) Remote sensor 1, base current and delta to calculate 1st top current (RSTHR1\_L Remote sensor 2, base current and delta to calculate 1st top current (RSTHR2\_L Remote sensor 3, base current and delta to calculate 1st top current (RSTHR3\_L Remote sensor 0 (only for WSS), delta to calculate 2nd top current (RSTHR0\_H) Remote sensor 1 (only for WSS), delta to calculate 2nd top current (RSTHR1\_H Remote sensor 2 (only for WSS), delta to calculate 2nd top current (RSTHR2\_H Remote sensor 3 (only for WSS), delta to calculate 2nd top current (RSTHR3\_H

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х
MISO_RS				DE	LTA 1S	Т ТОР	[9:0]							BAS	E CUF	RRENT	[9:0]			
MISO_RS	0	0	0	0	0	0	0	0	0	0				DEL	TA 2N	D TOP	[9:0]			

ID: 5C (RSTHR0\_L)

5D (RSTHR1\_L) 5E (RSTHR2\_L) 5F (RSTHR3\_L) 60 (RSTHR0\_H) 61 (RSTHR1\_H) 62 (RSTHR2\_H) 63 (RSTHR3\_H

Type: R

Read: 5C00 (RSTHR0\_L)

5D00 (RSTHR1\_L) 5E00 (RSTHR2\_L) 5F00 (RSTHR3\_L) 6000 (RSTHR0\_H) 6100 (RSTHR1\_H) 6200 (RSTHR2\_H) 6300 (RSTHR3\_H

Write: -

POR WSM SSM

BASE CURRENT [9:0]

\$A1 \$A1 \$A1 \$A1 PSI5/WSS base current measured by internal converter (93.75  $\mu$ A ±9% each LSB).

DELTA 1ST TOP \$103 \$103 \$103 PSI5/WSS delta measured by internal converter respect to base current [19:10] (93.75  $\mu$ A  $\pm$ 9% each LSB) to get top current.

Low threshold = base current+(DELTA\_1ST\_TOP/2) in case of WSS or PSI5 without current averaged algorithm (bit 4 of RSRCx register equal to 0).

Low threshold = base current+(DELTA\_1ST\_TOP) in case of PSI5 with current averaged algorithm (bit 4 of RSRCx register equal to 1).



DELTA 2ND TOP [9:0] \$7 \$103 \$103 WSS delta measured by internal converter respect to base current (93.75 µA ±9% each LSB) to get second top current.

High threshold = ((base current+DELTA\_1ST\_TOP)+(base current+DELTA\_2ND\_TOP))/2.

# 7.6.4 Arming signals register (ARM\_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			-		Х	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Χ	Х	Х
MISO	0	0	0	0	0	0	0	0	0	0	PSINHINT	PSINH_EXP_TIME	ACL_PIN_STATE	ACL_VALID	ARMINT_4	ARMINT_3	ARMINT_2	ARMINT_1	0	0

**ID**: 6A

Type: R

Read: 6A00

**PSINHINT** 

Write: -

POR WSM SSM

ARMINT\_x - - - State of ARMINT signals

Updated per Safing Engine output logic diagram in case of internal safing engine otherwise is the echo of ARMx pins

ACL\_VALID 0 0 0 Valid ACL detection

0 Cleared when ACL\_BAD=2 1 Set when ACL\_GOOD=3

ACL\_PIN\_STATE - - - Echo of ACL pin

PSINH\_EXP\_TIME 0 0 0 State of PSINH expiration timer

0 If timer is 01 If timer is counting

State of PSINHINT signal

Updated per PSINH output logic diagram in case of internal engine otherwise

is the echo of PSINH pin inverted

SPI interfaces L9680

# 7.6.5 Safing record compare complete register (SAF\_CC)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI/ MOSI_RS			-		Х	х	Х	Х	х	х	Х	х	х	х	х	х	Х	Х	х	Х
MISO/ MISO_RS	0	0	0	0	C_16	CC_15	CC_14	C_13	C_12	CC_11	C10	6_22	8_22	CC_7	9_22	cc_5	CC_4	c3	cc_2	CC_1

**ID**: FF

Type: R

**Read:** \$FF01 **Write:** \$80FE

POR WSM

CC\_xx 0 0 0 Indicates compare complete status of each of the 16 safing records, and defines the end of the sample cycle for safing

Cleared by SSM\_RESET or upon SPI read, set by safing engine when request, response mask and target registers match the incoming SPI frame

- 0 Compare not completed for record x
- 1 Compare completed for record x

L9680 Deployment drivers

# 8 Deployment drivers

The squib deployment block consists of 12 independent high side drivers and 12 independent low side drivers. Squib deployment logic requires a deploy command received through SPI communications and either an arming condition processed by safing logic or a proper ARMx input pin assessment, depending on whether the internal safing engine is used or not. Both conditions must exist in order for the deployment to occur. Once a deployment is initiated, it can only be terminated by an SSM RESET event.

L9680 allows all 12 squib loops to be deployed at the very same time or in other possible timing sequence. Deployment drivers are capable of granting a successful deployment also in case of short to ground on low-side circuit (SRx pins). Firing voltage capability across high side circuit is maximum 25 V. High side and low side drivers account for a maximum series total resistance of 2  $\Omega$ . Each loop is granted for a minimum number of deployments of 50, under all normal operating conditions and with a deployment repetition time higher than 10s. Both the High and the Low side FET drivers are equipped with passive gate turn-off circuitries to guarantee the FETs are kept in off state also when the device is unpowered or during power-up/down transients.

# 8.1 Control logic

A block diagram representing the deployment driver logic is shown below. Deployment driver logic features include:

- Deploy command logic
- Deployment current selection
- Deployment current monitoring and deploy success feedback
- Diagnostic control and feedback

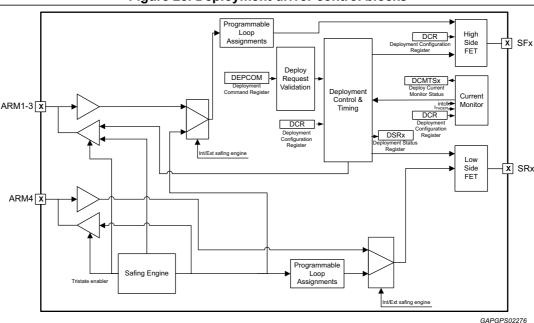


Figure 28. Deployment driver control blocks

Deployment drivers L9680

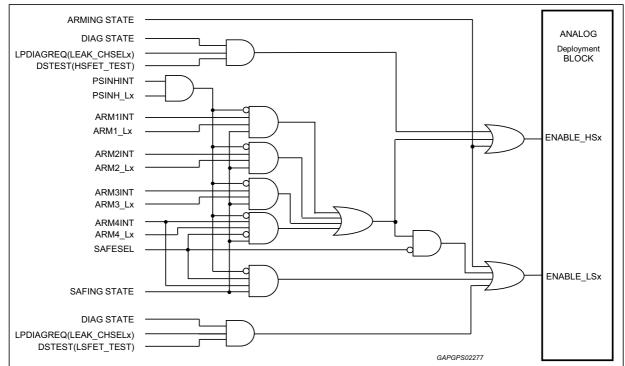
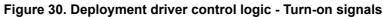
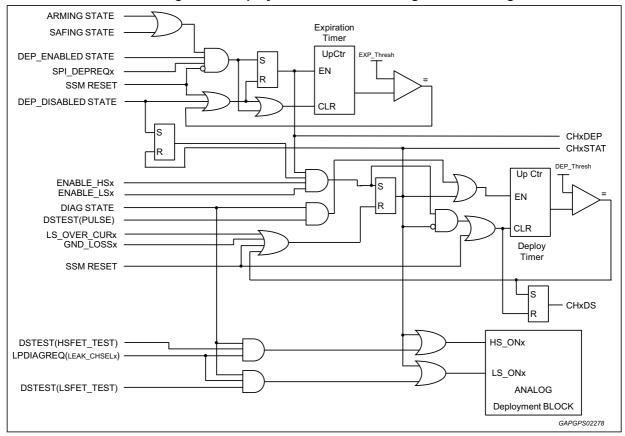


Figure 29. Deployment driver control logic - Enable signal





L9680 Deployment drivers

The high level block diagram for the deployment drivers is shown below:

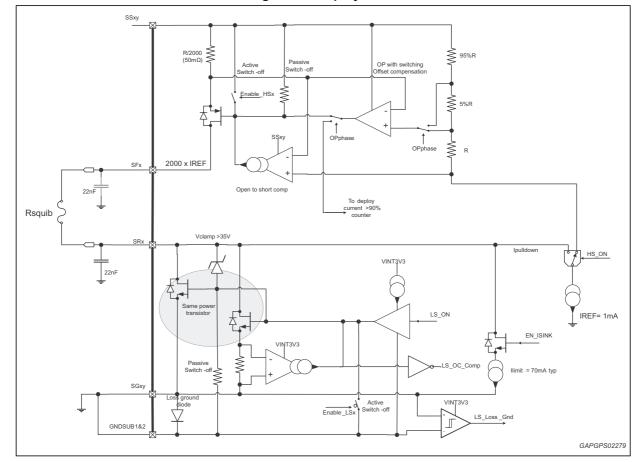


Figure 31. Deployment driver block

# 8.1.1 Deployment current selection

Deployment current is programmed for each channel using the Deploy Configuration Register (DCRx) shown in *Section 7.3.7*.

The deploy time selection allows the device to deploy for a time up to 4.032 ms. Careful considerations should be done in order to avoid damage on the squib driver section for excessive thermal heat. In order to prevent device damage, it is suggested to avoid excessive voltage drop between SSxy and SFxy. In case the 1.75 A deployment current level is selected, the voltage drop across the pins should be limited to maximum 17 V for deployment times longer than 0.7 ms and up to 2 ms and 15 V up to 3.2 ms. In case 1.2 A is selected, the voltage drop should be limited to maximum 22 V for deployment times longer than 2 ms and up to 3.2 ms.

# 8.1.2 Deploy command expiration timer

Deploy commands are received for all channels using SPI communications. Once a deploy command is received, it will remain valid for a specified time period selected in the *Deployment configuration registers (DCR\_x)*. The deploy status and deploy expiration timer can be read through the *Deployment status registers (DSR\_x)*. The deploy expiration timer is selectable via 2 bits and the maximum programmable time is 500 ms nominal.



DS11615 Rev 2 163/280

Deployment drivers L9680

# 8.1.3 Deployment control flow

Deployment control logic requires the following conditions to be true to successfully operate a deployment:

- POR = 0
- SSM to be either in Safing State or Arming State
- a valid arming condition processed by safing logic or ARMx signals to be set (depending on selection of internal or external safing engine)
- channel-specific deploy command request bits to be set via SPI in the Deploy command Register (DEPCOM)
- a global deployment state has to be active, as described in the following figure.

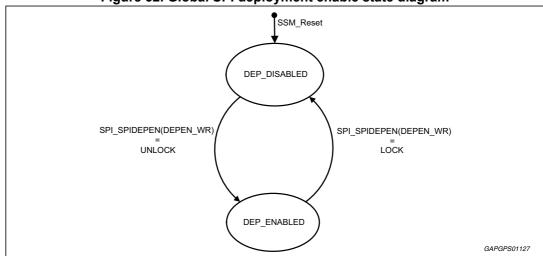


Figure 32. Global SPI deployment enable state diagram

In case a multiple deployment request would be needed, i.e. deploying the same channel in sequence, a toggle on DEP\_DISABLED has to be performed and a new DEPCOM command on the same channel has to be sent.

The SPI DEPCOM command is ignored if the device is in the DEP\_DISABLED state and the deploy command is not set. While in DEP\_ENABLED state, the following functionalities that could be active are forced to their reset state:

- All squib and DC sensor diagnostic current or voltage sources
- All squib, DC sensor and ADC diagnostic MUX settings, state machine, etc.

The SPI LOCK and SPI UNLOCK signals are available in the SPIDEPEN command:

High-side and Low-side enablers (ARMx) are assigned to the desired channels by means of the programmable loop matrix. Loop matrix registers are 4, one for each ARMx signals. In each loop matrix register 12 bits are present to associate independently loops with ARMx signals. In case external safing is selected LOOP\_MATRIX\_ARM4 register is don't care because ARM4 pin is used to arm the low side of all loops without association matrix. Deploy commands in the Deploy Command Register (DEPCOM) are channel specific.

Deployment requires a valid arming condition from safing logic or ARMx signals to be set any time before, during or after the specific sequence of deploy commands is received. It is feasible for a deploy command to be received without a valid arming condition from safing logic or the ARMx being set. In this case, the deploy command will be terminated according

L9680 **Deployment drivers** 

> to the Deploy command expiration timer. Likewise, a valid arming condition signal can be set without receiving a Deploy Command. In this case, the enabling signals will remain active according to the Arming Enable Pulse Stretch Timer or the ARMx enabling state. The Arming Enable Pulse Stretch Timers is available in the AEPSTS register.

#### 8.1.4 **Deployment current monitoring**

A current comparator is used to indicate when the output current from the HSD, SFx, exceeds the deployment current threshold, I<sub>THDEPL</sub>. The timer signal remains active and increments while the current meets the programmed deploy current as set in the Deploy Configuration Register. The deploy current counter value is stored in the Deploy Current Monitor Timer Register XY (DCMTSxy). There is a unique timer register for each channel.

If the deploy current falls below the specified current threshold momentarily and recovers, the deploy current counter will pause during the drop-out and continue once the current exceeds the threshold. The deploy current counter will not be reset by the presence or absence of current in the deployment channel.

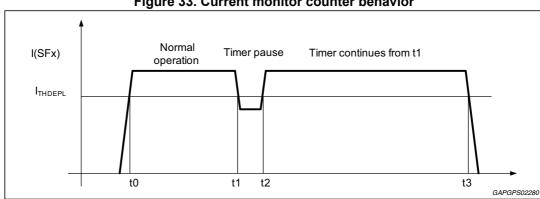


Figure 33. Current monitor counter behavior

The deploy current counter is reset to \$0000 as soon as a toggle on DEP\_DISABLED is performed and a new DEPCOM command on the same channel is received.

#### 8.1.5 **Deployment success**

Deploy success flag is set when the deploy timer elapses. This bit (CHxDS) is contained in the Deploy Status Register. Within the Global Status Word register (GSW), a single bit (DEPOK) is also set once any of the 12 deployment channels sets a deploy success flag.

#### 8.2 **Energy reserve - deployment voltage**

One deployment voltage source pin is used for adjacent channels (e.g. SS23 for channels 2 and 3). These pins are directly connected to the high side drivers for each channel.

### 8.3 Deployment ground return

L9680 is hosted in a particular frame allowing squib driver ground feedback to be connected to an internal ground ring. This ring is electrically connected to the package exposed pad and to the GNDSUB1 and GNDSUB2 pins. Connection to these two pins is made by means of a strong metal layer, therefore this connection is sufficient for all deployments occurring



DS11615 Rev 2 165/280

L9680 **Deployment drivers** 

> simultaneously, even in case of only one out of the three possible connections being available.

#### 8.4 Deployment driver protections

#### 8.4.1 **Delayed low-side deactivation**

To control voltage spikes at the squib pins during drivers deactivation at the end of a deployment, the low side driver is switched off after t<sub>depl</sub> is-div delay time with respect to the high side deactivation.

#### 8.4.2 Low-side voltage clamp

The Low side driver is protected against overvoltage at the SRx pins by means of a clamping structure as shown in Figure 31. When the Low side driver is turned off, voltage transients at the SRx pin may be caused by squib inductance. In this case a low side FET drain to gate clamp will reactivate the low side FET allowing for residual inductance current recirculation, thus preventing potential low side FET damage by overvoltage.

#### 8.4.3 Short to battery

The Low side driver is equipped with current limitation and overcurrent protection circuitry. In case of short to battery at the squib pins, the short circuit current is limited by the Low side driver to I<sub>LIMSRx</sub>. If this condition lasts for longer than t<sub>LIM</sub> deglitch filter time then the low and high-side drivers will be switched off and latched in this state until a new deployment is commanded after SPI\_DEPEN is re-triggered.

#### 8.4.4 Short to ground

The squib driver is designed to stand a short to ground at the squib pins during deployment. In particular, the current flowing through the short circuit is limited by the high side driver (deployment current) and the high-side FET is sized to handle the related energy.

In case the short to ground during deployment occurs after an open circuit, a protection against damage is also available. The high side current regulator would have normally reacted to the open circuit by increasing the Vgs of the high side FET. Thanks to a dedicated fast comparator detecting the open condition, the driver is able to discharge the FET gate quickly in order to reduce current overshoot and prevent potential driver damage when the short to ground occurs.

#### 8.4.5 Intermittent open squib

A dedicated protection is also available in case of intermittent open load during deployment. In this case, if load is restored after an open circuit, due to slow reaction of the high-side current regulation loop, the current through the squib is limited only to I<sub>LIMSRx</sub> by the low side driver. If this condition lasts for longer than t<sub>LIMOS</sub> then the high side is turned off for theorems and then reactivated. By this feature, intermittent open squib and short to battery faults may be distinguished and handled properly by the drivers.



L9680 Deployment drivers

# 8.5 Diagnostics

The L9680 provides the following diagnostic feedback for all deployment channels:

- High voltage leakage test for oxide isolation check on SFx and SRx
- Leakage to battery and ground on both SFx and SRx pins with or without a squib
- Short between loops diagnostics
- Squib resistance measurement with leakage cancellation and selectable range (10/50 Ω)
- High squib resistance with range from 500  $\Omega$  to 2000  $\Omega$
- SSxy, SFx and VER voltage status
- High and Low side FET diagnostics
- High side driver diagnostics
- Loss of ground return diagnostics
- High Side Safing FET diagnostics

The above diagnostic results are processed through a 10 bit Analog to digital algorithmic converter. These tests can be addressed in two different ways, with a high level approach or a low-level one. The main difference between the two approaches is that with the low level approach the user is allowed to precisely control the diagnostic circuitry, also deciding the proper timings involved in the different tests. On the other hand, the high level approach is an automatic way of getting diagnostic results for which an internal state machine is taking care of instructions and timings.

The following is block diagram of the Squib Diagnostics.



DS11615 Rev 2 167/280

Deployment drivers L9680

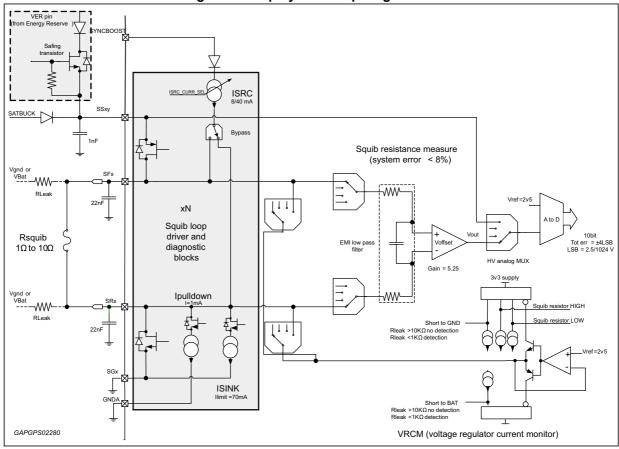


Figure 34. Deployment loop diagnostics

The leakage diagnostic includes short to battery, short to ground and shorts between loops. The test is applied to each SFx and SRx pin so shorts can be detected regardless of the resistance between the squib pins.

### 8.5.1 Low level diagnostic approach

In this approach, each of the test steps described in the sections below requires user intervention by issuing the proper SPI command.

## High voltage leakage test for oxide isolation check

This test is mandatory to address possible leakages that could not be experienced at low voltages on SFx or SRx pins. The I<sub>source</sub> current generator (ISRC) is enabled on the chosen SFx pin. To confirm that the SFx pin has then reached a suitable voltage level, a dedicated ADC measurement on the SFx pin can be requested. Once this test is performed, a leakage test on SFx and SRx pins can be issued to double check possible leakages.

### Leakage to battery/ground diagnostics

Prior to the real test, the Voltage Regulator Current Monitor block (VRCM) has to be tested and validated. The validation of VRCM goes into verifying both the short to battery and short to ground flags.

The  $I_{source}$  current generator (ISRC) is first connected to SFx pin to raise its voltage to SYNCBOOST. Then, the Voltage Regulator Current Monitor block (VRCM) is enabled and



L9680 Deployment drivers

connected to the selected SFx pin. The I<sub>sink</sub> current limited switch (ISNK) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to battery flag would be asserted.

Then, the I<sub>sink</sub> current limited switch (ISNK) is connected to SRx pin, the Voltage Regulator Current Monitor block (VRCM) is enabled and connected to the selected SRx pin. The I<sub>source</sub> current generator (ISRC) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to ground flag would be asserted.

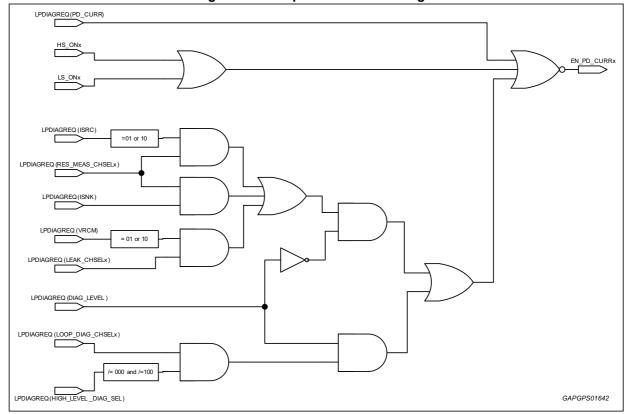


Figure 35. SRx pull-down enable logic

Once the VRCM block is validated, the real leakage tests can be performed. ISRC and ISNK currents have to be kept switched off. The VRCM shall be connected to the desired pin (either SFx or SRx pins); by doing this, also the pull-down current on the selected SRx pin is automatically deactivated). During the test, if no leakage is present the voltage on the selected SFx or SRx pin will be forced by the VRCM to the VREF level and no current is detected or sourced by the VRCM. If there is leakage to ground or battery, the VRCM will sink or source current trying to maintain VREF. Two current comparators, ISTB and ISTG, will detect the abnormal current flow and the relative flags will be given in the LPDIAGSTAT. These flags are not latched and report the real time status of the relevant comparators in case of low-level leakage diagnostic test. Voltage conversion is not required to have these flags updated. In LPDIAGSTAT register are also reported the channel and the pin (SFx or SRx) under test, respectively with LEAK CHSEL and SQP bit fields.

The pull-down currents on the other SRx pins are still active. Therefore, the leakage test that would show a leakage to ground may be depending on a real leakage on the pin under test or on a short between loops.



DS11615 Rev 2 169/280

Deployment drivers L9680

## Short between loops diagnostics

In case the previous test has reported a leakage to ground fault, the short between loops diagnostics shall be run. The same procedure is followed as described for normal leakage tests except the fact that in this case all the pull-down current generators have to be deactivated (not only the one for the pin under test), by means of the PD\_CURR bit in the Diagnostic Request Register (LPDIAGREQ). If a leakage or ground fault is not present, then the channel under test has a short to another squib loop.

Fault condition on squib channel	Channel leakage diagnostics with PD_CURR on (for other channels than the one under test	Channel leakage diagnostics with PD_CURR off (for all channels)
No shorts	No fault	No fault
Short to battery	STB fault	STB fault
Short to ground	STG fault	STG fault
Short between loops	STG fault	No fault

Table 10. Short between loops diagnostics decoding

The condition of two open channels, i.e. without squib resistance connecting SFx to SRx, that have a short between loops on SFx cannot be detected. If only one of the two shorted SFx pins is open, the fault will be indicated on the open channel.

## Squib resistance measurement

During a resistance measurement, a two-step process is performed. At the first step, both ISRC current generator and ISNK current limited switch are enabled and connected to the selected SFx and SRx channel, through ISRC, ISRC\_CURR\_SEL, ISNK and RES\_MEAS\_CHSEL bit fields in the Loop Diagnostic Request Register (LPDIAGREQ). The ISRC current can be configured to either 40 mA or 8 mA nominal value through the ISRC\_CURR\_SEL bit in the LPDIAGREQ register providing the user with two different measurement range options. A differential voltage is created between the SFx and SRx pin based on the ISRC current and squib resistance between the pins. The SPI interface will provide the first resistance measurement voltage (Vdiff1) based on the amplifying factor of the differential amplifier and a 10 bit internal ADC conversion. The second measurement step (bypass measurement) is performed redirecting ISRC to the selected SRx pin, while keeping ISNK on; this way, the differential amplifier and following ADC will output the offset measurement through SPI (Vdiff2). Microcontroller is then allowed to calculate the mathematical difference between first and second measurements to obtain the real squib resistance value.

$$V_{diff1} = G_{RSQ} \times \left[I_{SRC\_*} \times \left(\frac{R_{LKG\_SF} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}}\right) + \frac{R_{SQ}}{R_{LKG\_SF} + R_{SQ}}(V_{LKG\_SF} - V_{SRx\_RM})\right] + G_{RSQ} \times V_{off\_RSQ}$$

$$V_{diff2} = \frac{G_{RSQ} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \times (V_{LKG\_SF} - V_{SRx\_RM}) + G_{RSQ} \times V_{off\_RSQ}$$

$$R_{SQ} = \frac{V_{diff1} - V_{diff2}}{G_{RSQ} \times I_{SRC\_*}} \text{ (assuming } R_{LKG\_SF} >> R_{SQ})$$

L9680 Deployment drivers

The simplification in the calculation method reported above can result in some amount of error that is already incorporated in the overall tolerance of the squib resistance measurement reported in the electrical parameters table.

Values of each measurement step can be required addressing the proper ADCREQx code in Section 7.3.33: ADC request and data registers (DIAGCTRL x).

This calculation is tolerant to leakages and, thanks to a dedicated EMI low-pass filter, also to high frequency noises on squib lines. Moreover, L9680 features a slew rate control on the ISRC current generator to mitigate emissions.

### High squib resistance diagnostics

With this test, the device is able to understand if the squib resistance value is below 200  $\Omega$ , between 500  $\Omega$  and 2000  $\Omega$  or beyond 5000  $\Omega$ . During a high squib resistance diagnostics, VRCM and ISNK are enabled and connected respectively to SFx and SRx on the selected channel. VREF voltage level will be output on SFx. Current flowing on SFx will be measured and compared to I<sub>SRlow</sub> and I<sub>SRhigh</sub> thresholds to identify if the resistance is above or below RSRlow or RSRhigh levels. The results are reported in the LPDIAGSTAT register. The relative flags (HSR\_HI and HSR\_LO) are not latched and reflect the current status of the comparators.

## High and low side FET diagnostics

This couple of tests can only be run during the diagnostic mode of the power-up sequence *Figure 11*. Tests are performed individually for HS driver or LS driver, with two dedicated commands. Prior to either the HS or LS FET diagnostics being run, the VRCM has to be first enabled. Within the command to enable the VRCM, also the channel onto which the FET test will be run has to be selected with the LEAK\_CHSEL bit field. Running the leakage diagnostics with the appropriate delay time prior to either the HS or LS FET diagnostics will precondition the squib pin to the appropriate voltage level. When the FET diagnostic command is issued with the Diagnostic Register SPI command (SYSDIAGREQ), the VRCM flags will be cleared, the VRCM deglitch filter time is switched from the leakage diagnostic deglitch filter time (TFLT\_LKG) to the FET test deglitch filter time (TFLT\_LKGB\_FT) for both HS and LS and the output of the VRCM deglitch filter is now allowed to disable the appropriate HS or LS squib driver during FET test.

The device monitors the current through the VRCM. If the FET is working properly, this current will exceed  $I_{HS\_FET\_TH}$  or  $I_{LS\_FET\_TH}$  current threshold, respectively for HS or LS FET test for the deglitch filter time of TFLT\_LKGB\_FT, and the driver under test is turned off immediately and automatically.

If there is a substantial leakage fault to Vbat or GND present during the FET test, leading this leakage current to exceed the IHS\_FET\_TH or ILS\_FET\_TH current threshold, for the deglitch filter time of TFLT\_LKGB\_FT, then the driver under test is turned off immediately and automatically, and the corresponding VRCM flag, STG or STB, is set.

If the current does not exceed the current threshold, the test will be terminated and the driver is anyway turned off within  $T_{\text{FETTIMEOUT}}$ .



DS11615 Rev 2 171/280

Deployment drivers L9680

Tah	ٔ ما	11	ВС	FET	<b>TFST</b>

VRCM Flags		Result
STG	STB	Result
0	0	FET test fail
0	1	FET test pass OR Leakage to Vbat
1	0	FET test disabled due to Leakage to Gd
1	1	State not possible

### Table 12. LS FET TEST

VRCM Flags		Result
STG	STB	Result
0	0	FET test fail
0	1	FET test disabled due to Leakage to Vbat
1	0	FET test pass OR Leakage to GND
1	1	State not possible

During T<sub>FETTIMEOUT</sub> period, the bit stating that the FET is enabled will be set (FETON=1) and will be cleared as soon as the FET is switched back off.

For all conditions the current on SFx/SRx pins will not exceed the VRCM current limitation value ( $I_{LIM\_VRCM\_SINK}$  or  $I_{LIM\_VRCM\_SRC}$ ). There may be higher currents on the squib lines due to the presence of filter capacitors. During these FET tests, energy available to the squib is limited to less than  $E_{FET\_TEST}$ . For high side FET diagnostics, if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=1, STG=0]. If the returned result for the high side FET test is not as the previous then either the FET is not functional, a short to ground occurred during the test, or there is a missing SSxy connection for that channel.

For low side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=0, STG=1]. If the returned result for the low side FET test is not as the previous then either the FET is not functional or a short to battery occurred during the test. In case of ground loss the low-side FET diagnostic would not indicate a FET fault.

The VRCM flags will be given in the LPDIAGSTAT register. The status of the VRCM flags after FET test is latched and can be cleared upon either LPDIAGREQ or SYSDIAGREQ SPI commands.

Finally, after FET test is completed, the VRCM deglitch filter time is switched from the FET test deglitch filter time (TFLT\_LKGB\_FT) to the leakage diagnostic test deglitch filter time

L9680 Deployment drivers

(TFLT\_LKG) for both HS and LS and the output of the VRCM deglitch filter is now not allowed to disable the appropriate HS or LS squib driver anymore.

### High side driver diagnostics

This test is intended to verify the proper functionality of the HS FET driver, but also the external squib connection and other internal circuitries.

First, the ISNK current has to be activated via the LPDIAGREQ register; the channel onto which the ISNK current is activated has to be selected with the RES\_MEAS\_CHSEL bit field. Then, the HS FET related to the loop channel as indicated in the RES\_MEAS\_CHSEL bit field is activated with the dedicated DSTEST code for the HS squib driver test in the Diagnostic Register SPI command (SYSDIAGREQ). In such condition, the HS driver will control the FET current to a level I<sub>LIM\_HS\_FET</sub> much lower than the usual deployment current. The HS\_DRV\_OK flag will be set accordingly to the test result in the LPDIAGSTAT register, as soon as the deployment current monitoring comparator will detect that the current through the HS FET exceeds the diagnostic current threshold, 90%\*I<sub>LIM\_HS\_FET</sub>.

### Loss of ground return diagnostics

This diagnostics is available during a squib measurement or a high side driver diagnostics. This test is based on the voltage drop across the ground return, if the voltage drop exceeds  $SG_{xy\_OPEN}$ , ground connection is considered as lost. Should the ground connection on the squib driver circuit be missing, the bit related to the channel under test by the two above diagnostics will be activated in the LP\_GNDLOSS register. The flag is latched after a proper filter time  $T_{FLT\_SGOPEN}$  and cleared upon read.

## High side safing FET diagnostics

This test has to be issued during the Diag state of the power-up sequence (*Figure 11*). Safing FET has to be switched on with the proper code in DSTEST bit field of the SYSDIAGREQ. Therefore, when the command is received, the device will activate VSF regulator to supply the external safing FET controller. The user can measure the voltage levels of both the VSF regulator and the SSxy nodes. If the safing FET is properly switched on, the voltage on SSxy will be regulated.

The measurement request is done via Diagnostic Control command (DIAGCTRLx), while results will be reported through ADCRESx bit fields.

### **Deployment Timer diagnostic**

This test allows verifying the correct functionality and duration of the timers used to control the deployment times. This test can be executed only when the IC is in the Diag state by setting the appropriate code in the DSTEST field of the SYSDIAGREQ register. When the test is launched, the IC sequentially triggers the activation of the deployment timers of the various channels (each of them separated by 8ms idle time) and outputs the relevant waveform to the ARM1 output discrete pin. See the sequence detail in *Figure 36*. The  $\mu$ C can therefore test the deployment times by measuring the duration of the high pulses sent by the IC on the ARM1 pin. The deployment time configuration used during this test is the latest one programmed in the DCRx registers. In case the test is run on a channel with no DCRx deployment time previously configured, a default 8  $\mu$ s high pulse is output on ARM for the relevant channel.



DS11615 Rev 2 173/280

Deployment drivers L9680

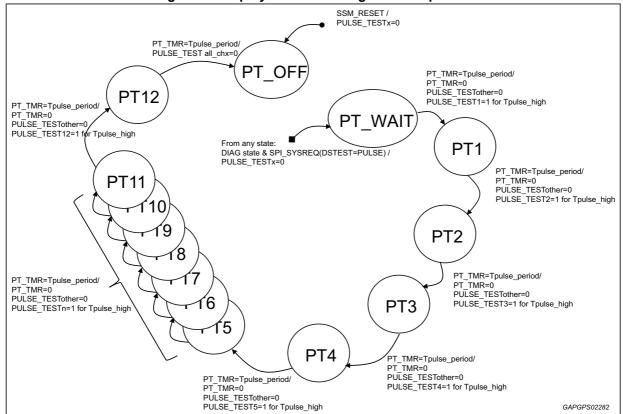


Figure 36. Deployment timer diagnostic sequence

### Squib diagnostics with common SRx connected loops

In case of two SRx pins are intentionally connected together, the PD\_CURR\_CSR bit of the Deployment Configuration register (DCR\_x, where x = 0, 2, 4, 6, 8, A) must be used to indicate which loop pairs have the common SRx connection. The purpose of this additional bit is to control the pull-down current on each channel to be consistent with or without the Common SRx connected loops. When the DCR\_x(PD\_CURR\_CSR) bit is set for one loop pair and the Deployment diagnostic is run on that loop pair, the pull-down current is disabled on both channels of the loop pair selected.

For the squib channel pair with common SRx connection, to understand if the two SFx pins are shorted together, the squib resistance measurement must be required with the following setting: LPDIAGREQ[12:11]=11. In this way the ISRC current generator is enabled on the channel selected by RES\_MEAS\_CHSEL[3:0] bits while the Differential Operational Amplifier is connected on the other channel of the squib channel pair. If the short between the two SFx pin is not present then the Squib resistance measurement results will be close to 0, otherwise it will be half the real squib resistance.

### Loop diagnostics control and results registers

Diagnostic tests and channels for each test are controlled through the Loop Diagnostic Request Register (LPDIAGREQ), diagnostic results are stored in the Loop Diagnostic Status Register (LPDIAGSTAT).

L9680 Deployment drivers

# 8.5.2 High level diagnostic approach

In this approach, the test steps described in the sections below are coded into a dedicated state machine that helps reducing the user intervention to a minimum.

The high-level diagnostic commands are contained in the LPDIAGREQ, LOOP\_DIAG\_SEL, and LOOP\_DIAG\_CHSEL registers. The high-level diagnostic response is available in the LPDIAGSTAT register.

The concept is depicted in the following figures.

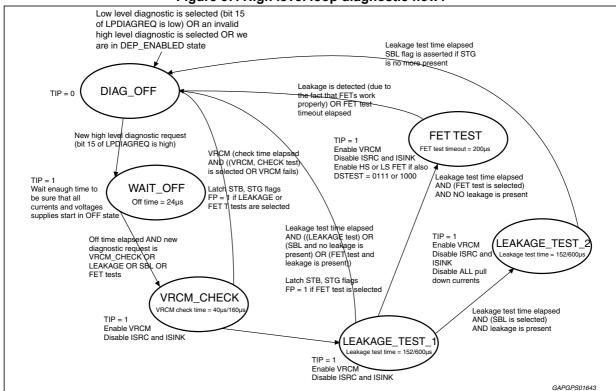


Figure 37. High level loop diagnostic flow1

DS11615 Rev 2 175/280

Deployment drivers L9680

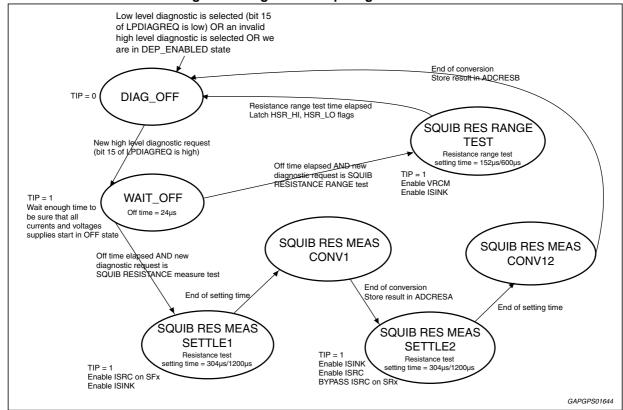


Figure 38. High level loop diagnostic flow2



L9680 Remote sensor interface

# 9 Remote sensor interface

The L9680 contains 4 remote sensor interfaces, capable of supporting PSI-5 protocol (synchronous mode, increased voltage, extended range) and active wheel speed sensors. A simplified block diagram of the interface is shown below. The interface supply is given on the SATBUCK pin (refer to *Figure 3: Power supply block diagram*). The circuitry consists of a power interface that mirrors current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each remote sensor channel. The voltage at the RSUx pins can be limited by the power interface in case of SATBUCK supply overvoltage to protect the external sensors. Decoded data are then output through the Remote Sensor Data Registers (RSDRx). Received signals can be processed to the corresponding discrete logic output pin WS0-WS3. The power interface also contains error detection circuitry. When a fault is detected, the error code is stored in a global SPI data buffer in the Remote Sensor Data Registers (RSDRx).

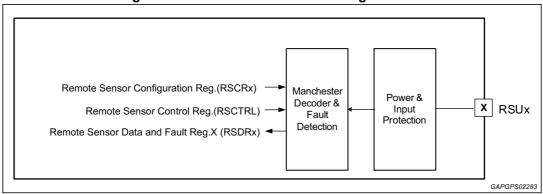


Figure 39. Remote sensor interface logic blocks

Remote sensor configuration can be addressed via the Remote Sensor Configuration Registers (RSCRx). Some of the bit fields in the RSCRx registers are available depending on the chosen configuration, remote sensor rather than wheel speed sensors. In particular, TSxDIS bit allows overriding the time slot control for PSI5 I/F and BLKTxSEL allows selection between 5ms and 10ms for the blanking time applied to the current limitation fault detection each time a channel is activated.

The Remote Sensor Control Register (RSCTRL) allow for interface channels to be switched on and Off and for Sync Pulse control via SPI.

The remote sensor interface reports both data information and fault information in the Remote Sensor Data Register (RSDRx). The device accommodates for a total of 12 data registers. Independent data registers are defined for each remote sensor interface and are formatted differently based on whether the interfaces are programmed for PSI-5 remote sensor functions or active wheel speeds.

In the VDA sensor communication, data bit D0 in the RSDRx register might be used by the sensor as a fault bit. Therefore, this bit is latched as D0\_L in order to detect whether a fault has occurred: the eight data bits are updated every speed pulse so intermittent fault conditions could be lost. This bit is cleared-upon-read.

If the device detects an error on the sensor interface, the MSB in RSDRx (FLTBIT) will be set to '1' and the following bits will be used to report the detected errors. Otherwise, the register will contain only data information. Detailed information on data and fault reporting are explained in the following sections.

are explained in the following sections.

DS11615 Rev 2 177/280

Remote sensor interface L9680

When a fault condition is detected, the RSFLT bit of the global status word (GSW) is set to 1. Faults other than Short to Ground and Over-temperature will only clear after read, not by the disabling of channel.

Data are cleared upon reading the RSDRx register.

### 9.1 PSI5 mode

All channels are compliant to the PSI-5 v1.3 specification as described below:

- Two-wire current interface
- Manchester coded digital data transmission
- High data transmission speeds of 125 kbps and 189 kbps
- Variable data word length (8 & 10 bit only)
- 1-bit parity
- Synchronous operating mode with 3 time slots

An example of the data format for one possible PSI-5 protocol configuration is shown below. Data size and the error checking may vary, but the presence of 2 sync start bits (referenced below as sync bits) and  $2\,T_{Gap}$  time is consistent regardless.

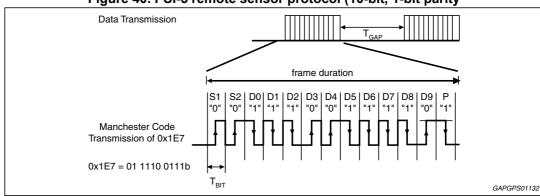


Figure 40. PSI-5 remote sensor protocol (10-bit, 1-bit parity

# 9.1.1 Functional description

The Remote Sensor Interface block provides a hardware connection between the microcontroller and up to twelve remote sensors (maximum three per channel). Each channel is independent on the others, and is not influenced by possible fault conditions occurring on other channels, such as short circuits to ground or to vehicle battery. Each channel is supplied by a current limited DC voltage derived from SATBUCK, and monitors the current sunk from its supply in order to extract encoded data. The remote sensor modulates the current draw to transmit Manchester-encoded data back to the receiver. The current level detection threshold for all channels is internally computed by the IC in order to adapt the signal level to the sensors quiescent current.

All channels can be enabled or disabled independently via SPI commands. The operational status of all channels can also be read via SPI command. All channels support individual selective sync-pulse control to allow communication back to the remote sensor via sync-pulse voltage modulation as described in the PSI5 v1.3 specification.

The message bits are encoded using a Manchester format, in which logic values are determined by a current transition in the middle of the bit time. When configured for PIS5 sensors each interface supports Manchester 2 encoding as shown in *Figure 41*. When configured for VDA sensors the protocol supported is Manchester 1.

Start bits = '00'

Logic '0'

Logic '1'

Manchester-2

PSI5

Figure 41. Manchester bit encoding

The sensor input filter time, deglitch filter, (delay until a threshold crossing is detected) can be configured in 15 steps. Filters can be selected individually for each channel, through the Remote Sensor Configuration Register, WSFILT bits

The received message data are stored in input data registers that are read out by the microcontroller via the SPI interface. For PSI5, three data registers per channel are used to store remote sensor messages received during timeslots 1, 2, and 3 respectively. Each register is updated after a certain delay (TWRITE\_EN\_DELAY) from the end of relative sensor message. All the bits inside the registers itself are simultaneously updated upon reception of the remote sensor message to prevent partial frame data from being sampled via the SPI interface. After the data for a given channel is read via the SPI interface, subsequent requests for data from this channel will result in an error response.

To allow for sampling synchronization of remote sensor data with the software in the microcontroller, the Remote sensor Interface block includes sync-pulse circuitry to signal initiation of sampling in the remote sensor. The sync-pulse is output to the remote sensors in the form of an increased voltage level on the RSUx pins when sampling is to be conducted. The higher voltage level required for the sync-pulse is sourced from the SYNCBOOST boost regulator. Pulse shaping is used to limit the slew rate of the pulses to reduce EMI. Feedback protection is provided to prevent fault conditions on one channel from affecting the others during sync-pulse generation. The microcontroller schedules the activation of the sync pulses to the four channels by providing a periodic signal to the SATSYNC pin. When a rising edge is detected on SATSYNC pin, the Remote sensor Interface block outputs sync pulses on channels RSU0-RSU3 in sequence to reduce the average current inrush to the remote sensors as shown in *Figure 42*. The voltage source in the Remote Sensor Interface block can source and sink current and is used to discharge the bus capacitance at the end of the sync pulse. The pull down device used to sink current is current limited.



DS11615 Rev 2 179/280

Remote sensor interface L9680

SATSYNC SATFD1 SATFD2 SATFD3 SATFD4

Figure 42. Remote sensor synchronization pulses

L9680 supports three time slots in a sync period with associated RSDRx registers. The messages received within one sync period are routed to the corresponding RSDRx register associated to each time slot. A time slot control is performed to check if the incoming messages fall within the valid time slots reported in Table 62 and sketched in Figure 43 If the end of the received message occurs outside a valid time slot, a SLOT ERROR fault will be detected and stored in the related RSDRx register. Slot error assignment is described in Figure 43. For instance, if the end of second message falls before expected valid time window the error slot 1 is asserted and then also the data received with the first message is lost. If two messages end within the same slot, the second message will be assigned to that slot, regardless its validity. The time slot control can be disabled by setting the TSxDIS bit in the RSCRx register.

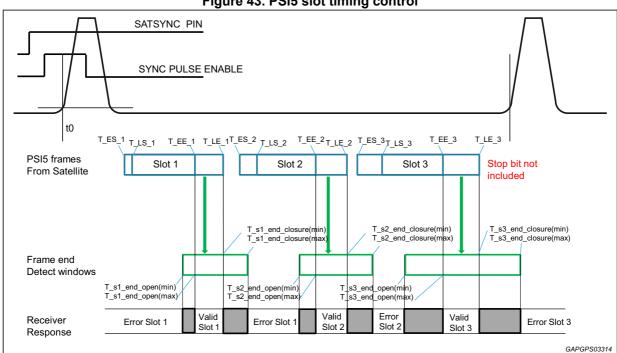


Figure 43. PSI5 slot timing control

The remote sensor interface is also able to detect faults occurring on the sensor interface. The Remote Sensor Data Register (RSDRx) will report multiple fault flags.

When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

Error bit INVALID is an OR-ed combination of the following errors:

- Start bit error outside of selected operating range
- Data length error or stop bit error
- Parity Error of received Remote sensor Message
- Bit time error (a data bit edge is not received inside the expected time window)

All fault bit related to channel error are loaded in the 3 time slot register and the fault has the priority, so the fault overwrite valid data.

## 9.1.2 Sensor data integrity: LCID and CRC

Each RSDRx data register contains a Logical Channel ID which is a 4/2-bit field for remote sensors used to link the received data to the corresponding logical channel number. Each RSDRx register contains also a CRC bit field computed on the data packet for data integrity check. To satisfy functional safety requirements LCID, DATA and CRC bit fields propagate through the same data path as a single item to the SPI output.

The polynomial calculation implemented for PSI5 data is described as in PSI5 specification  $g(x)=1+x+x^3$  with initialization value equal to '111'.

Below are the equations to calculate the CRC in combinatorial way.

CRC[2] = CRCext[0]+D[0]+D[1]+D[3]+D[6]+D[7]+D[8]+D[10]+D[13]+D[14]+D[15]

CRC[1] = CRCext[2]+D[0]+D[1]+D[2]+D[4]+D[7]+D[8]+D[9]+D[11]+D[14]+D[15]+D[16]

CRC[0] = CRCext[1]+CRCext[0]+D[0]+D[2]+D[5]+D[6]+D[7]+D[9]+D[12]+D[13]+D[14]+D[16]

Where D[16:0]= RSDR[16:0] and CRCext[n] are the starting seed values (all '1').

## 9.1.3 Detailed description

#### Manchester decoding

The Manchester decoder will support remote sensor communication as per PSI specification rev 1.3 for the modes configurable via the STS bits in the RSCRx registers. The Manchester Decoder checks the duty-cycle and period of the start bits to determine their validity, depending on the configuration of the PERIOD\_MEAS\_DISABLE bit in the RSCRx registers. The expected time windows for the mid bit transitions of each subsequent bit within the received frame are determined by means of the internal oscillator time base. Glitches shorter than 25% of the minimum bit time duration are rejected.



DS11615 Rev 2

181/280

Remote sensor interface L9680

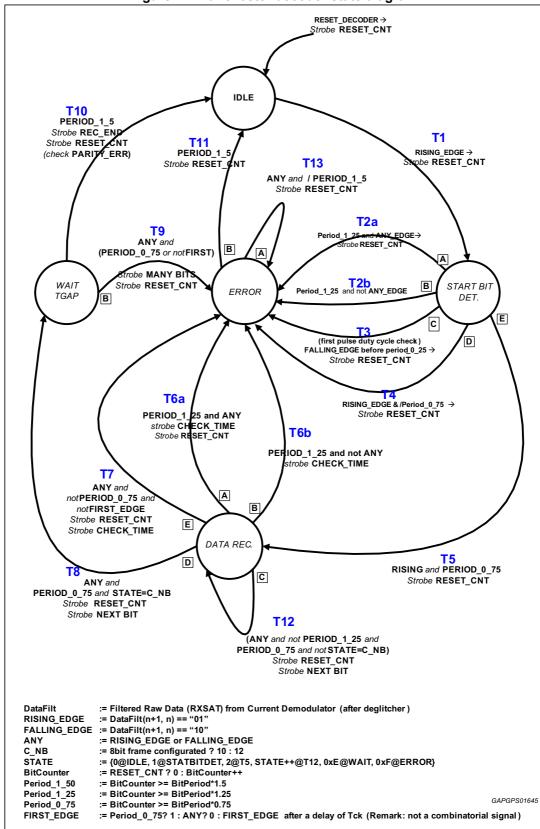


Figure 44. Manchester decoder state diagram



A Manchester Decoder Error occurs if one or more of the following are true:

- Two valid start bits are detected, and at least one of the expected 13 mid-bit transitions are not detected
- Two valid start bits are detected, and more than 13 mid-bit transitions are detected
- When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

The Manchester decoder re-initializes at the start of each timeslot, such that remote sensor frames violating timeslot boundaries will result in the setting of a Manchester Error. All errors are readable through the Sensor Fault Status Register and the RSFLT bit in the Global Status Word Register.

When a valid message is correctly decoded, the 10/8 data bits are stored into the appropriate RSDRx register together with the related LCID. The RSDRx register contains the 10/8 bits data as they are received from the sensor (no data range check/mask is done at this stage). The 8-bit data word is right-justified inside the 10-bit data field in the RSDRx registers.

#### Current sensor w/ auto-adjust trip current

The current sensor is responsible for translating the current drawn by the sensor into a digital state. Each remote sensor channel has a dedicated current sensor.

The current flowing through the RSU power stage is internally downscaled by a factor 100, sent to a 10 bits A/D converter and digitally processed to extract both the sensor quiescent and delta currents.

The delta current threshold for signal detection can either be fixed or auto-adjusted to the actual calculated sensor delta current, depending on the FIX\_THRESH bit setting in the RSCRx registers.

The current trip point is dynamically determined by adding the delta current threshold (fixed/auto-adjusted) to the quiescent current (auto-adjusted). The RSU current is compared against the current trip point to determine the current demodulator digital output. A logic '1' represents the sensor current above the current trip point. The current demodulator output is fed into the Manchester decoder and optionally to the WSx discrete output pins, depending on the configuration of the RSPTEN bit in the RSCRx registers.

Thanks to the quiescent and delta current tracking features the receiver is capable to automatically adapt to different nominal sensor currents and/or to be tolerant to sensor current drifts over lifetime.

Both the sensor quiescent and delta current tracking algorithms can be configured by setting appropriately the REDUCED\_RANGE, BLOCK\_CURR\_IN\_MSG and AVG/SSDIS bits in the RSCRx registers.



DS11615 Rev 2 183/280

Remote sensor interface L9680

## 9.2 Active wheel speed sensor

The remote sensor interface circuit conditions and decodes active wheel speed sensor signals with various pulse widths and output currents. The following sensor types are supported and selected through the Remote Sensor Configuration Register (RSCR)

- Standard active 2-level wheel speed sensors (7/14 mA)
- Three level (7/14/28 mA) VDA compliant sensor with direction and air gap information ('Requirement Specification for Standardized Interface for Wheel Speed Sensor with Additional Information', Version 2.0)
- PWM encoded 2-level sensors with 2 edges per tooth (see data sheet Infineon® IC TLE4942/BOSCH DF11)
- PWM encoded 2-level sensors with 1 edge per tooth (see data sheet Allegro® ATS651LSH/BOSCH DF11)

Received wheel speed frames from all the above sensors are decoded into signals suitable for the microcontroller through the four WSx output pins (WS0-WS3). Specific information is shown in *Figure 45*.

For all sensors, other than the standard active 2- level sensor, additional sensor data (diagnostics, etc...) are decoded and available within the Remote Sensor Data Registers (RSDR0, RSDR1, RSDR3, RSDR4). If standard active 2- level sensor is selected the content of the Remote Sensor Data Registers will be NO DATA fault.

Only for 2-level sensors (STD or PWM encoded) the user may choose to have all sensor data processed through the microcontroller by selecting pass through mode, WSPTEN, within the Remote Sensor Configuration Register (RSCR). In pass through mode, the remote sensor interface simply transforms the incoming sensor current pulses to digital voltage pulses on the WSx pins, no decoding is performed.

The sensor input filter time, deglitch filter (delay until a threshold crossing is detected) can be configured in 15 steps. Filters can be selected individually for each channel, through the Remote Sensor Configuration Register, WSFILT bits.

For PWM encoded sensors with 2 edges per tooth not in pass through mode, the standstill signal can be processed directly to the WSx output pins. This is done in the Remote Sensor Configuration Register, SSEN bit.

Since the decoder has to measure the pulses in order to determine, whether they are standstill pulses or not, the first standstill pulse will always be seen on the WSx output pins and the first not stand-still pulse after a stand-still period will be suppressed.

For 3-levels VDA sensors the device performs parity check on the received data frame. In case a parity error is detected, the INVALID fault bit of the RSDRx register will be set.

Data from the sensor are not latched: last incoming frame overwrites the previous one once validated. Faults coming from diagnostic (i.e. over current, short to ground or battery) are latched until the microcontroller reads them.

Sensor signal decoding is done according to two possible algorithms:

Auto-adjusting current trip points.

With this option, the IC is able to find sensor DC current value (named IB0) in the range from 2.5 mA to 21 mA (default is 7 mA).

The IC is also able to detect the current value of the data pulse and compute the first threshold (named Ith1): Ith1 = IB0 +  $\Delta$ Ith1/2 where  $\Delta$ Ith1 is in the range from 5 mA to 9.3 mA (default is 7 mA).



- Besides, in case of VDA selected, the ASIC is also able to recognize the current value of the speed pulse by computing a second threshold (named lth2): Ith2 = IB0 +  $\Delta$ Ith1 +  $\Delta$ Ith2/2 where  $\Delta$ Ith2 in the range from 10 mA to 18.6 mA (default is 14 mA)
- Fixed current trip points where the thresholds are set via SPI. The default value for first threshold is 9.8 mA and for second threshold is 19.6 mA

Figure 45. Wheel speed sensor protocols Three level current (VDA compliant sensor 14 mA with Manchester encoded information) 7 mA WSx pin Data and diagnostic by SPI: Three level sensors have eight data bits and a parity bit which are written into the register upon receiving. At higher speed not all bits can be transmitted. The data register for each wheel contains the number of data bits received between two speed pulses. 14 mA Two level current (Standard compliant sensor with only speed information) WSx pin Data by WSx pin (Pass-through mode) 14 mA Two level current PWM (One pulse per tooth with data encoded in pulse width) 45 us - right rotation 90 μs - left rotation 45 µs 45 µs 90 µs 90 µs (Pass-through mode) WSx pin Data by WSx pin and duty cycle by SPI Two level current PWM (Two pulses per tooth with data and diagnostic encoded in pulse width) 45 μs n x 45 μs (Pass-through mode) WSx pin Data by WSx pin and duty cycle by SPI (normal mode) GAPGPS02285

Remote sensor interface L9680

## 9.2.1 Wheel speed data register formats

When programmed as a wheel speed sensor interface, only four data registers are used (Remote Sensor Data Register RSDR0-RSDR3).

Independent data registers are defined for each wheel speed channel and their contents are determined by sensor type. Three level VDA sensors have eight data bits and. At fast wheel speed not all bits may be transmitted by the sensor: the IC is able both to process normal or either truncated frames by providing together with data, a 4 bit counter to inform the microcontroller about the number of received valid bits.

For PWM encoded sensors, each pulse length is written to the sensor data register with a typical resolution of 5  $\mu$ s per bit. In case of pulse width duration equal or higher than  $T_{STANDSTILL\_TH\_L}$  and less or equal than  $T_{STANDSTILL\_TH\_H2}$ , the standstill condition will be recognized and bit 15 in the corresponding register will be set.

The register is updated when a PWM falling edge is detected; in case of stuck-at 1 of the PWM signal the register is updated when the counter reaches the overflow value (0x1FF): in this case the standstill bit not set and the counter in overflow will signal a fault to the microcontroller.

#### 9.2.2 Test mode

In order test the input structures of the connected microcontroller, the L9680 features a wheel speed test mode that allows test patterns to be applied on the four wheel speed outputs WS0-WS3. The test mode can be entered via SPI and the test patterns can also be controlled via SPI commands. Test patterns can be composed only of static high or low signals, which can be selected via SPI. For failsafe reasons only one channel at a time can be switched into test mode.

## 9.3 Remote sensor interface fault protection

## 9.3.1 Short to ground, current limit

Each output is short circuit protected by an independent current limit. Should the output current level reach or exceed the ILIMTH for a time period greater than TILIMTH or the remote sensor interface the output stage is disabled. An internal up-down counter will count in 25 µs increment up to TILIMTH. The filter time is chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on. When the output is turned off due to current limit, the appropriate fault code STG is set in the Remote Sensor Data Register (RSDR). The fault timer latch is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Control Register (RSCTRL). This fault condition does not interfere neither with the normal operation of the IC, nor with the operation of the other channels. When a sensor fault is detected, the RSFLT bit of the GSW is set indicating a fault occurred and can be decoded by addressing the RSDR register.

In order to fulfill the blanking time requirement at channel activation as per PSI-5 specification, a dedicated masking time is applied to the current limitation fault detection each time a channel is activated.



## 9.3.2 Short to battery

All outputs are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage (10mV, minimum) to prevent disconnecting of the output under an open circuit condition. A short to battery is detected when the output RSUx pin voltage increases above SATBUCK or SYNCBOOST (depending on operation) supply pin voltage for a  $T_{STBTH}$  time. An internal up-counter will count in 1.5  $\mu$ s increment up to  $T_{STBTH}$ . The counter will be cleared if the short condition is not present for at least 1.5  $\mu$ s. The channel in short to battery is not shut down by this condition. Other channels are not affected in case of short of one output pin. As in the case previously described, the STB fault code can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The STB bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

#### 9.3.3 Cross link

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

## 9.3.4 Leakage to battery, sensor open

The sensor interface offers also open sensor detection. The auto-adjusting counter for remote sensor current sensing will drop to 0 in case the current flowing through RSUx pin is lower than 2.5 mA typ. The OPENDET fault flag is asserted when the fault condition lasts for longer than TRSUOP\_FILT deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown. This fault bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

## 9.3.5 Leakage to ground

The sensor interface offers as well the detection of a leakage to ground condition, that will possibly raise the sensor current higher than 42 mA/12 mA typ in PSI5/WSS modes respectively. The CURRENT\_HI fault flag is asserted when the fault condition lasts for longer than  $T_{RSUCH\_FILT}$  deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown. This fault bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

#### 9.3.6 Thermal shutdown

Each output is protected by an independent over-temperature detection circuit should the remote sensor interface thermal protection be triggered the output stage is disabled and a corresponding thermal fault is latched and reported through the RSTEMP flag in the Remote Sensor Data Register (RSDRx). The thermal fault flag is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Configuration Register (RSCRx).



DS11615 Rev 2 187/280

Watchdog timers L9680

# 10 Watchdog timers

This device offers a 2-level watchdog control approach. The first control level is given by means of a temporal watchdog (WD1). The WD1 window times are SPI programmable and a couple of specific codes have to be written within this window in order to serve the WD1 control. The second control level is featured by an algorithmic seed/key watchdog (WD2). Unlike the temporal watchdog, the algorithmic watchdog service must be maintained before a timeout occurs, i.e. there is no restriction on refreshing the watchdog too early. Both WD1 and WD2 watchdog functionalities can be tested trough the WD TEST SPI command.

## 10.1 Temporal watchdog (WD1)

The temporal watchdog ensures the system software is operating correctly by requiring periodic service from the microcontroller at a programmable rate. This service (watchdog refresh) must occur within a time window, and if serviced too early or too late will enter an error state reported via the FLTSR register (WD1\_WDR bit).

The overall WD1 functionality is described in the state diagram reported in Figure 46.

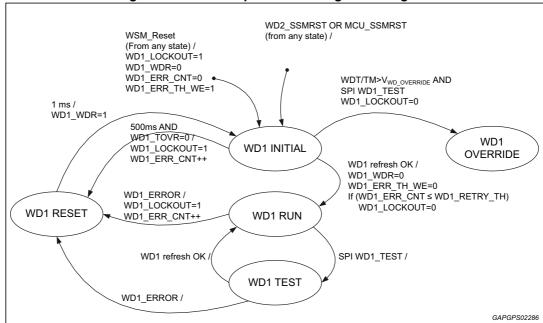


Figure 46. WD1 Temporal watchdog state diagram

Following the description of the WD1 states and signals (most of them reported in related SPI registers)

L9680 Watchdog timers

Table 13. Watchdog timer status description

State/Signal	Description			
WD1 INITIAL	Default state entered from startup. While in this state, no watchdog service is required, and the IC may stay in this state indefinitely. For system safety, all arming signals are disabled during this state to prevent deployment.			
WD1 RUN	Normal run time state where WD1 service is required.			
WD1 TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog without setting WD1_LOCKOUT=1, which can only be cleared via WSM reset. Deployment is inhibited when the WD state machine is in this state.			
WD1 RESET	State entered when a WD1_ERROR occurs. This is a timed-duration state that is automatically exited after 1ms.			
WD1 OVERRIDE	A special state used to disable watchdog functionality for development purposes. Other logic within the IC can use this state to emulate the WD1 RUN state without the need to service WD1.			
WSM_RESET	Signal used to reset the WD1 state machine to the WD1 INITIAL state and all signals to their inactive values			
WD1_refresh OK	Signal that is asserted only if the watchdog is refreshed ('A' - 'B' or 'B' - 'A' seq.) within the WD1 time window			
WD1_ERROR	Signal that is asserted if the watchdog refresh fails to occur during the WD1 time window.			
WD1_WDR	Watchdog Reset – latched signal that is activated whenever a watchdog error is qualified. For WD1, this occurs when WD1 service is required, but not received. This signal is SPI-readable.			
WD1_TM	Test Mode – a signal that indicates that WD1 is being tested. This signal is SPI-readable.			
WD1_LOCKOUT	A latched signal activated if an unexpected WD1 error occurs. This signal is permanently latched when set (until WSM_RESET). When set, all arming signals are disabled, preventing deployment. This signal is SPI-readable.			
SPI_WD1_TEST	SPI command used to enter WD1 TEST state from WD1 RUN state, or to enter WD1 OVERRIDE state from INITIAL state if WDT/TM pin voltage is greater than the threshold. This command has no effect in other states.			

## 10.1.1 Watchdog timer configuration

The watchdog timer can be configured on two different frequency modes:

- Fast watchdog with maximum range of 2ms and a resolution of 8 μs;
- Slow watchdog with maximum range of 16.3ms and a resolution of 64 μs.

The watchdog window times are SPI programmable. The configuration of watchdog timer frequency and window times can be done by setting the Watchdog Timer Configuration Register (WDTCR) with the appropriate values. However, this configuration is accepted only when the device is in the Init operating state, as shown in *Figure 11*. As soon as the device enters in Diag state, the watchdog control is enabled and the watchdog configuration is fixed and cannot be changed anymore.



DS11615 Rev 2 189/280

Watchdog timers L9680

#### 10.1.2 Watchdog timer operation

While in the WD1 INITIAL state, watchdog service must begin or a SPI command with WD1 TO DIS=1 must be received within the first 500 ms. If the WD1 Timeout Disable bit is set, the device can stay in the WD1 INITIAL state indefinitely without watchdog service.

To refresh WD1, the logic must receive a Watchdog Timer Register (WD1T) SPI command containing the expected key value within the WD1 time window (WDTMIN+WDTDELTA). If it is received too early, too late the WD1 ERROR signal will be asserted. The WD1 ERROR will not be asserted in case a SPI command containing the Watchdog Timer Register (WD1T) with an incorrect key value is received at any time relative to the window. This allows the system software to repeatedly transmit the key value until it needs to change to the correct key value. Upon reception of the correct key within the window, the logic will reset the watchdog timer to create a new window.

The timer is cleared upon writing code 'A' and code 'B' (either in 'A' - 'B' or 'B' - 'A' sequences) to the WD1CTL [1:0] bits, in the WD1T register. The watchdog timer value can be read via the WD1T register.

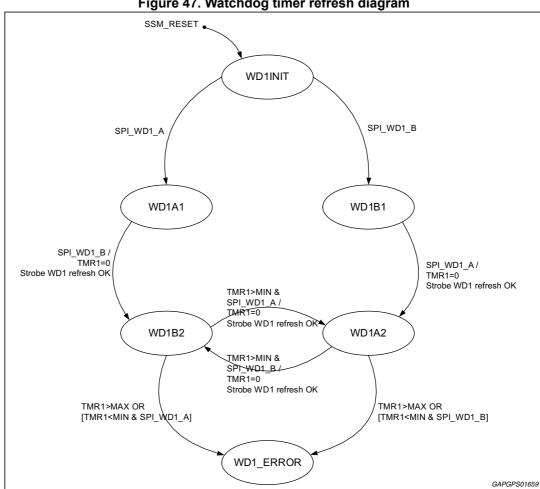


Figure 47. Watchdog timer refresh diagram

L9680 Watchdog timers

## 10.2 Algorithmic watchdog (WD2)

The algorithmic watchdog (WD2) is intended to protect higher software layers, and as such requires servicing at a much slower rate and allows for software jitter as compared with WD1. Additionally, WD2 is not implemented as a window watchdog, but is a maximum-time watchdog, where refresh is accepted at any time before the timer expires.

The overall WD2 functionality is described in the following state diagram:

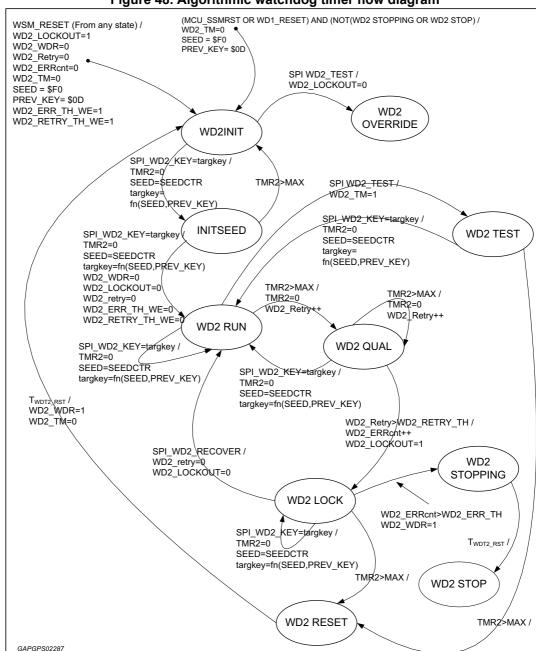


Figure 48. Algorithmic watchdog timer flow diagram

Watchdog timers L9680

Following the description of the WD2 states and signals (most of them available through SPI registers)

Table 14. WD2 states and signals

State / Signal	Description		
WD2 INIT	Default state entered from startup or after a SSM reset (if not in WD2 STOP state).		
WD2 OVERRIDE	Special state used to disable WD2 watchdog functionality.		
WD2 INITSEED	State entered when the correct default key is received in INIT state. Here the timer starts to count waiting for the real first key.		
WD2 RUN	Normal run-time state where WD2 service is required.		
WD2 TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog without affecting WD2 error (no reset is generated, WD2_LOCKOUT stay low). Only WD2_WDR latch could be set to 1, in this way $\mu$ C is able to verify the functionality of the watchdog.		
WD2 QUAL	A state used to qualify a number of WD2_ERROR occurrences before action is taken. The intent is to use this state to permit a retry strategy to account for software jitter.		
WD2 LOCK	A state entered after the allowed retries have been exhausted. This is where action is taken due to WD2 service failure.		
WD2 STOPPING	This is a timed-duration state that is automatically exited after 1ms		
WD2 STOP	A state used to prevent continual recovery of WD2 errors using the WD2_KEY key mechanism to restart watchdog service.		
WD2 RESET	State entered when a WD2_ERROR occurs after having been qualified in the WD2_QUAL state (when all retries are exhausted), or when testing the WD2. This is a timed-duration state that is automatically exited after 1ms.		
WSM_RESET	Watchdog State Machine reset – used to force a transition to the WD2 INIT state and reset all signals to their inactive states		
WD2_RETRY	Counter that tracks the number of retry attempts. It is incremented each time the logic detects a WD2 error while qualifying the error.		
WD2_WDR	Watchdog Reset – latched signal that is activated whenever a watchdog error is qualified. For WD2, this occurs when WD2 service not received after all retry attempts have previously failed. This signal is SPI-readable.		
WD2_TM	Test Mode – a signal that indicates that WD2 is being tested. This signal is SPI-readable.		
WD2_LOCKOUT	A latched signal that is activated on startup, or whenever a WD2 error is fully qualified (all retry attempts have failed). Recovery is still possible after this is set going into WD2 RUN state. This signal drives the WD2_LOCKOUT output pin. This signal is SPI-readable.		
SPI_WD2_TEST	SPI command used to enter WD2_TEST state or to enter WD2 OVERRIDE state from INIT.		
TMR2	Timer to count the maximum time limit to receive the correct key		
SPI_WD2_RECOVER	SPI command used to clear retry counter		
WD2_ERR_CNT	Counter that tracks the number of WD2 error occurred		



L9680 Watchdog timers

To refresh WD2, the logic must receive a WD2\_KEY command containing the expected key value before the WD2 timer expires. If it is received too late the refresh criteria have not been met. The WD2 error is asserted if the refresh does not occur before the end of the timeout. The WD2 error is not asserted if it receives continuously a WD2\_KEY command with the correct key. This allows the system software to repeatedly transmit the correct key value at any rate faster than the required timeout.

Upon reception of the correct key, the logic will generate a new seed value, then calculate a new key using the new seed and reset the watchdog timer to create a new timeout.

When in WD2 INITSEED state, the three steps above are executed anyway. The seed is latched from a free-running counter that starts when WSM is released. The WD2\_KEY command is used for transmission of the watchdog key, while WD2\_SEED command is used to read the new seed and the previous key.

The SEED is generated by latching the value from a free-running counter. The free-running seed counter runs at a rate of  $f_{WD2\_SEED}$  as specified in *Table 29*. The key value and seed value are 8-bits in length. The key shall be calculated as follows: (KEY = SEED  $\ddagger$  PrevKEY + \$01) where  $\ddagger$  denotes a bit-wise XOR operation

# 10.3 Watchdog reset assertion timer

Upon either a WD1 or a WD2 watchdog reset, the watchdog logic will momentarily assert the RESET pin for time duration  $T_{WDT1\_RST}$ /  $T_{WDT2\_RST}$ . When the RESET pin has been asserted through the watchdog reset assertion timer, stored faults are maintained and can be read by the microcontroller via SPI following the RESET period.

# 10.4 Watchdog timer disable input (WDT/TM)

This input pin has a passive and active pull-down and is used to disable the watchdog timer. The state of this pin can be read by SPI through the WDT/TM\_S bit in the GSW register. When WDT/TM pin is asserted, the watchdog timer is disabled, the timer is reset to its starting value and no faults are generated.

The WDT/TM input pin must not be biased HIGH (WDT/TM > V<sub>WDTDIS\_TH</sub>) prior to POR in order to have a proper start-up.

577

DS11615 Rev 2 193/280

DC sensor interface L9680

## 11 DC sensor interface

L9680 implements a circuitry able to interface with a variety of positioning sensors. The sensors that can be connected to the device are Hall-effect, resistive or simple switches.

Range of measurements is:

Resistive sensor: 65 Ω to 3 kΩ
 Hall-effect sensor: 1 mA to 2 0 mA.

Within the above ranges, accuracy of  $\pm 15\%$  is granted. A reduced accuracy is given in the range 1 mA to 2 mA. Hall sensor and switch interface block diagram is shown below.

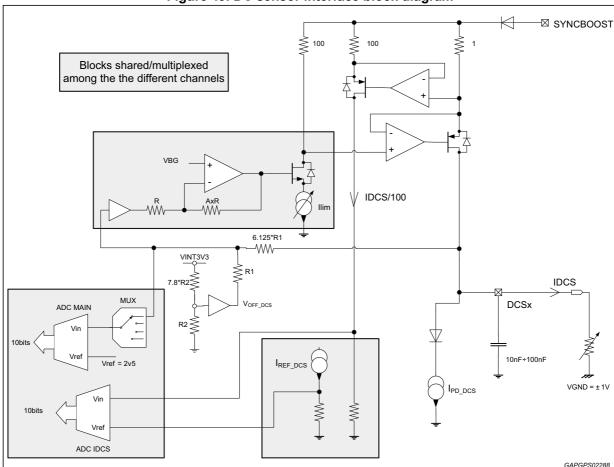


Figure 49. DC sensor interface block diagram

The global SPI contains several bits to control and configure the interface. The SWOEN bit is used to enable the output voltage on DCSx pins. The channel to be activated can be chosen by accordingly setting CHID bits. The interface activation is started and switched off upon user SPI command. Alternatively it could be configured via the SYS\_CFG(EN\_AUTO\_SWITCH\_OFF) bit to automatically switch off as soon as the measurement is complete, in case of current or resistance measurements; this would help preventing thermal conditions. The interface would not auto-switched off in case of voltage measurement, instead.

L9680 DC sensor interface

The voltage and current for the selected channel are made available to the main ADC by selecting the proper channel and enabling the measurement process by dedicated DIAGCTRLx commands.

The device offers the capability to actively keep all the DCSx lines discharged by means of a weak pull down. The pull down is active by default on all channels and it is deactivated in either of the following cases:

- 1. when the voltage source is active on the relevant channel
- 2. when a voltage measurement is requested on the relevant channel
- 3. if SPI bit SWCTRL(DCS\_PD\_CURR) is set (global pull-down disable for all channels)

In case of Hall-effect sensors, a single current measurement is processed. The current load needed for regulating the pin is internally reflected to a reference resistance, whose voltage drop is then measured through the internal ADC converter.

When resistive or switch sensors are used, a more complex measurement is performed. In a first step the current information as above described is provided. Then, also the information on the voltage level achieved on the output pin is provided via ADC. By processing these two values, the micro-controller can understand the resistive value. The DCSx voltage is internally rescaled by a voltage divider into the ADC converter voltage range as shown in Figure 48. Additionally a positive voltage offset is internally applied to the scaled voltage in order to allow voltage measurement capability for DCSx down to -1V.

In order to get accurate resistive information even in case of an external ground voltage shift on the sensor of up to +/-1V, the voltage measurement step actually needs two DCSx voltage measurements. A first voltage measurement has to be done with selection of 6.25V on the output channel and a second one with the regulator switched off. The difference between the two measurements will cancel out the offsets (both external ground shift and internal offset).

The DCSx current and voltage can be retrieved from ADC readings according to the following formulas and related parameters specified in the Electrical Characteristics section.

$$\begin{split} I_{DCSx} &= 100 \cdot \frac{I_{REF\_DCS}}{2} \cdot \text{DIAGCTRLn}(\text{ADCRESn}) \quad \text{@DIAGCTRL}(\text{ADCREQn} = \$04) \\ V_{DCSx} &= \text{RATIO}_{VDCSx} \cdot \left( \frac{\text{ADC}_{REF\_hi}}{2} \cdot \text{DIAGCTRLn}(\text{ADCRESn}) - \text{V}_{OFF\_DCSx} \right) - \\ &- \text{V}_{OFF\_DCSx} \cdot (\text{RATIO}_{VDCSx} - 1) \quad \text{@DIAGCTRLn}(\text{ADCREQn}) = \$03 \end{split}$$

The DCSx sensor resistance can be calculated according to the following formula:

$$\mathsf{R}_{\mathtt{sensor}_{\mathsf{x}}} = \frac{\Delta \mathsf{V}_{\mathtt{DCSx}}}{\mathsf{I}_{\mathtt{DCSx}}} = \frac{\mathsf{V}_{\mathtt{DCSx}}@(\mathsf{SWCTRL}(\mathsf{SWOEN}) = 1 - \mathsf{V}_{\mathtt{DCSx}}@(\mathsf{SWCTRL}(\mathsf{SWOEN}) = 0)}{\mathsf{I}_{\mathtt{DCSx}}}$$

@SWCTRL(CHID) = x

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.



DS11615 Rev 2 195/280

DC sensor interface L9680

Each output is protected against

- Overload conditions by current limit
- Ground offset between the ECU and the loads of up to ±1 V.
- Loss of ECU battery
- Loss of ground
- Unpowered shorts to battery
- Shorts to ground

## 11.1 Passenger inhibit interface

L9680 provides a feature to deactivate passenger restraint devices based on a preprogrammed mask. It generates a signal (PSINHINT) based on microcontroller-initiated measurements performed on DC Sensor channel 0. The PSINHINT signal is bitwise ANDed with the LOOP\_MATRIX\_PSINH mask register, allowing selective deactivation of squib loops independent of microcontroller control. This signal is also inverted and output on the PSINHB pin of the IC to activate externally controlled squib loops.

Figure 50. Passenger inhibit logic diagram SWCTRL(CHID) = '0000' SYS\_CFG(DCS\_PAD\_V) ADCREQ y[6:0] = DCSx I  $ADCREQ_y[6:0] = DCSx_V$ SAFING state DCS0 ON NEWDATA\_y ADCRES\_y[9:0] In window Down CTR PADTHRESH HI SET to 1s PADTHRESH LO SSM RESET CLR PSINH POL 0: Outside window inh DEP DISABLED state 1: Inside window inh 250Hz **PSINHINT** DIAG state **PSINHB** DSTEST(PSINH) **PSINHSEL** GAPGPS02289

An upper and lower threshold is preprogrammed via SPI by writing the desired 10-bits values into the PADTHRESH\_HI and PADTHRESH\_LO registers during the Diag state. These thresholds define the measurement window where the passenger restraints are active. Any measurement outside this window will result in the assertion of the PSINHINT signal (as described below), thereby deactivating the squib loops identified in the PSINH mask. The PSINH mask is also preprogrammed during the Diag state.

L9680 DC sensor interface

Another control (DCS\_PAD\_V bit in SYS\_CFG register) is preprogrammed to select either a voltage measurement or a current measurement on DCS0 for this purpose.

The automated control of the PSINHINT signal occurs when the microcontroller runs diagnostic testing of the DCS0 interface. A 1 second timer is included to ensure the diagnostic test is run periodically. When the timer expires (down-counts to 0), the PSINHINT signal is asserted. When the measurement of the DCS0 voltage or DCS current (as selected by the DCS\_PAD\_V bit) is taken, and the value falls within the preprogrammed window, the timer will be reloaded. If the measurement is outside the window, the timer will not be reloaded, and it will continue to count down until it expires, resulting in activation of PSINHINT. For testing purposes, the PSINHINT can be controlled directly via SPI while in DIAG state using the Diag State Test Selection (DSTEST) register.

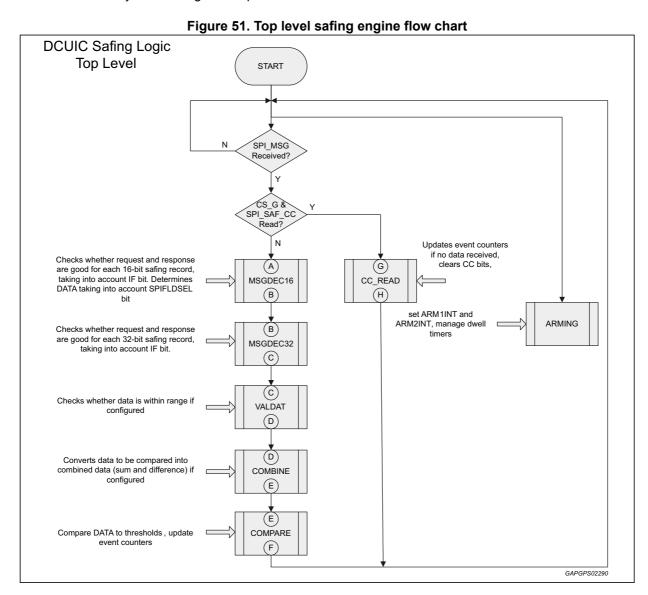


DS11615 Rev 2 197/280

# 12 Safing logic

## 12.1 Safing logic overview

The integrated safing logic uses data from on-board and remote locations by decoding the various SPI communications between the interfaces and the main microcontroller. The safing logic has several programmable features enabling its ability to decode SPI transmissions and can process data from up to 16 sensors. The operating mode involves simple symmetrical data threshold comparisons, with the use of symmetrical or asymmetrical counters. A high level diagram is shown in the figure below. Please note that this top-level diagram is simplified, and references more detailed flowcharts to show a) message decoding, b) valid data limits, c) effects of the 'combine' function, d) comparison to thresholds and arming, and e) the setting of the 'compare complete bit. Four independent arming outputs, ARM1INT, ARM2INT, ARM3INT and ARM4INT, are also mapped internally to any of the integrated squib drivers.



#### SPI sensor data decoding 12.2

Sensor data is regularly communicated with the main microcontroller through multiple SPI messages. The L9680 monitors SPI traffic on MISO\_RS bus. Since not all communications between sensors and the microcontroller contain data, it is important for the decoder to properly sort the communications and extract only the targeted data. The solution involves defining specific masking functions, contained within independent safing records, programmed by the user. The following figures detail the SPI message decoding methodology and the ensuing comparisons of valid sensor data to the programmed thresholds.

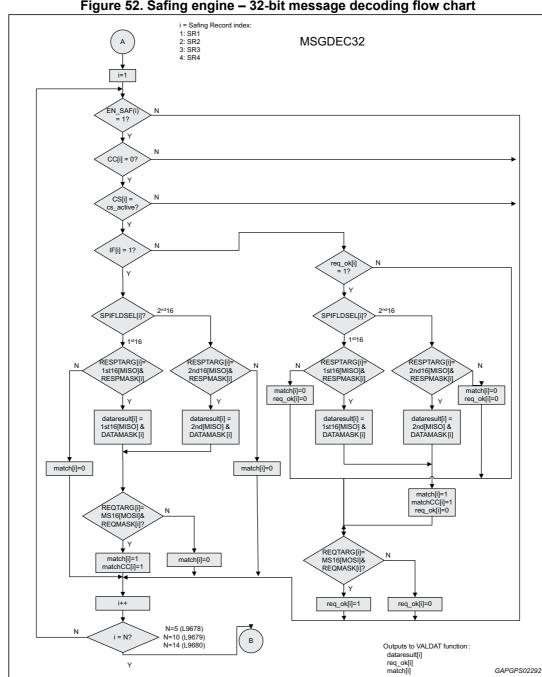


Figure 52. Safing engine - 32-bit message decoding flow chart

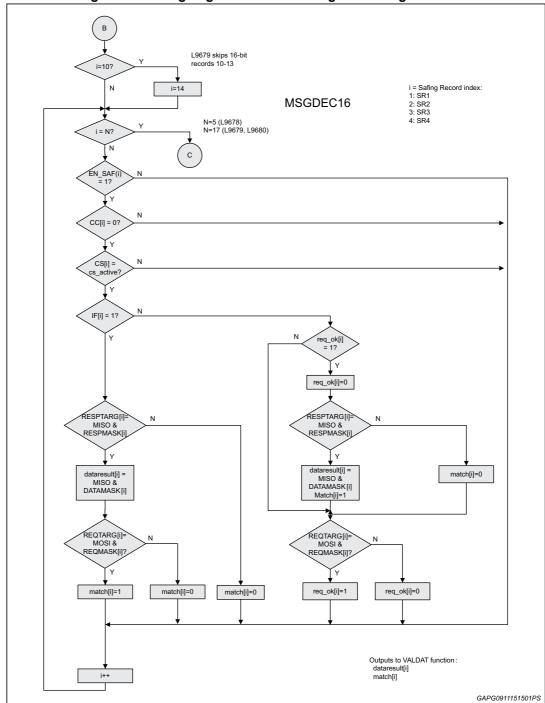


Figure 53. Safing engine - 16-bit Message decoding flow chart



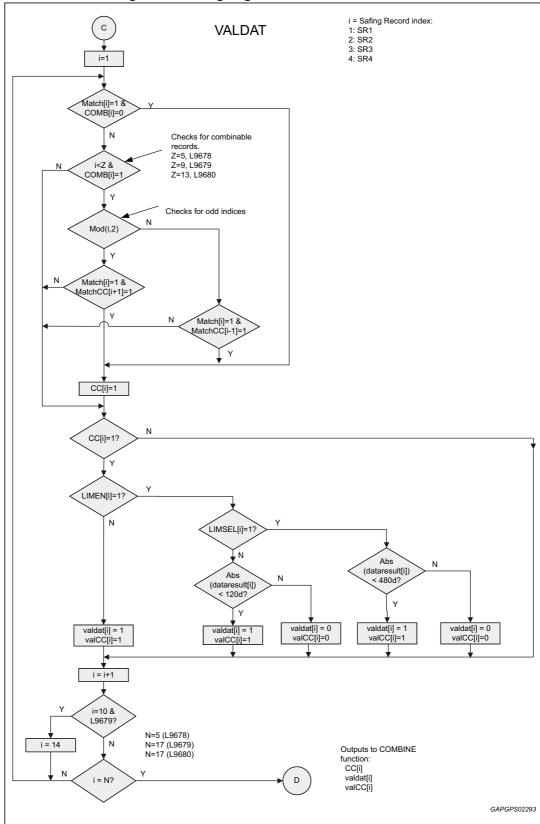


Figure 54. Safing engine - Validate data flow chart



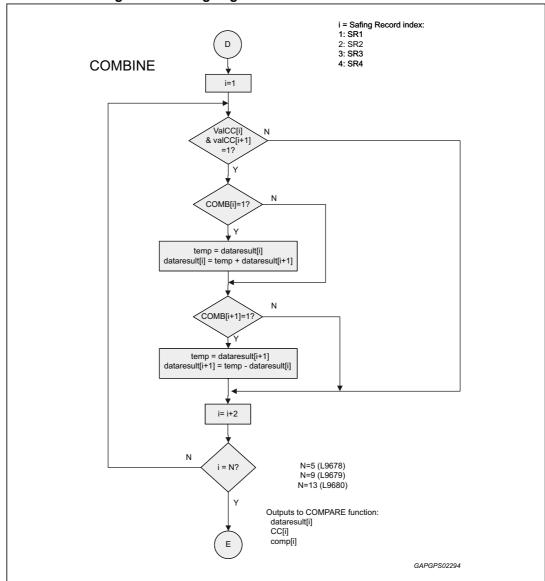


Figure 55. Safing engine - Combine function flow chart



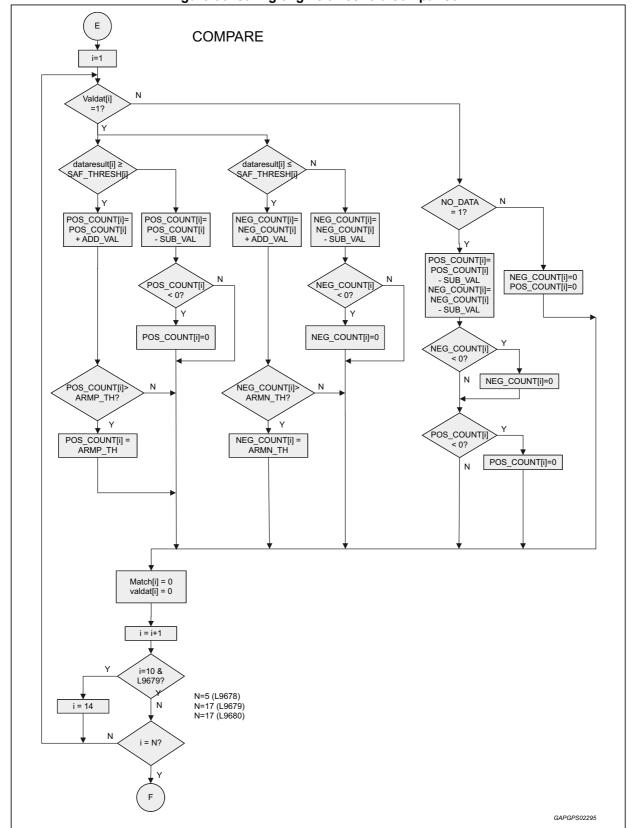


Figure 56. Safing engine threshold comparison



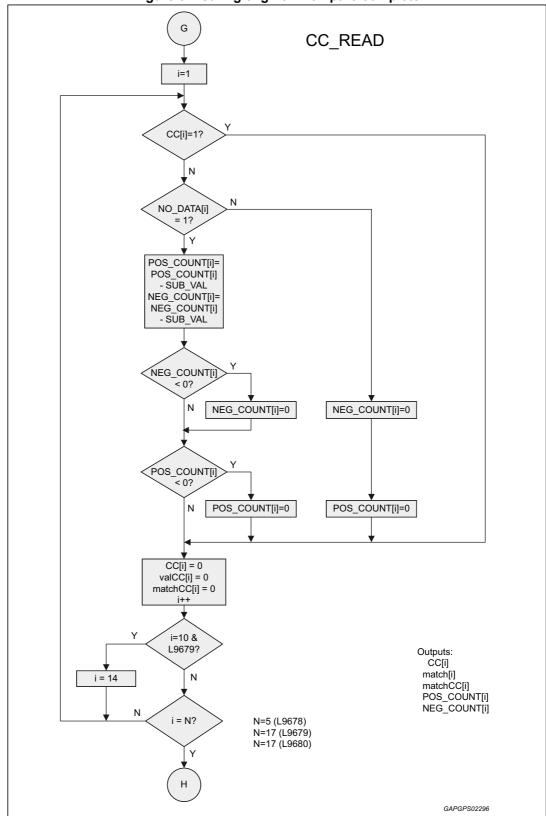


Figure 57. Safing engine - Compare complete



Each safing record has SPI accessible registers defined in the SPI command tables and summarized below:

- Request Mask and Request Target to understand what sensor the microcontroller is addressing
- Response Mask and Response Target to identify the sensor response
- Data Mask to extract relevant sensor data from the response.
  - Sensor data is extracted as a bit-wise AND result of the SAF\_DATA\_MASKx and monitored RS\_MISO data. The configuration of the set bits of the DATAMASK must be contiguous for both 16-bit and 32-bit records. The 32-bit records are comprised of Part1 as MSW and Part2 as LSW.
  - The extracted data is then right justified into a 16/32 bit register for 16/32 bit safing records, respectively, prior to further processing steps which assume data is signed should be "using two's complement representation".
- Safing Threshold specific value that sets the comparator limit for successful arming
- Control:
  - IF, In Frame to indicate serial data response is 'in frame'. There are two types of potential serial data responses, 'in frame' and 'out of frame'.
  - CS to align safing record with a specific SPI CS. The device contains 5 SPI CS inputs for the safing function (CS RS, SAF CSx)
  - ARM there are four internal arming signals, each active record is assigned or mapped to any arming signal. Several safing records can be mapped to a single arming output. ARMx outputs can be enabled also simultaneously.
  - Dwell Once an arming condition is detected, the safing record remains armed for the specified dwell time.
  - Comb (Combined Data) specific solution for dual axis high-g sensors specifically oriented off-axis.
  - LimEn (Limit Enable) to enable PSI5 out-of-range control.
  - LimSel (Limit Select) to select PSI5 out-of-range thresholds between 8-bit and 10-bit protocol.
  - SPIFLDSEL (SPI Field Select) to determine which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. Don't care for messages less than 32 bits.

If input packet matches multiple safing records, the safing engine should process all of them and treat them independently.

Safing record can only be evaluated on the first matching input packet. Any further data packet matches are ignored (i.e. once CC is set, record can't be processed until CC is cleared)

The En (Record Enable) bit for any record is programmable as on or off at any time and will enable/disable the record itself upon the following SATSYNC.

All CC bits are available in one register (SAF\_CC) for access in one single SPI read. After ARMing is achieved and CC is set, no further messages are considered until CC is cleared via read.

Safing Engine must not process sensor data in any state but Safing state (refer to *Figure 11*).

All safing records are cleared on SSM RESET.



DS11615 Rev 2 205/280

Comb (Combined Data) bit allows combining X and Y for off-axis oriented sensors. In this case, it is typical for such orientations to add or subtract the sensor response to translate the sensor signal to an on-axis response. Only couples of 16-bit long records have this feature (i.e. 1&2, 3&4, 5&6, 7&8, 9&10, 11&12).

Records are added and subtracted and results compare against two thresholds. Safing engine will process data as follows:

- Use record(n) and record(n+1), where n = 1, 3, 5, 7, 9, 11.
- The matching inputs used for math combinations are processed only after both are captured.
- The sum of the two matching inputs will be compared to the threshold of record(n).
- The difference of the two records will be compared to the threshold of record(n+1).
- If the Comb feature was enabled on only one of the two records in a couple, math would be performed only on it as shown in *Figure 56*

Example of Combine Function operation:

Record # Combine Bit Data Resulting value Record Threshold Configuration Result

Table 15. Example of combine function operation

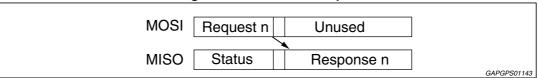
All items in the safing records, except En(Record Enable) bit, can be configured only in Diag state (refer to *Figure 11*). Additionally, the global bit to select internal or external safing engine is set in Init state.

# 12.3 In-frame and out-of-frame responses

Some sensors will communicate data within the current communication frame while others will send data on the next communication frame. Sometimes this is sensor specific and sometimes this is due to the amount of data to be transmitted. A simplified diagram shows the basic communication differences of in and out of frame responses.

In-frame example:

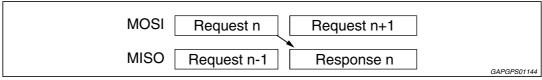
Figure 58. In-frame example



At least one bit needed to allow for synchronization between clock domains (SPI clock and system clock).

Out-of-frame example:

Figure 59. Out-of-frame example



Synchronization between clock domains relies upon inter-frame gap.

# 12.4 Safing state machine operation

State machine operation is disabled when the safing state machine reset signal is active as described in the power supply diagnostics and controls section of this document. The outputs of the state machine are ARMxREQ. As previously stated, there is a maximum of 16 safing records available to the state machine. Inputs to the safety state machine are programmed safing records and sensor data. The configuration of the state machine is common to all sensors.

#### 12.4.1 Simple threshold comparison operation

In this mode, sensor data received through the sensor SPI interface and validated by the safing record is passed to the safing algorithm. The simple threshold comparison algorithm compares the received data to two thresholds, SAF\_TH (positive threshold) and (-SAF\_TH) (negative threshold). If the sensor data is greater than SAF\_TH or is less than (-SAF\_TH) then and event is flagged and the event counter is incremented based on the programmed value of ADD\_VAL. If sensor data does not trigger the SAF\_TH comparators, the counter is decremented by SUB\_VAL. SUB\_VAL is programmed by the user and can be same or different than ADD\_VAL. This feature allows for an asymmetrical counter function making the system either more or less sensitive to sensor data. Since sensor data can indicate a positive or negative event, the algorithm maintains separate event counters, POS\_COUNT and NEG\_COUNT. ADD\_VAL and SUB\_VAL programmed values are the same for both event counters.

On each sensor sample, the event counters, POS\_COUNT and NEG\_COUNT, are updated based on the SAF\_TH comparators. Likewise, each event counter is compared with a corresponding arming threshold. In this case, POS\_COUNT value is compared to ARMP\_TH and NEG\_COUNT to ARMN\_TH. ARMP\_TH and ARMN\_TH are programmable thresholds set by the user. The compared result will set ARMP and ARMN to either '1' or '0' depending on the comparison status. If ARMP\_TH or ARMN\_TH are set to 0, the arming will be activated immediately entering in safing state.

POS\_COUNT and NEG\_COUNT are not updated if microcontroller stops reading SAF\_CC bits (this must be avoided otherwise ARMING set and reset will not be possible).

By way of the assignment of the ADD\_VAL, SUB\_VAL, ARMP\_TH and ARMN\_TH settings, the safing engine can be configured to assert arming for either a simple accumulation of COUNTs in a non-consecutive manner, or it could be set to require some number of consecutive samples.

## 12.5 Safing engine output logic (ARMxINT)

SPI messages are monitored and mapped to specific safing records. Each safing record is configured with its own threshold, dwell time and the appropriate ARMxINT signal to activate if safing criteria are met.

Any enabled safing record can be programmed to an arming signal. All safing records arming status is logically 'OR'd' to its programmed arming signal. For example, if safing records 1, 2, 4 are programmed to ARMINT1 and the records are enabled, any of the records can set the ARMINT1 signal. Configuration of safing record mapping to ARMXINT signals is specified in the in the SAF\_CONTROL\_x register (refer to *Table 67*).

While in Diag state, L9680 allows diagnostics of the squib driver HS and LS FETs, ARM pins, VSF output and firing timers. The ARM and VSF output tests are mutually exclusive.

For safety purposes, the safing logic circuitry is physically separated from the circuitry that contains the deployment logic.



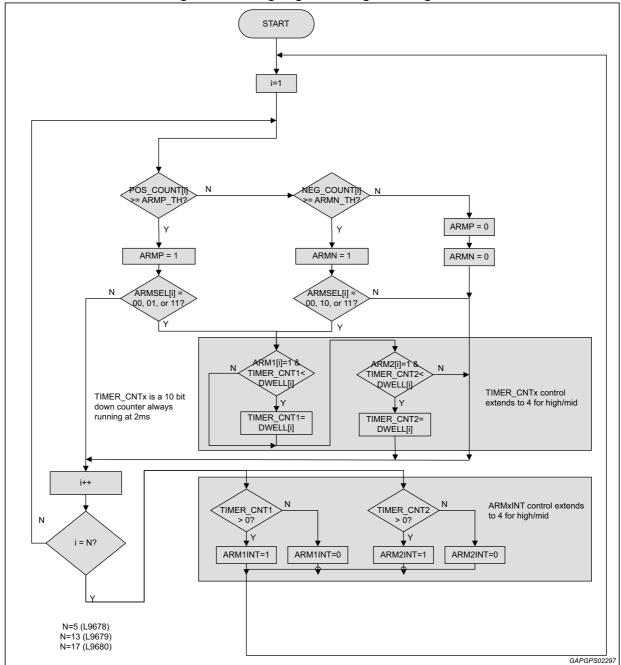


Figure 60. Safing engine arming flow diagram

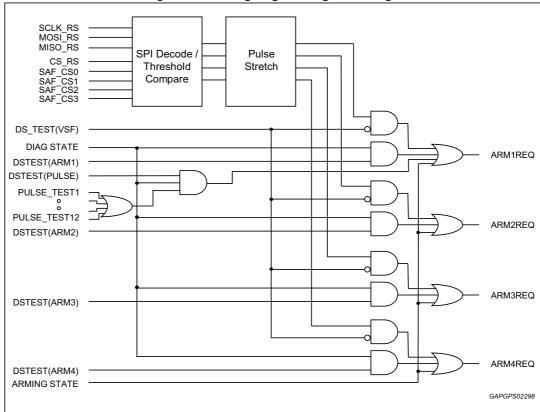


Figure 61. Safing engine diagnostic logic

A configurable mask for each internal ARMxINT signal is available for all of the integrated deployment loops. The un-masked ARMxINT signal for each loop will enable the respective loop drivers.

Activation of VSF (regulation rail for High Side Safing FET) occurs upon ARMxINT. Actual High Side Safing FET activation still requires microcontroller signal.

L9680 is able to provide arming signals to external deployment loops by means of four discrete output ARMx pins.

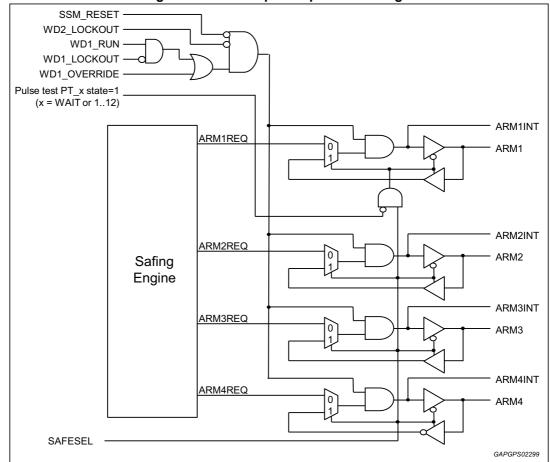


Figure 62. ARMx input/output control logic

## 12.5.1 Arming pulse stretch

Upon a valid command processed by the safing logic, the Dwell bit to stretch the arming time assertion (dwell time) applies to each safing record and is used to help safe the deployment sequence to avoid undesired behaviour.

Once dwell time has started, it will continue, regardless of the En (Record Enable) bit. Dwell will be truncated in case of SSM reset. Dwell values in the safing records are transferred to the ARMx signals. A dedicated counter is designed for each ARMx output pin. If different dwell values are assigned to the same ARMx, the longer value is used. Dwell times can only be extended, not reduced. If the remaining dwell time is less than the new dwell extension setting, the new setting will be loaded into the dwell counter.

Dwell times are user programmable.

The behaviour of the pulse stretch timer is shown below.

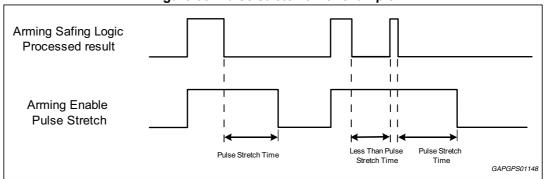


Figure 63. Pulse stretch timer example

The Arming Enable Pulse Stretch Timer status is available in the AEPSTS register.

#### 12.6 Additional communication line

The ACL pin is the Additional Communication Line input that provides a means of safely activating the arming outputs (ARMx and VSF) for disposal of restraints devices at the end of vehicle life.

The handshake sequence for activating the Arming outputs is illustrated in Figure 64. The strategy involves generation of a seed value from within the L9680 device using a freerunning 8-bit counter running at f<sub>SCRAP</sub> <sub>SEED</sub> rate, where it can be read by the microcontroller. The microcontroller uses it to generate an 8-bit key value. When the seed value is read (SPI SCRAP\_SEED command), L9680 also freezes the seed value and computes its own key, which is used for comparison to the key subsequently submitted by the microcontroller. The key value is submitted by the microcontroller using the SCRAP\_KEY command, and successful reception of this command with a key value matching the internally calculated key allows the successful completion of the first handshake. After that, in case a second handshake (seed-key) completes successfully and if a valid ACL is detected (as described below) the L9680 transitions from Scrap state to Arming state. To remain in Arming state the microcontroller must periodically refresh L9680 with the SCRAP KEY command containing the correct key value in the data field of the command, and L9680 must also receive the correct ACL signal. This must occur before the scrap timeout timer expires ( $T_{SCRAP\ TIMEOUT}$ ). The scrap key is derived from the seed value using a simple logical inversion on the even-numbered bits (0, 2, 4, 6). From a logical standpoint, this is equivalent to a bit-wise XOR of the seed value with 0x55.

While the SSM is in Arming state, the arming outputs are asserted (ARMx=1, VSF on). If the periodic scrap key is incorrect, or not received before the timeout expires, or the ACL is not correctly received, the SSM reverts back to the Scrap state, and the arming outputs are deactivated.

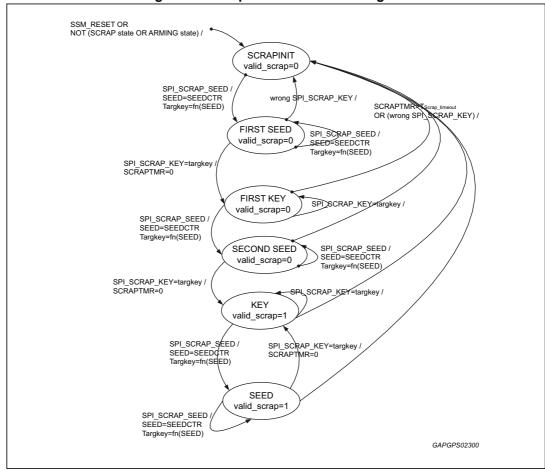
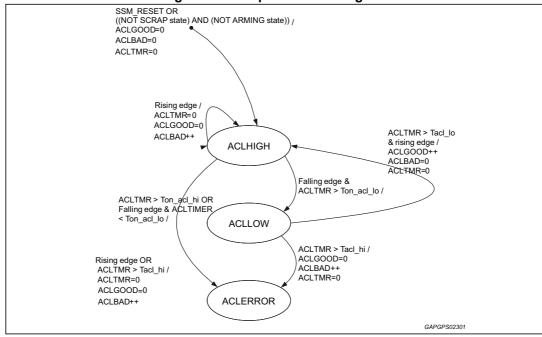


Figure 64. Scrap SEED-KEY state diagram

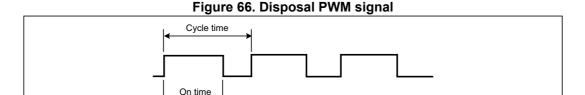




A specific waveform needs to be present on ACL input in order to instruct L9680 to arm all deployment loops. L9680 is designed to support the Additional Communication Line (ACL) aspect of the ISO-26021 standard, which requires an independent hardwired signal (ACL) to implement the scrapping feature. The disposal signal may come from either the vehicle's service connector, or the systems main microcontroller, depending on the end customer's requirements.

The arming function monitors the disposal PWM input (ACL pin) for a command to arm all loops for vehicle end-of-life airbag disposal. The disposal signal characteristic is shown in *Figure 66*. To remain in Arming state, at least three cycles of the ACL signal must be qualified (in addition to the periodic KEY value being received from the microcontroller). For the device to qualify the periodic ACL signal, the period and duty cycle are checked. Two consecutive cycles of invalid disposal signal are to be received to disqualify the ACL signal.

If the logic detects that the signal is incorrect or missing while in Scrap state, the device will stay in Scrap state; would it happen in Arming state, it will transition to Scrap state immediately.



The disposal PWM signal cycle time and on time parameters can be found in the electrical parameters tables.

47/

# 13 General purpose output (GPO) drivers

The L9680 contains three General Purpose Output (GPO) drivers configurable either as high-side or low-side modes. The drivers can be independently controlled in ON-OFF mode or in PWM mode setting the desired duty cycle value through the GPO Control Register (GPOCTRLx).

For low side driver configuration, the GPODx pin is the drain connection of an internal MOSFET and is the current sink for the output driver. The GPOSx pin is the source connection of the internal MOSFET and is externally connected to ground. For high side driver configuration, the GPODx pin will be connected to battery and GPOSx pin will be connected to load's high side.

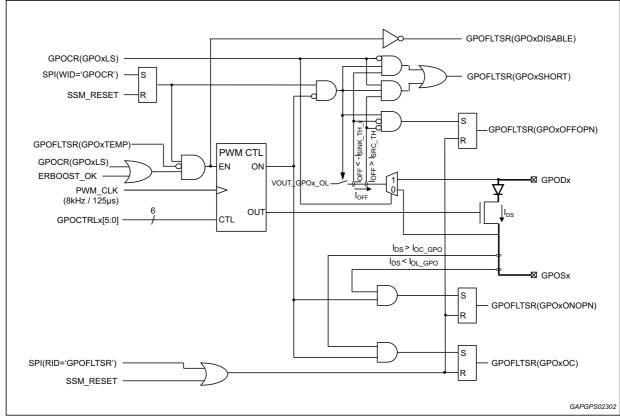


Figure 67. GPO driver and diagnostic block diagram

The drivers are configured in one of the two modes through the GPO Configuration Register (GPOCR) register. This hardware configuration is only allowed during the Init and Diag states.

When configured as high-side, the drivers need ER Boost voltage to be above the  $V_{\text{ERBST\_OK}}$  threshold to be enabled.

The default state of all drivers is off. The drivers can be independently activated via SPI control bits on GPO Control Register (GPOCTRLx). In addition, a set point on the GPOCTRLx will control the output drivers in PWM with a 125Hz frequency. If PWM control is desired, user should set the needed set point in the GPOxPWM bits of the GPOCTRLx while activating the interface. When all bits are set to '0', the GPOx output will be disabled.

577

DS11615 Rev 2 215/280

PWM control is based on a 125Hz frequency. 6 bits of GPOCTRLx are reserved to this mode, in order to control the drivers with 64 total levels from a 0% to a full 100% duty cycle.

When both GPO channels are used in PWM Mode at the same frequency they are synchronized to provide parallel configuration capability.

PWM control is implemented through a careful slew rate control to mitigate EMC emissions while operating the interface. The driver output structure is designed to stand -1V on its terminals and a +1V reverse voltage across source and drain.

The GPO driver is protected against short circuits and thermal overload conditions. The output driver contains diagnostics available in the GPO Fault Status Register (GPOFLTSR). All faults except for thermal overload will be latched until the GPOFLTSR register is read. Thermal overload faults will remain active after reading the GPOFLTSR register should the temperature remain above the thermal fault condition. For current limit faults, the output driver will operate in a linear mode (ILIM) until a thermal fault condition is detected.

Over-temp Detect

SPI(GPOCTRLx[5:0]=000000)

SSM\_RESET

SPI(RID='GPOFLTSR')

SSM\_RESET

GAPGPS02303

Figure 68. GPO Over temperature logic

The device offers also an open load diagnostics while in ON state. The diagnostics is run comparing the current through the output stage with a reference threshold I<sub>OpenLoad</sub>: should the output current be lower than the threshold, the open detection flag is asserted.

The device is also able to detect a fault condition during the OFF state by means of the Voltage Regulator Current Monitor (VRCM) block. During the OFF state the VRCM block tries to force a voltage  $V_{OUT\_GPOx\_OL}$  (2.5 V) on GPOD pin if LS mode is selected (with a current limitation of  $I_{LIM\_GPOD\_SRC/SINK}$ ) or on GPOS pin if the HS mode is selected (with a current limitation of  $I_{LIM\_GPOS\_SRC/SINK}$ ) and, at the same, it compares the current sourced or sunk in order to detect if a fault on GPO pins is present. The diagnostic in OFF state is able to detect the open load in both HS and LS modes, the short to ground fault in LS mode and the short to battery fault in HS mode:

	LS MODE		
	GPOxSHORT	GPOxOFFOPN	Interpretation
I <sub>OFF</sub> > I <sub>SRC_TH</sub>	1	0	Short to ground
- I <sub>SINK_TH_LS</sub> < I <sub>OFF</sub> < I <sub>SRC_TH</sub>	0	1	Open
I <sub>OFF</sub> < - I <sub>SINK_TH_LS</sub>	0	0	Normal

Table 16. Short to ground fault in LS mode



Table 17. Short to battery fault in HS mode

	HS I	MODE	
	GPOxSHORT	GPOxOFFOPN	Interpretation
I <sub>OFF</sub> > I <sub>SRC_TH</sub>	0	0	Normal
- I <sub>SINK_TH_HS</sub> < I <sub>OFF</sub> < I <sub>SRC_TH</sub>	0	1	Open
I <sub>OFF</sub> < - I <sub>SINK_TH_HS</sub>	1	0	Short to battery



# 14 System voltage diagnostics

L9680 has an integrated dedicated circuitry to provide diagnostic feedback and processing of several inputs. These inputs are addressed with an internal analog multiplexer and made available through the SPI digital interface with the Diagnostic Data commands. In order to avoid saturation of high voltage internal signals, an internal voltage divider is used.

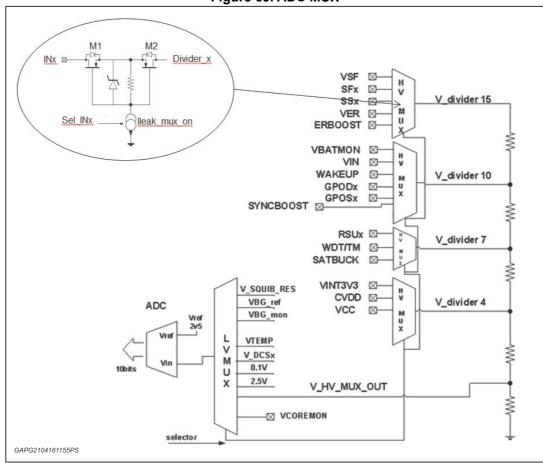


Figure 69. ADC MUX

The diagnostics circuitry is activated by four SPI Diagnostics Control commands (DIAGCTRLx); each of them can address all the available nodes to be monitored, except for what mentioned in *Table 18*.

DIAGCTRLx SPI command bit fields are structured in the following way:

#### **DIAGCTRL\_A (ADDRESS HEX 3A)**

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					х	х	х	х	х	х	х	х	х			ADCF	REQ_/	4[6:0]		
MISO	NEWDATA_A	ADCREQ_A[6:0]									ADC	RES_	A[9:0]							



#### **DIAGCTRL\_B (ADDRESS HEX 3B)**

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI		x					х	х	х	х	Х	х	х			ADCF	REQ_E	[6:0]		
MISO	NEWDATA_B 0 0 ADCREQ_B [6:0]								:0]						ADC	RES_	B [9:0			

#### **DIAGCTRL\_C (ADDRESS HEX 3C)**

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI		x x x x x x						х	х	х	Х			ADCF	REQ_C	[6:0]				
MISO	NEWDATA_C 0 0 ADCREQ_C [								:0]						ADC	RES_	C [9:0]			

#### **DIAGCTRL\_D (ADDRESS HEX 3D)**

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					х	х	х	х	х	х	х	х	Х			ADCF	REQ_D	[6:0]		
MISO	NEWDATA_D	ADCREQ_D [6:0]									ADC	RES_I	D [9:0]							

ADCREQ[A-D] bit fields, used to address the different measurements offered, are listed in *Table 18* for reference.

L9680 diagnostics is structured to take four automatic conversions at a time. In order to get four measurements, four different SPI commands have to be sent (DIAGCTRL\_A, DIAGCTRL B, DIAGCTRL C and DIAGCTRL D), in no particular order.

In case the voltage to be measured is not immediately available, the desired inputs for conversion have to be programmed by SPI in advance, to allow them to attain a stable voltage value. This case applies to the squib resistance measurement and diagnostics (refer to *Loop diagnostics control and results registers*) and to the DC sensor measurement (refer to *Section 11*).

CONVRDY\_0 bit in GSW is equal to (NEWDATA\_A or NEWDATA\_B), while CONVRDY\_1 bit in GSW corresponds to (NEWDATA\_C or NEWDATA\_D).

Each NEWDATAx flag is asserted when conversion is finished and cleared when result is read out. However result is cleared only when new result for that register is available.

When a new request is received it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived. The queue is 4 measures long so it's possible to send all 4 requests at the same time and then wait for the results. If a DIAGCTLRx command is received twice, the second conversion request will overwrite the previous one.

Requests are sent to the L9680 IC via the ADC measurement Registers (ADCREQx) as shown in *Table 18*. All diagnostics results are available on the ADCRESx registers, when addressed by the related ADCREQx register (e.g. data requested by ADCREQA would be written to ADCRESA).



DS11615 Rev 2 219/280

Table 18. Diagnostics control register (DIAGCTRLx)

	AD	C Re	que	est (	ADC	REC		Diagnostics control register (DIAG	ADC Results (ADCRESx)
		В	it[6:	0]			Hex	Voltage Measurement Selection	Bit[9:0]
0	0	0	0	0	0	0	\$00	Unused	
0	0	0	0	0	0	1	\$01	ADC ground reference	V <sub>ADC_GROUND</sub>
0	0	0	0	0	1	0	\$02	ADC Test Pattern 2	V <sub>ADC_FULLSCALE</sub>
0	0	0	0	0	1	1	\$03	DC Sensor ch. selected, Voltage	DCSV_selected
0	0	0	0	1	0	0	\$04	DC Sensor ch. selected, Current	DCSI_selected
0	0	0	0	1	0	1	\$05	DC Sensor ch. selected, Resistance <sup>(1)</sup>	DCSV and DCSI selected
0	0	0	0	1	1	0	\$06	Squib measurement loop selected	Voutx
0	0	0	0	1	1	1	\$07	Internal reference Voltage	VBGR
0	0	0	1	0	0	0	\$08	Internal reference monitor Voltage	VBGM
0	0	0	1	0	0	1	\$09	VCOREMON voltage	VCOREMON
0	0	0	1	0	1	0	\$0A	Temperature Measurement	TEMP
0	0	0	1	0	1	1	\$0B	DC Sensor ch 0, Voltage	DCSV_0
0	0	0	1	1	0	0	\$0C	DC Sensor ch 1, Voltage	DCSV_1
0	0	0	1	1	0	1	\$0D	DC Sensor ch 2, Voltage	DCSV_2
0	0	0	1	1	1	0	\$0E	DC Sensor ch 3, Voltage	DCSV_3
0	0	0	1	1	1	1	\$0F	DC Sensor ch 4, Voltage	DCSV_4
0	0	1	0	0	0	0	\$10	DC Sensor ch 5, Voltage	DCSV_5
0	0	1	0	0	0	1	\$11	DC Sensor ch 6, Voltage	DCSV_6
0	0	1	0	0	1	0	\$12	DC Sensor ch 7, Voltage	DCSV_7
0	0	1	0	0	1	1	\$13	DC Sensor ch 8, Voltage	DCSV_8
0	0	1	0	1	0	0	\$14	V <sub>B</sub> voltage of ER ESR measure <sup>(2)</sup>	V <sub>B</sub>
0	0	1	0	1	0	1	\$15	V <sub>A</sub> voltage of ER ESR measure <sup>(2)</sup>	V <sub>A</sub>
0	0	1	0	1	1	0	\$16	V <sub>C</sub> voltage of ER ESR measure <sup>(2)</sup>	V <sub>C</sub>
0	0	1	0	1	1	1	\$17	Unused	
0	0	1	1	0	0	0	\$18	Unused	
0	0	1	1	0	0	1	\$19	Unused	
0	0	1	1	0	1	0	\$1A	Unused	
0	0	1	1	0	1	1	\$1B	Unused	
0	0	1	1	1	0	0	\$1C	Unused	
0	0	1	1	1	0	1	\$1D	Unused	
0	0	1	1	1	1	0	\$1E	Unused	
0	0	1	1	1	1	1	\$1F	Unused	
0	1	0	0	0	0	0	\$20	VBATMON pin voltage	VBATMON

Table 18. Diagnostics control register (DIAGCTRLx) (continued)

	AD	C Re	que	st (	ADC	REC	Qx)	V-14 M	ADC Results (ADCRESx)
		В	it[6:	0]			Hex	Voltage Measurement Selection	Bit[9:0]
0	1	0	0	0	0	1	\$21	VIN pin voltage	VIN
0	1	0	0	0	1	0	\$22	Internal analog supply voltage (VINT3V3)	VINT3V3
0	1	0	0	0	1	1	\$23	Internal digital supply voltage (CVDD)	CVDD
0	1	0	0	1	0	0	\$24	ERBOOST pin voltage	ERBOOST
0	1	0	0	1	0	1	\$25	SYNCBOOST pin voltage	SYNCBOOST
0	1	0	0	1	1	0	\$26	VER pin voltage	VER
0	1	0	0	1	1	1	\$27	SATBUCK voltage	SATBUCK
0	1	0	1	0	0	0	\$28	VCC voltage	VCC
0	1	0	1	0	0	1	\$29	WAKEUP pin voltage	WAKEUP
0	1	0	1	0	1	0	\$2A	VSF pin voltage	VSF
0	1	0	1	0	1	1	\$2B	WDTDIS pin voltage	WDTDIS
0	1	0	1	1	0	0	\$2C	GPOD0 pin voltage	GPOD0
0	1	0	1	1	0	1	\$2D	GPOS0 pin voltage	GPOS0
0	1	0	1	1	1	0	\$2E	GPOD1 pin voltage	GPOD1
0	1	0	1	1	1	1	\$2F	GPOS1 pin voltage	GPOS1
0	1	1	0	0	0	0	\$30	GPOD2 pin voltage	GPOD2
0	1	1	0	0	0	1	\$31	GPOS2 pin voltage	GPOS2
0	1	1	0	0	1	0	\$32	RSU0 pin Voltage	RSU0
0	1	1	0	0	1	1	\$33	RSU1 pin Voltage	RSU1
0	1	1	0	1	0	0	\$34	RSU2 pin Voltage	RSU2
0	1	1	0	1	0	1	\$35	RSU3 pin Voltage	RSU3
0	1	1	0	1	1	0	\$36	SS0 pin voltage	SS0
0	1	1	0	1	1	1	\$37	SS1 pin voltage	SS1
0	1	1	1	0	0	0	\$38	SS2 pin voltage	SS2
0	1	1	1	0	0	1	\$39	SS3 pin voltage	SS3
0	1	1	1	0	1	0	\$3A	SS4 pin voltage	SS4
0	1	1	1	0	1	1	\$3B	SS5 pin voltage	SS5
0	1	1	1	1	0	0	\$3C	SS6 pin voltage	SS6
0	1	1	1	1	0	1	\$3D	SS7 pin voltage	SS7
0	1	1	1	1	1	0	\$3E	SS8 pin voltage	SS8
0	1	1	1	1	1	1	\$3F	SS9 pin voltage	SS9
1	0	0	0	0	0	0	\$40	SSA pin voltage	SSA
1	0	0	0	0	0	1	\$41	SSB pin voltage	SSB



DS11615 Rev 2 221/280

Table 18. Diagnostics control register (DIAGCTRLx) (continued)

	AD	C Re	que	est (	ADC	REC	Qx)	Voltage Management Calcation	ADC Results (ADCRESx)
		В	it[6:	0]			Hex	Voltage Measurement Selection	Bit[9:0]
1	0	0	0	0	1	0	\$42	Unused	-
1	0	0	0	0	1	1	\$43	Unused	-
1	0	0	0	1	0	0	\$44	Unused	-
1	0	0	0	1	0	1	\$45	Unused	-
1	0	0	0	1	1	0	\$46	SF0 pin voltage	SF0
1	0	0	0	1	1	1	\$47	SF1 pin voltage	SF1
1	0	0	1	0	0	0	\$48	SF2 pin voltage	SF2
1	0	0	1	0	0	1	\$49	SF3 pin voltage	SF3
1	0	0	1	0	1	0	\$4A	SF4 pin voltage	SF4
1	0	0	1	0	1	1	\$4B	SF5 pin voltage	SF5
1	0	0	1	1	0	0	\$4C	SF6 pin voltage	SF6
1	0	0	1	1	0	1	\$4D	SF7 pin voltage	SF7
1	0	0	1	1	1	0	\$4E	SF8 pin voltage	SF8
1	0	0	1	1	1	1	\$4F	SF9 pin voltage	SF9
1	0	1	0	0	0	0	\$50	SFA pin voltage	SFA
1	0 1 0 0 0 1 \$51					1	\$51	SFB pin voltage	SFB

The DC sensor resistance measurement can only be addressed through DIAGCRTL\_A command. Results are available through DIAGCTRL\_A and DIAGCTRL\_B, where ADCRES\_A will contain DCSI and ADCRES\_B will contain DCSV.

Proper scaling is necessary for various measurements. The divider ratios vary by measurement and are summarized by function in the table below.

Table 19. Diagnostics divider ratios

Measurements			Divider Ratio		
Measurements	15:1	10:1	7:1	4:1	1:1
VER	Х				
ERBOOST	Х				
VSF	Х				
SSxy	Х				
SFx	Х				
GPODx		Х			
GPOSx		Х			
SYNCBOOST		Х			
VIN		Х			



<sup>2.</sup> Valid only for ADCREQ\_x field of MISO response when ESR measure results are available.

Measurements			Divider Ratio		
weasurements	15:1	10:1	7:1	4:1	1:1
VBATMON		Х			
WAKEUP		Х			
SATBUCK			Х		
WDT/TM			Х		
RSUx			Х		
VCC				Х	
CVDD				Х	
VINT				Х	
VCOREMON					Х
Bandgap (BGR/BGM)					Х

Table 19. Diagnostics divider ratios (continued)

For measurements other than voltage (current, resistance, temperature etc.) the ranges are specified in the electrical parameters section of the relevant block.

### 14.1 Analog to digital algorithmic converter

The device hosts an integrated 10 bit Analog to Digital converter, running at a clock frequency of 16 MHz. The ADC output is processed by a D to D converter with the following functions:

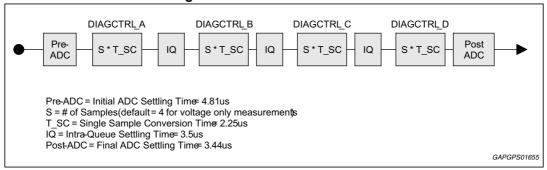
- Use of trimming bits to recover additional gain error due to resistor dividers mismatch;
- Digital low-pass filtering;
- Conversion from 12 to 10 bits.

10 bits data are filtered inside the digital section. The number of samples that are filtered vary depending on the chosen conversion. As per *Section 7.3.2*, the number of used samples in converting DC sensor, squib or temperature measurements defaults to 8. The number of samples for all other measurements defaults to 4. The sample number can be configured by accessing the SYS\_CFG register. After low pass filter, the residual total error is ±4 LSB. This error figure applies to the case of a ideal reference voltage: the spread of reference voltage causes a proportional error in the conversion output. The reference voltage of the ADC is set to 2.5 V.

The conversion time is comprised of several factors: the number of measurements loaded into the queue, the number of samples taken for any one measurement, and the various settling times. An example of conversion time calculation for a full ADC request queue is reported in *Figure 70*. The timings reported in *Figure 70* are nominal ones, min/max values can be obtained by considering the internal oscillator frequency variation reported in the DC characteristics section.



#### Figure 70. ADC conversion time





L9680 Temperature sensor

# 15 Temperature sensor

The L9680 provides an internal analog temperature sensor. The sensor is aimed to have a reference for the average junction temperature on silicon surface. The sensor is placed far away from power dissipating stages and squib deployment drivers. The output of the temperature sensor is available via SPI through ADC conversion, as shown in *Table 18*. The formula to calculate temperature from ADC reading is the following one:

$$T(^{\circ}C) = 180 - \left\{ \left(\frac{220}{1.652}\right) \cdot \left[ \left(\frac{ADC_{REF}}{2} \cdot DIAGCTRLn(ADCRESn)\right) - 0.739 \right] \right\}$$

@ DIAGCTRLn(ADCREQn) = 0Ahex

All parametric requirements for this block can be found in specification tables.



DS11615 Rev 2 225/280

### 16 Electrical characteristics

Every parameter in this chapter is fulfilled down to VIN<sub>GOOD(max)</sub>.

No device damage is granted to occur down to  $VIN_{BAD}(min)$ .

GNDA pin is used as ground reference for the voltage measurements performed within the device, unless otherwise stated.

All table or parameter declared 'Design Info' are not tested during production testing

# 16.1 Configuration and control

All electrical characteristics are valid for the following conditions unless otherwise noted. -40  $^{\circ}$ C  $\leq$  Ta  $\leq$  +95  $^{\circ}$ C.

Table 20. Configuration and control DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>NOV</sub>	Normal Operating Voltage	Design Info Depending on power supply configuration	6	13	18	V
2	$V_{JSV}$	Jump Start Voltage	Design Info 40°C ≤ Ta ≤ 50°C	18	-	26	٧
3	$V_{LDV}$	Load Dump Voltage	Transient Design Info	26.5	-	40	V
4	WU_mon	WAKEUP Monitor threshold	GNDSUBx as ground reference	-	-	1.5	٧
5	WU_off	WAKEUP Off threshold	GNDSUBx as ground reference Vin = 5.5 V and 35 V	2	2.5	3	٧
6	WU_on	WAKEUP On threshold	GNDSUBx as ground reference Vin = 5.5 V and 35 V	4	4.5	5	٧
7	WU <sub>RPD</sub>	WAKEUP Pull-down Resistor	GNDSUBx as ground reference	120	300	480	kΩ
8	VB <sub>GOOD0</sub>		SYS_CTL(VBATMON_TH_SEL)=00 or 11	5.5	5.75	6	V
9	VB <sub>BAD0</sub>		SYS_CTL(VBATMON_TH_SEL)=00 or 11	5	5.25	5.5	٧
10	VB <sub>GOOD1</sub>	VBATMON Thresholds	SYS_CTL(VBATMON_TH_SEL)=01	6.45	6.7	6.95	٧
11	VB <sub>BAD1</sub>		SYS_CTL(VBATMON_TH_SEL)=01	5.95	6.2	6.45	>
12	VB <sub>GOOD2</sub>		SYS_CTL(VBATMON_TH_SEL)=10	7.5	7.75	8	V
13	VB <sub>BAD2</sub>		SYS_CTL(VBATMON_TH_SEL)=10	7	7.25	7.6	>

Table 20. Configuration and control DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
13b	$\Delta V_{BGOOD2}VB_{BAD2}$	VBATMON delta thresholds	V <sub>BGOOD2</sub> VB <sub>BAD2</sub>	300	-	600	mV
14	I <sub>LKG_VBATMON_OFF</sub>	VBATMON input	Device OFF	-5	-	5	μA
15	I <sub>LKG_VBATMON_ON</sub>	leakage	Device ON Design Info	20	24	30	μA
16	R <sub>PD_VBATMON</sub>	VBATMON pull-down resistance	Device ON VBATMON < 10V Design Info	125	250	375	kΩ
17	I <sub>LKG_VBATMON_TOT</sub>	VBATMON total input leakage	I <sub>LKG_VBATMON_ON</sub> + R <sub>PD_VBATMO</sub> VBATMON = 18V	35	-	180	μA
18	VIN <sub>GOOD0</sub>		SYS_CTL(VIN_TH_SEL)=0	5	5.25	5.5	V
19	VIN <sub>BAD0</sub>	VIN Good and VIN Bad	SYS_CTL(VIN_TH_SEL)=0	4.5	4.75	5	V
20	VIN <sub>GOOD1</sub>	Thresholds	SYS_CTL(VIN_TH_SEL)=1	6.05	6.3	6.55	V
21	VIN <sub>BAD1</sub>		SYS_CTL(VIN_TH_SEL)=1	5.55	5.8	6.05	V
22	VIN <sub>FASTSLOPE</sub> _H		-	9.3	9.8	10.3	V
23	VIN <sub>FASTSLOPE_</sub> L	VIN Thresholds used to change Boost regulator transition time	-	9	9.5	10	V
24	VIN <sub>FASTSLOPE</sub> HYS		-	0.2	0.3	0.4	V
25	VIN <sub>SYNC_DIS_L</sub>		SYS_CTL(SYBST_V) =0	12.2	-	13.6	V
26	VIN <sub>SYNC_DIS_H</sub>	VIN SyncBoost Disable Thresholds	SYS_CTL(SYBST_V) = 1	15	-	16.2	V
27	VIN SYNC_DIS_LYS VIN SYNC_DIS_HYS		SYS_CTL(SYBST_V) = 0 / 1 Guaranteed by design	5	-	300	mV
28	I <sub>LKG_VIN_OFF</sub>	VIN input current	Device OFF VIN = 40V	-10	-	10	μA
29	I <sub>LKG_VIN_ON</sub>	TVIIN IIIPUL CUITEIIL	Device ON VIN = 12V	-	-	40	mA
30	C <sub>VIN</sub>	External VIN capacitor	Design Info	1		13 <sup>(1)</sup>	μF



Table 20. Configuration and control DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
31	I <sub>LKG_VER_OFF</sub>		Device OFF VER = 40V	-5	-	50	μA
32	I <sub>LKG_VER_ON_L</sub>	VER Input Leakage	Device ON ERBOOST > VER ER Charge OFF	50	-	200	μА
33	I <sub>LKG_VER_</sub> ON_H		Device ON ERBOOST < VER ER Charge OFF	100	-	500	μА
34	V <sub>WDTDIS_TH</sub>	WDT/TM threshold	Test go no go	10	12	14	V
35	V <sub>WDTDIS_HYST</sub>	WDT/TM hysteresis	Design Info	0.2	0.4	0.5	V
36	I <sub>PD_WDTDIS</sub>	WDT/TM Pull Down Resistance	V <sub>WDTDIS</sub> ≤ 5V	20	45	70	μА
37	V <sub>TH1_H_VCCSEL_</sub>		-	1.30	1.55	1.80	V
38	V <sub>TH1_L_VCCSEL</sub>	VCCSEL Input Voltage Thresholds 1	-	1.05	1.25	1.45	V
39	V <sub>HYS1_VCCSEL</sub>		-	0.2	ı	-	V
40	V <sub>TH2_H_VCCSEL_</sub>		-	5.9	6.4	6.9	V
41	V <sub>TH2_L_VCCSEL</sub>	VCCSEL Input Voltage Thresholds 2	-	5.6	6.1	6.6	V
42	V <sub>HYS2_VCCSEL</sub>		-	0.2	-	-	V
43	I <sub>PD_VCCSEL</sub>	VCCSEL Pull Down Current	VCCSEL= SATBUCK	20	45	70	μА

Table 20. Configuration and control DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
44	I <sub>TOTLKG_BAT</sub>	Battery Line Total Input Leakage	Room Temp WAKEUP = 0 All following pins at 13V: VBATMON, VIN, ERBSTSW, ERBOOST, SYNCBSTSW, SYNCBOOST Guaranteed by design	-	-	35	μА
45	Тл	Junction Temperature	Design Info	-	-	150	°C

<sup>1.</sup> Bigger capacitor can be used in case an external switch is used in parallel to the ER-Switch.

Table 21. Configuration and control AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>FLT_VBATMONTH</sub>	VBATMON thresholds deglitch filter time	-	26	30	34	μs
2	T <sub>FLT_VINGOOD_UP</sub>	VIN Good thresholds deglitch filter time rising edge	-	3	3.5	4	μs
3	T <sub>FLT_VINGOOD_DO</sub>	VIN Good thresholds deglitch filter time falling edge	SYS_CFG(VINGOOD_FILT_SEL) = 0	-	1	-	μs
4	T <sub>FLT_VINGOOD_DO</sub>	VIN Good thresholds deglitch filter time falling edge	SYS_CFG(VINGOOD_FILT_SEL) = 1	3	3.5	4	μs
6	T <sub>FLT_VINBAD_DOWN</sub>	VIN Bad thresholds deglitch filter time falling edge	-	3	3.5	4	μs
7	T <sub>FLT_VINBAD_UP</sub>	VIN Bad thresholds deglitch filter time rising edge	-	26	30	34	μs
8	T <sub>VINGOOD_BLK</sub>	VIN Good Thresholds blanking time	-	26	30	34	μs
9	T <sub>FLT_VINSYNCDIS_D</sub> OWN	VIN SyncBoost Disable deglitch filter time falling edge	-	3.3	-	4.2	μs
10	T <sub>FLT_VINSYNCDIS</sub> _UP	VIN SyncBoost Disable deglitch filter time rising edge	-	9.5	-	11	μs



229/280

Table 21. Configuration and control AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
11	T <sub>FLT_WAKEUP</sub>	Wakeup deglitch filter time	-	0.95	1.05	1.15	ms
12	T <sub>LATCH_WAKEUP</sub>	Wakeup latch time	-	9.7	10.8	11.9	ms
13	T <sub>PWRUP</sub>	Power-up Delay Time  - Wake-up to RESET released	-	-	-	10	ms

Table 22. Open ground detection DC specifications

No	Symbol	Parameter	Conditions / Comments	Min	Тур	Max	Unit
1	GNDA <sub>OPEN</sub>	GNDA open threshold	GNDSUBx=0	100	200	300	mV
2	GNDD <sub>OPEN</sub>	GNDD open threshold	GNDSUBx=0	100	200	300	mV
3	BSTGND <sub>OPEN</sub>	BSTGND open threshold	GNDSUBx=0	100	200	300	mV
4	I <sub>PU_BSTGND</sub>	BSTGND pull-up current	ER BOOST OFF and SYNC BOOST OFF	130	-	270	μA
5	SATGND <sub>OPEN</sub>	SATGND open threshold	GNDSUBx=0	100	200	300	mV
6	I <sub>PU_SATGND</sub>	SATGND pull-up current	SATBUCK OFF	80	120	160	μA
7	VCCGND <sub>OPEN</sub>	VCCGND open threshold	GNDSUBx=0	100	200	300	mV
8	I <sub>PU_VCCGND</sub>	VCCGND pull-up current	VCC BUCK OFF	80	120	160	μΑ

Table 23. GND\_OPEN\_AC - Open ground detection DC specifications

No	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	T <sub>FLT_GNDREFOPEN</sub>	GNDA and GNDD Open Deglitch Filter Time	-	7	11	16	μs
2	T <sub>FLT_GNDREGOPEN</sub>	BSTGND, SATGND, VCCGND Open Deglitch Filter Time	-	1.9	2.3	2.7	μs

# 16.2 Internal analog reference

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C

 $VIN_{BAD0(min)} \le VIN \le 35 V$ 

Table 24. Internal analog reference

N°	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	V <sub>BG1</sub>	Bandgap reference	Vin = 5.5 V and 35 V	-1%	1.2	+1%	V
2	V <sub>BG2</sub>	Bandgap monitor	Vin = 5.5 V and 35 V	-1%	1.2	+1%	V
3	V <sub>ADC_GROUND</sub>	ADC Ground reference	ADC total error included	90	104	120	mV
4	V <sub>ADC_FULLSCALE</sub>	ADC Full scale reference	-	-1.5%	2.5	+1.5%	V



# 16.3 Internal regulators

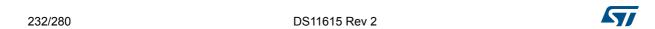
All electrical characteristics are valid for the following conditions unless otherwise noted. -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0}$   $\leq$  VIN  $\leq$  35 V

Table 25. Internal regulator DC specifications

No	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	V <sub>OUT_VINT3V3</sub>	VINT3V3 output voltage	Vin = 5.5 V, 12 V and 35 V	3.14	3.3	3.46	V
2	V <sub>OV_VINT3V3</sub>	VINT3V3 over voltage	-	3.47	-	3.7	V
3	V <sub>UV_VINT3V3</sub>	VINT3V3 under voltage	-	2.97	-	3.13	V
4	V <sub>OUT_CVDD</sub>	CVDD output voltage	Vin = 5.5 V, 12 V and 35 V	3.14	3.3	3.46	٧
5	I <sub>OUT_CVDD</sub>	CVDD current capability	External load is not allowed	-	-	50	mA
6	I <sub>LIM_CVDD</sub>	CVDD current limit	Vin = 5.5 V and 35 V	80	-	-	mA
7	V <sub>OV_CVDD</sub>	CVDD over voltage	-	3.47	-	3.7	٧
8	V <sub>UV_CVDD</sub>	CVDD under voltage	-	2.7	-	2.9	V
9	C <sub>CVDD</sub>	CVDD output capacitance	Design info	60	100	140	nF

Table 26. Internal regulators AC specifications

		•	•				
No	Symbol	Parameter	Comment	Min	Тур	Max	Unit
1	T <sub>FLT_VINT_CVDD_OV</sub>	Internal regulator over voltage deglitch filter time	-	7	11	16	μs
2	T <sub>FLT_VINT_CVDD_UV</sub>	Internal regulator under voltage deglitch filter time	-	7	11	16	μs



# 16.4 Watchdog

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0}$   $\leq$  VIN  $\leq$  35 V

Table 27. Temporal watchdog timer AC specifications (WD1)

No	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	т	Temporal watchdog timeout	_	-	-	2.00	ms
'	WDT1_TIMEOUT	Temporal waterloog timeout		-	-	16.3	ms
2	T <sub>WDT1_RST</sub>	Temporal watchdog reset time	-	0.9	1.0	1.1	ms

### Table 28. Algorithmic watchdog timer DC specifications (WD2)

No	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	V <sub>OH_WD2LCKOUT</sub>	WD2LockOut output voltage	I <sub>LOAD</sub> = -0.5 mA	VCC-0.6	-	VCC	V
2	V <sub>OL_WD2LCKOUT</sub>	VVD2LockOut output voltage	I <sub>LOAD</sub> = 2.0 mA	0	-	0.4	V

#### Table 29. Algorithmic watchdog timer AC specifications (WD2)

				-			
No	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	T <sub>WDT2_TIMEOUT</sub>	Algorithmic watchdog timeout	-	45	50	55	ms
2	T <sub>WDT2_RST</sub>	Algorithmic watchdog reset time	-	0.9	1.0	1.1	ms
3	T <sub>RISE_WD2LCKOUT</sub>	WD2LockOut rise time	50 pF load, 20%-80%	-	-	1.0	μs
4	T <sub>FALL_WD2LCKOUT</sub>	WD2LockOut fall time	50 pF load, 20%-80%	-	-	1.0	μs
5	f <sub>WD2_SEED</sub>	WD2 Seed Counter Rate	-	-	f <sub>osc</sub> 512	-	MHz

### 16.5 Oscillators

All electrical characteristics are valid for the following conditions unless otherwise noted: --40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{\rm GOOD0}$ (max)  $\leq$  VIN  $\leq$  35 V.

Table 30. Oscillators specifications

N #	Symbol	Parameter	Condition	Min	Тур	Max	Unit
1	fosc	Main oscillator average frequency	-	15.2	16	16.8	MHz
2	f <sub>MOD_</sub> osc	Main oscillator modulation frequency	SPI_CLK_CNF(MAIN_SS_DIS=0) Design Info	-	f <sub>osc</sub> 128	-	MHz
3	I <sub>MOD_OSC</sub>	Main oscillator modulation index	SPI_CLK_CNF(MAIN_SS_DIS=0)	2	4	6	%
4	f <sub>AUX</sub>	Aux oscillator average frequency	-	7.125	7.5	7.875	MHz
5	f <sub>MOD_AUX</sub>	Aux oscillator modulation frequency	SPI_CLK_CNF(AUX_SS_DIS=0) Design Info	-	f <sub>osc_AUX</sub> 128	-	MHz
6	I <sub>MOD_AUX</sub>	Aux oscillator modulation index	SPI_CLK_CNF(AUX_SS_DIS=0)	2	4	6	%
7	f <sub>OSC_LOW_</sub>	Main oscillator low frequency detection threshold	-	128 - f <sub>AUX_MIN</sub>	-	128 · f <sub>AUX_MAX</sub>	MHz
8	f <sub>OSC_HIGH_</sub> TH	Main oscillator high frequency detection threshold	-	<u>79</u> ⋅ f <sub>AUX_MIN</sub>	-	79/32 · f <sub>AUX_MAX</sub>	MHz

#### 16.6 Reset

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0} \leq$  VIN  $\leq$  35 V, VCCx(min)  $\leq$  VCCx  $\leq$  VCCx(max), VCC = 3.3 V or 5 V

Table 31. Reset DC specifications

No	Symbol	Parameter	Comment	Min	Тур	Max	Unit
1	V <sub>OH_RESET</sub>	RESET output voltage	I <sub>LOAD</sub> = -1.0 mA	VCC-0.4	-	VCC	V
2	V <sub>OL_RESET</sub>	TRESET output voltage	I <sub>LOAD</sub> = 2.0 mA	0	-	0.4	>
3	R <sub>PD_RESET</sub>	RESET pull down resistance	-	65	100	135	kΩ
4	VCORE <sub>UV</sub>	VCOREMON under voltage threshold	-	1.08	1.11	1.14	V
5	VCORE <sub>OV</sub>	VCOREMON over voltage threshold	-	1.26	1.29	1.32	V
6	R <sub>PD_VCORE</sub>	VCOREMON pull down resistance	-	65	100	135	kΩ
7	V <sub>IH_MCUFLT</sub>	MCUFAULTB high level input voltage	-	2	-	-	٧
8	V <sub>IL_MCUFLT</sub>	MCUFAULTB Low level Input Voltage	-	-	-	0.8	V
9	I <sub>PD_MCUFLT</sub>	MCUFAULTB Pull Down Current	MCUFAULTB= VCC	20	45	70	μA

### Table 32. Reset AC specifications

No	Symbol	Parameter	Comment	Min	Тур	Max	Unit
1	T <sub>RISE_RESET</sub>	Rise time	50 pF load, 20%-80%	-	-	1.00	μs
2	T <sub>FALL_RESET</sub>	Fall time	- 30 pr loau, 20 /0-00 /0	-	-	1.00	μs
3	T <sub>HOLD_RESET</sub>	Reset hold time	-	0.45	0.5	0.55	ms
4	T <sub>FLT_VCOREOV</sub>	VCOREMON over voltage deglitch filter time	-	27	30	33	μs
5	T <sub>FLT_VCOREUV</sub>	VCOREMON under voltage deglitch filter time	-	27	30	33	μs
6	T <sub>FLT_MCUFAULTB</sub>	MCUFAULTB Deglitch filter time	-	9	10	11	μs

### 16.7 SPI interface

All electrical characteristics are valid for both Global and Remote Sensor SPI and for the following conditions unless otherwise noted:

-40 °C  $\leq$  Ta  $\leq$  +95 °C,  $VIN_{GOOD0} \leq$  VIN  $\leq$  35 V,  $VCCx(min) \leq$  VCCx  $\leq$  VCCx(max), VCC = 3.3 V or 5 V

Table 33. Global and remote sensor SPI DC specifications

No	Symbol	Parameter	Comment	Min	Тур	Max	Unit
1	V <sub>IH_CS_G</sub> V <sub>IH_CS_RS</sub>	CS_x High level Input Voltage	-	2	ı	-	V
2	$V_{IL\_CS\_G}$ $V_{IL\_CS\_RS}$	CS_x Low level Input Voltage	-	-	ı	0.8	V
3	I <sub>PU_CS_G</sub> I <sub>PU_CS_RS</sub>	CS_x Pull Up Current	CS_x = 0V	-70	-45	-20	μA
4	V <sub>IH_MOSI_G</sub> V <sub>IH_MOSI_RS</sub>	MOSI_x High level Input Voltage	-	2	1	-	V
5	V <sub>IL_MOSI_G</sub> V <sub>IL_MOSI_RS</sub>	MOSI_x Low level Input Voltage	-	-	ı	0.8	V
6	I <sub>PD_MOSI_G</sub> I <sub>PD_MOSI_RS</sub>	MOSI_x Pull Down Current	MOSI_x = VCC	20	45	70	μA
8	V <sub>IH_SCLK_G</sub> V <sub>IH_SCLK_RS</sub>	SCLK_x High level Input Voltage	-	2	ı	-	V
9	V <sub>IL_SCLK_G</sub> V <sub>IL_SCLK_RS</sub>	SCLK_x Low level Input Voltage	-	ı	ı	0.8	V
10	I <sub>PD_SCLK_G</sub> I <sub>PD_SCLK_RS</sub>	SCLK_x Pull Down Current	SCLK_x = VCC	20	45	70	μA
12	V <sub>OH_MISO_G</sub> V <sub>OH_MISO_RS</sub>	MISO_x High level Output Voltage	I <sub>LOAD</sub> = -800 μA	VCC -0.5	-	vcc	V
13	V <sub>OL_MISO_G</sub> V <sub>OL_MISO_RS</sub>	MISO_x Low level Output Voltage	I <sub>LOAD</sub> = 2.0 mA	-	-	0.4	V
14	I <sub>LKG_MISO_G</sub> I <sub>LKG_MISO_RS</sub>	MISO_x Output Leakage	Tri-state leakage	-10	-	10	μA
15	V <sub>IH_MISO_RS</sub>	MISO_RS High level Input Voltage	-	2	-	-	V
16	V <sub>IL_MISO_RS</sub>	MISO_RS Low level Input Voltage	-	-	-	0.8	٧

Table 34. SPI AC specifications

No	Symbol	Parameter	Comments / Conditions	Min	Тур	Max	Unit
1	F <sub>SCLK</sub>	SPI transfer frequency	-	-	8	8.08	MHz
2	T <sub>SCLK</sub>	SCLK_x period	-	123.8	-	-	ns
3	T <sub>LEAD</sub>	Enable lead time	-	250	-	-	ns
4	T <sub>LAG</sub>	Enable lag time	-	50	-	-	ns
5	T <sub>HIGH_SCLK</sub>	SCLK_x high time	-	40	-	-	ns
6	T <sub>LOW_SCLK</sub>	SCLK_x low time	-	40	-	-	ns
7	T <sub>SETUP_MOSI</sub>	MOSI_x input setup time	-	20	-	-	ns
8	T <sub>HOLD_MOSI</sub>	MOSI_x input hold time	-	20	-	-	ns
9	T <sub>ACC_MISO</sub>	MISO_x access time		5	-	60	ns
10	T <sub>DIS_MISO</sub>	MISO_x disable time	80 pF load	20	-	100	ns
11	T <sub>VALID_MISO</sub>	MISO_x output valid time		5	-	30	ns
12	T <sub>HOLD_MISO</sub>	MISO_x Output Hold Time	80 pF load; Design Info	0	-	-	ns
13	T <sub>NODATA</sub>	SCLK_x hold time	-	20	-	-	ns
14	T <sub>FLT_CS</sub>	CS_x noise glitch rejection time	-	50	-	300	ns
15	T <sub>NODATA</sub>	SPI interframe time	-	400	-	-	ns
16	T <sub>SETUP_MISO_RS</sub>	MISO_RS Input Setup Time	-	20	-	-	ns
17	T <sub>HOLD_MISO_RS</sub>	MISO_RS Input Hold Time	-	20	-	-	ns

Note: All timing is shown with respect to 10% and 90% of the actual delivered VCC voltage.

SCLK\_x

MOSI\_x

MISO\_x

MSB OUT

DATA

LSB IN

DON'T

CARE

GAPGPS02305

Figure 71. SPI timing diagram

# 16.8 ERBoost regulator

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V.

Table 35. ERBoost regulator DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V	Boost output voltage	Across all line and I <sub>O_BST</sub> load (steady state) SYS_CTL(ER_BST_V)=0	22.6	23.8	25	V
2	Vo_erbst	Boost output voltage	Across all line and I <sub>O_BST</sub> load (steady state) 1SYS_CTL(ER_BST_V)=1	31.65	33	35	V
3	I <sub>O_ERBST</sub>	Boost output current	-	0.1	i	70	mA
4	dV <sub>SR_ac</sub>	Line transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	-	8%	%
5	$\mathrm{dV}_{\mathrm{LR}\_\mathrm{ac}}$	Load transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	ı	8%	%
6	R <sub>DSON_ERBST</sub>	Power switch resistance	-	-	-	1	Ω
7	I <sub>OC_ERBST</sub>		-	650	1	1350	mA
8	I <sub>OC_ERBST_ERON</sub>	Over current detection	ER Switch activated AND SW_REGS_CONF(LOW_E RBST_ILIM_ERON) = 1	125	-	600	mA
9	I <sub>LKG_ERBST_OFF</sub>		ERBOOST=40V Power-off or Sleep Mode	-5	1	+5	μА
10	I <sub>LKG_ERBST_</sub> ON	ERBOOST input current	Active or Passive Mode ERBoost reg. enabled ERBSTSW > ERBoost > VER ER Charge OFF VSF regulator OFF Any GPO channel not enabled Guarantee by design	60	-	200	μА
11	I <sub>LKG_ERBST_ON_wGPO</sub>		Active or Passive Mode ERBoost reg. enabled ERBSTSW > ERBoost > VER ER Charge OFF VSF regulator OFF All GPO channel activated	1.5	1	2.4	mA

Table 35. ERBoost regulator DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
12	V	ERBOOST voltage	BST33V = 0	18	20	22	V
13	V <sub>ERBST_OK</sub>	threshold	BST33V = 1	26	28	30	V
14	V	ERBOOST Over Voltage	SYS_CTL(ER_BST_V) = 0	22.6	-	25	V
15	V <sub>ERBST_OV</sub>	threshold	SYS_CTL(ER_BST_V) = 1	31.65	-	35	V
16	V <sub>ERBST_DIS_TH</sub>	Voltage difference between VIN and ERBOOST to deactivate the ER Boost regulator	VIN – ERBOOST Vin = 5.5 V, 12 V and 35 V	1.6	2.2	2.5	V
17	V <sub>ERBST_CLAMP_EN_TH</sub>	Voltage difference between ERBSTSW and ERBOOST to activate the ER Boost CLAMP	V <sub>ERBSTSW</sub> – V <sub>ERBOOST</sub>	2.7	3.3	3.7	V
18	T <sub>JSD_ERBST</sub>	Thermal shutdown	-	150	175	190	°C
19	T <sub>HYS_TSDERBST</sub>	Thermal shadown	-	5	10	15	°C

Table 36. ERBoost regulator AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	F <sub>SW_ERBST</sub>	ERBOOST switching frequency	-	1.8	1.882	2.0	MHz
2	T <sub>RISE_ERBSTSW_SLOW</sub> T <sub>FALL_ERBSTSW_SLOW</sub>	ERBSTSW transition time	10% to 90% voltage on ERBSTSW VIN ≥ VIN <sub>FASTSLOPE</sub> H = 10.3 V I <sub>load</sub> = 6 0mA SYS_CTL(ER_BST_V) = 1 Guaranteed by Design	15	-	35	ns
3	T <sub>RISE_ERBSTSW_FAST</sub> T <sub>FALL_ERBSTSW_FAST</sub>		10% to 90% voltage on ERBSTSW VIN = VIN <sub>FASTSLOPE_L</sub> =9 V	5	-	15	ns
4	T <sub>ON_ERBST</sub>	ERBOOST charge-up time	$C_{ERBOOST}$ = 2.2 µF Vin =12V, $I_{O\_ERBST}$ = 5mA SYS_CTL(ER_BST_V) = 1 Measured from CS_G edge to $V_{O\_ERBST}$ (min)	50	-	500	μs
5	T <sub>FLT_VIN_ERBST_COMP</sub>	Deglitch filter on VIN_ERBoost comparator	-	27	30	33	μs

Table 36. ERBoost regulator AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
6	T <sub>FLT_TSD_ERBST</sub>	Thermal shutdown filter time	-	-	-	10	μs
7	T <sub>SOFTST_ERBST</sub>	ERBOOST Soft-start Time	Design Info. Time from activation of ERBOOST when overcurrent is 40% of loc_erbst (loc_erbst_eron) to instant when overcurrent is 100% of loc_erbst (loc_erbst_eron)	-	-	1075	μs

### Table 37. ERBOOST Converter external components design info

No	Symbol	Component	Conditions	Min	Тур	Max	Unit
1	L <sub>ERBST</sub>	Inductance	-	8	10	12	μH
2	ESL <sub>ERBST</sub>	Inductance resistance	-	-	-	0.1	Ω
3	C <sub>BLK_ERBST</sub>	Output bulk capacitance to ensure regulator stability	Min cap value including derating factors	1	2.2	-	μF
4	ESR <sub>CBLK_ERBST</sub>	Bulk capacitor ESR	-		-	50	mΩ
5	V <sub>FSTR_ERBST</sub>	Steering diode forward voltage	I <sub>F</sub> =100 mA	-	-	0.85	V
6	I <sub>LKGSTR_ERBST</sub>	Steering diode reverse leakage	Ta = 95 °C	-	-	3	mA

# 16.9 ER CAP current generators and diagnostic

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V, 8 V  $\leq$  ERBOOST.

Table 38. ER CAP current generators and diagnostic DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	I <sub>ER_CHARGE</sub>	ER charge current	ERBOOST ≥ 8 V ERBOOST - VER ≥ 2 V ERBOOST = 24 V and 35 V	60	65	70	mA
2	I <sub>ER_DISCHARGE_LOW</sub>	ER discharge low level current	VER ≥ 6V	60	65	70	mA
3	I <sub>ER_DISCHARGE_HIGH</sub>	ER discharge high level current	VER ≥ 8V	589	640	691	mA
4	R <sub>DSON_ERCHARGE</sub>	ER charge power resistance	(V <sub>ERBOOST</sub> -V <sub>VER</sub> )/I <sub>VER</sub> I <sub>VER</sub> = 10mA	-	-	20	Ω
5	VER <sub>RANGE</sub>	VER voltage measurement range	-	20	-	35	V
6	VER <sub>ACC</sub>	VER voltage measurement accuracy	VER <sub>RANGE</sub>	-8	-	+8	%
7	ERCAP <sub>RANGE</sub>	Energy reserve capacitor measurement range	Design Info	-	-	10	mF
8	ERCAP <sub>ACC</sub>	Energy reserve capacitor measurement accuracy	ΔVERMIN = 2 V	-7	-	+7	%
9	ERCAP_ESR <sub>RANGE</sub>	Energy reserve capacitor ESR measurement range	-	200	-	600	mΩ
10	ERCAP_ESR <sub>ACC</sub>	Energy reserve capacitor ESR measurement accuracy	All errors included except the offset one (OFF <sub>ER_ESR</sub> )	-20		+20	%
11	G <sub>ER_ESR</sub>	Energy Reserve Capacitor ESR Measurement Gain	-	-13%	3	+13%	V/V
12	OFF <sub>ER_ESR</sub>	Energy Reserve Capacitor ESR Measurement Offset	Design Info	70	-	160	mΩ
13	T <sub>JSD_ERBST</sub>	ER charge thermal	-	150	175	190	°C
14	T <sub>HYS_TSDERBST</sub>	shutdown	-	5	10	15	°C
15	V <sub>VER_VBATMON_TH</sub>	Voltage difference between VER and VBATMON to activate the ER Discharge in passive mode	VER - VBATMON	1.6	2.2	2.5	V

Table 39. ER CAP current generators and diagnostic AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>ON_ERCAP</sub>	Energy reserve capacitor charge-up time	C <sub>VER</sub> ≤ 10mF nominal, BST33V = 0, Design Info	-	-	4	s
2	T <sub>ESR_DIAG</sub>	ER CAP ESR diagnostic duration	Total duration time from SPI command to ADC results availability	-5%	225	+5%	μs
3	T <sub>FLT_TSD_ERCHARGE</sub>	Thermal shutdown filter time	-	-	-	10	μs

### 16.10 ER switch

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V.

Table 40. ER Switch DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	R <sub>DSON_ERSW</sub>	Power switch resistance	Vin = 5.5 V and 35 V	0.5	-	3	Ω
2	I <sub>LIM_ERSW</sub>	ER switch current limit	VER = 17 V @ VIN = 12 V and VER = 35 V @ VIN = 31 V	608	810	980	mA
3	V <sub>ER_SW_OV_TH</sub>	ER switch Over Voltage threshold	ER switch turned off when VIN > V <sub>ER</sub> + V <sub>ER_SW_OV_TH</sub> Vin = 12 V and 35 V	10	-	200	mV
4	T <sub>JSD_ERSW</sub>	Thermal shutdown	-	150	175	190	°C
5	T <sub>HYS_TSDERSW</sub>	THEITHAI SHULUOWH	-	5	10	15	°C

Table 41. ER Switch AC specifications

No	Symbol	Parameter	Conditions	Min		Max	Unit
1	T <sub>ON_ERSW</sub>	ER turn-on time (time to reach either R <sub>DSON_ERSW</sub> or I <sub>LIM_ERSW</sub> )	C <sub>VIN</sub> = 10 μF	-	-	5	μs
2	T <sub>FLT_TSD_ERSW</sub>	Thermal shutdown filter time	-	-	-	10	μs
3	T <sub>BLK_ERSW</sub>	ER switch activation blanking time after thermal shutdown	-	-	1	-	ms

### **16.11 COVRACT**

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V; VIN $_{GOOD}(max) \leq$  VIN  $\leq$  35 V; VCCx(min)  $\leq$  VCCx  $\leq$  VCCx(max); VCC = 3.3 V or 5 V

Table 42. COVRACT DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>OH_COVRACT</sub>	COVRACT output voltage	I <sub>LOAD</sub> = -0.5 mA	VCC -0.6	-	vcc	V
2	V <sub>OL_COVRACT</sub>	· •	I <sub>LOAD</sub> = 2.0 mA	0	-	0.4	V
3	I <sub>REV_COVRACT</sub>	Reverse current short high voltage	COVRACT = 40 V VCC = 3.3 V	-	-	1	mA

#### **Table 43. COVRACT AC specifications**

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>RISE_COVRACT</sub>	Rise time	50 pF load, 20%-80%	-	-	1.00	μs
2	T <sub>FALL_COVRACT</sub>	Fall time	50 pF load, 20%-80%	ı	ı	1.00	μs

### 16.12 SYNCBOOST converter

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  VIN $_{SYNC\ DIS\ X}$ (min)

Table 44. SYNCBOOST converter DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V	SYNCBOOST output	Across all line and load, steady state SYS_CTL(SYBST) = 0	11.40	12	-	V
2	V <sub>O_SYNCBST</sub>	voltage	Across all line and load (steady state) SYS_CTL(SYBST) = 1	14.00	14.75	-	V
3	Io_syncbst_vl_ih		SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_M ODE) = 0	20	-	360	mA
4	I <sub>O_SYNCBST_VL_IL</sub>	SYNCBOOST output current	SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_M ODE) = 1	20	ı	240	mA
5	Io_syncbst_vh_ih		SYS_CTL(SYBST_V) = 1 SYS_CFG(LOW_POWER_M ODE) = 0	20	-	290	mA

Table 44. SYNCBOOST converter DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
6	Io_syncbst_vh_il	SYNCBOOST output current	SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_M ODE) = 1	20	-	190	mA
7	dV <sub>SR_ac</sub>		All line, load; dt = 100 μs;	-8%	-	8%	%
8	$dV_{LR\_ac}$	Line transient response	SYS_CTL(SYBST) = 0/1 Design Info	-8%	-	8%	%
9	R <sub>DSON_SYNCBST</sub>	Power switch resistance	-	-	-	0.5	Ω
10	I <sub>OC_SYNCBST_HIGH</sub>	Over current detection	SYS_CFG(LOW_POWER_ MODE) = 0	1.6	-	3.2	А
11	I <sub>OC_SYNCBST_LOW</sub>	of integrated MOS	SYS_CFG(LOW_POWER_ MODE) = 1	1.5	-	2.6	А
12	I <sub>LKG_SYNCBOOST</sub>	SYNCBOOST leakage	SYNCBOOST=40V Device off	-	-	10	μA
13	I <sub>LKG_SYNCBSTSW</sub>	SYNCBSTSW leakage	SYNCBSTSW=40V Device off	-	-	20	μA
14	V <sub>SYNCBST_OK</sub>	SYNCBOOST voltage threshold	-	9	10	11	V
15	V <sub>SYNCBST_OV</sub>	SYNCBOOST Over Voltage threshold	-	22	23	24	V
16	V <sub>SYNCBST_DIS_TH</sub>	Voltage difference between VIN and SYNCBOOST to deactivate the SYNC Boost regulator	V <sub>VIN</sub> -VS <sub>YNCBOOST</sub> Vin = 5.5 V, 12 V and 35 V	1.6	2.2	2.5	V
17	V <sub>SYNCBST_CLAMP_EN_TH</sub>	Voltage difference between SYNCBSTSW and SYNCBOOST to activate the SYNC Boost CLAMP	V <sub>SYNCBSTSW</sub> -V <sub>SYNCBOOST</sub>	2.7	3.3	3.7	V
18	V <sub>VIN_SYNCBST_RESTART_TH</sub>	Voltage threshold to restart Syncboost	SYS_CTL(RESTART_SYBST _SEL) = 0 Voltage threshold on VIN pin	9	-	10.3	V
19	V <sub>SYNCBST_RESTART_TH</sub>	regulator during ER State	SYS_CTL(RESTART_SYBST _SEL) = 1 Voltage threshold on SYNCBOOST pin	19	20	21	V
20	T <sub>JSDERSYNCBST</sub>	Thermal shutdown	-	150	175	190	С
21	T <sub>HYS_TSDSYNCBST</sub>	Thermal shutdown hysteresis	-	5	10	15	°C

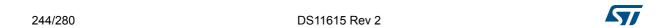


Table 45. SYNCBOOST converter AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	F <sub>SW_SYNCBST</sub>	SYNCBST switching frequency	-	1.8	1.882	2.0	MHz
2	T <sub>RISE_SYNCBSTSW_SLOW</sub> T <sub>FALL_SYNCBSTSW_SLOW</sub>	SYNCBSTSW	10% to 90% voltage on SYNCBSTSW VIN = VIN <sub>FASTSLOPE</sub> _H Design Info	15	-	30	ns
3	T <sub>RISE_SYNCBSTSW_FAST</sub> T <sub>FALL_SYNCBSTSW_FAST</sub>	transition time	10% to 90% voltage on SYNCBSTSW VIN = VIN <sub>FASTSLOPE_L</sub> Design Info	5	-	20	ns
4	T <sub>SOFTST_SYNCBST</sub>	SYNCBST Soft- start Time	Design Info. Time from activation of SYNCBOOST when overcurrent is 40 % of loc_syncbst_high (loc_syncbst_low) to instant when overcurrent is 100% of loc_syncbst_high (loc_syncbst_low)	,	,	1075	μs
5	T <sub>FLT_TSD_SYNCBST</sub>	Thermal shutdown filter time	-	-	-	10	μs
6	T <sub>BLK_SYNCSW</sub>	Sync boost activation blanking time after thermal shutdown	-	-	1	-	ms

### Table 46. SYNCBOOST converter external components design info

No	Symbol	Component	Conditions	Min	Тур	Max	Unit
1	L <sub>SYNCBST</sub>	Inductance	Min 4.7 µH nominal	3.76	-	-	μH
2	ESL <sub>SYNCBST</sub>	Inductance resistance	-	ı	ı	0.1	Ω
3	C <sub>BLK_SYNCBST</sub>	Output bulk capacitance	Min 2.2 μF nominal	1.76	-	-	μF
4	ESR <sub>CBLK_SYNCBST</sub>	Bulk capacitor ESR	-	1	-	50	mΩ
5	V <sub>FSTR</sub>	Steering diode forward voltage	I <sub>F</sub> = 1 A	ı	-	0.5	V
6	I <sub>LKGSTR</sub>	Steering diode reverse leakage	Ta = 95 °C	ı	ı	3	mA

### 16.13 SATBUCK converter

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35V, V $_{SYNCBST\_OK} \leq$  SYNCBOOST

Table 47. SATBUCK converter DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V	SATBUCK output	Across all line and load, steady state SAT_V = 0	6.92	7.2	7.48	V
2	V <sub>O_</sub> SATBCK	voltage	Across all line and load, steady state SAT_V = 1	8.64	9	9.36	V
3	I <sub>O_SATBCK_VH_IH</sub>		SAT_V =0 LOW_POWER_MODE = 0	20	-	450	mA
4	I <sub>O_SATBCK_VH_IL</sub>	SATBUCK output	SAT_V =0 LOW_POWER_MODE = 1	20	-	300	mA
5	I <sub>O_SATBCK_VL_IH</sub>	current	SAT_V =1 LOW_POWER_MODE = 0	20	ı	390	mA
6	I <sub>O_SATBCK_VL_IL</sub>		SAT_V =1 LOW_POWER_MODE = 1	20	-	240	mA
7	dV <sub>SR_ac</sub>	Line transient response	All line, load; dt=100 μs; SAT_V = 0/1 Design Info	-4%	-	4%	%
8	$dV_{LR\_ac}$	Load transient response	All line, load; dt=100 μs; SAT_V = 0/1 Design Info	-4%	-	4%	%
9	R <sub>DSON_SATBCK_HS</sub>	High side power switch resistance	SyncBoost = 12 V and 35V	-	-	0.6	Ω
10	R <sub>DSON_SATBCK_LS</sub>	Low side power switch resistance	SyncBoost = 12 V and 35V	-		0.6	Ω
11	I <sub>OC_HS_SATBCK_HI</sub>	High side over	LOW_POWER_MODE = 0	0.83	1.1	1.37	Α
12	I <sub>OC_HS_SATBCK_LO</sub>	current detection	LOW_POWER_MODE = 1	0.53	0.7	0.9	Α
13	I <sub>OCP_LS_SATBCK_LO</sub>	Low side positive over current	V <sub>SATBCKSW</sub> ≥ 0 V <sub>SYNCBST</sub> < V <sub>SYNCBST_RESTART_TH</sub>	1	-	100	mA
14	I <sub>OCP_LS_SATBCK_HI</sub>	detection	V <sub>SATBCKSW</sub> ≥ 0 FAST SLOPE	100	240	350	mA
15	I <sub>OCN_LS_SATBCK_HI</sub>	Low side negative over current	V <sub>SATBCKSW</sub> = 0 LOW_POWER_MODE = 0	0.94	1.25	1.56	Α
16	IOCN_LS_SATBCK_LO	detection	V <sub>SATBCKSW</sub> = 0 LOW_POWER_MODE = 1	0.64	0.85	1.06	Α
17	V <sub>SATBCK_OK_LOW</sub>	SATBUCK voltage	SYS_CTL(SAT_V) = 0	6.2	6.5	6.8	V
18	V <sub>SATBCK_OK_HIGH</sub>	threshold	SYS_CTL(SAT_V) = 1	7.7	8.1	8.5	V

Table 48. SATBUCK converter AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Units
1	F <sub>SW_SATBCK</sub>	SATBUCK switching frequency	-	1.8	1.882	2.0	MHz
	T <sub>RISE_SATBCKSW</sub>		10% to 90% voltage on SATBCKSW				
2	_SLOW T <sub>FALL_SATBCKSW</sub> _SLOW	SATBCKSW transition time	V <sub>SYNCBST</sub> < V <sub>SYNCBST_RESTART_TH</sub> Design Info	10	-	25	ns
3	T <sub>RISE_SATBCKSW</sub>	SATBORSW transition time	10% to 90% voltage on SATBCKSW V <sub>SYNCBST</sub> >	5	_	15	
3	T <sub>FALL_SATBCKSW</sub> _FAST		VSYNCBST P VSYNCBST_RESTART_TH Design Info	,	_	15	
4	T <sub>SOFTST_SATBCK</sub>	SATBUCK soft start time	From 10% to 90%	0.50	-	2	ms

#### Table 49. SATBUCK converter external components design info

No	Symbol	Component	Conditions	Min	Тур	Max	Unit
1	L <sub>SATBCK</sub>	Inductance	Min 4.7 μH nominal	3.76	-	-	μH
2	ESR <sub>LSATBCK</sub>	Inductance Resistance	-	-	-	0.25	Ω
3	C <sub>BLK_SATBCK</sub>	Output Bulk Capacitance	Min 4.7 µH nominal	3	-	30	μF
4	ESR <sub>CBLK_SATBCK</sub>	Bulk Capacitor ESR	-	-	-	50	mΩ

## 16.14 VCC regulator

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0} \leq$  VIN  $\leq$  35 V, V  $_{SATBCK\_OK} \leq$  SATBUCK

 $V_{UV\_VCOREMON} \leq VCOREMON \leq V_{OV\_VCOREMON}$ 

Table 50. VCC converter DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Units
1	V	VCCBUCK Output	Across all line and load, steady state VCCSEL < V <sub>TH1_L_VCCSEL</sub>	3.20	3.3	3.40	V
2	Vo_vcc	Voltage	Across all line and load, steady state VCCSEL = > V <sub>TH1_H_VCCSEL</sub>	4.85	5	5.15	V

Table 50. VCC converter DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Units
3	I <sub>O_VCC3V_</sub> HI		VCCSEL < V <sub>TH1_L_VCCSEL</sub> LOW_POWER_MODE = 0	20	-	420	mA
4	I <sub>O_VCC3V_LO</sub>	VCCBUCK output current	VCCSEL < V <sub>TH1_L_VCCSEL</sub> LOW_POWER_MODE = 1	20	-	230	mA
5	I <sub>O_VCC5V_HI</sub>		VCCSEL > V <sub>TH1_H_VCCSEL</sub> LOW_POWER_MODE = 0	20	-	270	mA
6	dV <sub>SR_ac</sub>	Line transient response	All line, load; dt=100 μs; Design Info	-4%	-	4%	%
7	dV <sub>LR_ac</sub>	Load transient response	All line, load; dt=100 μs; Design Info	-4%	-	4%	%
8	R <sub>DSON_VCCBCK_HS</sub>	High side power switch resistance	SATBUCK = 6.92 V and 9.36 V	-	-	0.6	Ω
9	R <sub>DSON_VCCBCK_LS</sub>	Low side power switch resistance	SATBUCK = 6.92 V and 9.36 V	-	-	0.6	Ω
10	I <sub>OC_HS_VCCBCK_HI</sub>	High side over current	SYS_CFG(LOW_POWER_ MODE) = 0	0.59	0.75	0.9	А
11	I <sub>OC_HS_VCCBCK_LO</sub>	detection	SYS_CFG(LOW_POWER_ MODE) = 1	0.4	0.56	0.7	А
12	I <sub>OCP_LS_VCCBCK</sub>	Low side positive over current detection	V <sub>VCCBCKSW</sub> > 0 SYS_CFG(LOW_POWER_ MODE) = 0 / 1	1	-	100	mA
13	IOCN_LS_VCCBCK_HI	Low side negative over	V <sub>VCCBCKSW</sub> = 0 LOW_POWER_MODE = 0	0.67	0.9	1.13	А
14	IO_VCC5V_HI  dV_SR_ac  dV_LR_ac  RDSON_VCCBCK_HS  RDSON_VCCBCK_LS  IOC_HS_VCCBCK_LO  IOCP_LS_VCCBCK_LO  IOCN_LS_VCCBCK_HI  IOCN_LS_VCCBCK_LO  VCC_OV3V  VCC_UV3V  VCC_UV5V  VCC_UV5V	current detection	V <sub>VCCBCKSW</sub> = 0 LOW_POWER_MODE = 1	0.49	0.65	0.82	А
15	I <sub>OF_VCC</sub>	Open feedback current on VCC	-	100	150	200	μА
16	VCC <sub>OV3V</sub>	VCC over voltage	VCCSEL < V <sub>TH2_L_VCCSEL</sub>	3.43	-	3.6	V
17	VCC <sub>OV5V</sub>	detection	VCCSEL > V <sub>TH2_H_VCCSEL</sub>	5.25	-	5.50	V
18	VCC <sub>UV3V</sub>	VCC under voltage	VCCSEL < V <sub>TH2_L_VCCSEL</sub>	3.0	-	3.17	V
19	VCC <sub>UV5V</sub>	detection high	VCCSEL > V <sub>TH2_H_VCCSEL</sub>	4.5	-	4.75	V
20	VCC <sub>UVL</sub>	VCC under voltage detection low	-	1.8	2	2.2	V

Table 51. VCC converter AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Units
1	F <sub>SW_VCCBCK</sub>	VCCBUCK switching frequency	-	1.8	1.882	2.0	MHz
2	T <sub>RISE_</sub> VCCBCKSW T <sub>FALL_</sub> VCCBCKSW	VCCBCKSW transition time	10% to 90% voltage on VCCBCKSW Design Info	8	-	20	ns
3	T <sub>SOFTST_VCCBCK</sub>	VCCBUCK soft start time	From 10% to 90%	0.5	-	2	ms
4	T <sub>FLT_VCCOV</sub>	VCC over voltage detection deglitch filter time	-	27	30	33	μs
5	T <sub>FLT_VCCOV_RAMPUP</sub>	VCC Over voltage detection deglitch filter time during VCC_RAMPUP state	VCC reg in VCC_RAMPUP state	1.5	2	2.5	μs
6	T <sub>FLT_VCCUV</sub>	VCC under voltage detection deglitch filter time	-	27	30	33	μs
7	T <sub>FLT_VCCUVL</sub>	VCC under voltage low detection deglitch filter time	-	1.5	2	2.5	μs

Table 52. VCC converter external components design info

No	Symbol	Component	Conditions	Min	Тур	Max	Unit
1	L <sub>VCCBCK</sub>	Inductance	Min 4.7 µH nominal	3.76	-	-	μH
2	ESR <sub>LVCCBCK</sub>	Inductance resistance	-	-	-	0.25	Ω
3	C <sub>BLK_VCCBCK</sub>	Output bulk capacitance	Min 4.7 μF nominal	3	-	30	μF
4	ESR <sub>CBLK_VCCBCK</sub>	Bulk capacitor ESR	-	-	-	50	mΩ

# 16.15 VSF regulator

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35V, VSF + 2V  $\leq$  ERBOOST

Table 53. VSF regulator DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1			All line, load, IO_VSF up to 6mA SYS_CGF(VSF_V)= 0	18	20	22	V
2	VSF	Output voltage	All line, load, IO_VSF up to 6mA Only in case SYS_CTL(ER_BST_V)=1 SYS_CGF(VSF_V) = 1	23	25	27	V
3	I <sub>LIM_VSF</sub>	Output load current limit	VSF = 0	7	10	13	mA
4	V <sub>DO_VSF</sub>	Drop-out voltage	V(ERBOOST-VSF)	-	-	2	V
5	C <sub>VSF</sub>	Output capacitance	Design Info	2.9	-	14	nF



Table 53. VSF regulator DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
6	I <sub>LKG_VSF_OFF</sub>	VSF input leakage	Device OFF	-5	-	5	μA
7	R <sub>PD_VSF</sub>	VSF pull-down resistance	Device ON VSF regulator OFF; VSF = 25V	60	125	220	kΩ
8	I <sub>PD_VSF</sub>	VSF pull-down current	Device ON VSF regulator ON; Design Info	34	40	46	μΑ
9	I <sub>PD_VSF_TOT</sub>	VSF total pull-down current	Device ON VSF regulator ON VSF = 25V SYS_CGF(VSF_V)= 1	147	230	462	μА

Table 54. VSF regulator AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>ON_VSF</sub>	VSF turn on time	C <sub>VSF</sub> = 14 nF Measured from VSF_EN=1 to VSF inside regulation limits	-	-	100	μs

# 16.16 Deployment drivers

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35V, 6V  $\leq$  SSxy  $\leq$  35V, SSxy - SFx  $\leq$  25V.

Table 55. Deployment drivers - DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	I <sub>DEPL_LO</sub>	Deployment Current  Deployment Current Counter Threshold  Low side Over Current	R = 2 ohms Considering 9mA as not detected leakage with a 1kOhm equivalent resistance from SFx to GND	1.33	1.4	1.6	А
2	I <sub>DEPL_HI</sub>		R = 2 ohms, 9V ≤ SSxy Considering 13.5mA as not detected leakage with a 1kOhm equivalent resistance from SFx to GND,	1.94	1.99	2.3	Α
3	I <sub>TH_DEPL</sub>	Deployment Current Counter Threshold	-	I <sub>DEPL</sub> x  90%	-	-	Α
4	I <sub>OC_SR</sub>	Low side Over Current Detection	-	2.2	3.1	4.0	А
5	I <sub>LIM_SR</sub>	Low side Current Limitation	-	2.2	3.1	4.0	Α

Table 55. Deployment drivers - DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
6	ΔI <sub>LIM_OC_SR</sub>	Difference between Current Limitation and OC Threshold	I <sub>LIM_SR</sub> - I <sub>OC_SR</sub>	0.1	-	-	mA
7	R <sub>DSON_HSLS</sub>	Combined High side MOS + Low side MOS On Resistances	Ta = 95°C	-	-	2	Ω
8	I <sub>REV_SF</sub>	Reverse Current on SFx	Without device malfunction <sup>(1)</sup> Not to be tested in series production	-	-	-100	mA
9	I <sub>LKG_SS_OFF</sub>		Device OFF SSxy ≤ 35 V SFx=SFy=0	-10	-	10	μА
10	ILKG_SS_ON_ 1CH		Device ON SSxy ≤ 35 V SFx = 0 SSxy Leakage current of each channel Not Tested	70	100	130	μА
11	I <sub>LKG_SS_ON</sub>	SSxy leakage current	Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels NOT armed (= 2 * 100µA)	140	200	260	μА
12	ILKG_SS_CH_ ARMED		Device ON SSxy ≤ 35 V SFx = 0 Total SSxy leakage current with only one channel armed (=520 + 100 µA)	450	620	850	μА
13	ILKG_SS_2CH _ARMED		Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels armed (= 2* 520 µA) Not Tested	884	1040	1196	μА



Table 55. Deployment drivers – DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
14	I <sub>LKG_SF_ON_</sub>		Device ON, SYNCBOOST = SSxy = 35V, SFx = 0V	-5	-	5	μА
15	I <sub>LKG_SF_ON_</sub> 35V		Device ON, SYNCBOOST = SSxy = 35V, SFx = 35V	-5	-	50	μА
16	ILKG_SF_OFF _0V	SF Leakage Current	Device OFF SYNCBOOST = open, SSxy = open but all SSxy pins connected, SFx = 0V	-5	-	5	μА
17	ILKG_SF_OFF _35V		Device OFF SYNCBOOST = open, SSxy = open but all SSxy pins connected, SFx = 35V	-5	-	50	μА
18	I <sub>LKG_SR_ON</sub>		Device ON, SYNCBOOST = SSxy = 35V, SRx = 0V-35	-	-	50	μА
19		SR Leakage Current	DEVICE OFF, SYNCBOOST = open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx=0V-20V	-	-	50	μА
20	P I <sub>LKG_SR_OFF</sub>		DEVICE OFF, SYNCBOOST = open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx=35V	-	-	30	μА
21	V <sub>SR_CLAMP</sub>	SR voltage clamp	-	35	-	40	V
22	L <sub>DEPL</sub>	Load Inductance	Maximum load inductance Design Info <sup>(2)</sup>	0	-	56	μH
23	C <sub>SFx</sub>	Load Capacitance	Maximum capacitance to GND	13	-	455	nF
24	C <sub>SRx</sub>	сова Фарабівнов	Design Info	13	-	455	nF



Table 55. Deployment drivers - DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
25	C <sub>SSxy</sub>	SSxy Capacitance	Maximum capacitance to GND connected directly to SSxy pin Design Information	-	-	10	nF
26	$R_{SFLx}$	Load Impedance	Design Info	-	-	6.5	Ω
27		Wire Length	Squib Loops containing a clock spring shall be limited to a maximum length of 3m	1	-	10	m
28	R <sub>Wirex</sub>	Wire Resistance	Design Info	16.8	-	63.4	mΩ/ m
29	L <sub>Wirex</sub>	Wire Inductance	Design Info	0.6	-	1.8	μΗ/ m
30	R <sub>CSx</sub>	Clock Spring Resistance	Maximum number of clock springs is 3 for any IC Design Info	0	-	0.7	Ω
31	L <sub>CSx</sub>	Clock Spring Inductance	Design Info	0	-	42.9	μH
32	k <sub>L_CS1</sub> – L_CS2	Clock Spring Coupling	Design Info	0.739	-	0.903	-
33	L <sub>EMI</sub>	Squib EMI protection	Design Info	0	-	7.7	μH

<sup>1.</sup> In case of an unsupplied device and shorted deployment pins (e.g. to battery voltage), the dynamic reverse current through the high side power stage depends on C<sub>SSxy</sub>.

```
Non-Clock Spring Loops: L_{DEPL}(max) = L_{Wire}(10m*2) + L_{EMI} = (3.6uH/m*10m) + 7.7uH = 43.7uH
```

 $\begin{array}{l} \textbf{Clock Spring Loops: } L_{Wire}(3m*2) + 2*L_{CSx} + L_{EMI} - (2*k_{L-CX}*SQRT(L\_CS1*L\_CS2)) = \\ (2*0.739*42.9uH) = 40.9uHClock Spring Loops with short to ground \\ L_{DEPL}(max) = L_{Wire}(3m) + L_{CSx} + L_{EMI} = (1.8uH/m*3m) + 42.9uH + 7.7uH = 56uH. \end{array}$ 

577

<sup>2.</sup>  $L_{\text{DEPL}}$  could be calculated in the following way:

Squib EMI Clock Spring Squib Load System Wiring Impedance **ESD/EMI Protection** Protection \_Impedance \_ I R\_CS1 L\_CS1 П R\_Wire 1 L\_Wire 1 п П R\_Squib Wire Lenght (m) k<sub>L\_CS1 - L\_CS2</sub> R\_Wire 2 I R\_CS2 L\_CS2 GAPGPS01153

Figure 72. Deployment drivers diagram

Table 56. Deployment drivers - AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1				- DCR		DCR	
3	T <sub>DEPL</sub>	Deployment time	DCR_x(Dep_Current) = I <sub>DEPL_LO</sub> ≥1.209A rising to 1.209A falling; T <sub>DEPL</sub> = DCR_x(Deploy_Time)* T <sub>DEP_TIME_RES</sub> - TDEL_IDEP	x(Depl oy_Ti me)* TDEP _TIM E_RE S - 65	-	_x(D eploy _Tim e)* T <sub>DEP</sub> _TIME _RES -	ms
4	T <sub>DEP_TIME_RES</sub>	DCR_x Deploy_Time resolution	-	-	1024 f <sub>osc</sub>	-	μs
5	T <sub>DEP_CC_RES</sub>	Deployment current counter resolution	-	-	256 f <sub>osc</sub>	-	μs
6	T <sub>RISE_IDEPL</sub>	Rise time 10% - 90% of I <sub>DEPL</sub>	SSxy = 25 V,	-	i	32	μs
7	T <sub>DEL_IDEP</sub>	Delay time SPI_CS to 90% I <sub>DEPL</sub>	R <sub>SQ</sub> = 2.2 ohm, C = 22 nF L = 44 µH	-	-	65	μs
8	T <sub>FALL_IDEPL</sub>	Fall time 90% - 10% I <sub>DEPL</sub>		-	-	32	μs
9	T <sub>DEL_SD_LS</sub>	Low side shutdown delay time (with respect to high-side deactivation)	-	50	-	-	μs

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
10	T <sub>FLT_ILIM_LS</sub>	Low side overcurrent to low side deactivation deglitch time in short to battery condition	-	80	100	120	μs
11	T <sub>FLT_OS_LS</sub>	Low side overcurrent to high side deactivation deglitch time in case of intermittent open to squib condition	-	-	-	20	μs
12	T <sub>OFF_OS_HS</sub>	High side OFF time in case of intermittent open to squib condition	-	4	-	12	μs

Table 56. Deployment drivers - AC specifications

## 16.17 Deployment driver diagnostic

## 16.17.1 Squib resistance measurement

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0}$ (max)  $\leq$  VIN  $\leq$  35 V, 6 V  $\leq$  SSxy  $\leq$  35 V, 7 V  $\leq$  SYNCBOOST  $\leq$  35 V.

Table 57. Deployment drivers diagnostics - Squib resistance measurement

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	R <sub>SQ_RANGE_1</sub>	Squib resistance range 1	LPDIAGREQ(ISRC_CURR_ SEL) = 0	0	-	10.0	Ω
2	R <sub>SQ_RANGE 2</sub>	Squib resistance range 2	LPDIAGREQ(ISRC_CURR_ SEL) = 1	0	-	50.0	Ω
3	G <sub>RSQ</sub>	Squib resistance measurement Differential amplifier gain	$V_{OUT\_RSQ} = G_{RSQ} \times [(V_{SF} - V_{SR})] + V_{off\_RSQ}$	-2%	5.2	+2%	V/V
4	$V_{ m off\_RSQ}$	Squib resistance measurement Differential amplifier offset	$V_{OUT\_RSQ} = G_{RSQ} \times [(V_{SF} - V_{SR})] + V_{off\_RSQ}$	200	-	400	mV
5	I <sub>SRC_HI_SF</sub> I <sub>SRC_HI_SR</sub>	Squib resistance measurement High current source	LPDIAGREQ(ISRC_CURR_ SEL) = 0 LPDIAGREQ(ISRC) = '01' or '10' SyncBoost = 11.5 V and 35 V	-5%	40	+5%	mA
6	I <sub>SRC_LO_SF</sub> I <sub>SRC_LO_SR</sub>	Squib resistance measurement Low current source	LPDIAGREQ(ISRC_CURR_ SEL) = 1 LPDIAGREQ(ISRC) ='01' or '10' SyncBoost = 11.5 V and 35 V	-10%	8	+10%	mA
7	I <sub>SRC_DELTA</sub>	Squib Resistance Measurement Delta Current Source	ISRC_HI_X - ISRC_LO_X	-5%	32	+5%	mA

Table 57. Deployment drivers diagnostics - Squib resistance measurement (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
8	SR <sub>ISRC</sub>	Squib resistance measurement current source slew-rate	-	3	7.5	12	mΑ/μs
9	V <sub>SRx_RM</sub>	SRx voltage during resistance measurement	LPDIAGREQ(ISRC)="01" or "10" LPDIAGREQ(ISINK)=1	0.4	0.7	1.2	V
10	I <sub>SINK_HI_SR</sub>	SRx current sink limit high	LPDIAGREQ(ISRC_CURR_ SEL) = 0 LPDIAGREQ(ISINK) = 1	50	75	100	mA
11	I <sub>SINK_LO_SR</sub>	SRx current sink limit low	LPDIAGREQ(ISRC_CURR_ SEL) = 1 LPDIAGREQ(ISINK) = 1	10	17.5	25	mA
12	I <sub>PD_SR_L</sub>	SRx current pull down	SYS_CTL(PD&VRCM_SEL) = 0	0.7	1	1.3	mA
13	I <sub>PD_SR_H</sub>	- SKX Current pull down	SYS_CTL(PD&VRCM_SEL) = 1	4.5	6	7.5	mA
14	R <sub>LKG_SF</sub>	SFx leakage resistance	Design info	1	-	-	kΩ
15	V <sub>LKG_SF</sub>	SFx leakage voltage source	Design info	-1	-	18	V
16	R <sub>SQ_ACC</sub>	Squib resistance measurement accuracy	After software calculation All errors included $R_{SQ}$ between 1.0 $\Omega$ and 10.0 $\Omega$ With High Current Source (40 mA)	-8%	-	+8	%
17	-	EMI input low-pass filter	Design Info	50	-	100	kHz

## 16.17.2 Squib leakage test (VRCM)

All electrical characteristics are valid for the following conditions unless otherwise noted: -40  $^{\circ}$ C  $\leq$  Ta  $\leq$  +95  $^{\circ}$ C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V.

Table 58. Squib Leakage Test (VRCM)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	.,	Output Voltage on SF or	I <sub>OUT</sub> = 0 mA	-10%	2.5	+10%	V
2	V <sub>OUT_VRCM</sub>	SR pins during Leakage test	I <sub>OUT</sub> = 6.6 mA	1.9	-	2.5	V
3	R <sub>LKG_GSG_TH</sub>		Leakage detected if $R_{LKG\_GSG}$ $\leq$ 1 kΩ and not detected if $R_{LKG\_GSG} \geq$ 10 kΩ Design Info	1	-	10	kΩ
4a	ILKG_GSQ_TH_L	Detection threshold, leakage to GND	Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -25 °C $\leq$ T <sub>j</sub> $\leq$ +150 °C guaranteed by design/characterization	-15.5 %	450	+15.5 %	μΑ
4b			Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -40 °C $\leq$ T <sub>j</sub> $\leq$ +150 °C	-17%	450	+15.5 %	μА
5	I <sub>LKG_GSQ_TH_H</sub>		SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	15%	mA
6	T <sub>FLT_LKG</sub>	Leakage to GND deglitch filter time	-	17	20	23	μs
7	R <sub>LKG_BSQ_TH</sub>		Leakage detected if $R_{LKG\_GSG}$ ≤ 1 kΩ and not detected if $R_{LKG\_GSG}$ ≥ 10 kΩ Design Info	1	-	10	kΩ
8a	I <sub>LKG_BSQ_TH</sub>	Detection threshold, leakage to battery	Equivalent to resistance range $-25  ^{\circ}\text{C} \leq \text{T}_{\text{j}} \leq +150  ^{\circ}\text{C}$ guaranteed by design/characterization	-12%	1.8	+15%	mA
8b			-40 °C ≤ T <sub>j</sub> ≤ +150 °C	-17%	1.8	+15%	mA
9	T <sub>FLT_LKG</sub>	Leakage to BAT deglitch filter time	-	17	20	23	μs
10	I <sub>LIM_VRCM_SRC</sub>	VPCM ourrent limitation	-	-20	-	-10	mA
11	I <sub>LIM_VRCM_SINK</sub>	VRCM current limitation	-	10	-	20	mA
12	V <sub>SHIFT</sub>	External ground or battery shift	Design Info	-1	-	+1	V

Table 58. Squib Leakage Test (VRCM)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
13	R <sub>SQ_LOW_TH</sub>		Design Info	200	-	500	Ω
14a	I <sub>RSQ_LOW_TH</sub>	Detection threshold for "resistance too low"	Equivalent to resistance range $-25 \text{ °C} \le T_j \le +150 \text{ °C}$ guaranteed by design/characterization	-12%	6	+12%	mA
14b			-40 °C ≤ T <sub>j</sub> ≤ +150 °C	-17%	6	+12%	mA
15	T <sub>FLT_RLOW</sub>	"Resistance too low" deglitch filter time	-	12	15	18	μs
16	R <sub>SQ_HIGH</sub>	Detection Threshold for	Design Info	2	-	5	kΩ
17	I <sub>RSQ_HIGH</sub>	"resistance too high"	Equivalent to resistance range	-17%	700	+17%	μA
18	T <sub>FLT_RHIGH</sub>	"Resistance too high" deglitch filter time	-	12	15	18	μs
19	T <sub>delay_STG_sele</sub>	Time needed to change the VRCM STG thresholds (450 µA-to-2 mA or 2 mA- to-450 µA)	guaranteed by design	-	-	2	μs

### 16.17.3 High/low side FET test

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0}$ (max)  $\leq$  VIN  $\leq$  35 V, 6 V  $\leq$  SSxy  $\leq$  35 V, 7 V  $\leq$  SYNCBOOST  $\leq$  35 V.

Table 59. High/low side FET test

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	I <sub>HS_FET_TH</sub>	Detection threshold high side FET test	-	-12%	1.8	+12%	mA
2	I <sub>LS_FET_TH</sub>	Detection threshold	SYS_CTL(PD&VRCM_SEL) = 0	-15.5%	450	+15.5%	μA
3	I <sub>LS_FET_TH_HIGH</sub>	low side FET test	SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	+15%	mA
4	E <sub>FET_TEST</sub>	Energy transferred to squib during HS/LS FET tests	Design Info	-	-	170	μJ
5	T <sub>DRIVER_DIS</sub>	Driver Disable time	Guarantee by design	-	-	1.5	μs
6	T <sub>TOT_FETTEST_A</sub> CTIVE	Total FET test activation time in case of no fault condition	Guarantee by design	-	-	4	μs
7	T <sub>FETTIMEOUT</sub>	HS/LS FET test timeout	-	190	200	210	μs

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
8	T <sub>FLT_LKGB_FT</sub>	Deglitch filter time during FET test on I <sub>HS_FET_TH</sub> / I <sub>LS_FET_TH</sub> current thresholds	-	0.8	1	1.2	μs
9	I <sub>LIM_HS_FET</sub>	HS FET current in HS driver diagnostics	Not tested, see item # 1 in errata sheet section	40	50	60	mA
10	SGxy <sub>OPEN</sub>	Squib open ground detection	GNDSUBx as ground reference	300	450	600	mV
11	T <sub>FLT_SGOPEN</sub>	Squib open ground detection filter time	-	46	50	54	μs

Table 59. High/low side FET test (continued)

### 16.17.4 Deployment timer test

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{\rm GOOD0} \leq$  VIN  $\leq$  35 V.

Table 60. Deployment timer test - AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	t <sub>PULSE</sub> PERIOD	Deployment timer pulse test period time		7	8	9	ms
2	I <sub>PULSE_HIGH</sub>	Deployment timer pulse test high time	SYSDIAGREQ(DSTEST)=PULSE	-	DCR_x( Deploy_ Time)* T <sub>DEP_TIM</sub> E_RES	-	μs

### 16.18 Remote sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V, V $_{SATBUCK}$ (min)  $\leq$  VSATBUCK,

 $V_{SYNCBOOST}(min) \leq VSYNCBOOST$ 

#### 16.18.1 PSI-5 interface

Table 61. PSI-5 satellite transceiver - DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	I <sub>RSU</sub>	Interface quiescent current	-	-35	-	-4	mA
2	V <sub>RSU_MAX</sub>	Max. output voltage excluding sync. pulse	(internal regulation, VSATBUCK = VSYNCBOOST)	-	-	11	٧



Table 61. PSI-5 satellite transceiver - DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
3	V <sub>RSU_SYNC_MAX</sub>	Max. output voltage including sync. pulse	(internal regulation, VSYNCBOOST = VIN) Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	-	16.5	V
4	R <sub>RSU</sub>	RSU output resistance	From I <sub>RSU</sub> = -4 mA to -65 mA	3	-	9.5	Ω
5	I <sub>STB_TH</sub>	Static reverse current into SATBUCK or SYNCBOOST pin (V <sub>SUPPLY</sub> )	V <sub>RSUx</sub> > V <sub>SUPPLY</sub> + V <sub>RSU_STB</sub>	0.0	-	10	mA
6	V <sub>RSU_STB</sub>	Output short to battery threshold	-	10.0	-	100	mV
7	I <sub>OCTH_PSI5</sub>	Over current detection threshold	Interface disabled after T <sub>FLT_OCTH_PSI5</sub>	-120	-	-66	mA
8	I <sub>LIM_PSI5</sub>	Output current limit	I <sub>RSUx</sub>	-130	-	-80	mA
9	Δl <sub>LIM_OC_PSI5</sub>	Difference between current limitation and OC threshold	ABS(I <sub>LIM_RSU</sub> ) - ABS(I <sub>OCTH_RSU</sub> )	10	-	-	mA
10	I <sub>BO</sub>	Base current	Default value	-15%	-15	+15%	mA
11	I <sub>LKGG</sub>	Trigger point for fault	To ground; detected by I <sub>B</sub>	-50.4	-42	-35	mA
12	I <sub>LKGB</sub>	current detection	To battery; detected by I <sub>B</sub>	-3.5	-	-1	
13	I <sub>OL</sub>	Output open load detection threshold	V <sub>RSUx</sub> = open	I <sub>LKGB</sub>	-	I <sub>LKGB</sub> (max)	mA
14	DAC <sub>RES</sub>	DAC resolution	-	-	10	-	Bit
15	I <sub>LSB</sub>	LSB current	Design Info	-	93.75	-	μΑ
16	V <sub>t2</sub>	Sync pulse amplitude	I <sub>RSU</sub> = 4 - 35 mA Referred to V <sub>RSUx</sub> voltage before sync pulse Syncboost = 12 V, 14.75 V, 18 V and 35 V	3.8	-	-	V
17	V <sub>SYNCDROP</sub>	Sync drop-out voltage	V <sub>SYNCBOOST</sub> - V <sub>RSUx</sub>	1	-	-	V
18	I <sub>LIM_SYNC_LS</sub>	Sync pulse current limit (LS driver)	-	50	-	80	mA
19	I <sub>LIM_SYNC</sub>	Static current limitation for each transceiver output RSUx	During sync pulse generator V <sub>RSUx=GND</sub>	-240	-	-120	mA
20	C <sub>1</sub>	Capacitor on RSUx Regulator	22 nF nominal Design Info	13	-	-	nF
21	R <sub>E2</sub>	RSU damping resistance	Design info	-	2.5	-	Ω
22	C <sub>2</sub>	ECU pin capacitance	5 nF nominal Design Information, not tested	4	-	6	nF
23	-	Total number of sensors connected to bus	Design info	1	-	3	-

Table 62. PSI-5 satellite transceiver - AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>Bit_125k</sub>	Bit time (125 kbps mode)	At the sensor connector	7.6	8	8.4	μs
2	T <sub>Bit_189k</sub>	Bit time (189 kbps mode)	At the sensor connector	5	5.3	5.6	μs
3	T <sub>FLT_OCTH_PSI5</sub>	Over Current Detection deglitch filter time	Normal operation	500	-	600	μs
4	т	Over Current	At interface power on (BLKTxSEL = 0)	4.6	-	5.4	ms
5	T <sub>BLK_OCTH_PSI5</sub>	Detection Blanking Time	At interface power on (BLKTxSEL = 1)	9.4	-	10.8	ms
6	Т <sub>SТВТН</sub>	Reverse Battery Blocking Enable Time	-	12	-	16	μs
7	$t_0$	Reference time	@0.5 V on top of V(RSUx) Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	0	-	-
8	t <sub>1</sub>	Start delay time	From t0 to SATSYNC Syncboost = 12 V, 14.75 V, 18 V and 35 V	-3	-	-	μs
9	t <sub>2</sub>	Sync signal sustain start	@ VRSU+3.8 V relative to t <sub>0</sub> Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	-	7	μs
10	SR <sub>RISE_RSU</sub>	Sync slope rising slew rate		0.43	-	1.5	V/µs
11	SR <sub>FALL_RSU</sub>	Sync slope falling slew rate		-1.5	-	-	V/µs
12	t <sub>3</sub>	Sync signal sustain time	Design Info	16	-	-	μs
13	t <sub>4</sub>	Discharge time limit	Design Info	-	-	35	μs
14	T <sub>BLANK</sub>	Decoder blanking time (decoding disabled)	Design Info	-	-	42	μs
15	T <sub>SYNC</sub>	Time between two sync pulses	Design Info	400	500	-	μs
16	T <sub>FLT_PSI5_HF</sub>	PSI5 Deglitch filter time	F = 189 kbaud Configurable by SPI (4bits)	1	-	2	μs
17	T <sub>FLT_PSI5_LF</sub>	PSI5 Deglitch filter time	F = 125 kbaud Configurable by SPI (4bits)	1.5	-	2.5	μs

Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
18			Related to t0, Sensor Side, P8P-500-3L	44	-	58.6	μs
19			Related to t0, Sensor Side, P8P-500-3H	44	-	58.6	μs
20	T T	Message start	Related to t0, Sensor Side, P8P-500-4H	44	-	58.6	μs
21	T_ES_1, T_LS_1	time, Slot 1	Related to t0, Sensor Side, P10P-500-3L	44	-	58.6	μs
22			Related to t0, Sensor Side, P10P-500-3H	44	-	58.6	μs
23			Related to t0, Sensor Side, P10P-500-4H	44	-	58.6	μs
24			Related to t0, Sensor Side, P8P-500-3L	181.3	-	210.4	μs
25			Related to t0, Sensor Side, P8P-500-3H	181.3	-	210.4	μs
26	т т	Message start	Related to t0, Sensor Side, P8P-500-4H	139.5	-	164.2	μs
27	T_ES_2, T_LS_2	time, Slot 2	Related to t0, Sensor Side, P10P-500-3L	181.3	-	210.4	μs
28			Related to t0, Sensor Side, P10P-500-3H	181.3	-	210.4	μs
29			Related to t0, Sensor Side, P10P-500-4H	139.5	-	164.2	μs
30			Related to t0, Sensor Side, P8P-500-3L	328.9	-	373.5	μs
31		Message start	Related to t0, Sensor Side, P8P-500-3H	328.9	-	373.5	μs
32	т т		Related to t0, Sensor Side, P8P-500-4H	245.5	-	281.3	μs
33	T_ES_3, T_LS_3	time, Slot 3	Related to t0, Sensor Side, P10P-500-3L	328.9	-	373.5	μs
34			Related to t0, Sensor Side, P10P-500-3H	328.9	-	373.5	μs
35			Related to t0, Sensor Side, P10P-500-4H	245.5	-	281.3	μs
36			Related to t <sub>0</sub> , Sensor Side, P8P-500-3L	107.2	-	127.6	μs
37			Related to t <sub>0</sub> , Sensor Side, P8P-500-3H	82	-	99.4	μs
38	т	Slot 1 End valid window,	Related to t <sub>0</sub> , Sensor Side, P8P-500-4H	82	-	99.4	μs
39	T_s1_end_open	opening time	Related to t <sub>0</sub> , Sensor Side, P10P-500-3L	121	-	142.8	μs
40			Related to t <sub>0</sub> , Sensor Side, P10P-500-3H	91	-	109.4	μs
41			Related to t <sub>0</sub> , Sensor Side, P10P-500-4H	91	-	109.4	μs
42			Related to t0, Sensor Side, P8P-500-3L	151	-	174.6	μs
43			Related to t0, Sensor Side, P8P-500-3H	119.8	-	139.9	μs
44	т,	Slot 1 End valid window,	Related to t0, Sensor Side, P8P-500-4H	119.8	-	139.9	μs
45	T_s1_end_closure	closure time	Related to t0, Sensor Side, P10P-500-3L	167.8	-	193	μs
46			Related to t0, Sensor Side, P10P-500-3H	131	-	152.5	μs
47			Related to t0, Sensor Side, P10P-500-4H	131	-	152.5	μs



Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
48			Related to t0, Sensor Side, P8P-500-3L	231.6	-	264.9	μs
49			Related to t0, Sensor Side, P8P-500-3H	206	-	236.7	μs
50	_	Slot 2 End valid	Related to t0, Sensor Side, P8P-500-4H	168	-	194.9	μs
51	T_s2_end_open	window, opening time	Related to t0, Sensor Side, P10P-500-3L	245.4	-	280.1	μs
52			Related to t0, Sensor Side, P10P-500-3H	215.5	-	246.7	μs
53			Related to t0, Sensor Side, P10P-500-4H	177.5	1	205	μs
54			Related to t0, Sensor Side, P8P-500-3L	302.8	-	342.1	μs
55			Related to t0, Sensor Side, P8P-500-3H	271.6	-	308	μs
56	_	Slot 2 End valid	Related to t0, Sensor Side, P8P-500-4H	225.4	-	256.5	μs
57	T_s2_end_closure	window, closure time	Related to t0, Sensor Side, P10P-500-3L	319.6	-	360.5	μs
58			Related to t0, Sensor Side, P10P-500-3H	282.7	-	320	μs
59			Related to t0, Sensor Side, P10P-500-4H	236.5	-	269	μs
60			Related to t0, Sensor Side, P8P-500-3L	365.1	-	412.5	μs
61			Related to t0, Sensor Side, P8P-500-3H	339.4	-	384.3	μs
62	_	Slot 3 End valid window, opening time	Related to t0, Sensor Side, P8P-500-4H	263.9	-	300.9	μs
63	T_s3_end_open		Related to t0, Sensor Side, P10P-500-3L	378.9	-	427.7	μs
64			Related to t0, Sensor Side, P10P-500-3H	348.5	-	394.3	μs
65			Related to t0, Sensor Side, P10P-500-4H	273	-	311	μs
66			Related to t0, Sensor Side, P8P-500-3L	465.9	-	522.7	μs
67			Related to t0, Sensor Side, P8P-500-3H	434.7	-	488	μs
68	_	Slot 3 End valid window,	Related to t0, Sensor Side, P8P-500-4H	342.5	-	386.1	μs
69	T_s3_end_closure	closure time	Related to t0, Sensor Side, P10P-500-3L	482.7	-	541.1	μs
70			Related to t0, Sensor Side, P10P-500-3H	445.9	-	500	μs
71			Related to t0, Sensor Side, P10P-500-4H	353.7	-	398.2	μs
72	T <sub>SYNC_DLY_SHORT</sub>	Sync Pulse Start	SYS_CFG(RSU_SYNCPULSE_SHIFT _CONF)=0 Related to Start of Sync Pulse on ch. N-1	-	160 f <sub>osc</sub>	-	μs
73	T <sub>SYNC_DLY_LONG</sub>	Delay	SYS_CFG(RSU_SYNCPULSE_SHIFT _CONF)=1 Related to Start of Sync Pulse on ch. N-1	-	288 f <sub>osc</sub>	-	μs
74	T <sub>FLT_OPEN_RSU</sub>	Open Detection Deglitch Filter Time	-	10	-	15	μs
75	T <sub>FLT_LKG_RSU</sub>	Leakage Deglitch Filter Time	-	10	-	15	μs



Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
76	T <sub>WRITE_EN_DELAY_LF</sub>	Data register	Design Info F = 125 kbaud Calculated from transition of last sensor bit to when data is available in SPI register	-	-	19	μs
77	T <sub>WRITE_EN_DELAY_HF</sub>	write delay	Design Info F = 189 kbaud Calculated from transition of last sensor bit to when data is available in SPI register	-	-	14	μs

## 16.18.2 WSS interface

Table 63. WSS sensor - DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	C <sub>1</sub>	RSU load capacitance	10nF nominal, Design Info	6	-	-	nF
2	V <sub>RSU_MAX</sub>	RSUx Max output voltage	(internal regulation, VSATBUCK=VSYNCBOOST)	-	-	11	V
3	R <sub>RSU</sub>	Output resistance	From I <sub>RSU</sub> =-4mA to -35mA	4	-	12	Ω
4	I <sub>BO</sub>	Base Current	Auto Adaptive option (default value)	+15%	-7	-15%	mA
5a	I <sub>TH1</sub>	7mA / 14mA detection	Fixed threshold option $-25 ^{\circ}\text{C} \leq \text{T}_{\text{j}} \leq +150 ^{\circ}\text{C}$ guaranteed by design/characterization	+15%	-9.8	-15%	mA
5b			Fixed threshold option $-40 ^{\circ}\text{C} \le \text{T}_{j} \le +150 ^{\circ}\text{C}$	+20%	-9.8	-20%	mA
6	I <sub>TH2</sub>	14mA / 28mA detection	Fixed threshold option	+15%	-19.6	-15%	mA
7a	I <sub>THOPEN</sub>	Open sensor detection	RSUx OPEN $-25 ^{\circ}\text{C} \leq \text{T}_{j} \leq +150 ^{\circ}\text{C}$ guaranteed by design/characterization	-4.5	-	-0.2	mA
7b			RSUx OPEN -40 °C $\leq$ T <sub>j</sub> $\leq$ +150 °C	-5.5	-	0	mA
8	I <sub>THGND</sub>	Leakage to GND threshold	V <sub>RSUx</sub> = GND	13.2	15	17.1	mA
9	I <sub>OCTH_WSS</sub>	Over Current Detection Threshold	output disabled after T <sub>FLT_OCTH_WSS</sub>	-65	-	-38	mA
10	I <sub>LIMTH_WSS</sub>	Output Current Limit	-	-65	ı	-40	mA
11	ΔI <sub>LIM_OC_WSS</sub>	Difference between Current Limitation and OC Threshold	I <sub>LIM_RSU</sub> - I <sub>OC_RSU</sub>	1	-	-	mA



Table 63. WSS sensor - DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
12	V <sub>RSU_STB</sub>	Output Short to Battery Threshold		10	-	100	mV
13	І <sub>ЅТВТН</sub>	Static reverse current into SATBUCK or SYNCBOOST pin (V_supply)	V <sub>RSUx</sub> > V_supply + V <sub>RSUxSTB</sub>	0.0	-	10	mA
14	V <sub>OH_WS</sub>	WSx Output Voltage	I <sub>LOAD</sub> = -1mA	VCC- 0.5	-	VCC	V
15	V <sub>OL_WS</sub>		I <sub>LOAD</sub> = 1mA	-	-	0.4	V
16	I <sub>LKG_WS</sub>	WSx Output Leakage	Tri-state leakage	-10	-	10	μA

Table 64. WSS sensor - AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	T <sub>FLT_WS</sub>	WS Deglitch filter time	Configurable by SPI (4bits)	8	-	15.6	μs
2	-	Latency time	between receiving sensor data @ RSUx pin and reaching threshold high level of WSx pin (trigger point 80% of RSUx modulated current)	-	-	2+ T <sub>FLT</sub> ws	μs
3	-	Jitter on Latency time	Design Info	-	-	125	ns
4	T <sub>FLT_OCTH_WS</sub>	Over Current Detection Deglitch filter time	-	500	-	600	μs
5	T <sub>FLT_OPEN_RS</sub> U	Open Detection Deglitch Filter Time	-	10	-	15	μs
6	T <sub>FLT_LKG_RSU</sub>	Leakage Deglitch Filter Time	-	10	-	15	μs
7	T <sub>STANDSTILL_T</sub>	Pulse duration to assert	-	1.13	-	-	ms
8	T <sub>STANDSTILL_T</sub>	standstill bit thresholds	-		-	2.55	ms

## 16.19 DC sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0}$   $\leq$  VIN  $\leq$  35 V, 8.5 V  $\leq$  SYNCBOOST  $\leq$  35 V.

Table 65. DC Sensor interface specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>OUT_DCSREG</sub>	DCS output voltage regulation mode	DCS regulator enabled SyncBoost = 11.5 V and 35 V	-10%	6.25	+10%	٧
2	I <sub>LIM_DCSREG</sub>	DCS current limitation regulation mode	DCS regulator enabled SyncBoost = 11.5 V and 35 V	24	27	30	mA
3	V <sub>DCS_RANGE1</sub>	DCS voltage measurement range1	First voltage measurement (V <sub>DCS_MEAS1</sub> ) to compensate external ground shift and internal offset	-1	-	1.4	V
4	V <sub>DCS_ACC1</sub>	DCS voltage measurement accuracy 1	V <sub>DCS</sub> = V <sub>DCS_RANGE1</sub> Included ADC error	-15	-	15	%
5	V <sub>DCS_RANGE2</sub>	DCS voltage measurement range 2	-	1.5	-	10	V
6	V <sub>DCS_ACC2</sub>	DCS voltage measurement accuracy 2	V <sub>DCS</sub> = V <sub>DCS_RANGE2</sub> Included ADC error	-8	-	+8	%
7	I <sub>DCS_RANGE1</sub>	DCS Current measurement range 1	-	1	-	2	mA
8	I <sub>DCS_ACC1</sub>	DCS current measurement accuracy 1	I <sub>DCS</sub> = I <sub>DCS_RANGE1</sub> Included ADC error	-30	-	+30	%
9	I <sub>DCS_RANGE2</sub>	DCS current measurement range 2	-	2	-	22	mA
10	I <sub>DCS_ACC2</sub>	DCS current measurement accuracy 2	I <sub>DCS</sub> = I <sub>DCS_RANGE2</sub> Included ADC error	-12	-	+12	%
11	I <sub>DCS_RANGE3</sub>	DCS current measurement range 3	Regulator in current limitation	-	I <sub>LIM_D</sub> CSREG	-	mA
12	I <sub>DCS_ACC3</sub>	DCS Current measurement accuracy 3	V <sub>DCS</sub> = 0V Included ADC error	-12	-	+12	%
13	R <sub>DCS_RANGE</sub>	DCS resistance measurement range	Design info	65	-	3000	Ω
14	R <sub>DCS_ACC</sub>	Accuracy of digital resistance measurement	Performing voltage measurements 1 and 2 After software calculation all errors included	-15	-	15	%
15	I <sub>PD_DCS</sub>	DCSx current pull down	V <sub>DCS</sub> = 1.5 V	130	200	260	μA
16	R <sub>PD_DCS</sub>	DCSx resistance pull down	Device active, DCSx current pull down disabled	90	150	210	kΩ

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
17	I <sub>PD_DCS_TOT</sub>	DCSx total current pull down	I <sub>PD_DCS_TOT</sub> = I <sub>PD_DCS</sub> + R <sub>PD_DCS</sub> V <sub>DCS</sub> = 6.5 V	160	240	330	μA
18	C <sub>DCS</sub>	Output capacitance	Design Info	10	-	-	nF
19	I <sub>REF_DCS</sub>	Internal Current Reference for DCS Current Measurement	-	-5%	300	+5%	μA
20	Ratio_VDCS	Divider ratio for DCSx voltage measurement	-	-3%	7.125	+3%	V/V
21	V <sub>OFF_DCS</sub>	DCSx internal offset during voltage measurement	-	0.35	0.375	0.39	\ \

Table 65. DC Sensor interface specifications

# 16.20 Safing engine

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V, VCCx(min)  $\leq$  VCCx  $\leq$  VCCx(max), VCC = 3.3 V or 5 V.

Table 66. Arming Interface – DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>TH_H_ACL</sub>	ACL input voltage	-	2.33	-	2.5	V
2	V <sub>TH_L_ACL</sub>	thresholds	-	1.58	-	1.71	V
3	V <sub>HYS_ACI</sub>	ACL hysteresis	-	0.6	0.75	0.9	V
4	R <sub>PD_ACL</sub>	ACL pull down resistance	V <sub>ACL</sub> = 3.3V	150	210	270	kΩ
5	V <sub>OH_ARM</sub>	ARMx output high voltage	I <sub>LOAD</sub> = -0.5 mA internal safing selected	VCC-0.60	-	vcc	V
6	V <sub>OL_ARM</sub>	ARMx output low voltage	I <sub>LOAD</sub> = 2.0 mA internal safing selected	0	-	0.4	V
7	R <sub>PD_ARM</sub>	ARMx pull down resistance	-	65	100	135	kΩ
8	V <sub>IH_ARM</sub>	ARMx high level input voltage	-	2	i	ı	V
9	$V_{IL\_ARM}$	ARMx low level input voltage	-	-	-	0.8	V
10	R <sub>PD_ARMx, x=1,2,3</sub>	ARM1,2,3 pull down resistor	External safing selected	60	100	140	kΩ
11	I <sub>PU_ARM4</sub>	ARM4 pull up current	ARM4 = 0V external safing selected	-100	-75	-50	μA
12	V <sub>OH_PSINHB</sub>	PSINHB output high voltage	I <sub>LOAD</sub> = -0.5 mA Internal safing selected	VCC-0.60	-	VCC	V



Table 66. Arming Interface – DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
13	V <sub>OL_PSINHB</sub>	PSINHB output low voltage	I <sub>LOAD</sub> = 2.0 mA Internal safing selected	0	-	0.4	V
14	R <sub>PD_PSINHB</sub>	PSINHB pull down resistance	-	65	100	135	kΩ
15	V <sub>IH_PSINHB</sub>	PSINHB high level input voltage	-	2	-	-	V
16	V <sub>IL_PSINHB</sub>	PSINHB low level input voltage	-	-	-	0.8	V
17	V <sub>IH_SAF_CSx</sub>	SAF_CSx high level input voltage	-	2	-	-	V
18	V <sub>IL_SAF_CSx</sub>	SAF_CSx low level input voltage	-	-	-	0.8	
19	I <sub>PU_SAF_CSx</sub>	SAF_CSx pull up current	SAF_CSx = 0 V to V <sub>IH_SAF_CSx(min)</sub>	-70	-45	-20	μA

Table 67. Arming interface - AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
110	Cyllibol	i arameter	Conditions	141111	iyp	Wax	Oilit
1	T <sub>ARM</sub>	Sensor sampling period	-	475	500	525	μs
2	T <sub>ACL_HI</sub>	ACL period time thresholds	-	213	-	237	ms
3	T <sub>ACL_LO</sub>	THOSE period time timesholds	-	168	-	187	ms
4	T <sub>ON_ACL_HI</sub>	ACL on-time thresholds	-	154	-	171	ms
5	T <sub>ON_ACL_LO</sub>	TAGE ON-LINE UNCONOIDS	-	114	-	126	ms
6	T <sub>VALID_ACL</sub>	Scrap validation T <sub>ACL</sub> and T <sub>ON_ACL</sub> valid	-	3	-	-	cycles
7	T <sub>INVALID_ACL</sub>	Scrap invalid T <sub>ACL</sub> invalid	-	2	-	-	cycles
8	T <sub>SCRAP_TIMEOUT</sub>	Scrap timeout timer	-	520	550	580	μs
9	f <sub>SCRAP_SEED</sub>	Scrap seed counter frequency	-	-	$\frac{f_{\rm osc}}{16}$	-	MHz
10			-	-	-	0	ms
11	т	Arming enable pulse stretch	-	30	32	34	ms
12	T <sub>PULSE_STRECH</sub>	time	-	242	-	270	ms
13			-	1934	-	2162	ms
14	T <sub>RISE_ARM</sub>	ARMx rise time		-	-	1.00	μs
15	T <sub>FALL_ARM</sub>	ARMx fall time	50 pF load, 20% to 80%	-	-	1.00	μs
16	T <sub>RISE_PSINHB</sub>	PSINHB rise time	internal safing selected	-	-	1.00	μs
17	T <sub>FALL_PSINHB</sub>	PSINHB fall time		-	-	1.00	μs

## 16.21 General purpose output drivers

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN<sub>GOOD0</sub>  $\leq$  VIN  $\leq$  35V, VGPODx + 5V  $\leq$  VERBOOST.

Table 68. GPO interface DC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>SAT_GPO_L</sub>	Output saturation voltage	$V_{GPOD} - V_{GPOS}$ $I_{LOAD} = 50 \text{ mA}$ ERBOOST = 35 V	-	-	0.5	V
2	V <sub>SAT_GPO_H</sub>	Output saturation voltage	V <sub>GPOD</sub> – V <sub>GPOS</sub> I <sub>LOAD</sub> = 70 mA	-	-	0.7	V
3	I <sub>LIM_GPO</sub>	Driver current limit	$V_{GPOD} - V_{GPOS} = 1.5 V$ ERBOOST = 35 V	73	110	160	mA
4	I <sub>OC_GPO</sub>	Over current detection	ERBOOST = 35 V	73	110	160	mA
5	V <sub>OUT_GPOD_OL</sub>	GPO diag OFF output voltage on GPOD in low side mode in open load condition	GPOxLS = 1 I <sub>OUT</sub> = 0 mA	-10%	2.5	+10%	V
6	V <sub>OUT_GPOS_OL</sub>	GPO diag OFF output voltage on GPOS in high side mode in open load condition	GPOxLS = 0 I <sub>OUT</sub> = 0 mA	-10%	2.5	+10%	V
7	I <sub>SRC_TH</sub>	GPO diag OFF state short to ground detection threshold	GPOxLS = 0 / 1	15	27	40	μА
8	I <sub>SINK_TH_LS</sub>	GPO Diag OFF state short to battery detection threshold low side mode	GPOxLS = 1 GPOS = 0	15	27	46	μА
9	I <sub>SINK_TH_</sub> HS	GPO Diag OFF state short to battery detection threshold high side mode	GPOxLS = 0	170	220	270	μA
10	I <sub>LIM_GPOD_SRC</sub>	GPO Diag OFF state	GPOxLS = 1, GPO Driver OFF, GPOD = 0 V, GPOS = 0 V	-90	-70	-50	μА
11	I <sub>LIM_GPOD_SINK</sub>	current limitation on GPOD	GPOxLS = 1, GPO Driver OFF, GPOD = 18 V, GPOS = 0 V	50	70	90	μА
12	I <sub>LIM_GPOS_SRC</sub>	GPO Diag OFF state	GPOxLS = 0, GPO Driver OFF, GPOD = 18 V, GPOS = 0 V	-90	-70	-50	μА
13	I <sub>LIM_GPOS_SINK</sub>	current limitation on GPOS	GPOxLS = 0, GPO driver OFF, GPOD = 18 V,GPOS = 18 V	320	400	480	μА

Table 68. GPO interface DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
14	I <sub>OL_GPO</sub>	Open load current threshold	GPO driver ON	0.5	1	3	mA
15	I <sub>DIAG_GPO</sub>	Diagnostic current on load	Voltage measurement in progress through Analog MUX Increased leakage for a short specified time (32µs)	-	-	130	μА
16	I <sub>LKG_GPOD_OFF</sub>		V <sub>GPOD</sub> = 18 V V <sub>GPOS</sub> = 0V ERBOOST = 35 V Power-off or Sleep Mode	-5	-	+5	μА
17	I <sub>LKG_GPOD_ON</sub>	GPOD output leakage current	V <sub>GPOD</sub> = 18 V V <sub>GPOS</sub> = 0 V ERBOOST = 35 V GPO Driver OFF Active or Passive Mode with GPO un-configured	-5	-	+5	μА
18	I <sub>LKG_GPOS_OFF</sub>		V <sub>GPOD</sub> = 18 V V <sub>GPOS</sub> = 0 V ERBOOST = 35 V Power-off or Sleep Mode	-5	-	+5	μА
19	I <sub>LKG_GPOS_ON</sub>	GPOS output leakage current	V <sub>GPOD</sub> = 18 V V <sub>GPOS</sub> = 0 V ERBOOST = 35 V GPO Driver OFF Active or Passive Mode with GPO un-configured	-5	-	+5	μА
20	I <sub>REV_GPO</sub>	Reverse current	V <sub>GPOS</sub> = V <sub>GPOD</sub> + 1 V GPO Driver OFF	-	-	1	mA
21	T <sub>JSD_GPO</sub>	Thermal shutdown	-	150	175	190	°C
22	T <sub>HYS_TSD_GPO</sub>	THOMAS GRACOWII	-	5	10	15	°C
23	C <sub>GPO</sub>	Load capacitor	Design Info	6	-	-	nF

Table 69. GPO driver interface – AC specifications

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	SR <sub>GPOx</sub>	GPOx output voltage slew rate	30% - 70%; R <sub>LOAD</sub> = 273 Ω, C <sub>LOAD</sub> = 100 nF	0.1	0.25	0.4	V/µs
2	T <sub>FLT_OC</sub>	Over current detection filter time	GPO Driver ON	10	12	14	μs
3	T <sub>FLT_UC</sub>	Open load detection filter time	GPO Driver ON	8	10	12	μs
4	T <sub>FLT_STB</sub>	Short to battery detection in OFF state deglitch filter time	GPO Driver OFF	8	10	15	μs
5	T <sub>FLT_STG</sub>	Short to GND detection in OFF state deglitch filter time	GPO Driver OFF	8	10	15	μs
6	T <sub>MASK_STUP_ON</sub>	Diagnostic mask delay after switch ON	C <sub>GPOX</sub> = 100 nF typ	136	-	200	μs
7	T <sub>MASK_STUP_OFF</sub>	Diagnostic mask delay after switch OFF	C <sub>GPOX</sub> = 100 nF typ	520	-	584	μs
8	T <sub>FLT_TSD</sub>	Thermal shutdown filter time	-	-	-	10	μs
9	F <sub>PWM</sub>	GPO PWM frequency	Design Info	-	125		Hz
10	DC <sub>PWM</sub>	GPO PWM duty cycle	Increment step = 1.6%	0	-	100	%

## 16.22 Analog to digital converter

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN $_{GOOD0} \leq$  VIN  $\leq$  35 V.

Table 70. Analog to digital converter

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
1	V <sub>ADC_RANGE</sub>	ADC input voltage range	-	0.1	-	2.5	V
2	V <sub>ADC_REF</sub>	ADC reference voltage	-	-1.5%	2.5	+1.5%	V
3	ADC_RES	ADC resolution (1)	Design Info	-	10	-	bit
4	DNL	Differential non linearity error (DNL)	Separation between adjacent levels, measured bit to bit of actual and an ideal output step. No missing codes	-1	-	+1	LSB
5	INL	Integral non linearity error (INL)	Maximum difference between the actual analog value at the transition between 2 adjacent steps and its ideal value	-3	-	+3	LSB
6	E <sub>QUANT</sub>	Quantization error	Design Info	-0.5	-	0.5	LSB
7	TotErr	Total error	Includes INL, DNL, ADC Reference voltage tolerance and quantization error	-15	-	+15	LSB
8	TotErr_0v1	ADC total error for 0.1 V input voltage	-	-5	-	+5	LSB
9	TotErr_2v4	ADC total error for 2.4 V input voltage	-	-15	-	+15	LSB
10	R <sub>LSB_1</sub>	Reproducibility:	1x sampling measurements. Guaranteed by design	-6	-	6	LSB
11	R <sub>LSB_4</sub>	conversion result variation for constant	4x sampling measurements. Guaranteed by design	-3	-	3	LSB
12	R <sub>LSB_8</sub>	input signal	8x sampling measurements. Guaranteed by design	-2.5	-	2.5	LSB
13	Pre-ADC	Pre-ADC settling time	-	-	4.81	-	μs
14	T_TSC	Single conversion time	-	-	2.25	-	μs
15	IQ	Intra-queue settling time	-	-	3.5	-	μs
16	Post-ADC	Post- ADC settling time	-	-	3.44	-	μs

Table 70. Analog to digital converter (continued)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
17	-	ADC conversion time - voltage	4x sampling for each of the 4 conversions in the queue Design Info	-	54.75	-	μs
18	-	ADC conversion time – current and voltage	8x sampling for DCS, temperature and squib loop resistance measurements + 4x sampling for remaining 2 conversions in the queue Design Info	-	51.25	-	μs

<sup>1.</sup> LSB = (2.5V / 1024) = 2.44mV



## 16.23 Voltage diagnostics (Analog MUX)

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0}$   $\leq$  VIN  $\leq$  35V.

Table 71. Voltage diagnostics (Analog MUX)

No	Symbol	Parameter	Conditions	Min	Тур	Max	Units
1	Ratio_1		V <sub>IN_RANGE_1</sub> = 0.1 V to 2.5 V	-	1	-	V/V
2	Ratio_4		V <sub>INPUT_RANGE_4</sub> = 1 V to 10 V	-3%	4	+3%	V/V
3	Ratio_7	Divider ratios	V <sub>INPUT_RANGE_7</sub> = 1.5V to 17.5V	-3%	7	+3%	V/V
4	Ratio_10		V <sub>INPUT_RANGE_10</sub> = 2 V to 25 V	-3%	10	+3%	V/V
5	Ratio_15		V <sub>INPUT_RANGE_15</sub> = 3 V to 35 V	-3%	15	+3%	V/V
6	Offset	Divider Offset	High impedance	-10	-	10	mV
7	R <sub>RATIO_4</sub>		Multiplexer input to GNDA	80	-	-	kΩ
8	R <sub>RATIO_7</sub>	Multiplexer input	Multiplexer input to GNDA	120	-	-	kΩ
9	R <sub>RATIO_10</sub>	resistance	Multiplexer input to GNDA	160	-	-	kΩ
10	R <sub>RATIO_15</sub>		Multiplexer input to GNDA	200	-	-	kΩ
11	I <sub>LEAK_MUX_</sub> ON	Additional multiplexer on-state input leakage current	For all divider ratio expect ratio_1	-	-	60	μА
12	V <sub>MEAS_ACC</sub>	Voltage measurement accuracy	(±15LSB) plus divider error (±3%)				

## 16.24 Temperature sensor

All electrical characteristics are valid for the following conditions unless otherwise noted: 40 °C  $\leq$  Ta  $\leq$  +95 °C, VIN  $_{GOOD0}$   $\leq$  VIN  $\leq$  35 V.

Table 72. Temperature sensor specifications

No	Symbol	Parameter Conditions		Min	Тур	Max	Unit
1	T <sub>MON_RANGE</sub>	Monitoring temperature range	-	-40	-	150	ů
2	T <sub>MON_ACC</sub>	Monitoring temperature accuracy	-	-15	-	15	°C

L9680 Quality information

## 17 Quality information

### 17.1 OTP memory

The device contains a 128-bits One-Time Programmable memory. This OTP memory is used for the following purposes:

- 1. 86 bits data + 3 bits CRC for critical parameters trimming: bandgaps, oscillators, reference currents, firing currents, DC sensor and RSU interface parameters.
- 2. 18 bits data for other blocks trimming: ADC, ER Cap Measurement
- 3. 20 bits data for die and wafer traceability
- 4. 1 bit for debug purpose

User read/write access to the OTP memory via SPI is only possible during production testing and require activation of a special test mode.

During mission mode, the trimming bits are automatically read from OTP and transferred to the related circuits at each POR cycle. During this operation, actual CRC of the protected trimming data is calculated and checked against the expected CRC stored in the OTP. In case of CRC check failure the OTPCRC\_ERR flag is set in the FLTSR register.

5

DS11615 Rev 2 275/280

Errata sheet L9680

# 18 Errata sheet

Table 73. Errata sheet

#	Component Revision	Category / Function	Issue Description		
1	L9680CC	Deployment Diagnostic	The high side driver diagnostic, described in section <i>on page</i> 173, doesn't work. As consequence, the I <sub>LIM_HS_FET</sub> parameter is not tested in production.		
2	L9680CC	WSS Over current detection	The over current threshold doesn't work. The user can use the leakage to ground flag to understand if a fault condition is present. The interface is anyway protected by means of thermal protection.		
					The safing records associated with CS_RS validate and process data with matching request/response masks even if these are not coming from CS_RS frames but from frames sniffed on SAF_CSx.
3	3 L9680CC Safing engine		This may lead to issues when expansion chip is used and CS_RS frames sent on expansion are sniffed by SAF_CSx at SBC side; the SBC fails to check its own CS_RS and therefore all RSUs safing records CC with matching request/response masks of expansion RSUs safing records will be updated upon the processing of the expansion RSU SPI data.  Workaround: use two different values for WID SPI bit when		
			addressing CS_RS at SBC (ie WID=1) and expansion (WID=0) side.		



L9680 **Package information** 

#### 19 **Package information**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

#### 19.1 TQFP100 (14x14x1.4 mm exp. pad down) package information

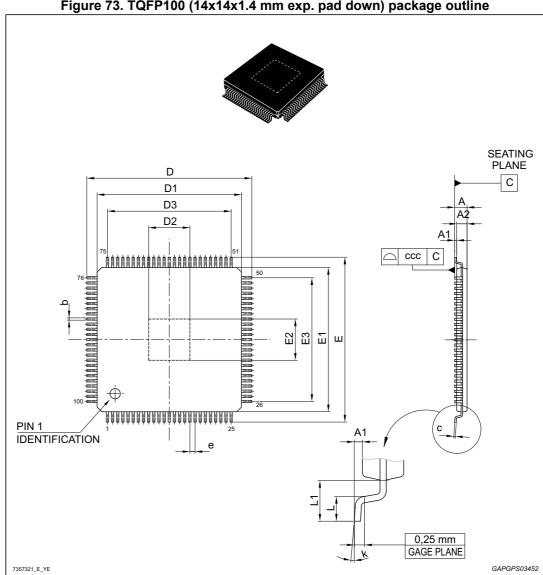


Figure 73. TQFP100 (14x14x1.4 mm exp. pad down) package outline

Package information L9680

Table 74. TQFP100 (14x14x1.4 mm exp. pad down) package mechanical data

	Dimensions								
Ref		Millimeters		Inches <sup>(1)</sup>					
	Min.	Тур.	Max.	Min.	Тур.	Max.			
А	-	-	1.20	-	-	0.0472			
A1	0.05	-	0.15	0.0020	-	0.0059			
A2	0.95	1.00	1.05	0.0374	0.0394	0.0413			
b	0.17	0.22	0.27	0.0067	0.0087	0.0106			
С	0.09	-	0.20	0.0035	-	0.0079			
D	15.80	16.00	16.20	0.6220	0.6299	0.6378			
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591			
D2 <sup>(2)</sup>	5.40	-	8.50	0.2126	-	0.3346			
D3	-	12.00	-	-	0.4724	-			
E	15.80	16.00	16.20	0.622	0.6299	0.6378			
E1	13.80	14.00	14.20	0.5433	0.5512	0.5591			
E2 <sup>(2))</sup>	5.40	-	8.50	0.2126	-	0.3346			
E3	-	12.00	-	-	0.4724	-			
е	-	0.50	-	-	0.0197	-			
L	0.45	0.60	0.75	0.0177	0.0236	0.0295			
L1	-	1.00	-	-	0.0394	-			
k	-	3.50	7.00	-	0.1378	0.2756			
ccc	-	-	0.08	-	-	0.0031			

<sup>1.</sup> Values in inches are converted from mm and rounded to 4 decimal digits.



<sup>2.</sup> The size of exposed pad is variable depending of lead frame design pad size. End user should verify "D2" and "E2" dimensions for each device application.

L9680 Revision history

# 20 Revision history

Table 75. Document revision history

Date	Revision	Changes
03-May-2016	1	Initial release.
23-Oct-2018	2	Modified in Table 2: Absolute maximum ratings the max. values for all SRx pins name from 40 V to 35 V.  Updated:  Section 5.2: Deployment drivers on page 24,  Section 6.2.5: Power-up and power-down sequences,  Section 6.10: VCOREMON external core voltage monitor'  Section 9.1.1: Functional description'  Table 25: Internal regulator DC specifications on page 232,  General conditions in Section 16.5: Oscillators on page 234,  Table 31: Reset DC specifications on page 237,  Table 34: SPI AC specifications on page 237,  Table 38: ER CAP current generators and diagnostic DC specifications on page 241,  Table 40: ER Switch DC specifications on page 242,  Table 41: SYNCBOOST converter DC specifications,  Table 47: SATBUCK converter DC specifications on page 246,,  Table 50: VCC converter DC specifications,  Table 57: Deployment drivers diagnostics - Squib resistance measurement on page 255,  General conditions in Section 16.17.2: Squib leakage test (VRCM) on page 257,  Table 61: PSI-5 satellite transceiver - DC specifications on page 259,  Table 62: PSI-5 satellite transceiver - AC specifications on page 261,  Table 63: DC Sensor interface specifications on page 269,  Table 65: DC Sensor interface specifications on page 269,  Table 67: Voltage diagnostics (Analog MUX) on page 274.  Corrected in Section 7.3.29 "register HIGH_LEV_DIAG_SEL" for "100" from "unused" to "ER cap ESR measure" and Section 7.3.31 "register HIGH_LEV_DIAG_SEL" for "100" from "unused" to "ER cap ESR measure" and Section 7.3.31 "register HIGH_LEV_DIAG_SEL" for "100" from "unused" to "ER cap ESR measure".  Updated Section 18: Errata sheet on page 276.

279/280

#### IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics - All rights reserved



Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

#### Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



**«JONHON»** (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А