

## Automotive-grade N-channel 500 V, 0.10 $\Omega$ typ., 26 A MDmesh™ DM2 Power MOSFET in a D<sup>2</sup>PAK package

Datasheet - production data

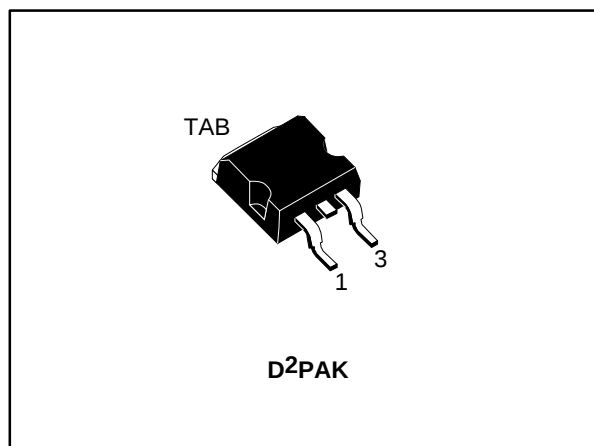
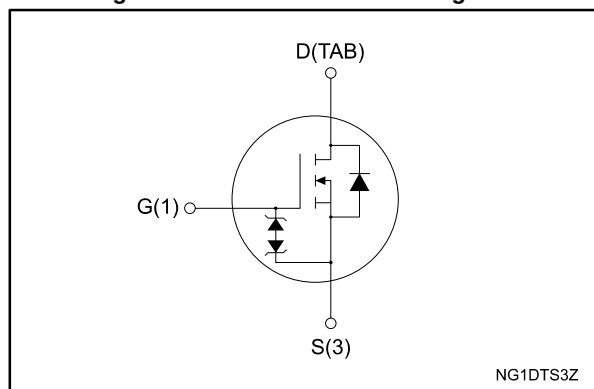


Figure 1: Internal schematic diagram



### Features

| Order code    | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> | P <sub>TOT</sub> |
|---------------|-----------------|--------------------------|----------------|------------------|
| STB34N50DM2AG | 500 V           | 0.12 $\Omega$            | 26 A           | 190 W            |

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

| Order code    | Marking  | Package            | Packing       |
|---------------|----------|--------------------|---------------|
| STB34N50DM2AG | 34N50DM2 | D <sup>2</sup> PAK | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol         | Parameter                                                              | Value      | Unit               |
|----------------|------------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                                    | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$  | 26         | A                  |
|                | Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$ | 16         |                    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                                 | 104        | A                  |
| $P_{TOT}$      | Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$           | 190        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                      | 50         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                              | 50         |                    |
| $T_{stg}$      | Storage temperature                                                    | -55 to 150 | $^{\circ}\text{C}$ |
| $T_j$          | Operating junction temperature                                         |            |                    |

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 26\text{ A}$ ,  $di/dt=800\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

(3)  $V_{DS} \leq 400\text{ V}$ .

Table 3: Thermal data

| Symbol              | Parameter                        | Value | Unit                        |
|---------------------|----------------------------------|-------|-----------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 0.65  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 30    |                             |

**Notes:**

(1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

| Symbol         | Parameter                                       | Value | Unit |
|----------------|-------------------------------------------------|-------|------|
| $I_{AR}^{(1)}$ | Avalanche current, repetitive or not repetitive | 5     | A    |
| $E_{AS}^{(2)}$ | Single pulse avalanche energy                   | 700   | mJ   |

**Notes:**

(1) pulse width limited by  $T_{jmax}$ .

(2) starting  $T_j = 25\text{ }^{\circ}\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5: Static**

| Symbol               | Parameter                         | Test conditions                                                            | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|----------------------------------------------------------------------------|------|------|------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage    | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA                               | 500  |      |      | V    |
| I <sub>DSS</sub>     | Zero gate voltage drain current   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 500 V                             |      |      | 10   | μA   |
|                      |                                   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 500 V, T <sub>case</sub> = 125 °C |      |      | 100  |      |
| I <sub>GSS</sub>     | Gate-body leakage current         | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V                             |      |      | ±5   | μA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                | 3    | 4    | 5    | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12.5 A                            |      | 0.10 | 0.12 | Ω    |

**Table 6: Dynamic**

| Symbol                              | Parameter                     | Test conditions                                                                                                                                  | Min. | Typ. | Max. | Unit |
|-------------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub>                    | Input capacitance             | V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V                                                                                        | -    | 1850 | -    | pF   |
| C <sub>oss</sub>                    | Output capacitance            |                                                                                                                                                  | -    | 100  | -    |      |
| C <sub>rss</sub>                    | Reverse transfer capacitance  |                                                                                                                                                  | -    | 2.7  | -    |      |
| C <sub>oss eq.</sub> <sup>(1)</sup> | Equivalent output capacitance | V <sub>DS</sub> = 0 to 400 V, V <sub>GS</sub> = 0 V                                                                                              | -    | 160  | -    | pF   |
| R <sub>G</sub>                      | Intrinsic gate resistance     | f = 1 MHz, I <sub>D</sub> = 0 A                                                                                                                  | -    | 4.5  | -    | Ω    |
| Q <sub>g</sub>                      | Total gate charge             | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 25 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 44   | -    | nC   |
| Q <sub>gs</sub>                     | Gate-source charge            |                                                                                                                                                  | -    | 10.5 | -    |      |
| Q <sub>gd</sub>                     | Gate-drain charge             |                                                                                                                                                  | -    | 19   | -    |      |

**Notes:**

<sup>(1)</sup> C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**Table 7: Switching times**

| Symbol              | Parameter           | Test conditions                                                                                                                                                                                                                                 | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>d(on)</sub>  | Turn-on delay time  | V <sub>DD</sub> = 250 V, I <sub>D</sub> = 12.5 A<br>R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 19.5 | -    | ns   |
| t <sub>r</sub>      | Rise time           |                                                                                                                                                                                                                                                 | -    | 11.5 | -    |      |
| t <sub>d(off)</sub> | Turn-off delay time |                                                                                                                                                                                                                                                 | -    | 65.5 | -    |      |
| t <sub>f</sub>      | Fall time           |                                                                                                                                                                                                                                                 | -    | 8.1  | -    |      |

Table 8: Source-drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                                     | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                                     | -    |      | 26   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                     | -    |      | 104  | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 26\text{ A}$                                                                                                                                                                                      | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                     | -    | 110  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                     | -    | 0.48 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                     | -    | 8.8  |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 100\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 190  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                     | -    | 1.52 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                     | -    | 16   |      | A             |

**Notes:**

<sup>(1)</sup> Pulse width is limited by safe operating area.

<sup>(2)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Table 9: Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                                            | Min.     | Typ. | Max. | Unit |
|---------------|-------------------------------|------------------------------------------------------------|----------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 250\text{ }\mu\text{A}$ , $I_D = 0\text{ A}$ | $\pm 30$ | -    | -    | V    |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

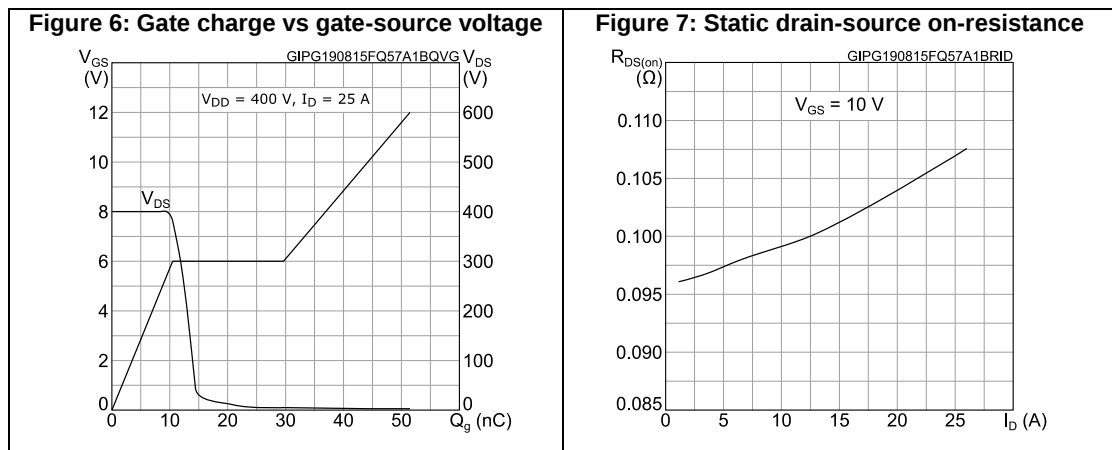
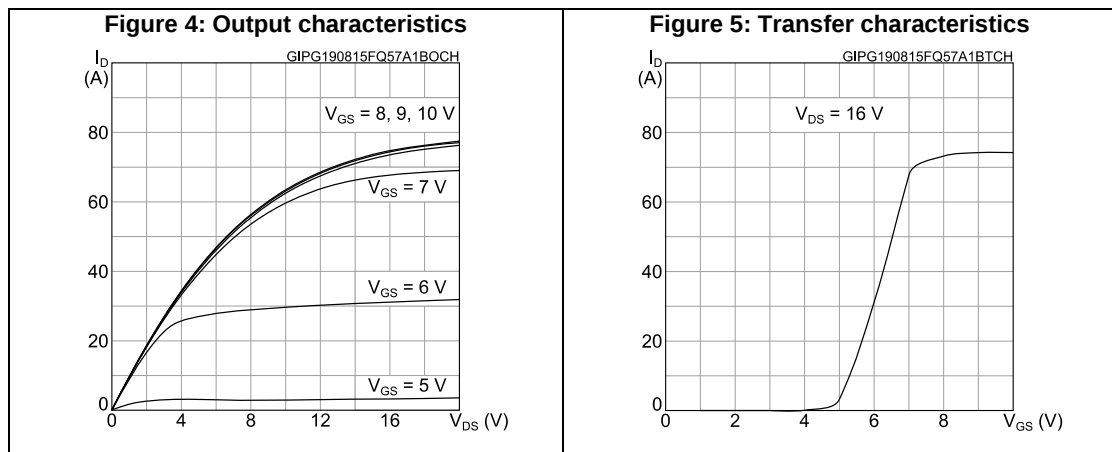
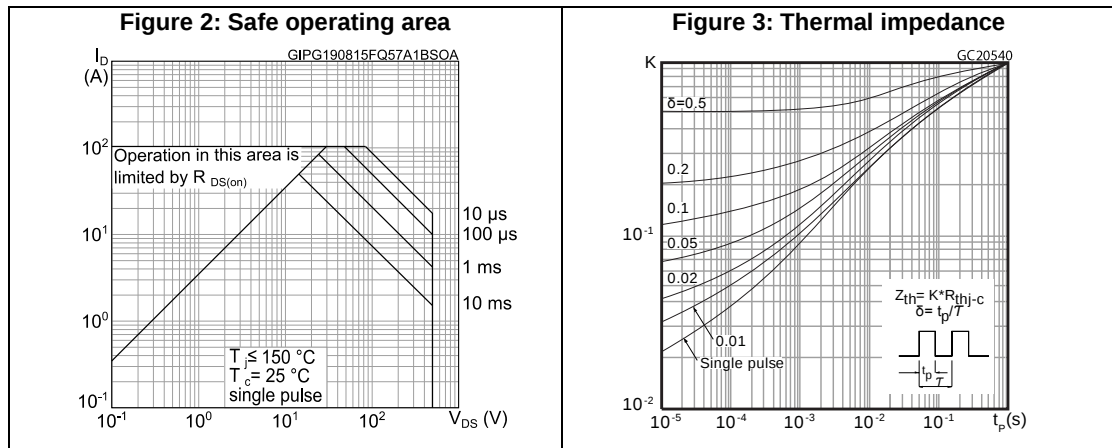


Figure 8: Capacitance variations

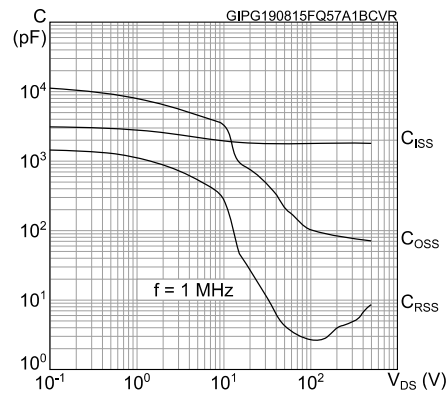


Figure 9: Normalized gate threshold voltage vs temperature

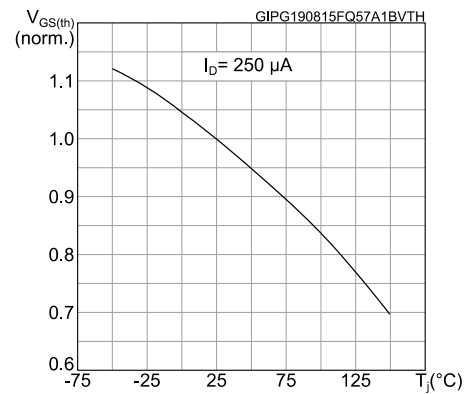


Figure 10: Normalized on-resistance vs temperature

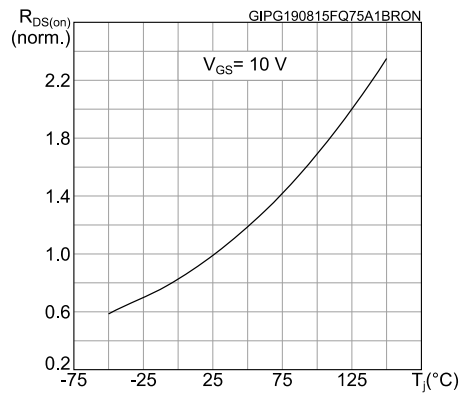


Figure 11: Normalized V(BR)DSS vs temperature

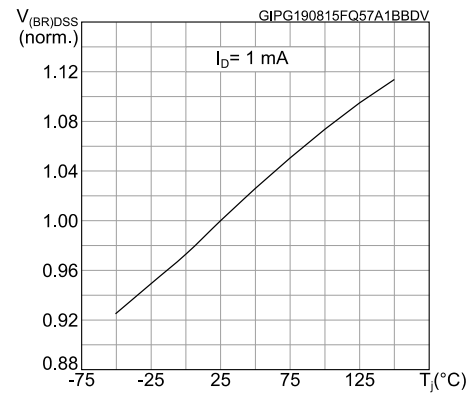


Figure 12: Output capacitance stored energy

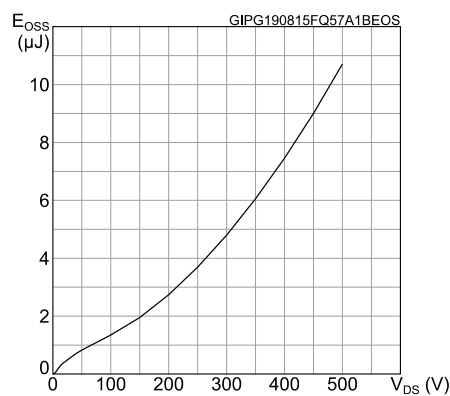
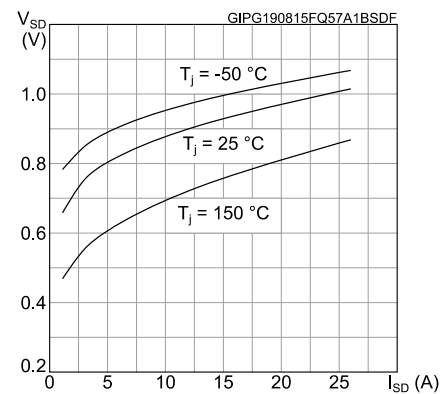


Figure 13: Source- drain diode forward characteristics



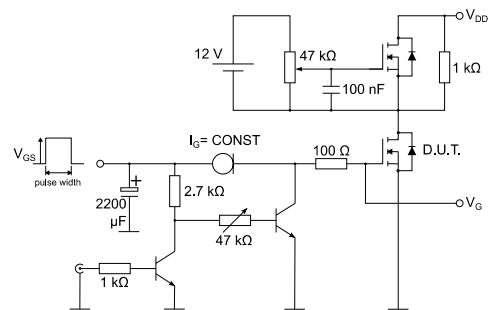
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



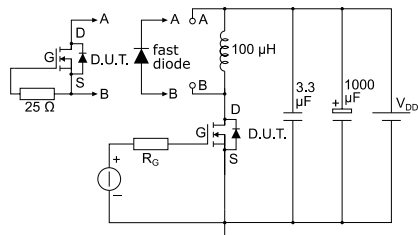
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



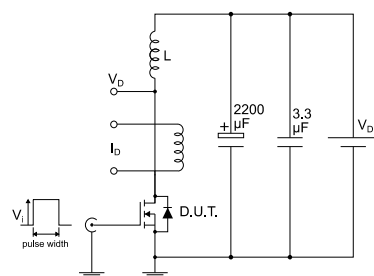
AM01469v1

**Figure 16: Test circuit for inductive load switching and diode recovery times**



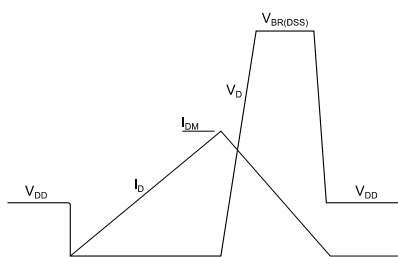
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**Figure 17: Unclamped inductive load test circuit**



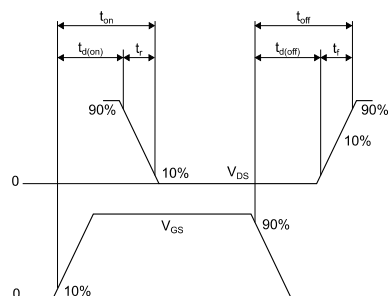
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**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



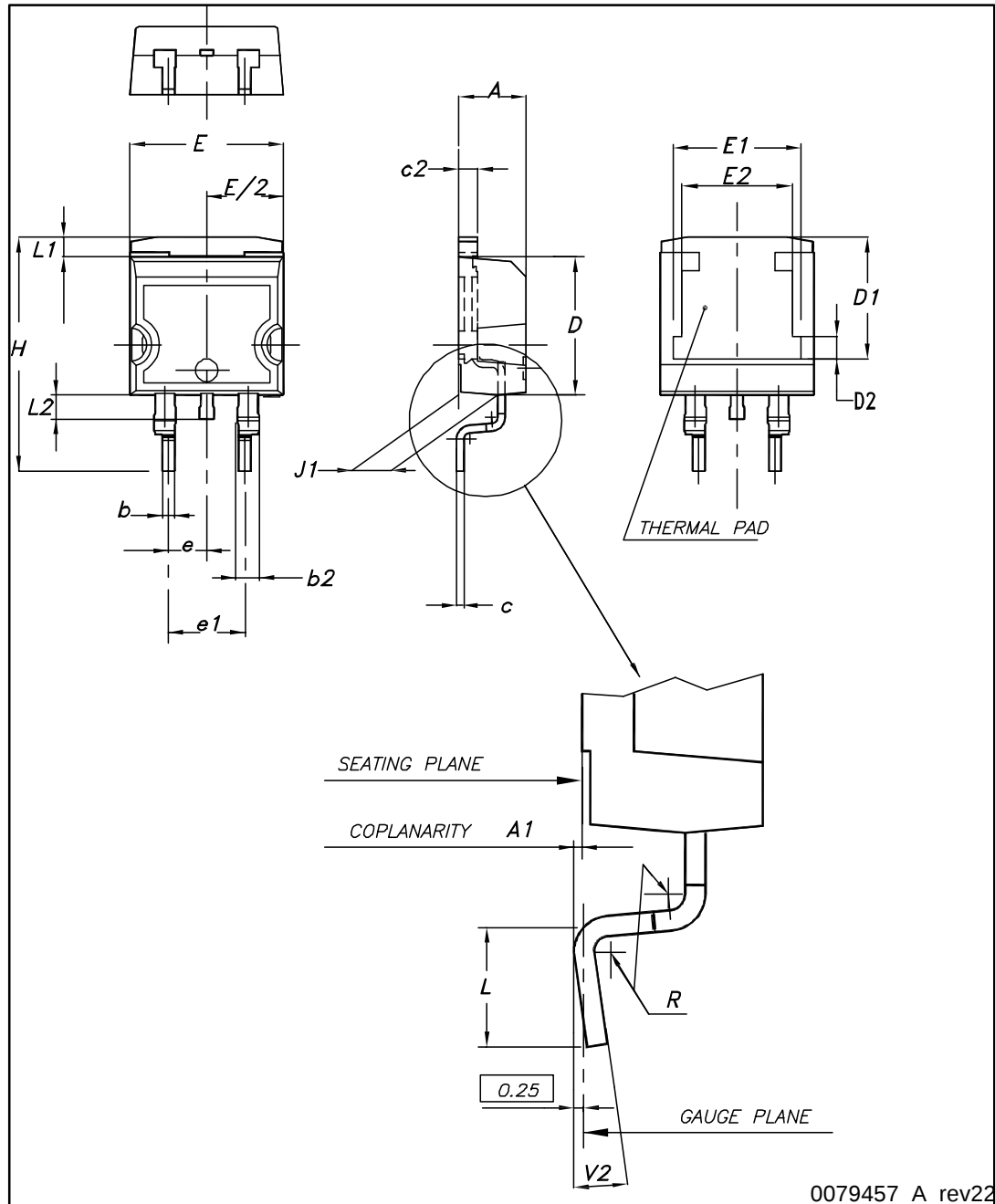
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

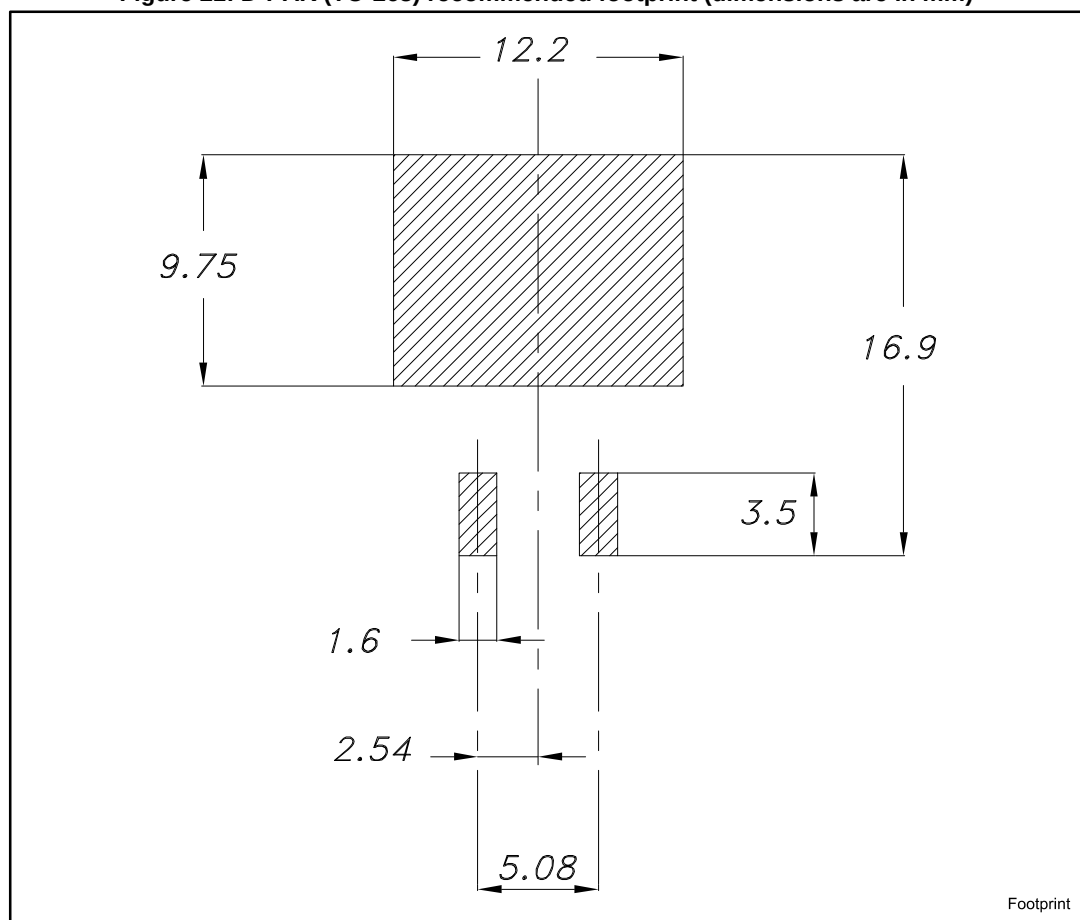
Figure 20: D<sup>2</sup>PAK (TO-263) type A package outline



0079457\_A\_rev22

Table 10: D<sup>2</sup>PAK (TO-263) type A package mechanical data

| Dim. | mm   |      |       |
|------|------|------|-------|
|      | Min. | Typ. | Max.  |
| A    | 4.40 |      | 4.60  |
| A1   | 0.03 |      | 0.23  |
| b    | 0.70 |      | 0.93  |
| b2   | 1.14 |      | 1.70  |
| c    | 0.45 |      | 0.60  |
| c2   | 1.23 |      | 1.36  |
| D    | 8.95 |      | 9.35  |
| D1   | 7.50 | 7.75 | 8.00  |
| D2   | 1.10 | 1.30 | 1.50  |
| E    | 10   |      | 10.40 |
| E1   | 8.50 | 8.70 | 8.90  |
| E2   | 6.85 | 7.05 | 7.25  |
| e    |      | 2.54 |       |
| e1   | 4.88 |      | 5.28  |
| H    | 15   |      | 15.85 |
| J1   | 2.49 |      | 2.69  |
| L    | 2.29 |      | 2.79  |
| L1   | 1.27 |      | 1.40  |
| L2   | 1.30 |      | 1.75  |
| R    |      | 0.4  |       |
| V2   | 0°   |      | 8°    |

Figure 21: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)

## 4.2 D<sup>2</sup>PAK packing information

**Figure 22: Tape**

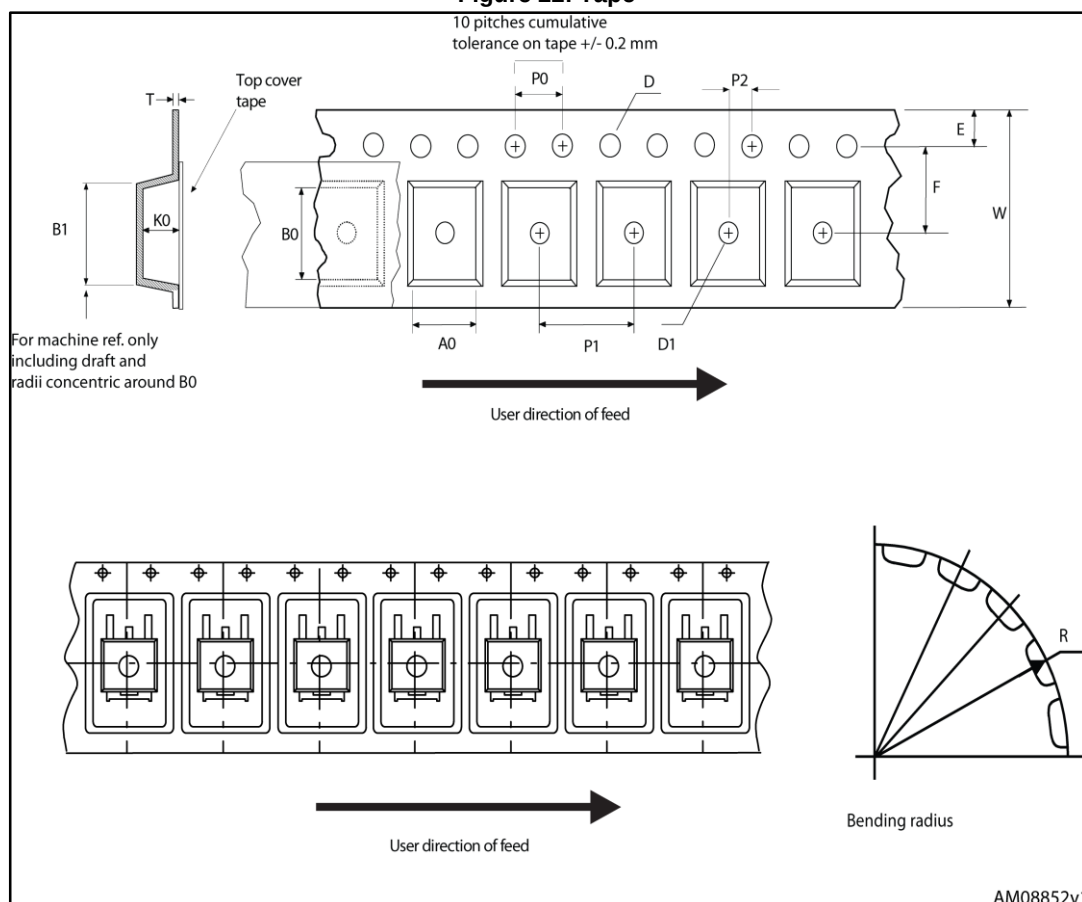
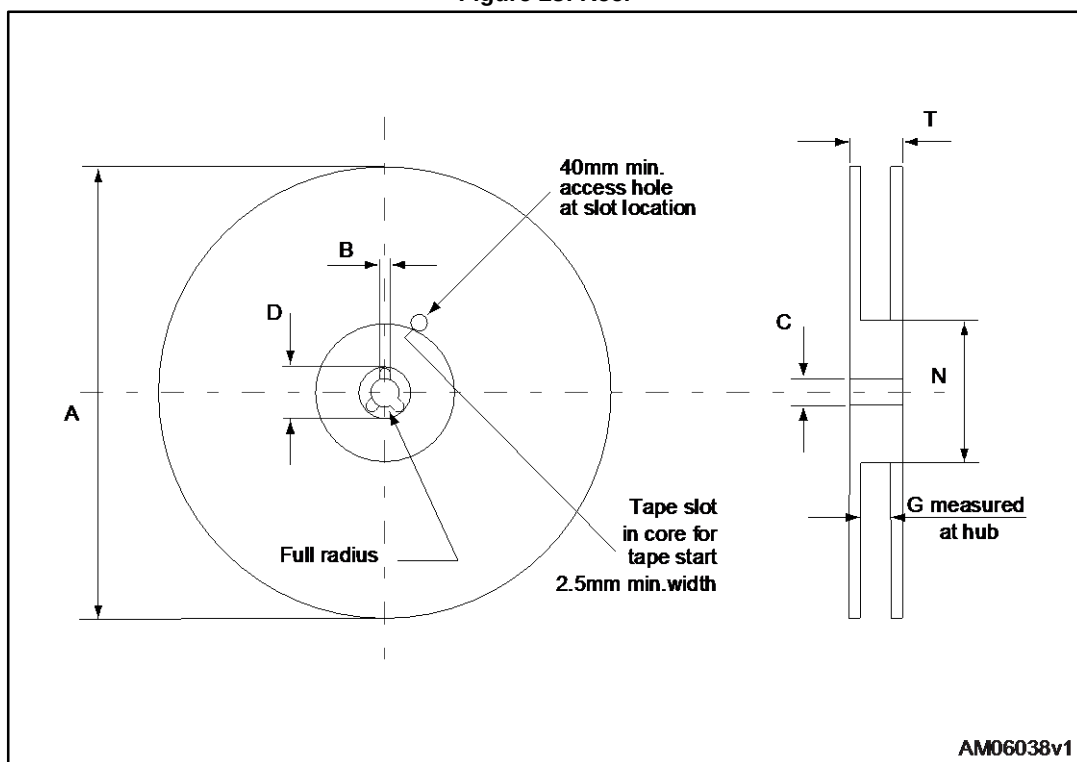


Figure 23: Reel

Table 11: D<sup>2</sup>PAK tape and reel mechanical data

| Tape |      |      | Reel     |      |      |
|------|------|------|----------|------|------|
| Dim. | mm   |      | Dim.     | mm   |      |
|      | Min. | Max. |          | Min. | Max. |
| A0   | 10.5 | 10.7 | A        |      | 330  |
| B0   | 15.7 | 15.9 | B        | 1.5  |      |
| D    | 1.5  | 1.6  | C        | 12.8 | 13.2 |
| D1   | 1.59 | 1.61 | D        | 20.2 |      |
| E    | 1.65 | 1.85 | G        | 24.4 | 26.4 |
| F    | 11.4 | 11.6 | N        | 100  |      |
| K0   | 4.8  | 5.0  | T        |      | 30.4 |
| P0   | 3.9  | 4.1  |          |      |      |
| P1   | 11.9 | 12.1 | Base qty |      | 1000 |
| P2   | 1.9  | 2.1  | Bulk qty |      | 1000 |
| R    | 50   |      |          |      |      |
| T    | 0.25 | 0.35 |          |      |      |
| W    | 23.7 | 24.3 |          |      |      |

## 5 Revision history

Table 12: Document revision history

| Date        | Revision | Changes         |
|-------------|----------|-----------------|
| 19-Aug-2015 | 1        | Initial version |

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