# PIC18F2423/2523/4423/4523
# Data Sheet

## 28/40/44-Pin, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

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# PIC18F2423/2523/4423/4523

## 28/40/44-Pin, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

### Power Management Features:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Ultra Low 50 nA Input Leakage
- Run mode Currents Down to 11 μA Typical
- Idle mode Currents Down to 2.5 μA Typical
- Sleep mode Current Down to 100 μA Typical
- Timer1 Oscillator: 900 nA, 32 kHz, 2V
- Watchdog Timer: 1.4 μA, 2V Typical
- Two-Speed Oscillator Start-up

### Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) – Available for Crystal and Internal Oscillators
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - Fast wake from Sleep and Idle, 1 μs typical
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds, from 31 kHz to 32 MHz, when used with PLL
  - User-tunable to Compensate for Frequency Drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

### Peripheral Highlights:

- 12-Bit, Up to 13-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep mode
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Three Programmable External Interrupts
- Four Input Change Interrupts
- Up to Two Capture/Compare/PWM (CCP) modules, One with Auto-Shutdown (28-pin devices)
- Enhanced Capture/Compare/PWM (ECCP) module (40/44-pin devices only):
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart

### Peripheral Highlights (Continued):

- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all four modes) and $I^2C$™ Master and Slave modes
- Enhanced USART module:
  - Support for RS-485, RS-232 and LIN/J2602
  - RS-232 operation using internal oscillator block (no external crystal required)
  - Auto-wake-up on Start bit
  - Auto-Baud Detect (ABD)

### Special Microcontroller Features:

- C Compiler Optimized Architecture: Optional Extended Instruction Set Designed to Optimize Re-Entrant Code
- 100,000 Erase/Write Cycle, Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle, Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT): Programmable Period, from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Operating Voltage Range: 2.0V to 5.5V
- Programmable, 16-Level High/Low-Voltage Detection (HLVD) module: Supports Interrupt on High/Low-Voltage Detection
- Programmable Brown-out Reset (BOR): With Software-Enable Option

**Note:** This document is supplemented by the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631). See **Section 1.0 "Device Overview"**.

| Device | Program Memory | | Data Memory | | I/O | 12-Bit A/D (ch) | CCP/ ECCP (PWM) | MSSP | | EUSART | Comp. | Timers 8/16-Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Flash (bytes) | # Single-Word Instructions | SRAM (bytes) | EEPROM (bytes) | | | | SPI | Master $I^2C$™ | | | |
| PIC18F2423 | 16K | 8192 | 768 | 256 | 25 | 10 | 2/0 | Y | Y | 1 | 2 | 1/3 |
| PIC18F2523 | 32K | 16384 | 1536 | 256 | 25 | 10 | 2/0 | Y | Y | 1 | 2 | 1/3 |
| PIC18F4423 | 16K | 8192 | 768 | 256 | 36 | 13 | 1/1 | Y | Y | 1 | 2 | 1/3 |
| PIC18F4523 | 32K | 16384 | 1536 | 256 | 36 | 13 | 1/1 | Y | Y | 1 | 2 | 1/3 |

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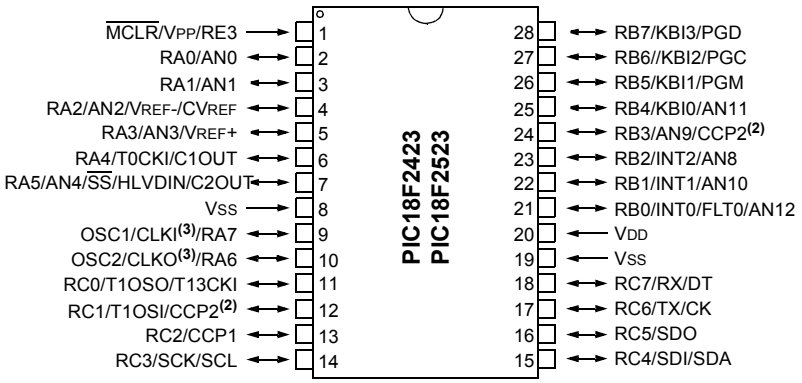
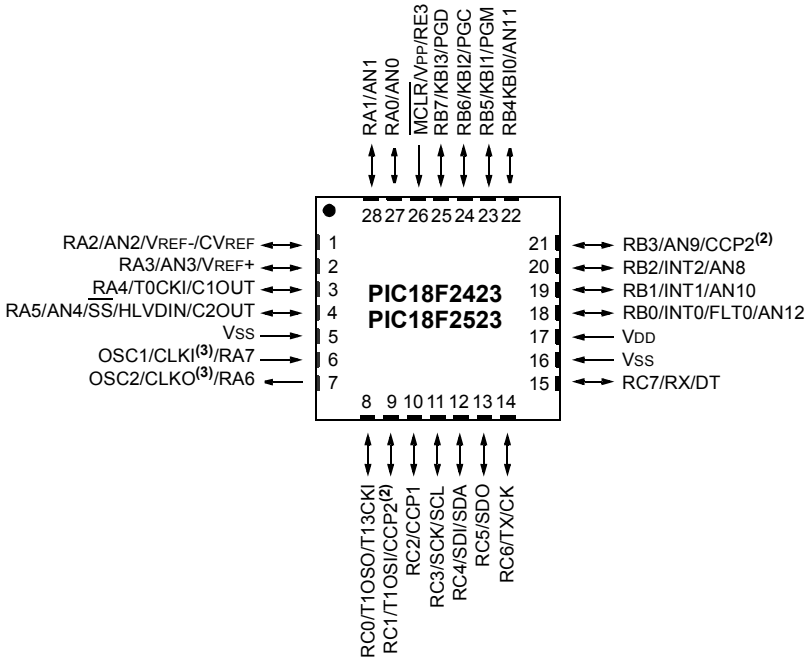
## Pin Diagrams

**28-Pin PDIP, SOIC**




**28-Pin QFN(1)**




**Note 1:** It is recommended to connect the bottom pad of QFN package parts to VSS.

**2:** RB3 is the alternate pin for CCP2 multiplexing.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).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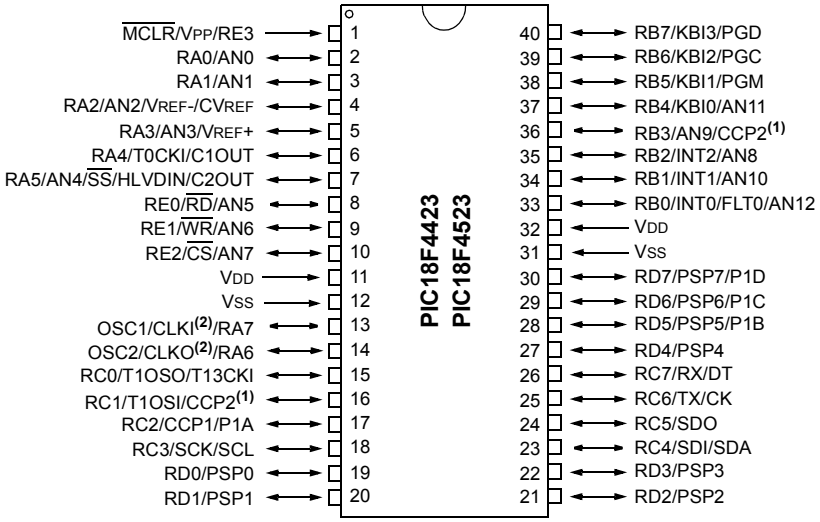
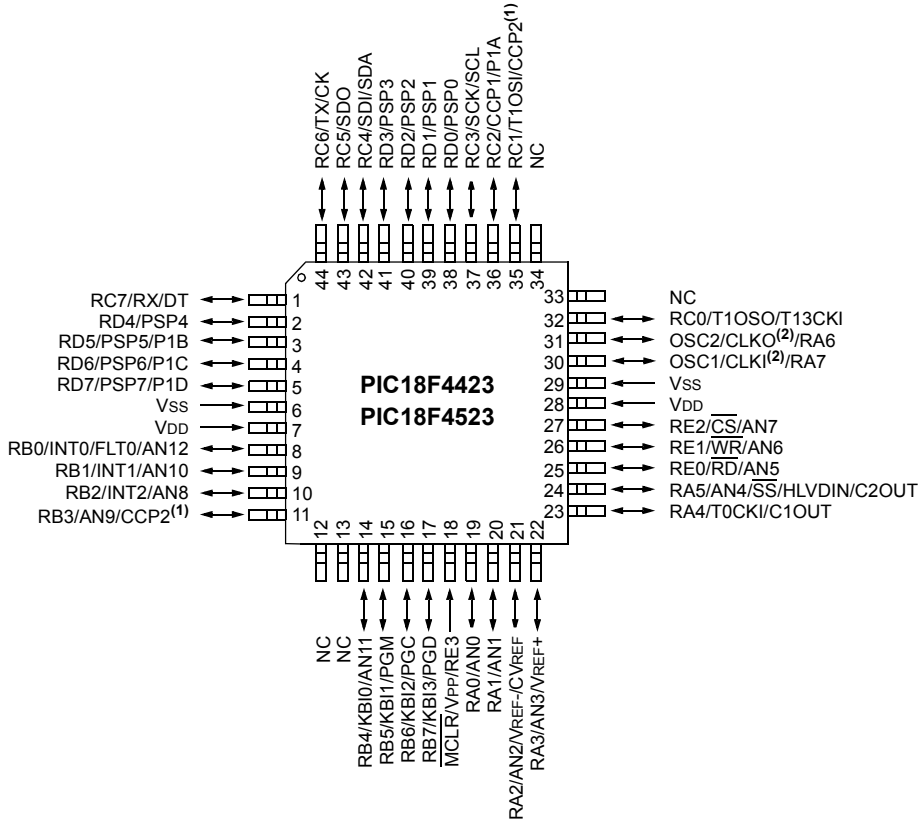
## Pin Diagrams (Continued)

**40-Pin PDIP**




**44-Pin TQFP**

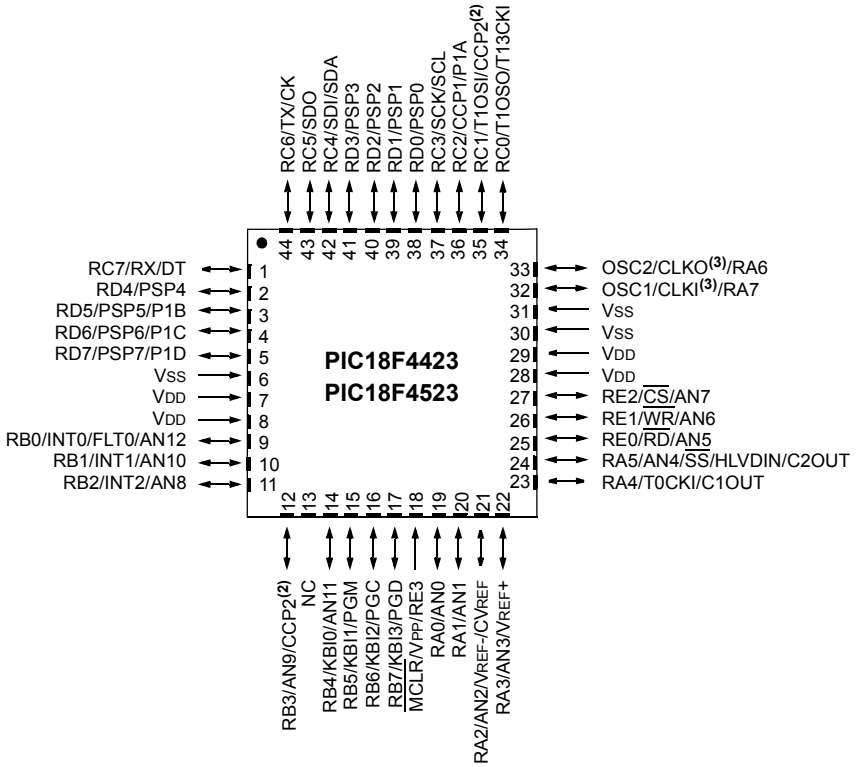



**Note 1:** RB3 is the alternate pin for CCP2 multiplexing.

**2:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

## Pin Diagrams (Continued)

**44-Pin QFN(1)**




**Note 1:** It is recommended to connect the bottom pad of QFN package parts to VSS.

**2:** RB3 is the alternate pin for CCP2 multiplexing.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).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# 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2423
- PIC18F2523
- PIC18F4423
- PIC18F4523
- PIC18LF2423
- PIC18LF2523
- PIC18LF4423
- PIC18LF4523

**Note:** This data sheet documents only the devices' features and specifications that are in addition to, or different from, the features and specifications of the PIC18F2420/2520/4420/4520 devices. For information on the features and specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. On top of these features, the PIC18F2423/2523/4423/4523 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

## 1.1 New Core Features

### 1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2423/2523/4423/4523 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller also can run with its CPU core disabled and the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 4.0 "Electrical Characteristics"** for values.

### 1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2423/2523/4423/4523 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes with the same pin options as the External Clock modes.
- An internal oscillator block that offers eight clock frequencies: an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and Internal Oscillator modes, allowing clock speeds of up to 40 MHz from the HS clock source. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz, all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** Constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** Allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

## 1.2 Other Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, thereby reducing code overhead.
- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it is possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18F2423/2523/4423/4523 family introduces an optional extension to the PIC18 instruction set that adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown, for disabling PWM outputs on interrupt or other select conditions, and auto-restart, to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **Extended Watchdog Timer (WDT):** This Enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 4.0 "Electrical Characteristics"** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F2423/2523/4423/4523 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18F2423/4423 devices – 16 Kbytes
  - PIC18F2523/4523 devices – 32 Kbytes
- A/D Channels:
  - PIC18F2423/2523 devices – 10
  - PIC18F4423/4523 devices – 13
- I/O Ports:
  - PIC18F2423/2523 devices – Three bidirectional ports
  - PIC18F4423/4523 devices – Five bidirectional ports
- CCP and Enhanced CCP Implementation:
  - PIC18F2423/2523 devices – Two standard CCP modules
  - PIC18F4423/4523 devices – One standard CCP module and one ECCP module
- Parallel Slave Port – Present only on PIC18F4423/4523 devices

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F2423/2523/4423/4523 family are available only as low-voltage devices, designated by "LF" (such as PIC18**LF**2423), and function over an extended $V_{DD}$ range of 2.0V to 5.5V.


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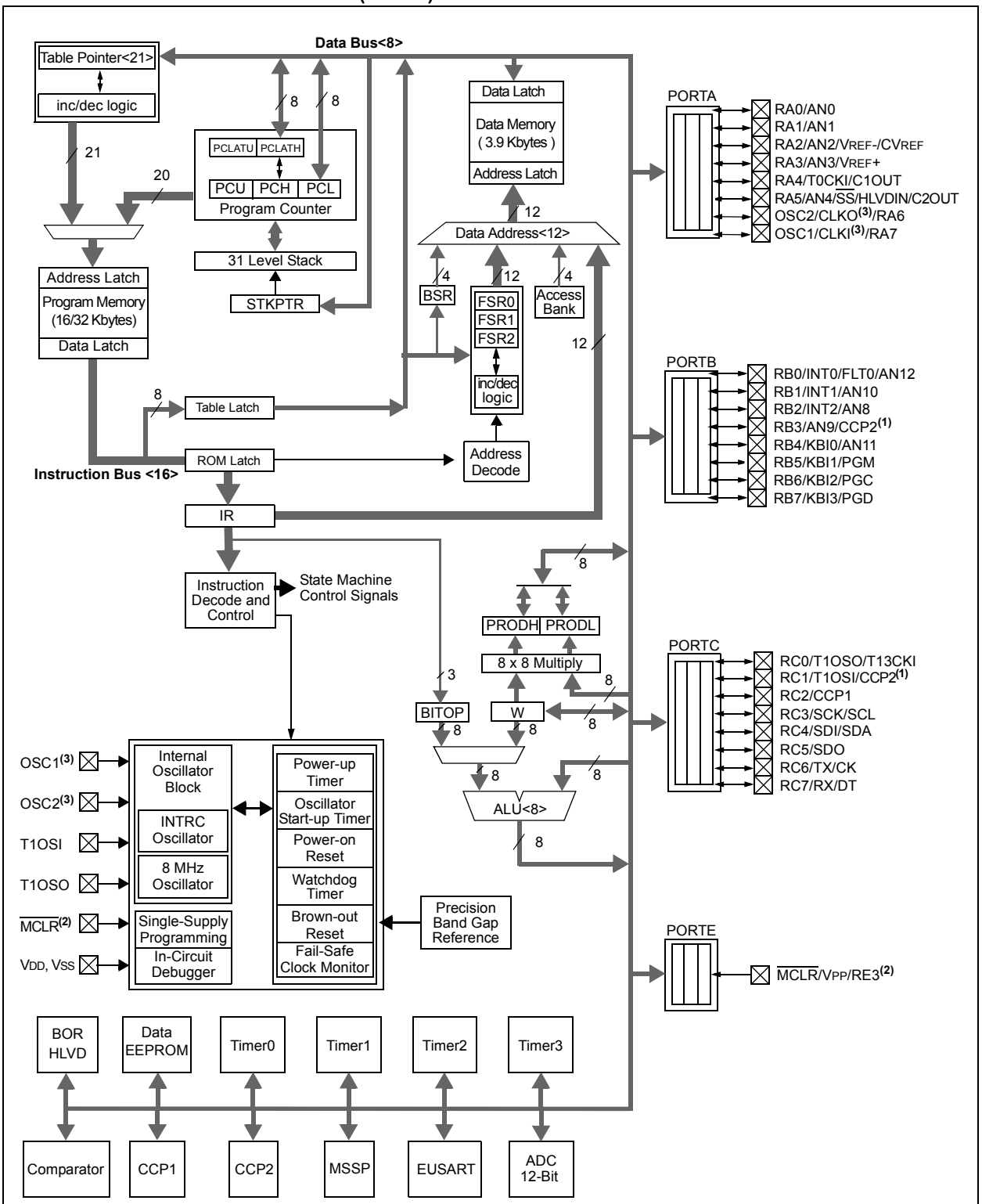
**TABLE 1-1: DEVICE FEATURES**

| Features | PIC18F2423 | PIC18F2523 | PIC18F4423 | PIC18F4523 |
|---|---|---|---|---|
| Operating Frequency | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz |
| Program Memory (Bytes) | 16,384 | 32,768 | 16,384 | 32,768 |
| Program Memory (Instructions) | 8,192 | 16,384 | 8,192 | 16,384 |
| Data Memory (Bytes) | 768 | 1,536 | 768 | 1,536 |
| Data EEPROM Memory (Bytes) | 256 | 256 | 256 | 256 |
| Interrupt Sources | 19 | 19 | 20 | 20 |
| I/O Ports | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, D, E | Ports A, B, C, D, E |
| Timers | 4 | 4 | 4 | 4 |
| Capture/Compare/PWM Modules | 2 | 2 | 1 | 1 |
| Enhanced Capture/Compare/PWM Modules | 0 | 0 | 1 | 1 |
| Serial Communications | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART |
| Parallel Communications (PSP) | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 10 Input Channels | 10 Input Channels | 13 Input Channels | 13 Input Channels |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT |
| Programmable High/Low-Voltage Detect | Yes | Yes | Yes | Yes |
| Programmable Brown-out Reset | Yes | Yes | Yes | Yes |
| Instruction Set | 75 Instructions; 83 with Extended Instruction Set enabled | 75 Instructions; 83 with Extended Instruction Set enabled | 75 Instructions; 83 with Extended Instruction Set enabled | 75 Instructions; 83 with Extended Instruction Set enabled |
| Packages | 28-Pin PDIP<br>28-Pin SOIC<br>28-Pin QFN | 28-Pin PDIP<br>28-Pin SOIC<br>28-Pin QFN | 40-Pin PDIP<br>44-Pin QFN<br>44-Pin TQFP | 40-Pin PDIP<br>44-Pin QFN<br>44-Pin TQFP |

**FIGURE 1-1: PIC18F2423/2523 (28-PIN) BLOCK DIAGRAM**




**Note 1:** CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

**2:** RE3 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).


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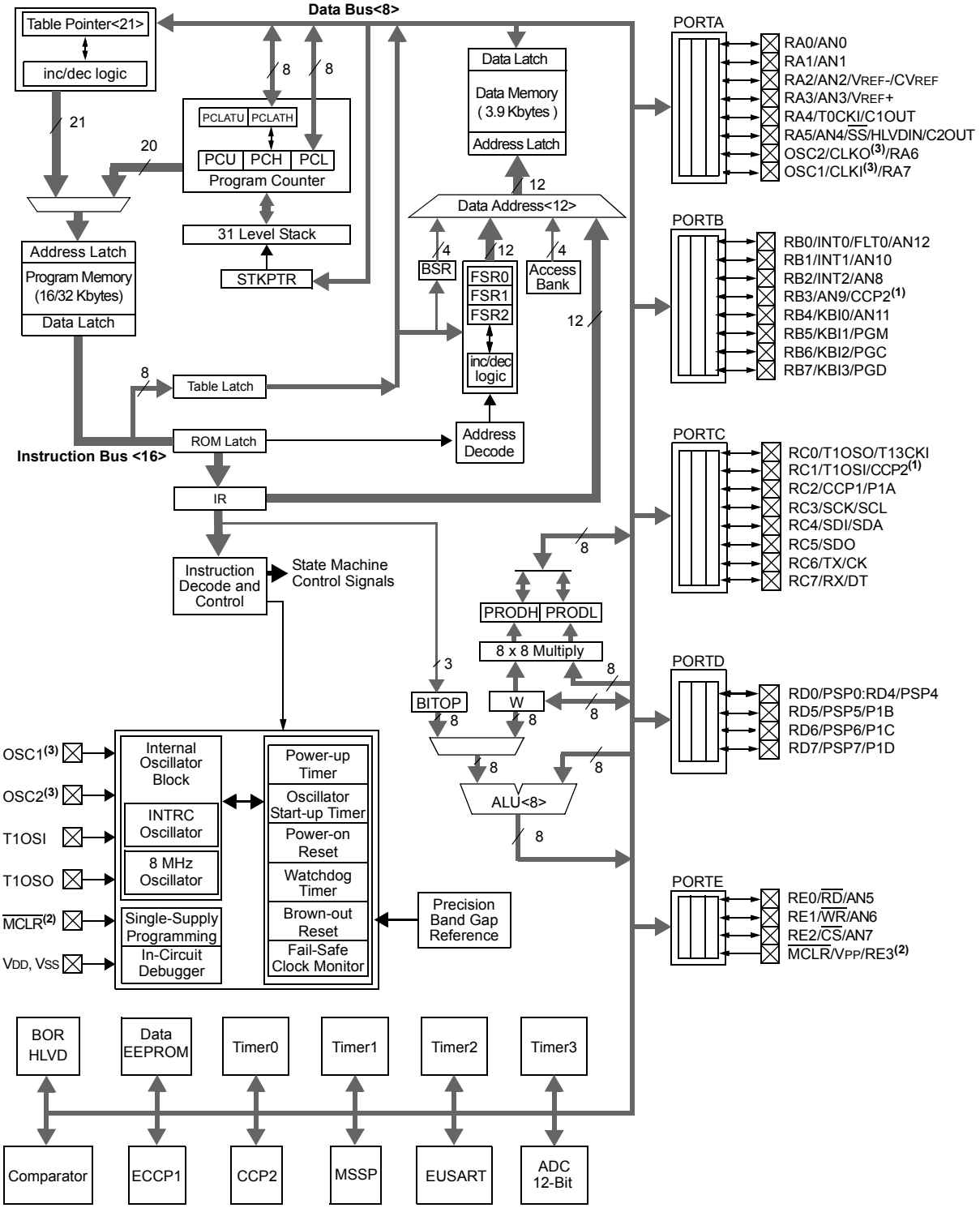
**FIGURE 1-2: PIC18F4423/4523 (40/44-PIN) BLOCK DIAGRAM**




**Note 1:** CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set or RB3 when CCP2MX is not set.

**2:** RE3 is only available when MCLR functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP, SOIC | QFN | | | |
| MCLR/VPP/RE3 | 1 | 26 | | | Master Clear (input) or programming voltage (input). |
| MCLR | | | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| VPP | | | P | | Programming voltage input. |
| RE3 | | | I | ST | Digital input. |
| OSC1/CLKI/RA7 | 9 | 6 | | | Oscillator crystal or external clock input. |
| OSC1 | | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. |
| CLKI | | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 10 | 7 | | | Oscillator crystal or clock output. |
| OSC2 | | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | | I/O | TTL | General purpose I/O pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP, SOIC | QFN | | | |
| | | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 2 | 27 | | | |
| RA0 | | | I/O | TTL | Digital I/O. |
| AN0 | | | I | Analog | Analog Input 0. |
| RA1/AN1 | 3 | 28 | | | |
| RA1 | | | I/O | TTL | Digital I/O. |
| AN1 | | | I | Analog | Analog Input 1. |
| RA2/AN2/VREF-/CVREF | 4 | 1 | | | |
| RA2 | | | I/O | TTL | Digital I/O. |
| AN2 | | | I | Analog | Analog Input 2. |
| VREF- | | | I | Analog | A/D reference voltage (low) input. |
| CVREF | | | O | Analog | Comparator reference voltage output. |
| RA3/AN3/VREF+ | 5 | 2 | | | |
| RA3 | | | I/O | TTL | Digital I/O. |
| AN3 | | | I | Analog | Analog Input 3. |
| VREF+ | | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI/C1OUT | 6 | 3 | | | |
| RA4 | | | I/O | ST | Digital I/O. |
| T0CKI | | | I | ST | Timer0 external clock input. |
| C1OUT | | | O | — | Comparator 1 output. |
| RA5/AN4/$\overline{SS}$/HLVDIN/ C2OUT | 7 | 4 | | | |
| RA5 | | | I/O | TTL | Digital I/O. |
| AN4 | | | I | Analog | Analog Input 4. |
| $\overline{SS}$ | | | I | TTL | SPI slave select input. |
| HLVDIN | | | I | Analog | High/Low-Voltage Detect input. |
| C2OUT | | | O | — | Comparator 2 output. |
| RA6 | | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP, SOIC | QFN | | | |
| | | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0/AN12 | 21 | 18 | | | |
| RB0 | | | I/O | TTL | Digital I/O. |
| INT0 | | | I | ST | External Interrupt 0. |
| FLT0 | | | I | ST | PWM Fault input for CCP1. |
| AN12 | | | I | Analog | Analog Input 12. |
| RB1/INT1/AN10 | 22 | 19 | | | |
| RB1 | | | I/O | TTL | Digital I/O. |
| INT1 | | | I | ST | External Interrupt 1. |
| AN10 | | | I | Analog | Analog Input 10. |
| RB2/INT2/AN8 | 23 | 20 | | | |
| RB2 | | | I/O | TTL | Digital I/O. |
| INT2 | | | I | ST | External Interrupt 2. |
| AN8 | | | I | Analog | Analog Input 8. |
| RB3/AN9/CCP2 | 24 | 21 | | | |
| RB3 | | | I/O | TTL | Digital I/O. |
| AN9 | | | I | Analog | Analog Input 9. |
| CCP2(1) | | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| RB4/KBI0/AN11 | 25 | 22 | | | |
| RB4 | | | I/O | TTL | Digital I/O. |
| KBI0 | | | I | TTL | Interrupt-on-change pin. |
| AN11 | | | I | Analog | Analog Input 11. |
| RB5/KBI1/PGM | 26 | 23 | | | |
| RB5 | | | I/O | TTL | Digital I/O. |
| KBI1 | | | I | TTL | Interrupt-on-change pin. |
| PGM | | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 27 | 24 | | | |
| RB6 | | | I/O | TTL | Digital I/O. |
| KBI2 | | | I | TTL | Interrupt-on-change pin. |
| PGC | | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 28 | 25 | | | |
| RB7 | | | I/O | TTL | Digital I/O. |
| KBI3 | | | I | TTL | Interrupt-on-change pin. |
| PGD | | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-2: PIC18F2423/2523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP, SOIC | QFN | | | |
| | | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 11 | 8 | | | |
| RC0 | | | I/O | ST | Digital I/O. |
| T1OSO | | | O | — | Timer1 oscillator output. |
| T13CKI | | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/CCP2 | 12 | 9 | | | |
| RC1 | | | I/O | ST | Digital I/O. |
| T1OSI | | | I | Analog | Timer1 oscillator input. |
| CCP2(2) | | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| RC2/CCP1 | 13 | 10 | | | |
| RC2 | | | I/O | ST | Digital I/O. |
| CCP1 | | | I/O | ST | Capture 1 input/Compare 1 output/PWM1 output. |
| RC3/SCK/SCL | 14 | 11 | | | |
| RC3 | | | I/O | ST | Digital I/O. |
| SCK | | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | | I/O | $I^2C$ | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI/SDA | 15 | 12 | | | |
| RC4 | | | I/O | ST | Digital I/O. |
| SDI | | | I | ST | SPI data in. |
| SDA | | | I/O | $I^2C$ | $I^2C$ data I/O. |
| RC5/SDO | 16 | 13 | | | |
| RC5 | | | I/O | ST | Digital I/O. |
| SDO | | | O | — | SPI data out. |
| RC6/TX/CK | 17 | 14 | | | |
| RC6 | | | I/O | ST | Digital I/O. |
| TX | | | O | — | EUSART asynchronous transmit. |
| CK | | | I/O | ST | EUSART synchronous clock (see related RX/DT). |
| RC7/RX/DT | 18 | 15 | | | |
| RC7 | | | I/O | ST | Digital I/O. |
| RX | | | I | ST | EUSART asynchronous receive. |
| DT | | | I/O | ST | EUSART synchronous data (see related TX/CK). |
| RE3 | — | — | — | — | See $\overline{MCLR}$/VPP/RE3 pin. |
| VSS | 8, 19 | 5, 16 | P | — | Ground reference for logic and I/O pins. |
| VDD | 20 | 17 | P | — | Positive supply for logic and I/O pins. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| $\overline{MCLR}$/VPP/RE3 | 1 | 18 | 18 | | | Master Clear (input) or programming voltage (input). |
| $\overline{MCLR}$ | | | | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| VPP | | | | P | | Programming voltage input. |
| RE3 | | | | I | ST | Digital input. |
| OSC1/CLKI/RA7 | 13 | 32 | 30 | | | Oscillator crystal or external clock input. |
| OSC1 | | | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; analog otherwise. |
| CLKI | | | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 14 | 33 | 31 | | | Oscillator crystal or clock output. |
| OSC2 | | | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | | | I/O | TTL | General purpose I/O pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 2 | 19 | 19 | | | |
| RA0 | | | | I/O | TTL | Digital I/O. |
| AN0 | | | | I | Analog | Analog Input 0. |
| RA1/AN1 | 3 | 20 | 20 | | | |
| RA1 | | | | I/O | TTL | Digital I/O. |
| AN1 | | | | I | Analog | Analog Input 1. |
| RA2/AN2/VREF-/CVREF | 4 | 21 | 21 | | | |
| RA2 | | | | I/O | TTL | Digital I/O. |
| AN2 | | | | I | Analog | Analog Input 2. |
| VREF- | | | | I | Analog | A/D reference voltage (low) input. |
| CVREF | | | | O | Analog | Comparator reference voltage output. |
| RA3/AN3/VREF+ | 5 | 22 | 22 | | | |
| RA3 | | | | I/O | TTL | Digital I/O. |
| AN3 | | | | I | Analog | Analog Input 3. |
| VREF+ | | | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI/C1OUT | 6 | 23 | 23 | | | |
| RA4 | | | | I/O | ST | Digital I/O. |
| T0CKI | | | | I | ST | Timer0 external clock input. |
| C1OUT | | | | O | — | Comparator 1 output. |
| RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT | 7 | 24 | 24 | | | |
| RA5 | | | | I/O | TTL | Digital I/O. |
| AN4 | | | | I | Analog | Analog Input 4. |
| $\overline{SS}$ | | | | I | TTL | SPI slave select input. |
| HLVDIN | | | | I | Analog | High/Low-Voltage Detect input. |
| C2OUT | | | | O | — | Comparator 2 output. |
| RA6 | | | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0/AN12 | 33 | 9 | 8 | | | |
| RB0 | | | | I/O | TTL | Digital I/O. |
| INT0 | | | | I | ST | External Interrupt 0. |
| FLT0 | | | | I | ST | PWM Fault input for Enhanced CCP1. |
| AN12 | | | | I | Analog | Analog Input 12. |
| RB1/INT1/AN10 | 34 | 10 | 9 | | | |
| RB1 | | | | I/O | TTL | Digital I/O. |
| INT1 | | | | I | ST | External Interrupt 1. |
| AN10 | | | | I | Analog | Analog Input 10. |
| RB2/INT2/AN8 | 35 | 11 | 10 | | | |
| RB2 | | | | I/O | TTL | Digital I/O. |
| INT2 | | | | I | ST | External Interrupt 2. |
| AN8 | | | | I | Analog | Analog Input 8. |
| RB3/AN9/CCP2 | 36 | 12 | 11 | | | |
| RB3 | | | | I/O | TTL | Digital I/O. |
| AN9 | | | | I | Analog | Analog Input 9. |
| CCP2(1) | | | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| RB4/KBI0/AN11 | 37 | 14 | 14 | | | |
| RB4 | | | | I/O | TTL | Digital I/O. |
| KBI0 | | | | I | TTL | Interrupt-on-change pin. |
| AN11 | | | | I | Analog | Analog Input 11. |
| RB5/KBI1/PGM | 38 | 15 | 15 | | | |
| RB5 | | | | I/O | TTL | Digital I/O. |
| KBI1 | | | | I | TTL | Interrupt-on-change pin. |
| PGM | | | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 39 | 16 | 16 | | | |
| RB6 | | | | I/O | TTL | Digital I/O. |
| KBI2 | | | | I | TTL | Interrupt-on-change pin. |
| PGC | | | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 40 | 17 | 17 | | | |
| RB7 | | | | I/O | TTL | Digital I/O. |
| KBI3 | | | | I | TTL | Interrupt-on-change pin. |
| PGD | | | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 15 | 34 | 32 | | | |
| RC0 | | | | I/O | ST | Digital I/O. |
| T1OSO | | | | O | — | Timer1 oscillator output. |
| T13CKI | | | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/CCP2 | 16 | 35 | 35 | | | |
| RC1 | | | | I/O | ST | Digital I/O. |
| T1OSI | | | | I | CMOS | Timer1 oscillator input. |
| CCP2(2) | | | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| RC2/CCP1/P1A | 17 | 36 | 36 | | | |
| RC2 | | | | I/O | ST | Digital I/O. |
| CCP1 | | | | I/O | ST | Capture 1 input/Compare 1 output/PWM1 output. |
| P1A | | | | O | — | Enhanced CCP1 output. |
| RC3/SCK/SCL | 18 | 37 | 37 | | | |
| RC3 | | | | I/O | ST | Digital I/O. |
| SCK | | | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | | | I/O | $I^2C$ | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI/SDA | 23 | 42 | 42 | | | |
| RC4 | | | | I/O | ST | Digital I/O. |
| SDI | | | | I | ST | SPI data in. |
| SDA | | | | I/O | $I^2C$ | $I^2C$ data I/O. |
| RC5/SDO | 24 | 43 | 43 | | | |
| RC5 | | | | I/O | ST | Digital I/O. |
| SDO | | | | O | — | SPI data out. |
| RC6/TX/CK | 25 | 44 | 44 | | | |
| RC6 | | | | I/O | ST | Digital I/O. |
| TX | | | | O | — | EUSART asynchronous transmit. |
| CK | | | | I/O | ST | EUSART synchronous clock (see related RX/DT). |
| RC7/RX/DT | 26 | 1 | 1 | | | |
| RC7 | | | | I/O | ST | Digital I/O. |
| RX | | | | I | ST | EUSART asynchronous receive. |
| DT | | | | I/O | ST | EUSART synchronous data (see related TX/CK). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled. |
| RD0/PSP0 | 19 | 38 | 38 | | | |
| RD0 | | | | I/O | ST | Digital I/O. |
| PSP0 | | | | I/O | TTL | Parallel Slave Port data. |
| RD1/PSP1 | 20 | 39 | 39 | | | |
| RD1 | | | | I/O | ST | Digital I/O. |
| PSP1 | | | | I/O | TTL | Parallel Slave Port data. |
| RD2/PSP2 | 21 | 40 | 40 | | | |
| RD2 | | | | I/O | ST | Digital I/O. |
| PSP2 | | | | I/O | TTL | Parallel Slave Port data. |
| RD3/PSP3 | 22 | 41 | 41 | | | |
| RD3 | | | | I/O | ST | Digital I/O. |
| PSP3 | | | | I/O | TTL | Parallel Slave Port data. |
| RD4/PSP4 | 27 | 2 | 2 | | | |
| RD4 | | | | I/O | ST | Digital I/O. |
| PSP4 | | | | I/O | TTL | Parallel Slave Port data. |
| RD5/PSP5/P1B | 28 | 3 | 3 | | | |
| RD5 | | | | I/O | ST | Digital I/O. |
| PSP5 | | | | I/O | TTL | Parallel Slave Port data. |
| P1B | | | | O | — | Enhanced CCP1 output. |
| RD6/PSP6/P1C | 29 | 4 | 4 | | | |
| RD6 | | | | I/O | ST | Digital I/O. |
| PSP6 | | | | I/O | TTL | Parallel Slave Port data. |
| P1C | | | | O | — | Enhanced CCP1 output. |
| RD7/PSP7/P1D | 30 | 5 | 5 | | | |
| RD7 | | | | I/O | ST | Digital I/O. |
| PSP7 | | | | I/O | TTL | Parallel Slave Port data. |
| P1D | | | | O | — | Enhanced CCP1 output. |

**Legend:** TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
$I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-3: PIC18F4423/4523 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTE is a bidirectional I/O port. |
| RE0/$\overline{RD}$/AN5 | 8 | 25 | 25 | | | |
| RE0 | | | | I/O | ST | Digital I/O. |
| $\overline{RD}$ | | | | I | TTL | Read control for Parallel Slave Port (see also $\overline{WR}$ and $\overline{CS}$ pins). |
| AN5 | | | | I | Analog | Analog Input 5. |
| RE1/$\overline{WR}$/AN6 | 9 | 26 | 26 | | | |
| RE1 | | | | I/O | ST | Digital I/O. |
| $\overline{WR}$ | | | | I | TTL | Write control for Parallel Slave Port (see $\overline{CS}$ and $\overline{RD}$ pins). |
| AN6 | | | | I | Analog | Analog Input 6. |
| RE2/$\overline{CS}$/AN7 | 10 | 27 | 27 | | | |
| RE2 | | | | I/O | ST | Digital I/O. |
| $\overline{CS}$ | | | | I | TTL | Chip select control for Parallel Slave Port (see related $\overline{RD}$ and $\overline{WR}$). |
| AN7 | | | | I | Analog | Analog Input 7. |
| RE3 | — | — | — | — | — | See $\overline{MCLR}$/VPP/RE3 pin. |
| VSS | 12, 31 | 6, 30, 31 | 6, 29 | P | — | Ground reference for logic and I/O pins. |
| VDD | 11, 32 | 7, 8, 28, 29 | 7, 28 | P | — | Positive supply for logic and I/O pins. |
| NC | — | 13 | 12, 13, 33, 34 | — | — | No connect. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

**NOTES:**


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## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the PIC18F2423/2523 devices and 13 for the PIC18F4423/4523 devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

Of the ADCONx registers:

- ADCON0 (shown in Register 2-1) – Controls the module's operation
- ADCON1 (Register 2-2) – Configures the functions of the port pins
- ADCON2 (Register 2-3) – Configures the A/D clock source, programmed acquisition time and justification

**REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)**(1,2)**
0110 = Channel 6 (AN6)**(1,2)**
0111 = Channel 7 (AN7)**(1,2)**
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented**(2)**
1110 = Unimplemented**(2)**
1111 = Unimplemented**(2)**

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on PIC18F2423/2523 devices.
**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

**REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0(1) | R/W(1) | R/W(1) | R/W(1) |
|---|---|---|---|---|---|---|---|
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit ($V_{REF-}$ source)
1 = $V_{REF-}$ (AN2)
0 = $V_{SS}$

bit 4 **VCFG0:** Voltage Reference Configuration bit ($V_{REF+}$ source)
1 = $V_{REF+}$ (AN3)
0 = $V_{DD}$

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

| PCFG<3:0> | AN12 | AN11 | AN10 | AN9 | AN8 | AN7(2) | AN6(2) | AN5(2) | AN4 | AN3 | AN2 | AN1 | AN0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000(1) | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111(1) | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input D = Digital I/O

**Note 1:** The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

**2:** AN5 through AN7 are only available on PIC18F4423/4523 devices.


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**REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage ($V_{DD}$ and $V_{SS}$), or the voltage level on the RA3/AN3/$V_{REF}$+ and RA2/AN2/$V_{REF}$-/C$V_{REF}$ pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

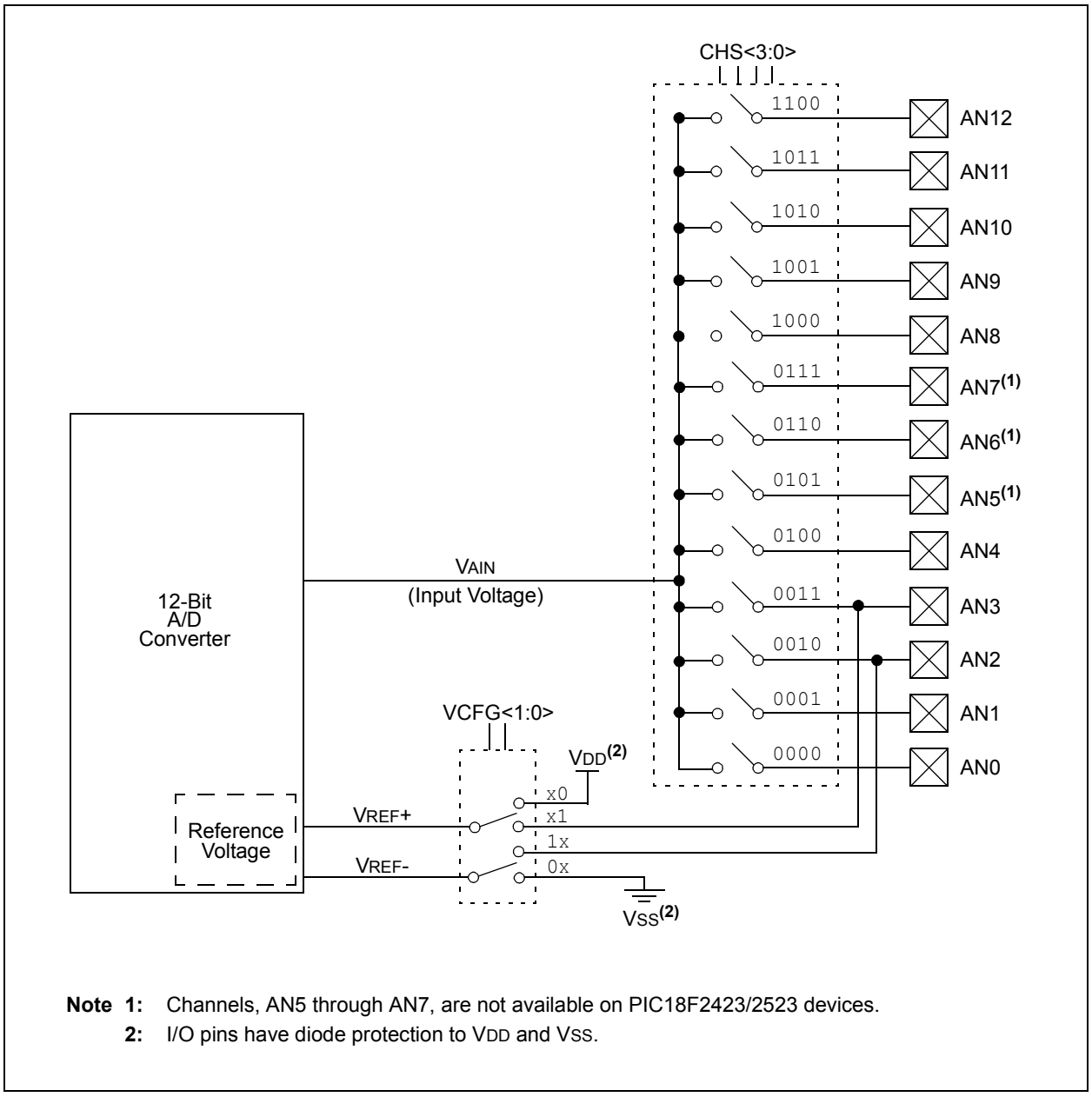
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**




**Note 1:** Channels, AN5 through AN7, are not available on PIC18F2423/2523 devices.

**2:** I/O pins have diode protection to $V_{DD}$ and $V_{SS}$.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The value in the ADRESH:ADRESL registers is unknown following POR and BOR Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**.

After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/$\overline{\text{DONE}}$ bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on the A/D module (ADCON0)
2. Configure the A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>).
5. Wait for the A/D conversion to complete by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read the A/D Result registers (ADRESH:ADRESL) and clear the ADIF bit, if required.
7. For the next conversion, go to step 1 or step 2, as required.

   The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**

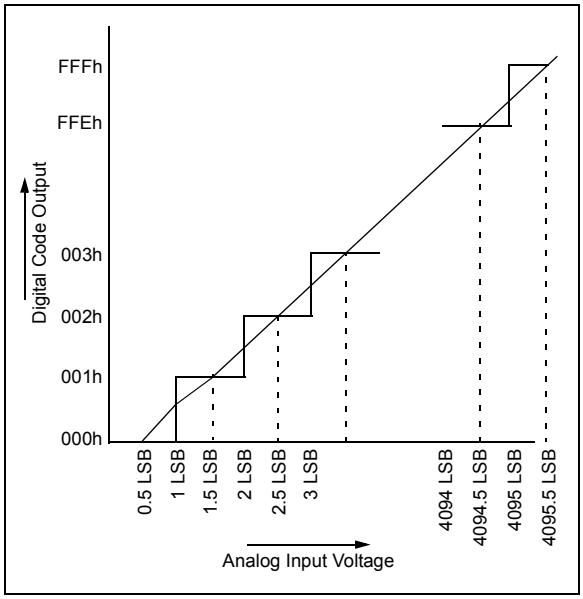
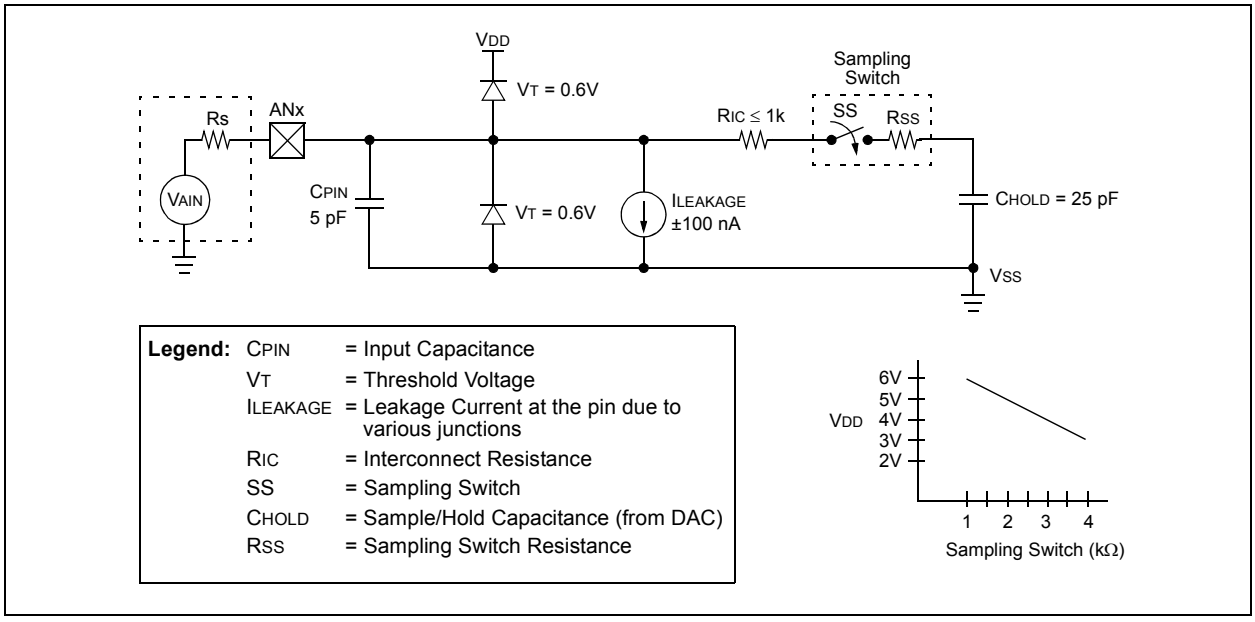



**FIGURE 2-3: ANALOG INPUT MODEL**



## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3.

The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.**

After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |
|---|---|

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the application system assumptions shown in Table 2-1:

**TABLE 2-1: TACQ ASSUMPTIONS**

| | | |
|---|---|---|
| CHOLD | = | 25 pF |
| Rs | = | 2.5 kΩ |
| Conversion Error | ≤ | 1/2 LSb |
| VDD | = | 3V → Rss = 4 kΩ |
| Temperature | = | 85°C (system maximum) |

**EQUATION 2-1: ACQUISITION TIME**

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

**EQUATION 2-2: A/D MINIMUM CHARGING TIME**

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \bullet (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ln(1/4096)$$

**EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME**

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$
$$T_{AMP} = 0.2\ \mu s$$
$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF}$ = 0 ms.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ln(1/4095)\ \mu s$$
$$-(25\ pF)(1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega)\ln(0.0004883)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$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## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option of having an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition time is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see parameter 130 on page 41.)

Table 2-2 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-2: TAD vs. DEVICE OPERATING FREQUENCIES**

| A/D Clock Source (TAD) | | Assumes TAD Min. = 0.8 μs |
|---|---|---|
| **Operation** | **ADCS<2:0>** | **Maximum FOSC** |
| 2 TOSC | 000 | 2.50 MHz |
| 4 TOSC | 100 | 5.00 MHz |
| 8 TOSC | 001 | 10.00 MHz |
| 16 TOSC | 101 | 20.00 MHz |
| 32 TOSC | 010 | 40.00 MHz |
| 64 TOSC | 110 | 40.00 MHz |
| RC(2) | x11 | 1.00 MHz(1) |

**Note 1:** The RC source has a typical TAD time of 2.5 μs.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT<2:0> bits do not need to be adjusted as the ADCS<2:0> bits adjust the TAD time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

| | |
|---|---|
| **Note 1:** | When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted. |
| **2:** | Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits. |
| **3:** | The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG<3:0> bits in ADCON1 are reset. |


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## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT<2:0> bits have been set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TCY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

| **Note:** | The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 3 TAD after enabling the A/D before beginning an acquisition and conversion cycle. |
|---|---|

## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity-gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**

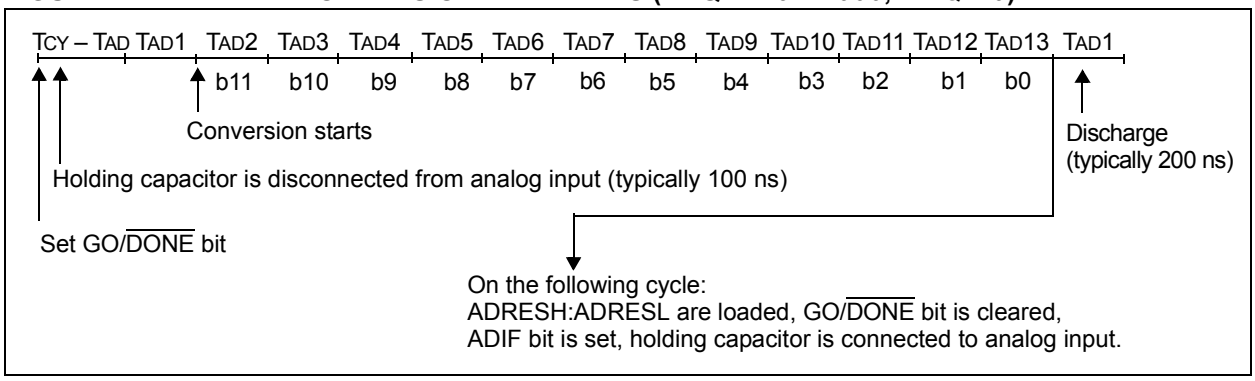
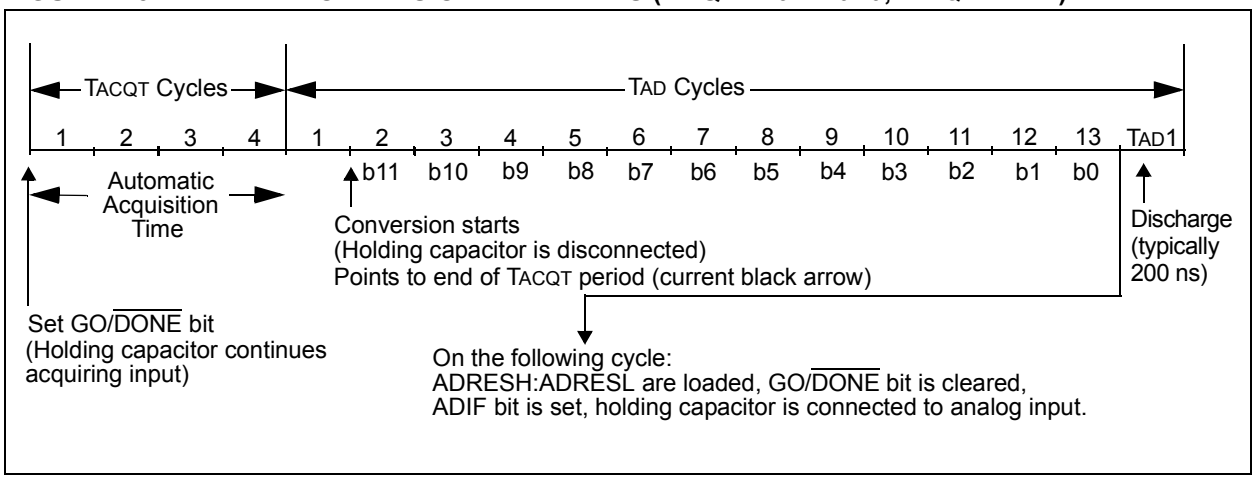



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



## 2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-3: REGISTERS ASSOCIATED WITH A/D OPERATION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset Values on page |
|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF | **(Note 4)** |
| PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | **(Note 4)** |
| PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | **(Note 4)** |
| IPR1 | PSPIP(1) | ADIP | RCIP | TXIP | SSPIP | CCP1IP | TMR2IP | TMR1IP | **(Note 4)** |
| PIR2 | OSCFIF | CMIF | — | EEIF | BCLIF | HLVDIF | TMR3IF | CCP2IF | **(Note 4)** |
| PIE2 | OSCFIE | CMIE | — | EEIE | BCLIE | HLVDIE | TMR3IE | CCP2IE | **(Note 4)** |
| IPR2 | OSCFIP | CMIP | — | EEIP | BCLIP | HLVDIP | TMR3IP | CCP2IP | **(Note 4)** |
| ADRESH | A/D Result Register High Byte | | | | | | | | **(Note 4)** |
| ADRESL | A/D Result Register Low Byte | | | | | | | | **(Note 4)** |
| ADCON0 | — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON | **(Note 4)** |
| ADCON1 | — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | **(Note 4)** |
| ADCON2 | ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 | **(Note 4)** |
| PORTA | RA7(2) | RA6(2) | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | **(Note 4)** |
| TRISA | TRISA7(2) | TRISA6(2) | PORTA Data Direction Control Register | | | | | | **(Note 4)** |
| PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | **(Note 4)** |
| TRISB | PORTB Data Direction Control Register | | | | | | | | **(Note 4)** |
| LATB | PORTB Data Latch Register (Read and Write to Data Latch) | | | | | | | | **(Note 4)** |
| PORTE(1) | — | — | — | — | RE3(3) | RE2 | RE1 | RE0 | **(Note 4)** |
| TRISE(1) | IBF | OBF | IBOV | PSPMODE | — | TRISE2 | TRISE1 | TRISE0 | **(Note 4)** |
| LATE(1) | — | — | — | — | — | PORTE Data Latch Register | | | **(Note 4)** |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers and/or bits are not implemented on PIC18F2423/2523 devices and are read as '0'.

**2:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**3:** RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

**4:** For these Reset values, see **Section 4.0 "Reset"** of the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).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## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to **Section 23.1 "Configuration Bits" in** the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631). Device ID information presented in this section is for the PIC18F2423/2523/4423/4523 devices only.

### 3.1 Device ID Registers

The Device ID registers are read-only registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

| File Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value |
|---|---|---|---|---|---|---|---|---|---|---|
| 3FFFFEh | DEVID1(1) | DEV3 | DEV2 | DEV1 | DEV0 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx(2) |
| 3FFFFFh | DEVID2(1) | DEV11 | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | xxxx xxxx(2) |

**Legend:** x = unknown, u = unchanged, — = unimplemented. Shaded cells are unimplemented, read as '0'.

**Note 1:** DEVID registers are read-only and cannot be programmed by the user.

**2:** See Register 3-1 and Register 3-2 for DEVID1 and DEVID2 values.

**REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2423/2523/4423/4523**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV3 | DEV2 | DEV1 | DEV0 | REV3 | REV2 | REV1 | REV0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Read-only bit | P = Programmable bit | U = Unimplemented bit, read as '0' |
| -n = Value when device is unprogrammed | | u = Unchanged from programmed state |

bit 7-4 **DEV<3:0>:** Device ID bits
1101 = PIC18F4423
1001 = PIC18F4523
0101 = PIC18F2423
0001 = PIC18F2523

bit 3-0 **REV<3:0>:** Revision ID bits
These bits are used to indicate the device revision.

**REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2423/2523/4423/4523**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV11(1) | DEV10(1) | DEV9(1) | DEV8(1) | DEV7(1) | DEV6(1) | DEV5(1) | DEV4(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Read-only bit | P = Programmable bit | U = Unimplemented bit, read as ‘0’ |
| -n = Value when device is unprogrammed | | u = Unchanged from programmed state |

bit 7-0 **DEV<11:4>:** Device ID bits(1)

These bits are used with the DEV<3:0> bits in Device ID Register 1 to identify the part number.

0001 0001 = PIC18F2423/2523 devices

0001 0000 = PIC18F4423/4523 devices

**Note 1:** These values for DEV<11:4> may be shared with other devices. The specific device is always identified by using the entire DEV<11:0> bit sequence.


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## 4.0 ELECTRICAL CHARACTERISTICS

**Note:** Other than some basic data, this section documents only the PIC18F2423/2523/4423/4523 devices' specifications that differ from those of the PIC18F2420/2520/4420/4520 devices. For detailed information on the electrical specifications shared by the PIC18F2423/2523/4423/4523 and PIC18F2420/2520/4420/4520 devices, see the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

### Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to $V_{SS}$ (except $V_{DD}$ and $\overline{MCLR}$) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +7.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ **(Note 2)** ..... 0V to +13.25V
Total power dissipation **(Note 1)** ..... 1.0W
Maximum current out of $V_{SS}$ pin ..... 300 mA
Maximum current into $V_{DD}$ pin ..... 250 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports ..... 200 mA

**Note 1:** Power dissipation is calculated as follows:
$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

**2:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$/$V_{PP}$/RE3 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$/$V_{PP}$/RE3 pin, rather than pulling this pin directly to $V_{SS}$.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 4-1: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**

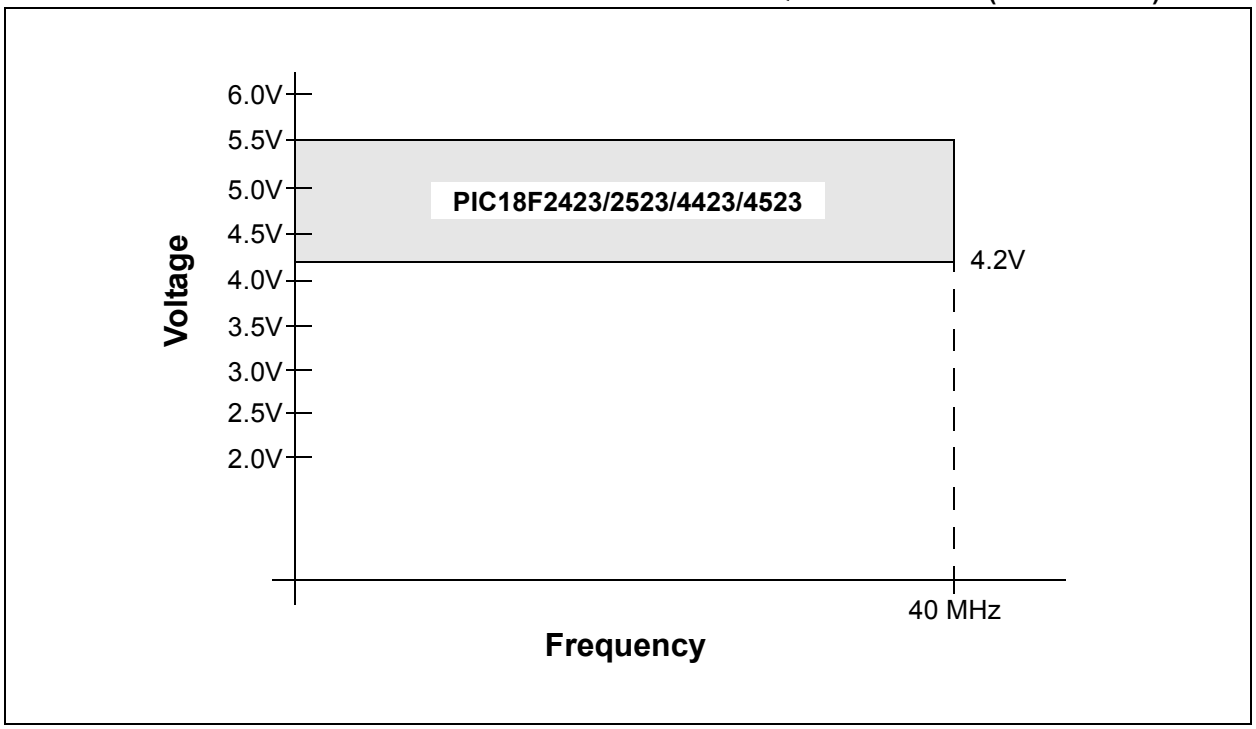


**FIGURE 4-2: PIC18F2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (EXTENDED)**

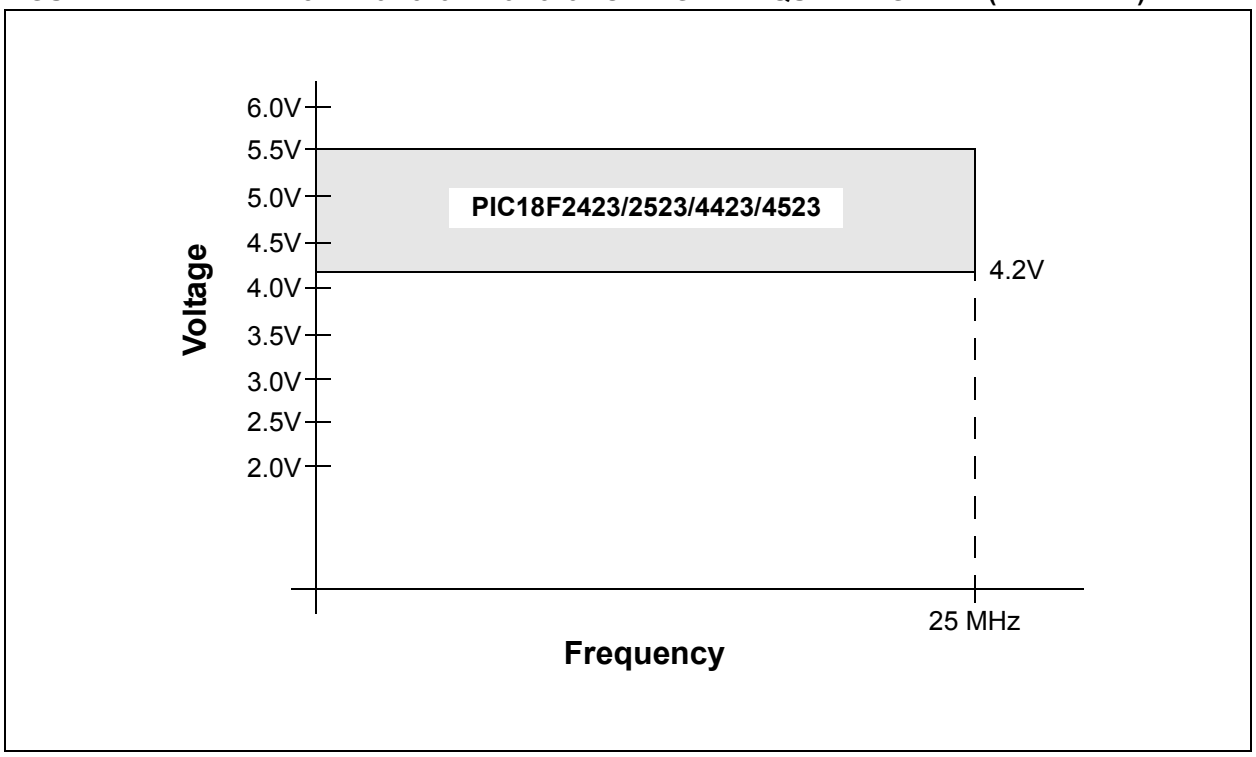



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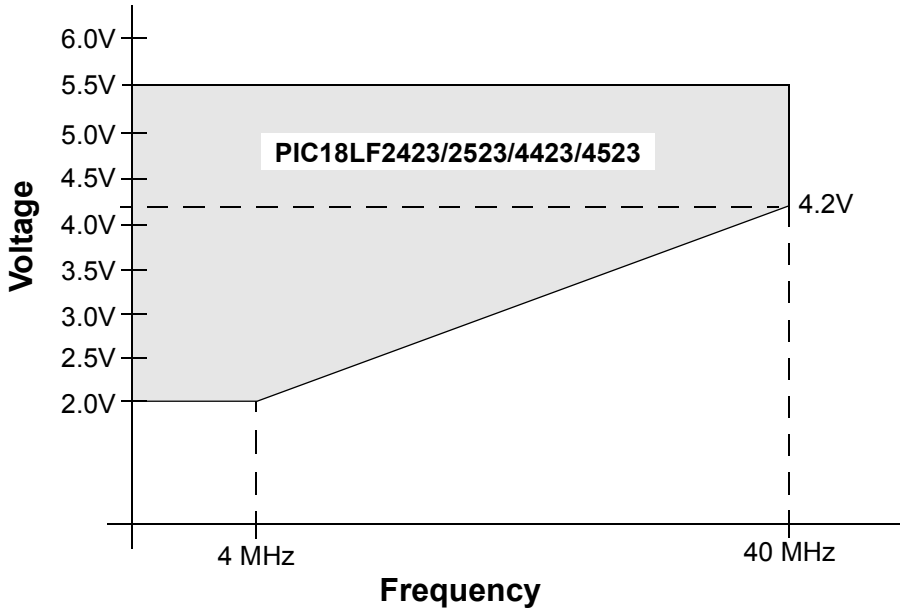
**FIGURE 4-3: PIC18LF2423/2523/4423/4523 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**




FMAX = (16.36 MHz/V) (VDDAPPMIN – 2.0V) + 4 MHz

**Note:** VDDAPPMIN is the minimum voltage of the PIC® device in the application.

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2423/2523/4423/4523 (INDUSTRIAL) PIC18LF2423/2523/4423/4523 (INDUSTRIAL)**

| Param No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | — | — | 12 | bit | | ΔVREF ≥ 3.0V |
| A03 | EIL | Integral Linearity Error | — | <±1 | ±2.0 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±2.0 | LSB | VDD = 5.0V | |
| A04 | EDL | Differential Linearity Error | — | <±1 | +1.5/-1.0 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | +1.5/-1.0 | LSB | VDD = 5.0V | |
| A06 | EOFF | Offset Error | — | <±1 | ±5 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±3 | LSB | VDD = 5.0V | |
| A07 | EGN | Gain Error | — | <±1 | ±1.25 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±2.00 | LSB | VDD = 5.0V | |
| A10 | — | Monotonicity | Guaranteed(1) | | | — | | VSS ≤ VAIN ≤ VREF |
| A20 | ΔVREF | Reference Voltage Range (VREFH – VREFL) | 3 | — | VDD – VSS | V | | For 12-bit resolution. |
| A21 | VREFH | Reference Voltage High | VSS + 3.0V | — | VDD + 0.3V | V | | For 12-bit resolution. |
| A22 | VREFL | Reference Voltage Low | VSS – 0.3V | — | VDD – 3.0V | V | | For 12-bit resolution. |
| A25 | VAIN | Analog Input Voltage | VREFL | — | VREFH | V | | |
| A30 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 2.5 | kΩ | | |
| A50 | IREF | VREF Input Current(2) | —<br>— | —<br>— | 5<br>150 | μA<br>μA | | During VAIN acquisition.<br>During A/D conversion cycle. |

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**2:** VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.


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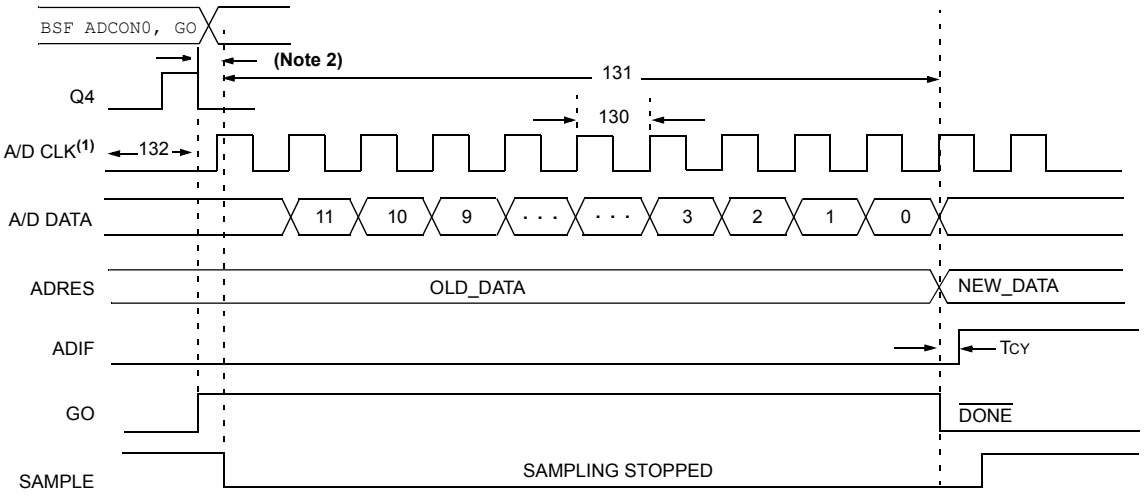
**FIGURE 4-4: A/D CONVERSION TIMING**




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

**2:** This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.

**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

| Param No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 130 | TAD | A/D Clock Period | PIC18**F**XXXX | 0.8 | 12.5(1) | µs | TOSC based, VREF ≥ 3.0V |
| | | | PIC18**LF**XXXX | 1.4 | 25.0(1) | µs | VDD = 3.0V; TOSC based, VREF full range |
| | | | PIC18**F**XXXX | — | 1 | µs | A/D RC mode |
| | | | PIC18**LF**XXXX | — | 3 | µs | VDD = 3.0V; A/D RC mode |
| 131 | TCNV | Conversion Time (not including acquisition time)(2) | | 13 | 14 | TAD | |
| 132 | TACQ | Acquisition Time(3) | | 1.4 | — | µs | |
| 135 | TSWC | Switching Time from Convert → Sample | | — | **(Note 4)** | | |
| 137 | TDIS | Discharge Time | | 0.2 | — | µs | |

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**2:** ADRES registers may be read on the following TCY cycle.

**3:** The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (RS) on the input channels is 50Ω.

**4:** On the following cycle of the device clock.

**NOTES:**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## 5.0 PACKAGING INFORMATION

For packaging information, see **Section 28.0 "Packaging Information"** in the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631).

**NOTES:**


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## APPENDIX A: REVISION HISTORY

### Revision A (June 2006)

Original data sheet for PIC18F2423/2523/4423/4523 devices.

### Revision B (January 2007)

This revision includes updates to the packaging diagrams.

### Revision C (September 2009)

Electrical specifications updated. Preliminary condition status removed. Converted document to the “mini data sheet” format.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

| Features | PIC18F2423 | PIC18F2523 | PIC18F4423 | PIC18F4523 |
|---|---|---|---|---|
| Program Memory (Bytes) | 16384 | 32768 | 16384 | 32768 |
| Program Memory (Instructions) | 8192 | 16384 | 8192 | 16384 |
| Interrupt Sources | 19 | 19 | 20 | 20 |
| I/O Ports | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, D, E | Ports A, B, C, D, E |
| Capture/Compare/PWM Modules | 2 | 2 | 1 | 1 |
| Enhanced Capture/Compare/PWM Modules | 0 | 0 | 1 | 1 |
| Parallel Communications (PSP) | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 10 Input Channels | 10 Input Channels | 13 Input Channels | 13 Input Channels |
| Packages | 28-Pin PDIP<br>28-Pin SOIC<br>28-Pin QFN | 28-Pin PDIP<br>28-Pin SOIC<br>28-Pin QFN | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN |

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**


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## APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

## APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration*". This Application Note is available as Literature Number DS00726.

**NOTES:**


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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| Device | PIC18F2423(1), PIC18F2523(1), PIC18F4423T(2), PIC18F4523T(2); VDD range 4.2V to 5.5V<br>PIC18F2423(1), PIC18F2523(1), PIC18F4423T(2), PIC18F4523T(2); VDD range 2.0V to 5.5V |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| Package | PT = TQFP (Thin Quad Flat pack)<br>ML = QFN<br>SO = SOIC<br>SP = Skinny Plastic DIP<br>P = PDIP |
| Pattern | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) PIC18F4523-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18F4523-I/PT = Industrial temp., TQFP package, Extended VDD limits.

c) PIC18F4523-E/P = Extended temp., PDIP package, normal VDD limits.

**Note 1:** F = Standard Voltage Range
LF = Wide Voltage Range

**2:** T = In tape and reel PLCC, and TQFP packages only.

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03/26/09


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# OCEAN CHIPS
## Океан Электроники
## Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

**«JONHON»** (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

**«FORSTAR»** (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

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